Clock splitting to reduce power consumption in RISC-V cores

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Abstract **- RISC-V is an open source instruction set architecture (ISA) for various application scenarios. A multi-core RISC processor might not always use all its core, thus the power in such cases can be reduced by splitting clock and supplying them to each core. This method can be used to disable the clock to unused core which reduces the overall power consumption, reducing heat and thereby increasing the performance of the core in use.**

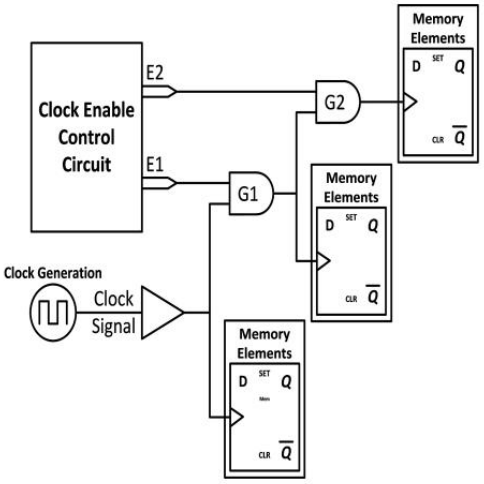
I. Introduction

Clock is the heartbeat of any microprocessor system, which is responsible for synchronization and timing of actions in the system. Even if the system is not performing any significant operation it consumes some dynamic power due to clock switching. This power loss can be reduced by disabling the clock to the system when it is not in use.

II. Improvements

The suggested improvement is to split clock and provide a control to enable and disable the clock to its corresponding system. This method is not only effective in multi-core systems but also in microcontrollers with multiple peripherals such as DAC, ADC, Op-Amp, etc. where the clock to the unused peripheral can be disabled thus reducing the power consumption and load on the clock which can result in increased performance.

Figure 1. Clock gating scheme
Adapted from Hsu & Lin, 2011.



III. Conclusion

The splitting of clock and adding controls may result in increased gate count but when put to use in a right way can result in significant improvement in the performance and reduce the power consumption.

References

[1] Arsalan Shahid, Saad Arif, Muhammad Yasir Qadri, UK Saba Munawar, "Power Optimization Using Clock Gating and Power Gating: A Review", July 2016.