

VLSI Lab 2
University of Bristol, UK

Roshan Thomas

0.1 Exercise 4.1: Designing a NAND3 gate

0.1.1 Part 3

The schematic for the NAND3 Layout,

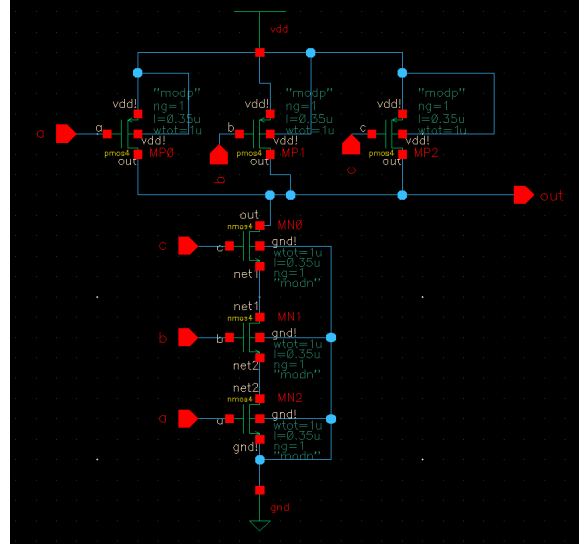


Figure 1: Schematic for the NAND3 Gate.

The layout for the NAND3 gate,

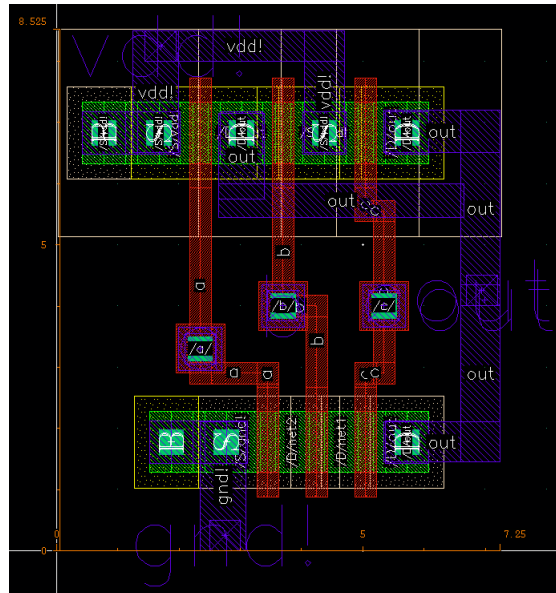


Figure 2: Layout for the NAND3 Gate.

The DRC and LVS checks passed without any errors, and can be seen in the figures below.

```
Host is
cmd is /eda/cadence/2022-23/RHELx86/ASSURA_04.16.113.618/tools.lnx86/assura/bin/assura /home/oj23092/VLSI_Design_Lab/ASSURA_DRC/NAND3/
NAND3.rsf -cdslib /home/oj23092/VLSI_Design_Lab/cds.lib -restart -gui
Starting the Assura DRC Run: IPC id ipc:31: pid 870000.
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
*WARNING* No DRC errors found.
```

Figure 3: DRC checker passed with no errors.

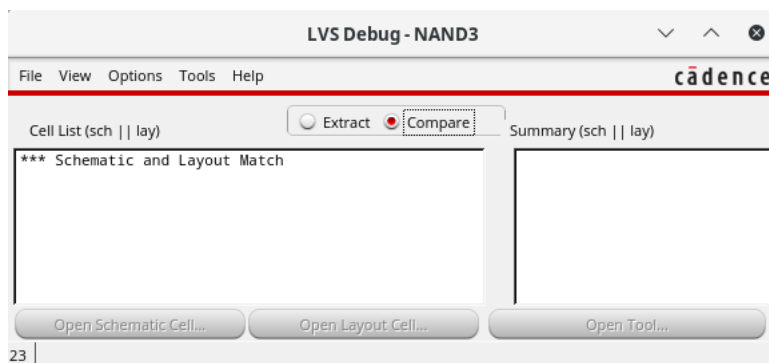


Figure 4: Schematic match for the LVS Checker.

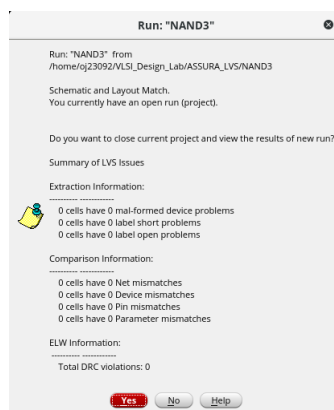


Figure 5: LVS Checker passed with no errors.

0.1.2 Part 4

The test-bench schematic for the NAND3 gate to test the response of the system to various inputs,

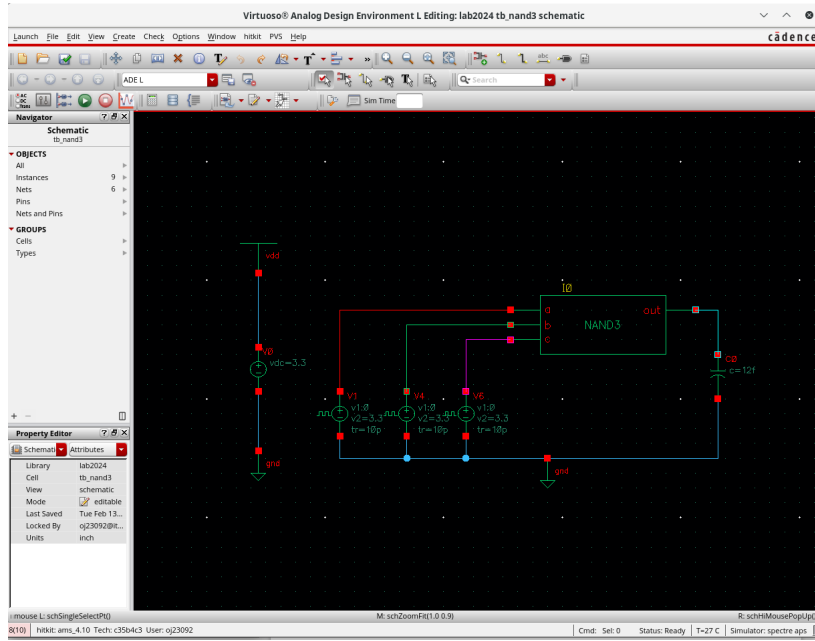


Figure 6: Test-bench for the NAND3 Gate.

The output waveform for the three input waveforms are shown below, where the input a is given by net3, input b is given by net2, input c is given by net1, and the output is given by net4 in Figure 7.

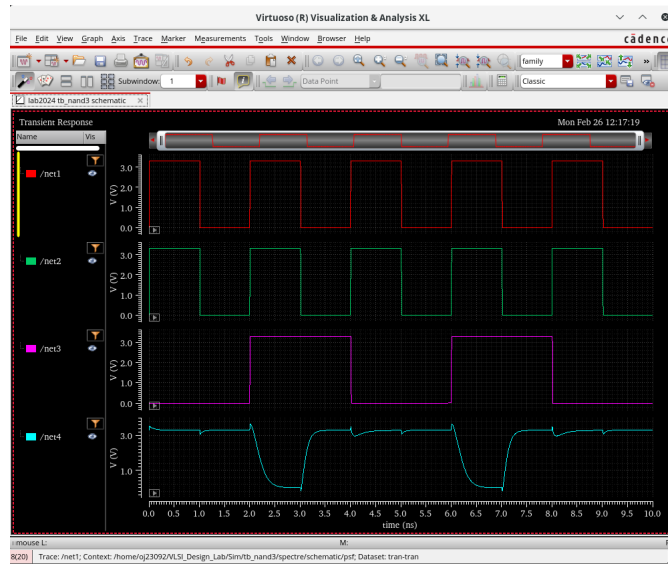


Figure 7: Input and Output Waveforms for the NAND3 Gate.

0.1.3 Part 5

The dimensions for the NAND3 layout are,

- Minimum Cell Width: $7.25\ \mu m$
- Minimum Cell Height: $8.525\ \mu m$
- Minimum Cell Area: $61.806\ \mu m^2$