VLSI Lab 1
University of Bristol, UK

Roshan Thomas

0.1 Exercise 3.1: Calculate the Equivalent Resistance of Minimum sized Transistors

0.1.1 Part 1

The delay values from the 50% point of the input waveform (t_{pd_LH}) and the output waveform (t_{pd_HL}) are given in the Table below. The value for t_{pd_LH} is calculated by subtracting the time delay when the input is going from the highest voltage point to the lowest voltage point, and the output is performing the opposite action. Similarly, t_{pd_HL} is calculated by subtracting the time it takes for the input to go from the lowest voltage point to the highest voltage point, and the output goes from the highest voltage point to the lowest.

Input	Output	t_{pd_LH}	t_{pd_HL}
low-high	high-low	N/A	0.07757 ns
high-low	low-high	0.0907 ns	N/A

Table 1: Delay values for the input and output waveforms

The W/L ratios for the PMOS and NMOS FETs used were $2\mu m/0.35\mu m$ and $1\mu m/0.35\mu m$ respectively, and the load capacitance was 12 fF.

Figure 1 shows the input (red) and the output (green) waveforms, with the 50% delay values marked at 1.65 V.

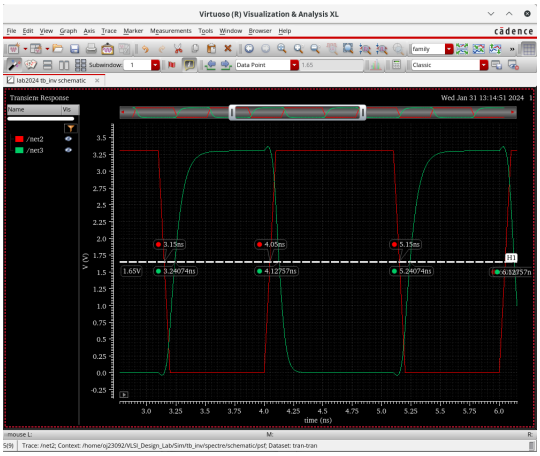

Figure 1: Input and Output Waveforms of Inverter.

0.1.2 Part 2

The circuit shown in Figure 2 shows the switch/resistor model for the inverter where the transistor resistance R_p, load capacitance C_L, switch, and voltage source V_{dd} is shown. In the charging cycle, the NMOS acts as an open circuit (open switch), and the PMOS is seen by the circuit as a resistance modelled by R_p.

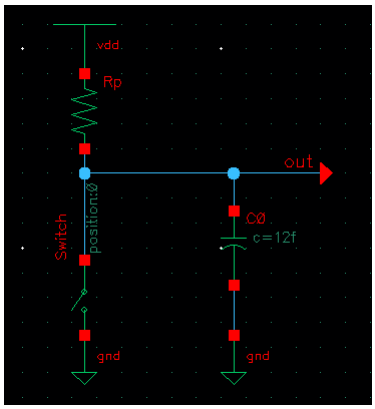

Figure 2: Symbolic Circuit Diagram of Switch/Resistor model of Inverter in the Charging Cycle.

0.1.3 Part 3

The expression for the output voltage across the load capacitor can be written as,

$$V_{\text{out}} = V_{DD}\left(1 - \exp\left(-\frac{t_{pd\_LH}}{R_p C_L}\right)\right) \tag{1}$$

Considering 50% delay,

$$V_{\text{out}} = V_{DD} \tag{2}$$

Equating (2) to (1),

$$0.5V_{DD} = V_{DD}\left(1 - \exp\left(-\frac{t_{pd\_LH}}{R_p C_L}\right)\right) \tag{3}$$

$$0.5 = 1 - \exp\left(-\frac{t_{pd\_LH}}{R_p C_L}\right) \tag{4}$$

$$0.5 = \exp\left(-\frac{t_{pd\_LH}}{R_p C_L}\right) \tag{5}$$

$$-\frac{t_{pd\_LH}}{R_p C_L} = \log(0.5) \tag{6}$$

$$-\frac{t_{pd\_LH}}{R_p C_L} = -0.69 \tag{7}$$

The resistance R_p in terms of the delay,

$$\boxed{R_p = \frac{t_{pd\_LH}}{0.69 \cdot C_L}} \tag{8}$$

Based on the delay observed in the previous parts with $t_{pd\_LH} = 0.0907\,ns$ and $C_L = 12\,fF$, the resistance R_p,

$$R_p = \frac{0.0907 \times 10^{-9}}{0.69 \times 12 \times 10^{-15}} = 10.9541\,k\Omega \approx 11\,k\Omega \tag{9}$$

0.1.4 Part 4

The resistance for a PMOS transistor can be calculated using (10),

$$R_p = R_{p,\,\min} \times \frac{W_{\min}}{W} \times \frac{L}{L_{\min}} \tag{10}$$

Rearranging the equation to get the minimum resistance for the transistor,

$$R_{p,\,\min} = R_p \times \frac{W}{W_{\min}} \times \frac{L_{\min}}{L} \tag{11}$$

Inserting the values for R_p and a minimum-sized PMOS transistor with $W/L = 1\mu m/0.35\mu m$,

$$R_{p,\,\min} = 10954.1\Omega \times \frac{1\mu m}{1\mu m} \times \frac{0.35\mu m}{0.35\mu m} = 10.9541\,k\Omega \approx 11\,k\Omega \tag{12}$$

Simulating the inverter for a minimum-sized PMOS transistor, the delay values for the input and output waveforms are,

Input	Output	t_{pd_LH}	t_{pd_HL}
low-high	high-low	N/A	0.06953 ns
high-low	low-high	0.15645 ns	N/A

Table 2: Delay values for the input and output waveforms, for the minimum-sized transistor.

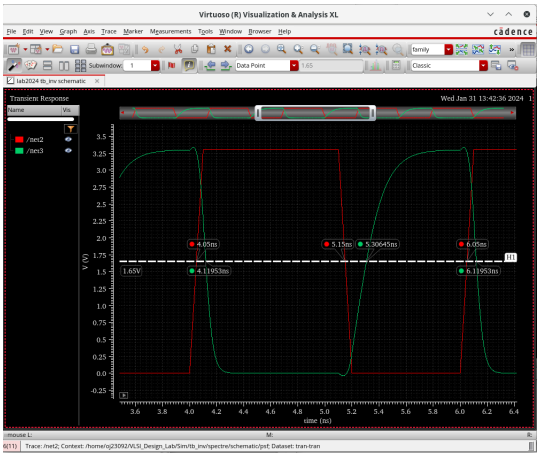

Figure 3: Input and Output Waveforms of Minimum-Sized Inverter.

The resistance R_p can be calculated as,

$$R_p = \frac{t_{pd\_LH}}{0.69 \cdot C_L} = \frac{0.15645 \times 10^{-9}}{0.69 \times 12 \times 10^{-15}} = 18.895\,k\Omega \tag{13}$$

$$R_{p,\,\min} = R_p = 18.895\,k\Omega \tag{14}$$

The analytical value and the simulated value of R_p has a discrepancy of about $7\,k\Omega$ which could be explained by the fact that a simplistic model using a resistor and switch is considered in the analytical calculation, whereas the simulated value by Cadence considers all the linear and non-linear effects in a FET, which adds to the resistance that is seen by the circuit.

0.1.5 Part 5

In the discharging cycle, the inverter is modelled as a switch/resistor model, where the PMOS is seen as open circuit (open switch), and the NMOS is seen as a resistor by the circuit, modelled by the resistance R_n. The load is seen as the capacitor C_L. Figure 4 shows the symbolic circuit diagram of the discharging cycle.

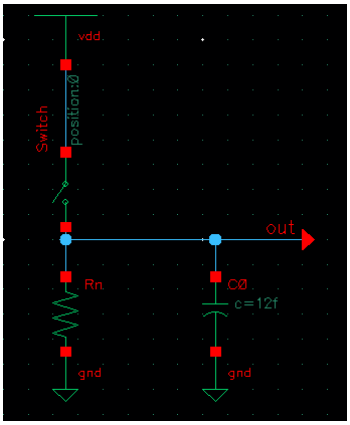

Figure 4: Symbolic Circuit Diagram of Switch/Resistor model of Inverter in the Discharging Cycle.

For the discharging cycle,

$$V_{\text{out}} = V_{DD} \exp\left(-\frac{t_{pd\_HL}}{R_n C_L}\right) \tag{15}$$

Considering 50% delay,

$$0.5V_{DD} = V_{DD} \exp\left(-\frac{t_{pd\_HL}}{R_n C_L}\right) \tag{16}$$

$$\boxed{R_n = \frac{t_{pd\_HL}}{0.6 \cdot C_L}} \tag{17}$$

Inserting the simulated values from Part 1 into (17),

$$R_n = \frac{0.07757 \times 10^{-9}}{0.69 \times 12 \times 10^{-15}} = 9.368\,k\Omega \tag{18}$$

The minimum resistance $R_{\text{n, min}}$,

$$R_{\text{n, min}} = 9.368\,k\Omega \tag{19}$$

0.2 Exercise 3.2: Calculating the Effect of Transistor Sizing

0.2.1 Part 1

The inverter is driving a load (capacitance) of 25 fF with a maximum 50% delay of 100 ps, for both the rising and falling edges.

Calculating the W/L required for the PMOS,

$$R_p = \frac{100 \times 10^{-12}}{0.69 \times 25 \times 10^{-15}} = 5797.1\Omega \tag{20}$$

The simulation result for the minimum PMOS resistance,

$$R_{\text{p, min}} = 18894.93\Omega \tag{21}$$

The required W/L can be calculated as

$$R_p = R_{\text{p, min}} \times \frac{W_{\text{min}}}{W} \times \frac{L}{L_{\text{min}}} \tag{22}$$

$$\frac{W}{L} = \frac{R_{\text{p, min}}}{R_p} \times \frac{W_{\text{min}}}{L_{\text{min}}} = \frac{18894.93}{5797.1} \times \frac{1}{0.35} \tag{23}$$

$$\frac{W}{L} = \frac{3.259\mu m}{0.35\mu m} \tag{24}$$

The required W/L for the NMOS can be calculated similarly,

$$R_n = \frac{100 * 10^{-12}}{0.69 \times 25 \times 10^{-15}} = 5797.1\Omega \tag{25}$$

$$R_{\text{n, min}} = 9368.36\Omega \tag{26}$$

$$\frac{W}{L} = \frac{R_{\text{n, min}}}{R_n} \times \frac{W_{\text{min}}}{L_{\text{min}}} = \frac{9368.36}{5797.1} \times \frac{1}{0.35} \tag{27}$$

$$\frac{W}{L} = \frac{1.61\mu m}{0.35\mu m} \tag{28}$$

0.2.2 Part 2

Using the W/L values for the PMOS and NMOS FETs, the delay for the rising and falling edges are shown below,

Input	Output	t_{pd_LH}	t_{pd_HL}
low-high	high-low	N/A	0.08802 ns
high-low	low-high	0.1028 ns ns	N/A

Table 3: Delay values for the input and output waveforms

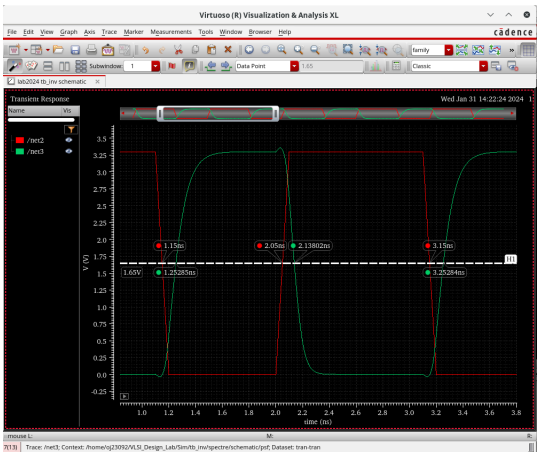

Figure 5: Input and Output Waveforms of Inverter.

Figure 5 shows the rising and falling edges where the red signal is the input, and the green signal is the output. As can be seen in Table 3 the simulated values for the rising and falling edges are 102.8 ps and 88.02 ps respectively, which is close to the required value of 100 ps.

There are deviations of $\pm 2\,ps$ with the calculated values and the simulated values. These values although minor can be attributed to the parasitic capacitances that have not been considered in the simplistic switch/resistor model. The circuit assumes a load having linear capacitance, but in reality the capacitances behave non-linearly. Also, parasitic capacitances in the wiring have not been accounted for which can cause the delay in the rising and falling times.

The accuracy of the switch/resistor model can be improved by accounting for the parasitic capacitances. Since the circuit uses multiple layers for the wiring to be established, as the wires cant be too close to the FETs because of its interference, the multiple layers of material causes parasitic capacitances which are not accounted for in the simplistic switch/resistor model. To account for these capacitances, capacitors can be added in parallel to the resistor.

Figure 6 shows the new circuit with the improvement where the capacitances C_1 and C_2 are the parasitic capacitances, and C_3 is the load capacitance. In a similar fashion, the circuit for the discharging cycle of the inverter can be created.

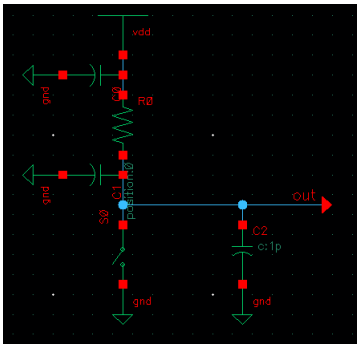

Figure 6: Symbolic Circuit Diagram of the Improved Switch/Resistor model of Inverter in the Charging Cycle.