

# ELE 231 LINEAR AND DIGITAL INTEGRATED CIRCUITS

Reference books

- Fundamentals of digital circuits by Amantha Kumar
- Digital logic and computer design by M Morris Mano
- Modern digital electronics by R.P. Jain
- Digital fundamentals by J.L. Floyd

## NUMBER SYSTEMS, LOGIC GATES AND BOOLEAN ALGEBRA

Electronic circuits are of two types analog and digital systems

Analog systems deals with voltage or current values which changes continuously with time. These systems produce noise.

Digital systems

advantages → Reduced noise i.e. eliminated, reliable, versatile, cheap, only two values are permitted 0 or 1, accuracy is more, storage

There are 4 types of Number Systems

① Decimal → 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 → 10 characters → Eg: (25.35)10

② Binary → 0, 1 → 2 characters → Eg: (10.10)2

③ Octal → 0, 1, 2, 3, 4, 5, 6, 7 → 8 characters → Eg: (35.13)8

④ Hexadecimal → 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F → 16 characters

→ Eg: (35.A)16, 35.A2 H  
Integer ↓ Fractional

Conversion of Numbers from one system to another systems

① 56.105

② 128.892

$$\begin{array}{r}
 2 | 56 & 0.105 \times 2 = 0.21 \\
 2 | 28 - 0 & 0.21 \times 2 = 0.42 \\
 2 | 14 - 0 & 0.42 \times 2 = 0.84 \\
 2 | 7 - 0 & 0.84 \times 2 = 1.68 \\
 2 | 3 - 1 & 0.68 \times 2 = 1.36 \\
 1 - 1 & 0.36 \times 2 = 0.72
 \end{array}$$

$$\begin{array}{r}
 8 | 128 & 0.892 \times 8 = 7.136 \\
 8 | 16 - 0 & 0.136 \times 8 = 1.088 \\
 8 | 2 - 0 & 0.088 \times 8 = 0.704 \\
 & 0.704 \times 8 = 5.632 \\
 & 0.632 \times 8 = 5.056 \\
 & 0.056 \times 8 = 0.448
 \end{array}$$

$$56.105 = (111000.000110)_2$$

$$= (70.06)_8$$

$$= (38.18)_{16}$$

$$128.892 = (200.710550)_8$$

$$= (01000000.11001001011010)_2$$

$$= (80.E45A)_{16}$$

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papergrid

③ 235.12

$$\begin{array}{r}
 8 | 235 \\
 8 | 29 - 3 \\
 3 - 5 \\
 0.12 \times 8 = 0.96 \\
 0.96 \times 8 = 7.68 \\
 0.68 \times 8 = 5.44 \\
 0.44 \times 8 = 3.52 \\
 0.52 \times 8 = 4.16 \\
 0.16 \times 8 = 1.28
 \end{array}$$

④ 560.31

$$\begin{array}{r}
 8 | 560 \\
 8 | 70 - 0 \\
 8 | 8 - 6 \\
 1 - 0 \\
 0.31 \times 8 = 2.48 \\
 0.48 \times 8 = 3.84 \\
 0.84 \times 8 = 6.72 \\
 0.72 \times 8 = 5.76 \\
 0.76 \times 8 = 6.08 \\
 0.08 \times 8 = 0.64
 \end{array}$$

$$235.12 = (3.53.075341)_8$$

$$560.31 = (1060.236560)_8$$

⑤ 360.35

$$\begin{array}{r}
 2 | 360 \\
 2 | 180 - 0 \\
 2 | 60 - 0 \\
 2 | 30 - 0 \\
 2 | 15 - 0 \\
 2 | 7 - 1 \\
 2 | 3 - 1 \\
 1 - 1
 \end{array}
 \begin{array}{l}
 0.35 \times 2 = 0.70 \\
 0.70 \times 2 = 1.40 \\
 0.40 \times 2 = 0.80 \\
 0.80 \times 2 = 1.60 \\
 0.60 \times 2 = 1.20 \\
 0.20 \times 2 = 0.40
 \end{array}$$

⑥ 76.825

$$\begin{array}{r}
 2 | 76 \\
 2 | 38 - 0 \\
 2 | 19 - 0 \\
 2 | 9 - 1 \\
 2 | 4 - 1 \\
 2 | 2 - 0 \\
 1 - 0
 \end{array}
 \begin{array}{l}
 0.825 \times 2 = 1.650 \\
 0.650 \times 2 = 1.300 \\
 0.300 \times 2 = 0.600 \\
 0.600 \times 2 = 1.200 \\
 0.200 \times 2 = 0.400 \\
 0.400 \times 2 = 0.800
 \end{array}$$

$$360.35 = (1110000.010110)_2$$

$$76.825 = (1001100.110100)_2$$

⑦ 2598.675

$$\begin{array}{r}
 16 | 2598 \\
 16 | 162 - 6 \\
 16 | 10 - 2 \\
 0.675 \times 16 = 10.800 \\
 0.8 \times 16 = 12.8 \\
 0.8 \times 16 = 12.8 \\
 0.8 \times 16 = 12.8
 \end{array}$$

$$2598.675 = (26.ACCC)_16$$

$$(101000100110.1010110011001100)_2$$

$$(5046.53146)_8$$

⑧ (4526.128)<sub>8</sub><sup>3</sup>

$$(100101010110.001010011)_2$$

$$(956.298)<sub>16</sub>$$

⑨ (001001001101110)<sub>2</sub>

$$(111.56)_8$$

$$(49.B8)<sub>16</sub>$$

⑩ 001100111101.101101101

$$(33D.B68)<sub>16</sub>$$

$$(11,75.555)_8$$

⑪ 89AB.C65 DF 14

$$(1000100110101011.110001100101101111)_2$$

$$(104653.6145676)_8$$

## Binary Arithmetic

### Laws of Binary addition

$$1+1 = 0 \quad \text{sum} \quad \text{carry}$$

$$1+0 = 1 \quad 0$$

$$0+1 = 1 \quad 0$$

$$0+0 = 0 \quad 0$$

## Binary Subtraction

### Laws of Binary Subtraction

$$1-1 = 0$$

$$1-0 = 1$$

$$0-1 = 1$$

$$0-0 = 0$$

$$\begin{array}{r} 1111 \\ 101101.1010 \end{array}$$

$$+\begin{array}{r} 110101.1000 \end{array}$$

$$\begin{array}{r} 1100011.0010 \\ \hline \end{array}$$

$$110110.110$$

$$-\begin{array}{r} 10101.101 \end{array}$$

$$\begin{array}{r} 100001.001 \end{array}$$

$$36.12$$

$$15.5$$

$$11.7$$

### Sign magnitude representation.

$$+12$$

$$-10$$

$$01100$$

+ sign magnitude.

### 2's complement method of subtraction

$$110111$$

$$1's \text{ comp} + 001000$$

$$\begin{array}{r} 110111 \\ + 001000 \\ \hline 111111 \end{array}$$

$$2's \text{ comp} \quad 001001$$

$$2's \text{ comp} \quad 00100000.00110$$

$$101111.11001$$

$$00100000.00110$$

$$0011$$

$$1101$$

### perform subtraction using 2's complement

$$1) 15 - 8$$

$$11001010$$

$$2) \cancel{25} - 12 - 15 = -3$$

$$1111$$

$$1000$$

$$110111$$

$$2's \text{ comp} \quad 1000$$

$$0111 = 7$$

$$00111111$$

$$00111111$$

$$00111111$$

$$00111111$$

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## ① Subtraction of a smaller no. from a larger no.

determine the 2's complement of the subtrahend

Add the 2's complement to the minuend

There is always a carry generated neglect the carry the answer is going to be the magnitude of the quantity

$$\begin{array}{r}
 14 - 28 \\
 00001010 \\
 00011100 \\
 11100010 \\
 +1 \\
 \hline
 11100100 \\
 00001101 \\
 \hline
 00001110 = -14
 \end{array}$$

## ② Subtraction of a larger no. from smaller no.

Determine the 2's complement of the larger number

Add the 2's complement to the smaller number (minuend)

There is no carry generated

The answer is going to be -ve

In order to get the 2's complement of the result

(a)  $34 - 22$

$$\begin{array}{r}
 00100010 \\
 00010010 \\
 11101001 \rightarrow 1's \\
 +1 \\
 \hline
 11101000 \rightarrow 2's
 \end{array}$$

$\overline{00100010}$

$\overline{11101010}$

$\overline{100001100}$

$\Rightarrow 1412$

(b)  $54 - 68$

$$\begin{array}{r}
 00110110 \\
 01000100 \\
 10111011 \\
 +1 \\
 \hline
 2's \quad 10111100
 \end{array}$$

$\overline{00110110}$

$\overline{10111100}$

$\overline{11110010} \Rightarrow 11110010$

$\overline{00000110} \quad 00000110$

$\overline{1110} \quad 00000110$

$\overline{11100110} \quad 14$

$\overline{01110010} \quad 14$



## Binary Coded Decimal

perform the following operation using 2's complement

①  $66.56 - 43.51$

010000010.1000111110000000

00101011.10000000

11010100.011111

+1

11010100.1000000

+01000010.100011

110010111.0000011

23.04

②  $15.32 - 29.54$

00001111.010100

00011101.100010

11100010.011101

11100010.011110

00001111.010100

11110001.110010

00001110.001101

1110.001110

+1

$0.32 \times 2 = 0.64$

$0.64 \times 2 = 1.28$

$0.28 \times 2 = 0.56$

$0.56 \times 2 = 1.12$

$0.12 \times 2 = 0.24$

$0.24 \times 2 = 0.48$

$0.48 \times 2 = 0.96$

$0.96 \times 2 = 1.92$

$0.56 \times 2 = 1.12$

$0.12 \times 2 = 0.24$

$0.24 \times 2 = 0.48$

$0.48 \times 2 = 0.96$

$0.96 \times 2 = 1.92$

$0.56 \times 2 = 1.12$

$0.12 \times 2 = 0.24$

$0.24 \times 2 = 0.48$

$0.48 \times 2 = 0.96$

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$0.56 \times 2 = 1.12$

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$0.48 \times 2 = 0.96$

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$0.56 \times 2 = 1.12$

$0.12 \times 2 = 0.24$

$0.24 \times 2 = 0.48$

$0.48 \times 2 = 0.96$

③  $-42 + 18.35$

011011.000000  $\rightarrow$  010110.0000  $\rightarrow$  1's of 42

010010.010110

010110.000000

~~010010.010110~~

101000.010110

## Logic gates and boolean algebra

Basic logic gates

OR gate

It is an electronic circuit in which the o/p is (high state) if any one of the i/p is at high state.

The symbol & truth table are as follows

IC 7432

$$Y = A + B$$

A

B

$$\begin{array}{ccc} A & B & Y \\ \hline 0 & 0 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \end{array}$$

$$\begin{array}{ccc} & & \text{Voltage} \\ \hline 0 & 0 & 0 \\ 0 & 1 & 4.3 \\ 1 & 0 & 4.3 \\ 1 & 1 & V_{DD} \end{array}$$

$$\begin{array}{ccc} & & \text{Voltage} \\ \hline 0 & 0 & 0 \\ 0 & 1 & 4.3 \\ 1 & 0 & 4.3 \\ 1 & 1 & V_{DD} \end{array}$$

$$\begin{array}{ccc} & & \text{Voltage} \\ \hline 0 & 0 & 0 \\ 0 & 1 & 4.3 \\ 1 & 0 & 4.3 \\ 1 & 1 & V_{DD} \end{array}$$

$$\begin{array}{ccc} & & \text{Voltage} \\ \hline 0 & 0 & 0 \\ 0 & 1 & 4.3 \\ 1 & 0 & 4.3 \\ 1 & 1 & V_{DD} \end{array}$$

$$\begin{array}{ccc} & & \text{Voltage} \\ \hline 0 & 0 & 0 \\ 0 & 1 & 4.3 \\ 1 & 0 & 4.3 \\ 1 & 1 & V_{DD} \end{array}$$

Draw truth table and symbol of 3 i/p orgate.

Symbol



$$Y = A + B + C$$

$$\begin{array}{cccc} & A & B & C \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}$$

$$\begin{array}{cccc} & A & B & C \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}$$

$$\begin{array}{cccc} & A & B & C \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}$$

$$\begin{array}{cccc} & A & B & C \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}$$

$$\begin{array}{cccc} & A & B & C \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}$$

$$\begin{array}{cccc} & A & B & C \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}$$

$$\begin{array}{cccc} & A & B & C \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}$$

$$\begin{array}{cccc} & A & B & C \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}$$

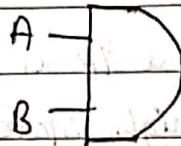
$$\begin{array}{cccc} & A & B & C \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{array}$$

electronic circuit

electrical circuit

AND late

It is an electronic circuit in which the o/p is high state if and only if both the inputs are in high state. The symbol & truth table is as follows



$Y = A \cdot B$  es función de  $A$ ,  $B$  y  $Y$  es  $V$

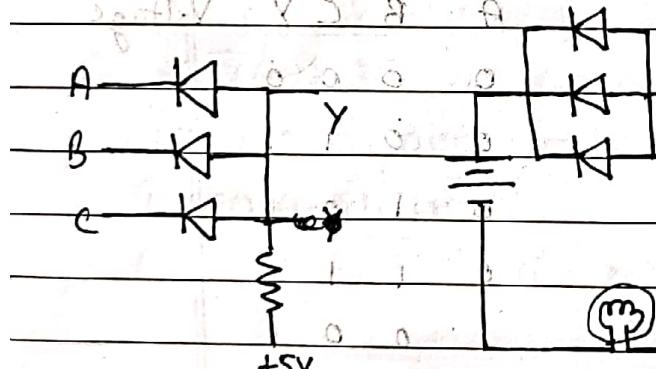
The diagram illustrates a series connection of two half-bridge converters. Each converter consists of an input terminal (A or B), a diode, and an inductor. The outputs of the two converters are connected in series. One output is connected to ground, and the other output is connected to a +5V source.

## Truth table & Symbol of 3 3/p AND Gate



$$Y = A \cdot B \cdot C$$

A B C Y



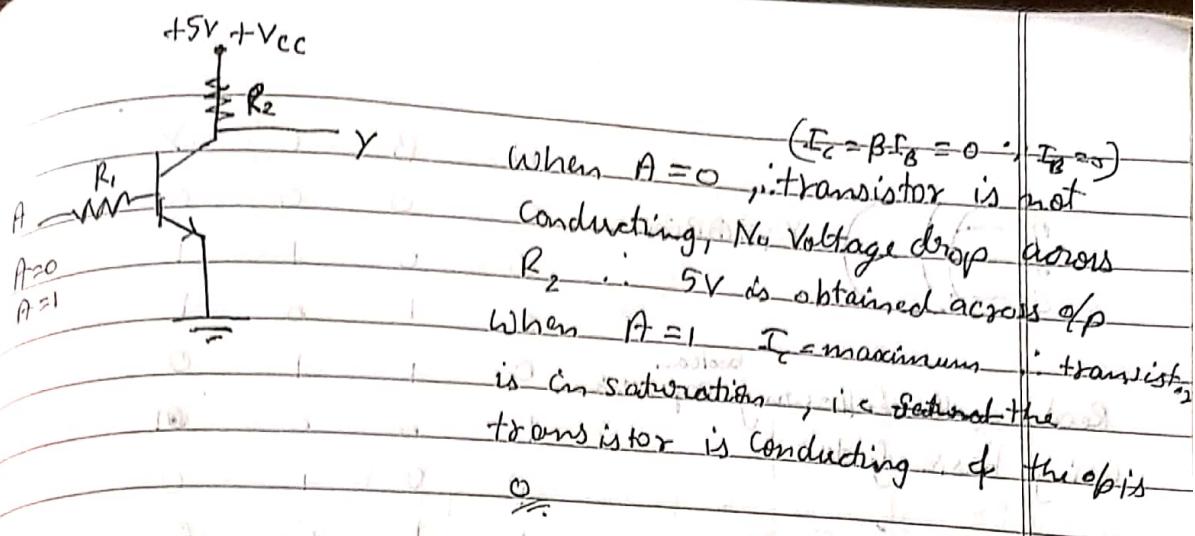
0	0	1	100
0	0	1	100
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Not late

It is an electronic circuit in which the o/p is always the opposite of the input i.e if  $\theta/p = 0$  o/p = 1 & if  $\theta/p = 0$  o/p = 1

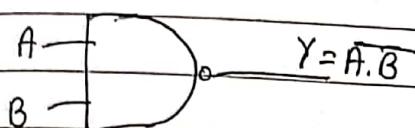


A B Y Voltage  
1 0 0.7  
0 1 5V



NAND gate

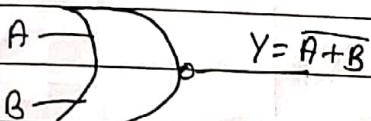
AND gate + NOT gate.



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate (Invertor + AND gate)

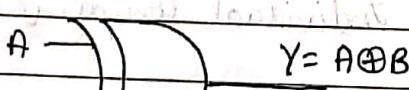
OR gate + NOT gate.



A B Y

0	0	1
0	1	0
1	0	0
1	1	0

Exclusive OR gate (XOR)



$$Y = A \oplus B$$

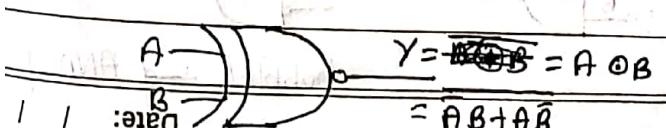
$$= \bar{A}B + A\bar{B}$$

A B Y

0	0	0
0	1	1
1	0	1
1	1	0

an electronic circuit in which the o/p is 1 when odd No of o/p's are in high state

Exclusive NOR gate (XNOR)



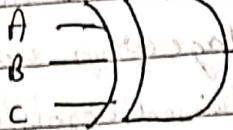
$$Y = \overline{A \oplus B} = A \odot B$$

$$= \bar{A}B + A\bar{B}$$

A B Y

0	0	1
0	1	0
1	0	0
1	1	1

papergrid



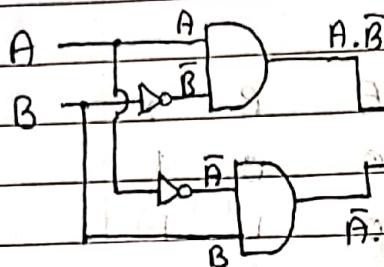
$$Y = A \oplus B \oplus C$$

A      B      C      Y

0	0	0	0
0	0	1	1
0	1	0	1
1	1	1	0
0	0	0	0
0	1	0	0
1	1	0	0

Realise the following expression using basic gates.

$$A \oplus B \text{ or } A \cdot \bar{B} + \bar{A} \cdot B$$



$$Y = A \cdot \bar{B} + \bar{A} \cdot B$$

$$\bar{A} \cdot \bar{B} = X$$



NAND gate & NOR gates are called as universal gates  
 $\therefore$  with these two gates any other gates can be realized.

XOR gate & XNOR gates are special gates

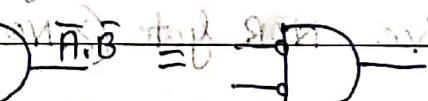
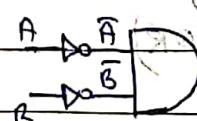
DeMorgan's theorem

$$\textcircled{1} \quad \overline{AB(A+B)} = A' \cdot B'$$

$$\textcircled{2} \quad (A \cdot B)' = A' + B'$$

The complement of the sum of two variables is equal to the product of individual complements.

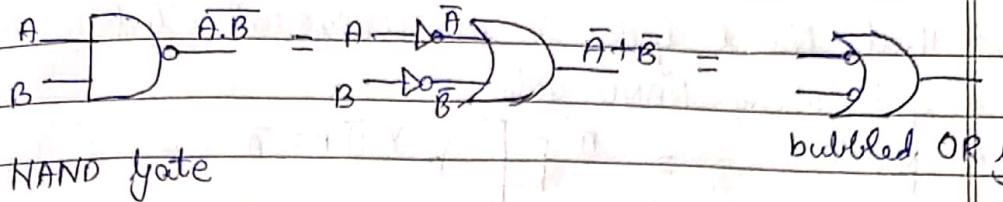
The complement of the product of two variables is equal to the sum of individual complements.



1. Nor gate

bubbled AND gate

Date: / /



A	B	$A+B$	$A \cdot B$	$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}$	$\bar{A} \cdot \bar{B}$	$\bar{A} \cdot \bar{B}$	$\bar{A}+\bar{B}$
0	0	0	0	1	1	1	1	1	1
0	1	1	0	1	0	0	1	0	1
1	0	1	0	0	1	0	1	0	1
1	1	1	0	0	0	1	0	0	0

Exclusive OR Gate

$$Y = A \oplus B$$

$$= \bar{A}B + A\bar{B}$$

$$= \bar{A}\bar{B} \cdot A\bar{B} = \bar{A}\bar{A} + A\bar{B} + BA + B\bar{B} = \bar{A}\bar{B} \cdot A\bar{B}$$

$$= (\bar{A} + \bar{B})(\bar{A} + B) = (A + \bar{B})(\bar{A} + B)$$

$$= AB + \bar{A}\bar{B}$$

Boolean laws

$$1) A + 0 = A$$

$$2) A \cdot 1 = A$$

$$3) A + 1 = 1$$

$$4) A + A = A$$

$$5) A \cdot A = A$$

$$6) A + \bar{A} = 1$$

$$7) A \cdot \bar{A} = 0$$

$$8) \bar{\bar{A}} = A$$

$$9) A \cdot 0 = 0$$

$$10) A + B = B + A$$

$$11) A \cdot B = B \cdot A$$

$$12) A(B+C) = AB+AC$$

$$13) A + BC = (A+B)(A+C)$$

$$14) A + AB = A$$

$$15) A(A+B) = A$$

$$16) A + \bar{A}B = A + B$$

$$17) A(\bar{A} + B) = AB + BA$$

$$18) AB + A\bar{B} = A$$

$$19) (A+B)(A+\bar{B}) = A$$

$$20) \bar{0} = 1$$

$$21) \bar{1} = 0$$

$$22) \bar{A} + \bar{B} = \bar{A} \cdot \bar{B}$$

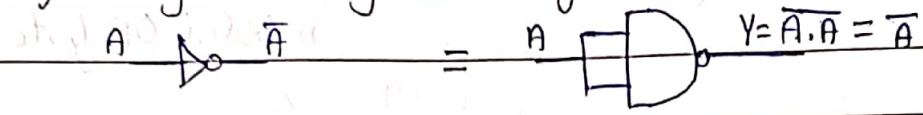
$$23) \bar{A} \cdot \bar{B} = \bar{A} + \bar{B}$$

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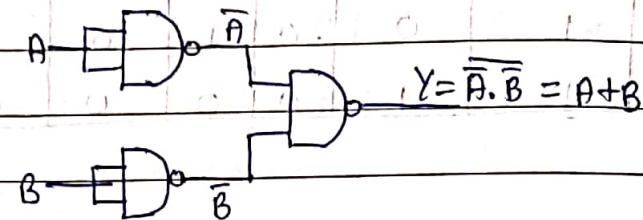
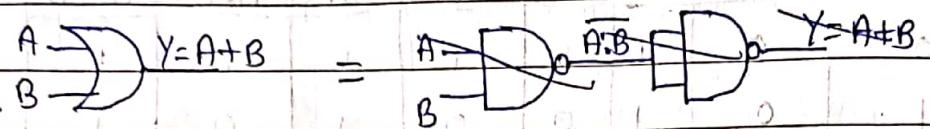
PAGE: 11

① Prove that Nand gate is an universal gate

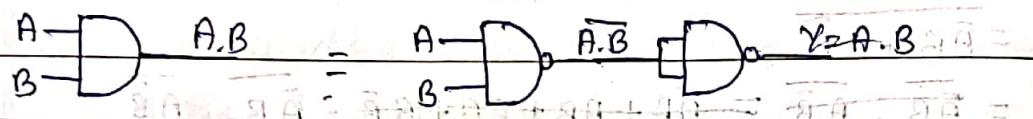
i) Not gate using NAND gate



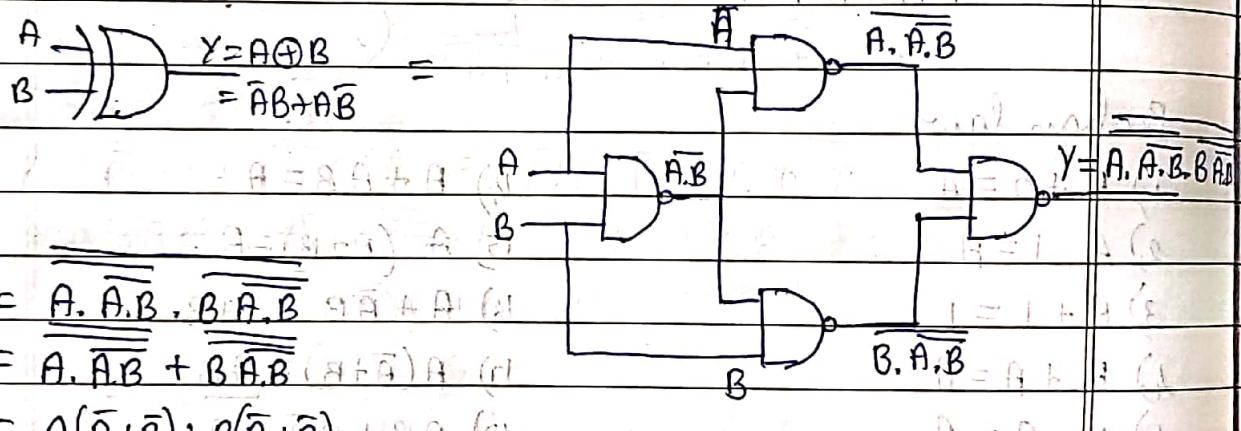
ii) OR gate using NAND gate



iii) AND gate using NAND gate



iv) Exclusive OR gate using NAND gate



② Prove that Nor gate is a universal gate

Prove that  $(\bar{A} + \bar{A+B}) \cdot (\bar{B} + \bar{B+C}) = A+B$

$$\begin{aligned} & (\overline{A} + \overline{A+B}) + (\overline{B} + \overline{B+C}) \quad [\text{De Morgan's Law}] \\ & \overline{\overline{A}} + \overline{A+B} + \overline{\overline{B}} + \overline{B+C} \end{aligned}$$

$$A \cdot A + A \cdot B + B \cdot A + B \cdot B + B + C$$

$$\underline{A + A \cdot B + B + BC}$$

$$\underline{A + B(A + I + C)}$$

A + B

$$\underbrace{A\bar{B} + ABC}_{\text{Simplification}} + \underbrace{A(B + A\bar{B})}_{\text{Distributive Law}} = 0$$

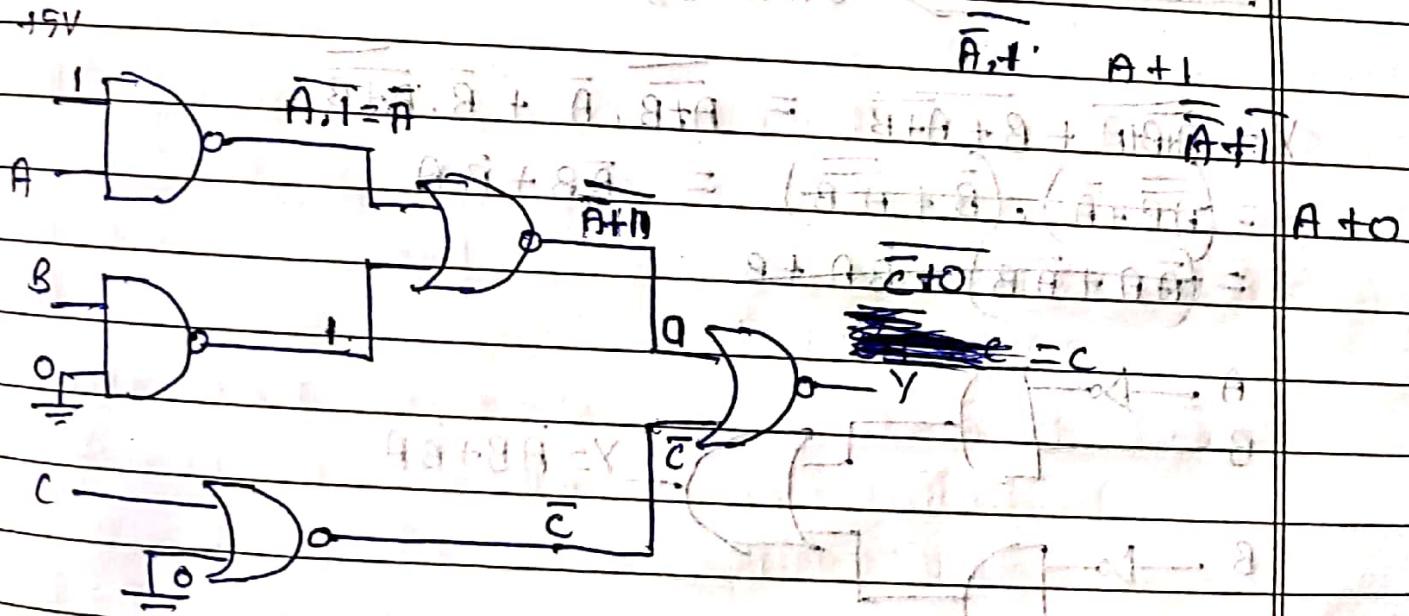
$$\overline{AB} + \overline{ABC}, \quad \overline{A(B + A\bar{B})} = 0$$

$$(A\bar{B} + A\bar{B}C) \cdot (\bar{A} + \bar{B} + A\bar{B}) \Rightarrow (A\bar{B} + A\bar{B}C), \bar{A} + (\bar{B}, A\bar{B})$$

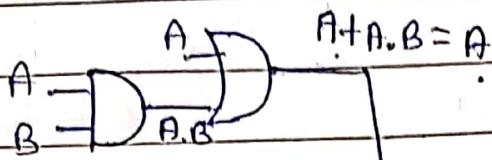
~~$\vdash A\bar{B}\bar{A} + \bar{A}BCA + \bar{B} \cdot (\bar{A} + \bar{B})$~~

$$= 0 + 0 + \dots$$

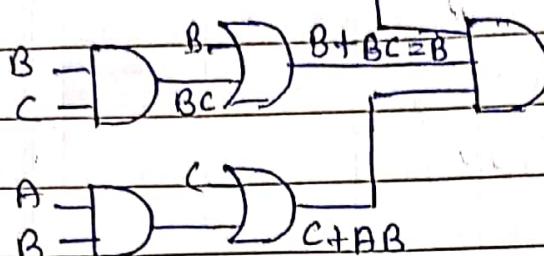
Write the boolean expression for the output in the following logic circuit.



Write the boolean expression for the logic diagram & also draw the logic diagram for the output.



$$A + A \cdot B = A$$

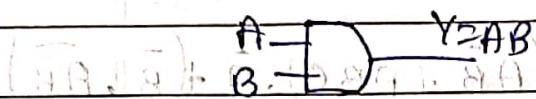
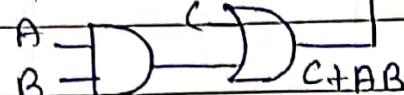


$$Y = A \cdot B \cdot (C + A \cdot B)$$

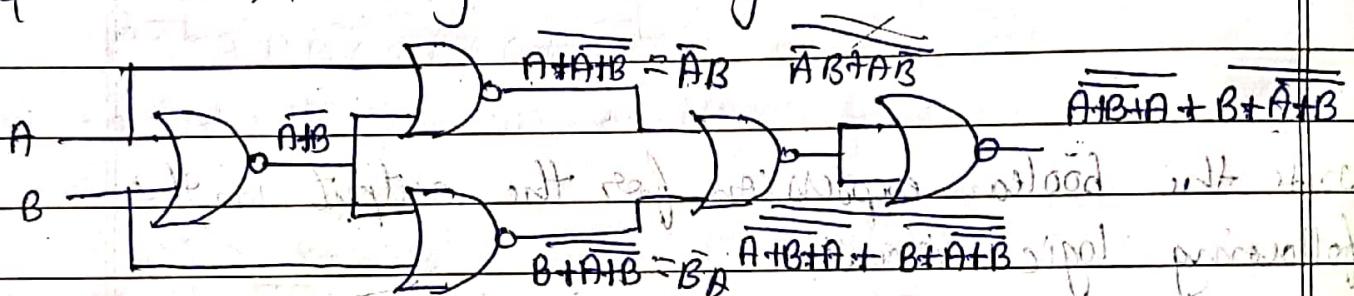
$$= A \cdot B \cdot C + A \cdot B$$

$$= A \cdot B \cdot (C + 1) = A \cdot B = Y$$

~~$$A + A \cdot B + B + B \cdot C + C + A \cdot B$$~~

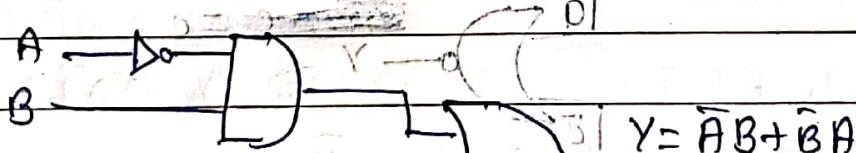


Write the O/p expression for the circuit shown. Simplify & realise it using basic gates



$$Y = \overline{(\overline{A} + B)A} + B + \overline{A + B} = \overline{\overline{A} + B} \cdot \overline{A} + B \cdot \overline{\overline{A} + B} \cdot \overline{A}$$

$$\begin{aligned} A + B &= (\overline{\overline{A} + B}) \cdot (\overline{B} + \overline{\overline{A} + B}) \\ &= (\overline{\overline{A}A + \overline{A}\overline{B}}) \cdot \overline{BA} + B \end{aligned}$$



H.W

reduce the following Boolean expression.

$$① F = A[B + \bar{C}(AB + A\bar{C})]$$

$$② f = (A + \bar{B}C), (A\bar{B} + ABC)$$

$$③ P.T (A + BC)(A\bar{B} + \bar{A}BC) = \bar{A}BC$$

$$① F = A[B + \bar{C}(AB + A\bar{C})]$$

$$= AB + A\bar{C}(\bar{A}\bar{B}, \bar{A}\bar{C})$$

$$= AB + A\bar{C}(\bar{A} + \bar{B})(\bar{A} + C)$$

$$= AB + A\bar{C}\bar{B} +$$

$$(A + \bar{B})(\bar{A} + C)$$

$$\bar{A} + \bar{A}C + \bar{B}\bar{A} + \bar{B}C$$

$$② f = (A + \bar{B}C), (A\bar{B} + ABC)$$

$$= \bar{A}, \bar{B}C (A\bar{B} + ABC)$$

$$= \bar{A}BC (A\bar{B} + ABC) = 0$$

$$③ (\bar{A} + \bar{B}C)(A\bar{B} + \bar{A}BC)$$

$$= \bar{A}BC (A\bar{B} + \bar{A} + \bar{B} + \bar{C})$$

$$= \bar{A}BC$$

Simplification of K Map

Minterms & Maxterms

$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$	Designation	A	B	$Y = A \cdot B$	minterms
$\bar{A}\bar{B}$	$m_0$	$m_1$	$m_3$	$m_2$		$0101$	$(0101)$	$\rightarrow \bar{A}\bar{B}$
$\bar{A}B$	$m_4$	$m_5$	$m_2$	$m_6$		$0110$	$(0110)$	$\rightarrow \bar{A}B$
$AB$	$m_2$	$m_3$	$m_4$	$m_5$		$1011$	$(1011)$	$\rightarrow A\bar{B}$
$A\bar{B}$	$m_8$	$m_9$	$m_{11}$	$m_{10}$		$1100$	$(1100)$	$\rightarrow AB$

2 Variables has 4 product terms

3 Variables has 8 product terms

A product term which contains all the variables of a function either in complemented or uncomplemented form is called a minterm.

An n variable function can have  $2^n$  minterms

a minterm assumes the value 1 only for one combination

The sum of minterms whose value is equal to 1 is the standard sum of the product form.  
 $\therefore$  SOP is the sum of number of product term where each product term contains all the variables of the function either complemented or uncomplemented form.

Convert the following boolean function into minterms.

$$\textcircled{1} \quad A + BC$$

$$\begin{matrix} 1 & 1 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 1 \\ 1 & 0 & 0 \end{matrix}$$

$$A + B \Rightarrow A_1 B_1 + A_1 \bar{B}_1 + \bar{B}_1 \bar{A}_1 + \bar{B}_1 A_1$$

$$(m_3 + m_2 + m_1)$$

$$= m_1 + m_2 + m_3$$

$$\textcircled{2} \quad A + BC$$

$$A(B + \bar{B})(C + \bar{C}) + BC(A + \bar{A})$$

$$ABC + A\bar{B}\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + ABC + \bar{A}BC$$

$$ABC + A\bar{B}\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC$$

$$m_1 + m_6 + m_5 + m_4 + m_3$$

$$= m_3 + m_4 + m_5 + m_6 + m_1$$

$$\textcircled{3} \quad (\bar{A} + C)(\bar{B} + D)$$

$$A\bar{B} + A\bar{D} + C\bar{B} + CD$$

$$A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + AC\bar{B} + \bar{A}CB + \cancel{(A\bar{C}\bar{B})}$$

$$A\bar{B}(C + \bar{C}) (D + \bar{D}) + AD(B + \bar{B})(C + \bar{C}) + C\bar{B}(A + \bar{A})(D + \bar{D}) + CD(\bar{A} + A)(B + \bar{B})$$

$$\Rightarrow A\bar{B}CD + A\bar{B}C\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + ADCB + A\bar{B}\bar{C}D + A\bar{B}CD$$

$$+ A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$$

$$+ \bar{A}BCD + \bar{A}\bar{B}CD + ABCD + A\bar{B}CD$$

$$\Rightarrow A\bar{B}CD + A\bar{B}C\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + ABCD + A\bar{B}\bar{C}D + \cancel{A\bar{B}C}$$

$$\cancel{A\bar{B}C\bar{D}} + \cancel{A\bar{B}CD} + \cancel{A\bar{B}C\bar{D}}$$

$$\Rightarrow m_1 + m_{10} + m_9 + m_8 + m_7 + m_{15} + m_3 + m_2 + m_1$$

$$\Rightarrow m_2 + m_3 + m_7 + m_8 + m_9 + m_{10} + m_{11} + m_{13} + m_{15}$$

A sum form term which contains all the variables of a function either in complemented or uncomplemented form is called a mace term.

An n variable function can have  $2^n$  mace terms. A mace term assumes the value 0 only for one combination.

The product of all the mace terms whose value is equal to zero is the standard product of the sum. Therefore a product of the sum is the product of a number of sum terms where each sum contains all the variables of the function either complemented or uncomplemented.

A B Mace terms designation

0 0  $A + B$  M<sub>0</sub>

0 1  $A + \bar{B}$  M<sub>1</sub>

1 0  $\bar{A} + B$  M<sub>2</sub>

1 1  $\bar{A} + \bar{B}$  M<sub>3</sub>

A B C Mace terms designation

0 0 0  $A + B + C$  M<sub>0</sub>

0 0 1  $A + B + \bar{C}$  M<sub>1</sub>

0 1 0  $A + \bar{B} + C$  M<sub>2</sub>

0 1 1  $A + \bar{B} + \bar{C}$  M<sub>3</sub>

1 0 0  $\bar{A} + B + C$  M<sub>4</sub>

1 0 1  $\bar{A} + B + \bar{C}$  M<sub>5</sub>

1 1 0  $\bar{A} + \bar{B} + C$  M<sub>6</sub>

1 1 1  $\bar{A} + \bar{B} + \bar{C}$  M<sub>7</sub>

Convert the following boolean expression into minterm form.

$$\begin{aligned} \text{Q1 } A \cdot \cancel{B+B} \quad Y &= A + BC \\ &= (A+B) (A+C) \quad \text{Distribution law} \\ &= (A+B+0) (A+C+0) \\ &= (A+B+C\bar{C}) (A+C+B\bar{B}) \\ &= (A+B+C) (A+B+\bar{C}) (A+B+C) (A+\bar{B}+C) \\ &= M_0 \cdot M_1 \cdot M_2 \end{aligned}$$

Simplification of Boolean equations using Karnaugh Map

4 Variable K-Map

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	$CD$
$\bar{A}\bar{B}$	$m_0$	$m_1$	$m_3$	$m_2$
$\bar{A}B$	$m_4$	$m_5$	$m_7$	$m_6$
$A\bar{B}$	$m_{12}$	$m_{13}$	$m_{15}$	$m_{14}$
$AB$	$m_8$	$m_9$	$m_{11}$	$m_{10}$

A K-map is a graphical device used to simplify a logic equation or to convert a truth table to its corresponding logic circuit in a simple orderly process.

A K-map is like a truth table showing the relationship b/w the logic input & desired output.

It is made up of squares or cells and may be considered as graphical representation of minterms. Each minterm is represented by a box & the boxes are arranged in an orderly manner such that adj. cells represent minterms which differ only by one variable.

A 0 represents complemented Variable & 1 represents uncomplemented Variable.

Steps:- for simplification of ~~minterms~~ boolean exp.

- Enter 1 on each the K Map for each minterm or fundamental product that

Corresponds to one minterm in the truth table.  
or the respective minterm value appearing  
in the expression

Place zeros in the other boxes.

(2) Examine the K Map for adjacent ones, encircle the octects, quads and pairs. ~~sup~~ remember to overlap and roll to get the largest groups possible.

(3) If any isolated 1's remain encircle them

(4) Eliminate any redundant group if exists

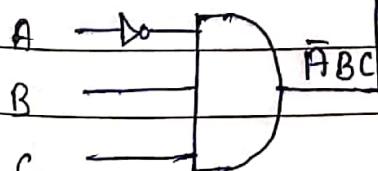
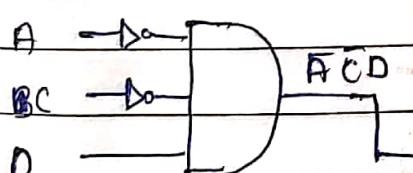
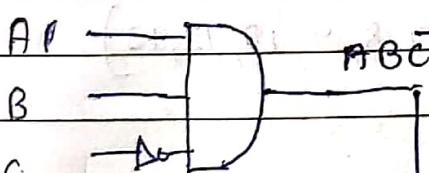
(5) With the Boolean equation by ORing the products corresponding to the encircled groups draw the equivalent logic circuit

Using K Map Simplify

$$Y = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$$

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	$CD$
$\bar{A}\bar{B}$	0	1	0	0
$\bar{A}B$	0	1	1	1
$A\bar{B}$	1	1	1	0
$AB$	0	0	1	0

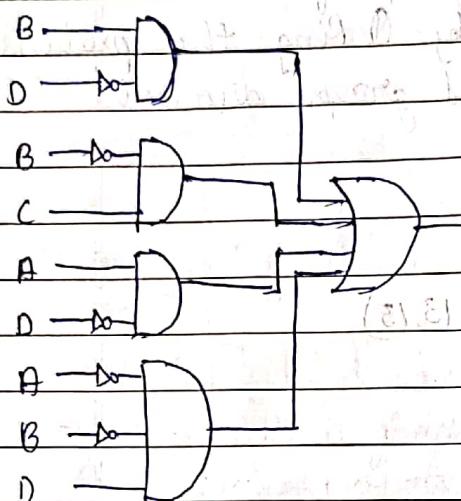
$$Y = ABC\bar{C} + \bar{A}\bar{C}D + \bar{A}BC + ACD$$



$$② Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$$

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	$CD$
$\bar{A}\bar{B}$	0	1	1	1
$\bar{A}B$	1	0	0	1
$A\bar{B}$	1	0	0	0
$AB$	0	1	1	1

$$Y = \bar{B}\bar{D} + \bar{B}C + A\bar{D} + \bar{A}\bar{B}D$$



Simplify using K Map & realize it for final answer  
using Nand gates

$$f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$$

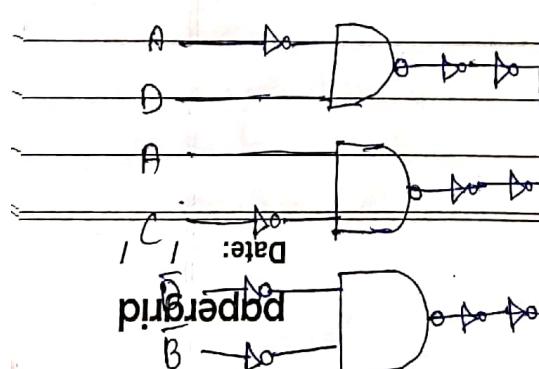
$\bar{C}\bar{D}$   $\bar{C}D$   $C\bar{D}$   $CD$

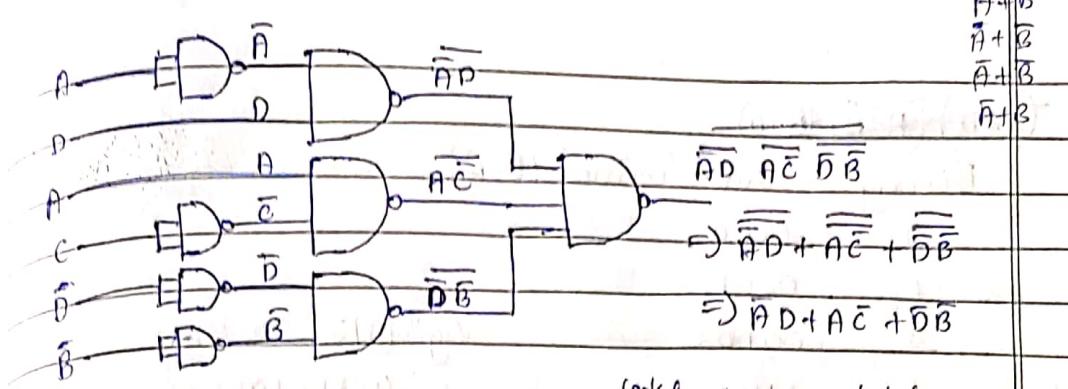
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	0	1	1	0
$A\bar{B}$	1	1	0	0
$AB$	0	1	1	1

$\bar{A}\bar{B}$	1	1	0	0
$\bar{A}B$	0	1	1	0
$A\bar{B}$	1	1	0	0
$AB$	0	1	1	1

$\bar{A}\bar{B}$	1	1	0	1
$\bar{A}B$	0	1	1	0
$A\bar{B}$	1	1	0	0
$AB$	0	1	1	1

$$Y = \bar{A}D + A\bar{C} + \bar{D}\bar{B}$$





Simplify using K Map in SOP and POS & Realize the final expression using Nand gates and RNOR gates respectively

$$F(A, B, C, D) = \sum m(0, 1, 2, 5, 8, 9, 10)$$

$\overline{CD} \quad \overline{BD} \quad CD \quad \overline{CB}$

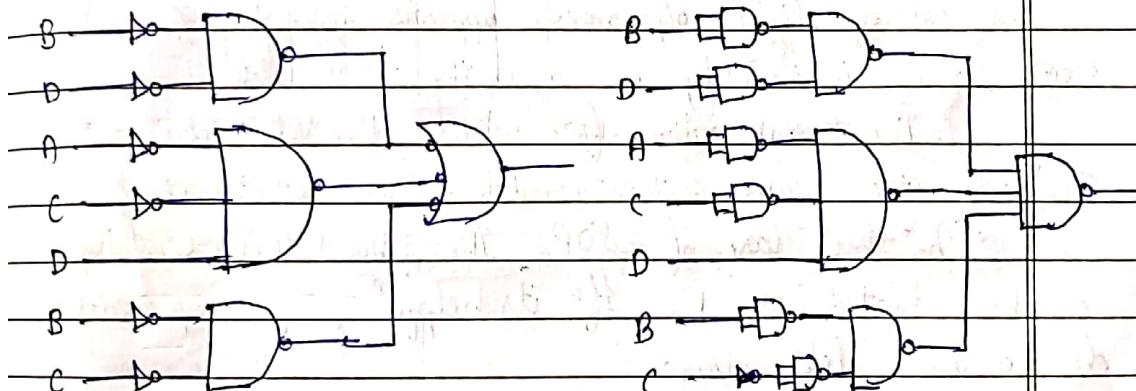
$$\begin{array}{|c|c|c|c|} \hline AB & 1 & 1 & 0 \\ \hline 1 & 1 & 0 & 1 \\ \hline 0 & 0 & 0 & 0 \\ \hline \end{array} \rightarrow \overline{B} \cdot \overline{D}$$

$$\begin{array}{|c|c|c|c|} \hline AB & 0 & 1 & 0 \\ \hline 0 & 1 & 0 & 0 \\ \hline \end{array} \rightarrow \overline{A} \cdot \overline{C} \cdot \overline{D}$$

$$\begin{array}{|c|c|c|c|} \hline AB & 0 & 0 & 0 \\ \hline 0 & 1 & 1 & 0 \\ \hline \end{array}$$

$$\overline{B} \cdot \overline{C}$$

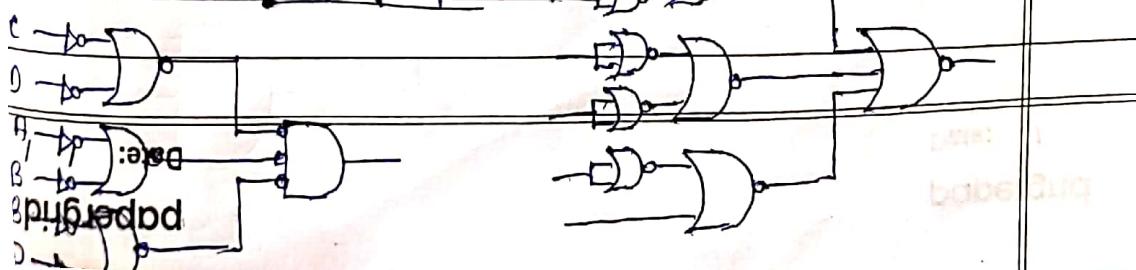
$$SOP \quad \overline{B} \cdot \overline{D} + \overline{A} \cdot \overline{C} \cdot \overline{D} + \overline{B} \cdot \overline{C} \rightarrow (\overline{B} + \overline{D})(\overline{A} + \overline{C} + \overline{D})(\overline{B} + \overline{C})$$



$C + D \quad C + \overline{D} \quad \overline{C} + \overline{D} \quad \overline{C} + D$

$$\begin{array}{|c|c|c|c|} \hline A+B & 1 & 1 & 0 & 1 \\ \hline A+\overline{B} & 0 & 1 & 0 & 0 \\ \hline \overline{A}+B & 0 & 0 & 0 & 0 \\ \hline \overline{A}+\overline{B} & 1 & 1 & 0 & 1 \\ \hline \end{array}$$

$$(\overline{C} + \overline{D})(\overline{A} + \overline{B})(\overline{B} + \overline{D})$$



~~(G.I)<sub>n</sub> (H.I)<sub>n</sub> (A.I)<sub>n</sub>~~

Binary coded decimal (BCD) Numbers are only from 0-9

0 0000

1 0001

2 0010

3 0011

4 0100

5 0101

6 0110

7 0111

8 1000

9 1001

Eg:- ① 15

0001 0101

② 96

1001 0110

### Don't care Conditions

In K Map Simplification certain input configurations never occur. These values are represented using 'X'.

In some digital circuits certain digital input

conditions never occur during the normal operation.

The corresponding o/p never appears since the o/p never occurs it is indicated by an x in the truth table.

∴ The combinations for which the values are not specified are called don't care conditions or don't care configurations.

In the case of SOP the Don't Care Condition can be treated as 1, if its helpful in map reduction else 0 and left alone.

In the same manner when we do POS reduction, the Don't care condition is treated as 0 if its helpful in map reduction else 1 and left alone.

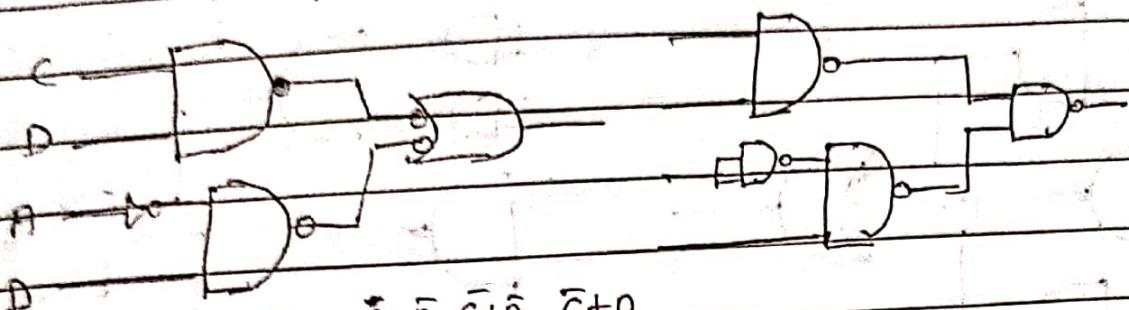
Simplify using K map

$$F(A, B, C, D) = \Sigma m(1, 3, 7, 11, 15) + \Sigma d(0, 2, 5)$$

	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
$\bar{A}\bar{B}$	X	1	1	X
$\bar{A}B$	0	X	1	0
$A\bar{B}$	0	0	1	0
$AB$	0	0	1	0

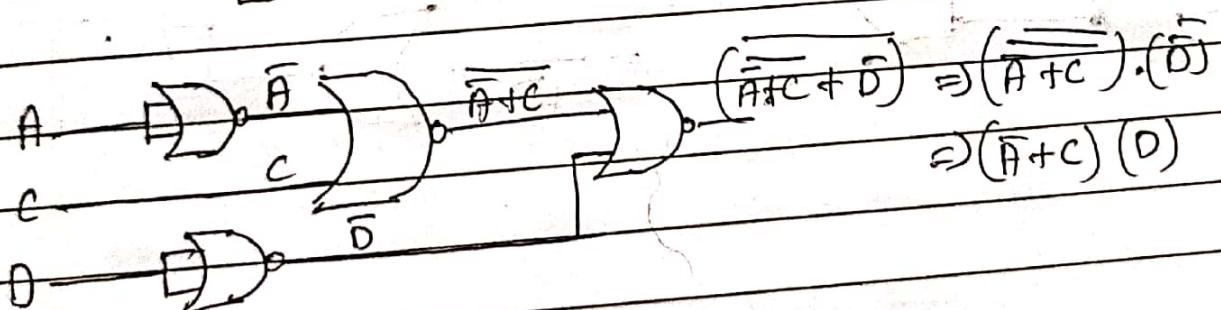
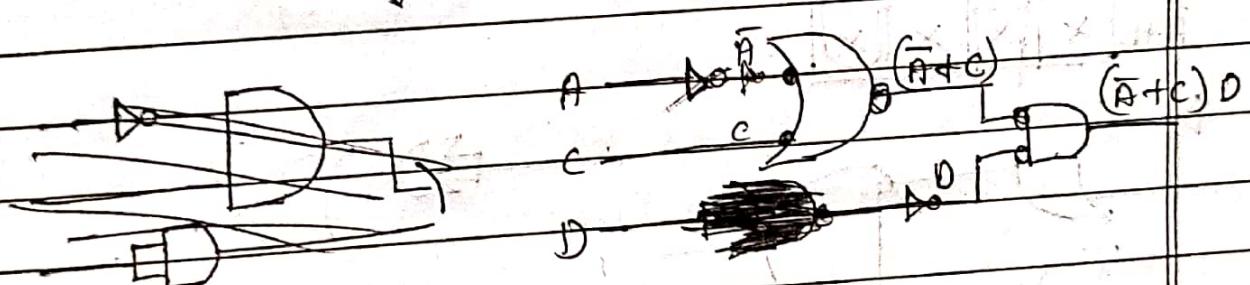
$$\Rightarrow \bar{A}\bar{D} \bar{D}D$$

$$Y = CD + \bar{A}D$$



	$C+D$	$\bar{C}+\bar{D}$	$\bar{C}+\bar{D}$	$\bar{C}+D$
$A+B$	X	1	1	X
$A+\bar{B}$	0	X	1	0
$\bar{A}+\bar{B}$	0	0	1	0
$\bar{A}+B$	0	0	1	0

$$Y = (\bar{A}+C)(D)$$



$$\begin{aligned}
 & (\bar{A}+\bar{C}+D) \Rightarrow (\bar{\bar{A}}+\bar{C}) \cdot (\bar{D}) \\
 & \Rightarrow (\bar{A}+C)(D)
 \end{aligned}$$

Simplify using K Map

$$F(w, x, y, z) = \sum m(0, 3, 4, 5, 7)$$

$$\sum d(8, 9, 10, 11, 12, 13, 14, 15)$$

	$\bar{A}B$	$A\bar{B}$	$AB$	$\bar{A}\bar{B}$	$w$	$x$	$y$	$z$	$\bar{w}$	$\bar{x}$	$\bar{y}$	$\bar{z}$
1	1	0	1	0	0	1	0	1	1	0	1	0
2	1	1	1	0	1	1	1	0	0	1	1	0
3	X	X	X	X	1	1	1	1	0	0	0	0
4	X	X	X	X	0	1	1	1	1	0	0	0

$$\bar{w}P$$

$$P$$

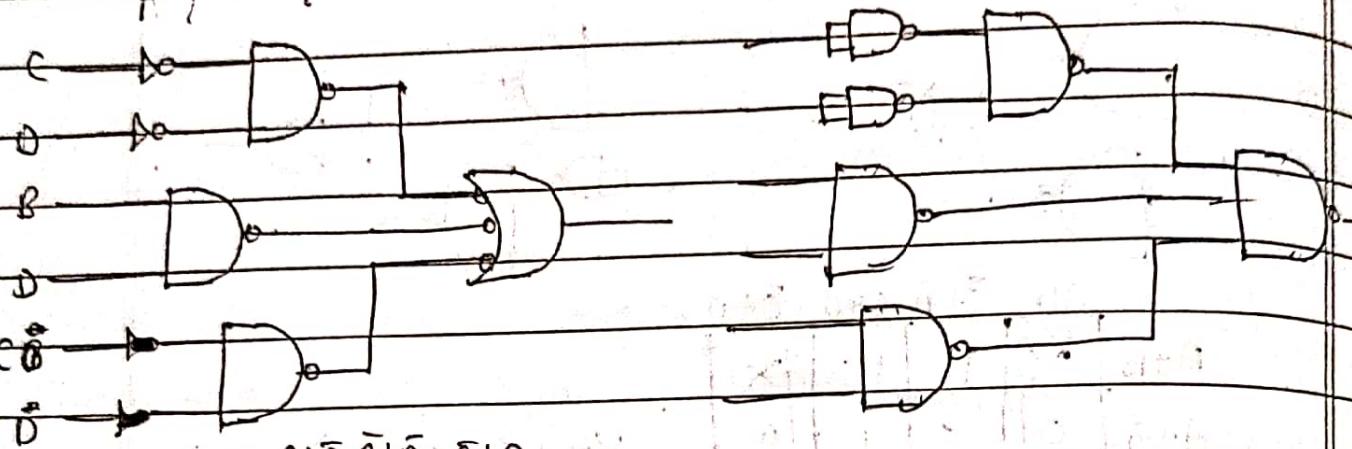
$$\bar{P}$$

	$\bar{A}B$	$A\bar{B}$	$AB$	$\bar{A}\bar{B}$	$w$	$x$	$y$	$z$	$\bar{w}$	$\bar{x}$	$\bar{y}$	$\bar{z}$
1	1	1	1	0	0	1	0	1	1	0	1	0
2	1	1	1	0	1	1	1	0	0	1	1	0
3	X	X	X	X	1	1	1	1	0	0	0	0
4	X	X	X	X	0	1	1	1	1	0	0	0

$$BD$$

$$F = \bar{C}\bar{D} + BD + \bar{B}\bar{D}CD$$

$$\bar{C}\bar{D}$$



	$C+D$	$C+\bar{D}$	$\bar{C}+\bar{D}$	$\bar{C}+D$
$A+B$	1	0	1	0
$A+\bar{B}$	1	1	1	0
$\bar{A}+\bar{B}$	X	X	X	X
$\bar{A}+B$	X	X	X	X

$$F = (\bar{C}+D)(B+C+\bar{D})$$



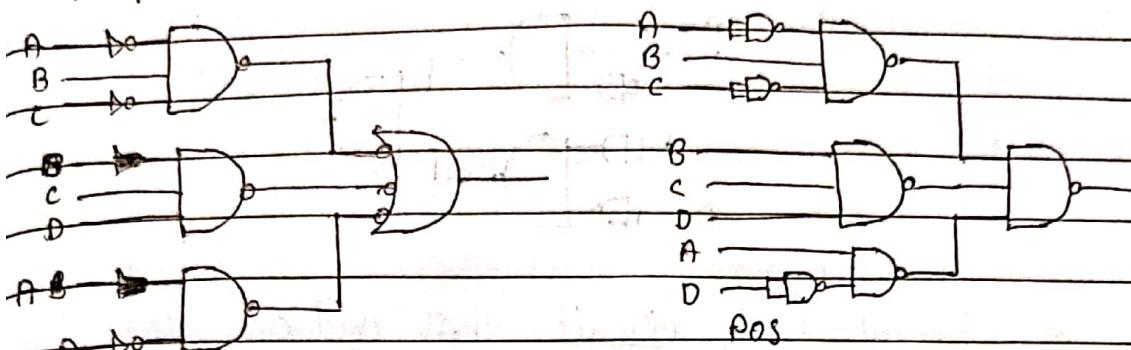
for sop m  
pos π M

Simplify using KMap

$$F(A, B, C, D) = \sum m(4, 5, 7, 12, 14, 15) \sum d(3, 8, 10)$$

	$\bar{C}D$	$\bar{C}D$	$CD$	$C\bar{D}$	
$A\bar{B}$	0	0	X	0	$\bar{A}B\bar{C}$
$\bar{A}B$	1	1	1	0	$\bar{A}CD$
$\bar{A}B$	1	1	1	1	$\bar{B}\bar{D}$
$AB$	1	0	1	1	-
$A\bar{B}$	X	0	0	X	-

$$Y = \bar{A}B\bar{C} + BCD + \bar{B}\bar{D}$$



$$Y = B(A + \bar{C} + D)(\bar{A} + C + \bar{D})$$

	$C+D$	$C\bar{D}$	$\bar{C}+\bar{D}$	$\bar{C}+D$	
$A+B$	0	0	X	0	$B$
$A+\bar{B}$	1	1	1	0	$A + \bar{C} + D$
$\bar{A}+\bar{B}$	1	0	1	1	$\bar{A} + C + \bar{D}$
$\bar{A}+B$	X	0	0	X	-

With the help of a suitable KMap Simplify the boolean function given below draw the logic circuit using basic gates. [7M]

$$Y = \sum m(3, 4, 6, 7, 8, 9, 12, 14) \oplus \sum d(1, 10, 15)$$

	$\bar{C}D$	$\bar{C}D$	$CD$	$C\bar{D}$	
$A\bar{B}$	0	X	1	0	$\bar{A}CD$
$\bar{A}B$	1	0	1	1	$B\bar{D}$
$\bar{A}B$	1	0	1	1	-
$A\bar{B}$	1	1	0	X	$A\bar{B}\bar{C}$

$$Y = \bar{A}CD + B\bar{D} + A\bar{B}\bar{C}$$

	$C+D$	$C\bar{D}$	$\bar{C}+\bar{D}$	$\bar{C}+D$	
$A+B$	0	X	1	0	-
$A+\bar{B}$	1	0	1	1	-
$\bar{A}+\bar{B}$	1	0	X	1	-
$\bar{A}+B$	1	1	0	X	-

$$Y = (A+B+D)(\bar{B}+C+\bar{D})(\bar{A}+B+\bar{C})$$

- Simplify Draw logic circuit using Nand gate.

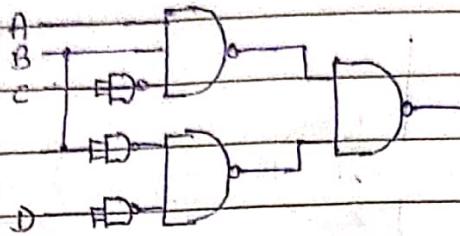
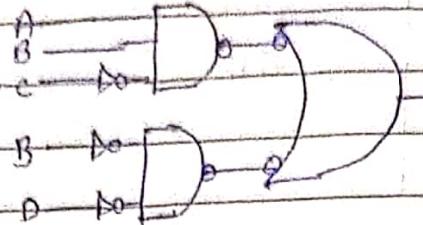
$$Y = \Sigma_m(0, 2, 10, 12, 13) \Sigma_d(3, 4, 5, 8, 11, 14, 15)$$

$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	X
$\bar{A}B$	X	X	0
AB	1	1	X
A $\bar{B}$	X	0	X

$$Y = AB\bar{C} + \bar{B}\bar{D}$$

$$\rightarrow ABC$$

$$\rightarrow \bar{B}\bar{D}$$



Design a 3 input logic circuit that produces logic 1 output when at least 2 inputs are at high state draw its truth table & the logic diagram after simplification using K Map

	A	B	C	$X = A + B + C$	$Y = A \cdot B \cdot C$
$m^0$	0	0	0	0	0
$m^1$	0	0	0	1	0
$m^2$	0	0	1	0	0
$m^3$	1	0	1	1	0
$m^4$	0	1	0	0	0
$m^5$	1	1	0	1	0
$m^6$	1	1	1	0	0
$m^7$	1	1	1	1	1

$\bar{C} C$

$\bar{A}\bar{B}$	$\bar{A}B$	AB	A $\bar{B}$
X	X	X	X
X	X	X	X
X	X	X	X

$\bar{A}\bar{B}$	$\bar{A}B$	AB	A $\bar{B}$	$\bar{B}C$	$\bar{B}C$	$\bar{B}C$	$BC$	$BC$
X	X	X	X	0	0	1	1	0
X	X	X	X	0	0	1	1	0
X	X	X	X	0	0	1	1	0
X	X	X	X	0	0	1	1	0

Design a 4/8/p logic circuit that produces a logic 1 output when 2 adjacent inputs are at high state. Write the truth table. Draw the logic diagram after simplification using K Map.

$\bar{B}D \quad \bar{C}D \quad CD \quad \bar{C}\bar{D}$

$\bar{A}\bar{B}$	0	0	1	0	$\rightarrow CD$
$\bar{A}B$	0	0	1	1	$\rightarrow BC$
$AB$	1	1	1	1	$\rightarrow AB$
$A\bar{B}$	0	1	0	0	$\rightarrow AD$

$$Y = CD + AB + BC + AD$$

A    B    C    D

0    0    0    0    0     $m^0$

0    0    0    1    0     $m^1$

0    1    0    0    0     $m^2$

0    0    1    0    0     $m^3$

0    1    0    0    1     $m^4$

0    0    1    1    0     $m^5$

0    1    1    0    1     $m^6$

0    1    1    1    1     $m^7$

1    0    0    0    0     $m^8$

1    0    0    1    0     $m^9$

1    1    0    0    1     $m^{10}$

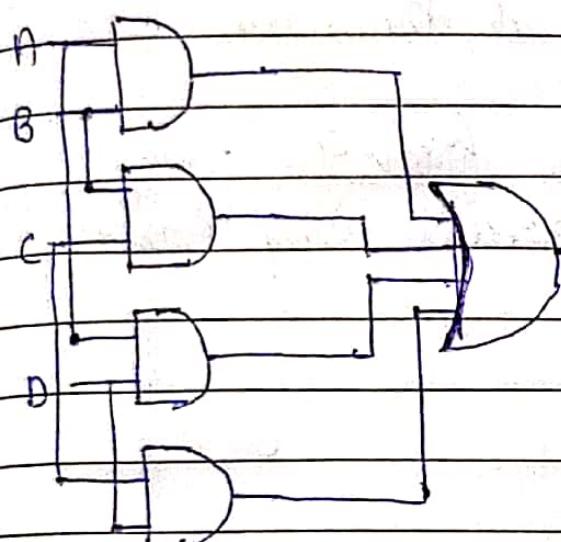
1    1    0    1    1     $m^{11}$

1    0    1    0    1     $m^{12}$

1    0    1    1    1     $m^{13}$

1    1    1    0    1     $m^{14}$

1    1    1    1    1     $m^{15}$



① Convert the following Numbers into their decimal equivalent  
i)  $(100011.111)_2$   
ii)  $(526.367)_8$  (2+2)

② Perform the following subtraction using 2's complement  
 $(29.39)_0 - (33.58)_{10}$  (4)

③ Convert the following Numbers into their hexadecimal equivalent  
i)  $(10001101.11011)_2$   
ii)  $(635.268)_{10}$  (2+2)

④ Perform subtraction using 2's complement

$$i) (10.1010)_{10} - (11.11)_{10}$$

$$ii) (1010111.111)_2 - (1010100.011)_2 \quad (2)$$

⑤ State & prove de morgan's theorem & draw the equivalent logic circuit.

⑥ Obtain the simplified expression from the Kmap shown below & draw a logic circuit using Nand gates.

AB CD 00 01 11 10

AB	00	0	0	X	1
AB	01	1	1	X	0
AB	11	1	1	X	0
AB	10	0	0	X	1

⑦ P.T : Nand gate is a universal gate

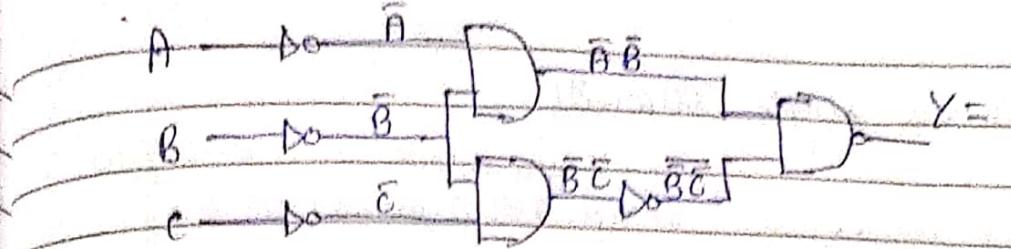
⑧ Realize AND, OR, NOT, NAND gates using NOR gate only. Write the necessary expression.

⑨ Draw logic circuit for XOR gate & XNOR gate using basic gates

⑩ Convert the following boolean expression into standard SOP and POS forms

$$X + \overline{Y}Z$$

⑪ Draw the logic circuit for the circuit for the logic diagram given below after applying boolean law



(12) Simplify the boolean expression using boolean laws

$$P = \bar{X}YZ + \bar{X}\bar{Y}Z + \bar{X}YZ + X\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} + XY\bar{Z}$$

$$+ XYZ$$

(13) Convert the following boolean expression into standard POS forms

$$XY + \bar{X}Z$$

(a) P.T.Q  $(\bar{A} + (A+B))(B + (B+C)) = A + B$

$\textcircled{b} \quad A - B C$

$$(b) (\bar{A} + \bar{B}C)(A\bar{B} + ABC) = \bar{A}BC$$

(14) Prove distributive law by truth table method.

$$(Z + \bar{Z}) + Z\bar{Z}$$

$$A + BC$$

$$XY + \bar{X}Z$$

$$A(B + \bar{B})(C + \bar{Z}) + ABC + \bar{A}BC$$

~~$X + Z\bar{Z} + \bar{X}Z + Y\bar{Y}$~~

$$\bar{ABC} + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + ABC$$

~~$(X + Z\bar{Z})(Y + Z\bar{Z})$~~

$$+ \bar{ABC}$$

~~$(\bar{A} + \bar{B} + C)(A + B + \bar{C})(\bar{A} + B + C)$~~

~~$(\bar{A} + \bar{B} + \bar{C})(A + B + \bar{C})$~~

$$2 | 635 \quad \cancel{268}$$

$$16 | 635 \quad \cancel{268}$$

$$\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$2 | 317 - 1$$

$$16 | 39 - 11 - B$$

$$(A + B + \bar{C})(A + \bar{B} + C)(A + B + C)$$

$$2 | 158 - 1$$

$$2 - 7$$

$$0.728 \times 16 = 11.648$$

$$2 | 79 - 0$$

$$0.289 \times 16 = 4.608$$

$$2 | 39 - 1$$

$$0.607 \times 16 = 9.728$$

$$2 | 14 - 1$$

$$0.286 \times 2 = 0.572$$

$$2 | 9 - 1$$

$$0.572 \times 2 = 1.144 \quad 27.6449 BH$$

$$2 | 4 - 1$$

$$0.1144 \times 2 = 8$$

$$2 | 2 - 0$$

$$0 \ 10 \ 1 \ \cancel{10} \\ \dots 1101011$$

# Combinational logic circuits

It is a circuit in which the output depends on the present input at that instant.

It has no memory element.

Eg:- ~~flip flops~~ Half adder, full adder

## Half adder.

It is a combinational logic circuit which is used to add two one bit values with outputs sum and carry.

Symbol

A

HA

B

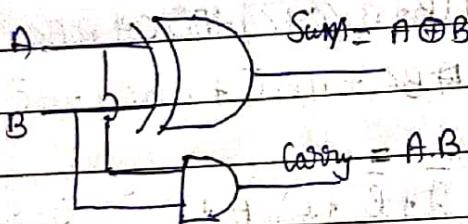
Sum

$$= \bar{A}B + A\bar{B} \text{ or } A \oplus B$$

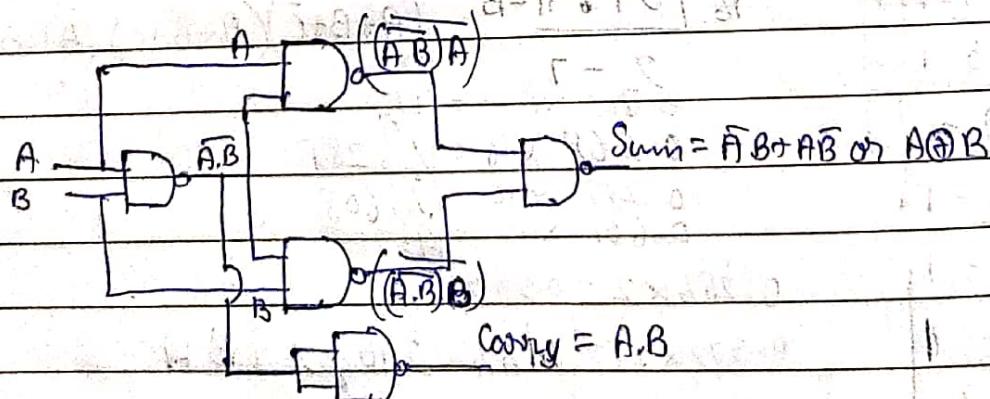
Carry

$$= A \cdot B$$

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



## Half adder using Nand gates



What is half adder write its truth table, realize half adder using NAND gates / Nor gates

$$(\bar{A}B) + (\bar{A}B)$$

$$(A \cdot \bar{B}) + (\bar{A} \cdot B)$$

$$\bar{A} \cdot A + B \cdot \bar{A} + \bar{A} \cdot B \cdot B = \bar{A}B + A\bar{B}$$

## Full adder

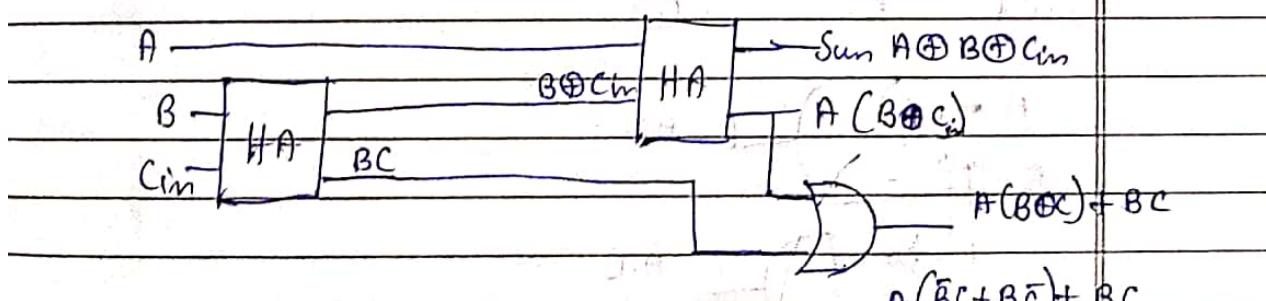
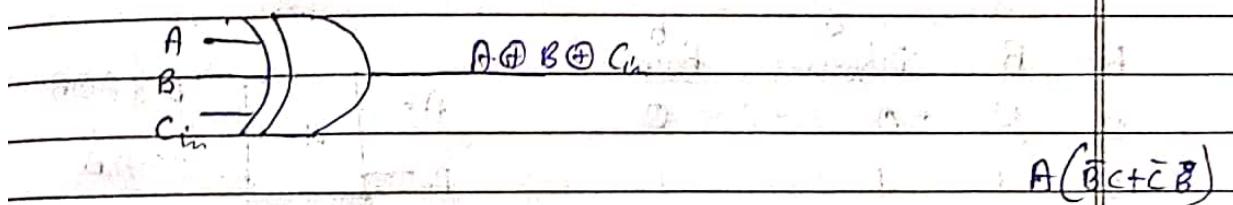
It is a combinational logic circuit which is used to adds two bits and a carry from the previous addition producing the sum and carry. The results of a full Adder addition can be shown in a truth table.

A		→ Sum $A \oplus B \oplus C_{in}$
B	FA	→ carry ( $C_o$ )
$C_{in}$		

Symbol

Truth table

A	B	$C_{in}$	Sum	Carry ( $C_o$ )	
0	0	0	0	0	$\bar{A}B$
0	0	1	1	0	$\bar{A}B + \bar{B}C + ABC$
0	1	0	1	0	$A\bar{B}C$
0	1	1	0	1	$AB + AC + BC$
1	0	0	1	0	$A(B+1) + BC$
1	0	1	0	1	$A$
1	1	0	0	1	$A + B$
1	1	1	1	0	

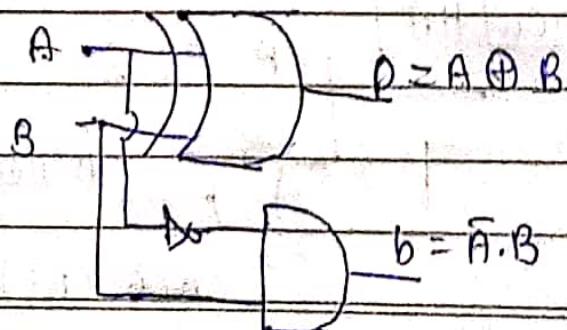
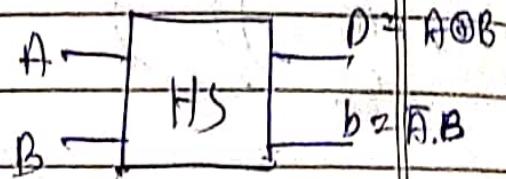


## Half Subtractor

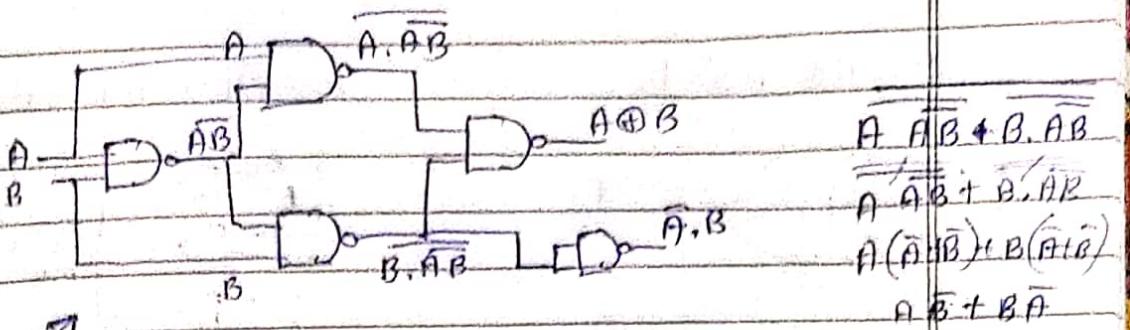
It is a combinational logic circuit that subtracts one bit from the other. It is used to subtract the MSB of the Subtrahend with LSb of the minuend. After the operation it produces a difference bit and a borrow bit.

This can be illustrated in a truth table.

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



Date: / /  
papergrid

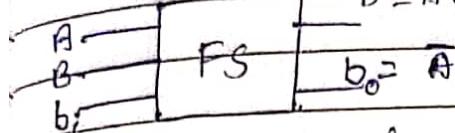


realize a half subtractor circuit using NAND gates only

### Full Subtractor

Symbol

$$D = A \oplus B \oplus b_i$$



Truth table

A	B	b <sub>i</sub>	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

It is a combinational logic circuit that performs subtraction of two bits, one is the minuend (suprandend) taking into account of the borrow from the previous subtraction. It subtracts 1 bit B from another bit A when already there is a borrow bit from this column for subtraction in the preceding column and it produces the o/p as a difference of bit & borrow bit.

K-map for difference, borrow

$\bar{B}C$	$\bar{B}C$	$BC$	$BC$
0	1	1	1
1	1	1	0
0	0	1	0

$b_i$ :  $b_o$ :

$\bar{A}\bar{B}$	0	1
$\bar{A}B$	1	0
$AB$	0	1
$A\bar{B}$	1	0

$b_i$ :  $b_o$ :

$\bar{A}\bar{B}$	0	1
$\bar{A}B$	1	1
$AB$	0	1
$A\bar{B}$	0	0

$\bar{A}C + \bar{A}B + BC$

$$\bar{A}(B + C) + BC$$

$$1(a \cdot 1) +$$

$$D = A \oplus B \oplus b_i$$

$$b_o = \bar{A}B + \bar{A}b_i + BB_i$$

$$= \bar{A}(B \oplus b_i) + BB_i$$

Date: / /

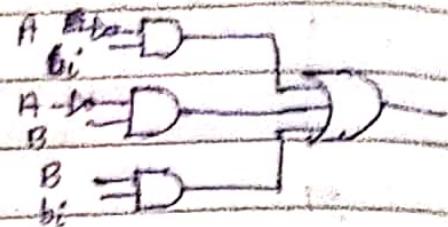
Paper grid

$$D = A \oplus B \oplus b_i$$

$$b_o = \bar{A}b_i + \bar{A}B + AB$$

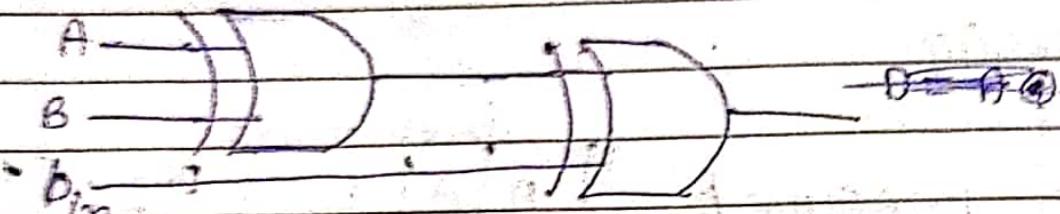


$$D =$$

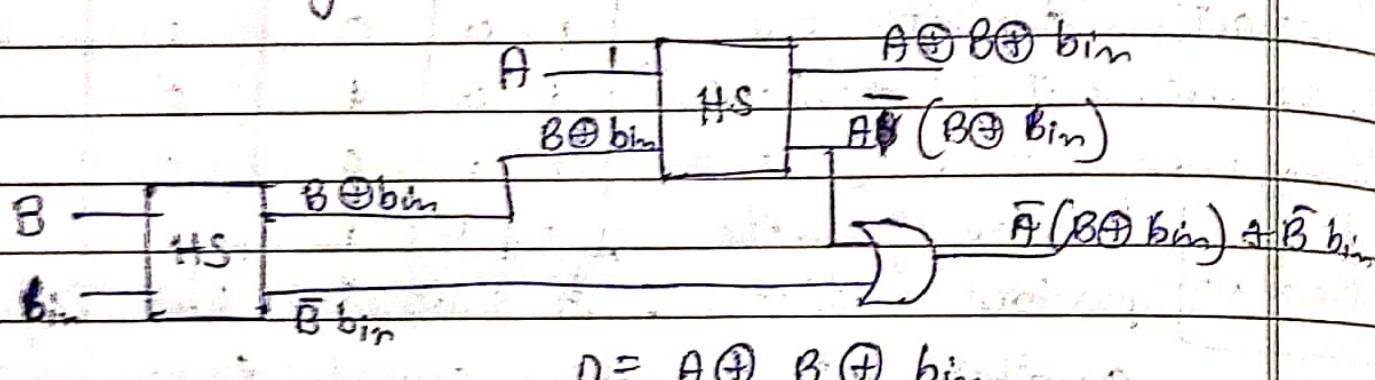


realize circuit

↑ FS using E NOR gates

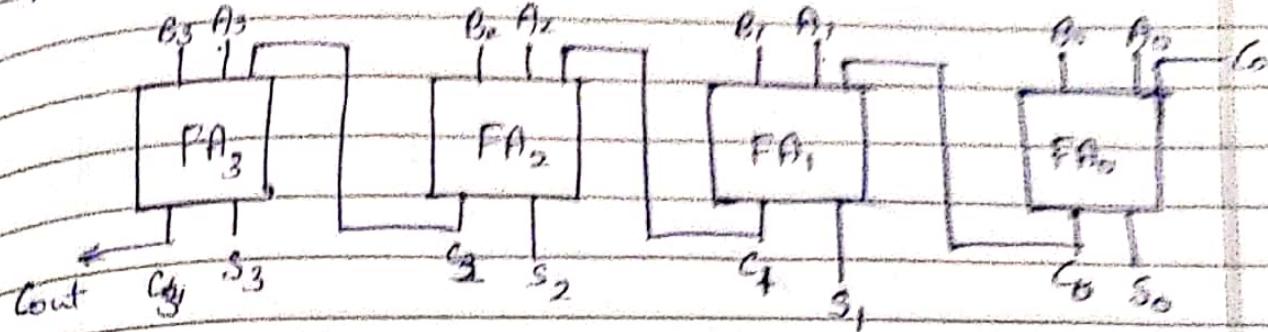


Realize FS circuit using two half subtractor circuit  
+ an OR gate.



$$D = A \oplus B \oplus b_i$$

4 bit parallel binary adder



Write the procedure to add

A 4 bit parallel binary adder. Combinations logic circuit that has 2 binary no. is parallel form it produces the arithmetic sum of the numbers in parallel form it consists of 4 full adder circuits connected one after another with the output carry from each ~~as~~ FA connected to the o/p carry of the next FA. In succession. This is illustrated in the diagram. Let us represent the numbers as A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub> & B<sub>0</sub>, B<sub>1</sub>, B<sub>2</sub>, B<sub>3</sub>. The resulting o/p bits can be represented as S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>

Explain the procedure of Addition of two 4-bit binary numbers using FA's

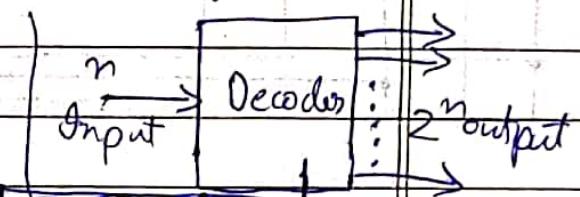
### Decoder

A decoder is a combinational circuit which is used to detect the presence of a specified combination of bits on its inputs and to indicate that presence by a specified o/p level. In its general form, a decoder has  $n$  i/p lines and  $2^n$  o/p lines, to indicate the presence of  $1$  or more combinations. In a decoder circuit, the o/p lines are such that, only one o/p line is activated for each one of the possible combinations of the i/p. i.e. an AND gate can be used for decoding the information as it produces a high o/p only when all i/p's are high. A NAND gate can also be used in the place of an AND gate as it gives a low o/p when all the i/p's are high.

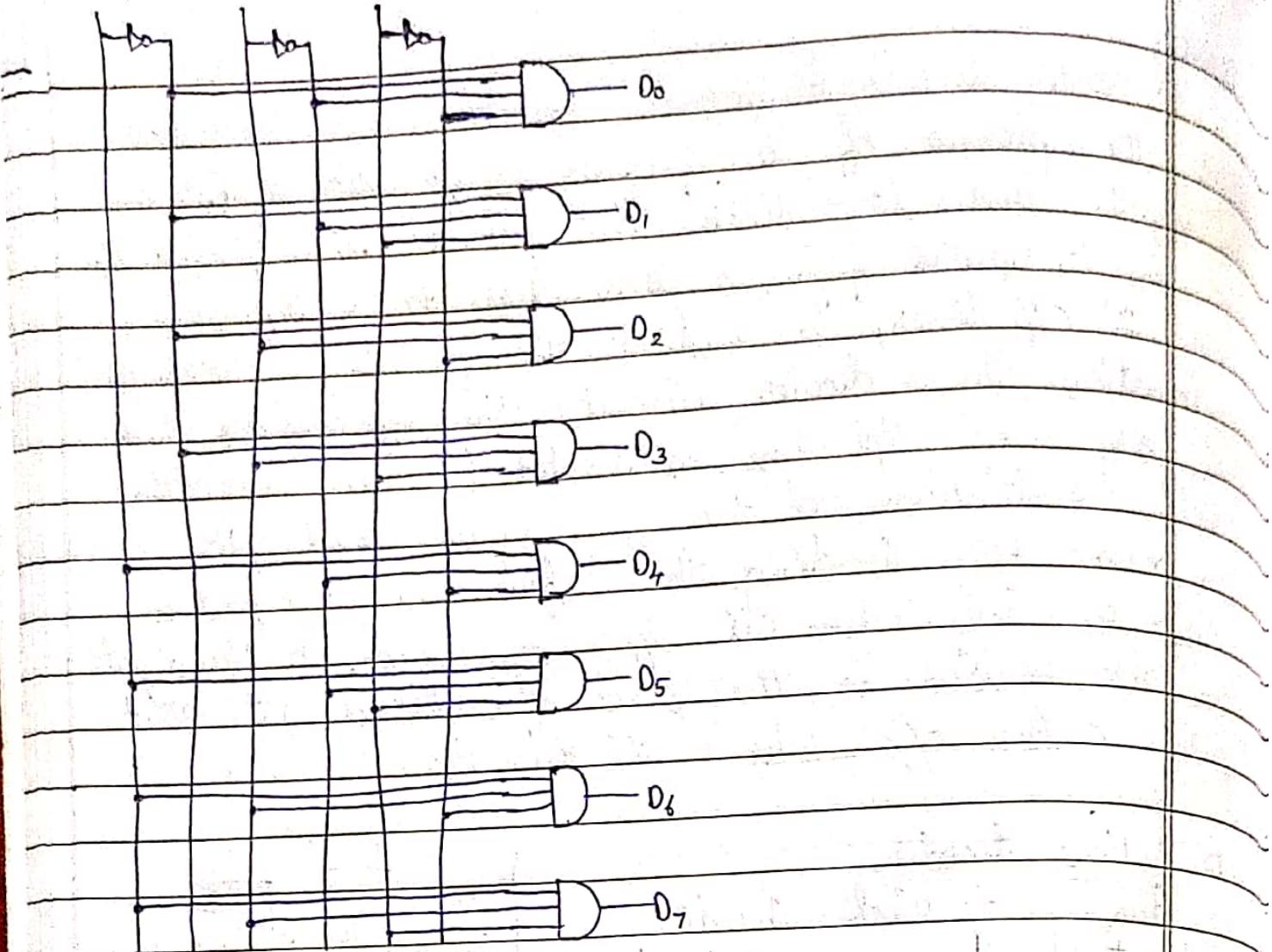
### Symbol

3 to 8 line decoder.

Binary to octal decoder.

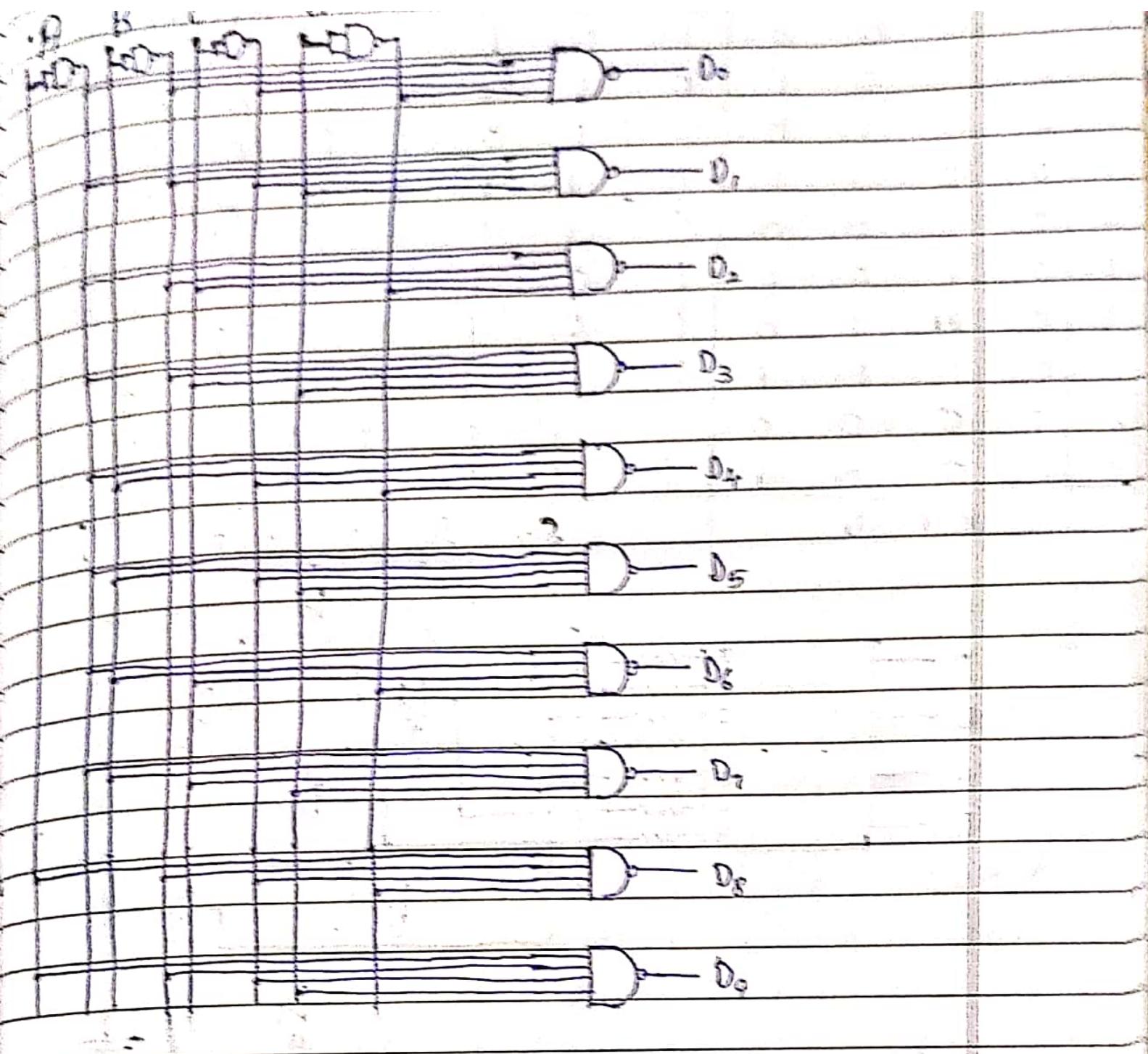


Input			Output							
A	B	C	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	1	0
1	1	1	0	1	0	0	0	0	0	0

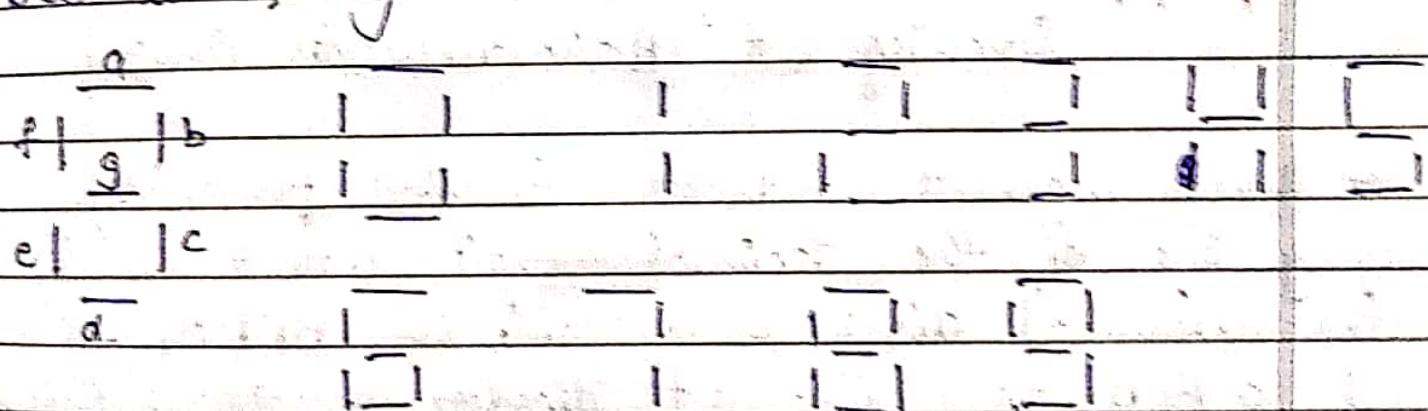


Draw the 'BCD to decimal decoder using NAND gate'

A	B	C	D	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	
0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
1	0	0	0	1	1	1	1	1	1	1	1	1	0	1
2	0	0	1	0	1	1	1	1	1	1	1	0	1	1
3	0	0	1	1	1	1	1	1	1	1	0	1	1	1
4	0	1	0	0	1	1	1	1	1	0	1	1	1	1
5	0	1	0	1	1	1	1	1	0	1	1	1	1	1
6	0	1	1	0	1	1	0	1	1	1	1	1	1	1
7	0	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1	0	0	0	1	0	1	1	1	1	1	1	1	1
9	1	0	0	1	0	1	1	1	1	1	1	1	1	1



BCD to 7 Segment Decodes

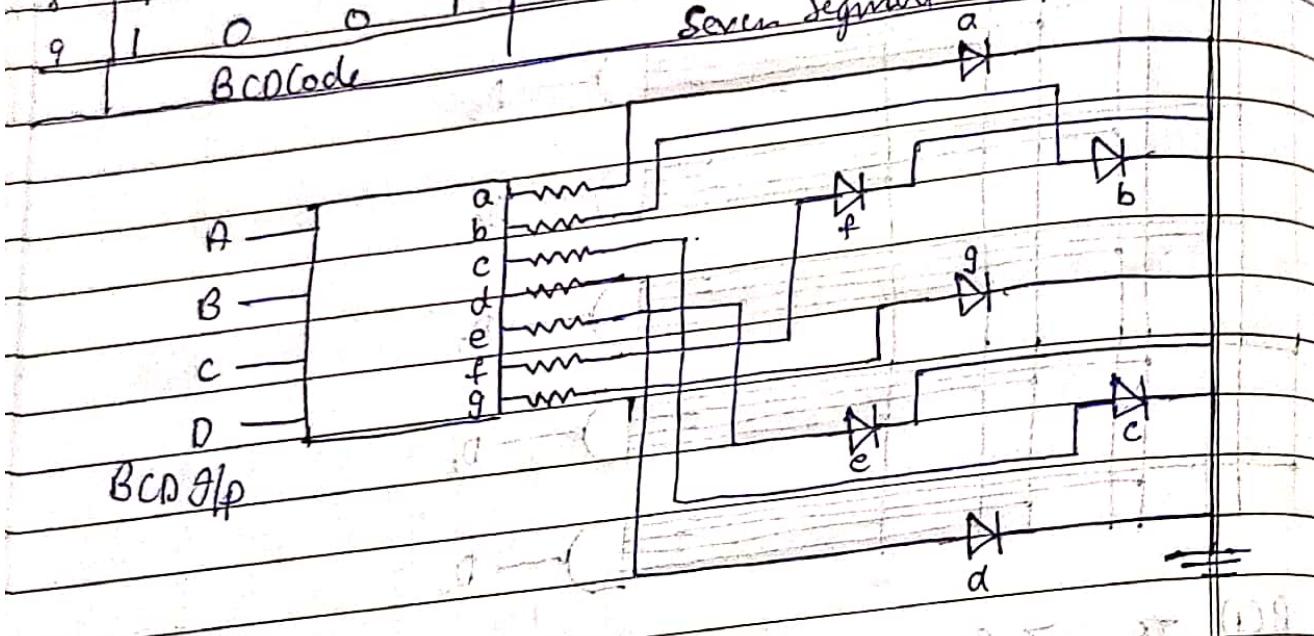


Truth table

D.No	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	1	1	0
2	0	0	1	0	1	1	1	1	0	0	1
3	0	0	1	1	0	1	1	1	0	1	1
4	0	1	0	0	1	0	1	1	1	1	1
5	0	1	0	1	1	0	1	1	0	0	0
6	0	1	1	1	1	1	1	1	1	1	1
7	0	1	1	1	1	1	1	1	0	1	1
8	1	0	0	0	1	1	1	1	1	0	1
9	1	0	0	1	1	1	1	1	1	1	1

BCD code

Seven Segment output



107416 / 7447  
Seven segment Active low decoder Driver

A seven segment indicator is used for displaying any one of the decimal digits 0 to 9 usually the decimal digit is available in BCD format & a BCD to 7 segment decoder accepts a decimal digit in BCD & generates the corresponding 7 segment code. Figure shows a BCD to 7 segment decoder with the 7 segment shown which is made up of the material that

emits light when the current is passed through it  
 The segments a, b, c, d, e, f, g run clockwise from the top for each segment to display a [1]  
 we need to light up segments ~~a~~ b & c only.  
 To display the no. 8 all segments should be lighted up. The seven segments are ~~opposite~~ appearing either in the common anode form or in the common cathode form.

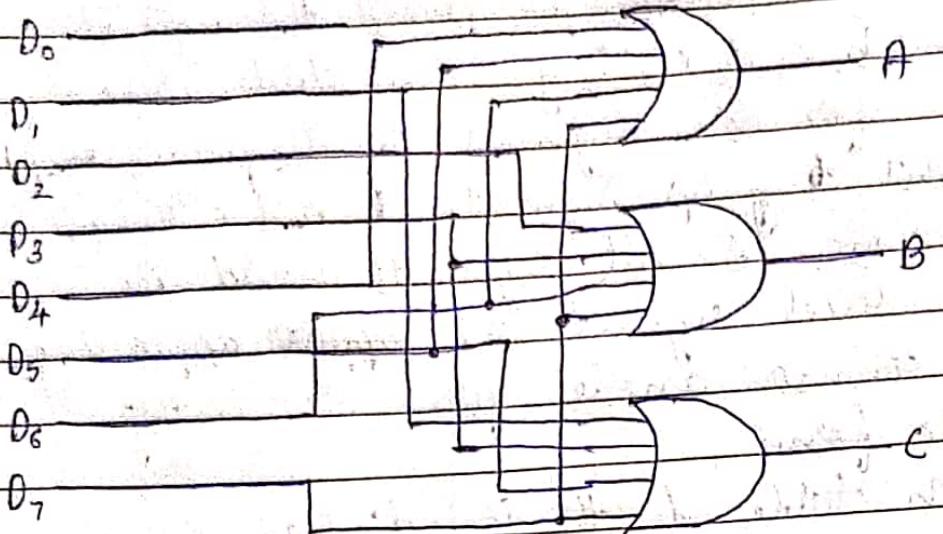
The truth table & the logic diagrams are given.  
 In order to display all this numbers a decoding logic is required for each segments

## ENCODER

An Encoder is a CLU Combinational Logic Circuit that essentially performs the reverse function of a decoder i.e an encoder accepts an active level on one of its inputs representing a digit such as decimal & converts it into a coded o/p such as binary i.e. the process of converting from familiar symbols & Numbers into a coded format is called as Encoding.

### 8 line to 3 line Encoder

Inputs								Outputs		
$D_7$	$D_6$	$D_5$	$D_4$	$D_3$	$D_2$	$D_1$	$D_0$	A	B	C
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	1	1	0
0	0	0	1	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1



Draw the Truth Table & circuit diagrams of  
Decimal to BCD Encoder

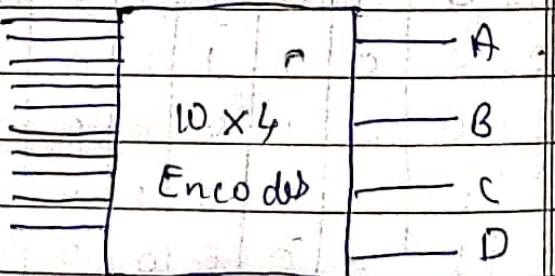
Decimal	Inputs								Outputs			
	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	A	B	C	D
0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	0	1
2	0	0	0	0	0	0	1	0	0	0	1	0
3	0	0	0	0	0	0	1	0	0	0	0	1
4	0	0	0	0	0	1	0	0	0	1	0	0
5	0	0	0	0	1	0	0	0	0	1	0	1
6	0	0	0	1	0	0	0	0	0	1	1	0
7	0	0	1	0	0	0	0	0	0	1	1	1
8	0	1	0	0	0	0	0	0	1	0	0	0
9	1	0	0	0	0	0	0	0	1	0	0	1

$$A = D_8 + D_9$$

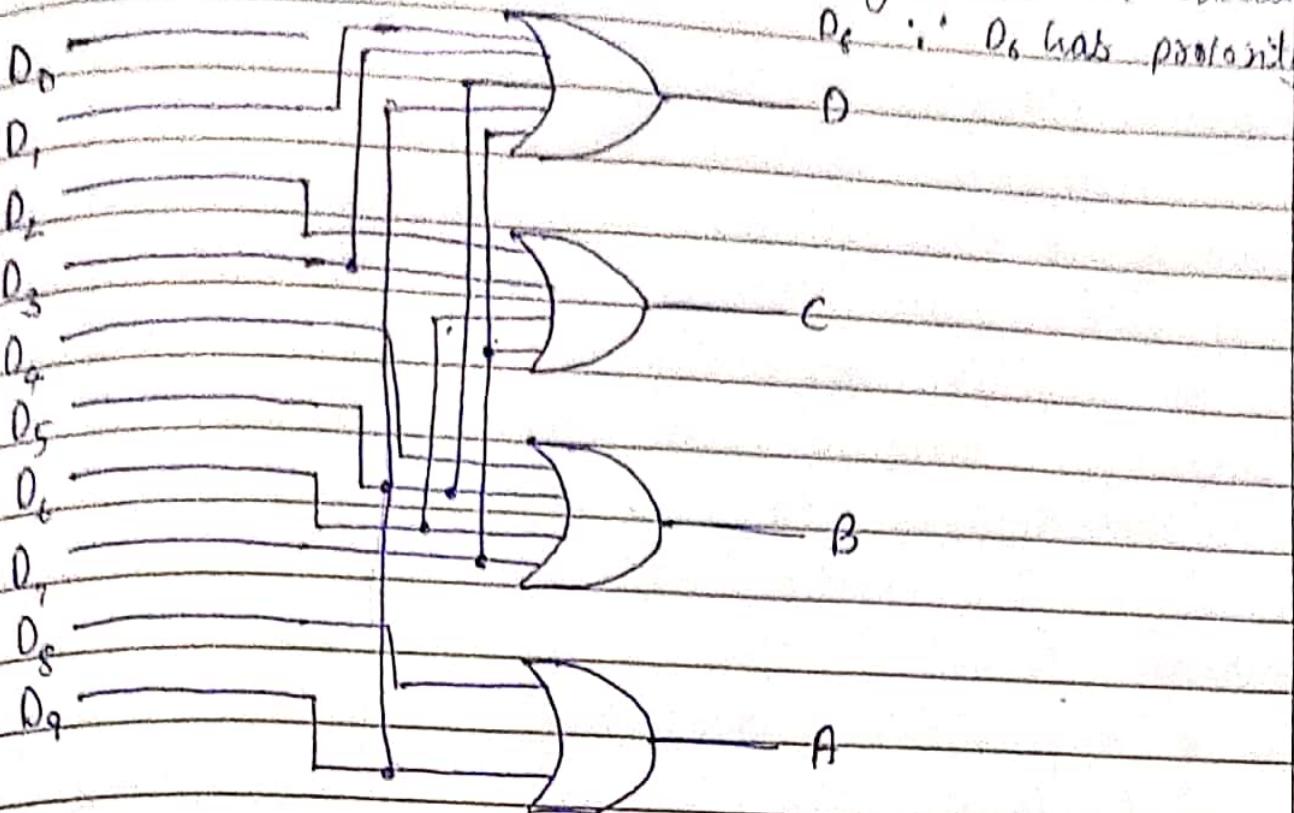
$$B = D_4 + D_5 + D_6 + D_7$$

$$C = D_2 + D_3 + D_6 + D_7$$

$$D = D_1 + D_3 + D_5 + D_7 + D_9$$



When two I/p  $D_6$  or  $D_7$  is in high state the encoder displays  $D_6$  i.e.  $D_6$  has priority.



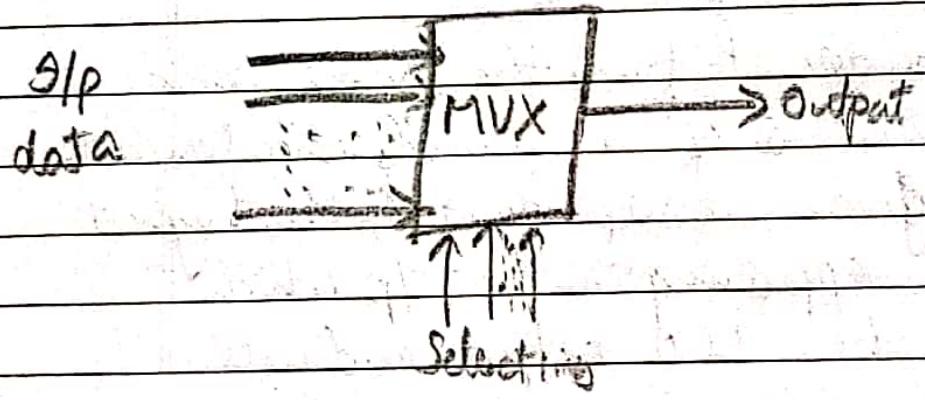
### Priority encoder

This type of encoder performs the same basic encoding function as that of a normal encoder but there is a priority given corresponding to the highest order decimal digit appearing on the I/p which will be displayed as the BCD output and will ignore all the lower decimal numbers.

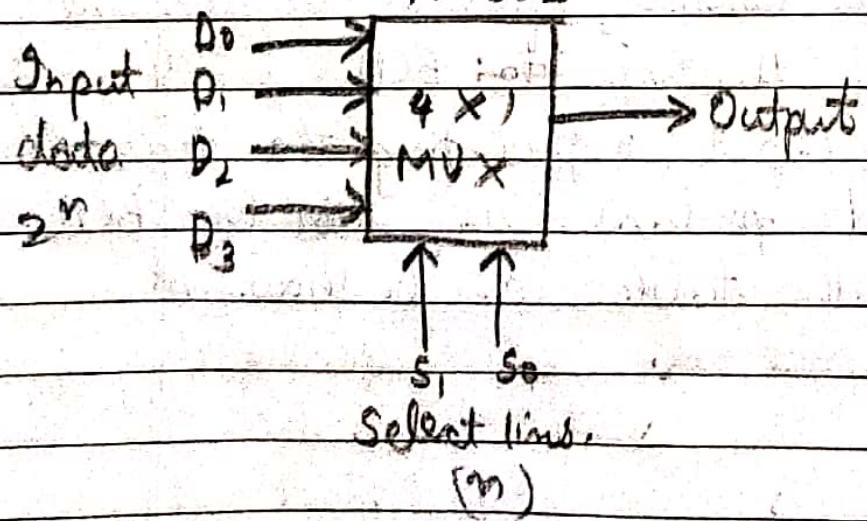
Eg:- If 6 & 3 I/p's are both high, the BCD o/p will be 0110 which represents the decimal 6. The IC 74147 is a decimal to BCD priority encoder & it has active low inputs representing the decimal digit 1 through 9 and produces an active low BCD code as o/p. The truth table can be shown as below.

## Multiplexer (MUX)

Multiplexers means Many with one. Multiplexing is the process of transmitting a large no of information units over a common channel, as line. A digital multiplexer or data selector is a combinational circuit that selects digital info from several sources ( $2^n$ ) and transmits this information on a single o/p line. i.e. the multiplexer has several Data I/O lines & a single o/p line. Selection of a particular o/p line is controlled by a set of select lines. The symbol of a multiplexer can be drawn as follows.



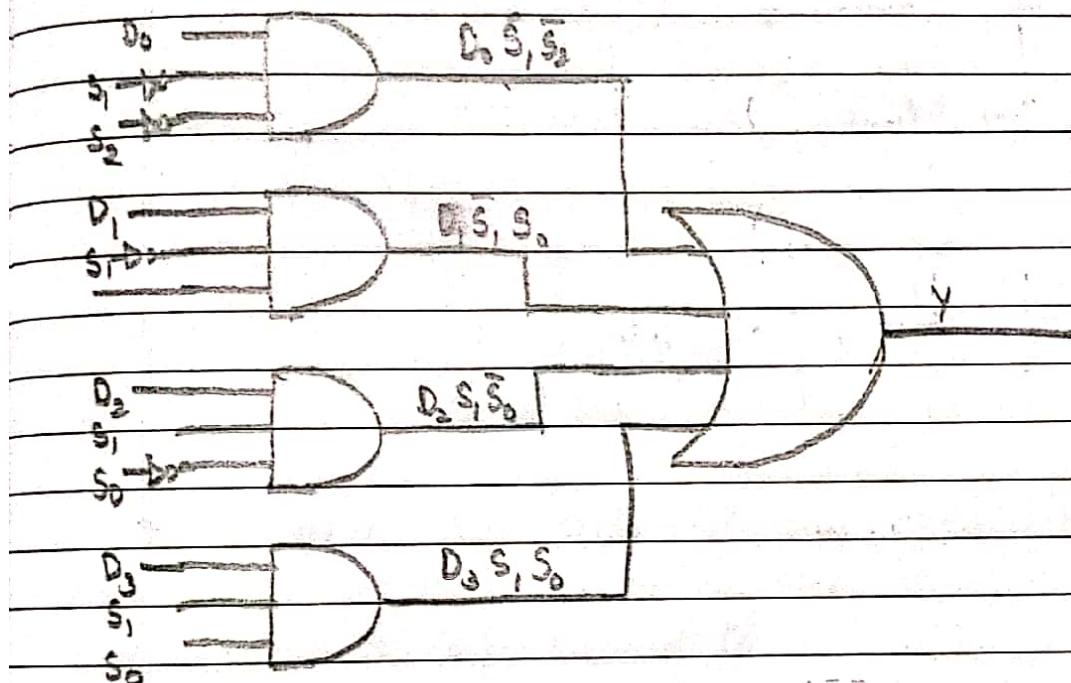
4 to 1 line multiplexer  
SYMBOL



## Truth Table

$S_1$	$S_2$	Output	$y$
0	0	$D_0$	
0	1	$D_1$	
1	0	$D_2$	
1	1	$D_3$	

$$y = D_0 \bar{S}_1 \bar{S}_2 + D_1 S_1 \bar{S}_2 + D_2 S_1 S_2 + D_3 \bar{S}_1 S_2$$



A 4:1 multiplexer requires 2 select lines  $S_0$  &  $S_1$ , which are decoded to select a particular and gate to send the data inputs  $D_0$  to  $D_3$ . Each of the 4 data input lines is applied to the respective and gate we can write the o/p Boolean exp.

$$y = D_0 \bar{S}_1 \bar{S}_2 + D_1 S_1 \bar{S}_2 + D_2 S_1 S_2 + D_3 \bar{S}_1 S_2$$

The data o/p  $y = D_0$  if & only if  $S_1 = 0$  &  $S_2 = 0$

The truth table lists the O/p to Q/p to O/p path for each possible bit combination of the select lines.

usually the multiplexer IC has an enabled O/p to control the operation of the unit

- ① Draw the sym bol logic diagram for the truth table of an 8:1 Mux & explain its working.

Date: / /

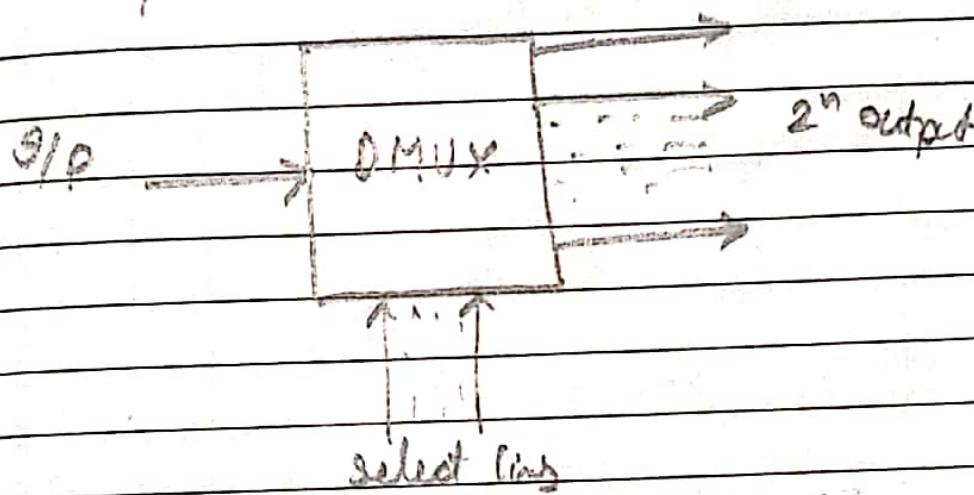
papergrid

## DeMultiplex [DEMUX]

Means 1 into many. De multiplexing is the process of taking info from one I/P and transmitting the same over several O/P's.

A DEMUX is a logic circuit that receives info on a single I/P and transmits the same over several O/P lines ( $2^n$ ).

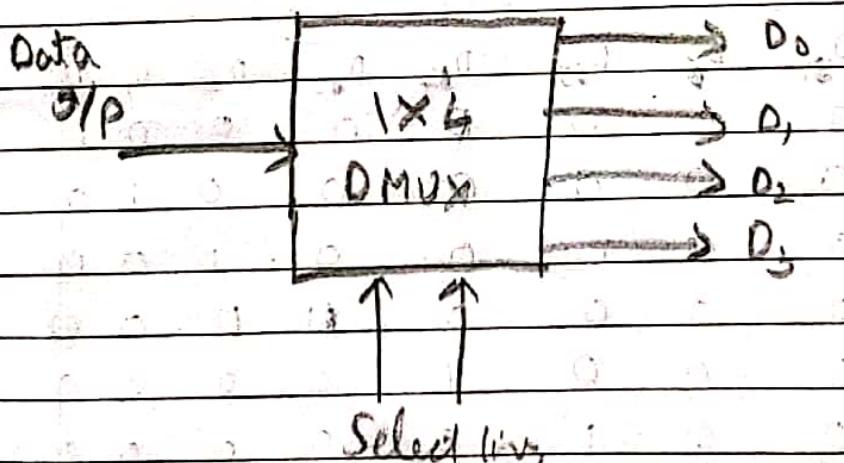
A DEMUX is the opposite of MUX action. The symbol can be shown as follows.



The select I/P code determines which O/P of the data will be transmitted as the serial data is changed into a parallel data. A DEMUX is also called as Data distributor.

## 1x4 DEMUX

### SYMBOL

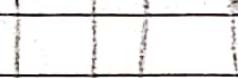


Input			Output	
$S_2$	$S_1$	$S_0$	D	$D_o$
0	0	0	0	1
0	1	0	0	0
1	0	0	1	0
1	1	1	0	0

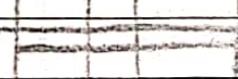
Data  $S_2, S_1, S_0$



DEMUX,  $S_2, S_1, S_0$



DEMUX,  $S_2, S_1, S_0$

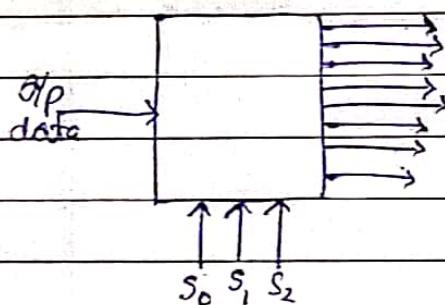


DEMUX,  $S_2, S_1, S_0$



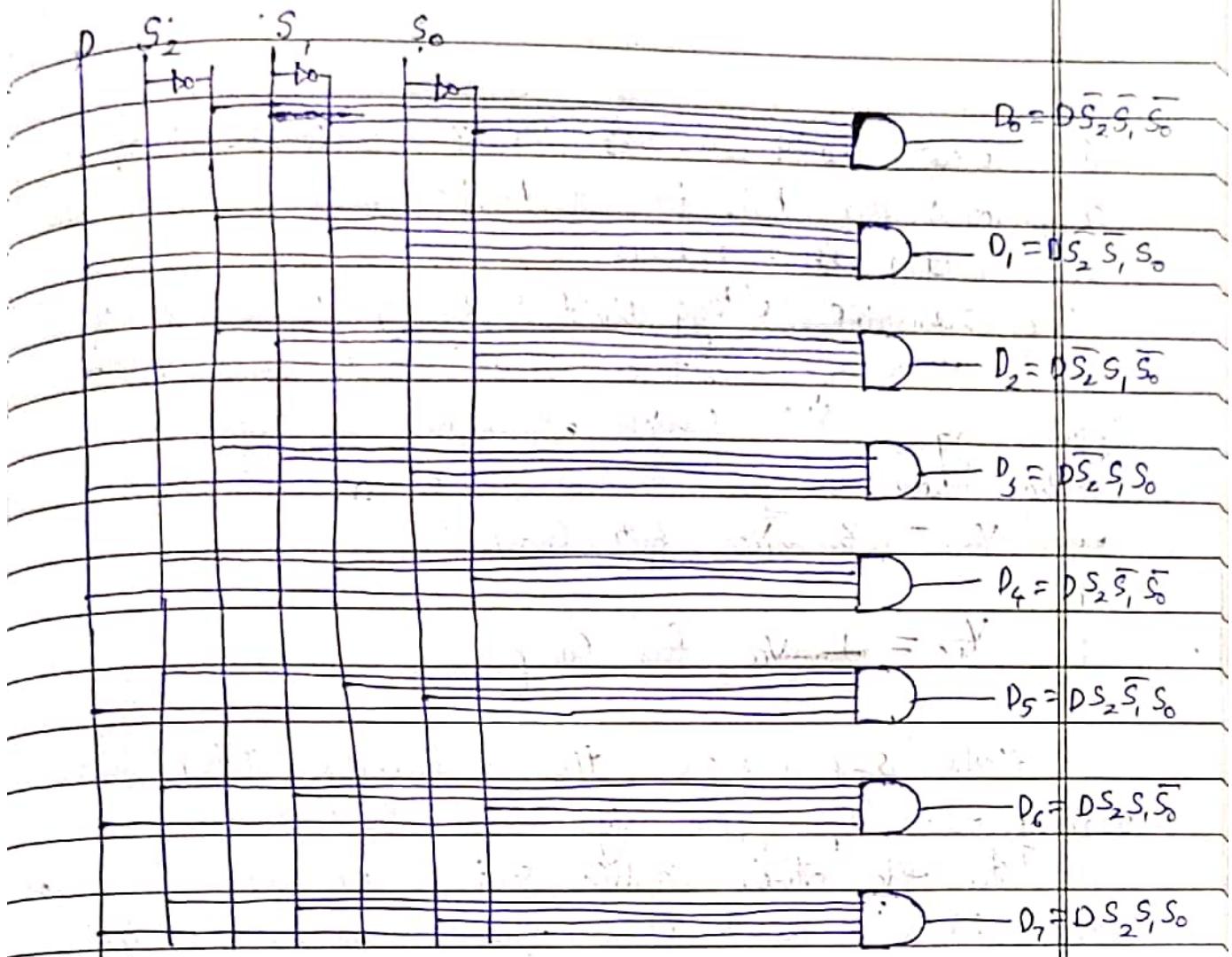
DEMUX,  $S_2, S_1, S_0$

Draw the symbol & logic diagram of 1:8 DMUX & explain its operation



$S_2$	$S_1$	$S_0$	$D_7$	$D_6$	$D_5$	$D_4$	$D_3$	$D_2$	$D_1$	$D_0$
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0

Date: 11/11/11



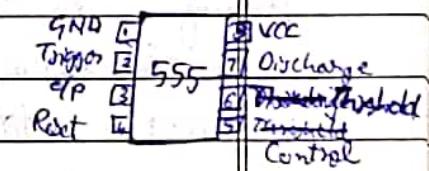
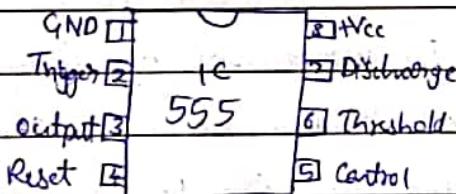
IC 555 Timer

What is an analogue IC & digital IC

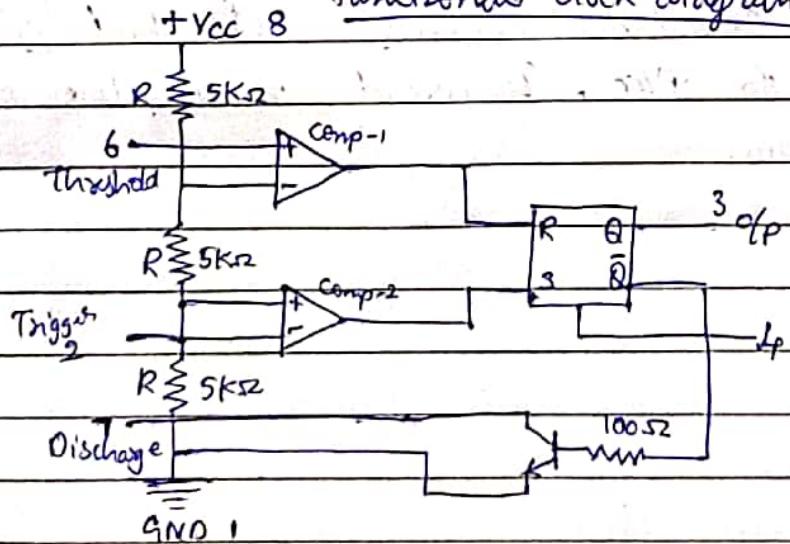
Analog IC  $\rightarrow$  741

Digital IC  $\rightarrow$  IC 555

IC 555  $\rightarrow$  oscillator



functional Block diagram



The circuit shows a 555 circuit which consists of 2 comparators, an RS FF and 1 transistor which operates as a switch. The resistor

The resistive voltage divider consists of 3 resistors of equal value of resistance ( $5k\Omega$ ). It is connected to power supply,  $V_{cc}$  which establishes the reference voltages for the comparators 1 & 2 as

$$\text{Comp-1} \quad V_{TH} = \frac{2}{3} V_{cc} \quad \text{for Comp-2}$$

$$V_{TC} = \frac{1}{3} V_{cc} \quad \text{for Comp-2}$$

When  $S=1$   $R=0$  the FF will Set to 1 which means the op-amp goes high and  $\bar{Q}=0$ .

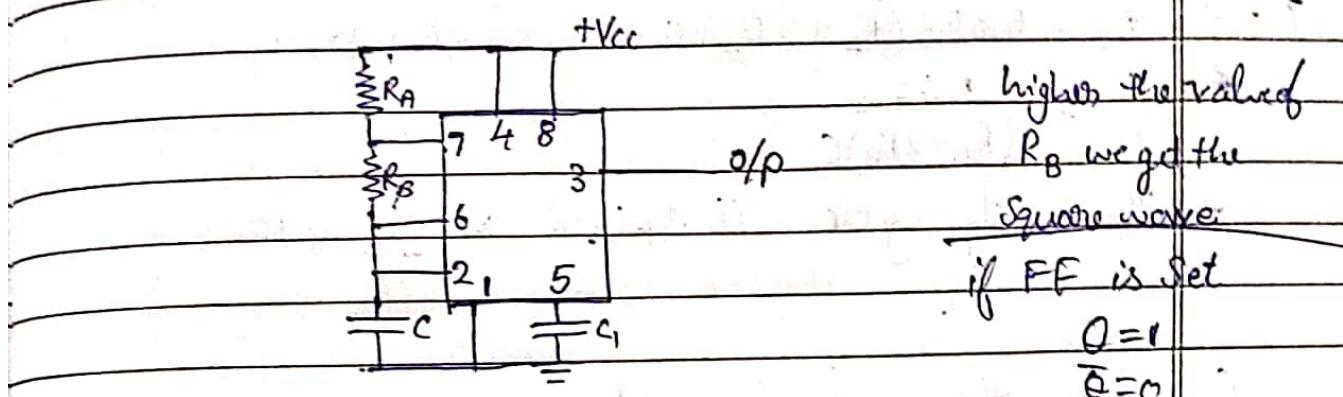
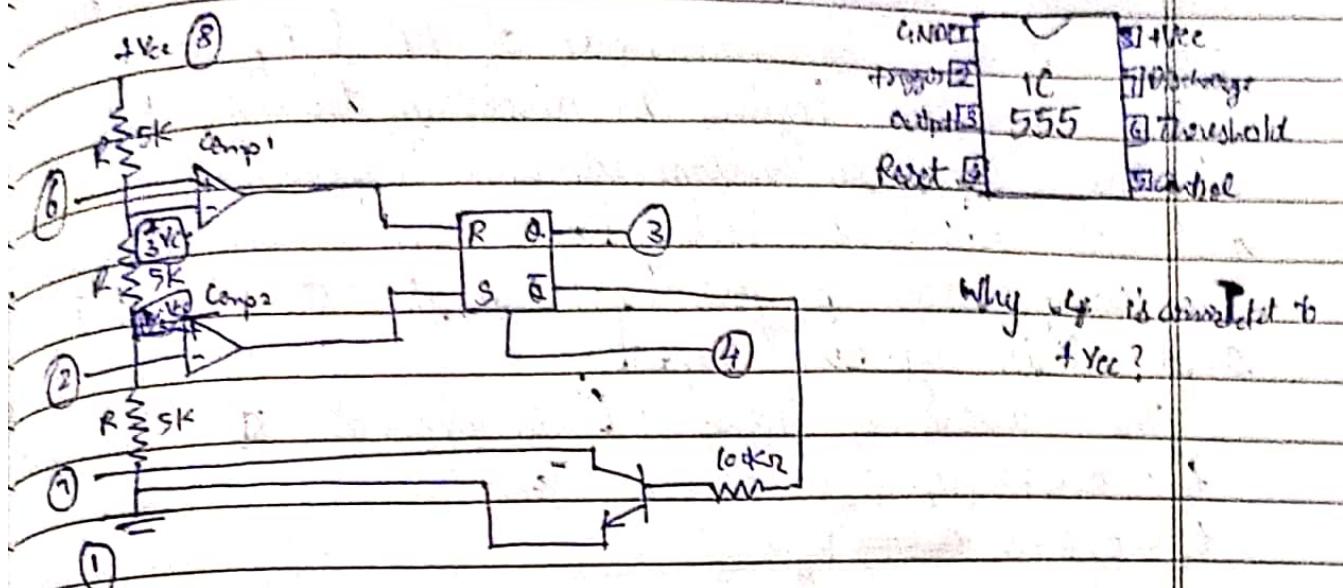
In the other stable state i.e. when  $S=0$   $R=1$  the FF will Reset to 0 which means the op-amp goes low &  $\bar{Q}=1$ .

The +ve Op terminal of Comp-1 is brought out to an external terminal of 555 package labelled as threshold.

Similarly the -ve Op terminal of Comp-2 is connected to an external terminal & labelled as trigger. The collector of transistor Q<sub>1</sub> is self-connected to an external terminal known as discharge.

There is a terminal known as reset which is always connected to +V<sub>cc</sub>. To avoid making the op-amp accidentally to zero.

# A Stable Multivibrator using IC 555



$$\begin{aligned} Q = 1 \\ Q = 0 \end{aligned}$$

The circuit diagram of a 555 IC working as an astable Multivibrator with two resistors  $R_A$  and  $R_B$  and an external capacitor  $C$  is as shown in the figure. Assume that the capacitor is fully discharged initially and the FF is in the Set condition i.e.  $Q=1$  and  $\bar{Q}=0$ . The transistor is at cutoff. The capacitor will charge <sup>up</sup> through the resistors  $R_A$  and  $R_B$  and the voltage across capacitor will rise exponentially towards  $+Vcc$ . When the voltage at pin no. 2 reaching the  $V_{TH}$  value  $\frac{1}{3}Vcc$  will not make any impact on the circuit operation. ∵ The FF remains in the Set condition when the capacitor voltage exceeds  $V_{TH} = \frac{1}{3}Vcc$  the output of Comp1 goes high which Resets the FF.

date: / / unfigured

i.e.  $\bar{Q}$  goes high and the transistor turned on. The saturated transistor causes the voltage to zero at the common node of  $R_A$  &  $R_B$  and the capacitor begins to discharge through  $R_B$ . The capacitor voltage decreases exponentially and will reach a value below  $V_{T1}$  which makes the comparator  $\bar{Q}$  goes high and sets the FF and this cycle repeats.

$$\text{The charging Time } t_1 \text{ is given as } 0.693(R_A + R_B)C$$

$$t_1 = 0.693(R_A + R_B)C \quad : \quad (T_1)$$

$$t_2 = 0.693 \cancel{R_A} R_B C$$

$$T = t_1 + t_2 = 0.693(R_A + 2R_B)C$$

$$f = \frac{1}{T} = \frac{1.445}{(R_A + 2R_B)C}$$

$\therefore$  The duty cycle is defined as  $\frac{t_1}{T} \times 100$

Calculate the ~~f~~ & Duty cycle output produced by 555 IC

$$R_A = 27\text{ k}\Omega$$

$$R_B = 56\text{ k}\Omega$$

$$C = 0.01\mu\text{F}$$

$$V_{CC} = 5\text{V}$$

$$f = \frac{1}{T} = \frac{1.445}{(27\text{k} + 2 \times 56\text{k}) 0.01 \times 10^{-6}} \quad T = 0.963 \times 10^{-3}$$

$$= 1039.5 \text{ Hz}$$

$$D = \frac{0.575 \times 10^{-3}}{0.963 \times 10^{-3}} \times 100$$

$$t_1 = 0.693(R_A + R_B)C$$

$$= 0.693(27\text{k} + 56\text{k}) 0.01 \times 10^{-6}$$

$$= 0.575 \times 10^{-3}$$

$$t_2 = 0.693 \times 56 \times 10 \times 0.01$$

$$= 0.388 \times 10^{-3}$$

Designs Astable timer using 555 with  
 $f = 50 \text{ KHz}$  60% duty cycle given  $C = 0.002 \mu\text{F}$

$$R_A = ?$$

$$D = \frac{t_1}{T}$$

$$R_B = ?$$

$$T$$

$$T = t_1 + t_2$$

$$f = \frac{1}{T}$$

$$T = \frac{1}{f} = \frac{1}{50 \text{ K}} = 0.02 \times 10^{-3}$$

$$D = \frac{t_1 \times 100}{T} \Rightarrow t_1 = D T = \frac{60}{100} \times 0.02 \times 10^{-3} = 1.2 \times 10^{-3}$$

$$T = t_1 + t_2$$

$$t_1 = 0.012 \times 10^{-3}$$

$$t_2 = T - t_1 = 0.02 \times 10^{-3} - 1.2 \times 10^{-3} = 0.012 \times 10^{-3}$$

$$t_2 = 0.008 \times 10^{-3}$$

$$\Rightarrow t_2 = 0.693 (R_B) C$$

$$R_B = \frac{t_2}{0.693 \times C} = \frac{0.008 \times 10^{-3}}{0.693 \times 0.002 \times 10^{-6}}$$

$$= 5.77 \times 10^3$$

$$R_B = 5.77 \text{ k}\Omega$$

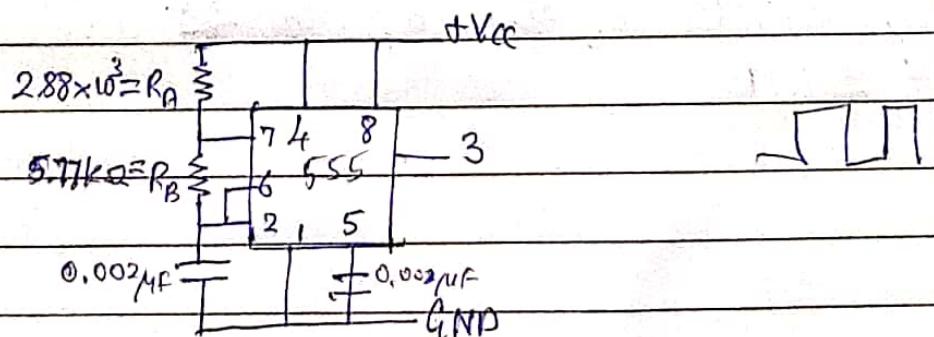
$$\Rightarrow t_1 = 0.693 (R_A + R_B) C$$

$$\frac{0.012 \times 10^{-3}}{0.002 \times 10^{-6} \times 0.693} = R_A + 5.77 \text{ k}\Omega$$

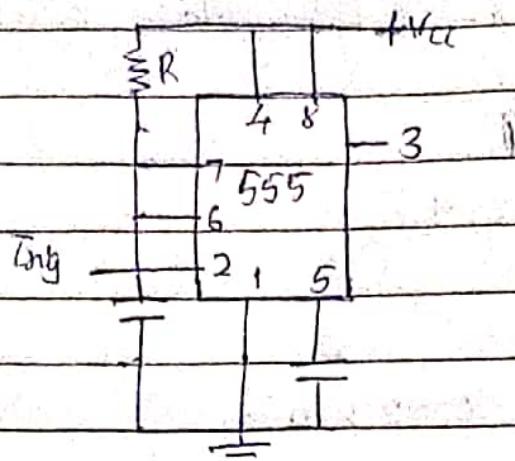
$$8.65 \times 10^3 = R_A + 5.77 \text{ k}\Omega$$

$$8.65 \times 10^3 - 5.77 \times 10^3 = 2.88 \times 10^3 \text{ k}\Omega$$

$$R_A = 2.88 \times 10^3$$

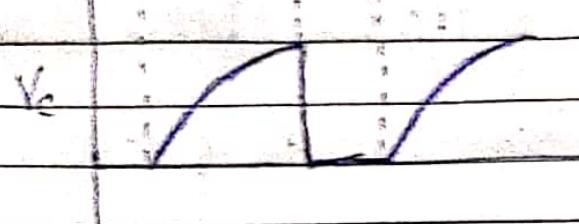
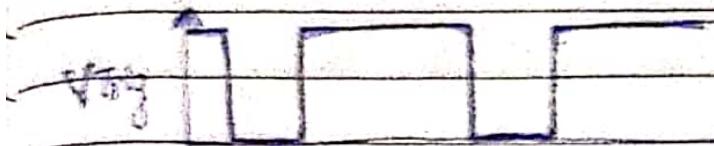


## Monostable Multivibrator



The circuit diagram of a Monostable Multivibrator using IC 555 is as shown in the figure. The external components are R and C. In the stable state the FF is reset.  $Q=0$  and  $\bar{Q}=1$ , and hence the transistors turns ON i.e. capacitor voltage = 0. The voltage at the trigger 2/p is kept high and  $\therefore$  the o/p of the comparator is low. To trigger the Multivibrator  $+ve$  pulse is applied to the trigger 2/p which makes the comparator 2 goes to high state thus setting the FF i.e.  $Q=1$  &  $\bar{Q}=0$ , turning off the transistors i.e. the capacitor begins to charge up through the resistance R and its value rises towards  $+VCC$ . The multivibrator is in the ~~transient~~ quasi state. When the  $V_c$  reaches above the threshold voltage the o/p of the comparator goes high resetting the FF turning on the transistors causing the capacitor to discharge. Now the Multivibrator is back in the stable state & ready to receive a new triggering pulse. The pulse width of the o/p can be given by.

$$t_p = 1.1RC$$



Ques

1. What is a half adder? write its TT & logic circuit with logic expression.

2. — U — half subtractor — U —

3. Illustrate the operation of n bit parallel adder with the help of a block diagram design a full adder circuit with TT & logic expression.

④ Design a Full adder circuit with TT & logic circuit & logic expression.

⑤ Design a truth table for 1 bit magnitude comparator.

⑥ Write expression for its output & draw logic circuit

⑦ With the help of a TT Design a Full subtractor circuit using logic gates.

⑧ Design a 2 bit magnitude comparator with the help of a TT & logic expression also draw the logic diagram using suitable gate.

⑨ Design a Full adder circuit using 2 HA's & An OR gate basic gates. With the TT & logic expression.

⑩ What is a decoder make a TT for slim to slim decoder and the expression for the output.

⑪ What is an encode make a TT for a decimal to BCD encoder & briefly explain its operation.

- (12) Draw the logic diagram of an octal to Binary encoder & write its T.T
- (13) Draw the logic diagram of BCD to Seven Segment decoder
- (14) Explain the working of 4:1 Multiplexer with T.D & a T.T.
- (15) What is a DMUX Draw a 1:4 line DMUX & also write its T.T.
- (16) Explain the internal connections/Construction of IC 555 with a block diagram.
- (17) Draw a neat labelled internal block diagram of IC 555
- (18) What is a Multivibrator circuit. Explain the working of mono stable Multivibrator with wave forms.
- (19) Explain the working of astable Multivibrator using IC 555  
Draw the necessary ~~time~~ waveforms.
- (20) Why is meant by Duty Cycle of an astable multivibrator? Is it possible to have a perfect square wave in an IC 555 as an astable multivibrator?
- (21) Draw the pin out diagram of IC 555 & explain the function of each Pin