

# EE386 – RESISTOR TRANSISTOR LOGIC

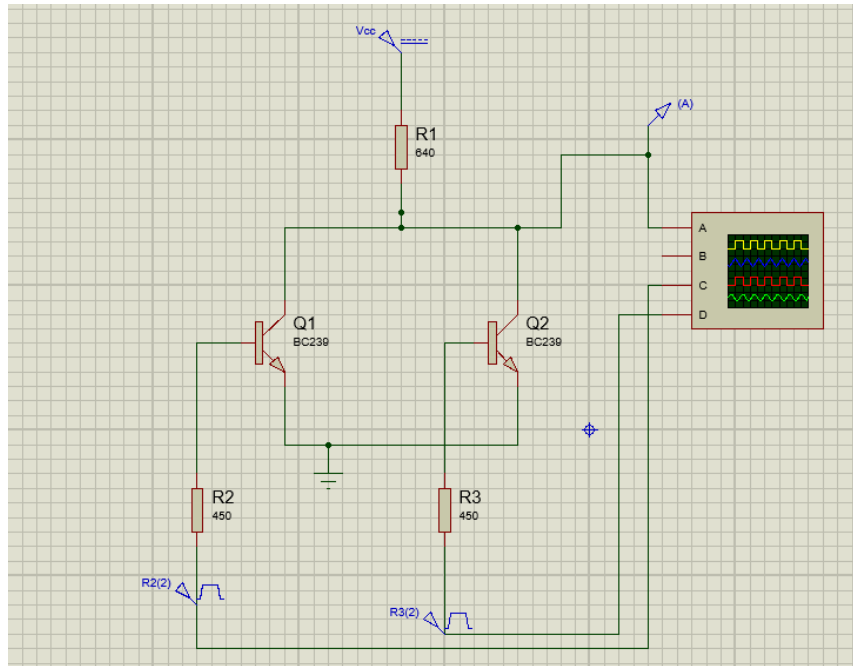
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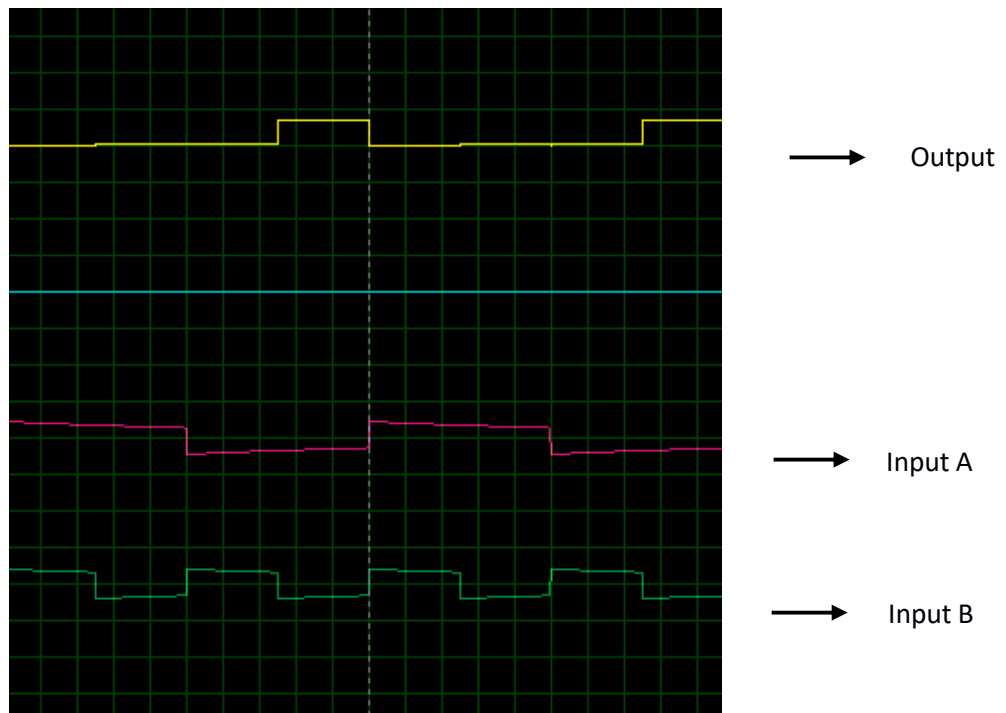
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## 1) Schematic implementation



2)

a)



b)

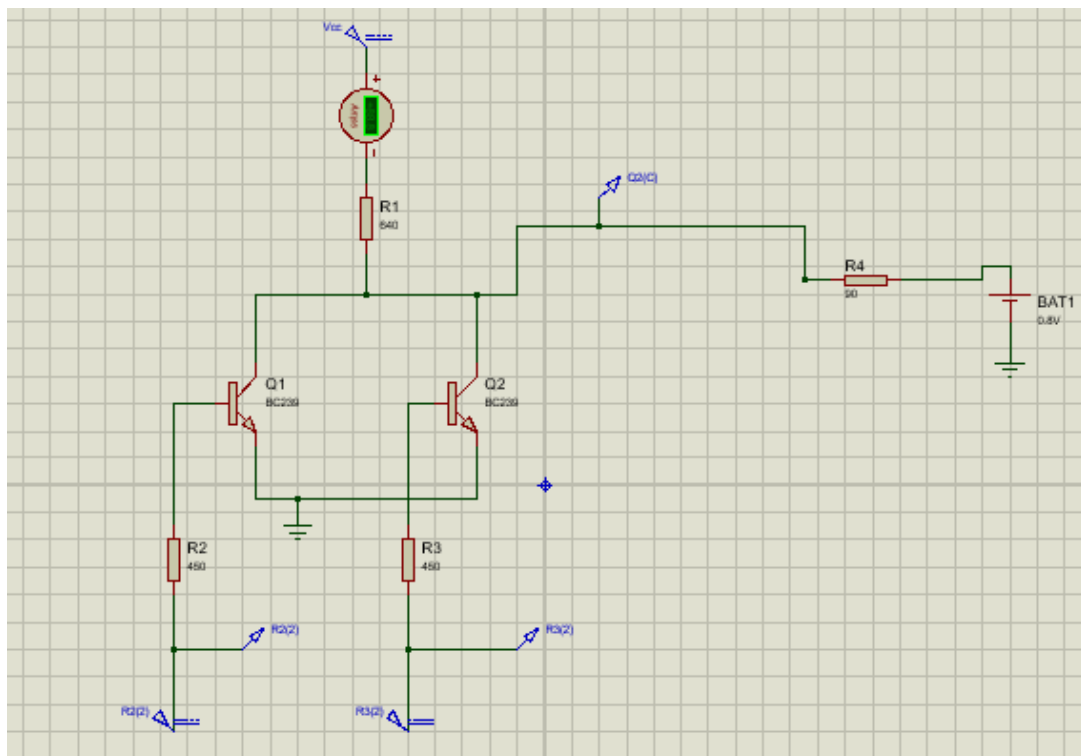
$V_A / V$	$V_B / V$	$V_o / V$
0.2	0.2	3.6
3.6	0.2	0.2
0.2	3.6	0.2
3.6	3.6	0.2

Output values of the RTL circuit is similar to the output values of a NOR gate

$V_A / V$	$V_B / V$	$V_o / V$
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate truth table

3)



a) For logic "LOW"  $\rightarrow$  Output voltage : 1.14521 V

For logic "HIGH"  $\rightarrow$  Output voltage : 0.198535 V

b) i) When output is at logic 'LOW'  $I_C = 5.32 \text{ mA}$

$$\begin{aligned}\text{power drawn by the circuit from the supply} &= 3.6 \times 5.32 \\ &= 19.152 \text{ mW}\end{aligned}$$

ii) When output is at logic 'LOW'  $I_C = 3.84 \text{ mA}$

$$\begin{aligned}\text{power drawn by the circuit from the supply} &= 3.6 \times 3.84 \\ &= 13.824 \text{ mW}\end{aligned}$$

c) For Logic "Low"

For RTL,  $V_{\text{out,low}} = 0.2 \text{ V} \rightarrow V_{\text{OL}} = 0.2 \text{ V}$

When  $V_A \geq$  cut in voltage of  $T_A$ ,  $T_B$  will start to conduct

Cut in voltage = 0.5 V  $\rightarrow V_{\text{IL}} = 0.5 \text{ V}$

$$\Delta L = V_{\text{IL}} - V_{\text{OL}} = 0.5 - 0.2 = 0.3 \text{ V}$$

For Logic "HIGH"

$V_O$  will depends on N ,

For N = 5;  $V_O = 1.1452 \text{ V} \rightarrow V_{\text{OH}} = 1.1452 \text{ V}$

$V_{\text{IH}}$  is minimum  $V_O$ , that can keep next stage transistors still in saturation.

For saturation :

$$\beta I_B > I_C$$

$$I_B > \frac{I_C}{\beta}$$

Let  $\beta = 30$ ,

$$V_{\text{CC}} = I_C R_C + V_{\text{CE,sat}}$$

$$I_C = (3.6 - 0.2) / 640 = 5.31 \text{ mA}$$

So  $I_{\text{C,max}} = 5.31 \text{ mA}$

$$I_B > 5.31 / 30 = 0.177 \text{ mA}$$

$$I_{\text{B,min}} = 0.177 \text{ mA}$$

$$V_{\text{out,min}} (V_{\text{IH}}) = I_{\text{B,min}} \times R_B + V_{\text{BE,sat}} = 0.177 \times 0.45 + 0.8 = 0.88 \text{ V}$$

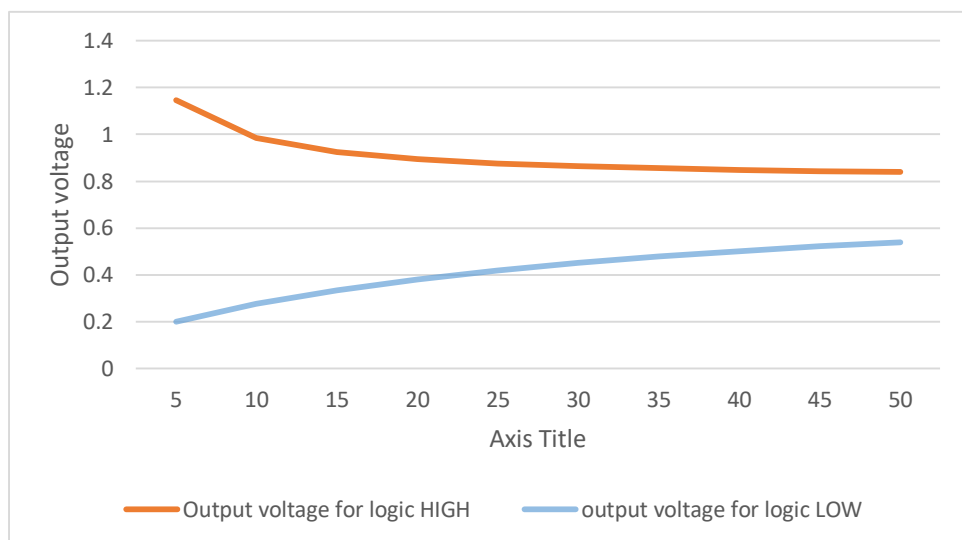
$$V_{\text{IH}} = 0.88 \text{ V}$$

$$V_{\text{OH}} = 1.1452 \text{ V}$$

$$\Delta H = V_{\text{OH}} - V_{\text{IH}} = 1.1452 - 0.88 = 0.27 \text{ V}$$

4) A)

Number of load gates	Output voltage for logic LOW	Output voltage for logic HIGH
5	0.198535	1.14521
10	0.274765	0.983942
15	0.33376	0.925373
20	0.380797	0.895094
25	0.41919	0.876596
30	0.451126	0.864122
35	0.478073	0.855142
40	0.501217	0.848369
45	0.521224	0.843077
50	0.538717	0.838829



B)  $V_{IL} = 0.5V$  and  $V_{IH} = 0.88V$

Number of load gates	Low level noise margin (V)	High level noise margin (V)
	$\Delta L = V_{IL} - V_{OL}$	$\Delta H = V_{OH} - V_{IH}$
5	0.303155	0.26521
10	0.226999	0.103942
15	0.167998	0.045373
20	0.120918	0.015094
25	0.082466	-0.003404
30	0.050465	-0.015878
35	0.023413	-0.024858
40	0.000243	-0.031631
45	-0.019825	-0.036923
50	-0.037377	-0.041171

