

## GATE

1. For the given digital circuit,  $A = B = 1$ . Assume that AND, OR, and NOT gates have propagation delays of 10 ns, 10 ns, and 5 ns respectively. All lines have zero propagation delay. Given that  $C = 1$  when the circuit is turned on, the frequency of steady-state oscillation of the output  $Y$  is \_\_\_\_\_.

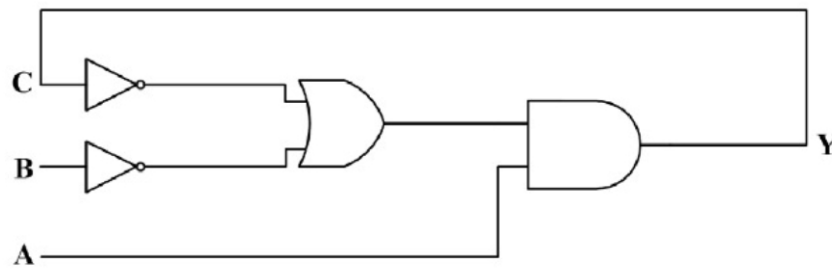


Figure 1: Image

- (a) 20 MHz
- (b) 15 MHz
- (c) 40 MHz
- (d) 50 MHz