GATE IN 2022

November 29, 2023

1. In the circuit diagram shown below, the logic gates operate with a supply voltage of 1 V. NAND and XNOR have 200 ps and 400 ps input-to-output delay, respectively.

   At time $t = T$, $A(t) = 0$, $B(t) = 1$ and $Z(t) = 0$. When the inputs are changed to $A(t) = 1$, $t = 2T$, a 1 V pulse is observed at Z. The pulse width of the 1 V pulse is _____ ps.

   (GATE IN 2022)

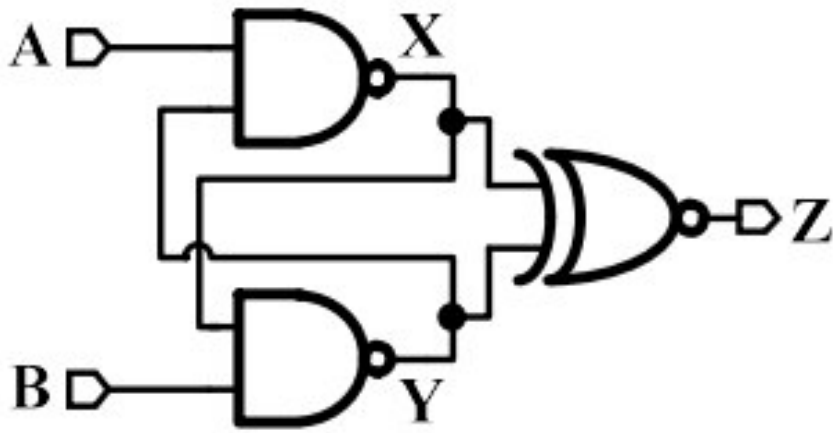

Figure 1: circuit

(a) 100

(b) 400

(c) 200

(d) 600

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