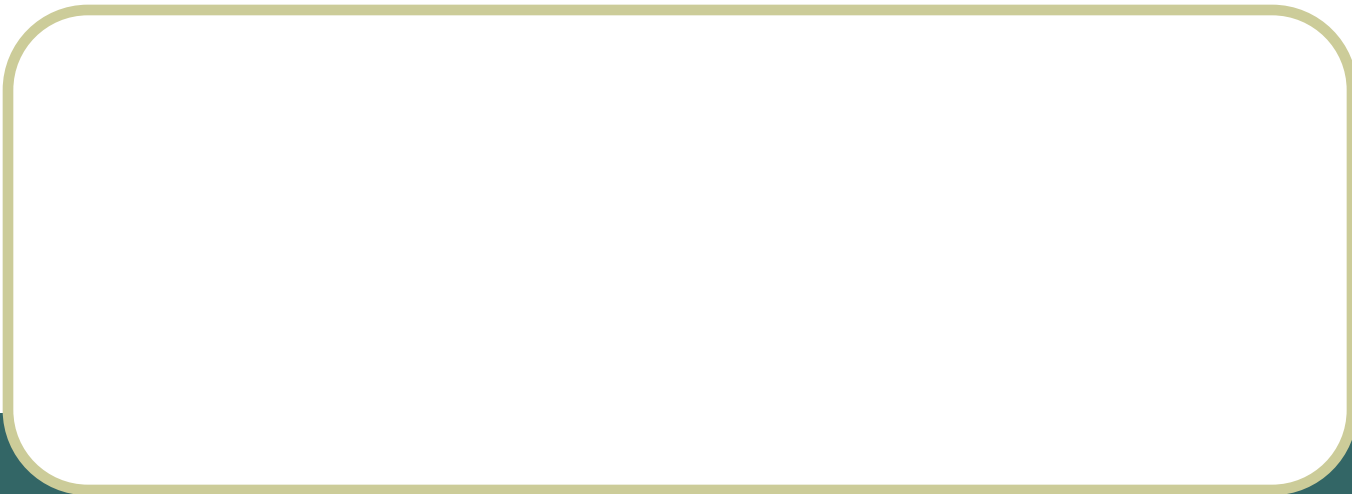


TIMING DIAGRAM OF 8085



TIMING DIAGRAM

- Timing Diagram is a graphical representation.
- It represents the execution time taken by each instruction in a graphical format.
- The execution time is represented in T-states.

CONTROL SIGNALS

IO/M (Active Low)	S1	S2	Data Bus Status (Output)
0	0	0	Halt
0	0	1	Memory WRITE
0	1	0	Memory READ
1	0	1	IO WRITE
1	1	0	IO READ
0	1	1	Opcode fetch
1	1	1	Interrupt acknowledge

INSTRUCTION CYCLE

- The time required to execute an instruction is called instruction cycle.

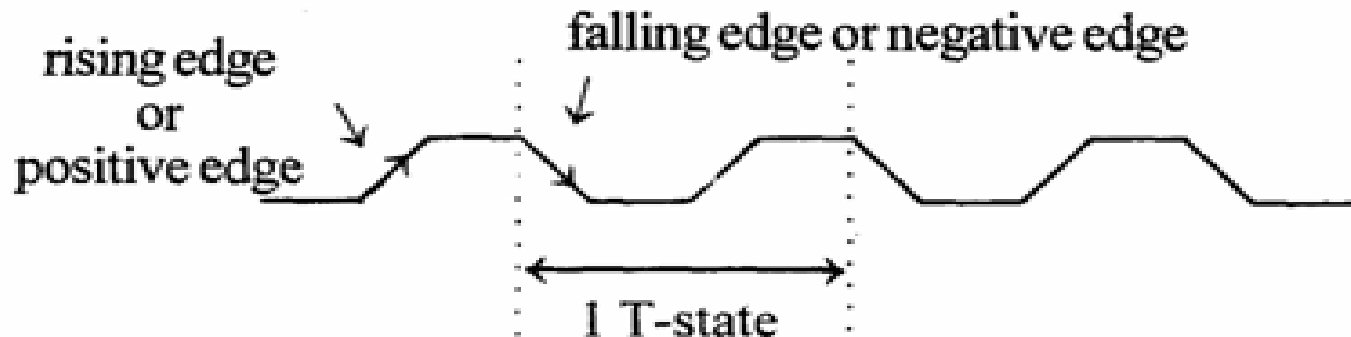
MACHINE CYCLE

- The time required to access the memory or input/output devices is called machine cycle.

T-STATE

- The machine cycle and instruction cycle takes multiple clock periods.
- A portion of an operation carried out in one system clock period is called as T-

Note : Time period, $T = 1/f$; where f = Internal clock frequency



MACHINE CYCLES OF 8085

The 8085 microprocessor has 5 basic machine cycles.

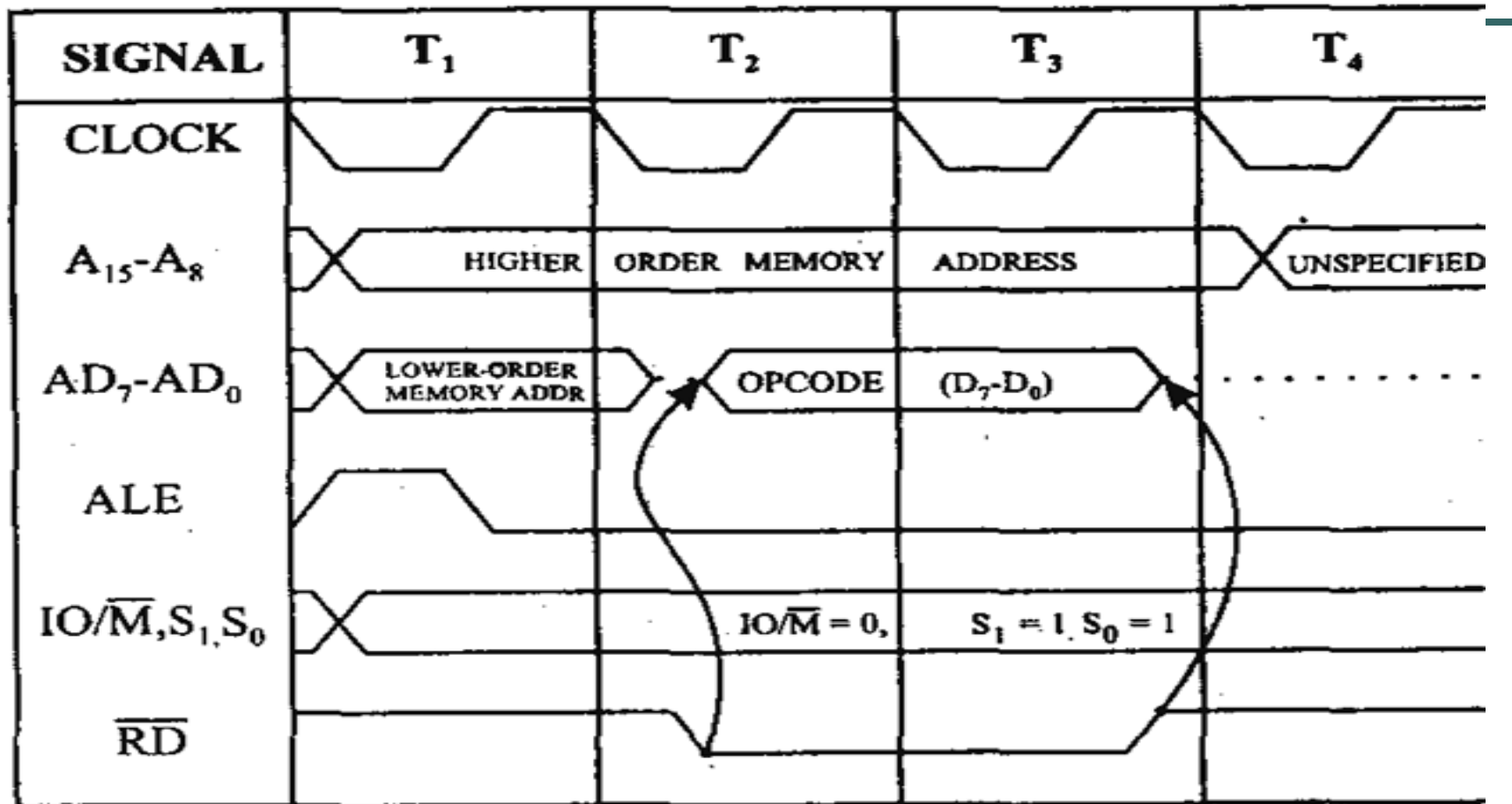
They are

1. Opcode fetch cycle (4T)
2. Memory read cycle (3 T)
3. Memory write cycle (3 T)
4. I/O read cycle (3 T)
5. I/O write cycle (3 T)

MACHINE CYCLES OF 8085

- The processor takes a definite time to execute the machine cycles. The time taken by the processor to execute a machine cycle is expressed in T-states.
- One T-state is equal to the time period of the internal clock signal of the processor.
- The T-state starts at the falling edge of a clock.

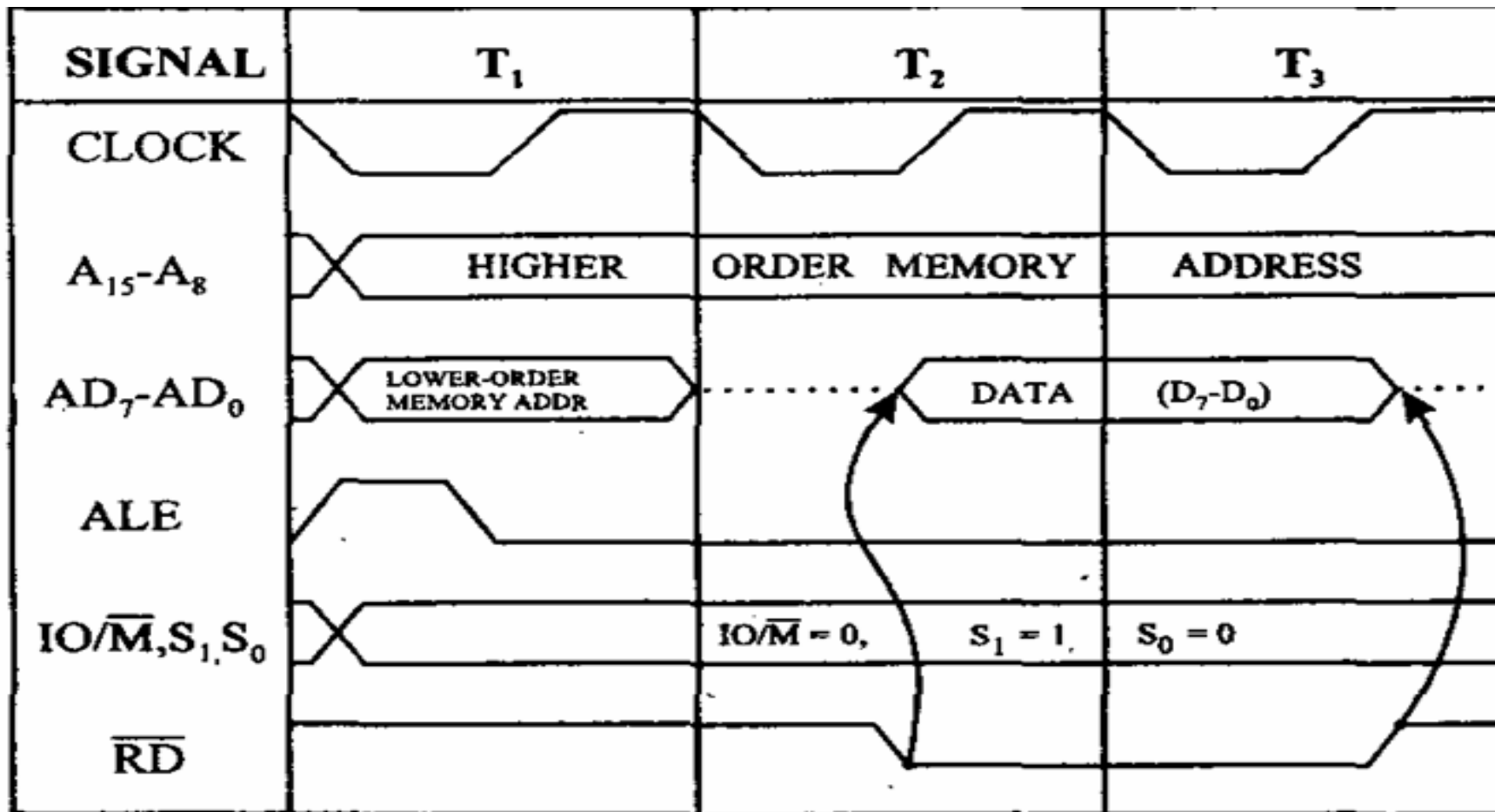
OPCODE FETCH MACHINE CYCLE OF 8085



OPCODE FETCH MACHINE CYCLE OF 8085

- Each instruction of the processor has one byte opcode.
- The opcodes are stored in memory. So, the processor executes the opcode fetch machine cycle to fetch the opcode from memory.
- Hence, every instruction starts with opcode fetch machine cycle.
- The time taken by the processor to execute the opcode fetch cycle is $4T$.
- In this time, the first, 3 T-states are used for fetching the opcode from memory and the remaining T-states are used for internal operations by the processor.

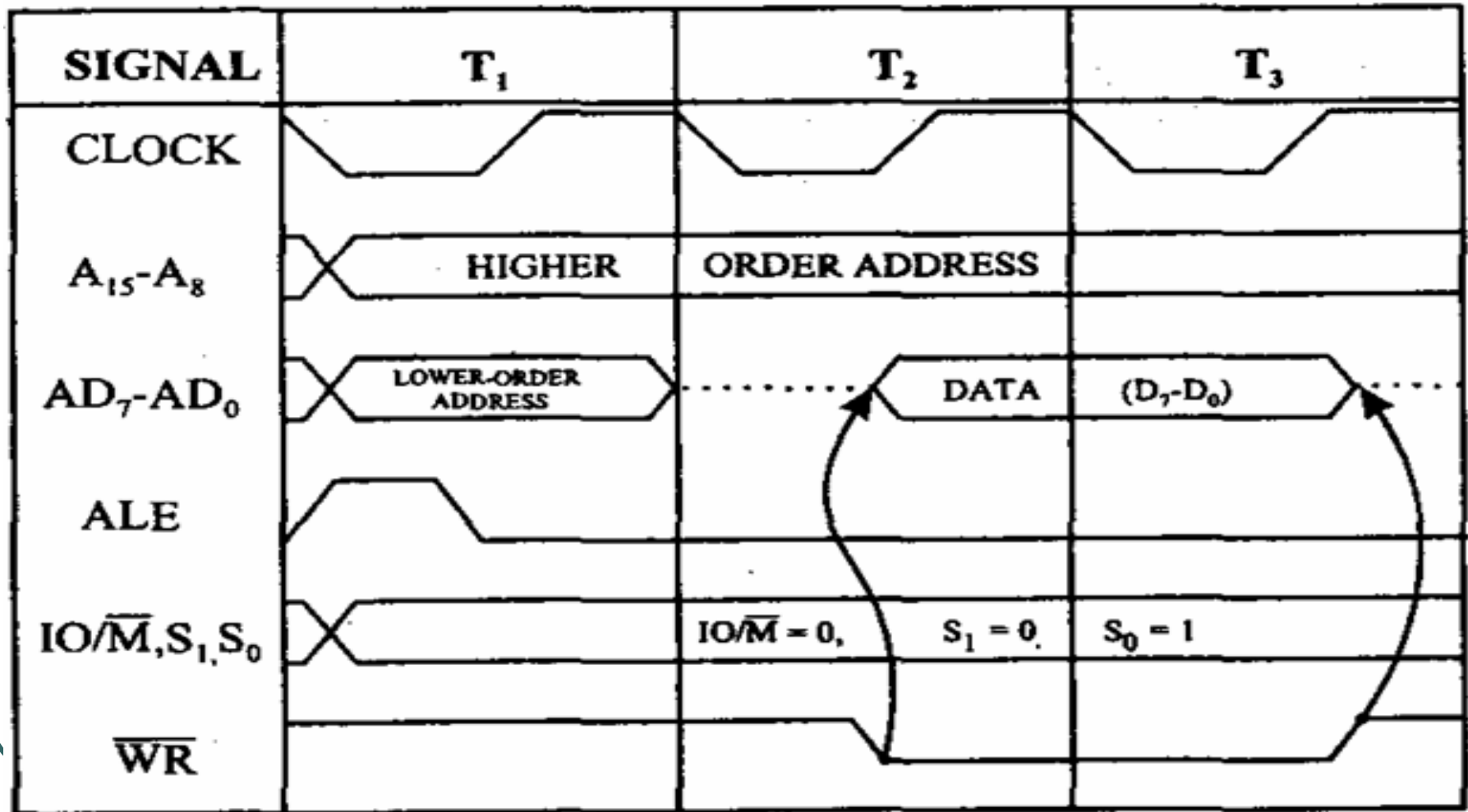
MEMORY READ MACHINE CYCLE OF 8085



MEMORY READ MACHINE CYCLE OF 8085

- The memory read machine cycle is executed by the processor to read a data byte from memory.
- The processor takes 3T states to execute this cycle
- The instructions which have more than one byte word size will use the machine cycle after the opcode fetch machine cycle.

MEMORY WRITE MACHINE CYCLE OF 8085



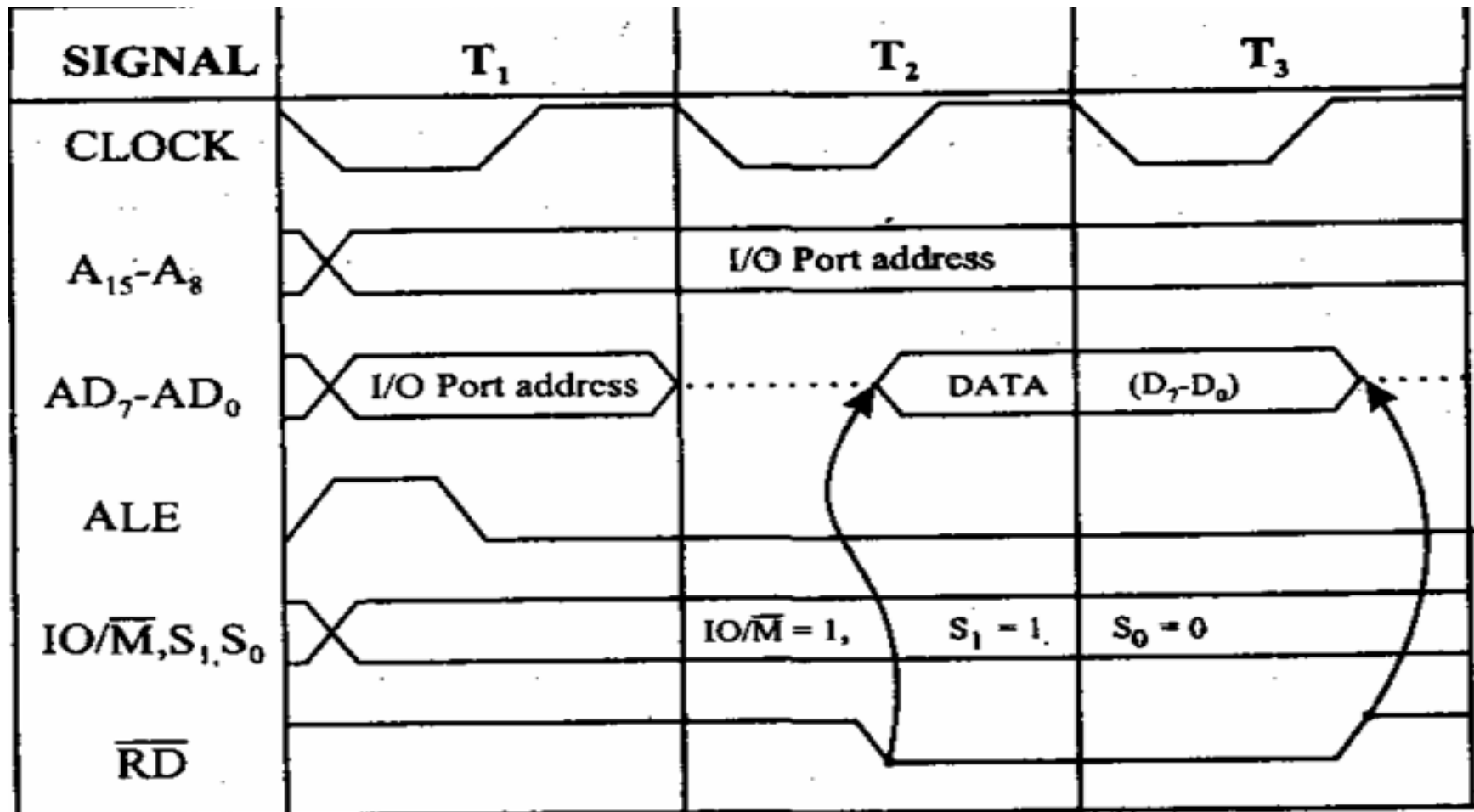
MEMORY WRITE MACHINE CYCLE OF 8085

- The memory write machine cycle is executed by the processor to write a data byte in a memory location.
- The processor takes, 3T states to execute this machine cycle

I/O READ CYCLE OF 8085

- The I/O Read cycle is executed by the processor to read a data byte from I/O port or from the peripheral.
- The processor takes 3T states to execute this machine cycle.
- The IN instruction uses this machine cycle during the execution.

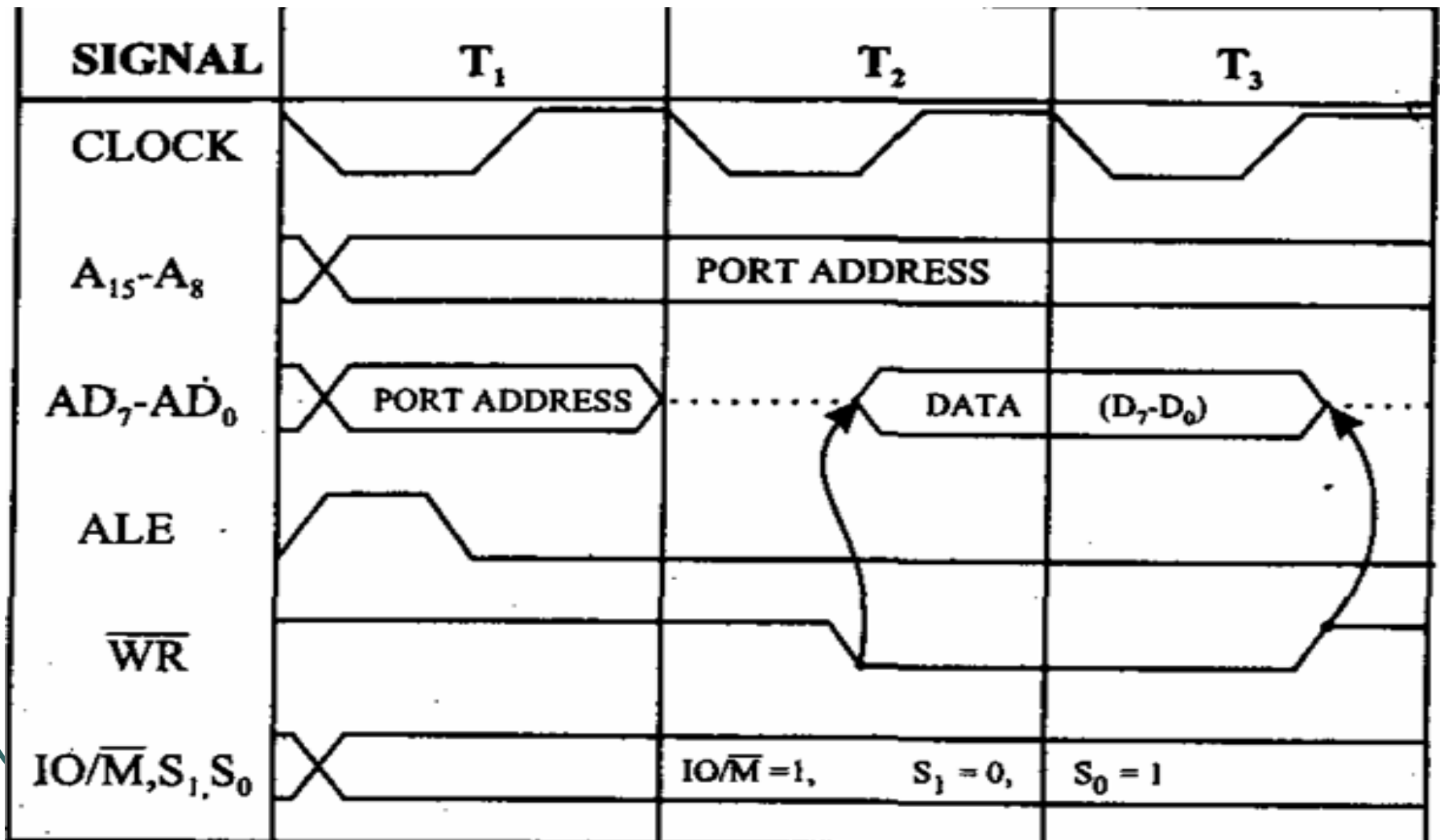
I/O READ CYCLE OF 8085



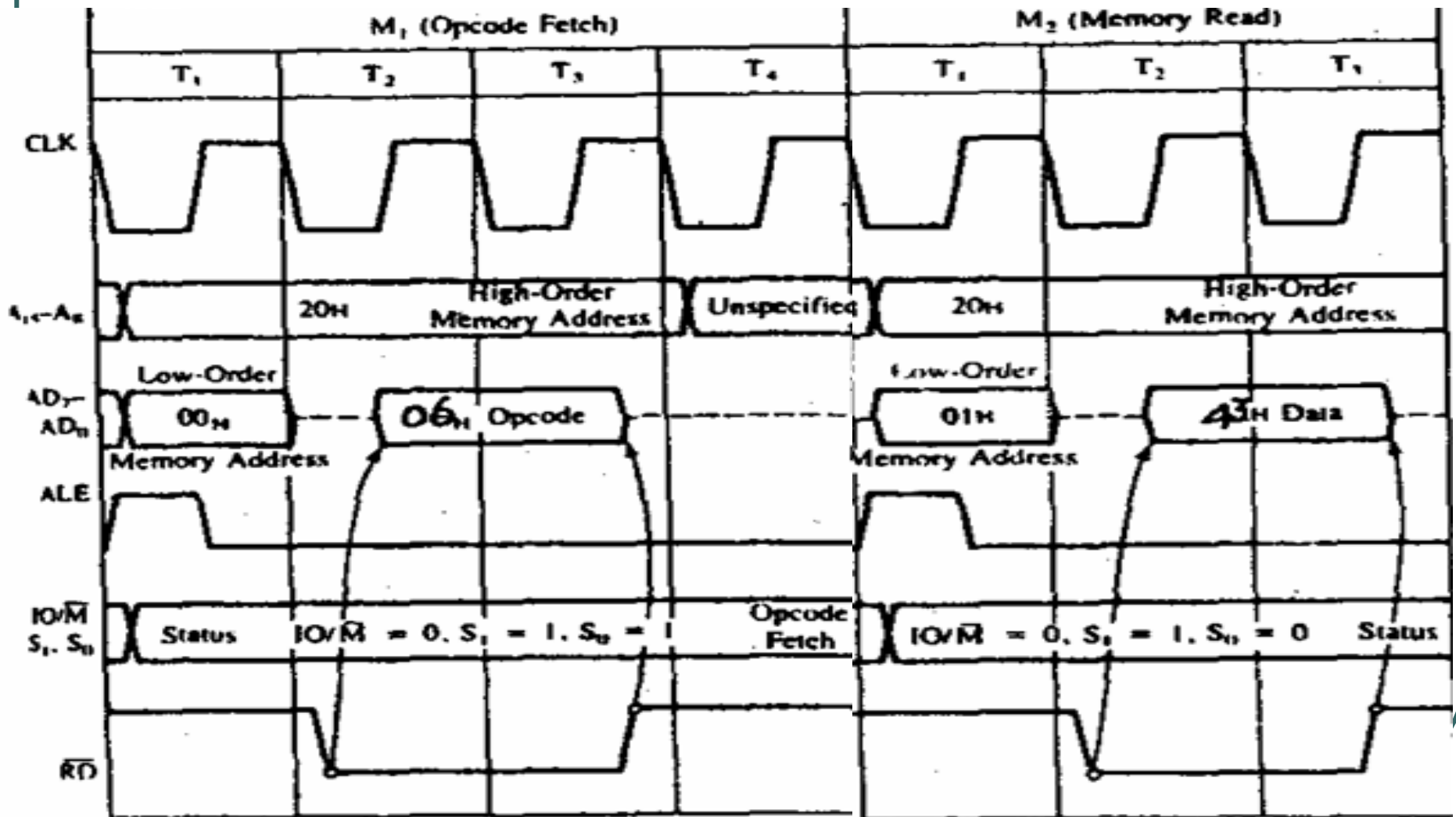
I/O WRITE CYCLE OF 8085

- The I/O write machine cycle is executed by the processor to write a data byte in the I/O port or to a peripheral, which is I/O, mapped in the system.
- The processor takes, 3T states to execute this machine cycle.

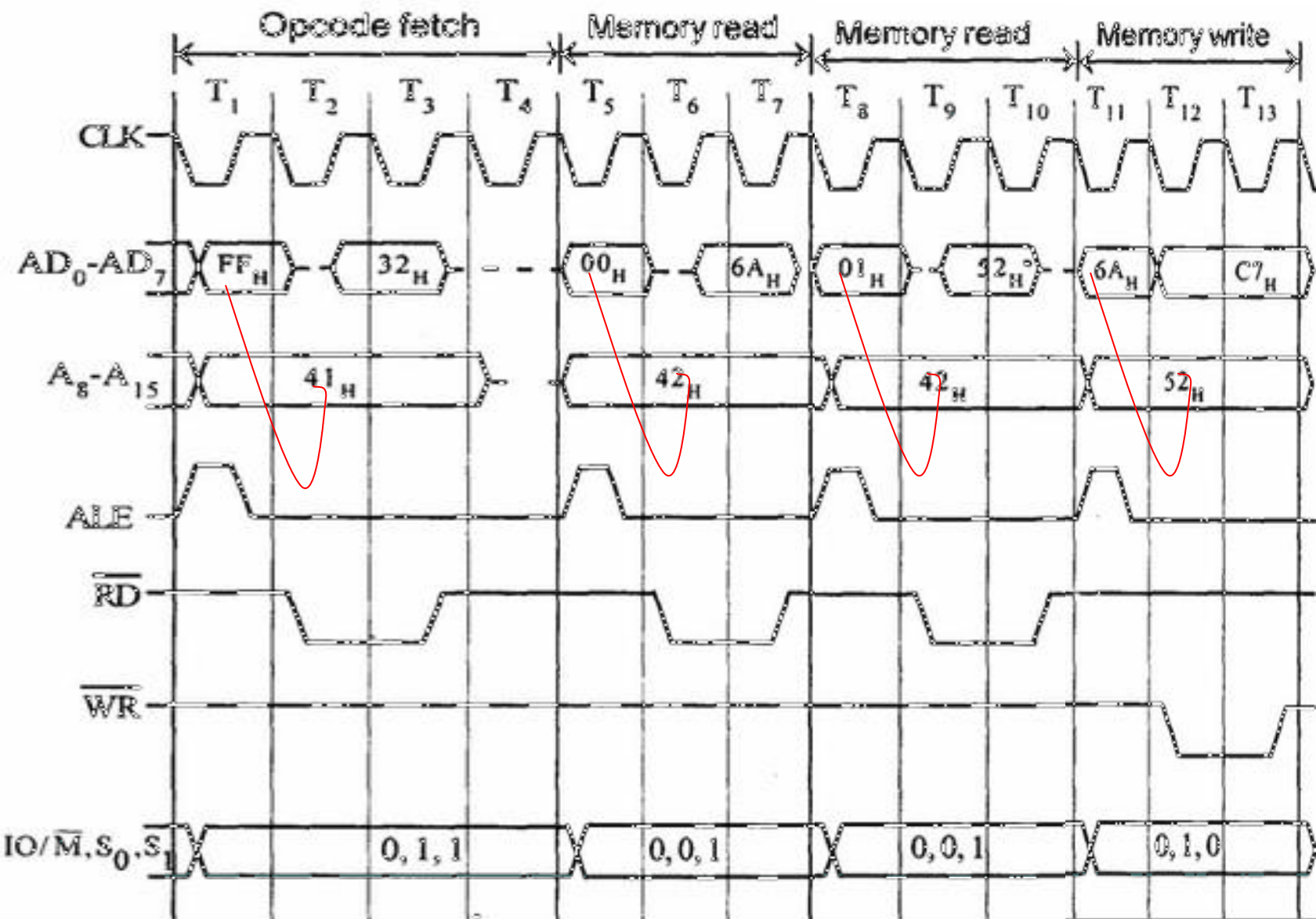
I/O WRITE CYCLE OF 8085



EXAMPLE INSTRUCTION : MVI B, 43



EXAMPLE INSTRUCTION : STA 526A



Decoding of multilexed address lines

