TIMING DIAGRAM

Timing diagram is the display of initiation of read/write and transfer of data operations under the control of 3-status signals IO / M, S1, and S0. All actions in the microprocessor are controlled by either leading or trailing edge of the clock.

MACHINE CYCLE

It is the time required by the microprocessor to complete the operation of accessing the memory devices or I/O devices. In machine cycle various operations like opcode fetch, memory read, memory write, I/O read, I/O write are performed.

T-STATE

Each clock cycle is called as T-states.

Each machine cycle is composed of many clock cycles. Since, the data and instructions, both are stored in the memory, the µP performs fetch operation to read the instruction or data and then execute the instruction. The 3-status signals: IO / M, S1, and S0 are generated at the beginning of each machine cycle. The unique combination of these 3-status signals identify read or write operation and remain valid for the duration of the cycle.

Table 1 Machine Cycle Status And Control Signals

	Status			*Controls*		
Machine cycle	IO / $\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch (OF)	0	1	1	0	1	1
Memory Read	0	1	0	0	1	1
Memory Write	0	0	1	1	0	1
I/O Read (I/OR)	1	1	0	0	1	1
I/O Write (I/OW)	1	0	1	1	0	1
Acknowledge of INTR (INTA)	1	1	1	1	1	0
BUS Idle (BI) : DAD	0	1	0	1	1	1
ACK of RST, TRAP	1	1	1	1	1	1
HALT	Z	0	0	Z	Z	1
HOLD	Z	X	X	Z	Z	1

X ⇒ Unspecified, and Z ⇒ High impedance state

Table1 shows details of the unique combination of these status signals to identify different machine cycles. Thus, time taken by any µP to execute one instruction is calculated in terms of the clock period. The execution of instruction always requires read and writes operations to transfer data to or from the µP and memory or I/O devices. Each read/ write operation constitutes one machine cycle (MC1) as indicated in Fig.1.7. Each machine cycle consists of many clock periods/ cycles, called T-states.

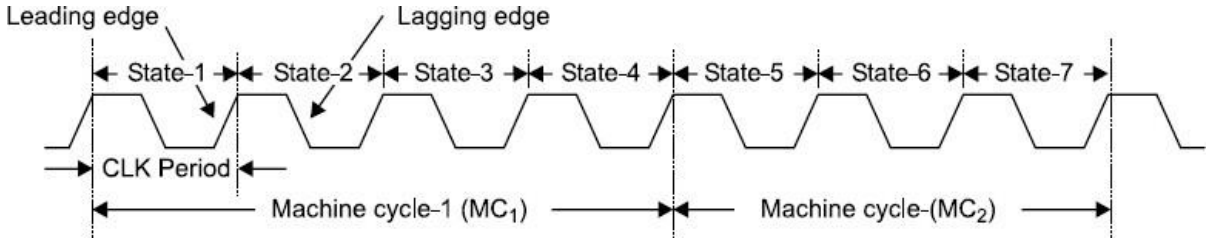

Fig.1.7 Machine cycle showing clock periods

PROCESSOR CYCLE:

The functions of the microprocessor are divided into fetch and execute cycle of any instruction of a program. The program is nothing but number of instructions stored in the memory in sequence. In the normal process of operation, the microprocessor fetches (receives or reads) and executes one instruction at a time in the sequence until it executes the halt (HLT) instruction.

INSTRUCTION CYCLE

An instruction cycle is defined as the time required to fetch and execute an instruction. For executing any program, basically 2-steps are followed sequentially with the help of clocks

- Fetch
- Execute.

The time taken by the µP in performing the fetch and execute operations are called fetch and execute cycle. Thus, sum of the fetch and execute cycle is called the instruction cycle as indicated in Fig. 8. Each read or writes operation constitutes a machine cycle. The instructions of 8085 require 1–5 machine cycles containing 3–6 states (clocks). The 1st machine cycle of any instruction is always an Op Code fetch cycle in which the processor decides the nature of instruction. It is of at least 4-states. It may go up to 6-states.

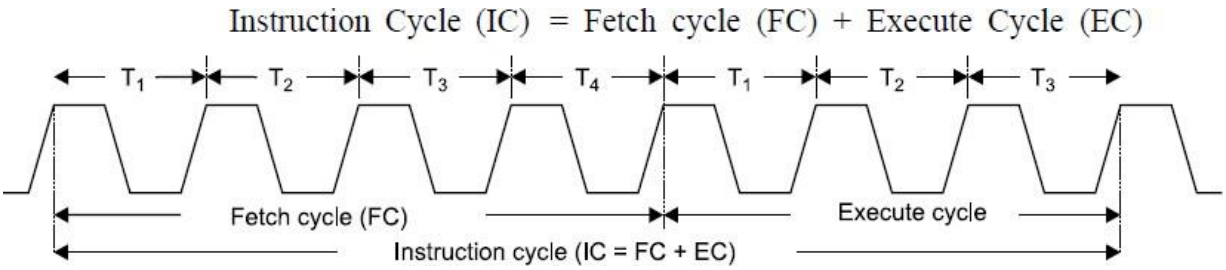

Fig.1.8 Processor cycle

RULES TO IDENTIFY NUMBER OF MACHINE CYCLES IN AN INSTRUCTION:

- If an addressing mode is direct, immediate or implicit then No. of machine cycles = No. of bytes.
- If the addressing mode is indirect then No. of machine cycles = No. of bytes + 1. Add +1 to the No. of machine cycles if it is memory read/write operation.
- If the operand is 8-bit or 16-bit address then, No. of machine cycles = No. of bytes +1.
- These rules are applicable to 80% of the instructions of 8085.

TIMING DIAGRAM OF OPCODE FETCH

The process of Opcode fetch operation requires minimum 4-clock cycles T1, T2, T3, and T4 and is the 1st machine cycle (M1) of every instruction.

Example
Fetch a byte 41H stored at memory location 2105H.

For fetching a byte, the microprocessor must find out the memory location where it is stored. Then provide condition (control) for data flow from memory to the microprocessor. The process of data flow and timing diagram of fetch operation are shown in Fig. 9. The microprocessor fetches Opcode of the instruction from the memory as per the sequence below

- A low IO/M means microprocessor wants to communicate with memory.
- The microprocessor sends a high on status signal S1 and S0 indicating fetch operation.
- The microprocessor sends 16-bit address. AD bus has address in 1st clock of the 1st machine cycle, T1.
- AD7 to AD0 address is latched in the external latch when ALE = 1.
- AD bus now can carry data.

- In T2, the RD control signal becomes low to enable the memory for read operation.
- The memory places opcode on the AD bus
- The data is placed in the data register (DR) and then it is transferred to IR.
- During T3 the RD signal becomes high and memory is disabled.
- During T4 the opcode is sent for decoding and decoded in T4.
- The execution is also completed in T4 if the instruction is single byte.
- More machine cycles are essential for 2- or 3-byte instructions. The 1st machine cycle M1 is meant for fetching the opcode. The machine cycles M2 and M3 are required either read/ write data or address from the memory or I/O devices.

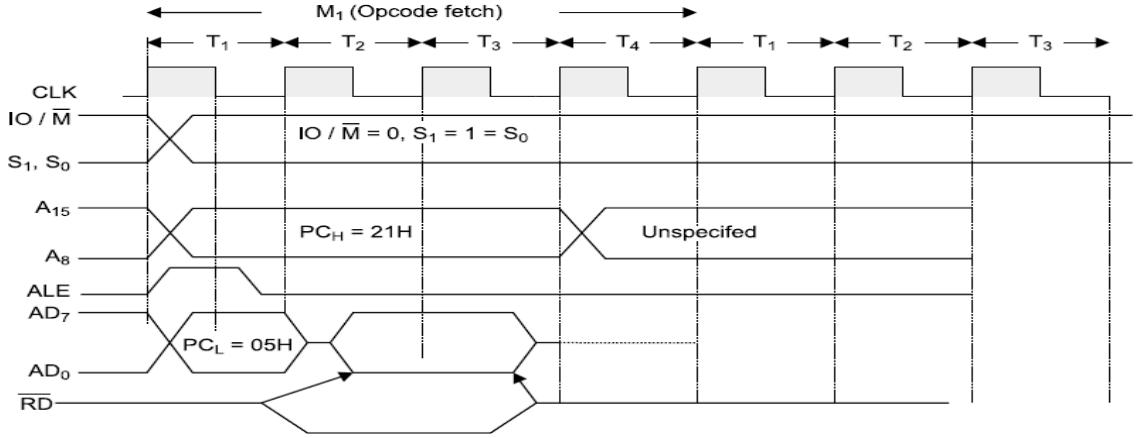

Fig. 1.9 Opcode fetch

Example For Opcode Fetch

- Explain the execution of MVI B, 05H stored at locations indicated below

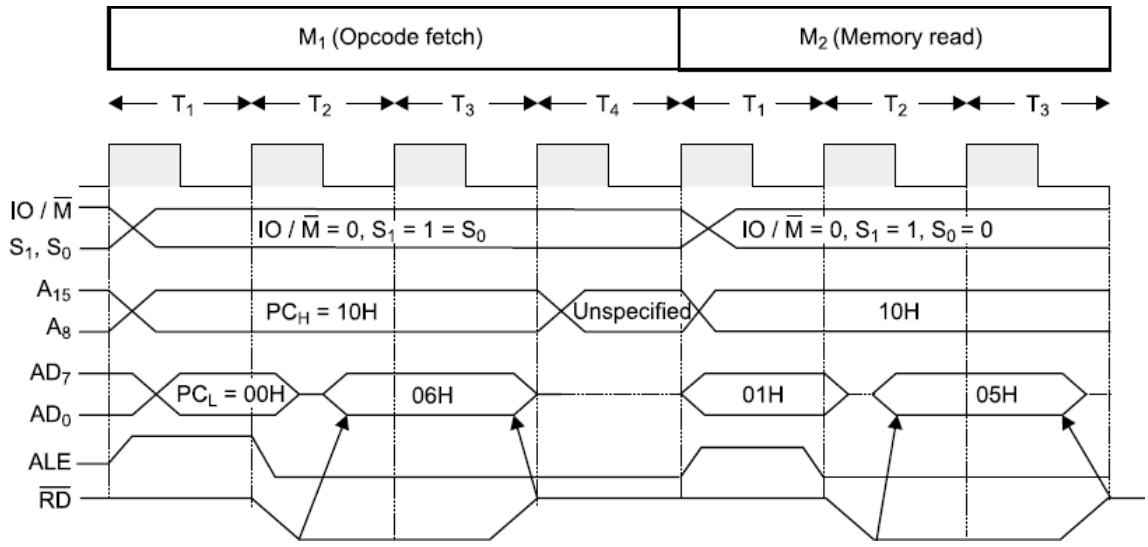

Fig. 1.10 Timing diagram for MVI B,05H

The MVI B, 05H instruction requires 2-machine cycles (M1 and M2). M1 requires 4-states and M2 requires 3-states, total of 7-states as shown in Fig. 10. Status signals IO/M, S1 and S0 specifies the 1st machine cycle as the op-code fetch. In T1-state, the high order address {10H} is placed on the bus A15 ⇔A8 and low-order address {00H} on the bus AD7 ⇔AD0 and ALE = 1. In T2 -state, the RD line goes low and the data 06 H from memory location 1000H are placed on the data bus. The fetch cycle becomes complete in T3-state. The instruction is decoded in the T4-state. During T4-state, the contents of the bus are unknown. With the change in the status signal, IO/M = 0, S1 = 1 and S0 = 0, the 2nd machine cycle is identified as the memory read. The address is 1001H and the data byte [05H] is fetched via the data bus. Both M1 and M2 perform memory read operation, but the M1 is called op-code fetch i.e., the 1st machine cycle of each instruction is identified as the opcode fetch cycle.

Mnemonic	*Instruction Byte*	*Machine Cycle*	*T-sstates*
MVI B,05H	Opcode	Opcode Fetch	4
	Immediate Data	Read Immediate Data	3
			7

TIMING DIAGRAM OF MEMORY READ

Operation:

- It is used to fetch one byte from the memory.
- It requires 3 T-States.
- It can be used to fetch operand or data from the memory.
- During T1, A8-A15 contains higher byte of address. At the same time ALE is high. Therefore Lower byte of address A0-A7 is selected from AD0-AD7 as shown in fig 11.
- Since it is memory ready operation, IO/M (bar) goes low.
- During T2 ALE goes low, RD (bar) goes low. Address is removed from AD0-AD7 and data D0-D7 appears on AD0-AD7.
- During T3, Data remains on AD0-AD7 till RD (bar) is at low signal.

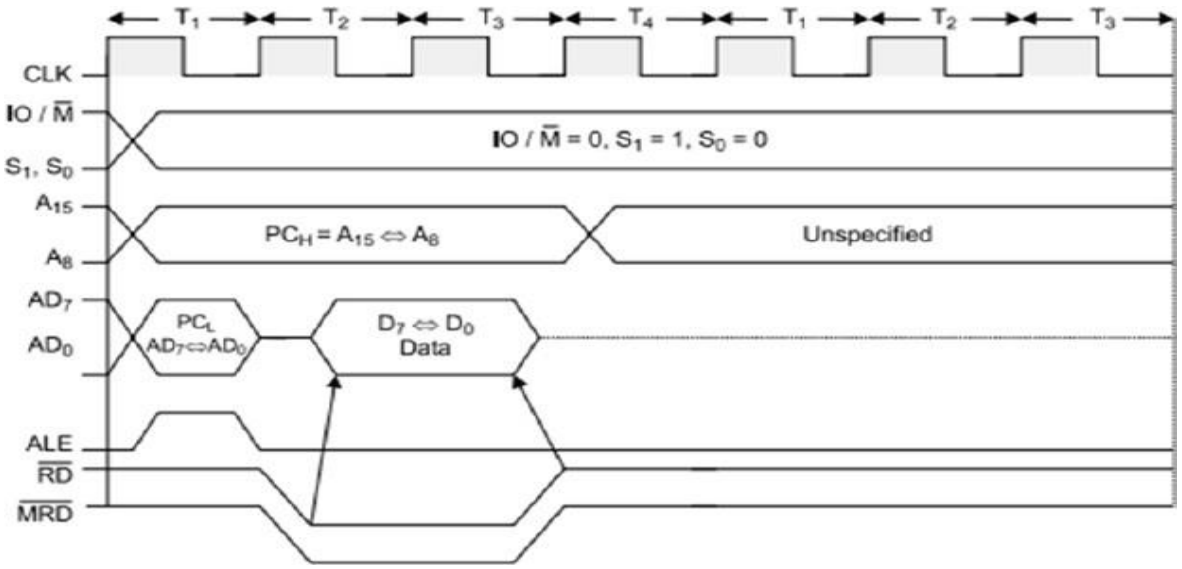

Fig 11. Timing Diagram of Memory Read

TIMING DIAGRAM FOR MEMORY WRITE

Operation:

- It is used to send one byte into memory.
- It requires 3 T-States.

- During T1, ALE is high and contains lower address A0-A7 from AD0-AD7.
- A8-A15 contains higher byte of address.
- As it is memory operation, IO/M (bar) goes low.
- During T2, ALE goes low, WR (bar) goes low and Address is removed from AD0-AD7 and then data appears on AD0-AD7 as in fig 12.
- Data remains on AD0-AD7 till WR (bar) is low.

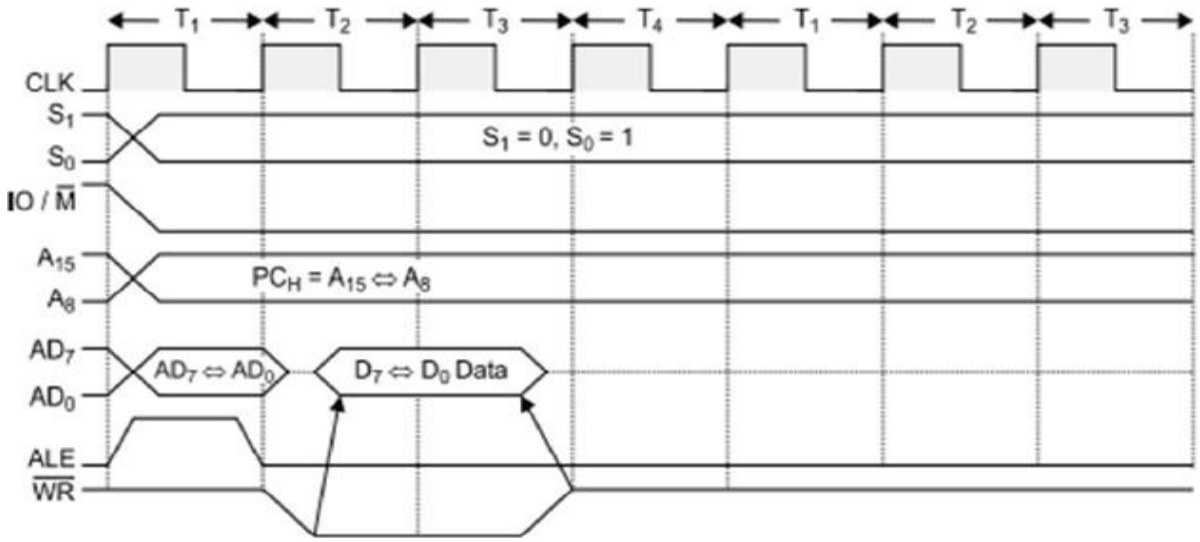

Fig 12.Memory Write timing diagram

TIMING DIAGRAM OF IO READ

Operation:

1. It is used to fetch one byte from an IO port.
2. It requires 3 T-States.
3. During T1, The Lower Byte of IO address is duplicated into higher order address bus A8-A15 as in fig13.
4. ALE is high and AD0-AD7 contains address of IO device.
5. IO/M (bar) goes high as it is an IO operation.
6. During T2, ALE goes low, RD (bar) goes low and data appears on AD0-AD7 as input from IO device.
7. During T3 Data remains on AD0-AD7 till RD (bar) is low.

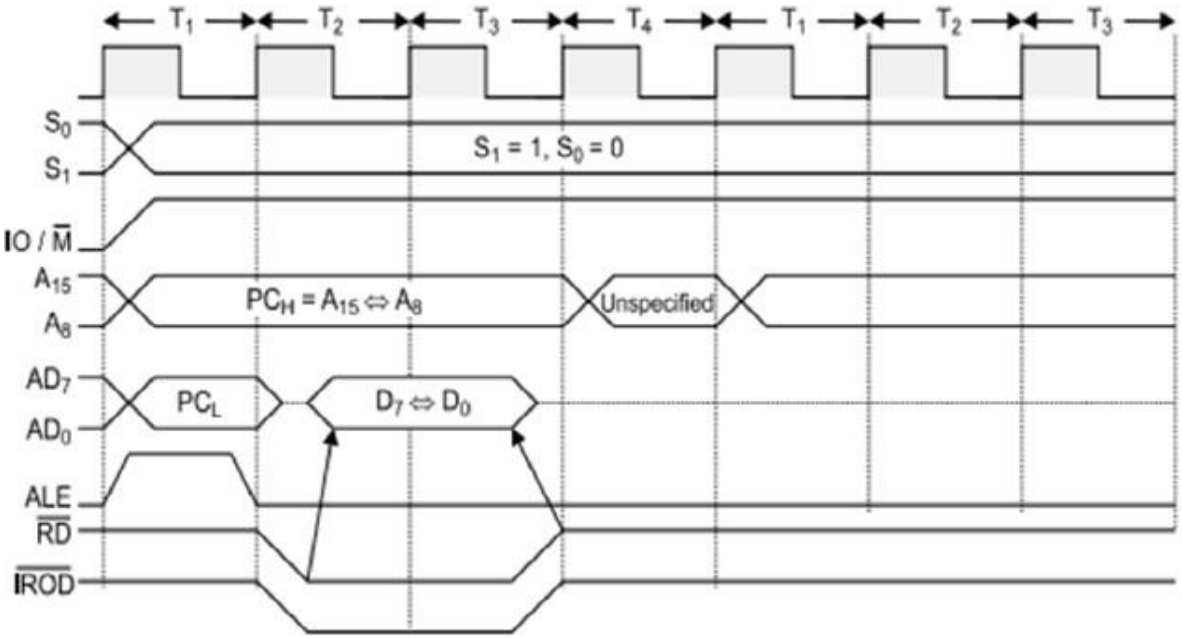

Fig 13.IO Read timing diagram

TIMING DIAGRAM OF IO WRITE

Operation:

1. It is used to writ one byte into IO device.
2. It requires 3 T-States.
3. During T1, the lower byte of address is duplicated into higher order address bus A8-A15 as in fig 14.
4. ALE is high and A0-A7 address is selected from AD0-AD7.
5. As it is an IO operation IO/M (bar) goes low.
6. During T2, ALE goes low, WR (bar) goes low and data appears on AD0-AD7 to write data into IO device.
7. During T3, Data remains on AD0-AD7 till WR(bar) is low.