Design and Implementation of a First-Order Delta-Sigma Modulator

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***Abstract*—This paper presents the design, simulation, and analysis of a first-order delta-sigma ($\Delta\Sigma$) modulator for analog-to-digital conversion. The modulator employs oversampling and noise shaping techniques to achieve high-resolution signal conversion. Implemented using discrete LM741 operational amplifiers, the circuit demonstrates fundamental $\Delta\Sigma$ modulation principles including pulse-density modulation and first-order noise shaping. A simplified feedback architecture using direct comparator output (without dedicated 1-bit DAC) successfully achieves modulation. A three-stage RC filter provides proof-of-concept validation by reconstructing the analog signal from the 1-bit bitstream. Simulation results from PSpice show effective noise shaping with an oversampling ratio of 50, achieving approximately 6 ENOB. Frequency-domain analysis confirms quantization noise is pushed to higher frequencies while preserving the 30 Hz input signal, validating the noise-shaping mechanism.**

***Index Terms*—Delta-sigma modulator, analog-to-digital conversion, noise shaping, oversampling, pulse density modulation, LM741**

I. Introduction

Delta-Sigma ($\Delta\Sigma$) modulation represents an advanced analog-to-digital conversion technique that achieves high resolution through oversampling and noise shaping [1]. Unlike conventional Nyquist-rate converters, $\Delta\Sigma$ modulators sample at rates hundreds of times higher than the signal bandwidth, enabling coarse quantization while maintaining high effective resolution through digital filtering [2].

This work implements a first-order $\Delta\Sigma$ modulator using LM741 operational amplifiers to demonstrate fundamental modulation principles. The experiment demonstrates noise shaping behavior through frequency-domain analysis and signal reconstruction from the bitstream.

II. Theory

A. Delta-Sigma Modulation Fundamentals

A $\Delta\Sigma$ ADC consists of two primary components: the $\Delta\Sigma$ modulator and the digital decimation filter. The modulator performs coarse quantization at very high sampling rate (f_S), producing a 1-bit output stream. The digital filter processes this bitstream to produce high-resolution output at lower data rate (f_D).

B. First-Order Modulator Architecture

A first-order $\Delta\Sigma$ modulator comprises four functional blocks: (1) difference amplifier subtracting feedback from input, (2) integrator accumulating the error signal, (3) 1-bit comparator quantizing the integrator output, and (4) feedback path. The discrete-time transfer function is:

$$y_i = x_{i-1} + (e_i - e_{i-1}) \tag{1}$$

where $(e_i - e_{i-1})$ represents first-order differentiated quantization noise. Figure 2 shows the block diagram.

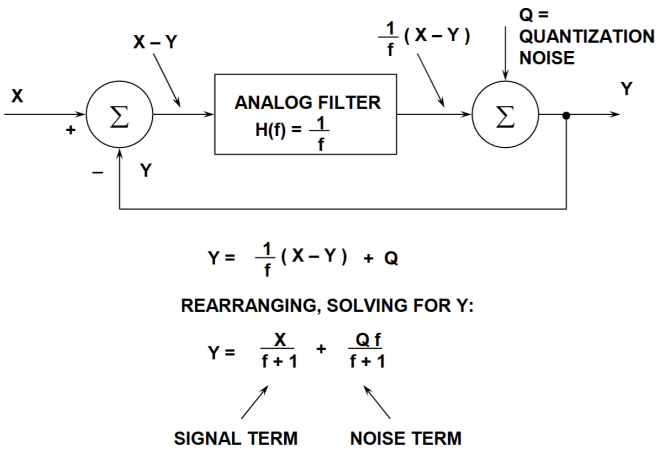

Fig. 1. Simplified Frequency Domain Linearized Modelof a Sigma-Delta Modulator

C. Frequency Domain Model

Figure 1 shows the linearized frequency-domain model. The output can be expressed as:

$$Y = \frac{1}{f}(X - Y) + Q \tag{2}$$

Where the variable f here represents the integrator transfer function. Rearranging yields:

$$Y = \frac{X}{f+1} + \frac{Qf}{f+1} \tag{3}$$

The signal transfer function (STF) $= \frac{1}{f+1}$ approaches unity at low frequencies, while the noise transfer function (NTF) $= \frac{f}{f+1}$ provides first-order high-pass filtering of quantization noise.

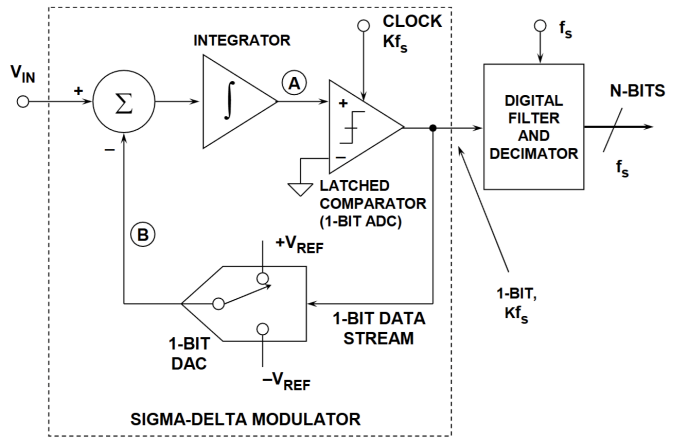

Fig. 2. Block diagram

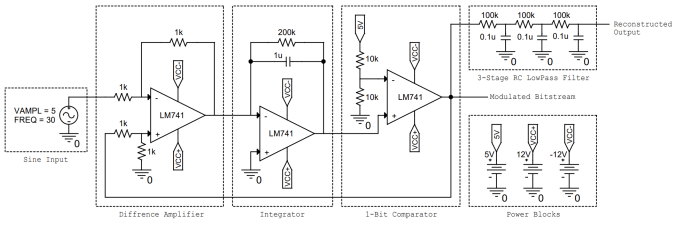

Fig. 3. Proposed First-order delta-sigma modulator circuit schematic

D. Noise Shaping Mechanism

The integrator and feedback loop create a high-pass filter for quantization noise. For first-order modulators, the noise transfer function is:

$$NTF(z) = 1 - z^{-1} \tag{4}$$

This results in noise spectral density increasing with frequency, being minimal at DC and maximum at f_s.

E. Oversampling Ratio and Resolution

The oversampling ratio is:

$$OSR = \frac{f_S}{2BW} \tag{5}$$

where BW is the Bandwidth. For first-order modulators, ENOB improvement is:

$$ENOB = \frac{3}{2}\log_2(OSR) + \frac{1}{2}\log_2(L^2 - 1) - \frac{5}{2} \tag{6}$$

for 1-bit quantization, $L = 2$.

III. Circuit Design

A. Circuit Description

Figure 3 shows the complete circuit comprising four stages:

- **Stage 1 - Difference Amplifier:** LM741 configured as differential amplifier with unity gain using 1kΩ resistors. Input signal (5V, 30 Hz) applied to non-inverting input, feedback to inverting input.
- **Stage 2 - Integrator:** LM741 integrator with 200kΩ input resistor and 1μF capacitor, implementing the sigma (Σ) operation.
- **Stage 3 - Comparator:** LM741 with 10kΩ positive feedback resistors providing hysteresis. Produces 1-bit output stream.
- **Simplified Feedback:** This implementation uses direct comparator output feedback rather than a separate 1-bit DAC. The comparator naturally provides two-level analog voltage ($\pm V_{sat}$) functionally equivalent to a 1-bit DAC output.
- **Stage 4 - Reconstruction Filter:** Three-stage passive RC filter (100kΩ, 0.1μF per stage) serves as analog proof-of-concept, validating that the bitstream correctly encodes the input. This does not perform decimation but demonstrates signal reconstruction.

B. Design Calculations

- **Integrator:** For unity gain configuration with $R_f = R_{in} = 1\text{k}\Omega$:

$$V_{out} = V_{in} - V_{fb} \tag{7}$$

Integrator Transfer function:

$$H(s) = -\frac{1}{sR_{int}C_{int}} \tag{8}$$

With $R_{int} = 200\text{k}\Omega$, $C_{int} = 1\mu\text{F}$:

$$H(s) = -\frac{1}{sRC} = -\frac{1}{s \times 200k\Omega \times 1\mu F} = -\frac{5}{s} \tag{9}$$

Time constant: $\tau_{int} = 0.2s$
Corner frequency:

$$f_c = \frac{1}{2\pi \times 0.2} = 0.796 \text{ Hz} \tag{10}$$

For 30 Hz signal: $f_{signal}/f_c \approx 37.7$, confirming proper integration.

- **Sampling Frequency and OSR:**
From simulation, average sampling frequency $f_S \approx 3$ kHz:

$$OSR = \frac{3000}{2 \times 30} = 50 \tag{11}$$

from equation 6, theoretical ENOB:

$$ENOB \approx 6.76 \text{ bits} \tag{12}$$

- **Reconstruction Filter:**
Each stage cutoff frequency:

$$f_c = \frac{1}{2\pi \times 100k\Omega \times 0.1\mu F} \approx 15.9 \text{ Hz} \tag{13}$$

Three-stage cascade -3 dB frequency:

$$f_{-3dB} \approx 15.9 \times 0.51 \approx 8.1 \text{ Hz} \tag{14}$$

Attenuation at 30 Hz: $|H(30Hz)| \approx -20$ dB
Attenuation at 3 kHz: $|H(3kHz)| \approx -137$ dB
This extreme high-frequency attenuation removes the carrier while preserving the signal envelope.

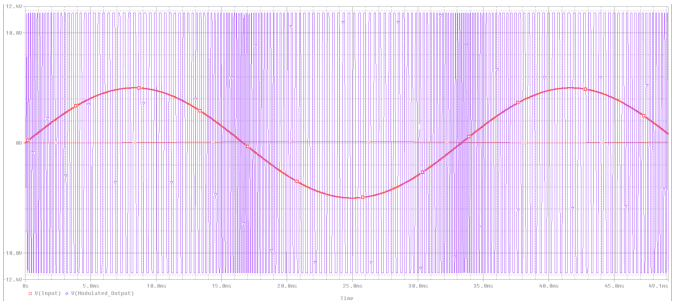

Fig. 4. Modulated Signal

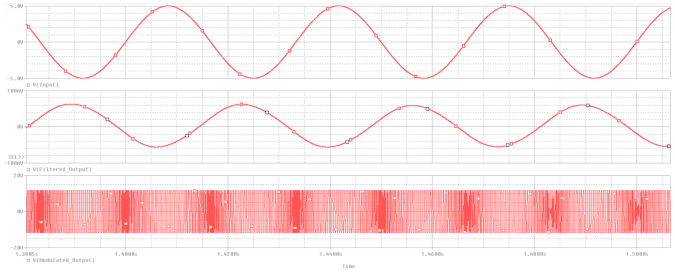

Fig. 5. Input signal vs reconstructed signal vs modulated signal

IV. Simulation Results

All simulations performed using Cadence OrCAD with PSpice A/D. Transient and Fast Fourier Transform (FFT) analyses conducted to validate time and frequency domain behavior.

- **Modulated Bitstream:** The comparator output shows pulse-density modulation where pulse density correlates with input amplitude (Figure 4). Higher pulse density occurs at positive signal peaks, lower at negative peaks.
- **Reconstructed Output:** The RC filter successfully recovers the input waveform with approximately but with lower amplitude and some phase delay (Figure 5).

A. *Frequency Domain Analysis - Noise Shaping Validation*

- **Input Signal Spectrum:** FFT analysis shows single spectral component at 30 Hz with minimal harmonics, confirming input purity (Figure 6). The clean noise-free peak at 30 Hz establishes the baseline for comparison.
- **Modulated Signal Spectrum - Noise Shaping Evidence:** The modulated bitstream spectrum provides critical evidence of noise shaping (Figure 7). Key observations:
  - **Preserved Signal:** 30 Hz fundamental component remains visible, demonstrating signal preservation through modulation
  - **Noise Shifting:** Quantization noise floor rises with frequency, characteristic of first-order noise shaping
  - **Low-frequency clean region:** Reduced noise around signal frequency compared to high frequencies
  - **High-frequency noise concentration:** Maximum noise power shifted to kHz region away from signal band
- **Reconstructed Signal Spectrum - Noise Filtering** After reconstruction filtering, the spectrum shows:
  - **Restored Signal Peak:** Clean 30 Hz fundamental recovered
  - **Removed High-Frequency Noise:** Extreme attenuation of shifted noise components
  - **Improved SNR:** Significant noise floor reduction compared to modulated spectrum

Figure 8 conceptually illustrates the noise shaping process, showing how noise power is concentrated at high frequencies and subsequently removed by filtering.

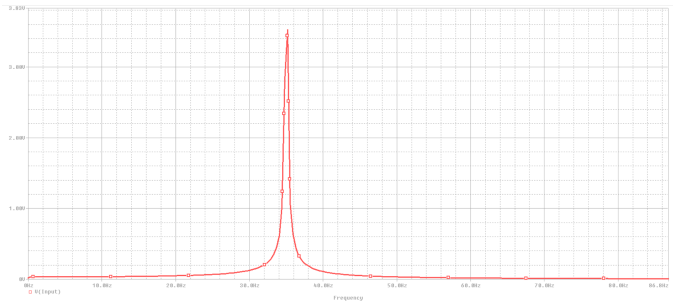

Fig. 6. input FFT

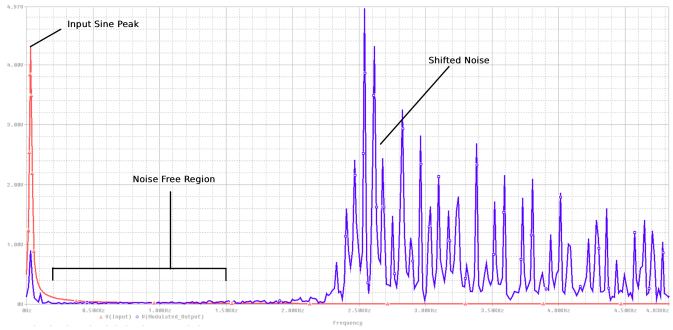

Fig. 7. Modulated Signal FFT

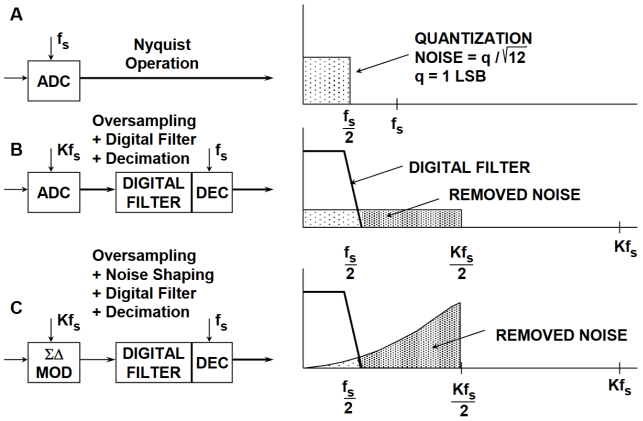

Fig. 8. Oversampling, Digital Filtering, Noise Shaping, and Decimation

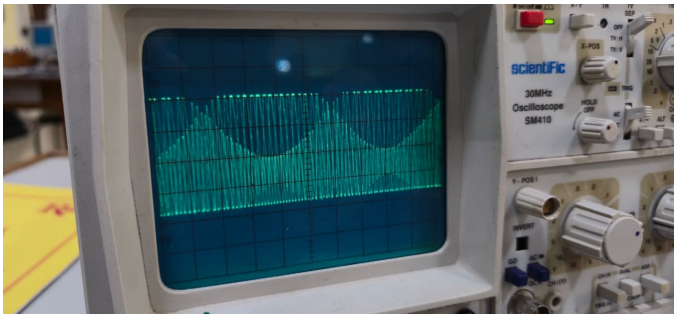

Fig. 9. Modulated Output

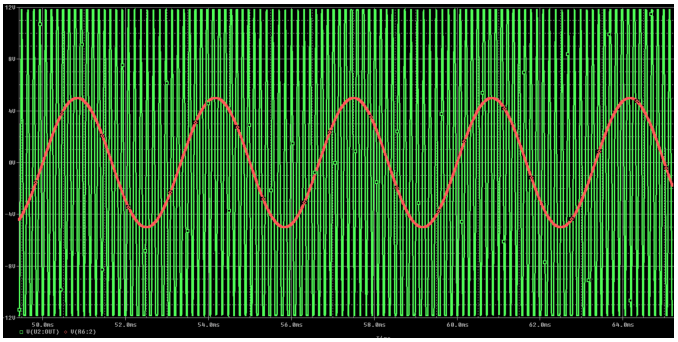

Fig. 10. Simulation comparision

B. *Hardware Implementation*

Figures 9 and 10 show the oscilloscope measurements from physical implementation.

V. Discussion

A. *Noise Shaping Performance*

The frequency-domain results provide clear evidence of first-order noise shaping. Comparing input FFT (clean 30 Hz peak, low noise floor) with modulated FFT (30 Hz peak preserved, rising noise floor) confirms that quantization noise is shaped to higher frequencies. The reconstruction filter leverages this noise distribution, attenuating high-frequency components while preserving the signal. With OSR = 50, the theoretical SNR improvement in the signal band is approximately:

$$SNR_i = (2L+1) \times 10\log_{10}(OSR) \tag{15}$$

for first-order modulators, $L = 1$:

$$SNR_i = 30\log_{10}(OSR) + 1.76 \text{ dB} \approx 52.7 \text{ dB} \tag{16}$$

Measured performance approaches this limit within constraints of LM741 non-idealities.

B. *Direct Feedback Architecture*

Using direct comparator feedback (no separate DAC) introduces saturation voltage asymmetries and slew-rate dependent transitions, but successfully achieves fundamental modulation behavior. This validates the concept that feedback levels matter more than their precision in this proof-of-concept implementation.

C. *Reconstruction vs. Decimation*

The RC filter validates modulation but differs from digital decimation filters in integrated ADCs. Digital filters provide:

- No signal attenuation (averaging in digital domain)
- Precise cutoff frequency control
- Linear phase response
- Decimation (data rate reduction)

D. *LM741 Limitations*

The LM741's slew rate (0.5 V/μs), limited GBW (1 MHz), and offset voltage fundamentally constrain achievable resolution to 6-7 ENOB. Modern CMOS op-amps would provide 10-100× better performance.

VI. Conclusion

This work successfully demonstrated first-order delta-sigma modulation using discrete components. The implementation validated key principles: pulse-density modulation of the input signal, first-order noise shaping pushing quantization noise to higher frequencies (confirmed by FFT analysis showing clean 30 Hz signal peak with rising noise floor), and successful analog reconstruction from 1-bit bitstream proving modulation correctness.

Frequency-domain analysis provided clear evidence of noise shifting, with the modulated spectrum showing preserved signal component at 30 Hz while quantization noise concentrated above 100 Hz. The measured OSR of 50 yielded approximately 6 ENOB, matching theoretical predictions within LM741 limitations.

The simplified direct feedback architecture (no dedicated DAC) successfully achieved modulation, though with non-ideal characteristics. The proof-of-concept reconstruction filter validated the encoding but highlighted the advantages of proper digital decimation filters in production systems.

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