```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     2 ************************************************************************
                                                     3 *
                                                     4 *   Zvector E7 instruction tests for VRR-a encoded:
                                                     5 *
                                                     6 *   E75C VISTR  - Vector Isolate String
                                                     7 *
                                                     8 *        James Wekel February 2025
                                                     9 ************************************************************************


                                                    11 ************************************************************************
                                                    12 *
                                                    13 *        basic instruction tests
                                                    14 *
                                                    15 ************************************************************************
                                                    16 *  This program tests proper functioning of the z/arch E7 VRR-a
                                                    17 *  Vector Isolate String instruction.
                                                    18 *  Exceptions are not tested.
                                                    19 *
                                                    20 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                    21 *  obvious coding errors.  None of the tests are thorough.  They are
                                                    22 *  NOT designed to test all aspects of any of the instructions.
                                                    23 *
                                                    24 ************************************************************************
                                                    25 *
                                                    26 *    *Testcase zvector-e7-08-VISTR
                                                    27 *    *
                                                    28 *    *   Zvector E7 instruction tests for VRR-a encoded:
                                                    29 *    *
                                                    30 *    *   E75C VISTR  - Vector Isolate String
                                                    31 *    *
                                                    32 *    *   # ---------------------------------------------------------
                                                    33 *    *   #  This tests only the basic function of the instruction.
                                                    34 *    *   #  Exceptions are NOT tested.
                                                    35 *    *   # ---------------------------------------------------------
                                                    36 *    *
                                                    37 *    mainsize    2
                                                    38 *    numcpu      1
                                                    39 *    sysclear
                                                    40 *    archlvl     z/Arch
                                                    41 *
                                                    42 *    loadcore    "$(testpath)/zvector-e7-08-VISTR.core" 0x0
                                                    43 *
                                                    44 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                    45 *    runtest     10        #
                                                    46 *    diag8cmd    disable   # (reset back to default)
                                                    47 *
                                                    48 *    *Done
                                                    49 *
                                                    50 ************************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    52 ************************************************************************
                                                    53 *        FCHECK Macro - Is a Facility Bit set?
                                                    54 *
                                                    55 *        If the facility bit is NOT set, an message is issued and
                                                    56 *        the test is skipped.
                                                    57 *
                                                    58 *        Fcheck uses R0, R1 and R2
                                                    59 *
                                                    60 * eg.    FCHECK 134,'vector-packed-decimal'
                                                    61 ************************************************************************
                                                    62          MACRO
                                                    63          FCHECK &BITNO,&NOTSETMSG
                                                    64 .*                       &BITNO : facility bit number to check
                                                    65 .*                       &NOTSETMSG : 'facility name'
                                                    66          LCLA  &FBBYTE           Facility bit in Byte
                                                    67          LCLA  &FBBIT            Facility bit within Byte
                                                    68
                                                    69          LCLA  &L(8)
                                                    70 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                    71
                                                    72 &FBBYTE  SETA  &BITNO/8
                                                    73 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                    74 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                    75
                                                    76          B     X&SYSNDX
                                                    77 *                                       Fcheck data area
                                                    78 *                                       skip messgae
                                                    79 SKT&SYSNDX DC  C'    Skipping tests: '
                                                    80          DC    C&NOTSETMSG
                                                    81          DC    C' (bit &BITNO) is not installed.'
                                                    82 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                    83 *                                       facility bits
                                                    84          DS    FD                       gap
                                                    85 FB&SYSNDX DS   4FD
                                                    86          DS    FD                       gap
                                                    87 *
                                                    88 X&SYSNDX EQU *
                                                    89          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                    90          STFLE FB&SYSNDX                get facility bits
                                                    91
                                                    92          XGR   R0,R0
                                                    93          IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                    94          N     R0,=F'&FBBIT'            is bit set?
                                                    95          BNZ   XC&SYSNDX
                                                    96 *
                                                    97 * facility bit not set, issue message and exit
                                                    98 *
                                                    99          LA    R0,SKL&SYSNDX            message length
                                                   100          LA    R1,SKT&SYSNDX            message address
                                                   101          BAL   R2,MSG
                                                   102
                                                   103          B     EOJ
                                                   104 XC&SYSNDX EQU *
                                                   105          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     107 ************************************************************************
                                                     108 *        Low core PSWs
                                                     109 ************************************************************************
                               00000000  0000438F   110 ZVE7TST  START 0
00000000                       00000000             111          USING ZVE7TST,R0            Low core addressability
                                                    112
                               00000140  00000000   113 SVOLDPSW EQU   ZVE7TST+X'140'        z/Arch Supervisor call old PSW

00000000                       00000000  000001A0   115          ORG   ZVE7TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                         116          DC    X'0000000180000000'
000001A8  00000000 00000200                         117          DC    AD(BEGIN)

000001B0                       000001B0  000001D0   119          ORG   ZVE7TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                         120          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                         121          DC    AD(X'DEAD')

000001E0                       000001E0  00000200   123          ORG   ZVE7TST+X'200'        Start of actual test program...

                                                    125 ************************************************************************
                                                    126 *                The actual "ZVE7TST" program itself...
                                                    127 ************************************************************************
                                                    128 *
                                                    129 *  Architecture Mode: z/Arch
                                                    130 *  Register Usage:
                                                    131 *
                                                    132 *    R0       (work)
                                                    133 *    R1-4     (work)
                                                    134 *    R5       Testing control table - current test base
                                                    135 *    R6-R7    (work)
                                                    136 *    R8       First base register
                                                    137 *    R9       Second base register
                                                    138 *    R10      Third base register
                                                    139 *    R11      E7TEST call return
                                                    140 *    R12      E7TESTS register
                                                    141 *    R13      (work)
                                                    142 *    R14      Subroutine call
                                                    143 *    R15      Secondary Subroutine call or work
                                                    144 *
                                                    145 ************************************************************************

00000200                       00000200             147          USING BEGIN,R8          FIRST Base Register
00000200                       00001200             148          USING BEGIN+4096,R9     SECOND Base Register
00000200                       00002200             149          USING BEGIN+8192,R10    THIRD Base Register

00000200  0580                                      151 BEGIN    BALR  R8,0              Initalize FIRST base register
00000202  0680                                      152          BCTR  R8,0              Initalize FIRST base register
00000204  0680                                      153          BCTR  R8,0              Initalize FIRST base register

00000206  4190 8800                    00000800     155          LA    R9,2048(,R8)      Initalize SECOND base register
0000020A  4190 9800                    00000800     156          LA    R9,2048(,R9)      Initalize SECOND base register
                                                    157
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000020E  41A0 9800                    00000800   158          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                    00000800   159          LA    R10,2048(,R10)   Initalize THIRD base register
                                                  160
00000216  B600 8354                    00000554   161          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 8355                    00000555   162          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 8355                    00000555   163          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 8354                    00000554   164          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                  165
                                                  166 ********************************************************************
                                                  167 * Is z/Architecture vector facility installed  (bit 129)
                                                  168 ********************************************************************
                                                  169
                                                  170          FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                    000002A8  171+         B     X0001
                                                  172+*                                  Fcheck data area
                                                  173+*                                  skip messgae
0000022A  40404040 E2928997                       174+SKT0001  DC    C'    Skipping tests: '
0000023E  A961C199 838889A3                       175+         DC    C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                       176+         DC    C' (bit 129) is not installed.'
                            0000004E  00000001    177+SKL0001  EQU   *-SKT0001
                                                  178+*                                  facility bits
00000278  00000000 00000000                       179+         DS    FD               gap
00000280  00000000 00000000                       180+FB0001   DS    4FD
000002A0  00000000 00000000                       181+         DS    FD               gap
                                                  182+*
                            000002A8  00000001    183+X0001    EQU   *
000002A8  4100 0004                    00000004   184+         LA    R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                    00000280   185+         STFLE FB0001           get facility bits
000002B0  B982 0000                               186+         XGR   R0,R0
000002B4  4300 8090                    00000290   187+         IC    R0,FB0001+16     get fbit byte
000002B8  5400 8368                    00000568   188+         N     R0,=F'64'        is bit set?
000002BC  4770 80D0                    000002D0   189+         BNZ   XC0001
                                                  190+*
                                                  191+* facility bit not set, issue message and exit
                                                  192+*
000002C0  4100 004E                    0000004E   193+         LA    R0,SKL0001       message length
000002C4  4110 802A                    0000022A   194+         LA    R1,SKT0001       message address
000002C8  4520 8270                    00000470   195+         BAL   R2,MSG
000002CC  47F0 8338                    00000538   196+         B     EOJ
                            000002D0  00000001    197+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    199 ********************************************************************************
                                                    200 *               Do tests in the E7TESTS table
                                                    201 ********************************************************************************
                                                    202
000002D0  58C0 836C                       0000056C  203           L     R12,=A(E7TESTS)          get table of test addresses
                                                    204
                                000002D4  00000001  205 NEXTE7    EQU   *
000002D4  5850 C000                       00000000  206           L     R5,0(0,R12)              get test address
000002D8  1255                                      207           LTR   R5,R5                       have a test?
000002DA  4780 8228                       00000428  208           BZ    ENDTEST                        done?
                                                    209
000002DE                        00000000            210           USING E7TEST,R5
                                                    211
000002DE  4800 5004                       00000004  212           LH    R0,TNUM                  save current test number
000002E2  5000 8E04                       00001004  213           ST    R0,TESTING               for easy reference
                                                    214
000002E6  E760 8EF8 0806                  000010F8  215           VL    V22,V1FUDGE              using V22 as v1 for instruction
000002EC  58B0 5000                       00000000  216           L     R11,TSUB                 get address of test routine
000002F0  05BB                                      217           BALR  R11,R11                  do test
                                                    218
000002F2  E310 500A 0076                  0000000A  219           LB    R1,CCMASK                (failure CC mask)
000002F8  8910 0004                       00000004  220           SLL   R1,4                     (shift to BC instr CC position)
000002FC  4410 8118                       00000318  221           EX    R1,TESTCC                fail if...
                                                    222
                                00000300  00000001  223 TESTREST EQU   *
00000300  E310 5030 0014                  00000030  224           LGF   R1,READDR                get address of expected result
00000306  D50F 5040 1000        00000040  00000000  225           CLC   V1OUTPUT,0(R1)           valid?
0000030C  4770 81B0                       000003B0  226           BNE   FAILMSG                     no, issue failed message
                                                    227
00000310  41C0 C004                       00000004  228           LA    R12,4(0,R12)             next test address
00000314  47F0 80D4                       000002D4  229           B     NEXTE7
                                                    230
00000318  4700 811C                       0000031C  231 TESTCC    BC    0,CCMSG                  (unexpected condition code?)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    233 ********************************************************************************
                                                    234 * cc was not as expected
                                                    235 ********************************************************************************
                               0000031C  00000001   236 CCMSG    EQU   *
                                                    237 *
                                                    238 * is CS set by test?
                                                    239 *
0000031C  E310 5008 0076                 00000008   240          LB    R1,M5                    Get M5
00000322  E310 8360 0080                 00000560   241          NG    R1,=D'1'                   issolate CS
00000328  4780 8100                      00000300   242          BZ    TESTREST                     not set?
                                                    243 *
                                                    244 * extract CC from extracted PSW
                                                    245 *
0000032C  5810 500C                      0000000C   246          L     R1,CCPSW
00000330  8810 000C                      0000000C   247          SRL   R1,12
00000334  5410 8370                      00000570   248          N     R1,=XL4'3'
00000338  4210 5014                      00000014   249          STC   R1,CCFOUND               save cc
                                                    250 *
                                                    251 * FILL IN MESSAGE
                                                    252 *
0000033C  4820 5004                      00000004   253          LH    R2,TNUM                  get test number and convert
00000340  4E20 8ED6                      000010D6   254          CVD   R2,DECNUM
00000344  D211 8EC0 8EAA      000010C0   000010AA   255          MVC   PRT3,EDIT
0000034A  DE11 8EC0 8ED6      000010C0   000010D6   256          ED    PRT3,DECNUM
00000350  D202 8E65 8ECD      00001065   000010CD   257          MVC   CCPRTNUM(3),PRT3+13      fill in message with test #
                                                    258
00000356  D207 8E82 5015      00001082   00000015   259          MVC   CCPRTNAME,OPNAME         fill in message with instruction
                                                    260
0000035C  B982 0022                                 261          XGR   R2,R2                    get CC as U8
00000360  4320 5009                      00000009   262          IC    R2,CC
00000364  4E20 8ED6                      000010D6   263          CVD   R2,DECNUM                and convert
00000368  D211 8EC0 8EAA      000010C0   000010AA   264          MVC   PRT3,EDIT
0000036E  DE11 8EC0 8ED6      000010C0   000010D6   265          ED    PRT3,DECNUM
00000374  D200 8E98 8ECF      00001098   000010CF   266          MVC   CCPRTEXP(1),PRT3+15      fill in message with CC field
                                                    267
0000037A  B982 0022                                 268          XGR   R2,R2                    get CCFOUND as U8
0000037E  4320 5014                      00000014   269          IC    R2,CCFOUND
00000382  4E20 8ED6                      000010D6   270          CVD   R2,DECNUM                and convert
00000386  D211 8EC0 8EAA      000010C0   000010AA   271          MVC   PRT3,EDIT
0000038C  DE11 8EC0 8ED6      000010C0   000010D6   272          ED    PRT3,DECNUM
00000392  D200 8EA8 8ECF      000010A8   000010CF   273          MVC   CCPRTGOT(1),PRT3+15      fill in message with ccfound
                                                    274
00000398  4100 0055                      00000055   275          LA    R0,CCPRTLNG              message length
0000039C  4110 8E55                      00001055   276          LA    R1,CCPRTLINE             messagfe address
000003A0  45F0 8236                      00000436   277          BAL   R15,RPTERROR
                                                    278
000003A4  5800 8374                      00000574   279          L     R0,=F'1'                 set failed test indicator
000003A8  5000 8E00                      00001000   280          ST    R0,FAILED
                                                    281
000003AC  47F0 8100                      00000300   282          B     TESTREST
                                                    283
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    285 ************************************************************************
                                                    286 * result not as expected:
                                                    287 *        issue message with test number, instruction under test
                                                    288 *              and instruction M3, M5
                                                    289 ************************************************************************
                                 000003B0  00000001 290 FAILMSG  EQU   *
000003B0  4820 5004                        00000004 291          LH    R2,TNUM              get test number and convert
000003B4  4E20 8ED6                        000010D6 292          CVD   R2,DECNUM
000003B8  D211 8EC0 8EAA       000010C0   000010AA 293          MVC   PRT3,EDIT
000003BE  DE11 8EC0 8ED6       000010C0   000010D6 294          ED    PRT3,DECNUM
000003C4  D202 8E18 8ECD       00001018   000010CD 295          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    296
000003CA  D207 8E33 5015       00001033   00000015 297          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    298
000003D0  B982 0022                                 299          XGR   R2,R2                get M3 as U8
000003D4  4320 5007                        00000007 300          IC    R2,M3
000003D8  4E20 8ED6                        000010D6 301          CVD   R2,DECNUM            and convert
000003DC  D211 8EC0 8EAA       000010C0   000010AA 302          MVC   PRT3,EDIT
000003E2  DE11 8EC0 8ED6       000010C0   000010D6 303          ED    PRT3,DECNUM
000003E8  D202 8E44 8ECD       00001044   000010CD 304          MVC   PRTM3(3),PRT3+13     fill in message with M3 field
                                                    305
000003EE  B982 0022                                 306          XGR   R2,R2                get M5 as U8
000003F2  4320 5008                        00000008 307          IC    R2,M5
000003F6  4E20 8ED6                        000010D6 308          CVD   R2,DECNUM            and convert
000003FA  D211 8EC0 8EAA       000010C0   000010AA 309          MVC   PRT3,EDIT
00000400  DE11 8EC0 8ED6       000010C0   000010D6 310          ED    PRT3,DECNUM
00000406  D202 8E51 8ECD       00001051   000010CD 311          MVC   PRTM5(3),PRT3+13     fill in message with M5 field
                                                    312
0000040C  4100 004D                        0000004D 313          LA    R0,PRTLNG            message length
00000410  4110 8E08                        00001008 314          LA    R1,PRTLINE           messagfe address
00000414  45F0 8236                        00000436 315          BAL   R15,RPTERROR

                                                    317 ************************************************************************
                                                    318 * continue after a failed test
                                                    319 ************************************************************************
                                 00000418  00000001 320 FAILCONT EQU   *
00000418  5800 8374                        00000574 321          L     R0,=F'1'                set failed test indicator
0000041C  5000 8E00                        00001000 322          ST    R0,FAILED
                                                    323
00000420  41C0 C004                        00000004 324          LA    R12,4(0,R12)            next test address
00000424  47F0 80D4                        000002D4 325          B     NEXTE7


                                                    327 ************************************************************************
                                                    328 * end of testing; set ending psw
                                                    329 ************************************************************************
                                 00000428  00000001 330 ENDTEST  EQU   *
00000428  5810 8E00                        00001000 331          L     R1,FAILED               did a test fail?
0000042C  1211                                      332          LTR   R1,R1
0000042E  4780 8338                        00000538 333          BZ    EOJ                     No, exit
00000432  47F0 8350                        00000550 334          B     FAILTEST                Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    336 ************************************************************************
                                                    337 *        RPTERROR          Report instruction test in error
                                                    338 *                             R0 = MESSGAE LENGTH
                                                    339 *                             R1 = ADDRESS OF MESSAGE
                                                    340 ************************************************************************

00000436  50F0 8254                 00000454       342 RPTERROR ST    R15,RPTSAVE          Save return address
0000043A  5050 8258                 00000458       343          ST    R5,RPTSVR5           Save R5
                                                    344 *
                                                    345 *        Use Hercules Diagnose for Message to console
                                                    346 *
0000043E  9002 8260                 00000460       347          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000442  4520 8270                 00000470       348          BAL   R2,MSG               call Hercules console MSG display
00000446  9802 8260                 00000460       349          LM    R0,R2,RPTDWSAV       restore regs


0000044A  5850 8258                 00000458       351          L     R5,RPTSVR5           Restore R5
0000044E  58F0 8254                 00000454       352          L     R15,RPTSAVE          Restore return address
00000452  07FF                                     353          BR    R15                  Return to caller

00000454  00000000                                 355 RPTSAVE  DC    F'0'                 R15 save area
00000458  00000000                                 356 RPTSVR5  DC    F'0'                 R5 save area

00000460  00000000 00000000                        358 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call


                                                    360 ************************************************************************
                                                    361 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    362 *                R2 = return address
                                                    363 ************************************************************************

00000470  4900 8378                 00000578       365 MSG      CH    R0,=H'0'             Do we even HAVE a message?
00000474  07D2                                     366          BNHR  R2                   No, ignore

00000476  9002 82AC                 000004AC       368          STM   R0,R2,MSGSAVE        Save registers

0000047A  4900 837A                 0000057A       370          CH    R0,=AL2(L'MSGMSG)    Message length within limits?
0000047E  47D0 8286                 00000486       371          BNH   MSGOK                Yes, continue
00000482  4100 005F                 0000005F       372          LA    R0,L'MSGMSG          No, set to maximum

00000486  1820                                     374 MSGOK    LR    R2,R0                Copy length to work register
00000488  0620                                     375          BCTR  R2,0                 Minus-1 for execute
0000048A  4420 82B8                 000004B8       376          EX    R2,MSGMVC            Copy message to O/P buffer

0000048E  4120 200A                 0000000A       378          LA    R2,1+L'MSGCMD(,R2)   Calculate true command length
00000492  4110 82BE                 000004BE       379          LA    R1,MSGCMD            Point to true command

00000496  83120008                                 381          DC    X'83',X'12',X'0008'  Issue Hercules Diagnose X'008'
0000049A  4780 82A6                 000004A6       382          BZ    MSGRET               Return if successful
                                                    383
0000049E  1222                                     384          LTR   R2,R2                Is Diag8 Ry (R2) 0?
000004A0  4780 82A6                 000004A6       385          BZ    MSGRET                 an error occurred but coninue
                                                    386
000004A4  0000                                     387          DC    H'0'                 CRASH for debugging purposes

000004A6  9802 82AC                 000004AC       389 MSGRET   LM    R0,R2,MSGSAVE        Restore registers
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000004AA  07F2                                      390          BR    R2                    Return to caller


000004AC  00000000 00000000                         392 MSGSAVE  DC    3F'0'                 Registers save area
000004B8  D200 82C7 1000      000004C7  00000000    393 MSGMVC   MVC   MSGMSG(0),0(R1)       Executed instruction

000004BE  D4E2C7D5 D6C8405C                         395 MSGCMD   DC    C'MSGNOH * '          *** HERCULES MESSAGE COMMAND ***
000004C7  40404040 40404040                         396 MSGMSG   DC    CL95' '               The message text to be displayed
                                                    397
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     399 ********************************************************************************
                                                     400 *        Normal completion or Abnormal termination PSWs
                                                     401 ********************************************************************************

00000528  00020001 80000000                          403 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
00000538  B2B2 8328                  00000528        405 EOJ      LPSWE EOJPSW                   Normal completion

00000540  00020001 80000000                          407 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
00000550  B2B2 8340                  00000540        409 FAILTEST LPSWE FAILPSW                  Abnormal termination

                                                     411 ********************************************************************************
                                                     412 *        Working Storage
                                                     413 ********************************************************************************

00000554  00000000                                   415 CTLR0    DS    F                        CR0
00000558  00000000                                   416          DS    F

00000560                                             418          LTORG ,                        Literals pool
00000560  00000000 00000001                          419                =D'1'
00000568  00000040                                   420                =F'64'
0000056C  00004254                                   421                =A(E7TESTS)
00000570  00000003                                   422                =XL4'3'
00000574  00000001                                   423                =F'1'
00000578  0000                                       424                =H'0'
0000057A  005F                                       425                =AL2(L'MSGMSG)
                                                     426
                                                     427 *        some constants
                                                     428
                         00000400  00000001          429 K        EQU   1024                     One KB
                         00001000  00000001          430 PAGE     EQU   (4*K)                    Size of one page
                         00010000  00000001          431 K64      EQU   (64*K)                   64 KB
                         00100000  00000001          432 MB       EQU   (K*K)                     1 MB
                                                     433
                         AABBCCDD  00000001          434 REG2PATT EQU   X'AABBCCDD'              Polluted Register pattern
                         000000DD  00000001          435 REG2LOW  EQU         X'DD'             (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     437 *=====================================================================
                                                     438 *
                                                     439 *  NOTE: start data on an address that is easy to display
                                                     440 *        within Hercules
                                                     441 *
                                                     442 *=====================================================================
                                                     443
0000057C                      0000057C  00001000     444          ORG   ZVE7TST+X'1000'
00001000  00000000                                   445 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                   446 TESTING  DC    F'0'                    current test number

                                                     448 ************************************************************************
                                                     449 *        TEST failed : result messgae
                                                     450 ************************************************************************
                                                     451 *
                                                     452 *        failed message and associated editting
                                                     453 *
00001008  40404040 40404040                          454 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                     455 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                          456          DC    C' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                          457 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 8840D4F3                          458          DC    C' with M3='
00001044  A7A7A7                                     459 PRTM3    DC    C'xxx'
00001047  6B                                         460          DC    C','
00001048  40A689A3 8840D4F5                          461          DC    C' with M5='
00001051  A7A7A7                                     462 PRTM5    DC    C'xxx'
00001054  4B                                         463          DC    C'.'
                                0000004D  00000001   464 PRTLNG   EQU   *-PRTLINE
                                                     465
                                                     466 ************************************************************************
                                                     467 *        TEST failed : CC message
                                                     468 ************************************************************************
                                                     469 *
                                                     470 *        failed message and associated editting
                                                     471 *
00001055  40404040 40404040                          472 CCPRTLINE DC   C'         Test # '
00001065  A7A7A7                                     473 CCPRTNUM DC    C'xxx'
00001068  40A69996 95874083                          474          DC    c' wrong cc for instruction '
00001082  A7A7A7A7 A7A7A7A7                          475 CCPRTNAME DC    CL8'xxxxxxxx'
0000108A  4085A797 8583A385                          476          DC    C' expected: cc='
00001098  A7                                         477 CCPRTEXP DC    C'x'
00001099  6B                                         478          DC    C','
0000109A  40998583 8589A585                          479          DC    C' received: cc='
000010A8  A7                                         480 CCPRTGOT DC    C'x'
000010A9  4B                                         481          DC    C'.'
                                00000055  00000001   482 CCPRTLNG   EQU   *-CCPRTLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    484 ************************************************************************
                                                    485 *        TEST failed : message working storge
                                                    486 ************************************************************************
000010AA  40212020 20202020                         487 EDIT     DC    XL18'4021202020202020202020202020202020'
                                                    488
000010BC  7E7E7E6E                                  489          DC    C'===>'
000010C0  40404040 40404040                         490 PRT3     DC    CL18' '
000010D2  4C7E7E7E                                  491          DC    C'<==='
000010D6  00000000 00000000                         492 DECNUM   DS    CL16


                                                    494 ************************************************************************
                                                    495 *        Vector instruction results, pollution and input
                                                    496 ************************************************************************
000010E8                                            497          DS    0F
000010E8  00000000 00000000                         498          DS    XL16                                    gap
000010F8  FFFFFFFF FFFFFFFF                         499 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
00001108  00000000 00000000                         500          DS    XL16


                                                    502 ************************************************************************
                                                    503 *        E7TEST DSECT
                                                    504 ************************************************************************


                                                    506 E7TEST   DSECT ,
00000000  00000000                                  507 TSUB     DC    A(0)                      pointer  to test
00000004  0000                                      508 TNUM     DC    H'00'                     Test Number
00000006  00                                        509          DC    X'00'
00000007  00                                        510 M3       DC    HL1'00'                   M3 used
00000008  00                                        511 M5       DC    HL1'00'                   M5 used
00000009  00                                        512 CC       DC    HL1'00'                   cc expected
0000000A  00                                        513 CCMASK   DC    HL1'00'                   not expected CC mask
                                                    514 *
                                                    515 *        CC extrtaction
                                                    516 *
0000000C  00000000 00000000                         517 CCPSW    DS    2F                        extract PSW after test (has CC)
00000014  00                                        518 CCFOUND  DS    X                         extracted cc
                                                    519
00000015  40404040 40404040                         520 OPNAME   DC    CL8' '                    E7 name
00000020  00000000                                  521 V1ADDR   DC    A(0)                      address of v1 result
00000024  00000000                                  522 V2ADDR   DC    A(0)                      address of v2 source
00000028  00000000                                  523 V3ADDR   DC    A(0)                      address of v3 source
0000002C  00000000                                  524 RELEN    DC    A(0)                      RESULT LENGTH
00000030  00000000                                  525 READDR   DC    A(0)                      result (expected) address
00000038  00000000 00000000                         526          DS    FD                           gap
00000040  00000000 00000000                         527 V1OUTPUT DS    XL16                      V1 Output
00000050  00000000 00000000                         528          DS    FD                           gap
                                                    529
                                                    530 *        test routine will be here (from VRR-a macro)
                                                    531 *
                                                    532 *        followed by
                                                    533 *              EXPECTED RESULT
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                              00000000  0000438F    535 ZVE7TST  CSECT ,
00001118                                            536          DS    0F


                                                    538 ************************************************************************
                                                    539 *     Macros to help build test tables
                                                    540 ************************************************************************


                                                    542 *
                                                    543 * macro to generate individual test
                                                    544 *
                                                    545          MACRO
                                                    546          VRR_A &INST,&M3,&M5,&CC
                                                    547 .*                                 &INST   - VRR-a instruction under test
                                                    548 .*                                 &M3     - M3 field - element size
                                                    549 .*                                 &M5     - M5 field - CS
                                                    550 .*                                 &CC     - expected CC
                                                    551
                                                    552          LCLA  &XCC(4)  &XCC has mask values for FAILED condition codes
                                                    553 &XCC(1)  SETA  7                   CC != 0
                                                    554 &XCC(2)  SETA  11                  CC != 1
                                                    555 &XCC(3)  SETA  13                  CC != 2
                                                    556 &XCC(4)  SETA  14                  CC != 3
                                                    557
                                                    558          GBLA  &TNUM
                                                    559 &TNUM    SETA  &TNUM+1
                                                    560
                                                    561          DS    0FD
                                                    562          USING *,R5               base for test data and test routine
                                                    563
                                                    564 T&TNUM   DC    A(X&TNUM)          address of test routine
                                                    565          DC    H'&TNUM'           test number
                                                    566          DC    X'00'
                                                    567          DC    HL1'&M3'                 M3 used
                                                    568          DC    HL1'&M5'                 M5 used
                                                    569          DC    HL1'&CC'           CC
                                                    570          DC    HL1'&XCC(&CC+1)'   CC failed mask
                                                    571
                                                    572          DS    2F                 extracted PSW after test (has CC)
                                                    573          DC    X'FF'              extracted CC, if test failed
                                                    574
                                                    575          DC    CL8'&INST'         instruction name
                                                    576          DC    A(RE&TNUM)         address of v1 result
                                                    577          DC    A(RE&TNUM+16)      address of v2 source
                                                    578          DC    A(RE&TNUM+32)      address of v3 source
                                                    579          DC    A(16)              result length
                                                    580 REA&TNUM DC    A(RE&TNUM)         result address
                                                    581          DS    FD                 gap
                                                    582 V1O&TNUM DS    XL16               V1 output
                                                    583          DS    FD                 gap
                                                    584 .*
                                                    585 *
                                                    586 X&TNUM   DS    0F
                                                    587          LA   R1,V1FUDGE         load v21 fudge
                                                    588          VL    v21,0(R1)
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      589
                                                      590          LGF   R1,V2ADDR          load v2 source
                                                      591          VL    v22,0(R1)          use v21 to test decoder
                                                      592
                                                      593          &INST V21,V22,&M3,&M5           test instruction
                                                      594
                                                      595          EPSW  R2,R0              extract psw
                                                      596          ST    R2,CCPSW              to save CC
                                                      597
                                                      598          VST   V21,V1O&TNUM       save v1 output
                                                      599
                                                      600          BR    R11                return
                                                      601
                                                      602 RE&TNUM  DC    0F                 V1 for this test
                                                      603
                                                      604          DROP  R5
                                                      605          MEND
                                                      607 *
                                                      608 * macro to generate table of pointers to individual tests
                                                      609 *
                                                      610          MACRO
                                                      611          PTTABLE
                                                      612          GBLA  &TNUM
                                                      613          LCLA  &CUR
                                                      614 &CUR     SETA  1
                                                      615 .*
                                                      616 TTABLE   DS    0F
                                                      617 .LOOP    ANOP
                                                      618 .*
                                                      619          DC    A(T&CUR)                 test address
                                                      620 .*
                                                      621 &CUR     SETA  &CUR+1
                                                      622          AIF   (&CUR LE &TNUM).LOOP
                                                      623 *
                                                      624          DC    A(0)                     end of table
                                                      625          DC    A(0)                     end of table
                                                      626 .*
                                                      627          MEND
                                                      628
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      630 ************************************************************************
                                                      631 *        E7 VRR-a tests
                                                      632 ************************************************************************
                                                      633          PRINT DATA
                                                      634 *
                                                      635 *
                                                      636 *   E75C VISTR  - Vector Isolate String
                                                      637 *
                                                      638 *        VRR-a instruction,
                                                      639 *              M3,                    element size
                                                      640 *              M5,                    CS
                                                      641 *              CC                     expected condition code
                                                      642 *
                                                      643 *              followed by
                                                      644 *                 16 byte V1 result
                                                      645 *                 16 byte V2 source
                                                      646
                                                      647 *-----------------------------------------------------------------
                                                      648 * VISTR  - Vector Isolate String
                                                      649 *-----------------------------------------------------------------
                                                      650
                                                      651 *-----------------------------------------------------------------
                                                      652 * case 0 -  simple debug                                  CS=1
                                                      653 *-----------------------------------------------------------------
                                                      654 *byte
                                                      655          VRR_A VISTR,0,1,0
00001118                                              656+         DS    0FD
00001118                          00001118            657+         USING *,R5             base for test data and test routine
00001118  00001170                                    658+T1       DC    A(X1)            address of test routine
0000111C  0001                                        659+         DC    H'1'             test number
0000111E  00                                          660+         DC    X'00'
0000111F  00                                          661+         DC    HL1'0'                M3 used
00001120  01                                          662+         DC    HL1'1'                M5 used
00001121  00                                          663+         DC    HL1'0'           CC
00001122  07                                          664+         DC    HL1'7'           CC failed mask
00001124  00000000 00000000                           665+         DS    2F               extracted PSW after test (has CC)
0000112C  FF                                          666+         DC    X'FF'            extracted CC, if test failed
0000112D  E5C9E2E3 D9404040                           667+         DC    CL8'VISTR'       instruction name
00001138  0000119C                                    668+         DC    A(RE1)           address of v1 result
0000113C  000011AC                                    669+         DC    A(RE1+16)        address of v2 source
00001140  000011BC                                    670+         DC    A(RE1+32)        address of v3 source
00001144  00000010                                    671+         DC    A(16)            result length
00001148  0000119C                                    672+REA1     DC    A(RE1)           result address
00001150  00000000 00000000                           673+         DS    FD               gap
00001158  00000000 00000000                           674+V1O1     DS    XL16             V1 output
00001160  00000000 00000000
00001168  00000000 00000000                           675+         DS    FD               gap
                                                      676+*
00001170                                              677+X1       DS    0F
00001170  4110 8EF8                     000010F8      678+         LA    R1,V1FUDGE      load v21 fudge
00001174  E751 0000 0806                00000000      679+         VL    v21,0(R1)
0000117A  E310 5024 0014                00000024      680+         LGF   R1,V2ADDR        load v2 source
00001180  E761 0000 0806                00000000      681+         VL    v22,0(R1)        use v21 to test decoder
00001186  E756 0010 0C5C                              682+         VISTR V21,V22,0,1              test instruction
0000118C  B98D 0020                                   683+         EPSW  R2,R0            extract psw
00001190  5020 500C                     0000000C      684+         ST    R2,CCPSW            to save CC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001194  E750 5040 080E                 00001158   685+         VST   V21,V1O1           save v1 output
0000119A  07FB                                      686+         BR    R11               return
0000119C                                            687+RE1      DC    0F                V1 for this test
0000119C                                            688+         DROP  R5
0000119C  00000000 00000000                         689          DC    XL16'00000000 00000000 00000000 00000000'   V1
000011A4  00000000 00000000
000011AC  00000000 00000000                         690          DC    XL16'00000000 00000000 00000000 00000000'   v2
000011B4  00000000 00000000
                                                    691
                                                    692          VRR_A VISTR,0,1,0
000011C0                                            693+         DS    0FD
000011C0                    000011C0                694+         USING *,R5              base for test data and test routine
000011C0  00001218                                  695+T2       DC    A(X2)             address of test routine
000011C4  0002                                      696+         DC    H'2'              test number
000011C6  00                                        697+         DC    X'00'
000011C7  00                                        698+         DC    HL1'0'                 M3 used
000011C8  01                                        699+         DC    HL1'1'                 M5 used
000011C9  00                                        700+         DC    HL1'0'            CC
000011CA  07                                        701+         DC    HL1'7'            CC failed mask
000011CC  00000000 00000000                         702+         DS    2F                extracted PSW after test (has CC)
000011D4  FF                                        703+         DC    X'FF'             extracted CC, if test failed
000011D5  E5C9E2E3 D9404040                         704+         DC    CL8'VISTR'        instruction name
000011E0  00001244                                  705+         DC    A(RE2)            address of v1 result
000011E4  00001254                                  706+         DC    A(RE2+16)         address of v2 source
000011E8  00001264                                  707+         DC    A(RE2+32)         address of v3 source
000011EC  00000010                                  708+         DC    A(16)             result length
000011F0  00001244                                  709+REA2     DC    A(RE2)            result address
000011F8  00000000 00000000                         710+         DS    FD                gap
00001200  00000000 00000000                         711+V1O2     DS    XL16              V1 output
00001208  00000000 00000000
00001210  00000000 00000000                         712+         DS    FD                gap
                                                    713+*
00001218                                            714+X2       DS    0F
00001218  4110 8EF8                       000010F8  715+         LA    R1,V1FUDGE       load v21 fudge
0000121C  E751 0000 0806                  00000000  716+         VL    v21,0(R1)
00001222  E310 5024 0014                  00000024  717+         LGF   R1,V2ADDR         load v2 source
00001228  E761 0000 0806                  00000000  718+         VL    v22,0(R1)         use v21 to test decoder
0000122E  E756 0010 0C5C                            719+         VISTR V21,V22,0,1               test instruction
00001234  B98D 0020                                 720+         EPSW  R2,R0             extract psw
00001238  5020 500C                       0000000C  721+         ST    R2,CCPSW             to save CC
0000123C  E750 9000 080E                  00001200  722+         VST   V21,V1O2          save v1 output
00001242  07FB                                      723+         BR    R11               return
00001244                                            724+RE2      DC    0F                V1 for this test
00001244                                            725+         DROP  R5
00001244  01020304 00000000                         726          DC    XL16'01020304 00000000 00000000 00000000'   V1
0000124C  00000000 00000000
00001254  01020304 00000000                         727          DC    XL16'01020304 00000000 0FFFFFFF FFFFFFFF'   v2
0000125C  0FFFFFFF FFFFFFFF
                                                    728
                                                    729          VRR_A VISTR,0,1,3
00001268                                            730+         DS    0FD
00001268                    00001268                731+         USING *,R5              base for test data and test routine
00001268  000012C0                                  732+T3       DC    A(X3)             address of test routine
0000126C  0003                                      733+         DC    H'3'              test number
0000126E  00                                        734+         DC    X'00'
0000126F  00                                        735+         DC    HL1'0'                 M3 used
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001270  01                                      736+         DC    HL1'1'                  M5 used
00001271  03                                      737+         DC    HL1'3'                CC
00001272  0E                                      738+         DC    HL1'14'               CC failed mask
00001274  00000000 00000000                       739+         DS    2F                    extracted PSW after test (has CC)
0000127C  FF                                      740+         DC    X'FF'                 extracted CC, if test failed
0000127D  E5C9E2E3 D9404040                       741+         DC    CL8'VISTR'            instruction name
00001288  000012EC                                742+         DC    A(RE3)                address of v1 result
0000128C  000012FC                                743+         DC    A(RE3+16)             address of v2 source
00001290  0000130C                                744+         DC    A(RE3+32)             address of v3 source
00001294  00000010                                745+         DC    A(16)                 result length
00001298  000012EC                                746+REA3     DC    A(RE3)                result address
000012A0  00000000 00000000                       747+         DS    FD                    gap
000012A8  00000000 00000000                       748+V1O3     DS    XL16                  V1 output
000012B0  00000000 00000000
000012B8  00000000 00000000                       749+         DS    FD                    gap
                                                  750+*
000012C0                                          751+X3       DS    0F
000012C0  4110 8EF8                    000010F8   752+         LA    R1,V1FUDGE          load v21 fudge
000012C4  E751 0000 0806               00000000   753+         VL    v21,0(R1)
000012CA  E310 5024 0014               00000024   754+         LGF   R1,V2ADDR            load v2 source
000012D0  E761 0000 0806               00000000   755+         VL    v22,0(R1)           use v21 to test decoder
000012D6  E756 0010 0C5C                          756+         VISTR V21,V22,0,1                 test instruction
000012DC  B98D 0020                               757+         EPSW  R2,R0               extract psw
000012E0  5020 500C                    0000000C   758+         ST    R2,CCPSW               to save CC
000012E4  E750 5040 080E               000012A8   759+         VST   V21,V1O3            save v1 output
000012EA  07FB                                    760+         BR    R11                 return
000012EC                                          761+RE3      DC    0F                      V1 for this test
000012EC                                          762+         DROP  R5
000012EC  01020304 05060708                       763          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v1
000012F4  090A0B0C 0D0E0F10
000012FC  01020304 05060708                       764          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v2
00001304  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    766 *halfword
                                                    767          VRR_A VISTR,1,1,0
00001310                                            768+         DS    0FD
00001310                      00001310              769+         USING *,R5              base for test data and test routine
00001310  00001368                                  770+T4       DC    A(X4)             address of test routine
00001314  0004                                      771+         DC    H'4'              test number
00001316  00                                        772+         DC    X'00'
00001317  01                                        773+         DC    HL1'1'                 M3 used
00001318  01                                        774+         DC    HL1'1'                 M5 used
00001319  00                                        775+         DC    HL1'0'            CC
0000131A  07                                        776+         DC    HL1'7'            CC failed mask
0000131C  00000000 00000000                         777+         DS    2F                extracted PSW after test (has CC)
00001324  FF                                        778+         DC    X'FF'             extracted CC, if test failed
00001325  E5C9E2E3 D9404040                         779+         DC    CL8'VISTR'        instruction name
00001330  00001394                                  780+         DC    A(RE4)            address of v1 result
00001334  000013A4                                  781+         DC    A(RE4+16)         address of v2 source
00001338  000013B4                                  782+         DC    A(RE4+32)         address of v3 source
0000133C  00000010                                  783+         DC    A(16)             result length
00001340  00001394                                  784+REA4     DC    A(RE4)            result address
00001348  00000000 00000000                         785+         DS    FD                gap
00001350  00000000 00000000                         786+V1O4     DS    XL16              V1 output
00001358  00000000 00000000
00001360  00000000 00000000                         787+         DS    FD                gap
                                                    788+*
00001368                                            789+X4       DS    0F
00001368  4110 8EF8                     000010F8    790+         LA    R1,V1FUDGE        load v21 fudge
0000136C  E751 0000 0806                00000000    791+         VL    v21,0(R1)
00001372  E310 5024 0014                00000024    792+         LGF   R1,V2ADDR         load v2 source
00001378  E761 0000 0806                00000000    793+         VL    v22,0(R1)         use v21 to test decoder
0000137E  E756 0010 1C5C                            794+         VISTR V21,V22,1,1             test instruction
00001384  B98D 0020                                 795+         EPSW  R2,R0             extract psw
00001388  5020 500C                     0000000C    796+         ST    R2,CCPSW             to save CC
0000138C  E750 5040 080E                00001350    797+         VST   V21,V1O4          save v1 output
00001392  07FB                                      798+         BR    R11               return
00001394                                            799+RE4      DC    0F                V1 for this test
00001394                                            800+         DROP  R5
00001394  00000000 00000000                         801          DC    XL16'00000000 00000000 00000000 00000000'   V1
0000139C  00000000 00000000
000013A4  00000000 00000000                         802          DC    XL16'00000000 00000000 00000000 00000000'   v2
000013AC  00000000 00000000
                                                    803
                                                    804          VRR_A VISTR,1,1,0
000013B8                                            805+         DS    0FD
000013B8                      000013B8              806+         USING *,R5              base for test data and test routine
000013B8  00001410                                  807+T5       DC    A(X5)             address of test routine
000013BC  0005                                      808+         DC    H'5'              test number
000013BE  00                                        809+         DC    X'00'
000013BF  01                                        810+         DC    HL1'1'                 M3 used
000013C0  01                                        811+         DC    HL1'1'                 M5 used
000013C1  00                                        812+         DC    HL1'0'            CC
000013C2  07                                        813+         DC    HL1'7'            CC failed mask
000013C4  00000000 00000000                         814+         DS    2F                extracted PSW after test (has CC)
000013CC  FF                                        815+         DC    X'FF'             extracted CC, if test failed
000013CD  E5C9E2E3 D9404040                         816+         DC    CL8'VISTR'        instruction name
000013D8  0000143C                                  817+         DC    A(RE5)            address of v1 result
000013DC  0000144C                                  818+         DC    A(RE5+16)         address of v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000013E0  0000145C                                819+          DC    A(RE5+32)           address of v3 source
000013E4  00000010                                820+          DC    A(16)               result length
000013E8  0000143C                                821+REA5      DC    A(RE5)              result address
000013F0  00000000 00000000                       822+          DS    FD                  gap
000013F8  00000000 00000000                       823+V1O5      DS    XL16                V1 output
00001400  00000000 00000000
00001408  00000000 00000000                       824+          DS    FD                  gap
                                                  825+*
00001410                                          826+X5        DS    0F
00001410  4110 8EF8                     000010F8  827+          LA    R1,V1FUDGE        load v21 fudge
00001414  E751 0000 0806                00000000  828+          VL    v21,0(R1)
0000141A  E310 5024 0014                00000024  829+          LGF   R1,V2ADDR          load v2 source
00001420  E761 0000 0806                00000000  830+          VL    v22,0(R1)          use v21 to test decoder
00001426  E756 0010 1C5C                          831+          VISTR V21,V22,1,1                test instruction
0000142C  B98D 0020                               832+          EPSW  R2,R0              extract psw
00001430  5020 500C                     0000000C  833+          ST    R2,CCPSW              to save CC
00001434  E750 5040 080E                000013F8  834+          VST   V21,V1O5           save v1 output
0000143A  07FB                                    835+          BR    R11                return
0000143C                                          836+RE5       DC    0F                 V1 for this test
0000143C                                          837+          DROP  R5
0000143C  10203040 00000000                       838           DC    XL16'01020304 00000000 00000000 000000000'  V1
00001444  00000000 00000000
0000144C  10203040 00000000                       839           DC    XL16'01020304 00000000 0FFFFFFF FFFFFFFF'  v2
00001454  FFFFFFFF FFFFFFFF
                                                  840
                                                  841           VRR_A VISTR,1,1,3
00001460                                          842+          DS    0FD
00001460                        00001460          843+          USING *,R5               base for test data and test routine
00001460  000014B8                                844+T6        DC    A(X6)              address of test routine
00001464  0006                                    845+          DC    H'6'               test number
00001466  00                                      846+          DC    X'00'
00001467  01                                      847+          DC    HL1'1'                  M3 used
00001468  01                                      848+          DC    HL1'1'                  M5 used
00001469  03                                      849+          DC    HL1'3'             CC
0000146A  0E                                      850+          DC    HL1'14'            CC failed mask
0000146C  00000000 00000000                       851+          DS    2F                 extracted PSW after test (has CC)
00001474  FF                                      852+          DC    X'FF'              extracted CC, if test failed
00001475  E5C9E2E3 D9404040                       853+          DC    CL8'VISTR'         instruction name
00001480  000014E4                                854+          DC    A(RE6)             address of v1 result
00001484  000014F4                                855+          DC    A(RE6+16)          address of v2 source
00001488  00001504                                856+          DC    A(RE6+32)          address of v3 source
0000148C  00000010                                857+          DC    A(16)              result length
00001490  000014E4                                858+REA6      DC    A(RE6)             result address
00001498  00000000 00000000                       859+          DS    FD                 gap
000014A0  00000000 00000000                       860+V1O6      DS    XL16               V1 output
000014A8  00000000 00000000
000014B0  00000000 00000000                       861+          DS    FD                 gap
                                                  862+*
000014B8                                          863+X6        DS    0F
000014B8  4110 8EF8                     000010F8  864+          LA    R1,V1FUDGE        load v21 fudge
000014BC  E751 0000 0806                00000000  865+          VL    v21,0(R1)
000014C2  E310 5024 0014                00000024  866+          LGF   R1,V2ADDR          load v2 source
000014C8  E761 0000 0806                00000000  867+          VL    v22,0(R1)          use v21 to test decoder
000014CE  E756 0010 1C5C                          868+          VISTR V21,V22,1,1                test instruction
000014D4  B98D 0020                               869+          EPSW  R2,R0              extract psw
000014D8  5020 500C                     0000000C  870+          ST    R2,CCPSW              to save CC
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000014DC  E750 5040 080E                  000014A0   871+         VST   V21,V1O6           save v1 output
000014E2  07FB                                       872+         BR    R11                 return
000014E4                                             873+RE6      DC    0F                  V1 for this test
000014E4                                             874+         DROP  R5
000014E4  01020304 05060708                          875          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v1
000014EC  090A0B0C 0D0E0F10
000014F4  01020304 05060708                          876          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v2
000014FC  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    878 *word
                                                    879          VRR_A VISTR,2,1,0
00001508                                            880+         DS    0FD
00001508                      00001508              881+         USING *,R5              base for test data and test routine
00001508  00001560                                  882+T7       DC    A(X7)             address of test routine
0000150C  0007                                      883+         DC    H'7'              test number
0000150E  00                                        884+         DC    X'00'
0000150F  02                                        885+         DC    HL1'2'                 M3 used
00001510  01                                        886+         DC    HL1'1'                 M5 used
00001511  00                                        887+         DC    HL1'0'            CC
00001512  07                                        888+         DC    HL1'7'            CC failed mask
00001514  00000000 00000000                         889+         DS    2F                extracted PSW after test (has CC)
0000151C  FF                                        890+         DC    X'FF'             extracted CC, if test failed
0000151D  E5C9E2E3 D9404040                         891+         DC    CL8'VISTR'        instruction name
00001528  0000158C                                  892+         DC    A(RE7)            address of v1 result
0000152C  0000159C                                  893+         DC    A(RE7+16)         address of v2 source
00001530  000015AC                                  894+         DC    A(RE7+32)         address of v3 source
00001534  00000010                                  895+         DC    A(16)             result length
00001538  0000158C                                  896+REA7     DC    A(RE7)            result address
00001540  00000000 00000000                         897+         DS    FD                gap
00001548  00000000 00000000                         898+V1O7     DS    XL16              V1 output
00001550  00000000 00000000
00001558  00000000 00000000                         899+         DS    FD                gap
                                                    900+*
00001560                                            901+X7       DS    0F
00001560  4110 8EF8                     000010F8    902+         LA    R1,V1FUDGE        load v21 fudge
00001564  E751 0000 0806                00000000    903+         VL    v21,0(R1)
0000156A  E310 5024 0014                00000024    904+         LGF   R1,V2ADDR         load v2 source
00001570  E761 0000 0806                00000000    905+         VL    v22,0(R1)         use v21 to test decoder
00001576  E756 0010 2C5C                            906+         VISTR V21,V22,2,1               test instruction
0000157C  B98D 0020                                 907+         EPSW  R2,R0             extract psw
00001580  5020 500C                     0000000C    908+         ST    R2,CCPSW             to save CC
00001584  E750 5040 080E                00001548    909+         VST   V21,V1O7          save v1 output
0000158A  07FB                                      910+         BR    R11               return
0000158C                                            911+RE7      DC    0F                V1 for this test
0000158C                                            912+         DROP  R5
0000158C  00000000 00000000                         913          DC    XL16'00000000 00000000 00000000 00000000'   V1
00001594  00000000 00000000
0000159C  00000000 00000000                         914          DC    XL16'00000000 00000000 00000000 00000000'   v2
000015A4  00000000 00000000
                                                    915
                                                    916          VRR_A VISTR,2,1,0
000015B0                                            917+         DS    0FD
000015B0                      000015B0              918+         USING *,R5              base for test data and test routine
000015B0  00001608                                  919+T8       DC    A(X8)             address of test routine
000015B4  0008                                      920+         DC    H'8'              test number
000015B6  00                                        921+         DC    X'00'
000015B7  02                                        922+         DC    HL1'2'                 M3 used
000015B8  01                                        923+         DC    HL1'1'                 M5 used
000015B9  00                                        924+         DC    HL1'0'            CC
000015BA  07                                        925+         DC    HL1'7'            CC failed mask
000015BC  00000000 00000000                         926+         DS    2F                extracted PSW after test (has CC)
000015C4  FF                                        927+         DC    X'FF'             extracted CC, if test failed
000015C5  E5C9E2E3 D9404040                         928+         DC    CL8'VISTR'        instruction name
000015D0  00001634                                  929+         DC    A(RE8)            address of v1 result
000015D4  00001644                                  930+         DC    A(RE8+16)         address of v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000015D8  00001654                                931+         DC    A(RE8+32)          address of v3 source
000015DC  00000010                                932+         DC    A(16)              result length
000015E0  00001634                                933+REA8     DC    A(RE8)             result address
000015E8  00000000 00000000                       934+         DS    FD                 gap
000015F0  00000000 00000000                       935+V1O8     DS    XL16               V1 output
000015F8  00000000 00000000
00001600  00000000 00000000                       936+         DS    FD                 gap
                                                  937+*
00001608                                          938+X8       DS    0F
00001608  4110 8EF8                     000010F8  939+         LA    R1,V1FUDGE        load v21 fudge
0000160C  E751 0000 0806                00000000  940+         VL    v21,0(R1)
00001612  E310 5024 0014                00000024  941+         LGF   R1,V2ADDR          load v2 source
00001618  E761 0000 0806                00000000  942+         VL    v22,0(R1)          use v21 to test decoder
0000161E  E756 0010 2C5C                          943+         VISTR V21,V22,2,1                test instruction
00001624  B98D 0020                               944+         EPSW  R2,R0              extract psw
00001628  5020 500C                     0000000C  945+         ST    R2,CCPSW              to save CC
0000162C  E750 5040 080E                000015F0  946+         VST   V21,V1O8           save v1 output
00001632  07FB                                    947+         BR    R11                return
00001634                                          948+RE8      DC    0F                 V1 for this test
00001634                                          949+         DROP  R5
00001634  10203040 00000000                       950          DC    XL16'01020304 00000000 00000000 000000000'  V1
0000163C  00000000 00000000
00001644  10203040 00000000                       951          DC    XL16'01020304 00000000 0FFFFFFF FFFFFFFF'  v2
0000164C  FFFFFFFF FFFFFFFF
                                                  952
                                                  953          VRR_A VISTR,2,1,3
00001658                                          954+         DS    0FD
00001658                        00001658          955+         USING *,R5               base for test data and test routine
00001658  000016B0                                956+T9       DC    A(X9)              address of test routine
0000165C  0009                                    957+         DC    H'9'               test number
0000165E  00                                      958+         DC    X'00'
0000165F  02                                      959+         DC    HL1'2'                  M3 used
00001660  01                                      960+         DC    HL1'1'                  M5 used
00001661  03                                      961+         DC    HL1'3'             CC
00001662  0E                                      962+         DC    HL1'14'            CC failed mask
00001664  00000000 00000000                       963+         DS    2F                 extracted PSW after test (has CC)
0000166C  FF                                      964+         DC    X'FF'              extracted CC, if test failed
0000166D  E5C9E2E3 D9404040                       965+         DC    CL8'VISTR'         instruction name
00001678  000016DC                                966+         DC    A(RE9)             address of v1 result
0000167C  000016EC                                967+         DC    A(RE9+16)          address of v2 source
00001680  000016FC                                968+         DC    A(RE9+32)          address of v3 source
00001684  00000010                                969+         DC    A(16)              result length
00001688  000016DC                                970+REA9     DC    A(RE9)             result address
00001690  00000000 00000000                       971+         DS    FD                 gap
00001698  00000000 00000000                       972+V1O9     DS    XL16               V1 output
000016A0  00000000 00000000
000016A8  00000000 00000000                       973+         DS    FD                 gap
                                                  974+*
000016B0                                          975+X9       DS    0F
000016B0  4110 8EF8                     000010F8  976+         LA    R1,V1FUDGE        load v21 fudge
000016B4  E751 0000 0806                00000000  977+         VL    v21,0(R1)
000016BA  E310 5024 0014                00000024  978+         LGF   R1,V2ADDR          load v2 source
000016C0  E761 0000 0806                00000000  979+         VL    v22,0(R1)          use v21 to test decoder
000016C6  E756 0010 2C5C                          980+         VISTR V21,V22,2,1                test instruction
000016CC  B98D 0020                               981+         EPSW  R2,R0              extract psw
000016D0  5020 500C                     0000000C  982+         ST    R2,CCPSW              to save CC
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000016D4  E750 5040 080E                  00001698   983+          VST   V21,V1O9           save v1 output
000016DA  07FB                                       984+          BR    R11                return
000016DC                                             985+RE9       DC    0F                 V1 for this test
000016DC                                             986+          DROP  R5
000016DC  01020304 05060708                          987           DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v1
000016E4  090A0B0C 0D0E0F10
000016EC  01020304 05060708                          988           DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v2
000016F4  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    990 *-------------------------------------------------------------------
                                                    991 * case 1 -  one zero                                        CS=1
                                                    992 *-------------------------------------------------------------------
                                                    993 *byte
                                                    994          VRR_A VISTR,0,1,3
00001700                                            995+         DS    0FD
00001700                      00001700              996+         USING *,R5              base for test data and test routine
00001700  00001758                                  997+T10      DC    A(X10)            address of test routine
00001704  000A                                      998+         DC    H'10'             test number
00001706  00                                        999+         DC    X'00'
00001707  00                                       1000+         DC    HL1'0'                 M3 used
00001708  01                                       1001+         DC    HL1'1'                 M5 used
00001709  03                                       1002+         DC    HL1'3'            CC
0000170A  0E                                       1003+         DC    HL1'14'           CC failed mask
0000170C  00000000 00000000                        1004+         DS    2F                extracted PSW after test (has CC)
00001714  FF                                       1005+         DC    X'FF'             extracted CC, if test failed
00001715  E5C9E2E3 D9404040                        1006+         DC    CL8'VISTR'        instruction name
00001720  00001784                                 1007+         DC    A(RE10)           address of v1 result
00001724  00001794                                 1008+         DC    A(RE10+16)        address of v2 source
00001728  000017A4                                 1009+         DC    A(RE10+32)        address of v3 source
0000172C  00000010                                 1010+         DC    A(16)             result length
00001730  00001784                                 1011+REA10    DC    A(RE10)           result address
00001738  00000000 00000000                        1012+         DS    FD                gap
00001740  00000000 00000000                        1013+V1O10    DS    XL16              V1 output
00001748  00000000 00000000
00001750  00000000 00000000                        1014+         DS    FD                gap
                                                   1015+*
00001758                                           1016+X10      DS    0F
00001758  4110 8EF8                      000010F8  1017+         LA    R1,V1FUDGE      load v21 fudge
0000175C  E751 0000 0806                 00000000  1018+         VL    v21,0(R1)
00001762  E310 5024 0014                 00000024  1019+         LGF   R1,V2ADDR        load v2 source
00001768  E761 0000 0806                 00000000  1020+         VL    v22,0(R1)         use v21 to test decoder
0000176E  E756 0010 0C5C                           1021+         VISTR V21,V22,0,1               test instruction
00001774  B98D 0020                                1022+         EPSW  R2,R0             extract psw
00001778  5020 500C                      0000000C  1023+         ST    R2,CCPSW             to save CC
0000177C  E750 5040 080E                 00001740  1024+         VST   V21,V1O10         save v1 output
00001782  07FB                                     1025+         BR    R11               return
00001784                                           1026+RE10     DC    0F                V1 for this test
00001784                                           1027+         DROP  R5
00001784  01020304 05060708                        1028          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v1
0000178C  090A0B0C 0D0E0F10
00001794  01020304 05060708                        1029          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v2
0000179C  090A0B0C 0D0E0F10
                                                   1030
                                                   1031          VRR_A VISTR,0,1,0
000017A8                                           1032+         DS    0FD
000017A8                      000017A8             1033+         USING *,R5              base for test data and test routine
000017A8  00001800                                 1034+T11      DC    A(X11)            address of test routine
000017AC  000B                                     1035+         DC    H'11'             test number
000017AE  00                                       1036+         DC    X'00'
000017AF  00                                       1037+         DC    HL1'0'                 M3 used
000017B0  01                                       1038+         DC    HL1'1'                 M5 used
000017B1  00                                       1039+         DC    HL1'0'            CC
000017B2  07                                       1040+         DC    HL1'7'            CC failed mask
000017B4  00000000 00000000                        1041+         DS    2F                extracted PSW after test (has CC)
000017BC  FF                                       1042+         DC    X'FF'             extracted CC, if test failed
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000017BD  E5C9E2E3 D9404040                        1043+          DC    CL8'VISTR'          instruction name
000017C8  0000182C                                 1044+          DC    A(RE11)             address of v1 result
000017CC  0000183C                                 1045+          DC    A(RE11+16)          address of v2 source
000017D0  0000184C                                 1046+          DC    A(RE11+32)          address of v3 source
000017D4  00000010                                 1047+          DC    A(16)               result length
000017D8  0000182C                                 1048+REA11     DC    A(RE11)             result address
000017E0  00000000 00000000                        1049+          DS    FD                  gap
000017E8  00000000 00000000                        1050+V1O11     DS    XL16                V1 output
000017F0  00000000 00000000
000017F8  00000000 00000000                        1051+          DS    FD                  gap
                                                   1052+*
00001800                                           1053+X11       DS    0F
00001800  4110 8EF8                      000010F8  1054+          LA    R1,V1FUDGE         load v21 fudge
00001804  E751 0000 0806                 00000000  1055+          VL    v21,0(R1)
0000180A  E310 5024 0014                 00000024  1056+          LGF   R1,V2ADDR           load v2 source
00001810  E761 0000 0806                 00000000  1057+          VL    v22,0(R1)           use v21 to test decoder
00001816  E756 0010 0C5C                           1058+          VISTR V21,V22,0,1                 test instruction
0000181C  B98D 0020                                1059+          EPSW  R2,R0               extract psw
00001820  5020 500C                      0000000C  1060+          ST    R2,CCPSW               to save CC
00001824  E750 5040 080E                 000017E8  1061+          VST   V21,V1O11           save v1 output
0000182A  07FB                                     1062+          BR    R11                 return
0000182C                                           1063+RE11      DC    0F                  V1 for this test
0000182C                                           1064+          DROP  R5
0000182C  01020304 05060708                        1065           DC    XL16'01020304 05060708 090A0B0C 0D0E0F00'   v1
00001834  090A0B0C 0D0E0F00
0000183C  01020304 05060708                        1066           DC    XL16'01020304 05060708 090A0B0C 0D0E0F00'   v2
00001844  090A0B0C 0D0E0F00
                                                   1067
                                                   1068           VRR_A VISTR,0,1,0
00001850                                           1069+          DS    0FD
00001850                       00001850            1070+          USING *,R5                base for test data and test routine
00001850  000018A8                                 1071+T12       DC    A(X12)              address of test routine
00001854  000C                                     1072+          DC    H'12'               test number
00001856  00                                       1073+          DC    X'00'
00001857  00                                       1074+          DC    HL1'0'                    M3 used
00001858  01                                       1075+          DC    HL1'1'                    M5 used
00001859  00                                       1076+          DC    HL1'0'              CC
0000185A  07                                       1077+          DC    HL1'7'              CC failed mask
0000185C  00000000 00000000                        1078+          DS    2F                  extracted PSW after test (has CC)
00001864  FF                                       1079+          DC    X'FF'               extracted CC, if test failed
00001865  E5C9E2E3 D9404040                        1080+          DC    CL8'VISTR'          instruction name
00001870  000018D4                                 1081+          DC    A(RE12)             address of v1 result
00001874  000018E4                                 1082+          DC    A(RE12+16)          address of v2 source
00001878  000018F4                                 1083+          DC    A(RE12+32)          address of v3 source
0000187C  00000010                                 1084+          DC    A(16)               result length
00001880  000018D4                                 1085+REA12     DC    A(RE12)             result address
00001888  00000000 00000000                        1086+          DS    FD                  gap
00001890  00000000 00000000                        1087+V1O12     DS    XL16                V1 output
00001898  00000000 00000000
000018A0  00000000 00000000                        1088+          DS    FD                  gap
                                                   1089+*
000018A8                                           1090+X12       DS    0F
000018A8  4110 8EF8                      000010F8  1091+          LA    R1,V1FUDGE         load v21 fudge
000018AC  E751 0000 0806                 00000000  1092+          VL    v21,0(R1)
000018B2  E310 5024 0014                 00000024  1093+          LGF   R1,V2ADDR           load v2 source
000018B8  E761 0000 0806                 00000000  1094+          VL    v22,0(R1)           use v21 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000018BE  E756 0010 0C5C                         1095+         VISTR V21,V22,0,1               test instruction
000018C4  B98D 0020                              1096+         EPSW  R2,R0               extract psw
000018C8  5020 500C                 0000000C     1097+         ST    R2,CCPSW               to save CC
000018CC  E750 5040 080E            00001890     1098+         VST   V21,V1O12           save v1 output
000018D2  07FB                                   1099+         BR    R11                 return
000018D4                                         1100+RE12     DC    0F                  V1 for this test
000018D4                                         1101+         DROP  R5
000018D4  01020304 05060708                      1102          DC    XL16'01020304 05060708 090A0B0C 0D000000'   v1
000018DC  090A0B0C 0D000000
000018E4  01020304 05060708                      1103          DC    XL16'01020304 05060708 090A0B0C 0D000F10'   v2
000018EC  090A0B0C 0D000F10
                                                 1104
                                                 1105          VRR_A VISTR,0,1,0
000018F8                                         1106+         DS    0FD
000018F8                    000018F8             1107+         USING *,R5                base base for test data and test routine
000018F8  00001950                               1108+T13      DC    A(X13)              address of test routine
000018FC  000D                                   1109+         DC    H'13'               test number
000018FE  00                                     1110+         DC    X'00'
000018FF  00                                     1111+         DC    HL1'0'                   M3 used
00001900  01                                     1112+         DC    HL1'1'                   M5 used
00001901  00                                     1113+         DC    HL1'0'              CC
00001902  07                                     1114+         DC    HL1'7'              CC failed mask
00001904  00000000 00000000                      1115+         DS    2F                  extracted PSW after test (has CC)
0000190C  FF                                     1116+         DC    X'FF'               extracted CC, if test failed
0000190D  E5C9E2E3 D9404040                      1117+         DC    CL8'VISTR'          instruction name
00001918  0000197C                               1118+         DC    A(RE13)             address of v1 result
0000191C  0000198C                               1119+         DC    A(RE13+16)          address of v2 source
00001920  0000199C                               1120+         DC    A(RE13+32)          address of v3 source
00001924  00000010                               1121+         DC    A(16)               result length
00001928  0000197C                               1122+REA13    DC    A(RE13)             result address
00001930  00000000 00000000                      1123+         DS    FD                  gap
00001938  00000000 00000000                      1124+V1O13    DS    XL16                V1 output
00001940  00000000 00000000
00001948  00000000 00000000                      1125+         DS    FD                  gap
                                                 1126+*
00001950                                         1127+X13      DS    0F
00001950  4110 8EF8                 000010F8     1128+         LA    R1,V1FUDGE         load v21 fudge
00001954  E751 0000 0806            00000000     1129+         VL    v21,0(R1)
0000195A  E310 5024 0014            00000024     1130+         LGF   R1,V2ADDR           load v2 source
00001960  E761 0000 0806            00000000     1131+         VL    v22,0(R1)           use v21 to test decoder
00001966  E756 0010 0C5C                         1132+         VISTR V21,V22,0,1               test instruction
0000196C  B98D 0020                              1133+         EPSW  R2,R0               extract psw
00001970  5020 500C                 0000000C     1134+         ST    R2,CCPSW               to save CC
00001974  E750 5040 080E            00001938     1135+         VST   V21,V1O13           save v1 output
0000197A  07FB                                   1136+         BR    R11                 return
0000197C                                         1137+RE13     DC    0F                  V1 for this test
0000197C                                         1138+         DROP  R5
0000197C  01020304 05060708                      1139          DC    XL16'01020304 05060708 090A0B0C 00000000'   v1
00001984  090A0B0C 00000000
0000198C  01020304 05060708                      1140          DC    XL16'01020304 05060708 090A0B0C 000E0F10'   v2
00001994  090A0B0C 000E0F10
                                                 1141
                                                 1142          VRR_A VISTR,0,1,0
000019A0                                         1143+         DS    0FD
000019A0                    000019A0             1144+         USING *,R5                base base for test data and test routine
000019A0  000019F8                               1145+T14      DC    A(X14)              address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000019A4  000E                                     1146+          DC    H'14'              test number
000019A6  00                                       1147+          DC    X'00'
000019A7  00                                       1148+          DC    HL1'0'                  M3 used
000019A8  01                                       1149+          DC    HL1'1'                  M5 used
000019A9  00                                       1150+          DC    HL1'0'             CC
000019AA  07                                       1151+          DC    HL1'7'             CC failed mask
000019AC  00000000 00000000                        1152+          DS    2F                 extracted PSW after test (has CC)
000019B4  FF                                       1153+          DC    X'FF'              extracted CC, if test failed
000019B5  E5C9E2E3 D9404040                        1154+          DC    CL8'VISTR'         instruction name
000019C0  00001A24                                 1155+          DC    A(RE14)            address of v1 result
000019C4  00001A34                                 1156+          DC    A(RE14+16)         address of v2 source
000019C8  00001A44                                 1157+          DC    A(RE14+32)         address of v3 source
000019CC  00000010                                 1158+          DC    A(16)              result length
000019D0  00001A24                                 1159+REA14     DC    A(RE14)            result address
000019D8  00000000 00000000                        1160+          DS    FD                 gap
000019E0  00000000 00000000                        1161+V1O14     DS    XL16               V1 output
000019E8  00000000 00000000
000019F0  00000000 00000000                        1162+          DS    FD                 gap
                                                   1163+*
000019F8                                           1164+X14       DS    0F
000019F8  4110 8EF8                      000010F8  1165+          LA    R1,V1FUDGE        load v21 fudge
000019FC  E751 0000 0806                 00000000  1166+          VL    v21,0(R1)
00001A02  E310 5024 0014                 00000024  1167+          LGF   R1,V2ADDR          load v2 source
00001A08  E761 0000 0806                 00000000  1168+          VL    v22,0(R1)          use v21 to test decoder
00001A0E  E756 0010 0C5C                           1169+          VISTR V21,V22,0,1                test instruction
00001A14  B98D 0020                                1170+          EPSW  R2,R0              extract psw
00001A18  5020 500C                      0000000C  1171+          ST    R2,CCPSW                to save CC
00001A1C  E750 5040 080E                 000019E0  1172+          VST   V21,V1O14          save v1 output
00001A22  07FB                                     1173+          BR    R11                return
00001A24                                           1174+RE14      DC    0F                 V1 for this test
00001A24                                           1175+          DROP  R5
00001A24  01020304 05060708                        1176           DC    XL16'01020304 05060708 090A0B00 00000000'   v1
00001A2C  090A0B00 00000000
00001A34  01020304 05060708                        1177           DC    XL16'01020304 05060708 090A0B00 0D0E0F10'   v2
00001A3C  090A0B00 0D0E0F10
                                                   1178
                                                   1179           VRR_A VISTR,0,1,0
00001A48                                           1180+          DS    0FD
00001A48                 00001A48                  1181+          USING *,R5               base for test data and test routine
00001A48  00001AA0                                 1182+T15       DC    A(X15)             address of test routine
00001A4C  000F                                     1183+          DC    H'15'              test number
00001A4E  00                                       1184+          DC    X'00'
00001A4F  00                                       1185+          DC    HL1'0'                  M3 used
00001A50  01                                       1186+          DC    HL1'1'                  M5 used
00001A51  00                                       1187+          DC    HL1'0'             CC
00001A52  07                                       1188+          DC    HL1'7'             CC failed mask
00001A54  00000000 00000000                        1189+          DS    2F                 extracted PSW after test (has CC)
00001A5C  FF                                       1190+          DC    X'FF'              extracted CC, if test failed
00001A5D  E5C9E2E3 D9404040                        1191+          DC    CL8'VISTR'         instruction name
00001A68  00001ACC                                 1192+          DC    A(RE15)            address of v1 result
00001A6C  00001ADC                                 1193+          DC    A(RE15+16)         address of v2 source
00001A70  00001AEC                                 1194+          DC    A(RE15+32)         address of v3 source
00001A74  00000010                                 1195+          DC    A(16)              result length
00001A78  00001ACC                                 1196+REA15     DC    A(RE15)            result address
00001A80  00000000 00000000                        1197+          DS    FD                 gap
00001A88  00000000 00000000                        1198+V1O15     DS    XL16               V1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001A90  00000000 00000000
00001A98  00000000 00000000                        1199+         DS    FD                  gap
                                                   1200+*
00001AA0                                           1201+X15      DS    0F
00001AA0  4110 8EF8                      000010F8  1202+         LA    R1,V1FUDGE         load v21 fudge
00001AA4  E751 0000 0806                 00000000  1203+         VL    v21,0(R1)
00001AAA  E310 5024 0014                 00000024  1204+         LGF   R1,V2ADDR           load v2 source
00001AB0  E761 0000 0806                 00000000  1205+         VL    v22,0(R1)           use v21 to test decoder
00001AB6  E756 0010 0C5C                           1206+         VISTR V21,V22,0,1                test instruction
00001ABC  B98D 0020                                1207+         EPSW  R2,R0               extract psw
00001AC0  5020 500C                      0000000C  1208+         ST    R2,CCPSW               to save CC
00001AC4  E750 5040 080E                 00001A88  1209+         VST   V21,V1O15           save v1 output
00001ACA  07FB                                     1210+         BR    R11                 return
00001ACC                                           1211+RE15     DC    0F                  V1 for this test
00001ACC                                           1212+         DROP  R5
00001ACC  01020304 05060708                        1213          DC    XL16'01020304 05060708 090A0000 00000000'   v1
00001AD4  090A0000 00000000
00001ADC  01020304 05060708                        1214          DC    XL16'01020304 05060708 090A000C 0D0E0F10'   v2
00001AE4  090A000C 0D0E0F10
                                                   1215
                                                   1216          VRR_A VISTR,0,1,0
00001AF0                                           1217+         DS    0FD
00001AF0                 00001AF0                  1218+         USING *,R5                base for test data and test routine
00001AF0  00001B48                                 1219+T16      DC    A(X16)              address of test routine
00001AF4  0010                                     1220+         DC    H'16'               test number
00001AF6  00                                       1221+         DC    X'00'
00001AF7  00                                       1222+         DC    HL1'0'                   M3 used
00001AF8  01                                       1223+         DC    HL1'1'                   M5 used
00001AF9  00                                       1224+         DC    HL1'0'              CC
00001AFA  07                                       1225+         DC    HL1'7'              CC failed mask
00001AFC  00000000 00000000                        1226+         DS    2F                  extracted PSW after test (has CC)
00001B04  FF                                       1227+         DC    X'FF'               extracted CC, if test failed
00001B05  E5C9E2E3 D9404040                        1228+         DC    CL8'VISTR'          instruction name
00001B10  00001B74                                 1229+         DC    A(RE16)             address of v1 result
00001B14  00001B84                                 1230+         DC    A(RE16+16)          address of v2 source
00001B18  00001B94                                 1231+         DC    A(RE16+32)          address of v3 source
00001B1C  00000010                                 1232+         DC    A(16)               result length
00001B20  00001B74                                 1233+REA16    DC    A(RE16)             result address
00001B28  00000000 00000000                        1234+         DS    FD                  gap
00001B30  00000000 00000000                        1235+V1O16    DS    XL16                V1 output
00001B38  00000000 00000000
00001B40  00000000 00000000                        1236+         DS    FD                  gap
                                                   1237+*
00001B48                                           1238+X16      DS    0F
00001B48  4110 8EF8                      000010F8  1239+         LA    R1,V1FUDGE         load v21 fudge
00001B4C  E751 0000 0806                 00000000  1240+         VL    v21,0(R1)
00001B52  E310 5024 0014                 00000024  1241+         LGF   R1,V2ADDR           load v2 source
00001B58  E761 0000 0806                 00000000  1242+         VL    v22,0(R1)           use v21 to test decoder
00001B5E  E756 0010 0C5C                           1243+         VISTR V21,V22,0,1                test instruction
00001B64  B98D 0020                                1244+         EPSW  R2,R0               extract psw
00001B68  5020 500C                      0000000C  1245+         ST    R2,CCPSW               to save CC
00001B6C  E750 5040 080E                 00001B30  1246+         VST   V21,V1O16           save v1 output
00001B72  07FB                                     1247+         BR    R11                 return
00001B74                                           1248+RE16     DC    0F                  V1 for this test
00001B74                                           1249+         DROP  R5
00001B74  01020304 05060708                        1250          DC    XL16'01020304 05060708 09000000 00000000'   v1
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001B7C  09000000 00000000
00001B84  01020304 05060708                        1251          DC    XL16'01020304 05060708 09000B0C 0D0E0F10'   v2
00001B8C  09000B0C 0D0E0F10
                                                   1252
                                                   1253          VRR_A VISTR,0,1,0
00001B98                                           1254+         DS    0FD
00001B98                     00001B98              1255+         USING *,R5                base for test data and test routine
00001B98  00001BF0                                 1256+T17      DC    A(X17)              address of test routine
00001B9C  0011                                     1257+         DC    H'17'               test number
00001B9E  00                                       1258+         DC    X'00'
00001B9F  00                                       1259+         DC    HL1'0'                   M3 used
00001BA0  01                                       1260+         DC    HL1'1'                   M5 used
00001BA1  00                                       1261+         DC    HL1'0'              CC
00001BA2  07                                       1262+         DC    HL1'7'              CC failed mask
00001BA4  00000000 00000000                        1263+         DS    2F                  extracted PSW after test (has CC)
00001BAC  FF                                       1264+         DC    X'FF'               extracted CC, if test failed
00001BAD  E5C9E2E3 D9404040                        1265+         DC    CL8'VISTR'          instruction name
00001BB8  00001C1C                                 1266+         DC    A(RE17)             address of v1 result
00001BBC  00001C2C                                 1267+         DC    A(RE17+16)          address of v2 source
00001BC0  00001C3C                                 1268+         DC    A(RE17+32)          address of v3 source
00001BC4  00000010                                 1269+         DC    A(16)               result length
00001BC8  00001C1C                                 1270+REA17    DC    A(RE17)             result address
00001BD0  00000000 00000000                        1271+         DS    FD                  gap
00001BD8  00000000 00000000                        1272+V1O17    DS    XL16                V1 output
00001BE0  00000000 00000000
00001BE8  00000000 00000000                        1273+         DS    FD                  gap
                                                   1274+*
00001BF0                                           1275+X17      DS    0F
00001BF0  4110 8EF8                      000010F8  1276+         LA    R1,V1FUDGE        load v21 fudge
00001BF4  E751 0000 0806                 00000000  1277+         VL    v21,0(R1)
00001BFA  E310 5024 0014                 00000024  1278+         LGF   R1,V2ADDR          load v2 source
00001C00  E761 0000 0806                 00000000  1279+         VL    v22,0(R1)           use v21 to test decoder
00001C06  E756 0010 0C5C                           1280+         VISTR V21,V22,0,1                test instruction
00001C0C  B98D 0020                                1281+         EPSW  R2,R0               extract psw
00001C10  5020 500C                      0000000C  1282+         ST    R2,CCPSW               to save CC
00001C14  E750 5040 080E                 00001BD8  1283+         VST   V21,V1O17           save v1 output
00001C1A  07FB                                     1284+         BR    R11                 return
00001C1C                                           1285+RE17     DC    0F                  V1 for this test
00001C1C                                           1286+         DROP  R5
00001C1C  01020304 05060708                        1287          DC    XL16'01020304 05060708 00000000 00000000'   v1
00001C24  00000000 00000000
00001C2C  01020304 05060708                        1288          DC    XL16'01020304 05060708 000A0B0C 0D0E0F10'   v2
00001C34  000A0B0C 0D0E0F10
                                                   1289
                                                   1290          VRR_A VISTR,0,1,0
00001C40                                           1291+         DS    0FD
00001C40                     00001C40              1292+         USING *,R5                base for test data and test routine
00001C40  00001C98                                 1293+T18      DC    A(X18)              address of test routine
00001C44  0012                                     1294+         DC    H'18'               test number
00001C46  00                                       1295+         DC    X'00'
00001C47  00                                       1296+         DC    HL1'0'                   M3 used
00001C48  01                                       1297+         DC    HL1'1'                   M5 used
00001C49  00                                       1298+         DC    HL1'0'              CC
00001C4A  07                                       1299+         DC    HL1'7'              CC failed mask
00001C4C  00000000 00000000                        1300+         DS    2F                  extracted PSW after test (has CC)
00001C54  FF                                       1301+         DC    X'FF'               extracted CC, if test failed
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001C55  E5C9E2E3 D9404040                        1302+          DC    CL8'VISTR'          instruction name
00001C60  00001CC4                                 1303+          DC    A(RE18)             address of v1 result
00001C64  00001CD4                                 1304+          DC    A(RE18+16)          address of v2 source
00001C68  00001CE4                                 1305+          DC    A(RE18+32)          address of v3 source
00001C6C  00000010                                 1306+          DC    A(16)               result length
00001C70  00001CC4                                 1307+REA18     DC    A(RE18)             result address
00001C78  00000000 00000000                        1308+          DS    FD                  gap
00001C80  00000000 00000000                        1309+V1O18     DS    XL16                V1 output
00001C88  00000000 00000000
00001C90  00000000 00000000                        1310+          DS    FD                  gap
                                                   1311+*
00001C98                                           1312+X18       DS    0F
00001C98  4110 8EF8                      000010F8  1313+          LA    R1,V1FUDGE         load v21 fudge
00001C9C  E751 0000 0806                 00000000  1314+          VL    v21,0(R1)
00001CA2  E310 5024 0014                 00000024  1315+          LGF   R1,V2ADDR           load v2 source
00001CA8  E761 0000 0806                 00000000  1316+          VL    v22,0(R1)           use v21 to test decoder
00001CAE  E756 0010 0C5C                           1317+          VISTR V21,V22,0,1                 test instruction
00001CB4  B98D 0020                                1318+          EPSW  R2,R0               extract psw
00001CB8  5020 500C                      0000000C  1319+          ST    R2,CCPSW               to save CC
00001CBC  E750 5040 080E                 00001C80  1320+          VST   V21,V1O18           save v1 output
00001CC2  07FB                                     1321+          BR    R11                 return
00001CC4                                           1322+RE18      DC    0F                  V1 for this test
00001CC4                                           1323+          DROP  R5
00001CC4  01020304 05060700                        1324           DC    XL16'01020304 05060700 00000000 00000000'   v1
00001CCC  00000000 00000000
00001CD4  01020304 05060700                        1325           DC    XL16'01020304 05060700 090A0B0C 0D0E0F10'   v2
00001CDC  090A0B0C 0D0E0F10
                                                   1326
                                                   1327           VRR_A VISTR,0,1,0
00001CE8                                           1328+          DS    0FD
00001CE8                           00001CE8        1329+          USING *,R5                base for test data and test routine
00001CE8  00001D40                                 1330+T19       DC    A(X19)              address of test routine
00001CEC  0013                                     1331+          DC    H'19'               test number
00001CEE  00                                       1332+          DC    X'00'
00001CEF  00                                       1333+          DC    HL1'0'                   M3 used
00001CF0  01                                       1334+          DC    HL1'1'                   M5 used
00001CF1  00                                       1335+          DC    HL1'0'              CC
00001CF2  07                                       1336+          DC    HL1'7'              CC failed mask
00001CF4  00000000 00000000                        1337+          DS    2F                  extracted PSW after test (has CC)
00001CFC  FF                                       1338+          DC    X'FF'               extracted CC, if test failed
00001CFD  E5C9E2E3 D9404040                        1339+          DC    CL8'VISTR'          instruction name
00001D08  00001D6C                                 1340+          DC    A(RE19)             address of v1 result
00001D0C  00001D7C                                 1341+          DC    A(RE19+16)          address of v2 source
00001D10  00001D8C                                 1342+          DC    A(RE19+32)          address of v3 source
00001D14  00000010                                 1343+          DC    A(16)               result length
00001D18  00001D6C                                 1344+REA19     DC    A(RE19)             result address
00001D20  00000000 00000000                        1345+          DS    FD                  gap
00001D28  00000000 00000000                        1346+V1O19     DS    XL16                V1 output
00001D30  00000000 00000000
00001D38  00000000 00000000                        1347+          DS    FD                  gap
                                                   1348+*
00001D40                                           1349+X19       DS    0F
00001D40  4110 8EF8                      000010F8  1350+          LA    R1,V1FUDGE         load v21 fudge
00001D44  E751 0000 0806                 00000000  1351+          VL    v21,0(R1)
00001D4A  E310 5024 0014                 00000024  1352+          LGF   R1,V2ADDR           load v2 source
00001D50  E761 0000 0806                 00000000  1353+          VL    v22,0(R1)           use v21 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001D56  E756 0010 0C5C                          1354+         VISTR V21,V22,0,1               test instruction
00001D5C  B98D 0020                               1355+         EPSW  R2,R0               extract psw
00001D60  5020 500C                     0000000C  1356+         ST    R2,CCPSW               to save CC
00001D64  E750 5040 080E                00001D28  1357+         VST   V21,V1O19           save v1 output
00001D6A  07FB                                    1358+         BR    R11                 return
00001D6C                                          1359+RE19     DC    0F                  V1 for this test
00001D6C                                          1360+         DROP  R5
00001D6C  01020304 05060000                       1361          DC    XL16'01020304 05060000 00000000 00000000'   v1
00001D74  00000000 00000000
00001D7C  01020304 05060008                       1362          DC    XL16'01020304 05060008 090A0B0C 0D0E0F10'   v2
00001D84  090A0B0C 0D0E0F10
                                                  1363
                                                  1364          VRR_A VISTR,0,1,0
00001D90                                          1365+         DS    0FD
00001D90                  00001D90                1366+         USING *,R5                base for test data and test routine
00001D90  00001DE8                                1367+T20      DC    A(X20)              address of test routine
00001D94  0014                                    1368+         DC    H'20'               test number
00001D96  00                                      1369+         DC    X'00'
00001D97  00                                      1370+         DC    HL1'0'                   M3 used
00001D98  01                                      1371+         DC    HL1'1'                   M5 used
00001D99  00                                      1372+         DC    HL1'0'              CC
00001D9A  07                                      1373+         DC    HL1'7'              CC failed mask
00001D9C  00000000 00000000                       1374+         DS    2F                  extracted PSW after test (has CC)
00001DA4  FF                                      1375+         DC    X'FF'               extracted CC, if test failed
00001DA5  E5C9E2E3 D9404040                       1376+         DC    CL8'VISTR'          instruction name
00001DB0  00001E14                                1377+         DC    A(RE20)             address of v1 result
00001DB4  00001E24                                1378+         DC    A(RE20+16)          address of v2 source
00001DB8  00001E34                                1379+         DC    A(RE20+32)          address of v3 source
00001DBC  00000010                                1380+         DC    A(16)               result length
00001DC0  00001E14                                1381+REA20    DC    A(RE20)             result address
00001DC8  00000000 00000000                       1382+         DS    FD                  gap
00001DD0  00000000 00000000                       1383+V1O20    DS    XL16                V1 output
00001DD8  00000000 00000000
00001DE0  00000000 00000000                       1384+         DS    FD                  gap
                                                  1385+*
00001DE8                                          1386+X20      DS    0F
00001DE8  4110 8EF8                     000010F8  1387+         LA    R1,V1FUDGE         load v21 fudge
00001DEC  E751 0000 0806                00000000  1388+         VL    v21,0(R1)
00001DF2  E310 5024 0014                00000024  1389+         LGF   R1,V2ADDR           load v2 source
00001DF8  E761 0000 0806                00000000  1390+         VL    v22,0(R1)           use v21 to test decoder
00001DFE  E756 0010 0C5C                          1391+         VISTR V21,V22,0,1               test instruction
00001E04  B98D 0020                               1392+         EPSW  R2,R0               extract psw
00001E08  5020 500C                     0000000C  1393+         ST    R2,CCPSW               to save CC
00001E0C  E750 5040 080E                00001DD0  1394+         VST   V21,V1O20           save v1 output
00001E12  07FB                                    1395+         BR    R11                 return
00001E14                                          1396+RE20     DC    0F                  V1 for this test
00001E14                                          1397+         DROP  R5
00001E14  01020304 05000000                       1398          DC    XL16'01020304 05000000 00000000 00000000'   v1
00001E1C  00000000 00000000
00001E24  01020304 05000708                       1399          DC    XL16'01020304 05000708 090A0B0C 0D0E0F10'   v2
00001E2C  090A0B0C 0D0E0F10
                                                  1400
                                                  1401          VRR_A VISTR,0,1,0
00001E38                                          1402+         DS    0FD
00001E38                  00001E38                1403+         USING *,R5                base for test data and test routine
00001E38  00001E90                                1404+T21      DC    A(X21)              address of test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001E3C  0015                                    1405+          DC    H'21'              test number
00001E3E  00                                      1406+          DC    X'00'
00001E3F  00                                      1407+          DC    HL1'0'                  M3 used
00001E40  01                                      1408+          DC    HL1'1'                  M5 used
00001E41  00                                      1409+          DC    HL1'0'             CC
00001E42  07                                      1410+          DC    HL1'7'             CC failed mask
00001E44  00000000 00000000                       1411+          DS    2F                 extracted PSW after test (has CC)
00001E4C  FF                                      1412+          DC    X'FF'              extracted CC, if test failed
00001E4D  E5C9E2E3 D9404040                       1413+          DC    CL8'VISTR'         instruction name
00001E58  00001EBC                                1414+          DC    A(RE21)            address of v1 result
00001E5C  00001ECC                                1415+          DC    A(RE21+16)         address of v2 source
00001E60  00001EDC                                1416+          DC    A(RE21+32)         address of v3 source
00001E64  00000010                                1417+          DC    A(16)              result length
00001E68  00001EBC                                1418+REA21     DC    A(RE21)            result address
00001E70  00000000 00000000                       1419+          DS    FD                 gap
00001E78  00000000 00000000                       1420+V1O21     DS    XL16               V1 output
00001E80  00000000 00000000
00001E88  00000000 00000000                       1421+          DS    FD                 gap
                                                  1422+*
00001E90                                          1423+X21       DS    0F
00001E90  4110 8EF8                  000010F8     1424+          LA    R1,V1FUDGE        load v21 fudge
00001E94  E751 0000 0806             00000000     1425+          VL    v21,0(R1)
00001E9A  E310 5024 0014             00000024     1426+          LGF   R1,V2ADDR          load v2 source
00001EA0  E761 0000 0806             00000000     1427+          VL    v22,0(R1)          use v21 to test decoder
00001EA6  E756 0010 0C5C                          1428+          VISTR V21,V22,0,1                test instruction
00001EAC  B98D 0020                               1429+          EPSW  R2,R0              extract psw
00001EB0  5020 500C                  0000000C     1430+          ST    R2,CCPSW                to save CC
00001EB4  E750 5040 080E             00001E78     1431+          VST   V21,V1O21          save v1 output
00001EBA  07FB                                    1432+          BR    R11                return
00001EBC                                          1433+RE21      DC    0F                 V1 for this test
00001EBC                                          1434+          DROP  R5
00001EBC  01020304 00000000                       1435           DC    XL16'01020304 00000000 00000000 00000000'   v1
00001EC4  00000000 00000000
00001ECC  01020304 00060708                       1436           DC    XL16'01020304 00060708 090A0B0C 0D0E0F10'   v2
00001ED4  090A0B0C 0D0E0F10
                                                  1437
                                                  1438           VRR_A VISTR,0,1,0
00001EE0                                          1439+          DS    0FD
00001EE0                       00001EE0           1440+          USING *,R5               base for test data and test routine
00001EE0  00001F38                                1441+T22       DC    A(X22)             address of test routine
00001EE4  0016                                    1442+          DC    H'22'              test number
00001EE6  00                                      1443+          DC    X'00'
00001EE7  00                                      1444+          DC    HL1'0'                  M3 used
00001EE8  01                                      1445+          DC    HL1'1'                  M5 used
00001EE9  00                                      1446+          DC    HL1'0'             CC
00001EEA  07                                      1447+          DC    HL1'7'             CC failed mask
00001EEC  00000000 00000000                       1448+          DS    2F                 extracted PSW after test (has CC)
00001EF4  FF                                      1449+          DC    X'FF'              extracted CC, if test failed
00001EF5  E5C9E2E3 D9404040                       1450+          DC    CL8'VISTR'         instruction name
00001F00  00001F64                                1451+          DC    A(RE22)            address of v1 result
00001F04  00001F74                                1452+          DC    A(RE22+16)         address of v2 source
00001F08  00001F84                                1453+          DC    A(RE22+32)         address of v3 source
00001F0C  00000010                                1454+          DC    A(16)              result length
00001F10  00001F64                                1455+REA22     DC    A(RE22)            result address
00001F18  00000000 00000000                       1456+          DS    FD                 gap
00001F20  00000000 00000000                       1457+V1O22     DS    XL16               V1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001F28  00000000 00000000
00001F30  00000000 00000000                        1458+         DS    FD                  gap
                                                   1459+*
00001F38                                           1460+X22      DS    0F
00001F38  4110 8EF8                      000010F8  1461+         LA    R1,V1FUDGE        load v21 fudge
00001F3C  E751 0000 0806                 00000000  1462+         VL    v21,0(R1)
00001F42  E310 5024 0014                 00000024  1463+         LGF   R1,V2ADDR          load v2 source
00001F48  E761 0000 0806                 00000000  1464+         VL    v22,0(R1)          use v21 to test decoder
00001F4E  E756 0010 0C5C                           1465+         VISTR V21,V22,0,1                test instruction
00001F54  B98D 0020                                1466+         EPSW  R2,R0              extract psw
00001F58  5020 500C                      0000000C  1467+         ST    R2,CCPSW              to save CC
00001F5C  E750 5040 080E                 00001F20  1468+         VST   V21,V1O22          save v1 output
00001F62  07FB                                     1469+         BR    R11                return
00001F64                                           1470+RE22     DC    0F                 V1 for this test
00001F64                                           1471+         DROP  R5
00001F64  01020300 00000000                        1472          DC    XL16'01020300 00000000 00000000 00000000'   v1
00001F6C  00000000 00000000
00001F74  01020300 05060708                        1473          DC    XL16'01020300 05060708 090A0B0C 0D0E0F10'   v2
00001F7C  090A0B0C 0D0E0F10
                                                   1474
                                                   1475          VRR_A VISTR,0,1,0
00001F88                                           1476+         DS    0FD
00001F88                       00001F88            1477+         USING *,R5               base for test data and test routine
00001F88  00001FE0                                 1478+T23      DC    A(X23)             address of test routine
00001F8C  0017                                     1479+         DC    H'23'              test number
00001F8E  00                                       1480+         DC    X'00'
00001F8F  00                                       1481+         DC    HL1'0'                  M3 used
00001F90  01                                       1482+         DC    HL1'1'                  M5 used
00001F91  00                                       1483+         DC    HL1'0'             CC
00001F92  07                                       1484+         DC    HL1'7'             CC failed mask
00001F94  00000000 00000000                        1485+         DS    2F                 extracted PSW after test (has CC)
00001F9C  FF                                       1486+         DC    X'FF'              extracted CC, if test failed
00001F9D  E5C9E2E3 D9404040                        1487+         DC    CL8'VISTR'         instruction name
00001FA8  0000200C                                 1488+         DC    A(RE23)            address of v1 result
00001FAC  0000201C                                 1489+         DC    A(RE23+16)         address of v2 source
00001FB0  0000202C                                 1490+         DC    A(RE23+32)         address of v3 source
00001FB4  00000010                                 1491+         DC    A(16)              result length
00001FB8  0000200C                                 1492+REA23    DC    A(RE23)            result address
00001FC0  00000000 00000000                        1493+         DS    FD                 gap
00001FC8  00000000 00000000                        1494+V1O23    DS    XL16               V1 output
00001FD0  00000000 00000000
00001FD8  00000000 00000000                        1495+         DS    FD                 gap
                                                   1496+*
00001FE0                                           1497+X23      DS    0F
00001FE0  4110 8EF8                      000010F8  1498+         LA    R1,V1FUDGE        load v21 fudge
00001FE4  E751 0000 0806                 00000000  1499+         VL    v21,0(R1)
00001FEA  E310 5024 0014                 00000024  1500+         LGF   R1,V2ADDR          load v2 source
00001FF0  E761 0000 0806                 00000000  1501+         VL    v22,0(R1)          use v21 to test decoder
00001FF6  E756 0010 0C5C                           1502+         VISTR V21,V22,0,1                test instruction
00001FFC  B98D 0020                                1503+         EPSW  R2,R0              extract psw
00002000  5020 500C                      0000000C  1504+         ST    R2,CCPSW              to save CC
00002004  E750 5040 080E                 00001FC8  1505+         VST   V21,V1O23          save v1 output
0000200A  07FB                                     1506+         BR    R11                return
0000200C                                           1507+RE23     DC    0F                 V1 for this test
0000200C                                           1508+         DROP  R5
0000200C  01020000 00000000                        1509          DC    XL16'01020000 00000000 00000000 00000000'   v1
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002014  00000000 00000000
0000201C  01020004 05060708                        1510          DC    XL16'01020004 05060708 090A0B0C 0D0E0F10'   v2
00002024  090A0B0C 0D0E0F10
                                                   1511
                                                   1512          VRR_A VISTR,0,1,0
00002030                                           1513+         DS    0FD
00002030                     00002030              1514+         USING *,R5               base for test data and test routine
00002030  00002088                                 1515+T24      DC    A(X24)             address of test routine
00002034  0018                                     1516+         DC    H'24'              test number
00002036  00                                       1517+         DC    X'00'
00002037  00                                       1518+         DC    HL1'0'                  M3 used
00002038  01                                       1519+         DC    HL1'1'                  M5 used
00002039  00                                       1520+         DC    HL1'0'             CC
0000203A  07                                       1521+         DC    HL1'7'             CC failed mask
0000203C  00000000 00000000                        1522+         DS    2F                 extracted PSW after test (has CC)
00002044  FF                                       1523+         DC    X'FF'              extracted CC, if test failed
00002045  E5C9E2E3 D9404040                        1524+         DC    CL8'VISTR'         instruction name
00002050  000020B4                                 1525+         DC    A(RE24)            address of v1 result
00002054  000020C4                                 1526+         DC    A(RE24+16)         address of v2 source
00002058  000020D4                                 1527+         DC    A(RE24+32)         address of v3 source
0000205C  00000010                                 1528+         DC    A(16)              result length
00002060  000020B4                                 1529+REA24    DC    A(RE24)            result address
00002068  00000000 00000000                        1530+         DS    FD                 gap
00002070  00000000 00000000                        1531+V1O24    DS    XL16               V1 output
00002078  00000000 00000000
00002080  00000000 00000000                        1532+         DS    FD                 gap
                                                   1533+*
00002088                                           1534+X24      DS    0F
00002088  4110 8EF8                     000010F8   1535+         LA    R1,V1FUDGE       load v21 fudge
0000208C  E751 0000 0806                00000000   1536+         VL    v21,0(R1)
00002092  E310 5024 0014                00000024   1537+         LGF   R1,V2ADDR         load v2 source
00002098  E761 0000 0806                00000000   1538+         VL    v22,0(R1)          use v21 to test decoder
0000209E  E756 0010 0C5C                           1539+         VISTR V21,V22,0,1                test instruction
000020A4  B98D 0020                                1540+         EPSW  R2,R0              extract psw
000020A8  5020 500C                     0000000C   1541+         ST    R2,CCPSW              to save CC
000020AC  E750 5040 080E                00002070   1542+         VST   V21,V1O24          save v1 output
000020B2  07FB                                     1543+         BR    R11                return
000020B4                                           1544+RE24     DC    0F                 V1 for this test
000020B4                                           1545+         DROP  R5
000020B4  01000000 00000000                        1546          DC    XL16'01000000 00000000 00000000 00000000'   v1
000020BC  00000000 00000000
000020C4  01000304 05060708                        1547          DC    XL16'01000304 05060708 090A0B0C 0D0E0F10'   v2
000020CC  090A0B0C 0D0E0F10
                                                   1548
                                                   1549          VRR_A VISTR,0,1,0
000020D8                                           1550+         DS    0FD
000020D8                     000020D8              1551+         USING *,R5               base for test data and test routine
000020D8  00002130                                 1552+T25      DC    A(X25)             address of test routine
000020DC  0019                                     1553+         DC    H'25'              test number
000020DE  00                                       1554+         DC    X'00'
000020DF  00                                       1555+         DC    HL1'0'                  M3 used
000020E0  01                                       1556+         DC    HL1'1'                  M5 used
000020E1  00                                       1557+         DC    HL1'0'             CC
000020E2  07                                       1558+         DC    HL1'7'             CC failed mask
000020E4  00000000 00000000                        1559+         DS    2F                 extracted PSW after test (has CC)
000020EC  FF                                       1560+         DC    X'FF'              extracted CC, if test failed
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000020ED  E5C9E2E3 D9404040                      1561+          DC    CL8'VISTR'          instruction name
000020F8  0000215C                               1562+          DC    A(RE25)             address of v1 result
000020FC  0000216C                               1563+          DC    A(RE25+16)          address of v2 source
00002100  0000217C                               1564+          DC    A(RE25+32)          address of v3 source
00002104  00000010                               1565+          DC    A(16)               result length
00002108  0000215C                               1566+REA25     DC    A(RE25)             result address
00002110  00000000 00000000                      1567+          DS    FD                  gap
00002118  00000000 00000000                      1568+V1O25     DS    XL16                V1 output
00002120  00000000 00000000
00002128  00000000 00000000                      1569+          DS    FD                  gap
                                                 1570+*
00002130                                         1571+X25       DS    0F
00002130  4110 8EF8                    000010F8  1572+          LA    R1,V1FUDGE         load v21 fudge
00002134  E751 0000 0806               00000000  1573+          VL    v21,0(R1)
0000213A  E310 5024 0014               00000024  1574+          LGF   R1,V2ADDR           load v2 source
00002140  E761 0000 0806               00000000  1575+          VL    v22,0(R1)           use v21 to test decoder
00002146  E756 0010 0C5C                         1576+          VISTR V21,V22,0,1                 test instruction
0000214C  B98D 0020                              1577+          EPSW  R2,R0               extract psw
00002150  5020 500C                    0000000C  1578+          ST    R2,CCPSW               to save CC
00002154  E750 5040 080E               00002118  1579+          VST   V21,V1O25           save v1 output
0000215A  07FB                                   1580+          BR    R11                 return
0000215C                                         1581+RE25      DC    0F                  V1 for this test
0000215C                                         1582+          DROP  R5
0000215C  00000000 00000000                      1583           DC    XL16'00000000 00000000 00000000 00000000'   v1
00002164  00000000 00000000
0000216C  00020304 05060708                      1584           DC    XL16'00020304 05060708 090A0B0C 0D0E0F10'   v2
00002174  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   1586 *halfword
                                                   1587          VRR_A VISTR,1,1,3
00002180                                           1588+         DS    0FD
00002180                     00002180              1589+         USING *,R5              base for test data and test routine
00002180  000021D8                                 1590+T26      DC    A(X26)            address of test routine
00002184  001A                                     1591+         DC    H'26'             test number
00002186  00                                       1592+         DC    X'00'
00002187  01                                       1593+         DC    HL1'1'                 M3 used
00002188  01                                       1594+         DC    HL1'1'                 M5 used
00002189  03                                       1595+         DC    HL1'3'            CC
0000218A  0E                                       1596+         DC    HL1'14'           CC failed mask
0000218C  00000000 00000000                        1597+         DS    2F                extracted PSW after test (has CC)
00002194  FF                                       1598+         DC    X'FF'             extracted CC, if test failed
00002195  E5C9E2E3 D9404040                       1599+         DC    CL8'VISTR'        instruction name
000021A0  00002204                                 1600+         DC    A(RE26)           address of v1 result
000021A4  00002214                                 1601+         DC    A(RE26+16)        address of v2 source
000021A8  00002224                                 1602+         DC    A(RE26+32)        address of v3 source
000021AC  00000010                                 1603+         DC    A(16)             result length
000021B0  00002204                                 1604+REA26    DC    A(RE26)           result address
000021B8  00000000 00000000                        1605+         DS    FD                gap
000021C0  00000000 00000000                        1606+V1O26    DS    XL16              V1 output
000021C8  00000000 00000000
000021D0  00000000 00000000                        1607+         DS    FD                gap
                                                   1608+*
000021D8                                           1609+X26      DS    0F
000021D8  4110 8EF8                      000010F8  1610+         LA    R1,V1FUDGE        load v21 fudge
000021DC  E751 0000 0806                 00000000  1611+         VL    v21,0(R1)
000021E2  E310 5024 0014                 00000024  1612+         LGF   R1,V2ADDR         load v2 source
000021E8  E761 0000 0806                 00000000  1613+         VL    v22,0(R1)         use v21 to test decoder
000021EE  E756 0010 1C5C                           1614+         VISTR V21,V22,1,1               test instruction
000021F4  B98D 0020                                1615+         EPSW  R2,R0             extract psw
000021F8  5020 500C                      0000000C  1616+         ST    R2,CCPSW             to save CC
000021FC  E750 5040 080E                 000021C0  1617+         VST   V21,V1O26         save v1 output
00002202  07FB                                     1618+         BR    R11               return
00002204                                           1619+RE26     DC    0F                V1 for this test
00002204                                           1620+         DROP  R5
00002204  88888888 77777777                        1621          DC    XL16'88888888 77777777 66666666 55555555'   v1
0000220C  66666666 55555555
00002214  88888888 77777777                        1622          DC    XL16'88888888 77777777 66666666 55555555'   v2
0000221C  66666666 55555555
                                                   1623
                                                   1624          VRR_A VISTR,1,1,0
00002228                                           1625+         DS    0FD
00002228                     00002228              1626+         USING *,R5              base for test data and test routine
00002228  00002280                                 1627+T27      DC    A(X27)            address of test routine
0000222C  001B                                     1628+         DC    H'27'             test number
0000222E  00                                       1629+         DC    X'00'
0000222F  01                                       1630+         DC    HL1'1'                 M3 used
00002230  01                                       1631+         DC    HL1'1'                 M5 used
00002231  00                                       1632+         DC    HL1'0'            CC
00002232  07                                       1633+         DC    HL1'7'            CC failed mask
00002234  00000000 00000000                        1634+         DS    2F                extracted PSW after test (has CC)
0000223C  FF                                       1635+         DC    X'FF'             extracted CC, if test failed
0000223D  E5C9E2E3 D9404040                        1636+         DC    CL8'VISTR'        instruction name
00002248  000022AC                                 1637+         DC    A(RE27)           address of v1 result
0000224C  000022BC                                 1638+         DC    A(RE27+16)        address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002250  000022CC                                1639+          DC    A(RE27+32)          address of v3 source
00002254  00000010                                1640+          DC    A(16)               result length
00002258  000022AC                                1641+REA27     DC    A(RE27)             result address
00002260  00000000 00000000                       1642+          DS    FD                  gap
00002268  00000000 00000000                       1643+V1O27     DS    XL16                V1 output
00002270  00000000 00000000
00002278  00000000 00000000                       1644+          DS    FD                  gap
                                                  1645+*
00002280                                          1646+X27       DS    0F
00002280  4110 8EF8                     000010F8  1647+          LA    R1,V1FUDGE        load v21 fudge
00002284  E751 0000 0806                00000000  1648+          VL    v21,0(R1)
0000228A  E310 5024 0014                00000024  1649+          LGF   R1,V2ADDR          load v2 source
00002290  E761 0000 0806                00000000  1650+          VL    v22,0(R1)          use v21 to test decoder
00002296  E756 0010 1C5C                          1651+          VISTR V21,V22,1,1                test instruction
0000229C  B98D 0020                               1652+          EPSW  R2,R0              extract psw
000022A0  5020 500C                     0000000C  1653+          ST    R2,CCPSW              to save CC
000022A4  E750 5040 080E                00002268  1654+          VST   V21,V1O27          save v1 output
000022AA  07FB                                    1655+          BR    R11                return
000022AC                                          1656+RE27      DC    0F                 V1 for this test
000022AC                                          1657+          DROP  R5
000022AC  88888888 77777777                       1658           DC    XL16'88888888 77777777 66666666 55550000'   v1
000022B4  66666666 55550000
000022BC  88888888 77777777                       1659           DC    XL16'88888888 77777777 66666666 55550000'   v2
000022C4  66666666 55550000
                                                  1660
                                                  1661           VRR_A VISTR,1,1,0

000022D0                                          1662+          DS    0FD
000022D0                  000022D0                1663+          USING *,R5               base for test data and test routine
000022D0  00002328                                1664+T28       DC    A(X28)             address of test routine
000022D4  001C                                    1665+          DC    H'28'              test number
000022D6  00                                      1666+          DC    X'00'
000022D7  01                                      1667+          DC    HL1'1'                  M3 used
000022D8  01                                      1668+          DC    HL1'1'                  M5 used
000022D9  00                                      1669+          DC    HL1'0'             CC
000022DA  07                                      1670+          DC    HL1'7'             CC failed mask
000022DC  00000000 00000000                       1671+          DS    2F                 extracted PSW after test (has CC)
000022E4  FF                                      1672+          DC    X'FF'              extracted CC, if test failed
000022E5  E5C9E2E3 D9404040                       1673+          DC    CL8'VISTR'         instruction name
000022F0  00002354                                1674+          DC    A(RE28)            address of v1 result
000022F4  00002364                                1675+          DC    A(RE28+16)         address of v2 source
000022F8  00002374                                1676+          DC    A(RE28+32)         address of v3 source
000022FC  00000010                                1677+          DC    A(16)              result length
00002300  00002354                                1678+REA28     DC    A(RE28)            result address
00002308  00000000 00000000                       1679+          DS    FD                 gap
00002310  00000000 00000000                       1680+V1O28     DS    XL16               V1 output
00002318  00000000 00000000
00002320  00000000 00000000                       1681+          DS    FD                 gap
                                                  1682+*
00002328                                          1683+X28       DS    0F
00002328  4110 8EF8                     000010F8  1684+          LA    R1,V1FUDGE        load v21 fudge
0000232C  E751 0000 0806                00000000  1685+          VL    v21,0(R1)
00002332  E310 5024 0014                00000024  1686+          LGF   R1,V2ADDR          load v2 source
00002338  E761 0000 0806                00000000  1687+          VL    v22,0(R1)          use v21 to test decoder
0000233E  E756 0010 1C5C                          1688+          VISTR V21,V22,1,1                test instruction
00002344  B98D 0020                               1689+          EPSW  R2,R0              extract psw
00002348  5020 500C                     0000000C  1690+          ST    R2,CCPSW              to save CC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000234C  E750 5040 080E                 00002310  1691+          VST   V21,V1O28          save v1 output
00002352  07FB                                     1692+          BR    R11               return
00002354                                           1693+RE28      DC    0F                V1 for this test
00002354                                           1694+          DROP  R5
00002354  88888888 77777777                        1695           DC    XL16'88888888 77777777 66666666 00000000'   v1
0000235C  66666666 00000000
00002364  88888888 77777777                        1696           DC    XL16'88888888 77777777 66666666 00005555'   v2
0000236C  66666666 00005555
                                                   1697
                                                   1698           VRR_A VISTR,1,1,0
00002378                                           1699+          DS    0FD
00002378                    00002378               1700+          USING *,R5              base for test data and test routine
00002378  000023D0                                 1701+T29       DC    A(X29)            address of test routine
0000237C  001D                                     1702+          DC    H'29'             test number
0000237E  00                                       1703+          DC    X'00'
0000237F  01                                       1704+          DC    HL1'1'                 M3 used
00002380  01                                       1705+          DC    HL1'1'                 M5 used
00002381  00                                       1706+          DC    HL1'0'            CC
00002382  07                                       1707+          DC    HL1'7'            CC failed mask
00002384  00000000 00000000                        1708+          DS    2F                extracted PSW after test (has CC)
0000238C  FF                                       1709+          DC    X'FF'             extracted CC, if test failed
0000238D  E5C9E2E3 D9404040                        1710+          DC    CL8'VISTR'        instruction name
00002398  000023FC                                 1711+          DC    A(RE29)           address of v1 result
0000239C  0000240C                                 1712+          DC    A(RE29+16)        address of v2 source
000023A0  0000241C                                 1713+          DC    A(RE29+32)        address of v3 source
000023A4  00000010                                 1714+          DC    A(16)             result length
000023A8  000023FC                                 1715+REA29     DC    A(RE29)           result address
000023B0  00000000 00000000                        1716+          DS    FD                gap
000023B8  00000000 00000000                        1717+V1O29     DS    XL16              V1 output
000023C0  00000000 00000000
000023C8  00000000 00000000                        1718+          DS    FD                gap
                                                   1719+*
000023D0                                           1720+X29       DS    0F
000023D0  4110 8EF8                      000010F8  1721+          LA    R1,V1FUDGE       load v21 fudge
000023D4  E751 0000 0806                 00000000  1722+          VL    v21,0(R1)
000023DA  E310 5024 0014                 00000024  1723+          LGF   R1,V2ADDR          load v2 source
000023E0  E761 0000 0806                 00000000  1724+          VL    v22,0(R1)         use v21 to test decoder
000023E6  E756 0010 1C5C                           1725+          VISTR V21,V22,1,1               test instruction
000023EC  B98D 0020                                1726+          EPSW  R2,R0             extract psw
000023F0  5020 500C                      0000000C  1727+          ST    R2,CCPSW             to save CC
000023F4  E750 5040 080E                 000023B8  1728+          VST   V21,V1O29           save v1 output
000023FA  07FB                                     1729+          BR    R11               return
000023FC                                           1730+RE29      DC    0F                V1 for this test
000023FC                                           1731+          DROP  R5
000023FC  88888888 77777777                        1732           DC    XL16'88888888 77777777 66660000 00000000'   v1
00002404  66660000 00000000
0000240C  88888888 77777777                        1733           DC    XL16'88888888 77777777 66660000 55555555'   v2
00002414  66660000 55555555
                                                   1734
                                                   1735           VRR_A VISTR,1,1,0
00002420                                           1736+          DS    0FD
00002420                    00002420               1737+          USING *,R5              base for test data and test routine
00002420  00002478                                 1738+T30       DC    A(X30)            address of test routine
00002424  001E                                     1739+          DC    H'30'             test number
00002426  00                                       1740+          DC    X'00'
00002427  01                                       1741+          DC    HL1'1'                 M3 used
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002428  01                                      1742+         DC    HL1'1'                 M5 used
00002429  00                                      1743+         DC    HL1'0'               CC
0000242A  07                                      1744+         DC    HL1'7'               CC failed mask
0000242C  00000000 00000000                       1745+         DS    2F                   extracted PSW after test (has CC)
00002434  FF                                      1746+         DC    X'FF'                extracted CC, if test failed
00002435  E5C9E2E3 D9404040                       1747+         DC    CL8'VISTR'           instruction name
00002440  000024A4                                1748+         DC    A(RE30)              address of v1 result
00002444  000024B4                                1749+         DC    A(RE30+16)           address of v2 source
00002448  000024C4                                1750+         DC    A(RE30+32)           address of v3 source
0000244C  00000010                                1751+         DC    A(16)                result length
00002450  000024A4                                1752+REA30    DC    A(RE30)              result address
00002458  00000000 00000000                       1753+         DS    FD                   gap
00002460  00000000 00000000                       1754+V1O30    DS    XL16                 V1 output
00002468  00000000 00000000
00002470  00000000 00000000                       1755+         DS    FD                   gap
                                                  1756+*
00002478                                          1757+X30      DS    0F
00002478  4110 8EF8                    000010F8   1758+         LA    R1,V1FUDGE         load v21 fudge
0000247C  E751 0000 0806               00000000   1759+         VL    v21,0(R1)
00002482  E310 5024 0014               00000024   1760+         LGF   R1,V2ADDR           load v2 source
00002488  E761 0000 0806               00000000   1761+         VL    v22,0(R1)           use v21 to test decoder
0000248E  E756 0010 1C5C                          1762+         VISTR V21,V22,1,1                 test instruction
00002494  B98D 0020                               1763+         EPSW  R2,R0               extract psw
00002498  5020 500C                    0000000C   1764+         ST    R2,CCPSW               to save CC
0000249C  E750 5040 080E               00002460   1765+         VST   V21,V1O30           save v1 output
000024A2  07FB                                    1766+         BR    R11                 return
000024A4                                          1767+RE30     DC    0F                  V1 for this test
000024A4                                          1768+         DROP  R5
000024A4  88888888 77777777                      1769          DC    XL16'88888888 77777777 00000000 00000000'   v1
000024AC  00000000 00000000
000024B4  88888888 77777777                      1770          DC    XL16'88888888 77777777 00006666 55555555'   v2
000024BC  00006666 55555555
                                                  1771
                                                  1772          VRR_A VISTR,1,1,0
000024C8                                          1773+         DS    0FD
000024C8                       000024C8           1774+         USING *,R5                base for test data and test routine
000024C8  00002520                                1775+T31      DC    A(X31)              address of test routine
000024CC  001F                                    1776+         DC    H'31'               test number
000024CE  00                                      1777+         DC    X'00'
000024CF  01                                      1778+         DC    HL1'1'                 M3 used
000024D0  01                                      1779+         DC    HL1'1'                 M5 used
000024D1  00                                      1780+         DC    HL1'0'               CC
000024D2  07                                      1781+         DC    HL1'7'               CC failed mask
000024D4  00000000 00000000                       1782+         DS    2F                   extracted PSW after test (has CC)
000024DC  FF                                      1783+         DC    X'FF'                extracted CC, if test failed
000024DD  E5C9E2E3 D9404040                       1784+         DC    CL8'VISTR'           instruction name
000024E8  0000254C                                1785+         DC    A(RE31)              address of v1 result
000024EC  0000255C                                1786+         DC    A(RE31+16)           address of v2 source
000024F0  0000256C                                1787+         DC    A(RE31+32)           address of v3 source
000024F4  00000010                                1788+         DC    A(16)                result length
000024F8  0000254C                                1789+REA31    DC    A(RE31)              result address
00002500  00000000 00000000                       1790+         DS    FD                   gap
00002508  00000000 00000000                       1791+V1O31    DS    XL16                 V1 output
00002510  00000000 00000000
00002518  00000000 00000000                       1792+         DS    FD                   gap
                                                  1793+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002520                                           1794+X31      DS    0F
00002520  4110 8EF8                      000010F8  1795+          LA    R1,V1FUDGE         load v21 fudge
00002524  E751 0000 0806                 00000000  1796+          VL    v21,0(R1)
0000252A  E310 5024 0014                 00000024  1797+          LGF   R1,V2ADDR           load v2 source
00002530  E761 0000 0806                 00000000  1798+          VL    v22,0(R1)           use v21 to test decoder
00002536  E756 0010 1C5C                           1799+          VISTR V21,V22,1,1                 test instruction
0000253C  B98D 0020                                1800+          EPSW  R2,R0               extract psw
00002540  5020 500C                      0000000C  1801+          ST    R2,CCPSW               to save CC
00002544  E750 5040 080E                 00002508  1802+          VST   V21,V1O31           save v1 output
0000254A  07FB                                     1803+          BR    R11                 return
0000254C                                           1804+RE31     DC    0F                  V1 for this test
0000254C                                           1805+          DROP  R5
0000254C  88888888 77770000                        1806           DC    XL16'88888888 77770000 00000000 00000000'   v1
00002554  00000000 00000000
0000255C  88888888 77770000                        1807           DC    XL16'88888888 77770000 66666666 55555555'   v2
00002564  66666666 55555555
                                                   1808
                                                   1809           VRR_A VISTR,1,1,0
00002570                                           1810+          DS    0FD
00002570                         00002570          1811+          USING *,R5                base for test data and test routine
00002570  000025C8                                 1812+T32      DC    A(X32)              address of test routine
00002574  0020                                     1813+          DC    H'32'               test number
00002576  00                                       1814+          DC    X'00'
00002577  01                                       1815+          DC    HL1'1'                  M3 used
00002578  01                                       1816+          DC    HL1'1'                  M5 used
00002579  00                                       1817+          DC    HL1'0'              CC
0000257A  07                                       1818+          DC    HL1'7'              CC failed mask
0000257C  00000000 00000000                        1819+          DS    2F                  extracted PSW after test (has CC)
00002584  FF                                       1820+          DC    X'FF'               extracted CC, if test failed
00002585  E5C9E2E3 D9404040                       1821+          DC    CL8'VISTR'          instruction name
00002590  000025F4                                 1822+          DC    A(RE32)             address of v1 result
00002594  00002604                                 1823+          DC    A(RE32+16)          address of v2 source
00002598  00002614                                 1824+          DC    A(RE32+32)          address of v3 source
0000259C  00000010                                 1825+          DC    A(16)               result length
000025A0  000025F4                                 1826+REA32    DC    A(RE32)             result address
000025A8  00000000 00000000                        1827+          DS    FD                  gap
000025B0  00000000 00000000                        1828+V1O32    DS    XL16                V1 output
000025B8  00000000 00000000
000025C0  00000000 00000000                        1829+          DS    FD                  gap
                                                   1830+*
000025C8                                           1831+X32      DS    0F
000025C8  4110 8EF8                      000010F8  1832+          LA    R1,V1FUDGE         load v21 fudge
000025CC  E751 0000 0806                 00000000  1833+          VL    v21,0(R1)
000025D2  E310 5024 0014                 00000024  1834+          LGF   R1,V2ADDR           load v2 source
000025D8  E761 0000 0806                 00000000  1835+          VL    v22,0(R1)           use v21 to test decoder
000025DE  E756 0010 1C5C                           1836+          VISTR V21,V22,1,1                 test instruction
000025E4  B98D 0020                                1837+          EPSW  R2,R0               extract psw
000025E8  5020 500C                      0000000C  1838+          ST    R2,CCPSW               to save CC
000025EC  E750 5040 080E                 000025B0  1839+          VST   V21,V1O32           save v1 output
000025F2  07FB                                     1840+          BR    R11                 return
000025F4                                           1841+RE32     DC    0F                  V1 for this test
000025F4                                           1842+          DROP  R5
000025F4  88888888 00000000                        1843           DC    XL16'88888888 00000000 00000000 00000000'   v1
000025FC  00000000 00000000
00002604  88888888 00007777                        1844           DC    XL16'88888888 00007777 66666666 55555555'   v2
0000260C  66666666 55555555
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1845
                                                    1846          VRR_A VISTR,1,1,0
00002618                                            1847+         DS    0FD
00002618                      00002618              1848+         USING *,R5              base for test data and test routine
00002618  00002670                                  1849+T33      DC    A(X33)            address of test routine
0000261C  0021                                      1850+         DC    H'33'             test number
0000261E  00                                        1851+         DC    X'00'
0000261F  01                                        1852+         DC    HL1'1'                 M3 used
00002620  01                                        1853+         DC    HL1'1'                 M5 used
00002621  00                                        1854+         DC    HL1'0'            CC
00002622  07                                        1855+         DC    HL1'7'            CC failed mask
00002624  00000000 00000000                         1856+         DS    2F                extracted PSW after test (has CC)
0000262C  FF                                        1857+         DC    X'FF'             extracted CC, if test failed
0000262D  E5C9E2E3 D9404040                         1858+         DC    CL8'VISTR'        instruction name
00002638  0000269C                                  1859+         DC    A(RE33)           address of v1 result
0000263C  000026AC                                  1860+         DC    A(RE33+16)        address of v2 source
00002640  000026BC                                  1861+         DC    A(RE33+32)        address of v3 source
00002644  00000010                                  1862+         DC    A(16)             result length
00002648  0000269C                                  1863+REA33    DC    A(RE33)           result address
00002650  00000000 00000000                         1864+         DS    FD                gap
00002658  00000000 00000000                         1865+V1O33    DS    XL16              V1 output
00002660  00000000 00000000
00002668  00000000 00000000                         1866+         DS    FD                gap
                                                    1867+*
00002670                                            1868+X33      DS    0F
00002670  4110 8EF8                       000010F8  1869+         LA    R1,V1FUDGE        load v21 fudge
00002674  E751 0000 0806                  00000000  1870+         VL    v21,0(R1)
0000267A  E310 5024 0014                  00000024  1871+         LGF   R1,V2ADDR         load v2 source
00002680  E761 0000 0806                  00000000  1872+         VL    v22,0(R1)         use v21 to test decoder
00002686  E756 0010 1C5C                            1873+         VISTR V21,V22,1,1               test instruction
0000268C  B98D 0020                                 1874+         EPSW  R2,R0             extract psw
00002690  5020 500C                       0000000C  1875+         ST    R2,CCPSW             to save CC
00002694  E750 5040 080E                  00002658  1876+         VST   V21,V1O33         save v1 output
0000269A  07FB                                      1877+         BR    R11               return
0000269C                                            1878+RE33     DC    0F                V1 for this test
0000269C                                            1879+         DROP  R5
0000269C  88880000 00000000                         1880          DC    XL16'88880000 00000000 00000000 00000000'   v1
000026A4  00000000 00000000
000026AC  88880000 77777777                         1881          DC    XL16'88880000 77777777 66666666 55555555'   v2
000026B4  66666666 55555555
                                                    1882
                                                    1883          VRR_A VISTR,1,1,0
000026C0                                            1884+         DS    0FD
000026C0                      000026C0              1885+         USING *,R5              base for test data and test routine
000026C0  00002718                                  1886+T34      DC    A(X34)            address of test routine
000026C4  0022                                      1887+         DC    H'34'             test number
000026C6  00                                        1888+         DC    X'00'
000026C7  01                                        1889+         DC    HL1'1'                 M3 used
000026C8  01                                        1890+         DC    HL1'1'                 M5 used
000026C9  00                                        1891+         DC    HL1'0'            CC
000026CA  07                                        1892+         DC    HL1'7'            CC failed mask
000026CC  00000000 00000000                         1893+         DS    2F                extracted PSW after test (has CC)
000026D4  FF                                        1894+         DC    X'FF'             extracted CC, if test failed
000026D5  E5C9E2E3 D9404040                         1895+         DC    CL8'VISTR'        instruction name
000026E0  00002744                                  1896+         DC    A(RE34)           address of v1 result
000026E4  00002754                                  1897+         DC    A(RE34+16)        address of v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000026E8  00002764                                1898+          DC    A(RE34+32)          address of v3 source
000026EC  00000010                                1899+          DC    A(16)               result length
000026F0  00002744                                1900+REA34     DC    A(RE34)             result address
000026F8  00000000 00000000                       1901+          DS    FD                  gap
00002700  00000000 00000000                       1902+V1O34     DS    XL16                V1 output
00002708  00000000 00000000
00002710  00000000 00000000                       1903+          DS    FD                  gap
                                                  1904+*
00002718                                          1905+X34       DS    0F
00002718  4110 8EF8                     000010F8  1906+          LA    R1,V1FUDGE        load v21 fudge
0000271C  E751 0000 0806                00000000  1907+          VL    v21,0(R1)
00002722  E310 5024 0014                00000024  1908+          LGF   R1,V2ADDR          load v2 source
00002728  E761 0000 0806                00000000  1909+          VL    v22,0(R1)          use v21 to test decoder
0000272E  E756 0010 1C5C                          1910+          VISTR V21,V22,1,1                test instruction
00002734  B98D 0020                               1911+          EPSW  R2,R0              extract psw
00002738  5020 500C                     0000000C  1912+          ST    R2,CCPSW              to save CC
0000273C  E750 5040 080E                00002700  1913+          VST   V21,V1O34          save v1 output
00002742  07FB                                    1914+          BR    R11                return
00002744                                          1915+RE34      DC    0F                 V1 for this test
00002744                                          1916+          DROP  R5
00002744  00000000 00000000                       1917           DC    XL16'00000000 00000000 00000000 00000000'   v1
0000274C  00000000 00000000
00002754  00008888 77777777                       1918           DC    XL16'00008888 77777777 66666666 55555555'   v2
0000275C  66666666 55555555
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1920 *word
                                                   1921          VRR_A VISTR,2,1,3
00002768                                           1922+         DS    0FD
00002768                     00002768              1923+         USING *,R5              base for test data and test routine
00002768  000027C0                                 1924+T35      DC    A(X35)            address of test routine
0000276C  0023                                     1925+         DC    H'35'             test number
0000276E  00                                       1926+         DC    X'00'
0000276F  02                                       1927+         DC    HL1'2'                 M3 used
00002770  01                                       1928+         DC    HL1'1'                 M5 used
00002771  03                                       1929+         DC    HL1'3'            CC
00002772  0E                                       1930+         DC    HL1'14'           CC failed mask
00002774  00000000 00000000                        1931+         DS    2F                extracted PSW after test (has CC)
0000277C  FF                                       1932+         DC    X'FF'             extracted CC, if test failed
0000277D  E5C9E2E3 D9404040                        1933+         DC    CL8'VISTR'        instruction name
00002788  000027EC                                 1934+         DC    A(RE35)           address of v1 result
0000278C  000027FC                                 1935+         DC    A(RE35+16)        address of v2 source
00002790  0000280C                                 1936+         DC    A(RE35+32)        address of v3 source
00002794  00000010                                 1937+         DC    A(16)             result length
00002798  000027EC                                 1938+REA35    DC    A(RE35)           result address
000027A0  00000000 00000000                        1939+         DS    FD                gap
000027A8  00000000 00000000                        1940+V1O35    DS    XL16              V1 output
000027B0  00000000 00000000
000027B8  00000000 00000000                        1941+         DS    FD                gap
                                                   1942+*
000027C0                                           1943+X35      DS    0F
000027C0  4110 8EF8                     000010F8   1944+         LA    R1,V1FUDGE        load v21 fudge
000027C4  E751 0000 0806                00000000   1945+         VL    v21,0(R1)
000027CA  E310 5024 0014                00000024   1946+         LGF   R1,V2ADDR         load v2 source
000027D0  E761 0000 0806                00000000   1947+         VL    v22,0(R1)         use v21 to test decoder
000027D6  E756 0010 2C5C                           1948+         VISTR V21,V22,2,1               test instruction
000027DC  B98D 0020                                1949+         EPSW  R2,R0             extract psw
000027E0  5020 500C                     0000000C   1950+         ST    R2,CCPSW             to save CC
000027E4  E750 5040 080E                000027A8   1951+         VST   V21,V1O35         save v1 output
000027EA  07FB                                     1952+         BR    R11               return
000027EC                                           1953+RE35     DC    0F                V1 for this test
000027EC                                           1954+         DROP  R5
000027EC  AAAAAAAA BBBBBBBB                        1955          DC    XL16'AAAAAAAA BBBBBBBB CCCCCCCC DDDDDDDD'   v1
000027F4  CCCCCCCC DDDDDDDD
000027FC  AAAAAAAA BBBBBBBB                        1956          DC    XL16'AAAAAAAA BBBBBBBB CCCCCCCC DDDDDDDD'   v2
00002804  CCCCCCCC DDDDDDDD
                                                   1957
                                                   1958          VRR_A VISTR,2,1,0
00002810                                           1959+         DS    0FD
00002810                     00002810              1960+         USING *,R5              base for test data and test routine
00002810  00002868                                 1961+T36      DC    A(X36)            address of test routine
00002814  0024                                     1962+         DC    H'36'             test number
00002816  00                                       1963+         DC    X'00'
00002817  02                                       1964+         DC    HL1'2'                 M3 used
00002818  01                                       1965+         DC    HL1'1'                 M5 used
00002819  00                                       1966+         DC    HL1'0'            CC
0000281A  07                                       1967+         DC    HL1'7'            CC failed mask
0000281C  00000000 00000000                        1968+         DS    2F                extracted PSW after test (has CC)
00002824  FF                                       1969+         DC    X'FF'             extracted CC, if test failed
00002825  E5C9E2E3 D9404040                        1970+         DC    CL8'VISTR'        instruction name
00002830  00002894                                 1971+         DC    A(RE36)           address of v1 result
00002834  000028A4                                 1972+         DC    A(RE36+16)        address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002838  000028B4                          1973+          DC    A(RE36+32)          address of v3 source
0000283C  00000010                          1974+          DC    A(16)               result length
00002840  00002894                          1975+REA36     DC    A(RE36)             result address
00002848  00000000 00000000                 1976+          DS    FD                  gap
00002850  00000000 00000000                 1977+V1O36     DS    XL16                V1 output
00002858  00000000 00000000
00002860  00000000 00000000                 1978+          DS    FD                  gap
                                            1979+*
00002868                                    1980+X36       DS    0F
00002868  4110 8EF8                 000010F8 1981+          LA    R1,V1FUDGE        load v21 fudge
0000286C  E751 0000 0806            00000000 1982+          VL    v21,0(R1)
00002872  E310 5024 0014            00000024 1983+          LGF   R1,V2ADDR          load v2 source
00002878  E761 0000 0806            00000000 1984+          VL    v22,0(R1)          use v21 to test decoder
0000287E  E756 0010 2C5C                     1985+          VISTR V21,V22,2,1                test instruction
00002884  B98D 0020                          1986+          EPSW  R2,R0              extract psw
00002888  5020 500C                 0000000C 1987+          ST    R2,CCPSW              to save CC
0000288C  E750 5040 080E            00002850 1988+          VST   V21,V1O36          save v1 output
00002892  07FB                               1989+          BR    R11                return
00002894                                     1990+RE36      DC    0F                 V1 for this test
00002894                                     1991+          DROP  R5
00002894  AAAAAAAA BBBBBBBB                  1992           DC    XL16'AAAAAAAA BBBBBBBB CCCCCCCC 00000000'   v1
0000289C  CCCCCCCC 00000000
000028A4  AAAAAAAA BBBBBBBB                  1993           DC    XL16'AAAAAAAA BBBBBBBB CCCCCCCC 00000000'   v2
000028AC  CCCCCCCC 00000000
                                             1994
                                             1995            VRR_A VISTR,2,1,0
000028B8                                     1996+          DS    0FD
000028B8                    000028B8         1997+          USING *,R5               base for test data and test routine
000028B8  00002910                           1998+T37       DC    A(X37)             address of test routine
000028BC  0025                               1999+          DC    H'37'              test number
000028BE  00                                 2000+          DC    X'00'
000028BF  02                                 2001+          DC    HL1'2'                  M3 used
000028C0  01                                 2002+          DC    HL1'1'                  M5 used
000028C1  00                                 2003+          DC    HL1'0'             CC
000028C2  07                                 2004+          DC    HL1'7'             CC failed mask
000028C4  00000000 00000000                  2005+          DS    2F                 extracted PSW after test (has CC)
000028CC  FF                                 2006+          DC    X'FF'              extracted CC, if test failed
000028CD  E5C9E2E3 D9404040                  2007+          DC    CL8'VISTR'         instruction name
000028D8  0000293C                           2008+          DC    A(RE37)            address of v1 result
000028DC  0000294C                           2009+          DC    A(RE37+16)         address of v2 source
000028E0  0000295C                           2010+          DC    A(RE37+32)         address of v3 source
000028E4  00000010                           2011+          DC    A(16)              result length
000028E8  0000293C                           2012+REA37     DC    A(RE37)            result address
000028F0  00000000 00000000                  2013+          DS    FD                 gap
000028F8  00000000 00000000                  2014+V1O37     DS    XL16               V1 output
00002900  00000000 00000000
00002908  00000000 00000000                  2015+          DS    FD                 gap
                                             2016+*
00002910                                     2017+X37       DS    0F
00002910  4110 8EF8                 000010F8 2018+          LA    R1,V1FUDGE        load v21 fudge
00002914  E751 0000 0806            00000000 2019+          VL    v21,0(R1)
0000291A  E310 5024 0014            00000024 2020+          LGF   R1,V2ADDR          load v2 source
00002920  E761 0000 0806            00000000 2021+          VL    v22,0(R1)          use v21 to test decoder
00002926  E756 0010 2C5C                     2022+          VISTR V21,V22,2,1                test instruction
0000292C  B98D 0020                          2023+          EPSW  R2,R0              extract psw
00002930  5020 500C                 0000000C 2024+          ST    R2,CCPSW              to save CC
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002934  E750 5040 080E                 000028F8  2025+         VST   V21,V1O37          save v1 output
0000293A  07FB                                     2026+         BR    R11               return
0000293C                                           2027+RE37     DC    0F                V1 for this test
0000293C                                           2028+         DROP  R5
0000293C  AAAAAAAA BBBBBBBB                        2029          DC    XL16'AAAAAAAA BBBBBBBB 00000000 00000000'   v1
00002944  00000000 00000000
0000294C  AAAAAAAA BBBBBBBB                        2030          DC    XL16'AAAAAAAA BBBBBBBB 00000000 DDDDDDDD'   v2
00002954  00000000 DDDDDDDD
                                                   2031
                                                   2032          VRR_A VISTR,2,1,0
00002960                                           2033+         DS    0FD
00002960                    00002960               2034+         USING *,R5              base for test data and test routine
00002960  000029B8                                 2035+T38      DC    A(X38)            address of test routine
00002964  0026                                     2036+         DC    H'38'             test number
00002966  00                                       2037+         DC    X'00'
00002967  02                                       2038+         DC    HL1'2'                 M3 used
00002968  01                                       2039+         DC    HL1'1'                 M5 used
00002969  00                                       2040+         DC    HL1'0'            CC
0000296A  07                                       2041+         DC    HL1'7'            CC failed mask
0000296C  00000000 00000000                        2042+         DS    2F                extracted PSW after test (has CC)
00002974  FF                                       2043+         DC    X'FF'             extracted CC, if test failed
00002975  E5C9E2E3 D9404040                        2044+         DC    CL8'VISTR'        instruction name
00002980  000029E4                                 2045+         DC    A(RE38)           address of v1 result
00002984  000029F4                                 2046+         DC    A(RE38+16)        address of v2 source
00002988  00002A04                                 2047+         DC    A(RE38+32)        address of v3 source
0000298C  00000010                                 2048+         DC    A(16)             result length
00002990  000029E4                                 2049+REA38    DC    A(RE38)           result address
00002998  00000000 00000000                        2050+         DS    FD                gap
000029A0  00000000 00000000                        2051+V1O38    DS    XL16              V1 output
000029A8  00000000 00000000
000029B0  00000000 00000000                        2052+         DS    FD                gap
                                                   2053+*
000029B8                                           2054+X38      DS    0F
000029B8  4110 8EF8                      000010F8  2055+         LA    R1,V1FUDGE       load v21 fudge
000029BC  E751 0000 0806                 00000000  2056+         VL    v21,0(R1)
000029C2  E310 5024 0014                 00000024  2057+         LGF   R1,V2ADDR         load v2 source
000029C8  E761 0000 0806                 00000000  2058+         VL    v22,0(R1)         use v21 to test decoder
000029CE  E756 0010 2C5C                           2059+         VISTR V21,V22,2,1               test instruction
000029D4  B98D 0020                                2060+         EPSW  R2,R0             extract psw
000029D8  5020 500C                      0000000C  2061+         ST    R2,CCPSW             to save CC
000029DC  E750 5040 080E                 000029A0  2062+         VST   V21,V1O38         save v1 output
000029E2  07FB                                     2063+         BR    R11               return
000029E4                                           2064+RE38     DC    0F                V1 for this test
000029E4                                           2065+         DROP  R5
000029E4  AAAAAAAA 00000000                        2066          DC    XL16'AAAAAAAA 00000000 00000000 00000000'   v1
000029EC  00000000 00000000
000029F4  AAAAAAAA 00000000                        2067          DC    XL16'AAAAAAAA 00000000 CCCCCCCC DDDDDDDD'   v2
000029FC  CCCCCCCC DDDDDDDD
                                                   2068
                                                   2069          VRR_A VISTR,2,1,0
00002A08                                           2070+         DS    0FD
00002A08                    00002A08               2071+         USING *,R5              base for test data and test routine
00002A08  00002A60                                 2072+T39      DC    A(X39)            address of test routine
00002A0C  0027                                     2073+         DC    H'39'             test number
00002A0E  00                                       2074+         DC    X'00'
00002A0F  02                                       2075+         DC    HL1'2'                 M3 used
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002A10  01                                       2076+          DC    HL1'1'                 M5 used
00002A11  00                                       2077+          DC    HL1'0'              CC
00002A12  07                                       2078+          DC    HL1'7'              CC failed mask
00002A14  00000000 00000000                        2079+          DS    2F                  extracted PSW after test (has CC)
00002A1C  FF                                       2080+          DC    X'FF'               extracted CC, if test failed
00002A1D  E5C9E2E3 D9404040                        2081+          DC    CL8'VISTR'          instruction name
00002A28  00002A8C                                 2082+          DC    A(RE39)             address of v1 result
00002A2C  00002A9C                                 2083+          DC    A(RE39+16)          address of v2 source
00002A30  00002AAC                                 2084+          DC    A(RE39+32)          address of v3 source
00002A34  00000010                                 2085+          DC    A(16)               result length
00002A38  00002A8C                                 2086+REA39     DC    A(RE39)             result address
00002A40  00000000 00000000                        2087+          DS    FD                  gap
00002A48  00000000 00000000                        2088+V1O39     DS    XL16                V1 output
00002A50  00000000 00000000
00002A58  00000000 00000000                        2089+          DS    FD                  gap
                                                   2090+*
00002A60                                           2091+X39       DS    0F
00002A60  4110 8EF8                      000010F8  2092+          LA    R1,V1FUDGE        load v21 fudge
00002A64  E751 0000 0806                 00000000  2093+          VL    v21,0(R1)
00002A6A  E310 5024 0014                 00000024  2094+          LGF   R1,V2ADDR          load v2 source
00002A70  E761 0000 0806                 00000000  2095+          VL    v22,0(R1)           use v21 to test decoder
00002A76  E756 0010 2C5C                           2096+          VISTR V21,V22,2,1                 test instruction
00002A7C  B98D 0020                                2097+          EPSW  R2,R0               extract psw
00002A80  5020 500C                      0000000C  2098+          ST    R2,CCPSW               to save CC
00002A84  E750 5040 080E                 00002A48  2099+          VST   V21,V1O39           save v1 output
00002A8A  07FB                                     2100+          BR    R11                 return
00002A8C                                           2101+RE39      DC    0F                       V1 for this test
00002A8C                                           2102+          DROP  R5
00002A8C  00000000 00000000                        2103           DC    XL16'00000000 00000000 00000000 00000000'   v1
00002A94  00000000 00000000
00002A9C  00000000 BBBBBBBB                        2104           DC    XL16'00000000 BBBBBBBB CCCCCCCC DDDDDDDD'   v2
00002AA4  CCCCCCCC DDDDDDDD
                                                   2105
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2107 *-------------------------------------------------------------------
                                                   2108 * case 2 -  two zeros                                        CS=1
                                                   2109 *-------------------------------------------------------------------
                                                   2110 *byte
                                                   2111          VRR_A VISTR,0,1,0
00002AB0                                           2112+         DS    0FD
00002AB0                      00002AB0             2113+         USING *,R5              base for test data and test routine
00002AB0  00002B08                                 2114+T40      DC    A(X40)            address of test routine
00002AB4  0028                                     2115+         DC    H'40'             test number
00002AB6  00                                       2116+         DC    X'00'
00002AB7  00                                       2117+         DC    HL1'0'                 M3 used
00002AB8  01                                       2118+         DC    HL1'1'                 M5 used
00002AB9  00                                       2119+         DC    HL1'0'            CC
00002ABA  07                                       2120+         DC    HL1'7'            CC failed mask
00002ABC  00000000 00000000                        2121+         DS    2F                extracted PSW after test (has CC)
00002AC4  FF                                       2122+         DC    X'FF'             extracted CC, if test failed
00002AC5  E5C9E2E3 D9404040                        2123+         DC    CL8'VISTR'        instruction name
00002AD0  00002B34                                 2124+         DC    A(RE40)           address of v1 result
00002AD4  00002B44                                 2125+         DC    A(RE40+16)        address of v2 source
00002AD8  00002B54                                 2126+         DC    A(RE40+32)        address of v3 source
00002ADC  00000010                                 2127+         DC    A(16)             result length
00002AE0  00002B34                                 2128+REA40    DC    A(RE40)           result address
00002AE8  00000000 00000000                        2129+         DS    FD                gap
00002AF0  00000000 00000000                        2130+V1O40    DS    XL16              V1 output
00002AF8  00000000 00000000
00002B00  00000000 00000000                        2131+         DS    FD                gap
                                                   2132+*
00002B08                                           2133+X40      DS    0F
00002B08  4110 8EF8                       000010F8 2134+         LA    R1,V1FUDGE      load v21 fudge
00002B0C  E751 0000 0806                  00000000 2135+         VL    v21,0(R1)
00002B12  E310 5024 0014                  00000024 2136+         LGF   R1,V2ADDR        load v2 source
00002B18  E761 0000 0806                  00000000 2137+         VL    v22,0(R1)        use v21 to test decoder
00002B1E  E756 0010 0C5C                           2138+         VISTR V21,V22,0,1              test instruction
00002B24  B98D 0020                                2139+         EPSW  R2,R0            extract psw
00002B28  5020 500C                       0000000C 2140+         ST    R2,CCPSW            to save CC
00002B2C  E750 5040 080E                  00002AF0 2141+         VST   V21,V1O40          save v1 output
00002B32  07FB                                     2142+         BR    R11              return
00002B34                                           2143+RE40     DC    0F               V1 for this test
00002B34                                           2144+         DROP  R5
00002B34  01020304 05060708                        2145          DC    XL16'01020304 05060708 090A0B0C 00000000'   v1
00002B3C  090A0B0C 00000000
00002B44  01020304 05060708                        2146          DC    XL16'01020304 05060708 090A0B0C 000E0F00'   v2
00002B4C  090A0B0C 000E0F00
                                                   2147
                                                   2148          VRR_A VISTR,0,1,0
00002B58                                           2149+         DS    0FD
00002B58                      00002B58             2150+         USING *,R5              base for test data and test routine
00002B58  00002BB0                                 2151+T41      DC    A(X41)            address of test routine
00002B5C  0029                                     2152+         DC    H'41'             test number
00002B5E  00                                       2153+         DC    X'00'
00002B5F  00                                       2154+         DC    HL1'0'                 M3 used
00002B60  01                                       2155+         DC    HL1'1'                 M5 used
00002B61  00                                       2156+         DC    HL1'0'            CC
00002B62  07                                       2157+         DC    HL1'7'            CC failed mask
00002B64  00000000 00000000                        2158+         DS    2F                extracted PSW after test (has CC)
00002B6C  FF                                       2159+         DC    X'FF'             extracted CC, if test failed
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002B6D  E5C9E2E3 D9404040                        2160+          DC    CL8'VISTR'          instruction name
00002B78  00002BDC                                 2161+          DC    A(RE41)             address of v1 result
00002B7C  00002BEC                                 2162+          DC    A(RE41+16)          address of v2 source
00002B80  00002BFC                                 2163+          DC    A(RE41+32)          address of v3 source
00002B84  00000010                                 2164+          DC    A(16)               result length
00002B88  00002BDC                                 2165+REA41     DC    A(RE41)             result address
00002B90  00000000 00000000                        2166+          DS    FD                  gap
00002B98  00000000 00000000                        2167+V1O41     DS    XL16                V1 output
00002BA0  00000000 00000000
00002BA8  00000000 00000000                        2168+          DS    FD                  gap
                                                   2169+*
00002BB0                                           2170+X41       DS    0F
00002BB0  4110 8EF8                       000010F8 2171+          LA    R1,V1FUDGE         load v21 fudge
00002BB4  E751 0000 0806                  00000000 2172+          VL    v21,0(R1)
00002BBA  E310 5024 0014                  00000024 2173+          LGF   R1,V2ADDR           load v2 source
00002BC0  E761 0000 0806                  00000000 2174+          VL    v22,0(R1)           use v21 to test decoder
00002BC6  E756 0010 0C5C                           2175+          VISTR V21,V22,0,1                 test instruction
00002BCC  B98D 0020                                2176+          EPSW  R2,R0               extract psw
00002BD0  5020 500C                       0000000C 2177+          ST    R2,CCPSW               to save CC
00002BD4  E750 5040 080E                  00002B98 2178+          VST   V21,V1O41           save v1 output
00002BDA  07FB                                     2179+          BR    R11                 return
00002BDC                                           2180+RE41      DC    0F                  V1 for this test
00002BDC                                           2181+          DROP  R5
00002BDC  01020304 05060708                        2182           DC    XL16'01020304 05060708 090A0B00 00000000'   v1
00002BE4  090A0B00 00000000
00002BEC  01020304 05060708                        2183           DC    XL16'01020304 05060708 090A0B00 0D000F10'   v2
00002BF4  090A0B00 0D000F10
                                                   2184
                                                   2185           VRR_A VISTR,0,1,0
00002C00                                           2186+          DS    0FD
00002C00                  00002C00                 2187+          USING *,R5                base for test data and test routine
00002C00  00002C58                                 2188+T42       DC    A(X42)              address of test routine
00002C04  002A                                     2189+          DC    H'42'               test number
00002C06  00                                       2190+          DC    X'00'
00002C07  00                                       2191+          DC    HL1'0'                    M3 used
00002C08  01                                       2192+          DC    HL1'1'                    M5 used
00002C09  00                                       2193+          DC    HL1'0'              CC
00002C0A  07                                       2194+          DC    HL1'7'              CC failed mask
00002C0C  00000000 00000000                        2195+          DS    2F                  extracted PSW after test (has CC)
00002C14  FF                                       2196+          DC    X'FF'               extracted CC, if test failed
00002C15  E5C9E2E3 D9404040                        2197+          DC    CL8'VISTR'          instruction name
00002C20  00002C84                                 2198+          DC    A(RE42)             address of v1 result
00002C24  00002C94                                 2199+          DC    A(RE42+16)          address of v2 source
00002C28  00002CA4                                 2200+          DC    A(RE42+32)          address of v3 source
00002C2C  00000010                                 2201+          DC    A(16)               result length
00002C30  00002C84                                 2202+REA42     DC    A(RE42)             result address
00002C38  00000000 00000000                        2203+          DS    FD                  gap
00002C40  00000000 00000000                        2204+V1O42     DS    XL16                V1 output
00002C48  00000000 00000000
00002C50  00000000 00000000                        2205+          DS    FD                  gap
                                                   2206+*
00002C58                                           2207+X42       DS    0F
00002C58  4110 8EF8                       000010F8 2208+          LA    R1,V1FUDGE         load v21 fudge
00002C5C  E751 0000 0806                  00000000 2209+          VL    v21,0(R1)
00002C62  E310 5024 0014                  00000024 2210+          LGF   R1,V2ADDR           load v2 source
00002C68  E761 0000 0806                  00000000 2211+          VL    v22,0(R1)           use v21 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002C6E  E756 0010 0C5C                          2212+         VISTR V21,V22,0,1               test instruction
00002C74  B98D 0020                               2213+         EPSW  R2,R0               extract psw
00002C78  5020 500C                 0000000C      2214+         ST    R2,CCPSW               to save CC
00002C7C  E750 5040 080E            00002C40      2215+         VST   V21,V1O42           save v1 output
00002C82  07FB                                    2216+         BR    R11                 return
00002C84                                          2217+RE42     DC    0F                  V1 for this test
00002C84                                          2218+         DROP  R5
00002C84  01020304 05060708                       2219          DC    XL16'01020304 05060708 090A0000 00000000'   v1
00002C8C  090A0000 00000000
00002C94  01020304 05060708                       2220          DC    XL16'01020304 05060708 090A000C 000E0F10'   v2
00002C9C  090A000C 000E0F10
                                                  2221
                                                  2222          VRR_A VISTR,0,1,0
00002CA8                                          2223+         DS    0FD
00002CA8                    00002CA8              2224+         USING *,R5                base for test data and test routine
00002CA8  00002D00                                2225+T43      DC    A(X43)              address of test routine
00002CAC  002B                                    2226+         DC    H'43'               test number
00002CAE  00                                      2227+         DC    X'00'
00002CAF  00                                      2228+         DC    HL1'0'                   M3 used
00002CB0  01                                      2229+         DC    HL1'1'                   M5 used
00002CB1  00                                      2230+         DC    HL1'0'              CC
00002CB2  07                                      2231+         DC    HL1'7'              CC failed mask
00002CB4  00000000 00000000                       2232+         DS    2F                  extracted PSW after test (has CC)
00002CBC  FF                                      2233+         DC    X'FF'               extracted CC, if test failed
00002CBD  E5C9E2E3 D9404040                       2234+         DC    CL8'VISTR'          instruction name
00002CC8  00002D2C                                2235+         DC    A(RE43)             address of v1 result
00002CCC  00002D3C                                2236+         DC    A(RE43+16)          address of v2 source
00002CD0  00002D4C                                2237+         DC    A(RE43+32)          address of v3 source
00002CD4  00000010                                2238+         DC    A(16)               result length
00002CD8  00002D2C                                2239+REA43    DC    A(RE43)             result address
00002CE0  00000000 00000000                       2240+         DS    FD                  gap
00002CE8  00000000 00000000                       2241+V1O43    DS    XL16                V1 output
00002CF0  00000000 00000000
00002CF8  00000000 00000000                       2242+         DS    FD                  gap
                                                  2243+*
00002D00                                          2244+X43      DS    0F
00002D00  4110 8EF8                 000010F8      2245+         LA    R1,V1FUDGE         load v21 fudge
00002D04  E751 0000 0806            00000000      2246+         VL    v21,0(R1)
00002D0A  E310 5024 0014            00000024      2247+         LGF   R1,V2ADDR           load v2 source
00002D10  E761 0000 0806            00000000      2248+         VL    v22,0(R1)           use v21 to test decoder
00002D16  E756 0010 0C5C                          2249+         VISTR V21,V22,0,1               test instruction
00002D1C  B98D 0020                               2250+         EPSW  R2,R0               extract psw
00002D20  5020 500C                 0000000C      2251+         ST    R2,CCPSW               to save CC
00002D24  E750 5040 080E            00002CE8      2252+         VST   V21,V1O43           save v1 output
00002D2A  07FB                                    2253+         BR    R11                 return
00002D2C                                          2254+RE43     DC    0F                  V1 for this test
00002D2C                                          2255+         DROP  R5
00002D2C  01020304 05060708                       2256          DC    XL16'01020304 05060708 00000000 00000000'   v1
00002D34  00000000 00000000
00002D3C  01020304 05060708                       2257          DC    XL16'01020304 05060708 00A0B000 0D0E0F10'   v2
00002D44  00A0B000 0D0E0F10
                                                  2258
                                                  2259          VRR_A VISTR,0,1,0
00002D50                                          2260+         DS    0FD
00002D50                    00002D50              2261+         USING *,R5                base for test data and test routine
00002D50  00002DA8                                2262+T44      DC    A(X44)              address of test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002D54  002C                                    2263+          DC    H'44'               test number
00002D56  00                                      2264+          DC    X'00'
00002D57  00                                      2265+          DC    HL1'0'                   M3 used
00002D58  01                                      2266+          DC    HL1'1'                   M5 used
00002D59  00                                      2267+          DC    HL1'0'              CC
00002D5A  07                                      2268+          DC    HL1'7'              CC failed mask
00002D5C  00000000 00000000                       2269+          DS    2F                  extracted PSW after test (has CC)
00002D64  FF                                      2270+          DC    X'FF'               extracted CC, if test failed
00002D65  E5C9E2E3 D9404040                       2271+          DC    CL8'VISTR'          instruction name
00002D70  00002DD4                                2272+          DC    A(RE44)             address of v1 result
00002D74  00002DE4                                2273+          DC    A(RE44+16)          address of v2 source
00002D78  00002DF4                                2274+          DC    A(RE44+32)          address of v3 source
00002D7C  00000010                                2275+          DC    A(16)               result length
00002D80  00002DD4                                2276+REA44     DC    A(RE44)             result address
00002D88  00000000 00000000                       2277+          DS    FD                  gap
00002D90  00000000 00000000                       2278+V1O44     DS    XL16                V1 output
00002D98  00000000 00000000
00002DA0  00000000 00000000                       2279+          DS    FD                  gap
                                                  2280+*
00002DA8                                          2281+X44       DS    0F
00002DA8  4110 8EF8                    000010F8   2282+          LA    R1,V1FUDGE        load v21 fudge
00002DAC  E751 0000 0806               00000000   2283+          VL    v21,0(R1)
00002DB2  E310 5024 0014               00000024   2284+          LGF   R1,V2ADDR          load v2 source
00002DB8  E761 0000 0806               00000000   2285+          VL    v22,0(R1)           use v21 to test decoder
00002DBE  E756 0010 0C5C                          2286+          VISTR V21,V22,0,1                 test instruction
00002DC4  B98D 0020                               2287+          EPSW  R2,R0               extract psw
00002DC8  5020 500C                    0000000C   2288+          ST    R2,CCPSW                  to save CC
00002DCC  E750 5040 080E               00002D90   2289+          VST   V21,V1O44          save v1 output
00002DD2  07FB                                    2290+          BR    R11                 return
00002DD4                                          2291+RE44      DC    0F                  V1 for this test
00002DD4                                          2292+          DROP  R5
00002DD4  01020304 05060708                       2293           DC    XL16'01020304 05060708 00000000 00000000'   v1
00002DDC  00000000 00000000
00002DE4  01020304 05060708                       2294           DC    XL16'01020304 05060708 000A000C 0D0E0F10'   v2
00002DEC  000A000C 0D0E0F10
                                                  2295
                                                  2296           VRR_A VISTR,0,1,0
00002DF8                                          2297+          DS    0FD
00002DF8                       00002DF8           2298+          USING *,R5                base for test data and test routine
00002DF8  00002E50                                2299+T45       DC    A(X45)              address of test routine
00002DFC  002D                                    2300+          DC    H'45'               test number
00002DFE  00                                      2301+          DC    X'00'
00002DFF  00                                      2302+          DC    HL1'0'                   M3 used
00002E00  01                                      2303+          DC    HL1'1'                   M5 used
00002E01  00                                      2304+          DC    HL1'0'              CC
00002E02  07                                      2305+          DC    HL1'7'              CC failed mask
00002E04  00000000 00000000                       2306+          DS    2F                  extracted PSW after test (has CC)
00002E0C  FF                                      2307+          DC    X'FF'               extracted CC, if test failed
00002E0D  E5C9E2E3 D9404040                       2308+          DC    CL8'VISTR'          instruction name
00002E18  00002E7C                                2309+          DC    A(RE45)             address of v1 result
00002E1C  00002E8C                                2310+          DC    A(RE45+16)          address of v2 source
00002E20  00002E9C                                2311+          DC    A(RE45+32)          address of v3 source
00002E24  00000010                                2312+          DC    A(16)               result length
00002E28  00002E7C                                2313+REA45     DC    A(RE45)             result address
00002E30  00000000 00000000                       2314+          DS    FD                  gap
00002E38  00000000 00000000                       2315+V1O45     DS    XL16                V1 output
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00002E40  00000000 00000000
00002E48  00000000 00000000                         2316+         DS    FD                  gap
                                                    2317+*
00002E50                                            2318+X45      DS    0F
00002E50  4110 8EF8                       000010F8  2319+         LA    R1,V1FUDGE         load v21 fudge
00002E54  E751 0000 0806                  00000000  2320+         VL    v21,0(R1)
00002E5A  E310 5024 0014                  00000024  2321+         LGF   R1,V2ADDR           load v2 source
00002E60  E761 0000 0806                  00000000  2322+         VL    v22,0(R1)           use v21 to test decoder
00002E66  E756 0010 0C5C                            2323+         VISTR V21,V22,0,1                test instruction
00002E6C  B98D 0020                                 2324+         EPSW  R2,R0               extract psw
00002E70  5020 500C                       0000000C  2325+         ST    R2,CCPSW               to save CC
00002E74  E750 5040 080E                  00002E38  2326+         VST   V21,V1O45           save v1 output
00002E7A  07FB                                      2327+         BR    R11                 return
00002E7C                                            2328+RE45     DC    0F                  V1 for this test
00002E7C                                            2329+         DROP  R5
00002E7C  01020304 05060708                         2330          DC    XL16'01020304 05060708 09000000 00000000'   v1
00002E84  09000000 00000000
00002E8C  01020304 05060708                         2331          DC    XL16'01020304 05060708 09000B0C 0D0E0F10'   v2
00002E94  09000B0C 0D0E0F10
                                                    2332
                                                    2333          VRR_A VISTR,0,1,0
00002EA0                                            2334+         DS    0FD
00002EA0                  00002EA0                  2335+         USING *,R5                base for test data and test routine
00002EA0  00002EF8                                  2336+T46      DC    A(X46)              address of test routine
00002EA4  002E                                      2337+         DC    H'46'               test number
00002EA6  00                                        2338+         DC    X'00'
00002EA7  00                                        2339+         DC    HL1'0'                   M3 used
00002EA8  01                                        2340+         DC    HL1'1'                   M5 used
00002EA9  00                                        2341+         DC    HL1'0'              CC
00002EAA  07                                        2342+         DC    HL1'7'              CC failed mask
00002EAC  00000000 00000000                         2343+         DS    2F                  extracted PSW after test (has CC)
00002EB4  FF                                        2344+         DC    X'FF'               extracted CC, if test failed
00002EB5  E5C9E2E3 D9404040                         2345+         DC    CL8'VISTR'          instruction name
00002EC0  00002F24                                  2346+         DC    A(RE46)             address of v1 result
00002EC4  00002F34                                  2347+         DC    A(RE46+16)          address of v2 source
00002EC8  00002F44                                  2348+         DC    A(RE46+32)          address of v3 source
00002ECC  00000010                                  2349+         DC    A(16)               result length
00002ED0  00002F24                                  2350+REA46    DC    A(RE46)             result address
00002ED8  00000000 00000000                         2351+         DS    FD                  gap
00002EE0  00000000 00000000                         2352+V1O46    DS    XL16                V1 output
00002EE8  00000000 00000000
00002EF0  00000000 00000000                         2353+         DS    FD                  gap
                                                    2354+*
00002EF8                                            2355+X46      DS    0F
00002EF8  4110 8EF8                       000010F8  2356+         LA    R1,V1FUDGE         load v21 fudge
00002EFC  E751 0000 0806                  00000000  2357+         VL    v21,0(R1)
00002F02  E310 5024 0014                  00000024  2358+         LGF   R1,V2ADDR           load v2 source
00002F08  E761 0000 0806                  00000000  2359+         VL    v22,0(R1)           use v21 to test decoder
00002F0E  E756 0010 0C5C                            2360+         VISTR V21,V22,0,1                test instruction
00002F14  B98D 0020                                 2361+         EPSW  R2,R0               extract psw
00002F18  5020 500C                       0000000C  2362+         ST    R2,CCPSW               to save CC
00002F1C  E750 5040 080E                  00002EE0  2363+         VST   V21,V1O46           save v1 output
00002F22  07FB                                      2364+         BR    R11                 return
00002F24                                            2365+RE46     DC    0F                  V1 for this test
00002F24                                            2366+         DROP  R5
00002F24  01020304 00000000                         2367          DC    XL16'01020304 00000000 00000000 00000000'   v1
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002F2C  00000000 00000000
00002F34  01020304 00060708                        2368          DC    XL16'01020304 00060708 000A0B0C 0D0E0F10'   v2
00002F3C  000A0B0C 0D0E0F10
                                                   2369
                                                   2370          VRR_A VISTR,0,1,0
00002F48                                           2371+         DS    0FD
00002F48                     00002F48              2372+         USING *,R5               base for test data and test routine
00002F48  00002FA0                                 2373+T47      DC    A(X47)             address of test routine
00002F4C  002F                                     2374+         DC    H'47'              test number
00002F4E  00                                       2375+         DC    X'00'
00002F4F  00                                       2376+         DC    HL1'0'                  M3 used
00002F50  01                                       2377+         DC    HL1'1'                  M5 used
00002F51  00                                       2378+         DC    HL1'0'             CC
00002F52  07                                       2379+         DC    HL1'7'             CC failed mask
00002F54  00000000 00000000                        2380+         DS    2F                 extracted PSW after test (has CC)
00002F5C  FF                                       2381+         DC    X'FF'              extracted CC, if test failed
00002F5D  E5C9E2E3 D9404040                        2382+         DC    CL8'VISTR'         instruction name
00002F68  00002FCC                                 2383+         DC    A(RE47)            address of v1 result
00002F6C  00002FDC                                 2384+         DC    A(RE47+16)         address of v2 source
00002F70  00002FEC                                 2385+         DC    A(RE47+32)         address of v3 source
00002F74  00000010                                 2386+         DC    A(16)              result length
00002F78  00002FCC                                 2387+REA47    DC    A(RE47)            result address
00002F80  00000000 00000000                        2388+         DS    FD                 gap
00002F88  00000000 00000000                        2389+V1O47    DS    XL16               V1 output
00002F90  00000000 00000000
00002F98  00000000 00000000                        2390+         DS    FD                 gap
                                                   2391+*
00002FA0                                           2392+X47      DS    0F
00002FA0  4110 8EF8                       000010F8 2393+         LA    R1,V1FUDGE       load v21 fudge
00002FA4  E751 0000 0806                  00000000 2394+         VL    v21,0(R1)
00002FAA  E310 5024 0014                  00000024 2395+         LGF   R1,V2ADDR          load v2 source
00002FB0  E761 0000 0806                  00000000 2396+         VL    v22,0(R1)          use v21 to test decoder
00002FB6  E756 0010 0C5C                           2397+         VISTR V21,V22,0,1                test instruction
00002FBC  B98D 0020                                2398+         EPSW  R2,R0              extract psw
00002FC0  5020 500C                       0000000C 2399+         ST    R2,CCPSW              to save CC
00002FC4  E750 5040 080E                  00002F88 2400+         VST   V21,V1O47          save v1 output
00002FCA  07FB                                     2401+         BR    R11                return
00002FCC                                           2402+RE47     DC    0F                 V1 for this test
00002FCC                                           2403+         DROP  R5
00002FCC  01020304 00000000                        2404          DC    XL16'01020304 00000000 00000000 00000000'   v1
00002FD4  00000000 00000000
00002FDC  01020304 00060700                        2405          DC    XL16'01020304 00060700 090A0B0C 0D0E0F10'   v2
00002FE4  090A0B0C 0D0E0F10
                                                   2406
                                                   2407          VRR_A VISTR,0,1,0
00002FF0                                           2408+         DS    0FD
00002FF0                     00002FF0              2409+         USING *,R5               base for test data and test routine
00002FF0  00003048                                 2410+T48      DC    A(X48)             address of test routine
00002FF4  0030                                     2411+         DC    H'48'              test number
00002FF6  00                                       2412+         DC    X'00'
00002FF7  00                                       2413+         DC    HL1'0'                  M3 used
00002FF8  01                                       2414+         DC    HL1'1'                  M5 used
00002FF9  00                                       2415+         DC    HL1'0'             CC
00002FFA  07                                       2416+         DC    HL1'7'             CC failed mask
00002FFC  00000000 00000000                        2417+         DS    2F                 extracted PSW after test (has CC)
00003004  FF                                       2418+         DC    X'FF'              extracted CC, if test failed
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003005  E5C9E2E3 D9404040                        2419+         DC    CL8'VISTR'          instruction name
00003010  00003074                                 2420+         DC    A(RE48)             address of v1 result
00003014  00003084                                 2421+         DC    A(RE48+16)          address of v2 source
00003018  00003094                                 2422+         DC    A(RE48+32)          address of v3 source
0000301C  00000010                                 2423+         DC    A(16)               result length
00003020  00003074                                 2424+REA48    DC    A(RE48)             result address
00003028  00000000 00000000                        2425+         DS    FD                  gap
00003030  00000000 00000000                        2426+V1O48    DS    XL16                V1 output
00003038  00000000 00000000
00003040  00000000 00000000                        2427+         DS    FD                  gap
                                                   2428+*
00003048                                           2429+X48      DS    0F
00003048  4110 8EF8                      000010F8  2430+         LA    R1,V1FUDGE         load v21 fudge
0000304C  E751 0000 0806                 00000000  2431+         VL    v21,0(R1)
00003052  E310 5024 0014                 00000024  2432+         LGF   R1,V2ADDR           load v2 source
00003058  E761 0000 0806                 00000000  2433+         VL    v22,0(R1)           use v21 to test decoder
0000305E  E756 0010 0C5C                           2434+         VISTR V21,V22,0,1                 test instruction
00003064  B98D 0020                                2435+         EPSW  R2,R0               extract psw
00003068  5020 500C                      0000000C  2436+         ST    R2,CCPSW               to save CC
0000306C  E750 5040 080E                 00003030  2437+         VST   V21,V1O48           save v1 output
00003072  07FB                                     2438+         BR    R11                 return
00003074                                           2439+RE48     DC    0F                  V1 for this test
00003074                                           2440+         DROP  R5
00003074  01020304 00000000                        2441          DC    XL16'01020304 00000000 00000000 00000000'   v1
0000307C  00000000 00000000
00003084  01020304 00060008                        2442          DC    XL16'01020304 00060008 090A0B0C 0D0E0F10'   v2
0000308C  090A0B0C 0D0E0F10
                                                   2443
                                                   2444          VRR_A VISTR,0,1,0
00003098                                           2445+         DS    0FD
00003098                       00003098            2446+         USING *,R5                base for test data and test routine
00003098  000030F0                                 2447+T49      DC    A(X49)              address of test routine
0000309C  0031                                     2448+         DC    H'49'               test number
0000309E  00                                       2449+         DC    X'00'
0000309F  00                                       2450+         DC    HL1'0'                   M3 used
000030A0  01                                       2451+         DC    HL1'1'                   M5 used
000030A1  00                                       2452+         DC    HL1'0'              CC
000030A2  07                                       2453+         DC    HL1'7'              CC failed mask
000030A4  00000000 00000000                        2454+         DS    2F                  extracted PSW after test (has CC)
000030AC  FF                                       2455+         DC    X'FF'               extracted CC, if test failed
000030AD  E5C9E2E3 D9404040                        2456+         DC    CL8'VISTR'          instruction name
000030B8  0000311C                                 2457+         DC    A(RE49)             address of v1 result
000030BC  0000312C                                 2458+         DC    A(RE49+16)          address of v2 source
000030C0  0000313C                                 2459+         DC    A(RE49+32)          address of v3 source
000030C4  00000010                                 2460+         DC    A(16)               result length
000030C8  0000311C                                 2461+REA49    DC    A(RE49)             result address
000030D0  00000000 00000000                        2462+         DS    FD                  gap
000030D8  00000000 00000000                        2463+V1O49    DS    XL16                V1 output
000030E0  00000000 00000000
000030E8  00000000 00000000                        2464+         DS    FD                  gap
                                                   2465+*
000030F0                                           2466+X49      DS    0F
000030F0  4110 8EF8                      000010F8  2467+         LA    R1,V1FUDGE         load v21 fudge
000030F4  E751 0000 0806                 00000000  2468+         VL    v21,0(R1)
000030FA  E310 5024 0014                 00000024  2469+         LGF   R1,V2ADDR           load v2 source
00003100  E761 0000 0806                 00000000  2470+         VL    v22,0(R1)           use v21 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003106  E756 0010 0C5C                          2471+         VISTR V21,V22,0,1               test instruction
0000310C  B98D 0020                               2472+         EPSW  R2,R0               extract psw
00003110  5020 500C                     0000000C  2473+         ST    R2,CCPSW               to save CC
00003114  E750 5040 080E                000030D8  2474+         VST   V21,V1O49           save v1 output
0000311A  07FB                                    2475+         BR    R11                 return
0000311C                                          2476+RE49     DC    0F                  V1 for this test
0000311C                                          2477+         DROP  R5
0000311C  01020304 00000000                       2478          DC    XL16'01020304 00000000 00000000 00000000'   v1
00003124  00000000 00000000
0000312C  01020304 00000708                       2479          DC    XL16'01020304 00000708 090A0B0C 0D0E0F10'   v2
00003134  090A0B0C 0D0E0F10
                                                  2480
                                                  2481          VRR_A VISTR,0,1,0
00003140                                          2482+         DS    0FD
00003140                        00003140          2483+         USING *,R5                base for test data and test routine
00003140  00003198                                2484+T50      DC    A(X50)              address of test routine
00003144  0032                                    2485+         DC    H'50'               test number
00003146  00                                      2486+         DC    X'00'
00003147  00                                      2487+         DC    HL1'0'                   M3 used
00003148  01                                      2488+         DC    HL1'1'                   M5 used
00003149  00                                      2489+         DC    HL1'0'              CC
0000314A  07                                      2490+         DC    HL1'7'              CC failed mask
0000314C  00000000 00000000                       2491+         DS    2F                  extracted PSW after test (has CC)
00003154  FF                                      2492+         DC    X'FF'               extracted CC, if test failed
00003155  E5C9E2E3 D9404040                       2493+         DC    CL8'VISTR'          instruction name
00003160  000031C4                                2494+         DC    A(RE50)             address of v1 result
00003164  000031D4                                2495+         DC    A(RE50+16)          address of v2 source
00003168  000031E4                                2496+         DC    A(RE50+32)          address of v3 source
0000316C  00000010                                2497+         DC    A(16)               result length
00003170  000031C4                                2498+REA50    DC    A(RE50)             result address
00003178  00000000 00000000                       2499+         DS    FD                  gap
00003180  00000000 00000000                       2500+V1O50    DS    XL16                V1 output
00003188  00000000 00000000
00003190  00000000 00000000                       2501+         DS    FD                  gap
                                                  2502+*
00003198                                          2503+X50      DS    0F
00003198  4110 8EF8                     000010F8  2504+         LA    R1,V1FUDGE         load v21 fudge
0000319C  E751 0000 0806                00000000  2505+         VL    v21,0(R1)
000031A2  E310 5024 0014                00000024  2506+         LGF   R1,V2ADDR           load v2 source
000031A8  E761 0000 0806                00000000  2507+         VL    v22,0(R1)           use v21 to test decoder
000031AE  E756 0010 0C5C                          2508+         VISTR V21,V22,0,1               test instruction
000031B4  B98D 0020                               2509+         EPSW  R2,R0               extract psw
000031B8  5020 500C                     0000000C  2510+         ST    R2,CCPSW               to save CC
000031BC  E750 5040 080E                00003180  2511+         VST   V21,V1O50           save v1 output
000031C2  07FB                                    2512+         BR    R11                 return
000031C4                                          2513+RE50     DC    0F                  V1 for this test
000031C4                                          2514+         DROP  R5
000031C4  01000000 00000000                       2515          DC    XL16'01000000 00000000 00000000 00000000'   v1
000031CC  00000000 00000000
000031D4  01000304 00060708                       2516          DC    XL16'01000304 00060708 090A0B0C 0D0E0F10'   v2
000031DC  090A0B0C 0D0E0F10
                                                  2517
                                                  2518          VRR_A VISTR,0,1,0
000031E8                                          2519+         DS    0FD
000031E8                        000031E8          2520+         USING *,R5                base for test data and test routine
000031E8  00003240                                2521+T51      DC    A(X51)              address of test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000031EC  0033                                    2522+          DC    H'51'               test number
000031EE  00                                      2523+          DC    X'00'
000031EF  00                                      2524+          DC    HL1'0'                   M3 used
000031F0  01                                      2525+          DC    HL1'1'                   M5 used
000031F1  00                                      2526+          DC    HL1'0'              CC
000031F2  07                                      2527+          DC    HL1'7'              CC failed mask
000031F4  00000000 00000000                       2528+          DS    2F                  extracted PSW after test (has CC)
000031FC  FF                                      2529+          DC    X'FF'               extracted CC, if test failed
000031FD  E5C9E2E3 D9404040                       2530+          DC    CL8'VISTR'          instruction name
00003208  0000326C                                2531+          DC    A(RE51)             address of v1 result
0000320C  0000327C                                2532+          DC    A(RE51+16)          address of v2 source
00003210  0000328C                                2533+          DC    A(RE51+32)          address of v3 source
00003214  00000010                                2534+          DC    A(16)               result length
00003218  0000326C                                2535+REA51     DC    A(RE51)             result address
00003220  00000000 00000000                       2536+          DS    FD                  gap
00003228  00000000 00000000                       2537+V1O51     DS    XL16                V1 output
00003230  00000000 00000000
00003238  00000000 00000000                       2538+          DS    FD                  gap
                                                  2539+*
00003240                                          2540+X51       DS    0F
00003240  4110 8EF8                  000010F8     2541+          LA    R1,V1FUDGE        load v21 fudge
00003244  E751 0000 0806             00000000     2542+          VL    v21,0(R1)
0000324A  E310 5024 0014             00000024     2543+          LGF   R1,V2ADDR          load v2 source
00003250  E761 0000 0806             00000000     2544+          VL    v22,0(R1)          use v21 to test decoder
00003256  E756 0010 0C5C                          2545+          VISTR V21,V22,0,1                test instruction
0000325C  B98D 0020                               2546+          EPSW  R2,R0              extract psw
00003260  5020 500C                  0000000C     2547+          ST    R2,CCPSW                to save CC
00003264  E750 5040 080E             00003228     2548+          VST   V21,V1O51          save v1 output
0000326A  07FB                                    2549+          BR    R11                return
0000326C                                          2550+RE51      DC    0F                 V1 for this test
0000326C                                          2551+          DROP  R5
0000326C  01000000 00000000                       2552           DC    XL16'01000000 00000000 00000000 00000000'   v1
00003274  00000000 00000000
0000327C  01000300 05060708                       2553           DC    XL16'01000300 05060708 090A0B0C 0D0E0F10'   v2
00003284  090A0B0C 0D0E0F10
                                                  2554
                                                  2555           VRR_A VISTR,0,1,0
00003290                                          2556+          DS    0FD
00003290                       00003290           2557+          USING *,R5               base for test data and test routine
00003290  000032E8                                2558+T52       DC    A(X52)             address of test routine
00003294  0034                                    2559+          DC    H'52'              test number
00003296  00                                      2560+          DC    X'00'
00003297  00                                      2561+          DC    HL1'0'                   M3 used
00003298  01                                      2562+          DC    HL1'1'                   M5 used
00003299  00                                      2563+          DC    HL1'0'             CC
0000329A  07                                      2564+          DC    HL1'7'             CC failed mask
0000329C  00000000 00000000                       2565+          DS    2F                 extracted PSW after test (has CC)
000032A4  FF                                      2566+          DC    X'FF'              extracted CC, if test failed
000032A5  E5C9E2E3 D9404040                       2567+          DC    CL8'VISTR'         instruction name
000032B0  00003314                                2568+          DC    A(RE52)            address of v1 result
000032B4  00003324                                2569+          DC    A(RE52+16)         address of v2 source
000032B8  00003334                                2570+          DC    A(RE52+32)         address of v3 source
000032BC  00000010                                2571+          DC    A(16)              result length
000032C0  00003314                                2572+REA52     DC    A(RE52)            result address
000032C8  00000000 00000000                       2573+          DS    FD                 gap
000032D0  00000000 00000000                       2574+V1O52     DS    XL16               V1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000032D8  00000000 00000000
000032E0  00000000 00000000                        2575+         DS    FD                  gap
                                                   2576+*
000032E8                                           2577+X52      DS    0F
000032E8  4110 8EF8                      000010F8  2578+         LA    R1,V1FUDGE         load v21 fudge
000032EC  E751 0000 0806                 00000000  2579+         VL    v21,0(R1)
000032F2  E310 5024 0014                 00000024  2580+         LGF   R1,V2ADDR           load v2 source
000032F8  E761 0000 0806                 00000000  2581+         VL    v22,0(R1)           use v21 to test decoder
000032FE  E756 0010 0C5C                           2582+         VISTR V21,V22,0,1                test instruction
00003304  B98D 0020                                2583+         EPSW  R2,R0               extract psw
00003308  5020 500C                      0000000C  2584+         ST    R2,CCPSW               to save CC
0000330C  E750 5040 080E                 000032D0  2585+         VST   V21,V1O52           save v1 output
00003312  07FB                                     2586+         BR    R11                 return
00003314                                           2587+RE52     DC    0F                  V1 for this test
00003314                                           2588+         DROP  R5
00003314  01000000 00000000                        2589          DC    XL16'01000000 00000000 00000000 00000000'   v1
0000331C  00000000 00000000
00003324  01000004 05060708                        2590          DC    XL16'01000004 05060708 090A0B0C 0D0E0F10'   v2
0000332C  090A0B0C 0D0E0F10
                                                   2591
                                                   2592          VRR_A VISTR,0,1,0
00003338                                           2593+         DS    0FD
00003338                         00003338          2594+         USING *,R5                base for test data and test routine
00003338  00003390                                 2595+T53      DC    A(X53)              address of test routine
0000333C  0035                                     2596+         DC    H'53'               test number
0000333E  00                                       2597+         DC    X'00'
0000333F  00                                       2598+         DC    HL1'0'                   M3 used
00003340  01                                       2599+         DC    HL1'1'                   M5 used
00003341  00                                       2600+         DC    HL1'0'              CC
00003342  07                                       2601+         DC    HL1'7'              CC failed mask
00003344  00000000 00000000                        2602+         DS    2F                  extracted PSW after test (has CC)
0000334C  FF                                       2603+         DC    X'FF'               extracted CC, if test failed
0000334D  E5C9E2E3 D9404040                        2604+         DC    CL8'VISTR'          instruction name
00003358  000033BC                                 2605+         DC    A(RE53)             address of v1 result
0000335C  000033CC                                 2606+         DC    A(RE53+16)          address of v2 source
00003360  000033DC                                 2607+         DC    A(RE53+32)          address of v3 source
00003364  00000010                                 2608+         DC    A(16)               result length
00003368  000033BC                                 2609+REA53    DC    A(RE53)             result address
00003370  00000000 00000000                        2610+         DS    FD                  gap
00003378  00000000 00000000                        2611+V1O53    DS    XL16                V1 output
00003380  00000000 00000000
00003388  00000000 00000000                        2612+         DS    FD                  gap
                                                   2613+*
00003390                                           2614+X53      DS    0F
00003390  4110 8EF8                      000010F8  2615+         LA    R1,V1FUDGE         load v21 fudge
00003394  E751 0000 0806                 00000000  2616+         VL    v21,0(R1)
0000339A  E310 5024 0014                 00000024  2617+         LGF   R1,V2ADDR           load v2 source
000033A0  E761 0000 0806                 00000000  2618+         VL    v22,0(R1)           use v21 to test decoder
000033A6  E756 0010 0C5C                           2619+         VISTR V21,V22,0,1                test instruction
000033AC  B98D 0020                                2620+         EPSW  R2,R0               extract psw
000033B0  5020 500C                      0000000C  2621+         ST    R2,CCPSW               to save CC
000033B4  E750 5040 080E                 00003378  2622+         VST   V21,V1O53           save v1 output
000033BA  07FB                                     2623+         BR    R11                 return
000033BC                                           2624+RE53     DC    0F                  V1 for this test
000033BC                                           2625+         DROP  R5
000033BC  00000000 00000000                        2626          DC    XL16'00000000 00000000 00000000 00000000'   v1
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000033C4  00000000 00000000
000033CC  00000304 05060708                         2627          DC    XL16'00000304 05060708 090A0B0C 0D0E0F10'   v2
000033D4  090A0B0C 0D0E0F10
                                                    2628
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   2630 *halfword
                                                   2631          VRR_A VISTR,1,1,0
000033E0                                           2632+         DS    0FD
000033E0                       000033E0            2633+         USING *,R5              base for test data and test routine
000033E0  00003438                                 2634+T54      DC    A(X54)            address of test routine
000033E4  0036                                     2635+         DC    H'54'             test number
000033E6  00                                       2636+         DC    X'00'
000033E7  01                                       2637+         DC    HL1'1'                 M3 used
000033E8  01                                       2638+         DC    HL1'1'                 M5 used
000033E9  00                                       2639+         DC    HL1'0'            CC
000033EA  07                                       2640+         DC    HL1'7'            CC failed mask
000033EC  00000000 00000000                        2641+         DS    2F                extracted PSW after test (has CC)
000033F4  FF                                       2642+         DC    X'FF'             extracted CC, if test failed
000033F5  E5C9E2E3 D9404040                        2643+         DC    CL8'VISTR'        instruction name
00003400  00003464                                 2644+         DC    A(RE54)           address of v1 result
00003404  00003474                                 2645+         DC    A(RE54+16)        address of v2 source
00003408  00003484                                 2646+         DC    A(RE54+32)        address of v3 source
0000340C  00000010                                 2647+         DC    A(16)             result length
00003410  00003464                                 2648+REA54    DC    A(RE54)           result address
00003418  00000000 00000000                        2649+         DS    FD                gap
00003420  00000000 00000000                        2650+V1O54    DS    XL16              V1 output
00003428  00000000 00000000
00003430  00000000 00000000                        2651+         DS    FD                gap
                                                   2652+*
00003438                                           2653+X54      DS    0F
00003438  4110 8EF8                    000010F8    2654+         LA    R1,V1FUDGE        load v21 fudge
0000343C  E751 0000 0806               00000000    2655+         VL    v21,0(R1)
00003442  E310 5024 0014               00000024    2656+         LGF   R1,V2ADDR         load v2 source
00003448  E761 0000 0806               00000000    2657+         VL    v22,0(R1)         use v21 to test decoder
0000344E  E756 0010 1C5C                           2658+         VISTR V21,V22,1,1               test instruction
00003454  B98D 0020                                2659+         EPSW  R2,R0             extract psw
00003458  5020 500C                    0000000C    2660+         ST    R2,CCPSW             to save CC
0000345C  E750 5040 080E               00003420    2661+         VST   V21,V1O54         save v1 output
00003462  07FB                                     2662+         BR    R11               return
00003464                                           2663+RE54     DC    0F                V1 for this test
00003464                                           2664+         DROP  R5
00003464  88888888 77777777                        2665          DC    XL16'88888888 77777777 00000000 00000000'   v1
0000346C  00000000 00000000
00003474  88888888 77777777                        2666          DC    XL16'88888888 77777777 00006666 55550000'   v2
0000347C  00006666 55550000
                                                   2667
                                                   2668          VRR_A VISTR,1,1,0
00003488                                           2669+         DS    0FD
00003488                       00003488            2670+         USING *,R5              base for test data and test routine
00003488  000034E0                                 2671+T55      DC    A(X55)            address of test routine
0000348C  0037                                     2672+         DC    H'55'             test number
0000348E  00                                       2673+         DC    X'00'
0000348F  01                                       2674+         DC    HL1'1'                 M3 used
00003490  01                                       2675+         DC    HL1'1'                 M5 used
00003491  00                                       2676+         DC    HL1'0'            CC
00003492  07                                       2677+         DC    HL1'7'            CC failed mask
00003494  00000000 00000000                        2678+         DS    2F                extracted PSW after test (has CC)
0000349C  FF                                       2679+         DC    X'FF'             extracted CC, if test failed
0000349D  E5C9E2E3 D9404040                        2680+         DC    CL8'VISTR'        instruction name
000034A8  0000350C                                 2681+         DC    A(RE55)           address of v1 result
000034AC  0000351C                                 2682+         DC    A(RE55+16)        address of v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000034B0  0000352C                                2683+          DC    A(RE55+32)          address of v3 source
000034B4  00000010                                2684+          DC    A(16)               result length
000034B8  0000350C                                2685+REA55     DC    A(RE55)             result address
000034C0  00000000 00000000                       2686+          DS    FD                  gap
000034C8  00000000 00000000                       2687+V1O55     DS    XL16                V1 output
000034D0  00000000 00000000
000034D8  00000000 00000000                       2688+          DS    FD                  gap
                                                  2689+*
000034E0                                          2690+X55       DS    0F
000034E0  4110 8EF8                     000010F8  2691+          LA    R1,V1FUDGE        load v21 fudge
000034E4  E751 0000 0806                00000000  2692+          VL    v21,0(R1)
000034EA  E310 5024 0014                00000024  2693+          LGF   R1,V2ADDR          load v2 source
000034F0  E761 0000 0806                00000000  2694+          VL    v22,0(R1)           use v21 to test decoder
000034F6  E756 0010 1C5C                          2695+          VISTR V21,V22,1,1                test instruction
000034FC  B98D 0020                               2696+          EPSW  R2,R0               extract psw
00003500  5020 500C                     0000000C  2697+          ST    R2,CCPSW               to save CC
00003504  E750 5040 080E                000034C8  2698+          VST   V21,V1O55           save v1 output
0000350A  07FB                                    2699+          BR    R11                 return
0000350C                                          2700+RE55      DC    0F                  V1 for this test
0000350C                                          2701+          DROP  R5
0000350C  88888888 77777777                       2702           DC    XL16'88888888 77777777 00000000 00000000'   v1
00003514  00000000 00000000
0000351C  88888888 77777777                       2703           DC    XL16'88888888 77777777 00006666 00005555'   v2
00003524  00006666 00005555
                                                  2704
                                                  2705           VRR_A VISTR,1,1,0
00003530                                          2706+          DS    0FD
00003530                        00003530          2707+          USING *,R5                base for test data and test routine
00003530  00003588                                2708+T56       DC    A(X56)              address of test routine
00003534  0038                                    2709+          DC    H'56'               test number
00003536  00                                      2710+          DC    X'00'
00003537  01                                      2711+          DC    HL1'1'                   M3 used
00003538  01                                      2712+          DC    HL1'1'                   M5 used
00003539  00                                      2713+          DC    HL1'0'              CC
0000353A  07                                      2714+          DC    HL1'7'              CC failed mask
0000353C  00000000 00000000                       2715+          DS    2F                  extracted PSW after test (has CC)
00003544  FF                                      2716+          DC    X'FF'               extracted CC, if test failed
00003545  E5C9E2E3 D9404040                       2717+          DC    CL8'VISTR'          instruction name
00003550  000035B4                                2718+          DC    A(RE56)             address of v1 result
00003554  000035C4                                2719+          DC    A(RE56+16)          address of v2 source
00003558  000035D4                                2720+          DC    A(RE56+32)          address of v3 source
0000355C  00000010                                2721+          DC    A(16)               result length
00003560  000035B4                                2722+REA56     DC    A(RE56)             result address
00003568  00000000 00000000                       2723+          DS    FD                  gap
00003570  00000000 00000000                       2724+V1O56     DS    XL16                V1 output
00003578  00000000 00000000
00003580  00000000 00000000                       2725+          DS    FD                  gap
                                                  2726+*
00003588                                          2727+X56       DS    0F
00003588  4110 8EF8                     000010F8  2728+          LA    R1,V1FUDGE        load v21 fudge
0000358C  E751 0000 0806                00000000  2729+          VL    v21,0(R1)
00003592  E310 5024 0014                00000024  2730+          LGF   R1,V2ADDR          load v2 source
00003598  E761 0000 0806                00000000  2731+          VL    v22,0(R1)           use v21 to test decoder
0000359E  E756 0010 1C5C                          2732+          VISTR V21,V22,1,1                test instruction
000035A4  B98D 0020                               2733+          EPSW  R2,R0               extract psw
000035A8  5020 500C                     0000000C  2734+          ST    R2,CCPSW               to save CC
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000035AC  E750 5040 080E                 00003570  2735+          VST   V21,V1O56          save v1 output
000035B2  07FB                                     2736+          BR    R11               return
000035B4                                           2737+RE56      DC    0F                V1 for this test
000035B4                                           2738+          DROP  R5
000035B4  88888888 77777777                        2739           DC    XL16'88888888 77777777 00000000 00000000'   v1
000035BC  00000000 00000000
000035C4  88888888 77777777                        2740           DC    XL16'88888888 77777777 00000000 55555555'   v2
000035CC  00000000 55555555
                                                   2741
                                                   2742           VRR_A VISTR,1,1,0
000035D8                                           2743+          DS    0FD
000035D8                  000035D8                 2744+          USING *,R5              base for test data and test routine
000035D8  00003630                                 2745+T57       DC    A(X57)            address of test routine
000035DC  0039                                     2746+          DC    H'57'             test number
000035DE  00                                       2747+          DC    X'00'
000035DF  01                                       2748+          DC    HL1'1'                 M3 used
000035E0  01                                       2749+          DC    HL1'1'                 M5 used
000035E1  00                                       2750+          DC    HL1'0'            CC
000035E2  07                                       2751+          DC    HL1'7'            CC failed mask
000035E4  00000000 00000000                        2752+          DS    2F                extracted PSW after test (has CC)
000035EC  FF                                       2753+          DC    X'FF'             extracted CC, if test failed
000035ED  E5C9E2E3 D9404040                        2754+          DC    CL8'VISTR'        instruction name
000035F8  0000365C                                 2755+          DC    A(RE57)           address of v1 result
000035FC  0000366C                                 2756+          DC    A(RE57+16)        address of v2 source
00003600  0000367C                                 2757+          DC    A(RE57+32)        address of v3 source
00003604  00000010                                 2758+          DC    A(16)             result length
00003608  0000365C                                 2759+REA57     DC    A(RE57)           result address
00003610  00000000 00000000                        2760+          DS    FD                gap
00003618  00000000 00000000                        2761+V1O57     DS    XL16              V1 output
00003620  00000000 00000000
00003628  00000000 00000000                        2762+          DS    FD                gap
                                                   2763+*
00003630                                           2764+X57       DS    0F
00003630  4110 8EF8                      000010F8  2765+          LA    R1,V1FUDGE       load v21 fudge
00003634  E751 0000 0806                 00000000  2766+          VL    v21,0(R1)
0000363A  E310 5024 0014                 00000024  2767+          LGF   R1,V2ADDR          load v2 source
00003640  E761 0000 0806                 00000000  2768+          VL    v22,0(R1)         use v21 to test decoder
00003646  E756 0010 1C5C                           2769+          VISTR V21,V22,1,1               test instruction
0000364C  B98D 0020                                2770+          EPSW  R2,R0             extract psw
00003650  5020 500C                      0000000C  2771+          ST    R2,CCPSW             to save CC
00003654  E750 5040 080E                 00003618  2772+          VST   V21,V1O57         save v1 output
0000365A  07FB                                     2773+          BR    R11               return
0000365C                                           2774+RE57      DC    0F                V1 for this test
0000365C                                           2775+          DROP  R5
0000365C  88888888 00000000                        2776           DC    XL16'88888888 00000000 00000000 00000000'   v1
00003664  00000000 00000000
0000366C  88888888 00007777                        2777           DC    XL16'88888888 00007777 00006666 55555555'   v2
00003674  00006666 55555555
                                                   2778
                                                   2779           VRR_A VISTR,1,1,0
00003680                                           2780+          DS    0FD
00003680                  00003680                 2781+          USING *,R5              base for test data and test routine
00003680  000036D8                                 2782+T58       DC    A(X58)            address of test routine
00003684  003A                                     2783+          DC    H'58'             test number
00003686  00                                       2784+          DC    X'00'
00003687  01                                       2785+          DC    HL1'1'                 M3 used
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003688  01                                      2786+          DC    HL1'1'                 M5 used
00003689  00                                      2787+          DC    HL1'0'              CC
0000368A  07                                      2788+          DC    HL1'7'              CC failed mask
0000368C  00000000 00000000                       2789+          DS    2F                  extracted PSW after test (has CC)
00003694  FF                                      2790+          DC    X'FF'               extracted CC, if test failed
00003695  E5C9E2E3 D9404040                       2791+          DC    CL8'VISTR'          instruction name
000036A0  00003704                                2792+          DC    A(RE58)             address of v1 result
000036A4  00003714                                2793+          DC    A(RE58+16)          address of v2 source
000036A8  00003724                                2794+          DC    A(RE58+32)          address of v3 source
000036AC  00000010                                2795+          DC    A(16)               result length
000036B0  00003704                                2796+REA58     DC    A(RE58)             result address
000036B8  00000000 00000000                       2797+          DS    FD                  gap
000036C0  00000000 00000000                       2798+V1O58     DS    XL16                V1 output
000036C8  00000000 00000000
000036D0  00000000 00000000                       2799+          DS    FD                  gap
                                                  2800+*
000036D8                                          2801+X58       DS    0F
000036D8  4110 8EF8                    000010F8   2802+          LA    R1,V1FUDGE        load v21 fudge
000036DC  E751 0000 0806               00000000   2803+          VL    v21,0(R1)
000036E2  E310 5024 0014               00000024   2804+          LGF   R1,V2ADDR          load v2 source
000036E8  E761 0000 0806               00000000   2805+          VL    v22,0(R1)           use v21 to test decoder
000036EE  E756 0010 1C5C                          2806+          VISTR V21,V22,1,1                 test instruction
000036F4  B98D 0020                               2807+          EPSW  R2,R0               extract psw
000036F8  5020 500C                    0000000C   2808+          ST    R2,CCPSW               to save CC
000036FC  E750 5040 080E               000036C0   2809+          VST   V21,V1O58           save v1 output
00003702  07FB                                    2810+          BR    R11                 return
00003704                                          2811+RE58      DC    0F                  V1 for this test
00003704                                          2812+          DROP  R5
00003704  88888888 00000000                       2813           DC    XL16'88888888 00000000 00000000 00000000'   v1
0000370C  00000000 00000000
00003714  88888888 00000000                       2814           DC    XL16'88888888 00000000 66666666 55555555'   v2
0000371C  66666666 55555555
                                                  2815
                                                  2816           VRR_A VISTR,1,1,0
00003728                                          2817+          DS    0FD
00003728                       00003728           2818+          USING *,R5                base for test data and test routine
00003728  00003780                                2819+T59       DC    A(X59)              address of test routine
0000372C  003B                                    2820+          DC    H'59'               test number
0000372E  00                                      2821+          DC    X'00'
0000372F  01                                      2822+          DC    HL1'1'                 M3 used
00003730  01                                      2823+          DC    HL1'1'                 M5 used
00003731  00                                      2824+          DC    HL1'0'              CC
00003732  07                                      2825+          DC    HL1'7'              CC failed mask
00003734  00000000 00000000                       2826+          DS    2F                  extracted PSW after test (has CC)
0000373C  FF                                      2827+          DC    X'FF'               extracted CC, if test failed
0000373D  E5C9E2E3 D9404040                       2828+          DC    CL8'VISTR'          instruction name
00003748  000037AC                                2829+          DC    A(RE59)             address of v1 result
0000374C  000037BC                                2830+          DC    A(RE59+16)          address of v2 source
00003750  000037CC                                2831+          DC    A(RE59+32)          address of v3 source
00003754  00000010                                2832+          DC    A(16)               result length
00003758  000037AC                                2833+REA59     DC    A(RE59)             result address
00003760  00000000 00000000                       2834+          DS    FD                  gap
00003768  00000000 00000000                       2835+V1O59     DS    XL16                V1 output
00003770  00000000 00000000
00003778  00000000 00000000                       2836+          DS    FD                  gap
                                                  2837+*
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003780                                           2838+X59      DS    0F
00003780  4110 8EF8                      000010F8  2839+          LA    R1,V1FUDGE         load v21 fudge
00003784  E751 0000 0806                 00000000  2840+          VL    v21,0(R1)
0000378A  E310 5024 0014                 00000024  2841+          LGF   R1,V2ADDR           load v2 source
00003790  E761 0000 0806                 00000000  2842+          VL    v22,0(R1)           use v21 to test decoder
00003796  E756 0010 1C5C                           2843+          VISTR V21,V22,1,1                test instruction
0000379C  B98D 0020                                2844+          EPSW  R2,R0               extract psw
000037A0  5020 500C                      0000000C  2845+          ST    R2,CCPSW               to save CC
000037A4  E750 5040 080E                 00003768  2846+          VST   V21,V1O59           save v1 output
000037AA  07FB                                     2847+          BR    R11                 return
000037AC                                           2848+RE59      DC    0F                  V1 for this test
000037AC                                           2849+          DROP  R5
000037AC  88880000 00000000                        2850           DC    XL16'88880000 00000000 00000000 00000000'   v1
000037B4  00000000 00000000
000037BC  88880000 00007777                        2851           DC    XL16'88880000 00007777 66666666 55555555'   v2
000037C4  66666666 55555555
                                                   2852
                                                   2853           VRR_A VISTR,1,1,0
000037D0                                           2854+          DS    0FD
000037D0                         000037D0          2855+          USING *,R5                base for test data and test routine
000037D0  00003828                                 2856+T60       DC    A(X60)              address of test routine
000037D4  003C                                     2857+          DC    H'60'               test number
000037D6  00                                       2858+          DC    X'00'
000037D7  01                                       2859+          DC    HL1'1'                   M3 used
000037D8  01                                       2860+          DC    HL1'1'                   M5 used
000037D9  00                                       2861+          DC    HL1'0'              CC
000037DA  07                                       2862+          DC    HL1'7'              CC failed mask
000037DC  00000000 00000000                        2863+          DS    2F                  extracted PSW after test (has CC)
000037E4  FF                                       2864+          DC    X'FF'               extracted CC, if test failed
000037E5  E5C9E2E3 D9404040                        2865+          DC    CL8'VISTR'          instruction name
000037F0  00003854                                 2866+          DC    A(RE60)             address of v1 result
000037F4  00003864                                 2867+          DC    A(RE60+16)          address of v2 source
000037F8  00003874                                 2868+          DC    A(RE60+32)          address of v3 source
000037FC  00000010                                 2869+          DC    A(16)               result length
00003800  00003854                                 2870+REA60     DC    A(RE60)             result address
00003808  00000000 00000000                        2871+          DS    FD                  gap
00003810  00000000 00000000                        2872+V1O60     DS    XL16                V1 output
00003818  00000000 00000000
00003820  00000000 00000000                        2873+          DS    FD                  gap
                                                   2874+*
00003828                                           2875+X60       DS    0F
00003828  4110 8EF8                      000010F8  2876+          LA    R1,V1FUDGE         load v21 fudge
0000382C  E751 0000 0806                 00000000  2877+          VL    v21,0(R1)
00003832  E310 5024 0014                 00000024  2878+          LGF   R1,V2ADDR           load v2 source
00003838  E761 0000 0806                 00000000  2879+          VL    v22,0(R1)           use v21 to test decoder
0000383E  E756 0010 1C5C                           2880+          VISTR V21,V22,1,1                test instruction
00003844  B98D 0020                                2881+          EPSW  R2,R0               extract psw
00003848  5020 500C                      0000000C  2882+          ST    R2,CCPSW               to save CC
0000384C  E750 5040 080E                 00003810  2883+          VST   V21,V1O60           save v1 output
00003852  07FB                                     2884+          BR    R11                 return
00003854                                           2885+RE60      DC    0F                  V1 for this test
00003854                                           2886+          DROP  R5
00003854  00000000 00000000                        2887           DC    XL16'00000000 00000000 00000000 00000000'   v1
0000385C  00000000 00000000
00003864  00000000 77777777                        2888           DC    XL16'00000000 77777777 66666666 55555555'   v2
0000386C  66666666 55555555
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2890 *word
                                                   2891          VRR_A VISTR,2,1,0
00003878                                           2892+         DS    0FD
00003878                       00003878            2893+         USING *,R5              base for test data and test routine
00003878  000038D0                                 2894+T61      DC    A(X61)            address of test routine
0000387C  003D                                     2895+         DC    H'61'             test number
0000387E  00                                       2896+         DC    X'00'
0000387F  02                                       2897+         DC    HL1'2'                 M3 used
00003880  01                                       2898+         DC    HL1'1'                 M5 used
00003881  00                                       2899+         DC    HL1'0'            CC
00003882  07                                       2900+         DC    HL1'7'            CC failed mask
00003884  00000000 00000000                        2901+         DS    2F                extracted PSW after test (has CC)
0000388C  FF                                       2902+         DC    X'FF'             extracted CC, if test failed
0000388D  E5C9E2E3 D9404040                        2903+         DC    CL8'VISTR'        instruction name
00003898  000038FC                                 2904+         DC    A(RE61)           address of v1 result
0000389C  0000390C                                 2905+         DC    A(RE61+16)        address of v2 source
000038A0  0000391C                                 2906+         DC    A(RE61+32)        address of v3 source
000038A4  00000010                                 2907+         DC    A(16)             result length
000038A8  000038FC                                 2908+REA61    DC    A(RE61)           result address
000038B0  00000000 00000000                        2909+         DS    FD                gap
000038B8  00000000 00000000                        2910+V1O61    DS    XL16              V1 output
000038C0  00000000 00000000
000038C8  00000000 00000000                        2911+         DS    FD                gap
                                                   2912+*
000038D0                                           2913+X61      DS    0F
000038D0  4110 8EF8                     000010F8   2914+         LA    R1,V1FUDGE        load v21 fudge
000038D4  E751 0000 0806                00000000   2915+         VL    v21,0(R1)
000038DA  E310 5024 0014                00000024   2916+         LGF   R1,V2ADDR         load v2 source
000038E0  E761 0000 0806                00000000   2917+         VL    v22,0(R1)         use v21 to test decoder
000038E6  E756 0010 2C5C                           2918+         VISTR V21,V22,2,1               test instruction
000038EC  B98D 0020                                2919+         EPSW  R2,R0             extract psw
000038F0  5020 500C                     0000000C   2920+         ST    R2,CCPSW             to save CC
000038F4  E750 5040 080E                000038B8   2921+         VST   V21,V1O61         save v1 output
000038FA  07FB                                     2922+         BR    R11               return
000038FC                                           2923+RE61     DC    0F                V1 for this test
000038FC                                           2924+         DROP  R5
000038FC  AAAAAAAA 00000000                        2925          DC    XL16'AAAAAAAA 00000000 00000000 00000000'   v1
00003904  00000000 00000000
0000390C  AAAAAAAA 00000000                        2926          DC    XL16'AAAAAAAA 00000000 CCCCCCCC 00000000'   v2
00003914  CCCCCCCC 00000000
                                                   2927
                                                   2928           VRR_A VISTR,2,1,0
00003920                                           2929+         DS    0FD
00003920                       00003920            2930+         USING *,R5              base for test data and test routine
00003920  00003978                                 2931+T62      DC    A(X62)            address of test routine
00003924  003E                                     2932+         DC    H'62'             test number
00003926  00                                       2933+         DC    X'00'
00003927  02                                       2934+         DC    HL1'2'                 M3 used
00003928  01                                       2935+         DC    HL1'1'                 M5 used
00003929  00                                       2936+         DC    HL1'0'            CC
0000392A  07                                       2937+         DC    HL1'7'            CC failed mask
0000392C  00000000 00000000                        2938+         DS    2F                extracted PSW after test (has CC)
00003934  FF                                       2939+         DC    X'FF'             extracted CC, if test failed
00003935  E5C9E2E3 D9404040                        2940+         DC    CL8'VISTR'        instruction name
00003940  000039A4                                 2941+         DC    A(RE62)           address of v1 result
00003944  000039B4                                 2942+         DC    A(RE62+16)        address of v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003948  000039C4                          2943+          DC    A(RE62+32)          address of v3 source
0000394C  00000010                          2944+          DC    A(16)               result length
00003950  000039A4                          2945+REA62     DC    A(RE62)             result address
00003958  00000000 00000000                 2946+          DS    FD                  gap
00003960  00000000 00000000                 2947+V1O62     DS    XL16                V1 output
00003968  00000000 00000000
00003970  00000000 00000000                 2948+          DS    FD                  gap
                                            2949+*
00003978                                    2950+X62       DS    0F
00003978  4110 8EF8                 000010F8 2951+          LA    R1,V1FUDGE        load v21 fudge
0000397C  E751 0000 0806            00000000 2952+          VL    v21,0(R1)
00003982  E310 5024 0014            00000024 2953+          LGF   R1,V2ADDR          load v2 source
00003988  E761 0000 0806            00000000 2954+          VL    v22,0(R1)          use v21 to test decoder
0000398E  E756 0010 2C5C                     2955+          VISTR V21,V22,2,1                test instruction
00003994  B98D 0020                          2956+          EPSW  R2,R0              extract psw
00003998  5020 500C                 0000000C 2957+          ST    R2,CCPSW              to save CC
0000399C  E750 5040 080E            00003960 2958+          VST   V21,V1O62          save v1 output
000039A2  07FB                               2959+          BR    R11                return
000039A4                                     2960+RE62      DC    0F                 V1 for this test
000039A4                                     2961+          DROP  R5
000039A4  AAAAAAAA 00000000                  2962           DC    XL16'AAAAAAAA 00000000 00000000 00000000'   v1
000039AC  00000000 00000000
000039B4  AAAAAAAA 00000000                  2963           DC    XL16'AAAAAAAA 00000000 00000000 DDDDDDDD'   v2
000039BC  00000000 DDDDDDDD
                                             2964
                                             2965           VRR_A VISTR,2,1,0
000039C8                                     2966+          DS    0FD
000039C8                    000039C8         2967+          USING *,R5               base for test data and test routine
000039C8  00003A20                           2968+T63       DC    A(X63)             address of test routine
000039CC  003F                               2969+          DC    H'63'              test number
000039CE  00                                 2970+          DC    X'00'
000039CF  02                                 2971+          DC    HL1'2'                  M3 used
000039D0  01                                 2972+          DC    HL1'1'                  M5 used
000039D1  00                                 2973+          DC    HL1'0'             CC
000039D2  07                                 2974+          DC    HL1'7'             CC failed mask
000039D4  00000000 00000000                  2975+          DS    2F                 extracted PSW after test (has CC)
000039DC  FF                                 2976+          DC    X'FF'              extracted CC, if test failed
000039DD  E5C9E2E3 D9404040                  2977+          DC    CL8'VISTR'         instruction name
000039E8  00003A4C                           2978+          DC    A(RE63)            address of v1 result
000039EC  00003A5C                           2979+          DC    A(RE63+16)         address of v2 source
000039F0  00003A6C                           2980+          DC    A(RE63+32)         address of v3 source
000039F4  00000010                           2981+          DC    A(16)              result length
000039F8  00003A4C                           2982+REA63     DC    A(RE63)            result address
00003A00  00000000 00000000                  2983+          DS    FD                 gap
00003A08  00000000 00000000                  2984+V1O63     DS    XL16               V1 output
00003A10  00000000 00000000
00003A18  00000000 00000000                  2985+          DS    FD                 gap
                                             2986+*
00003A20                                     2987+X63       DS    0F
00003A20  4110 8EF8                 000010F8 2988+          LA    R1,V1FUDGE        load v21 fudge
00003A24  E751 0000 0806            00000000 2989+          VL    v21,0(R1)
00003A2A  E310 5024 0014            00000024 2990+          LGF   R1,V2ADDR          load v2 source
00003A30  E761 0000 0806            00000000 2991+          VL    v22,0(R1)          use v21 to test decoder
00003A36  E756 0010 2C5C                     2992+          VISTR V21,V22,2,1                test instruction
00003A3C  B98D 0020                          2993+          EPSW  R2,R0              extract psw
00003A40  5020 500C                 0000000C 2994+          ST    R2,CCPSW              to save CC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003A44  E750 5040 080E                 00003A08  2995+          VST   V21,V1O63          save v1 output
00003A4A  07FB                                     2996+          BR    R11               return
00003A4C                                           2997+RE63      DC    0F                V1 for this test
00003A4C                                           2998+          DROP  R5
00003A4C  00000000 00000000                        2999           DC    XL16'00000000 00000000 00000000 00000000'   v1
00003A54  00000000 00000000
00003A5C  00000000 00000000                        3000           DC    XL16'00000000 00000000 CCCCCCCC DDDDDDDD'   v2
00003A64  CCCCCCCC DDDDDDDD
                                                   3001
                                                   3002           VRR_A VISTR,2,1,0
00003A70                                           3003+          DS    0FD
00003A70                  00003A70                 3004+          USING *,R5              base for test data and test routine
00003A70  00003AC8                                 3005+T64       DC    A(X64)            address of test routine
00003A74  0040                                     3006+          DC    H'64'             test number
00003A76  00                                       3007+          DC    X'00'
00003A77  02                                       3008+          DC    HL1'2'                 M3 used
00003A78  01                                       3009+          DC    HL1'1'                 M5 used
00003A79  00                                       3010+          DC    HL1'0'            CC
00003A7A  07                                       3011+          DC    HL1'7'            CC failed mask
00003A7C  00000000 00000000                        3012+          DS    2F                extracted PSW after test (has CC)
00003A84  FF                                       3013+          DC    X'FF'             extracted CC, if test failed
00003A85  E5C9E2E3 D9404040                        3014+          DC    CL8'VISTR'        instruction name
00003A90  00003AF4                                 3015+          DC    A(RE64)           address of v1 result
00003A94  00003B04                                 3016+          DC    A(RE64+16)        address of v2 source
00003A98  00003B14                                 3017+          DC    A(RE64+32)        address of v3 source
00003A9C  00000010                                 3018+          DC    A(16)             result length
00003AA0  00003AF4                                 3019+REA64     DC    A(RE64)           result address
00003AA8  00000000 00000000                        3020+          DS    FD                gap
00003AB0  00000000 00000000                        3021+V1O64     DS    XL16              V1 output
00003AB8  00000000 00000000
00003AC0  00000000 00000000                        3022+          DS    FD                gap
                                                   3023+*
00003AC8                                           3024+X64       DS    0F
00003AC8  4110 8EF8                      000010F8  3025+          LA    R1,V1FUDGE       load v21 fudge
00003ACC  E751 0000 0806                 00000000  3026+          VL    v21,0(R1)
00003AD2  E310 5024 0014                 00000024  3027+          LGF   R1,V2ADDR         load v2 source
00003AD8  E761 0000 0806                 00000000  3028+          VL    v22,0(R1)         use v21 to test decoder
00003ADE  E756 0010 2C5C                           3029+          VISTR V21,V22,2,1               test instruction
00003AE4  B98D 0020                                3030+          EPSW  R2,R0             extract psw
00003AE8  5020 500C                      0000000C  3031+          ST    R2,CCPSW             to save CC
00003AEC  E750 5040 080E                 00003AB0  3032+          VST   V21,V1O64         save v1 output
00003AF2  07FB                                     3033+          BR    R11               return
00003AF4                                           3034+RE64      DC    0F                V1 for this test
00003AF4                                           3035+          DROP  R5
00003AF4  00000000 00000000                        3036           DC    XL16'00000000 00000000 00000000 00000000'   v1
00003AFC  00000000 00000000
00003B04  00000000 BBBBBBBB                        3037           DC    XL16'00000000 BBBBBBBB CCCCCCCC DDDDDDDD'   v2
00003B0C  CCCCCCCC DDDDDDDD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    3039 *-------------------------------------------------------------------
                                                    3040 * case 3 -  same value before and after zeros         CS=1
                                                    3041 *-------------------------------------------------------------------
                                                    3042 *byte
                                                    3043          VRR_A VISTR,0,1,0
00003B18                                            3044+         DS    0FD
00003B18                      00003B18              3045+         USING *,R5              base for test data and test routine
00003B18  00003B70                                  3046+T65      DC    A(X65)            address of test routine
00003B1C  0041                                      3047+         DC    H'65'             test number
00003B1E  00                                        3048+         DC    X'00'
00003B1F  00                                        3049+         DC    HL1'0'                 M3 used
00003B20  01                                        3050+         DC    HL1'1'                 M5 used
00003B21  00                                        3051+         DC    HL1'0'            CC
00003B22  07                                        3052+         DC    HL1'7'            CC failed mask
00003B24  00000000 00000000                         3053+         DS    2F                extracted PSW after test (has CC)
00003B2C  FF                                        3054+         DC    X'FF'             extracted CC, if test failed
00003B2D  E5C9E2E3 D9404040                         3055+         DC    CL8'VISTR'        instruction name
00003B38  00003B9C                                  3056+         DC    A(RE65)           address of v1 result
00003B3C  00003BAC                                  3057+         DC    A(RE65+16)        address of v2 source
00003B40  00003BBC                                  3058+         DC    A(RE65+32)        address of v3 source
00003B44  00000010                                  3059+         DC    A(16)             result length
00003B48  00003B9C                                  3060+REA65    DC    A(RE65)           result address
00003B50  00000000 00000000                         3061+         DS    FD                gap
00003B58  00000000 00000000                         3062+V1O65    DS    XL16              V1 output
00003B60  00000000 00000000
00003B68  00000000 00000000                         3063+         DS    FD                gap
                                                    3064+*
00003B70                                            3065+X65      DS    0F
00003B70  4110 8EF8                       000010F8  3066+         LA    R1,V1FUDGE      load v21 fudge
00003B74  E751 0000 0806                  00000000  3067+         VL    v21,0(R1)
00003B7A  E310 5024 0014                  00000024  3068+         LGF   R1,V2ADDR        load v2 source
00003B80  E761 0000 0806                  00000000  3069+         VL    v22,0(R1)         use v21 to test decoder
00003B86  E756 0010 0C5C                            3070+         VISTR V21,V22,0,1               test instruction
00003B8C  B98D 0020                                 3071+         EPSW  R2,R0             extract psw
00003B90  5020 500C                       0000000C  3072+         ST    R2,CCPSW             to save CC
00003B94  E750 5040 080E                  00003B58  3073+         VST   V21,V1O65         save v1 output
00003B9A  07FB                                      3074+         BR    R11               return
00003B9C                                            3075+RE65     DC    0F                V1 for this test
00003B9C                                            3076+         DROP  R5
00003B9C  88888888 88888888                         3077          DC    XL16'88888888 88888888 88888888 00000000'   v1
00003BA4  88888888 00000000
00003BAC  88888888 88888888                         3078          DC    XL16'88888888 88888888 88888888 00888888'   v2
00003BB4  88888888 00888888
                                                    3079
                                                    3080          VRR_A VISTR,0,1,0
00003BC0                                            3081+         DS    0FD
00003BC0                      00003BC0              3082+         USING *,R5              base for test data and test routine
00003BC0  00003C18                                  3083+T66      DC    A(X66)            address of test routine
00003BC4  0042                                      3084+         DC    H'66'             test number
00003BC6  00                                        3085+         DC    X'00'
00003BC7  00                                        3086+         DC    HL1'0'                 M3 used
00003BC8  01                                        3087+         DC    HL1'1'                 M5 used
00003BC9  00                                        3088+         DC    HL1'0'            CC
00003BCA  07                                        3089+         DC    HL1'7'            CC failed mask
00003BCC  00000000 00000000                         3090+         DS    2F                extracted PSW after test (has CC)
00003BD4  FF                                        3091+         DC    X'FF'             extracted CC, if test failed
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003BD5  E5C9E2E3 D9404040                        3092+          DC    CL8'VISTR'          instruction name
00003BE0  00003C44                                 3093+          DC    A(RE66)             address of v1 result
00003BE4  00003C54                                 3094+          DC    A(RE66+16)          address of v2 source
00003BE8  00003C64                                 3095+          DC    A(RE66+32)          address of v3 source
00003BEC  00000010                                 3096+          DC    A(16)               result length
00003BF0  00003C44                                 3097+REA66     DC    A(RE66)             result address
00003BF8  00000000 00000000                        3098+          DS    FD                  gap
00003C00  00000000 00000000                        3099+V1O66     DS    XL16                V1 output
00003C08  00000000 00000000
00003C10  00000000 00000000                        3100+          DS    FD                  gap
                                                   3101+*
00003C18                                           3102+X66       DS    0F
00003C18  4110 8EF8                      000010F8  3103+          LA    R1,V1FUDGE         load v21 fudge
00003C1C  E751 0000 0806                 00000000  3104+          VL    v21,0(R1)
00003C22  E310 5024 0014                 00000024  3105+          LGF   R1,V2ADDR           load v2 source
00003C28  E761 0000 0806                 00000000  3106+          VL    v22,0(R1)           use v21 to test decoder
00003C2E  E756 0010 0C5C                           3107+          VISTR V21,V22,0,1                 test instruction
00003C34  B98D 0020                                3108+          EPSW  R2,R0               extract psw
00003C38  5020 500C                      0000000C  3109+          ST    R2,CCPSW               to save CC
00003C3C  E750 5040 080E                 00003C00  3110+          VST   V21,V1O66           save v1 output
00003C42  07FB                                     3111+          BR    R11                 return
00003C44                                           3112+RE66      DC    0F                  V1 for this test
00003C44                                           3113+          DROP  R5
00003C44  88888888 88888888                        3114           DC    XL16'88888888 88888888 88000000 00000000'   v1
00003C4C  88000000 00000000
00003C54  88888888 88888888                        3115           DC    XL16'88888888 88888888 88008880 88888888'   v2
00003C5C  88008880 88888888
                                                   3116
                                                   3117           VRR_A VISTR,0,1,0
00003C68                                           3118+          DS    0FD
00003C68                       00003C68            3119+          USING *,R5                base for test data and test routine
00003C68  00003CC0                                 3120+T67       DC    A(X67)              address of test routine
00003C6C  0043                                     3121+          DC    H'67'               test number
00003C6E  00                                       3122+          DC    X'00'
00003C6F  00                                       3123+          DC    HL1'0'                    M3 used
00003C70  01                                       3124+          DC    HL1'1'                    M5 used
00003C71  00                                       3125+          DC    HL1'0'              CC
00003C72  07                                       3126+          DC    HL1'7'              CC failed mask
00003C74  00000000 00000000                        3127+          DS    2F                  extracted PSW after test (has CC)
00003C7C  FF                                       3128+          DC    X'FF'               extracted CC, if test failed
00003C7D  E5C9E2E3 D9404040                        3129+          DC    CL8'VISTR'          instruction name
00003C88  00003CEC                                 3130+          DC    A(RE67)             address of v1 result
00003C8C  00003CFC                                 3131+          DC    A(RE67+16)          address of v2 source
00003C90  00003D0C                                 3132+          DC    A(RE67+32)          address of v3 source
00003C94  00000010                                 3133+          DC    A(16)               result length
00003C98  00003CEC                                 3134+REA67     DC    A(RE67)             result address
00003CA0  00000000 00000000                        3135+          DS    FD                  gap
00003CA8  00000000 00000000                        3136+V1O67     DS    XL16                V1 output
00003CB0  00000000 00000000
00003CB8  00000000 00000000                        3137+          DS    FD                  gap
                                                   3138+*
00003CC0                                           3139+X67       DS    0F
00003CC0  4110 8EF8                      000010F8  3140+          LA    R1,V1FUDGE         load v21 fudge
00003CC4  E751 0000 0806                 00000000  3141+          VL    v21,0(R1)
00003CCA  E310 5024 0014                 00000024  3142+          LGF   R1,V2ADDR           load v2 source
00003CD0  E761 0000 0806                 00000000  3143+          VL    v22,0(R1)           use v21 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003CD6  E756 0010 0C5C                           3144+         VISTR V21,V22,0,1               test instruction
00003CDC  B98D 0020                                3145+         EPSW  R2,R0               extract psw
00003CE0  5020 500C                     0000000C   3146+         ST    R2,CCPSW               to save CC
00003CE4  E750 5040 080E                00003CA8   3147+         VST   V21,V1O67           save v1 output
00003CEA  07FB                                     3148+         BR    R11                 return
00003CEC                                           3149+RE67     DC    0F                  V1 for this test
00003CEC                                           3150+         DROP  R5
00003CEC  88888800 00000000                        3151          DC    XL16'88888800 00000000 00000000 00000000'   v1
00003CF4  00000000 00000000
00003CFC  88888800 88888888                        3152          DC    XL16'88888800 88888888 88888888 88888888'   v2
00003D04  88888888 88888888
                                                   3153
                                                   3154          VRR_A VISTR,0,1,0
00003D10                                           3155+         DS    0FD
00003D10                        00003D10           3156+         USING *,R5                base for test data and test routine
00003D10  00003D68                                 3157+T68      DC    A(X68)              address of test routine
00003D14  0044                                     3158+         DC    H'68'               test number
00003D16  00                                       3159+         DC    X'00'
00003D17  00                                       3160+         DC    HL1'0'                   M3 used
00003D18  01                                       3161+         DC    HL1'1'                   M5 used
00003D19  00                                       3162+         DC    HL1'0'              CC
00003D1A  07                                       3163+         DC    HL1'7'              CC failed mask
00003D1C  00000000 00000000                        3164+         DS    2F                  extracted PSW after test (has CC)
00003D24  FF                                       3165+         DC    X'FF'               extracted CC, if test failed
00003D25  E5C9E2E3 D9404040                        3166+         DC    CL8'VISTR'          instruction name
00003D30  00003D94                                 3167+         DC    A(RE68)             address of v1 result
00003D34  00003DA4                                 3168+         DC    A(RE68+16)          address of v2 source
00003D38  00003DB4                                 3169+         DC    A(RE68+32)          address of v3 source
00003D3C  00000010                                 3170+         DC    A(16)               result length
00003D40  00003D94                                 3171+REA68    DC    A(RE68)             result address
00003D48  00000000 00000000                        3172+         DS    FD                  gap
00003D50  00000000 00000000                        3173+V1O68    DS    XL16                V1 output
00003D58  00000000 00000000
00003D60  00000000 00000000                        3174+         DS    FD                  gap
                                                   3175+*
00003D68                                           3176+X68      DS    0F
00003D68  4110 8EF8                     000010F8   3177+         LA    R1,V1FUDGE         load v21 fudge
00003D6C  E751 0000 0806                00000000   3178+         VL    v21,0(R1)
00003D72  E310 5024 0014                00000024   3179+         LGF   R1,V2ADDR           load v2 source
00003D78  E761 0000 0806                00000000   3180+         VL    v22,0(R1)           use v21 to test decoder
00003D7E  E756 0010 0C5C                           3181+         VISTR V21,V22,0,1               test instruction
00003D84  B98D 0020                                3182+         EPSW  R2,R0               extract psw
00003D88  5020 500C                     0000000C   3183+         ST    R2,CCPSW               to save CC
00003D8C  E750 5040 080E                00003D50   3184+         VST   V21,V1O68           save v1 output
00003D92  07FB                                     3185+         BR    R11                 return
00003D94                                           3186+RE68     DC    0F                  V1 for this test
00003D94                                           3187+         DROP  R5
00003D94  88888888 88888888                        3188          DC    XL16'88888888 88888888 88888888 00000000'   v1
00003D9C  88888888 00000000
00003DA4  88888888 88888888                        3189          DC    XL16'88888888 88888888 88888888 00880088'   v2
00003DAC  88888888 00880088
                                                   3190
                                                   3191          VRR_A VISTR,0,1,0
00003DB8                                           3192+         DS    0FD
00003DB8                        00003DB8           3193+         USING *,R5                base for test data and test routine
00003DB8  00003E10                                 3194+T69      DC    A(X69)              address of test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003DBC  0045                                    3195+          DC    H'69'               test number
00003DBE  00                                      3196+          DC    X'00'
00003DBF  00                                      3197+          DC    HL1'0'                   M3 used
00003DC0  01                                      3198+          DC    HL1'1'                   M5 used
00003DC1  00                                      3199+          DC    HL1'0'              CC
00003DC2  07                                      3200+          DC    HL1'7'              CC failed mask
00003DC4  00000000 00000000                       3201+          DS    2F                  extracted PSW after test (has CC)
00003DCC  FF                                      3202+          DC    X'FF'               extracted CC, if test failed
00003DCD  E5C9E2E3 D9404040                       3203+          DC    CL8'VISTR'          instruction name
00003DD8  00003E3C                                3204+          DC    A(RE69)             address of v1 result
00003DDC  00003E4C                                3205+          DC    A(RE69+16)          address of v2 source
00003DE0  00003E5C                                3206+          DC    A(RE69+32)          address of v3 source
00003DE4  00000010                                3207+          DC    A(16)               result length
00003DE8  00003E3C                                3208+REA69     DC    A(RE69)             result address
00003DF0  00000000 00000000                       3209+          DS    FD                  gap
00003DF8  00000000 00000000                       3210+V1O69     DS    XL16                V1 output
00003E00  00000000 00000000
00003E08  00000000 00000000                       3211+          DS    FD                  gap
                                                  3212+*
00003E10                                          3213+X69       DS    0F
00003E10  4110 8EF8                  000010F8     3214+          LA    R1,V1FUDGE        load v21 fudge
00003E14  E751 0000 0806             00000000     3215+          VL    v21,0(R1)
00003E1A  E310 5024 0014             00000024     3216+          LGF   R1,V2ADDR          load v2 source
00003E20  E761 0000 0806             00000000     3217+          VL    v22,0(R1)           use v21 to test decoder
00003E26  E756 0010 0C5C                          3218+          VISTR V21,V22,0,1                 test instruction
00003E2C  B98D 0020                               3219+          EPSW  R2,R0               extract psw
00003E30  5020 500C                  0000000C     3220+          ST    R2,CCPSW                 to save CC
00003E34  E750 5040 080E             00003DF8     3221+          VST   V21,V1O69           save v1 output
00003E3A  07FB                                    3222+          BR    R11                 return
00003E3C                                          3223+RE69      DC    0F                  V1 for this test
00003E3C                                          3224+          DROP  R5
00003E3C  88888888 88888888                       3225           DC    XL16'88888888 88888888 88000000 00000000'   v1
00003E44  88000000 00000000
00003E4C  88888888 88888888                       3226           DC    XL16'88888888 88888888 88008880 00888888'   v2
00003E54  88008880 00888888
                                                  3227
                                                  3228           VRR_A VISTR,0,1,0
00003E60                                          3229+          DS    0FD
00003E60                       00003E60           3230+          USING *,R5                base for test data and test routine
00003E60  00003EB8                                3231+T70       DC    A(X70)              address of test routine
00003E64  0046                                    3232+          DC    H'70'               test number
00003E66  00                                      3233+          DC    X'00'
00003E67  00                                      3234+          DC    HL1'0'                   M3 used
00003E68  01                                      3235+          DC    HL1'1'                   M5 used
00003E69  00                                      3236+          DC    HL1'0'              CC
00003E6A  07                                      3237+          DC    HL1'7'              CC failed mask
00003E6C  00000000 00000000                       3238+          DS    2F                  extracted PSW after test (has CC)
00003E74  FF                                      3239+          DC    X'FF'               extracted CC, if test failed
00003E75  E5C9E2E3 D9404040                       3240+          DC    CL8'VISTR'          instruction name
00003E80  00003EE4                                3241+          DC    A(RE70)             address of v1 result
00003E84  00003EF4                                3242+          DC    A(RE70+16)          address of v2 source
00003E88  00003F04                                3243+          DC    A(RE70+32)          address of v3 source
00003E8C  00000010                                3244+          DC    A(16)               result length
00003E90  00003EE4                                3245+REA70     DC    A(RE70)             result address
00003E98  00000000 00000000                       3246+          DS    FD                  gap
00003EA0  00000000 00000000                       3247+V1O70     DS    XL16                V1 output
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00003EA8  00000000 00000000
00003EB0  00000000 00000000                         3248+         DS    FD                  gap
                                                    3249+*
00003EB8                                            3250+X70      DS    0F
00003EB8  4110 8EF8                       000010F8  3251+         LA    R1,V1FUDGE        load v21 fudge
00003EBC  E751 0000 0806                  00000000  3252+         VL    v21,0(R1)
00003EC2  E310 5024 0014                  00000024  3253+         LGF   R1,V2ADDR          load v2 source
00003EC8  E761 0000 0806                  00000000  3254+         VL    v22,0(R1)          use v21 to test decoder
00003ECE  E756 0010 0C5C                            3255+         VISTR V21,V22,0,1                test instruction
00003ED4  B98D 0020                                 3256+         EPSW  R2,R0              extract psw
00003ED8  5020 500C                       0000000C  3257+         ST    R2,CCPSW              to save CC
00003EDC  E750 5040 080E                  00003EA0  3258+         VST   V21,V1O70          save v1 output
00003EE2  07FB                                      3259+         BR    R11                return
00003EE4                                            3260+RE70     DC    0F                 V1 for this test
00003EE4                                            3261+         DROP  R5
00003EE4  88888800 00000000                         3262          DC    XL16'88888800 00000000 00000000 00000000'   v1
00003EEC  00000000 00000000
00003EF4  88888800 88888888                         3263          DC    XL16'88888800 88888888 88880088 88888888'   v2
00003EFC  88880088 88888888
                                                    3264
                                                    3265 *halfword
                                                    3266          VRR_A VISTR,1,1,0
00003F08                                            3267+         DS    0FD
00003F08                          00003F08          3268+         USING *,R5               base for test data and test routine
00003F08  00003F60                                  3269+T71      DC    A(X71)             address of test routine
00003F0C  0047                                      3270+         DC    H'71'              test number
00003F0E  00                                        3271+         DC    X'00'
00003F0F  01                                        3272+         DC    HL1'1'                  M3 used
00003F10  01                                        3273+         DC    HL1'1'                  M5 used
00003F11  00                                        3274+         DC    HL1'0'             CC
00003F12  07                                        3275+         DC    HL1'7'             CC failed mask
00003F14  00000000 00000000                         3276+         DS    2F                 extracted PSW after test (has CC)
00003F1C  FF                                        3277+         DC    X'FF'              extracted CC, if test failed
00003F1D  E5C9E2E3 D9404040                         3278+         DC    CL8'VISTR'         instruction name
00003F28  00003F8C                                  3279+         DC    A(RE71)            address of v1 result
00003F2C  00003F9C                                  3280+         DC    A(RE71+16)         address of v2 source
00003F30  00003FAC                                  3281+         DC    A(RE71+32)         address of v3 source
00003F34  00000010                                  3282+         DC    A(16)              result length
00003F38  00003F8C                                  3283+REA71    DC    A(RE71)            result address
00003F40  00000000 00000000                         3284+         DS    FD                 gap
00003F48  00000000 00000000                         3285+V1O71    DS    XL16               V1 output
00003F50  00000000 00000000
00003F58  00000000 00000000                         3286+         DS    FD                 gap
                                                    3287+*
00003F60                                            3288+X71      DS    0F
00003F60  4110 8EF8                       000010F8  3289+         LA    R1,V1FUDGE        load v21 fudge
00003F64  E751 0000 0806                  00000000  3290+         VL    v21,0(R1)
00003F6A  E310 5024 0014                  00000024  3291+         LGF   R1,V2ADDR          load v2 source
00003F70  E761 0000 0806                  00000000  3292+         VL    v22,0(R1)          use v21 to test decoder
00003F76  E756 0010 1C5C                            3293+         VISTR V21,V22,1,1                test instruction
00003F7C  B98D 0020                                 3294+         EPSW  R2,R0              extract psw
00003F80  5020 500C                       0000000C  3295+         ST    R2,CCPSW              to save CC
00003F84  E750 5040 080E                  00003F48  3296+         VST   V21,V1O71          save v1 output
00003F8A  07FB                                      3297+         BR    R11                return
00003F8C                                            3298+RE71     DC    0F                 V1 for this test
00003F8C                                            3299+         DROP  R5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003F8C  88888888 88888888                      3300          DC    XL16'88888888 88888888 88888888 00000000'   v1
00003F94  88888888 00000000
00003F9C  88888888 88888888                      3301          DC    XL16'88888888 88888888 88888888 00008888'   v2
00003FA4  88888888 00008888
                                                 3302
                                                 3303          VRR_A VISTR,1,1,0
00003FB0                                         3304+         DS    0FD
00003FB0                    00003FB0             3305+         USING *,R5                base for test data and test routine
00003FB0  00004008                               3306+T72      DC    A(X72)              address of test routine
00003FB4  0048                                   3307+         DC    H'72'               test number
00003FB6  00                                     3308+         DC    X'00'
00003FB7  01                                     3309+         DC    HL1'1'                   M3 used
00003FB8  01                                     3310+         DC    HL1'1'                   M5 used
00003FB9  00                                     3311+         DC    HL1'0'              CC
00003FBA  07                                     3312+         DC    HL1'7'              CC failed mask
00003FBC  00000000 00000000                      3313+         DS    2F                  extracted PSW after test (has CC)
00003FC4  FF                                     3314+         DC    X'FF'               extracted CC, if test failed
00003FC5  E5C9E2E3 D9404040                      3315+         DC    CL8'VISTR'          instruction name
00003FD0  00004034                               3316+         DC    A(RE72)             address of v1 result
00003FD4  00004044                               3317+         DC    A(RE72+16)          address of v2 source
00003FD8  00004054                               3318+         DC    A(RE72+32)          address of v3 source
00003FDC  00000010                               3319+         DC    A(16)               result length
00003FE0  00004034                               3320+REA72    DC    A(RE72)             result address
00003FE8  00000000 00000000                      3321+         DS    FD                  gap
00003FF0  00000000 00000000                      3322+V1O72    DS    XL16                V1 output
00003FF8  00000000 00000000
00004000  00000000 00000000                      3323+         DS    FD                  gap
                                                 3324+*
00004008                                         3325+X72      DS    0F
00004008  4110 8EF8                   000010F8   3326+         LA    R1,V1FUDGE        load v21 fudge
0000400C  E751 0000 0806              00000000   3327+         VL    v21,0(R1)
00004012  E310 5024 0014              00000024   3328+         LGF   R1,V2ADDR          load v2 source
00004018  E761 0000 0806              00000000   3329+         VL    v22,0(R1)           use v21 to test decoder
0000401E  E756 0010 1C5C                         3330+         VISTR V21,V22,1,1                test instruction
00004024  B98D 0020                              3331+         EPSW  R2,R0               extract psw
00004028  5020 500C                   0000000C   3332+         ST    R2,CCPSW               to save CC
0000402C  E750 5040 080E              00003FF0   3333+         VST   V21,V1O72           save v1 output
00004032  07FB                                   3334+         BR    R11                 return
00004034                                         3335+RE72     DC    0F                  V1 for this test
00004034                                         3336+         DROP  R5
00004034  88888888 00000000                      3337          DC    XL16'88888888 00000000 00000000 00000000'   v1
0000403C  00000000 00000000
00004044  88888888 00008888                      3338          DC    XL16'88888888 00008888 88888888 88888888'   v2
0000404C  88888888 88888888
                                                 3339
                                                 3340          VRR_A VISTR,1,1,0
00004058                                         3341+         DS    0FD
00004058                    00004058             3342+         USING *,R5                base for test data and test routine
00004058  000040B0                               3343+T73      DC    A(X73)              address of test routine
0000405C  0049                                   3344+         DC    H'73'               test number
0000405E  00                                     3345+         DC    X'00'
0000405F  01                                     3346+         DC    HL1'1'                   M3 used
00004060  01                                     3347+         DC    HL1'1'                   M5 used
00004061  00                                     3348+         DC    HL1'0'              CC
00004062  07                                     3349+         DC    HL1'7'              CC failed mask
00004064  00000000 00000000                      3350+         DS    2F                  extracted PSW after test (has CC)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000406C  FF                                       3351+          DC    X'FF'                extracted CC, if test failed
0000406D  E5C9E2E3 D9404040                        3352+          DC    CL8'VISTR'           instruction name
00004078  000040DC                                 3353+          DC    A(RE73)              address of v1 result
0000407C  000040EC                                 3354+          DC    A(RE73+16)           address of v2 source
00004080  000040FC                                 3355+          DC    A(RE73+32)           address of v3 source
00004084  00000010                                 3356+          DC    A(16)                result length
00004088  000040DC                                 3357+REA73     DC    A(RE73)              result address
00004090  00000000 00000000                        3358+          DS    FD                   gap
00004098  00000000 00000000                        3359+V1O73     DS    XL16                 V1 output
000040A0  00000000 00000000
000040A8  00000000 00000000                        3360+          DS    FD                   gap
                                                   3361+*
000040B0                                           3362+X73       DS    0F
000040B0  4110 8EF8                      000010F8  3363+          LA    R1,V1FUDGE          load v21 fudge
000040B4  E751 0000 0806                 00000000  3364+          VL    v21,0(R1)
000040BA  E310 5024 0014                 00000024  3365+          LGF   R1,V2ADDR            load v2 source
000040C0  E761 0000 0806                 00000000  3366+          VL    v22,0(R1)            use v21 to test decoder
000040C6  E756 0010 1C5C                           3367+          VISTR V21,V22,1,1                 test instruction
000040CC  B98D 0020                                3368+          EPSW  R2,R0                extract psw
000040D0  5020 500C                      0000000C  3369+          ST    R2,CCPSW                to save CC
000040D4  E750 5040 080E                 00004098  3370+          VST   V21,V1O73            save v1 output
000040DA  07FB                                     3371+          BR    R11                  return
000040DC                                           3372+RE73      DC    0F                   V1 for this test
000040DC                                           3373+          DROP  R5
000040DC  88888888 88888888                        3374           DC    XL16'88888888 88888888 00000000 00000000'   v1
000040E4  00000000 00000000
000040EC  88888888 88888888                        3375           DC    XL16'88888888 88888888 00000888 00008888'   v2
000040F4  00000888 00008888
                                                   3376
                                                   3377           VRR_A VISTR,1,1,0
00004100                                           3378+          DS    0FD
00004100                       00004100            3379+          USING *,R5                 base for test data and test routine
00004100  00004158                                 3380+T74       DC    A(X74)               address of test routine
00004104  004A                                     3381+          DC    H'74'                test number
00004106  00                                       3382+          DC    X'00'
00004107  01                                       3383+          DC    HL1'1'                    M3 used
00004108  01                                       3384+          DC    HL1'1'                    M5 used
00004109  00                                       3385+          DC    HL1'0'               CC
0000410A  07                                       3386+          DC    HL1'7'               CC failed mask
0000410C  00000000 00000000                        3387+          DS    2F                   extracted PSW after test (has CC)
00004114  FF                                       3388+          DC    X'FF'                extracted CC, if test failed
00004115  E5C9E2E3 D9404040                        3389+          DC    CL8'VISTR'           instruction name
00004120  00004184                                 3390+          DC    A(RE74)              address of v1 result
00004124  00004194                                 3391+          DC    A(RE74+16)           address of v2 source
00004128  000041A4                                 3392+          DC    A(RE74+32)           address of v3 source
0000412C  00000010                                 3393+          DC    A(16)                result length
00004130  00004184                                 3394+REA74     DC    A(RE74)              result address
00004138  00000000 00000000                        3395+          DS    FD                   gap
00004140  00000000 00000000                        3396+V1O74     DS    XL16                 V1 output
00004148  00000000 00000000
00004150  00000000 00000000                        3397+          DS    FD                   gap
                                                   3398+*
00004158                                           3399+X74       DS    0F
00004158  4110 8EF8                      000010F8  3400+          LA    R1,V1FUDGE          load v21 fudge
0000415C  E751 0000 0806                 00000000  3401+          VL    v21,0(R1)
00004162  E310 5024 0014                 00000024  3402+          LGF   R1,V2ADDR            load v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004168  E761 0000 0806                 00000000  3403+         VL    v22,0(R1)          use v21 to test decoder
0000416E  E756 0010 1C5C                           3404+         VISTR V21,V22,1,1                test instruction
00004174  B98D 0020                                3405+         EPSW  R2,R0              extract psw
00004178  5020 500C                      0000000C  3406+         ST    R2,CCPSW              to save CC
0000417C  E750 5040 080E                 00004140  3407+         VST   V21,V1O74          save v1 output
00004182  07FB                                     3408+         BR    R11                return
00004184                                           3409+RE74     DC    0F                 V1 for this test
00004184                                           3410+         DROP  R5
00004184  88880000 00000000                        3411          DC    XL16'88880000 00000000 00000000 00000000'   v1
0000418C  00000000 00000000
00004194  88880000 88888888                        3412          DC    XL16'88880000 88888888 00000888 00008888'   v2
0000419C  00000888 00008888
                                                   3413 *-------------------------------------------------------------------
                                                   3414 * case 4 -  misc                                          CS=1
                                                   3415 *-------------------------------------------------------------------
                                                   3416
                                                   3417          VRR_A VISTR,0,1,0
000041A8                                           3418+         DS    0FD
000041A8                 000041A8                  3419+         USING *,R5               base for test data and test routine
000041A8  00004200                                 3420+T75      DC    A(X75)             address of test routine
000041AC  004B                                     3421+         DC    H'75'              test number
000041AE  00                                       3422+         DC    X'00'
000041AF  00                                       3423+         DC    HL1'0'                  M3 used
000041B0  01                                       3424+         DC    HL1'1'                  M5 used
000041B1  00                                       3425+         DC    HL1'0'             CC
000041B2  07                                       3426+         DC    HL1'7'             CC failed mask
000041B4  00000000 00000000                        3427+         DS    2F                 extracted PSW after test (has CC)
000041BC  FF                                       3428+         DC    X'FF'              extracted CC, if test failed
000041BD  E5C9E2E3 D9404040                        3429+         DC    CL8'VISTR'         instruction name
000041C8  0000422C                                 3430+         DC    A(RE75)            address of v1 result
000041CC  0000423C                                 3431+         DC    A(RE75+16)         address of v2 source
000041D0  0000424C                                 3432+         DC    A(RE75+32)         address of v3 source
000041D4  00000010                                 3433+         DC    A(16)              result length
000041D8  0000422C                                 3434+REA75    DC    A(RE75)            result address
000041E0  00000000 00000000                        3435+         DS    FD                 gap
000041E8  00000000 00000000                        3436+V1O75    DS    XL16               V1 output
000041F0  00000000 00000000
000041F8  00000000 00000000                        3437+         DS    FD                 gap
                                                   3438+*
00004200                                           3439+X75      DS    0F
00004200  4110 8EF8                      000010F8  3440+         LA    R1,V1FUDGE        load v21 fudge
00004204  E751 0000 0806                 00000000  3441+         VL    v21,0(R1)
0000420A  E310 5024 0014                 00000024  3442+         LGF   R1,V2ADDR          load v2 source
00004210  E761 0000 0806                 00000000  3443+         VL    v22,0(R1)          use v21 to test decoder
00004216  E756 0010 0C5C                           3444+         VISTR V21,V22,0,1                test instruction
0000421C  B98D 0020                                3445+         EPSW  R2,R0              extract psw
00004220  5020 500C                      0000000C  3446+         ST    R2,CCPSW              to save CC
00004224  E750 5040 080E                 000041E8  3447+         VST   V21,V1O75          save v1 output
0000422A  07FB                                     3448+         BR    R11                return
0000422C                                           3449+RE75     DC    0F                 V1 for this test
0000422C                                           3450+         DROP  R5
0000422C  88838182 84868700                        3451          DC    XL16'88838182 84868700 00000000 00000000'   v1
00004234  00000000 00000000
0000423C  88838182 84868700                        3452          DC    XL16'88838182 84868700 81880000 000D1111'   v2
00004244  81880000 000D1111
                                                   3453
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     3454
0000424C  00000000                                   3455          DC    F'0'     END OF TABLE
00004250  00000000                                   3456          DC    F'0'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3458 *
                                                   3459 * table of pointers to individual tests
                                                   3460 *
00004254                                           3461 E7TESTS  DS    0F
                                                   3462          PTTABLE
00004254                                           3463+TTABLE   DS    0F
00004254  00001118                                 3464+         DC    A(T1)                    test address
00004258  000011C0                                 3465+         DC    A(T2)                    test address
0000425C  00001268                                 3466+         DC    A(T3)                    test address
00004260  00001310                                 3467+         DC    A(T4)                    test address
00004264  000013B8                                 3468+         DC    A(T5)                    test address
00004268  00001460                                 3469+         DC    A(T6)                    test address
0000426C  00001508                                 3470+         DC    A(T7)                    test address
00004270  000015B0                                 3471+         DC    A(T8)                    test address
00004274  00001658                                 3472+         DC    A(T9)                    test address
00004278  00001700                                 3473+         DC    A(T10)                   test address
0000427C  000017A8                                 3474+         DC    A(T11)                   test address
00004280  00001850                                 3475+         DC    A(T12)                   test address
00004284  000018F8                                 3476+         DC    A(T13)                   test address
00004288  000019A0                                 3477+         DC    A(T14)                   test address
0000428C  00001A48                                 3478+         DC    A(T15)                   test address
00004290  00001AF0                                 3479+         DC    A(T16)                   test address
00004294  00001B98                                 3480+         DC    A(T17)                   test address
00004298  00001C40                                 3481+         DC    A(T18)                   test address
0000429C  00001CE8                                 3482+         DC    A(T19)                   test address
000042A0  00001D90                                 3483+         DC    A(T20)                   test address
000042A4  00001E38                                 3484+         DC    A(T21)                   test address
000042A8  00001EE0                                 3485+         DC    A(T22)                   test address
000042AC  00001F88                                 3486+         DC    A(T23)                   test address
000042B0  00002030                                 3487+         DC    A(T24)                   test address
000042B4  000020D8                                 3488+         DC    A(T25)                   test address
000042B8  00002180                                 3489+         DC    A(T26)                   test address
000042BC  00002228                                 3490+         DC    A(T27)                   test address
000042C0  000022D0                                 3491+         DC    A(T28)                   test address
000042C4  00002378                                 3492+         DC    A(T29)                   test address
000042C8  00002420                                 3493+         DC    A(T30)                   test address
000042CC  000024C8                                 3494+         DC    A(T31)                   test address
000042D0  00002570                                 3495+         DC    A(T32)                   test address
000042D4  00002618                                 3496+         DC    A(T33)                   test address
000042D8  000026C0                                 3497+         DC    A(T34)                   test address
000042DC  00002768                                 3498+         DC    A(T35)                   test address
000042E0  00002810                                 3499+         DC    A(T36)                   test address
000042E4  000028B8                                 3500+         DC    A(T37)                   test address
000042E8  00002960                                 3501+         DC    A(T38)                   test address
000042EC  00002A08                                 3502+         DC    A(T39)                   test address
000042F0  00002AB0                                 3503+         DC    A(T40)                   test address
000042F4  00002B58                                 3504+         DC    A(T41)                   test address
000042F8  00002C00                                 3505+         DC    A(T42)                   test address
000042FC  00002CA8                                 3506+         DC    A(T43)                   test address
00004300  00002D50                                 3507+         DC    A(T44)                   test address
00004304  00002DF8                                 3508+         DC    A(T45)                   test address
00004308  00002EA0                                 3509+         DC    A(T46)                   test address
0000430C  00002F48                                 3510+         DC    A(T47)                   test address
00004310  00002FF0                                 3511+         DC    A(T48)                   test address
00004314  00003098                                 3512+         DC    A(T49)                   test address
00004318  00003140                                 3513+         DC    A(T50)                   test address
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000431C  000031E8                             3514+          DC    A(T51)                  test address
00004320  00003290                             3515+          DC    A(T52)                  test address
00004324  00003338                             3516+          DC    A(T53)                  test address
00004328  000033E0                             3517+          DC    A(T54)                  test address
0000432C  00003488                             3518+          DC    A(T55)                  test address
00004330  00003530                             3519+          DC    A(T56)                  test address
00004334  000035D8                             3520+          DC    A(T57)                  test address
00004338  00003680                             3521+          DC    A(T58)                  test address
0000433C  00003728                             3522+          DC    A(T59)                  test address
00004340  000037D0                             3523+          DC    A(T60)                  test address
00004344  00003878                             3524+          DC    A(T61)                  test address
00004348  00003920                             3525+          DC    A(T62)                  test address
0000434C  000039C8                             3526+          DC    A(T63)                  test address
00004350  00003A70                             3527+          DC    A(T64)                  test address
00004354  00003B18                             3528+          DC    A(T65)                  test address
00004358  00003BC0                             3529+          DC    A(T66)                  test address
0000435C  00003C68                             3530+          DC    A(T67)                  test address
00004360  00003D10                             3531+          DC    A(T68)                  test address
00004364  00003DB8                             3532+          DC    A(T69)                  test address
00004368  00003E60                             3533+          DC    A(T70)                  test address
0000436C  00003F08                             3534+          DC    A(T71)                  test address
00004370  00003FB0                             3535+          DC    A(T72)                  test address
00004374  00004058                             3536+          DC    A(T73)                  test address
00004378  00004100                             3537+          DC    A(T74)                  test address
0000437C  000041A8                             3538+          DC    A(T75)                  test address
                                               3539+*
00004380  00000000                             3540+          DC    A(0)                    end of table
00004384  00000000                             3541+          DC    A(0)                    end of table
                                               3542
00004388  00000000                             3543           DC    F'0'     END OF TABLE
0000438C  00000000                             3544           DC    F'0'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                         3546 ********************************************************************************
                                         3547 *        Register equates
                                         3548 ********************************************************************************


                           00000000  00000001  3550 R0       EQU   0
                           00000001  00000001  3551 R1       EQU   1
                           00000002  00000001  3552 R2       EQU   2
                           00000003  00000001  3553 R3       EQU   3
                           00000004  00000001  3554 R4       EQU   4
                           00000005  00000001  3555 R5       EQU   5
                           00000006  00000001  3556 R6       EQU   6
                           00000007  00000001  3557 R7       EQU   7
                           00000008  00000001  3558 R8       EQU   8
                           00000009  00000001  3559 R9       EQU   9
                           0000000A  00000001  3560 R10      EQU   10
                           0000000B  00000001  3561 R11      EQU   11
                           0000000C  00000001  3562 R12      EQU   12
                           0000000D  00000001  3563 R13      EQU   13
                           0000000E  00000001  3564 R14      EQU   14
                           0000000F  00000001  3565 R15      EQU   15


                                         3567 ********************************************************************************
                                         3568 *        Register equates
                                         3569 ********************************************************************************


                           00000000  00000001  3571 V0       EQU   0
                           00000001  00000001  3572 V1       EQU   1
                           00000002  00000001  3573 V2       EQU   2
                           00000003  00000001  3574 V3       EQU   3
                           00000004  00000001  3575 V4       EQU   4
                           00000005  00000001  3576 V5       EQU   5
                           00000006  00000001  3577 V6       EQU   6
                           00000007  00000001  3578 V7       EQU   7
                           00000008  00000001  3579 V8       EQU   8
                           00000009  00000001  3580 V9       EQU   9
                           0000000A  00000001  3581 V10      EQU   10
                           0000000B  00000001  3582 V11      EQU   11
                           0000000C  00000001  3583 V12      EQU   12
                           0000000D  00000001  3584 V13      EQU   13
                           0000000E  00000001  3585 V14      EQU   14
                           0000000F  00000001  3586 V15      EQU   15
                           00000010  00000001  3587 V16      EQU   16
                           00000011  00000001  3588 V17      EQU   17
                           00000012  00000001  3589 V18      EQU   18
                           00000013  00000001  3590 V19      EQU   19
                           00000014  00000001  3591 V20      EQU   20
                           00000015  00000001  3592 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001  3593 V22       EQU   22
                                00000017  00000001  3594 V23       EQU   23
                                00000018  00000001  3595 V24       EQU   24
                                00000019  00000001  3596 V25       EQU   25
                                0000001A  00000001  3597 V26       EQU   26
                                0000001B  00000001  3598 V27       EQU   27
                                0000001C  00000001  3599 V28       EQU   28
                                0000001D  00000001  3600 V29       EQU   29
                                0000001E  00000001  3601 V30       EQU   30
                                0000001F  00000001  3602 V31       EQU   31
                                                    3603
                                                    3604           END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	151	117 147 148 149
CC	U	00000009	1	512	262
CCFOUND	X	00000014	1	518	249 269
CCMASK	U	0000000A	1	513	219
CCMSG	U	0000031C	1	236	231
CCPRTEXP	C	00001098	1	477	266
CCPRTGOT	C	000010A8	1	480	273
CCPRTLINE	C	00001055	16	472	482 276
CCPRTLNG	U	00000055	1	482	275
CCPRTNAME	C	00001082	8	475	259
CCPRTNUM	C	00001065	3	473	257
CCPSW	F	0000000C	4	517	246 684 721 758 796 833 870 908 945 982 1023 1060 1097 1134 1171 1208 1245 1282 1319 1356 1393 1430 1467 1504 1541 1578 1616 1653 1690 1727 1764 1801 1838 1875 1912 1950 1987 2024 2061 2098 2140 2177 2214 2251 2288 2325 2362 2399 2436 2473 2510 2547 2584 2621 2660 2697 2734 2771 2808 2845 2882 2920 2957 2994 3031 3072 3109 3146 3183 3220 3257 3295 3332 3369 3406 3446
CTLR0	F	00000554	4	415	161 162 163 164
DECNUM	C	000010D6	16	492	254 256 263 265 270 272 292 294 301 303 308 310
E7TEST	4	00000000	88	506	210
E7TESTS	F	00004254	4	3461	203
EDIT	X	000010AA	18	487	255 264 271 293 302 309
ENDTEST	U	00000428	1	330	208
EOJ	I	00000538	4	405	196 333
EOJPSW	D	00000528	8	403	405
FAILCONT	U	00000418	1	320	
FAILED	F	00001000	4	445	280 322 331
FAILMSG	U	000003B0	1	290	226
FAILPSW	D	00000540	8	407	409
FAILTEST	I	00000550	4	409	334
FB0001	F	00000280	8	180	184 185 187
IMAGE	1	00000000	17296	0	
K	U	00000400	1	429	430 431 432
K64	U	00010000	1	431	
M3	U	00000007	1	510	300
M5	U	00000008	1	511	240 307
MB	U	00100000	1	432	
MSG	I	00000470	4	365	195 348
MSGCMD	C	000004BE	9	395	378 379
MSGMSG	C	000004C7	95	396	372 393 370
MSGMVC	I	000004B8	6	393	376
MSGOK	I	00000486	2	374	371
MSGRET	I	000004A6	4	389	382 385
MSGSAVE	F	000004AC	4	392	368 389
NEXTE7	U	000002D4	1	205	229 325
OPNAME	C	00000015	8	520	259 297
PAGE	U	00001000	1	430	
PRT3	C	000010C0	18	490	255 256 257 264 265 266 271 272 273 293 294 295 302 303 304 309 310 311
PRTLINE	C	00001008	16	454	464 314
PRTLNG	U	0000004D	1	464	313
PRTM3	C	00001044	3	459	304
PRTM5	C	00001051	3	462	311
PRTNAME	C	00001033	8	457	297
PRTNUM	C	00001018	3	455	295
R0	U	00000000	1	3550	111 161 164 184 186 187 188 193 212 213 275 279 280

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					313 321 322 347 349 365 368 370 372 374 389 683 720
					757 795 832 869 907 944 981 1022 1059 1096 1133 1170 1207
					1244 1281 1318 1355 1392 1429 1466 1503 1540 1577 1615 1652 1689
					1726 1763 1800 1837 1874 1911 1949 1986 2023 2060 2097 2139 2176
					2213 2250 2287 2324 2361 2398 2435 2472 2509 2546 2583 2620 2659
					2696 2733 2770 2807 2844 2881 2919 2956 2993 3030 3071 3108 3145
					3182 3219 3256 3294 3331 3368 3405 3445
R1	U	00000001	1	3551	194 219 220 221 224 225 240 241 246 247 248 249 276
					314 331 332 379 393 678 679 680 681 715 716 717 718
					752 753 754 755 790 791 792 793 827 828 829 830 864
					865 866 867 902 903 904 905 939 940 941 942 976 977
					978 979 1017 1018 1019 1020 1054 1055 1056 1057 1091 1092 1093
					1094 1128 1129 1130 1131 1165 1166 1167 1168 1202 1203 1204 1205
					1239 1240 1241 1242 1276 1277 1278 1279 1313 1314 1315 1316 1350
					1351 1352 1353 1387 1388 1389 1390 1424 1425 1426 1427 1461 1462
					1463 1464 1498 1499 1500 1501 1535 1536 1537 1538 1572 1573 1574
					1575 1610 1611 1612 1613 1647 1648 1649 1650 1684 1685 1686 1687
					1721 1722 1723 1724 1758 1759 1760 1761 1795 1796 1797 1798 1832
					1833 1834 1835 1869 1870 1871 1872 1906 1907 1908 1909 1944 1945
					1946 1947 1981 1982 1983 1984 2018 2019 2020 2021 2055 2056 2057
					2058 2092 2093 2094 2095 2134 2135 2136 2137 2171 2172 2173 2174
					2208 2209 2210 2211 2245 2246 2247 2248 2282 2283 2284 2285 2319
					2320 2321 2322 2356 2357 2358 2359 2393 2394 2395 2396 2430 2431
					2432 2433 2467 2468 2469 2470 2504 2505 2506 2507 2541 2542 2543
					2544 2578 2579 2580 2581 2615 2616 2617 2618 2654 2655 2656 2657
					2691 2692 2693 2694 2728 2729 2730 2731 2765 2766 2767 2768 2802
					2803 2804 2805 2839 2840 2841 2842 2876 2877 2878 2879 2914 2915
					2916 2917 2951 2952 2953 2954 2988 2989 2990 2991 3025 3026 3027
					3028 3066 3067 3068 3069 3103 3104 3105 3106 3140 3141 3142 3143
					3177 3178 3179 3180 3214 3215 3216 3217 3251 3252 3253 3254 3289
					3290 3291 3292 3326 3327 3328 3329 3363 3364 3365 3366 3400 3401
					3402 3403 3440 3441 3442 3443
R10	U	0000000A	1	3560	149 158 159
R11	U	0000000B	1	3561	216 217 686 723 760 798 835 872 910 947 984 1025 1062
					1099 1136 1173 1210 1247 1284 1321 1358 1395 1432 1469 1506 1543
					1580 1618 1655 1692 1729 1766 1803 1840 1877 1914 1952 1989 2026
					2063 2100 2142 2179 2216 2253 2290 2327 2364 2401 2438 2475 2512
					2549 2586 2623 2662 2699 2736 2773 2810 2847 2884 2922 2959 2996
					3033 3074 3111 3148 3185 3222 3259 3297 3334 3371 3408 3448
R12	U	0000000C	1	3562	203 206 228 324
R13	U	0000000D	1	3563	
R14	U	0000000E	1	3564	
R15	U	0000000F	1	3565	277 315 342 352 353
R2	U	00000002	1	3552	195 253 254 261 262 263 268 269 270 291 292 299 300
					301 306 307 308 347 348 349 366 368 374 375 376 378
					384 389 390 683 684 720 721 757 758 795 796 832 833
					869 870 907 908 944 945 981 982 1022 1023 1059 1060 1096
					1097 1133 1134 1170 1171 1207 1208 1244 1245 1281 1282 1318 1319
					1355 1356 1392 1393 1429 1430 1466 1467 1503 1504 1540 1541 1577
					1578 1615 1616 1652 1653 1689 1690 1726 1727 1763 1764 1800 1801
					1837 1838 1874 1875 1911 1912 1949 1950 1986 1987 2023 2024 2060
					2061 2097 2098 2139 2140 2176 2177 2213 2214 2250 2251 2287 2288
					2324 2325 2361 2362 2398 2399 2435 2436 2472 2473 2509 2510 2546
					2547 2583 2584 2620 2621 2659 2660 2696 2697 2733 2734 2770 2771
					2807 2808 2844 2845 2881 2882 2919 2920 2956 2957 2993 2994 3030
					3031 3071 3072 3108 3109 3145 3146 3182 3183 3219 3220 3256 3257

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					3294 3295 3331 3332 3368 3369 3405 3406 3445 3446
R3	U	00000003	1	3553	
R4	U	00000004	1	3554	
R5	U	00000005	1	3555	206 207 210 343 351 657 688 694 725 731 762 769 800
					806 837 843 874 881 912 918 949 955 986 996 1027 1033
					1064 1070 1101 1107 1138 1144 1175 1181 1212 1218 1249 1255 1286
					1292 1323 1329 1360 1366 1397 1403 1434 1440 1471 1477 1508 1514
					1545 1551 1582 1589 1620 1626 1657 1663 1694 1700 1731 1737 1768
					1774 1805 1811 1842 1848 1879 1885 1916 1923 1954 1960 1991 1997
					2028 2034 2065 2071 2102 2113 2144 2150 2181 2187 2218 2224 2255
					2261 2292 2298 2329 2335 2366 2372 2403 2409 2440 2446 2477 2483
					2514 2520 2551 2557 2588 2594 2625 2633 2664 2670 2701 2707 2738
					2744 2775 2781 2812 2818 2849 2855 2886 2893 2924 2930 2961 2967
					2998 3004 3035 3045 3076 3082 3113 3119 3150 3156 3187 3193 3224
					3230 3261 3268 3299 3305 3336 3342 3373 3379 3410 3419 3450
R6	U	00000006	1	3556	
R7	U	00000007	1	3557	
R8	U	00000008	1	3558	147 151 152 153 155
R9	U	00000009	1	3559	148 155 156 158
RE1	F	0000119C	4	687	668 669 670 672
RE10	F	00001784	4	1026	1007 1008 1009 1011
RE11	F	0000182C	4	1063	1044 1045 1046 1048
RE12	F	000018D4	4	1100	1081 1082 1083 1085
RE13	F	0000197C	4	1137	1118 1119 1120 1122
RE14	F	00001A24	4	1174	1155 1156 1157 1159
RE15	F	00001ACC	4	1211	1192 1193 1194 1196
RE16	F	00001B74	4	1248	1229 1230 1231 1233
RE17	F	00001C1C	4	1285	1266 1267 1268 1270
RE18	F	00001CC4	4	1322	1303 1304 1305 1307
RE19	F	00001D6C	4	1359	1340 1341 1342 1344
RE2	F	00001244	4	724	705 706 707 709
RE20	F	00001E14	4	1396	1377 1378 1379 1381
RE21	F	00001EBC	4	1433	1414 1415 1416 1418
RE22	F	00001F64	4	1470	1451 1452 1453 1455
RE23	F	0000200C	4	1507	1488 1489 1490 1492
RE24	F	000020B4	4	1544	1525 1526 1527 1529
RE25	F	0000215C	4	1581	1562 1563 1564 1566
RE26	F	00002204	4	1619	1600 1601 1602 1604
RE27	F	000022AC	4	1656	1637 1638 1639 1641
RE28	F	00002354	4	1693	1674 1675 1676 1678
RE29	F	000023FC	4	1730	1711 1712 1713 1715
RE3	F	000012EC	4	761	742 743 744 746
RE30	F	000024A4	4	1767	1748 1749 1750 1752
RE31	F	0000254C	4	1804	1785 1786 1787 1789
RE32	F	000025F4	4	1841	1822 1823 1824 1826
RE33	F	0000269C	4	1878	1859 1860 1861 1863
RE34	F	00002744	4	1915	1896 1897 1898 1900
RE35	F	000027EC	4	1953	1934 1935 1936 1938
RE36	F	00002894	4	1990	1971 1972 1973 1975
RE37	F	0000293C	4	2027	2008 2009 2010 2012
RE38	F	000029E4	4	2064	2045 2046 2047 2049
RE39	F	00002A8C	4	2101	2082 2083 2084 2086
RE4	F	00001394	4	799	780 781 782 784
RE40	F	00002B34	4	2143	2124 2125 2126 2128
RE41	F	00002BDC	4	2180	2161 2162 2163 2165
RE42	F	00002C84	4	2217	2198 2199 2200 2202

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE43	F	00002D2C	4	2254	2235	2236	2237	2239
RE44	F	00002DD4	4	2291	2272	2273	2274	2276
RE45	F	00002E7C	4	2328	2309	2310	2311	2313
RE46	F	00002F24	4	2365	2346	2347	2348	2350
RE47	F	00002FCC	4	2402	2383	2384	2385	2387
RE48	F	00003074	4	2439	2420	2421	2422	2424
RE49	F	0000311C	4	2476	2457	2458	2459	2461
RE5	F	0000143C	4	836	817	818	819	821
RE50	F	000031C4	4	2513	2494	2495	2496	2498
RE51	F	0000326C	4	2550	2531	2532	2533	2535
RE52	F	00003314	4	2587	2568	2569	2570	2572
RE53	F	000033BC	4	2624	2605	2606	2607	2609
RE54	F	00003464	4	2663	2644	2645	2646	2648
RE55	F	0000350C	4	2700	2681	2682	2683	2685
RE56	F	000035B4	4	2737	2718	2719	2720	2722
RE57	F	0000365C	4	2774	2755	2756	2757	2759
RE58	F	00003704	4	2811	2792	2793	2794	2796
RE59	F	000037AC	4	2848	2829	2830	2831	2833
RE6	F	000014E4	4	873	854	855	856	858
RE60	F	00003854	4	2885	2866	2867	2868	2870
RE61	F	000038FC	4	2923	2904	2905	2906	2908
RE62	F	000039A4	4	2960	2941	2942	2943	2945
RE63	F	00003A4C	4	2997	2978	2979	2980	2982
RE64	F	00003AF4	4	3034	3015	3016	3017	3019
RE65	F	00003B9C	4	3075	3056	3057	3058	3060
RE66	F	00003C44	4	3112	3093	3094	3095	3097
RE67	F	00003CEC	4	3149	3130	3131	3132	3134
RE68	F	00003D94	4	3186	3167	3168	3169	3171
RE69	F	00003E3C	4	3223	3204	3205	3206	3208
RE7	F	0000158C	4	911	892	893	894	896
RE70	F	00003EE4	4	3260	3241	3242	3243	3245
RE71	F	00003F8C	4	3298	3279	3280	3281	3283
RE72	F	00004034	4	3335	3316	3317	3318	3320
RE73	F	000040DC	4	3372	3353	3354	3355	3357
RE74	F	00004184	4	3409	3390	3391	3392	3394
RE75	F	0000422C	4	3449	3430	3431	3432	3434
RE8	F	00001634	4	948	929	930	931	933
RE9	F	000016DC	4	985	966	967	968	970
REA1	A	00001148	4	672				
REA10	A	00001730	4	1011				
REA11	A	000017D8	4	1048				
REA12	A	00001880	4	1085				
REA13	A	00001928	4	1122				
REA14	A	000019D0	4	1159				
REA15	A	00001A78	4	1196				
REA16	A	00001B20	4	1233				
REA17	A	00001BC8	4	1270				
REA18	A	00001C70	4	1307				
REA19	A	00001D18	4	1344				
REA2	A	000011F0	4	709				
REA20	A	00001DC0	4	1381				
REA21	A	00001E68	4	1418				
REA22	A	00001F10	4	1455				
REA23	A	00001FB8	4	1492				
REA24	A	00002060	4	1529				
REA25	A	00002108	4	1566				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA26	A	000021B0	4	1604	
REA27	A	00002258	4	1641	
REA28	A	00002300	4	1678	
REA29	A	000023A8	4	1715	
REA3	A	00001298	4	746	
REA30	A	00002450	4	1752	
REA31	A	000024F8	4	1789	
REA32	A	000025A0	4	1826	
REA33	A	00002648	4	1863	
REA34	A	000026F0	4	1900	
REA35	A	00002798	4	1938	
REA36	A	00002840	4	1975	
REA37	A	000028E8	4	2012	
REA38	A	00002990	4	2049	
REA39	A	00002A38	4	2086	
REA4	A	00001340	4	784	
REA40	A	00002AE0	4	2128	
REA41	A	00002B88	4	2165	
REA42	A	00002C30	4	2202	
REA43	A	00002CD8	4	2239	
REA44	A	00002D80	4	2276	
REA45	A	00002E28	4	2313	
REA46	A	00002ED0	4	2350	
REA47	A	00002F78	4	2387	
REA48	A	00003020	4	2424	
REA49	A	000030C8	4	2461	
REA5	A	000013E8	4	821	
REA50	A	00003170	4	2498	
REA51	A	00003218	4	2535	
REA52	A	000032C0	4	2572	
REA53	A	00003368	4	2609	
REA54	A	00003410	4	2648	
REA55	A	000034B8	4	2685	
REA56	A	00003560	4	2722	
REA57	A	00003608	4	2759	
REA58	A	000036B0	4	2796	
REA59	A	00003758	4	2833	
REA6	A	00001490	4	858	
REA60	A	00003800	4	2870	
REA61	A	000038A8	4	2908	
REA62	A	00003950	4	2945	
REA63	A	000039F8	4	2982	
REA64	A	00003AA0	4	3019	
REA65	A	00003B48	4	3060	
REA66	A	00003BF0	4	3097	
REA67	A	00003C98	4	3134	
REA68	A	00003D40	4	3171	
REA69	A	00003DE8	4	3208	
REA7	A	00001538	4	896	
REA70	A	00003E90	4	3245	
REA71	A	00003F38	4	3283	
REA72	A	00003FE0	4	3320	
REA73	A	00004088	4	3357	
REA74	A	00004130	4	3394	
REA75	A	000041D8	4	3434	
REA8	A	000015E0	4	933	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA9	A	00001688	4	970		
READDR	A	00000030	4	525	224	
REG2LOW	U	000000DD	1	435		
REG2PATT	U	AABBCCDD	1	434		
RELEN	A	0000002C	4	524		
RPTDWSAV	D	00000460	8	358	347	349
RPTERROR	I	00000436	4	342	277	315
RPTSAVE	F	00000454	4	355	342	352
RPTSVR5	F	00000458	4	356	343	351
SKL0001	U	0000004E	1	177	193	
SKT0001	C	0000022A	20	174	177	194
SVOLDPSW	U	00000140	0	113		
T1	A	00001118	4	658	3464	
T10	A	00001700	4	997	3473	
T11	A	000017A8	4	1034	3474	
T12	A	00001850	4	1071	3475	
T13	A	000018F8	4	1108	3476	
T14	A	000019A0	4	1145	3477	
T15	A	00001A48	4	1182	3478	
T16	A	00001AF0	4	1219	3479	
T17	A	00001B98	4	1256	3480	
T18	A	00001C40	4	1293	3481	
T19	A	00001CE8	4	1330	3482	
T2	A	000011C0	4	695	3465	
T20	A	00001D90	4	1367	3483	
T21	A	00001E38	4	1404	3484	
T22	A	00001EE0	4	1441	3485	
T23	A	00001F88	4	1478	3486	
T24	A	00002030	4	1515	3487	
T25	A	000020D8	4	1552	3488	
T26	A	00002180	4	1590	3489	
T27	A	00002228	4	1627	3490	
T28	A	000022D0	4	1664	3491	
T29	A	00002378	4	1701	3492	
T3	A	00001268	4	732	3466	
T30	A	00002420	4	1738	3493	
T31	A	000024C8	4	1775	3494	
T32	A	00002570	4	1812	3495	
T33	A	00002618	4	1849	3496	
T34	A	000026C0	4	1886	3497	
T35	A	00002768	4	1924	3498	
T36	A	00002810	4	1961	3499	
T37	A	000028B8	4	1998	3500	
T38	A	00002960	4	2035	3501	
T39	A	00002A08	4	2072	3502	
T4	A	00001310	4	770	3467	
T40	A	00002AB0	4	2114	3503	
T41	A	00002B58	4	2151	3504	
T42	A	00002C00	4	2188	3505	
T43	A	00002CA8	4	2225	3506	
T44	A	00002D50	4	2262	3507	
T45	A	00002DF8	4	2299	3508	
T46	A	00002EA0	4	2336	3509	
T47	A	00002F48	4	2373	3510	
T48	A	00002FF0	4	2410	3511	
T49	A	00003098	4	2447	3512	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T5	A	000013B8	4	807	3468
T50	A	00003140	4	2484	3513
T51	A	000031E8	4	2521	3514
T52	A	00003290	4	2558	3515
T53	A	00003338	4	2595	3516
T54	A	000033E0	4	2634	3517
T55	A	00003488	4	2671	3518
T56	A	00003530	4	2708	3519
T57	A	000035D8	4	2745	3520
T58	A	00003680	4	2782	3521
T59	A	00003728	4	2819	3522
T6	A	00001460	4	844	3469
T60	A	000037D0	4	2856	3523
T61	A	00003878	4	2894	3524
T62	A	00003920	4	2931	3525
T63	A	000039C8	4	2968	3526
T64	A	00003A70	4	3005	3527
T65	A	00003B18	4	3046	3528
T66	A	00003BC0	4	3083	3529
T67	A	00003C68	4	3120	3530
T68	A	00003D10	4	3157	3531
T69	A	00003DB8	4	3194	3532
T7	A	00001508	4	882	3470
T70	A	00003E60	4	3231	3533
T71	A	00003F08	4	3269	3534
T72	A	00003FB0	4	3306	3535
T73	A	00004058	4	3343	3536
T74	A	00004100	4	3380	3537
T75	A	000041A8	4	3420	3538
T8	A	000015B0	4	919	3471
T9	A	00001658	4	956	3472
TESTCC	I	00000318	4	231	221
TESTING	F	00001004	4	446	213
TESTREST	U	00000300	1	223	242 282
TNUM	H	00000004	2	508	212 253 291
TSUB	A	00000000	4	507	216
TTABLE	F	00004254	4	3463	
V0	U	00000000	1	3571	
V1	U	00000001	1	3572	
V10	U	0000000A	1	3581	
V11	U	0000000B	1	3582	
V12	U	0000000C	1	3583	
V13	U	0000000D	1	3584	
V14	U	0000000E	1	3585	
V15	U	0000000F	1	3586	
V16	U	00000010	1	3587	
V17	U	00000011	1	3588	
V18	U	00000012	1	3589	
V19	U	00000013	1	3590	
V1ADDR	A	00000020	4	521	
V1FUDGE	X	000010F8	16	499	215 678 715 752 790 827 864 902 939 976 1017 1054 1091 1128 1165 1202 1239 1276 1313 1350 1387 1424 1461 1498 1535 1572 1610 1647 1684 1721 1758 1795 1832 1869 1906 1944 1981 2018 2055 2092 2134 2171 2208 2245 2282 2319 2356 2393 2430 2467 2504 2541 2578 2615 2654 2691 2728 2765 2802 2839 2876 2914 2951 2988 3025 3066 3103 3140 3177 3214 3251 3289 3326 3363 3400 3440

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V101	X	00001158	16	674	685
V1010	X	00001740	16	1013	1024
V1011	X	000017E8	16	1050	1061
V1012	X	00001890	16	1087	1098
V1013	X	00001938	16	1124	1135
V1014	X	000019E0	16	1161	1172
V1015	X	00001A88	16	1198	1209
V1016	X	00001B30	16	1235	1246
V1017	X	00001BD8	16	1272	1283
V1018	X	00001C80	16	1309	1320
V1019	X	00001D28	16	1346	1357
V102	X	00001200	16	711	722
V1020	X	00001DD0	16	1383	1394
V1021	X	00001E78	16	1420	1431
V1022	X	00001F20	16	1457	1468
V1023	X	00001FC8	16	1494	1505
V1024	X	00002070	16	1531	1542
V1025	X	00002118	16	1568	1579
V1026	X	000021C0	16	1606	1617
V1027	X	00002268	16	1643	1654
V1028	X	00002310	16	1680	1691
V1029	X	000023B8	16	1717	1728
V103	X	000012A8	16	748	759
V1030	X	00002460	16	1754	1765
V1031	X	00002508	16	1791	1802
V1032	X	000025B0	16	1828	1839
V1033	X	00002658	16	1865	1876
V1034	X	00002700	16	1902	1913
V1035	X	000027A8	16	1940	1951
V1036	X	00002850	16	1977	1988
V1037	X	000028F8	16	2014	2025
V1038	X	000029A0	16	2051	2062
V1039	X	00002A48	16	2088	2099
V104	X	00001350	16	786	797
V1040	X	00002AF0	16	2130	2141
V1041	X	00002B98	16	2167	2178
V1042	X	00002C40	16	2204	2215
V1043	X	00002CE8	16	2241	2252
V1044	X	00002D90	16	2278	2289
V1045	X	00002E38	16	2315	2326
V1046	X	00002EE0	16	2352	2363
V1047	X	00002F88	16	2389	2400
V1048	X	00003030	16	2426	2437
V1049	X	000030D8	16	2463	2474
V105	X	000013F8	16	823	834
V1050	X	00003180	16	2500	2511
V1051	X	00003228	16	2537	2548
V1052	X	000032D0	16	2574	2585
V1053	X	00003378	16	2611	2622
V1054	X	00003420	16	2650	2661
V1055	X	000034C8	16	2687	2698
V1056	X	00003570	16	2724	2735
V1057	X	00003618	16	2761	2772
V1058	X	000036C0	16	2798	2809
V1059	X	00003768	16	2835	2846
V106	X	000014A0	16	860	871

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1O60	X	00003810	16	2872	2883
V1O61	X	000038B8	16	2910	2921
V1O62	X	00003960	16	2947	2958
V1O63	X	00003A08	16	2984	2995
V1O64	X	00003AB0	16	3021	3032
V1O65	X	00003B58	16	3062	3073
V1O66	X	00003C00	16	3099	3110
V1O67	X	00003CA8	16	3136	3147
V1O68	X	00003D50	16	3173	3184
V1O69	X	00003DF8	16	3210	3221
V1O7	X	00001548	16	898	909
V1O70	X	00003EA0	16	3247	3258
V1O71	X	00003F48	16	3285	3296
V1O72	X	00003FF0	16	3322	3333
V1O73	X	00004098	16	3359	3370
V1O74	X	00004140	16	3396	3407
V1O75	X	000041E8	16	3436	3447
V1O8	X	000015F0	16	935	946
V1O9	X	00001698	16	972	983
V1OUTPUT	X	00000040	16	527	225
V2	U	00000002	1	3573	
V20	U	00000014	1	3591	
V21	U	00000015	1	3592	679 682 685 716 719 722 753 756 759 791 794 797 828 831 834 865 868 871 903 906 909 940 943 946 977 980 983 1018 1021 1024 1055 1058 1061 1092 1095 1098 1129 1132 1135 1166 1169 1172 1203 1206 1209 1240 1243 1246 1277 1280 1283 1314 1317 1320 1351 1354 1357 1388 1391 1394 1425 1428 1431 1462 1465 1468 1499 1502 1505 1536 1539 1542 1573 1576 1579 1611 1614 1617 1648 1651 1654 1685 1688 1691 1722 1725 1728 1759 1762 1765 1796 1799 1802 1833 1836 1839 1870 1873 1876 1907 1910 1913 1945 1948 1951 1982 1985 1988 2019 2022 2025 2056 2059 2062 2093 2096 2099 2135 2138 2141 2172 2175 2178 2209 2212 2215 2246 2249 2252 2283 2286 2289 2320 2323 2326 2357 2360 2363 2394 2397 2400 2431 2434 2437 2468 2471 2474 2505 2508 2511 2542 2545 2548 2579 2582 2585 2616 2619 2622 2655 2658 2661 2692 2695 2698 2729 2732 2735 2766 2769 2772 2803 2806 2809 2840 2843 2846 2877 2880 2883 2915 2918 2921 2952 2955 2958 2989 2992 2995 3026 3029 3032 3067 3070 3073 3104 3107 3110 3141 3144 3147 3178 3181 3184 3215 3218 3221 3252 3255 3258 3290 3293 3296 3327 3330 3333 3364 3367 3370 3401 3404 3407 3441 3444 3447
V22	U	00000016	1	3593	215 681 682 718 719 755 756 793 794 830 831 867 868 905 906 942 943 979 980 1020 1021 1057 1058 1094 1095 1131 1132 1168 1169 1205 1206 1242 1243 1279 1280 1316 1317 1353 1354 1390 1391 1427 1428 1464 1465 1501 1502 1538 1539 1575 1576 1613 1614 1650 1651 1687 1688 1724 1725 1761 1762 1798 1799 1835 1836 1872 1873 1909 1910 1947 1948 1984 1985 2021 2022 2058 2059 2095 2096 2137 2138 2174 2175 2211 2212 2248 2249 2285 2286 2322 2323 2359 2360 2396 2397 2433 2434 2470 2471 2507 2508 2544 2545 2581 2582 2618 2619 2657 2658 2694 2695 2731 2732 2768 2769 2805 2806 2842 2843 2879 2880 2917 2918 2954 2955 2991 2992 3028 3029 3069 3070 3106 3107 3143 3144 3180 3181 3217 3218 3254 3255 3292 3293 3329 3330 3366 3367 3403 3404 3443 3444
V23	U	00000017	1	3594	
V24	U	00000018	1	3595	
V25	U	00000019	1	3596	
V26	U	0000001A	1	3597	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V27	U	0000001B	1	3598	
V28	U	0000001C	1	3599	
V29	U	0000001D	1	3600	
V2ADDR	A	00000024	4	522	680 717 754 792 829 866 904 941 978 1019 1056 1093 1130 1167 1204 1241 1278 1315 1352 1389 1426 1463 1500 1537 1574 1612 1649 1686 1723 1760 1797 1834 1871 1908 1946 1983 2020 2057 2094 2136 2173 2210 2247 2284 2321 2358 2395 2432 2469 2506 2543 2580 2617 2656 2693 2730 2767 2804 2841 2878 2916 2953 2990 3027 3068 3105 3142 3179 3216 3253 3291 3328 3365 3402 3442
V3	U	00000003	1	3574	
V30	U	0000001E	1	3601	
V31	U	0000001F	1	3602	
V3ADDR	A	00000028	4	523	
V4	U	00000004	1	3575	
V5	U	00000005	1	3576	
V6	U	00000006	1	3577	
V7	U	00000007	1	3578	
V8	U	00000008	1	3579	
V9	U	00000009	1	3580	
X0001	U	000002A8	1	183	171 184
X1	F	00001170	4	677	658
X10	F	00001758	4	1016	997
X11	F	00001800	4	1053	1034
X12	F	000018A8	4	1090	1071
X13	F	00001950	4	1127	1108
X14	F	000019F8	4	1164	1145
X15	F	00001AA0	4	1201	1182
X16	F	00001B48	4	1238	1219
X17	F	00001BF0	4	1275	1256
X18	F	00001C98	4	1312	1293
X19	F	00001D40	4	1349	1330
X2	F	00001218	4	714	695
X20	F	00001DE8	4	1386	1367
X21	F	00001E90	4	1423	1404
X22	F	00001F38	4	1460	1441
X23	F	00001FE0	4	1497	1478
X24	F	00002088	4	1534	1515
X25	F	00002130	4	1571	1552
X26	F	000021D8	4	1609	1590
X27	F	00002280	4	1646	1627
X28	F	00002328	4	1683	1664
X29	F	000023D0	4	1720	1701
X3	F	000012C0	4	751	732
X30	F	00002478	4	1757	1738
X31	F	00002520	4	1794	1775
X32	F	000025C8	4	1831	1812
X33	F	00002670	4	1868	1849
X34	F	00002718	4	1905	1886
X35	F	000027C0	4	1943	1924
X36	F	00002868	4	1980	1961
X37	F	00002910	4	2017	1998
X38	F	000029B8	4	2054	2035
X39	F	00002A60	4	2091	2072
X4	F	00001368	4	789	770
X40	F	00002B08	4	2133	2114
X41	F	00002BB0	4	2170	2151

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X42	F	00002C58	4	2207	2188
X43	F	00002D00	4	2244	2225
X44	F	00002DA8	4	2281	2262
X45	F	00002E50	4	2318	2299
X46	F	00002EF8	4	2355	2336
X47	F	00002FA0	4	2392	2373
X48	F	00003048	4	2429	2410
X49	F	000030F0	4	2466	2447
X5	F	00001410	4	826	807
X50	F	00003198	4	2503	2484
X51	F	00003240	4	2540	2521
X52	F	000032E8	4	2577	2558
X53	F	00003390	4	2614	2595
X54	F	00003438	4	2653	2634
X55	F	000034E0	4	2690	2671
X56	F	00003588	4	2727	2708
X57	F	00003630	4	2764	2745
X58	F	000036D8	4	2801	2782
X59	F	00003780	4	2838	2819
X6	F	000014B8	4	863	844
X60	F	00003828	4	2875	2856
X61	F	000038D0	4	2913	2894
X62	F	00003978	4	2950	2931
X63	F	00003A20	4	2987	2968
X64	F	00003AC8	4	3024	3005
X65	F	00003B70	4	3065	3046
X66	F	00003C18	4	3102	3083
X67	F	00003CC0	4	3139	3120
X68	F	00003D68	4	3176	3157
X69	F	00003E10	4	3213	3194
X7	F	00001560	4	901	882
X70	F	00003EB8	4	3250	3231
X71	F	00003F60	4	3288	3269
X72	F	00004008	4	3325	3306
X73	F	000040B0	4	3362	3343
X74	F	00004158	4	3399	3380
X75	F	00004200	4	3439	3420
X8	F	00001608	4	938	919
X9	F	000016B0	4	975	956
XC0001	U	000002D0	1	197	189
ZVE7TST	J	00000000	17296	110	113 115 119 123 444 111
=A(E7TESTS)	A	0000056C	4	421	203
=AL2(L'MSGMSG)	R	0000057A	2	425	370
=D'1'	D	00000560	8	419	241
=F'1'	F	00000574	4	423	279 321
=F'64'	F	00000568	4	420	188
=H'0'	H	00000578	2	424	365
=XL4'3'	X	00000570	4	422	248

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 MACRO    DEFN   REFERENCES

FCHECK     63    170
PTTABLE   611   3462
VRR_A     546    655    692    729    767    804    841    879    916    953    994   1031   1068   1105   1142   1179   1216   1253
               1290   1327   1364   1401   1438   1475   1512   1549   1587   1624   1661   1698   1735   1772   1809   1846   1883
               1921   1958   1995   2032   2069   2111   2148   2185   2222   2259   2296   2333   2370   2407   2444   2481   2518
               2555   2592   2631   2668   2705   2742   2779   2816   2853   2891   2928   2965   3002   3043   3080   3117   3154
               3191   3228   3266   3303   3340   3377   3417
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   DESC      SYMBOL    SIZE      POS         ADDR

Entry: 0

Image       IMAGE     17296   0000-438F   0000-438F
  Region                17296   0000-438F   0000-438F
    CSECT   ZVE7TST   17296   0000-438F   0000-438F
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   STMT                         FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e7-08-VISTR.asm

** NO ERRORS FOUND **
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