SMA Ver.	0. 7. 0 zvector- e7-	- 23- VLREP		03 Apr 2025 15: 41: 04 Page
LOC	OBJECT CODE	ADDR1	ADDR2	STMI
				2 ********************
				3 *
				4 * Zvector E7 instruction tests for VRX encoded: 5 *
				6 * E705 VLREP - Vector Load and Replicate
				7 * 8 * James Wekel March 2025
				9 *******************
				11 *********************
				12 * 13 * basic instruction tests
				14 *
				15 ************************************
				17 * Vector Load and Replicate instruction.
				18 * Exceptions are not tested. 19 *
				20 * NOTE: As VLREP is missing, this test uses the Extended Mnemonics:
				21 * VREPLB, VREPLH, VLŘEPF, VLREPG
				22 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				24 * obvious coding errors. None of the tests are thorough. They are
				25 * NOT designed to test all aspects of any of the instructions. 26 *
				27 *********************
				28 * 29 * *Testcase zvector-e7-23-VLREP
				30 * *
				31 * * Zvector E7 instruction tests for VRX encoded: 32 * *
				33 * * E705 VLREP - Vector Load and Replicate
				34 * * 35 * * #
				36 * * # This tests only the basic function of the instructions.
				37 * * # Exceptions are NOT tested. 38 * * #
				39 * *
				40 * mainsize 2
				41 * numcpu 1 42 * sysclear
				43 * archl vl z/Arch
				44 * 45 * loadcore "\$(testpath)/zvector-e7-23-VLREP.core" 0x0
				46 *
				47 * diag8cmd enable # (needed for messages to Hercules console) 48 * runtest 5
				49 * diag8cmd disable # (reset back to default)
				50 * 51 * *Done
				52 *
				53 ********************

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				55 ****	******	***************
				56 *		K Macro - Is a Facility Bit set?
				57 * 58 *	If th	e facility bit is NOT set, an message is issued and
				59 *	the t	est is skipped.
				60 * 61 *	Fchec	k uses R0, R1 and R2
				62 * 63 * eg.	ЕСИЕС	K 134, 'vector-packed-decimal'
				64 *****	*******	***************
				65 66	MACRO ECHEC	K &BITNO, &NOTSETMSG
				67 .*	TOILLO	&BITNO: facility bit number to check
				68 . * 69	LCLA	&NOTSETMSG: 'facility name' &FBBYTE Facility bit in Byte
				70		&FBBIT Facility bit within Byte
				71 72	LCLA	&L(8)
				73 &L(1) 74		128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				75 &FBBY		&BITNO/8
				76 &FBBI 77 .*	T SETA MNOTE	&L((&BITNO-(&FBBYTE*8))+1) 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				78		
				79 80 *	В	X&SYSNDX Fcheck data area
				81 *	WCMDW DC	ski p messgae
				82 SK1&S 83	SYSNDX DC DC	C' Skipping tests: ' C&NOTSETMSG
				84	DC	C' (bit &BITNO) is not installed.'
				86 *		*-SKT&SYSNDX facility bits
				87 88 FB&SY	DS ZNDY DS	FD gap 4FD
				89	DS	FD gap
				90 * 91 X&SYS	SNDX EQU *	
				92	LÅ	RO, ((X&SYSNDX-FB&SYSNDX)/8)-1
				93 94	STFLE	FB&SYSNDX get facility bits
				95	XGR	RO, RO DO EDECYCNDY SEPRIFE Got Shit byto
				96 97	IC N	RO, FB&SYSNDX+&FBBYTE get fbit byte RO, =F' &FBBIT' is bit set?
				98 99 *	BNZ	XC&SYSNDX
				100 * fac	cility bit	not set, issue message and exit
				101 * 102	LA	
				103	LA	R1, SKT&SYSNDX message address
				104 105	BAL	R2, MSG
				106	В	ЕОЈ
				107 XC&SY 108	SNDX EQU MEND	*
				100	1783111	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI				
				110 ******* 111 * 112 *****		ore PSWs	**************************************	
00000000		00000000 00000000	000016FB	113 ZVE7TST 114	START		Low core addressability	
		00000140	00000000	115 116 SVOLDPSV	W EQU	ZVE7TST+X' 140'	z/Arch Supervisor call old PSW	
0000000 000001A0 000001A8	00000001 80000000 00000000 00000200	00000000	000001A0	118 119 120	ORG DC DC	ZVE7TST+X' 1A0' X' 000000018000000 AD(BEGIN)	z/Architecure RESTART PSW	
000001A0	0000000 00000200			120	ьс	AD(DEGIN)		
000001B0 000001D0 000001D8	00020001 80000000 00000000 0000DEAD	000001B0	000001D0	122 123 124	ORG DC DC	ZVE7TST+X' 1D0' X' 000200018000000 AD(X' DEAD')	z/Architecure PROGRAM CHECK PSW 00'	
000001E0		000001E0	00000200	126	ORG	ZVE7TST+X' 200'	Start of actual test program	
				128 ******* 129 * 130 ******	****** ****	**************************************	**************************************	
				133 * Regis	tectur ster Us	e Mode: z/Arch age:		
				134 * 135 * RO 136 * R1-4		work) work)		
				137 * R5 138 * R6-R 139 * R8	R7 (esting control tal work) irst base registeı	ole - current test base	
				140 * R9 141 * R10 142 * R11	S T	econd base registe hird base registe 7TEST call return	er	
				143 * R12 144 * R13	E (7TESTS register work)		
				145 * R14 146 * R15 147 * 148 ******	S	ubroutine call econdary Subroutiı *******	ne call or work	
00000200 00000200		00000200 00001200		150 151	USI NG USI NG	BEGIN, R8 BEGIN+4096, R9	FIRST Base Register SECOND Base Register	
00000200		00002200		152		BEGIN+8192, R10	THIRD Base Register	
00000202				154 BEGIN 155 156	BALR BCTR BCTR	R8 , 0	Initalize FIRST base register Initalize FIRST base register Initalize FIRST base register	
	4190 8800 4190 9800		00000800 0000800	158 159 160	LA LA	R9, 2048(, R8) R9, 2048(, R9)	Initalize SECOND base register Initalize SECOND base register	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				229 ******* 230 * result 231 *	not a	s expected:	**************************************	
				232 * 233 ******		and instructio	est number, instruction under test n m3 **************	
0000030A	45F0 812C	0000030A	00000001 0000032C	234 FAILMSG 235	EQU BAL	* R15, RPTERROR		
				~0.	ue aft	er a failed tes	**************************************	
0000030E	5800 829C	0000030E	00000001 0000049C	240 FAILCONT 241	EQU L	* RO , = F ' 1'	set failed test indicator	
00000312 00000316	5000 8E00 41C0 C004		00001000 0000004	242 243 244	ST LA	RO, FAILED R12, 4(0, R12)	next test address	
0000031A	47F0 80D4		000002D4	245	В	NEXTE7		
				248 * end of 249 ******	***** testi *****	**************************************	**************************************	
0000031E 00000322	5810 8E00 1211	0000031E	00000001 00001000	250 ENDTEST 251 252	EQU L LTR	* R1, FAILED R1, R1	did a test fail?	
00000324 00000328	4780 8270 47F0 8288		00000470 00000488	253 254	BZ B	EOJ FAI LTEST	No, exit Yes, exit with BAD PSW	

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LOC	OBJECT CODE	ADDR1	ADDR2	STM			
				295 ******** 296 * 297 * 298 ******		HERCULES MESSAGE poin R2 = return address	**************************************
000003A8 000003AC	4900 82A0 07D2		000004A0	300 MSG 301	CH BNHR	RO, =H' O' R2	Do we even HAVE a message? No, ignore
000003AE	9002 81E4		000003E4	303	STM	RO, R2, MSGSAVE	Save registers
000003B2 000003B6 000003BA	4900 82A2 47D0 81BE 4100 005F		000004A2 000003BE 0000005F	305 306 307	CH BNH LA	RO, =AL2(L' MSGMSG) MSGOK RO, L' MSGMSG	Message length within limits? Yes, continue No, set to maximum
000003BE 000003C0 000003C2	1820 0620 4420 81F0		000003F0	309 MSGOK 310 311	LR BCTR EX	R2, R0 R2, 0 R2, MSGMVC	Copy length to work register Minus-1 for execute Copy message to O/P buffer
000003C6 000003CA	4120 200A 4110 81F6		0000000A 000003F6	313 314	LA LA	R2, 1+L' MSGCMD(, R2) R1, MSGCMD	Calculate true command length Point to true command
000003CE 000003D2	83120008 4780 81DE		000003DE	316 317	DC BZ	X' 83', X' 12', X' 0008' MSGRET	Issue Hercules Diagnose X'008' Return if successful
000003D6 000003D8	1222 4780 81DE		000003DE	318 319 320	LTR BZ	R2, R2 MSGRET	Is Diag8 Ry (R2) 0? an error occurred but coninue
000003DC	0000			321 322	DC	Н' О'	CRASH for debugging purposes
000003DE 000003E2	9802 81E4 07F2		000003E4	324 MSGRET 325	LM BR	RO, R2, MSGSAVE R2	Restore registers Return to caller
000003E4	0000000 00000000			327 MSGSAVE		3F' 0'	Registers save area
000003F0	D200 81FF 1000	000003FF	0000000	328 MSGMVC	MVC	MSGMSG(0), O(R1)	Executed instruction
000003F6 000003FF	D4E2C7D5 D6C8405C 40404040 40404040			330 MSGCMD 331 MSGMSG 332	DC DC	C' MSGNOH * ' CL95' '	*** HERCULES MESSAGE COMMAND *** The message text to be displayed

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LOC	OBJECT CODE	ADDR1	ADDR2	STM					
				334 335 336	****** * ******	****** Norma *****	**************************************	**************************************	
00000460	00020001 80000000			338	EOJPSW	DC	OD' O' , X' 000200	018000000', AD(0)	
00000470	B2B2 8260		00000460	340	EOJ	LPSWE	EOJPSW	Normal completion	
00000478	00020001 80000000			342	FAI LPSW	DC	OD' O' , X' 000200	018000000', AD(X'BAD')	
00000488	B2B2 8278		00000478	344	FAI LTEST	LPSWE	FAILPSW	Abnormal termination	
				346 347 348	***** * *****	****** Worki : *****	**************************************	************	
	00000000 0000000			350 351	CTLRO	DS DS	F F	CRO	
00000494				353		LTORG		Literals pool	
00000494 00000498 0000049C	00000040 000016BC 00000001			354 355 356		LIONG	=F' 64' =A(E7TESTS) =F' 1'	Li ceruis poor	
000004A0 000004A2	0000 005F			357 358 359			=H' 0' =AL2(L' MSGMSG)		
		00000	000000	360 361			constants		
		00000400 00001000 00010000 00100000	00000001 00000001 00000001 00000001	364 365	PAGE K64	EQU EQU EQU EQU	1024 (4*K) (64*K) (K*K)	One KB Size of one page 64 KB 1 MB	
		AABBCCDD 000000DD	00000001 00000001	366 367	REG2PATT REG2LOW	EQU	X' AABBCCDD' X' DD'	Polluted Register pattern (last byte above)	

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LOC	OBJECT CODE	ADDR1	ADDR2	STM			
				412 *	E7TEST DSECT	**************************************	
00000000 00000004 00000006 00000007 000000010 00000014 00000018 0000001C 00000020 00000028 00000038	00000000 000 00 40404040 40404040 00000000			415 E7TEST 416 TSUB 417 TNUM 418 419 MB 420 421 OPNAME 422 V2ADDR 423 V3ADDR 424 RELEN 425 READDR 426 427 V10UTPUT 428 429 430 * 431 * 432 *	DS FD	pointer to test Test Number m3 used E7 name address of v2 source address of v3 source RESULT LENGTH result (expected) address gap V1 Output gap be here (from VRX macro)	
000010B4		00000000	000016FВ	433 * 435 ZVE7TST 436	EXPECTED RES CSECT , DS OF	ULT	
				439 * Ma	cros to help build	**************************************	
				444 * 445 446	to generate individ MACRO VRX &INST, &MB		
				447 . * 448 . * 449 450 451 &TNUM 452	GBLA &TNUM SETA &TNUM+1	&INST - VRX instruction under test &m3 - m3 field	
				453 454 455 456 T&TNUM 457 458	DS OFD USING *, R5 DC A(X&TNUM) DC H' &TNUM' DC X' 00'	base for test data and test routine address of test routine test number	
				459 460 461	DC HL1' &MB' DC CL8' &I NST' DC A(RE&TNUM+16	m3 instruction name address of v2 source	

LOC	OBJECT CODE	ADDR1	ADDR2	STMI				Page	1
oc .	ODSECT CODE	ADDKI	ADDIC		D.C	A (DEOTNIM, OO)	- dd		
				462 463	DC DC	A(RE&TNUM+32) A(16)	address of v3 source result length		
				464 REA&TNUM 465	DC DS	A(RE&TNUM)	result length result address		
				466 V10&TNUM	DS DS	FD XL16	gap V1 output		
				467 468 . *	DS	FD	gap		
				469 *					
				470 X&TNUM 471	DS VL	OF v22, V1FUDGE	fudgo v29		
				471 472	LGF	R1, V2ADDR	fudge v22 load source address		
				473 474	ot NCT		test instruction		
				475	&I NSI	νωω, υ(υ, κ 1) (test Thstruction		
				476 477	VST BR	V22, V10&TNUM R11	save v1 output return		
				478					
				479 RE&TNUM 480	DC	0F	xl16 expected result		
				481	DROP	R5			
				482	MEND				
				484 *					
				485 * macro	to gene	erate table of p	oointers to individual tests		
				486 * 487	MACRO				
				488	PTTAB]	LE			
				489 490	GBLA LCLA	&TNUM &CUR			
				491 &CUR	SETA				
				492 .* 493 TTABLE	DS	OF			
				494 . LOOP	ANOP	V 2			
				495 . * 496	DC	A(T&CUR)			
				497 . *					
				498 &CUR 499	SETA AI F	&CUR+1 (&CUR LE &TNUM)	. LOOP		
				500 *					
				501 502	DC DC	A(0) A(0)	END OF TABLE		
				503 . *		(0)			
				504	MEND				

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				506 ******	*****	******	***********	
				507 * 508 ******		X tests	***********	
				509	PRINT			
				510	WIDED	V4 II	. J. D 12 4 -	
				511 * E705 512 *	VLKEP	- Vector Load ar	id Replicate	
				513 *	VRX i	nstruction, m3		
				514 * 515 *		followed by	ted result (V1)	
				516 *		16 byte source		
				517 * 518 *				
				519 * VLRE	P - V	ector Load and Rep		
				520 * 521 *Byte				
				522		VLREPB, O		
000010B8		000010B8		523+	DS USING	OFD	has for test data and test wenting	
000010B8 000010B8	000010F8	00001088		524+ 525+T1	DC DC	*, K5 A(X1)	base for test data and test routine address of test routine	
000010BC	0001			526 +	DC	H' 1'	test number	
000010BE 000010BF	00 00			527+ 528+	DC DC	X' 00' HL1' 0'	m3	
000010C0	E5D3D9C5 D7C24040			529 +	DC	CL8' VLREPB'	instruction name	
000010C8 000010CC	00001124 00001134			530+ 531+	DC DC	A(RE1+16) A(RE1+32)	address of v2 source address of v3 source	
000010D0	0000010			532+	DC	A(16)	result length	
	00001114 00000000 00000000			533+REA1 534+	DC DS	A(RE1) FD	result address	
000010E0	0000000 00000000			535+V101	DS	XL16	gap V1 output	
	00000000 00000000 0000000 00000000			536+	DS	FD	(an	
00001010	0000000 0000000			537+*			gap	
000010F8 000010F8	E760 8E94 0806		00001094	538+X1 539+	DS VL	OF v22, V1FUDGE	fudge v22	
000010F8	E310 5010 0014		00001094	540+	LGF	R1, V2ADDR	load source address	
	E760 1000 0805		0000000	541 +			st instruction	
0000110A 00001110	E760 5028 080E 07FB		000010E0	542+ 543+	VST BR	V22, V101 R11	save v1 output return	
00001114				544+RE1	DC	OF	xl16 expected result	
00001114 00001114	FFFFFFF FFFFFFF			545+ 546	DROP DC	R5 XL16' FFFFFFFFFFF	FFFFF FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	
0000111C	FFFFFFFF FFFFFFFF							
	FFFFFFF FFFFFFF 01020304 05060708			547	DC	XL16' FFFFFFFFFFF	FFFFF 0102030405060708' source	
	00000100			548	*****	III DEDE		
00001138				549 550+	VRX DS	VLREPB, O OFD		
00001138	0000115	00001138		551 +	USING	*, R 5	base for test data and test routine	
00001138 0000113C	00001178 0002			552+T2 553+	DC DC	A(X2) H' 2'	address of test routine test number	
0000113E	00			554 +	DC	X' 00'		
0000113F 00001140	00 E5D3D9C5 D7C24040			555+ 556+	DC DC	HL1' 0' CL8' VLREPB'	m3 instruction name	
00001148	000011A4			557 +	DC	A(RE2+16)	address of v2 source	
0000114C	000011B4			558 +	DC	A(RE2+32)	address of v3 source	

1000 150	ASMA Ver.	0. 7. 0 zvector- e7- 2	23- VLREP					03 Apr 2025	15: 41: 04	Page	15
00001154 0000100000 00000000 00000000 00000000	LOC	OBJECT CODE	ADDR1	ADDR2	STMI						
00001160 00000000 00000000 00000000 000000	00001154	00001194			560+REA2	DC	A(RE2)	result address			
10001178 178	00001160 00001168	00000000 00000000 0000000 00000000			562+V102	DS	XL16				
00001178 E760 8E94 0866 00014 00000010 566+ VL VL VL VL VL VL VL V		0000000 00000000			564 +*			gap			
00001190 07FB 570+REZ DC 07	0000117E 00001184	E310 5010 0014 E760 1000 0805		00000010 00000000	567+ 568+	VL LGF VLREP	R1, V2ADDR B V22, O(0, R1) test	load source address t instruction			
00001194 01010101 01010101 01010101 01010101	00001190 00001194			00001160	570+ 571+RE2	BR DC	R11 0F	return			
00001184	00001194 0000119C	01010101 01010101			573	DC	XL16' 0101010101010		resul t		
00001188						DC	XL16' 0102030405060	0708 090A0B0C0D0E0F00'	source		
000011B8 000011F8 0003			00001180		576 577+	DS	OFD	have for took data and d			
000011BF 00	000011B8 000011BC	0003	00001188		579+T3 580+	DC DC	A(X3) H' 3'	address of test routine	test routi	ne	
000011D0	000011BF 000011C0	00 E5D3D9C5 D7C24040			582+ 583+	DC DC	HL1' O' CL8' VLREPB'	instruction name			
000011E8	000011D0	0000010			586 +	DC DC	A(16)	result length			
591+* 592+X3 DS OF	000011E0 000011E8	00000000 00000000 0000000 00000000			589+V103	DS	XL16	gap V1 output			
000011F8		00000000 00000000			591 +*			gap			
00001214	000011F8 000011FE 00001204	E310 5010 0014 E760 1000 0805		00000010 00000000	593+ 594+ 595+	VL LGF VLREP	v22, V1FUDGE R1, V2ADDR B V22, O(0, R1) test	load source address			
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	00001210 00001214			000011E0	597+ 598+RE3	BR DC	R11 OF	return			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	00001214 0000121C	FEFEFEFE FEFEFEFE			600	DC	XL16' FEFEFEFEFEFE		resul t		
$\begin{array}{cccccccccccccccccccccccccccccccccccc$					602		XL16' FEFDFCFBFAF9	F8F7 090A0B0C0D0E0F00'	source		
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	00001238				604	VRX					
	$00001238 \\ 00001238$		00001238		606+ 607+T4	USI NG DC	*, R5 A(X4)	address of test routine	test routi	ne	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI						
0000123E	00			609+		X' 00'	0			
0000123F	O1			610+			m3			
$00001240 \\ 00001248$	E5D3D9C5 D7C84040 000012A4			611+ 612+		CL8' VLREPH' A(RE4+16)	instruction name address of v2 source			
00001248 0000124C	000012A4 000012B4			613+		A(RE4+10) A(RE4+32)	address of v2 source			
00001240	00000010			614+			result length			
00001254	00001294			615+REA4		A(RE4)	result address			
00001258	0000000 00000000			616 +						
00001260	0000000 00000000			617+V104	DS	XL16	gap V1 output			
00001268	00000000 00000000									
00001270	0000000 00000000			618+	DS	FD	gap			
00001970				619+* 620+X4	DC	OF				
00001278 00001278	E760 8E94 0806		00001094	621+			fudge v22			
00001278 0000127E	E310 5010 0014		00001034	622+		R1, V2ADDR	load source address			
00001272	E760 1000 1805		00000000	623+			instruction			
0000128A	E760 5028 080E		00001260	624+		, , ,	save v1 output			
00001290	07FB			625 +	BR	R11	return			
00001294				626+RE4	DC		xl16 expected result			
00001294				627+		R5		.		
00001294	FFAAFFAA FFAAFFAA			628	DC	XL16' FFAAFFAAFFAA	FFAA FFAAFFAAFFAA'	resul t		
	FFAAFFAA FFAAFFAA FFAAFFFF FFFFFFF			629	DC	VI 16' EEAAEEEEEEE	FFFF 0102030405060708'	COUMOO		
	01020304 05060708			029	DС	ALIO FFAAFFFFFFF	FFF 0102030403000708	source		
000012AC	01020304 03000708			630						
				631	VRX	VLREPH, 1				
000012B8				632+	DS	OFD				
000012B8		000012B8		633+	USING		base for test data and t	test routin	ıe	
000012B8	000012F8			634+T5		A(X5)	address of test routine			
000012BC	0005			635+			test number			
000012BE 000012BF	00 01			636+ 637+	DC DC	X' 00' HL1' 1'	m3			
000012BF 000012C0	E5D3D9C5 D7C84040			638+	DC	CL8' VLREPH'	instruction name			
000012C8	00001324			639+		A(RE5+16)	address of v2 source			
000012CC	00001334			640 +			address of v3 source			
000012D0	0000010			641+			result length			
000012D4	00001314			642+REA5		A(RE5)	result address			
000012D8	00000000 00000000			643+		FD	gap			
000012E0	00000000 00000000			644+V105	DS	XL16	Ĭ1 output			
000012E8 000012F0	0000000 0000000 0000000 0000000			645+	DS	FD	dan			
UUUU12FU				646+*	טע	I'V	gap			
000012F8				647+X5	DS	0F				
000012F8	E760 8E94 0806		00001094	648+			fudge v22			
000012FE	E310 5010 0014		0000010	649+	LGF	R1, V2ADDR	load source address			
00001304	E760 1000 1805		00000000	650+			instruction			
0000130A	E760 5028 080E		000012E0	651+			save v1 output			
00001310	07FB			652+ 653+RE5			return			
00001314 00001314				654+		OF R5	xl16 expected result			
	01020102 01020102			655			0102 0102010201020102'	resul t		
	01020102 01020102			000	D 0	ALLO CIUMUIUMUIUM	,ion didmolondidmolon	I Court		
	01020304 05060708			656	DC	XL16' 0102030405060	0708 090A0B0C0D0E0F00'	source		
	O9OAOBOC ODOEOFOO									
				657	****	THE DEDUCTION OF				
				658	VRX	VLREPH, 1				

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
001338				659 +	DS	OFD		
001338		00001338		660+	USING		base for test data and test routine	
001338	00001378			661+T6	DC	A(X6)	address of test routine	
00133C	0006			662+	DC	H' 6'	test number	
00133E	00			663+	DC	X' 00'		
)0133F	01			664+	DC	HL1' 1'	m3	
001340	E5D3D9C5 D7C84040			665+	DC	CL8' VLREPH'	instruction name	
01348	000013A4			666+	DC	A(RE6+16)	address of v2 source	
00134C	000013B4			667+	DC	A(RE6+32)	address of v3 source	
001350	00000010			668+	DC	A(16)	result length	
01354	00001394			669+REA6	DC	A(RE6)	result address	
001358	0000000 00000000			670+	DS	FD	gap V1 output	
001360	00000000 00000000			671+V106	DS	XL16	V1 output	
001368	00000000 00000000			070	D.C	TID		
001370	0000000 00000000			672+	DS	FD	gap	
001070				673+*	D.C.	OF		
001378	E700 0E04 0000		00001004	674+X6	DS	OF	£	
001378	E760 8E94 0806		00001094	675+	VL	v22, V1FUDGE	fudge v22	
00137E	E310 5010 0014		00000010	676+	LGF	R1, V2ADDR	load source address	
001384	E760 1000 1805		0000000	677+		H V22, 0(0, R1)	test instruction	
00138A	E760 5028 080E 07FB		00001360	678+ 679+	VST	V22, V106	save v1 output	
001390	U/FD			680+RE6	BR DC	R11 OF	return	
001394				681+	DROP	R5	xl16 expected result	
001394 001394	07FD07FD 07FD07FD			682	DROP DC		07FD07FD 07FD07FD07FD0 result	
01394 00139C	07FD07FD 07FD07FD			002	DC	ALIO U/FDU/FD	orruotru otruotruotruotru tesuit	
00139C 0013A4	07FDFCFB FAF9F8F7			683	DC	VI 16! OTENECED	FAF9F8F7 090A0B0C0D0E0F00' source	
013A4 0013AC	090A0B0C OD0E0F00			003	DC	ALIO U/FDFCFB	SFAF9F8F7 090A0B0C0D0E0F00' source	
JUIJAC	OSOAOBOC ODOLOFOO			684				
				685 *Word				
				686	VRX	VLREPF, 2		
0013B8				687+	DS	OFD		
0013B8		000013B8		688+	USING		base for test data and test routine	
0013B8	000013F8	00001010		689+T7	DC	A(X7)	address of test routine	
0013BC	0007			690+	DC	H' 7'	test number	
0013BE	00			691+	DC	X' 00'	0000 11411001	
0013BF	02			692+	DC	HL1' 2'	m3	
0013C0	E5D3D9C5 D7C64040			693+	DC	CL8' VLREPF'	instruction name	
0013C8	00001424			694+	DC	A(RE7+16)	address of v2 source	
0013CC	00001434			695 +	DC	A(RE7+32)	address of v3 source	
0013D0	0000010			696 +	DC	A(16)	result length	
0013D4	00001414			697+REA7	DC	A(RE7)	result address	
0013D8	0000000 00000000			698 +	DS	FD	gap	
0013E0	0000000 00000000			699+V107	DS	XL16	Ĭ1 output	
)013E8	0000000 00000000			~~~				
013F0	0000000 00000000			700+	DS	FD	gap	
04050				701+*	D.C			
013F8	Eggo OFO4 OCCO		00001001	702+X7	DS	OF	C 1	
013F8	E760 8E94 0806		00001094	703+	VL	v22, V1FUDGE	fudge v22	
0013FE	E310 5010 0014		00000010	704+	LGF	R1, V2ADDR	load source address	
001404	E760 1000 2805		0000000	705+		F V22, 0(0, R1)		
0140A	E760 5028 080E		000013E0	706+	VST	V22, V107	save v1 output	
01410	07FB			707+	BR	R11	return	
001414				708+RE7	DC	OF	xl16 expected result	
001414	01020304 01020304			709+ 710	DROP DC	R5	01020304 0102030401020304' result	
				/ 111			TOUR TOUR TOUR TOUR TOUR TOUR TOUR TOUR	

ASMA Ver.	0. 7. 0 zvector- e7- 2	23- VLREP					03 Apr 2025	15: 41: 04	Page	18
LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00001424	01020304 01020304 01020304 05060708 090A0B0C 0D0E0F00			711	DC	XL16' 010203040506	0708 090A0B0C0D0E0F00'	source		
00001420	OSOAOBOC ODOEOFOO			712 713	VRX	VLREPF, 2				
00001438				714+	DS	OFD				
00001438 00001438	00001478	00001438		715+ 716+T8	USI NG DC	*, R5 A(X8)	base for test data and taddress of test routine	test routi	ne	
0000143C	0008			717+	DC	Н' 8'	test number			
0000143E 0000143F	00 02			718+ 719+	DC DC	X' 00' HL1' 2'	m3			
00001440	E5D3D9C5 D7C64040			720 +	DC	CL8' VLREPF'	instruction name			
00001448 0000144C	000014A4 000014B4			721+ 722+	DC DC	A(RE8+16) A(RE8+32)	address of v2 source address of v3 source			
00001450	0000010			723+	DC	A(16)	result length			
00001454 00001458	00001494 00000000 00000000			724+REA8 725+	DC DS	A(RE8) FD	result address			
00001460	00000000 00000000			726+V108	DS	XL16	gap V1 output			
	00000000 00000000 0000000 00000000			727+	DS	FD	gap			
				728+*			9I			
00001478 00001478	E760 8E94 0806		00001094	729+X8 730+	DS VL	OF v22, V1FUDGE	fudge v22			
0000147E	E310 5010 0014		0000010	731+	LGF	R1, V2ADDR	load source address			
	E760 1000 2805 E760 5028 080E		0000000 00001460	732+ 733+	VLKEPI VST	F V22, 0(0, R1) test V22, V108	t instruction save v1 output			
00001490	07FB			734+	BR	R11	return			
00001494 00001494				735+RE8 736+	DC DROP	0F R5	xl16 expected result			
	F9F8F704 F9F8F704 F9F8F704			737	DC	XL16' F9F8F704F9F8	F704 F9F8F704F9F8F704'	resul t		
000014A4	F9F8F704 05060708			738	DC	XL16' F9F8F7040506	0708 FFFFFFFFFFFFFF	source		
000014AC	FFFFFFF FFFFFFF			739						
				740	VRX	VLREPF, 2				
000014B8 000014B8		000014B8		741+ 742+	DS USING	OFD * R5	base for test data and t	est routi	ne	
000014B8	000014F8	000014100		743+T9	DC	A(X9)	address of test routine	test Touth		
000014BC 000014BE	0009 00			744+ 745+	DC DC	H' 9' X' 00'	test number			
000014BF	02			746 +	DC	HL1' 2'	m3			
000014C0 000014C8	E5D3D9C5 D7C64040 00001524			747+ 748+	DC DC	CL8' VLREPF' A(RE9+16)	instruction name address of v2 source			
000014CC	00001534			749 +	DC	A(RE9+32)	address of v3 source			
000014D0 000014D4	00000010 00001514			750+ 751+REA9	DC DC	A(16) A(RE9)	result length result address			
000014D8	00000000 00000000			752 +	DS	FD	gap V1 output			
000014E0 000014E8	00000000 00000000 0000000 00000000			753+V109	DS	XL16	vi output			
000014F0	00000000 00000000			754+	DS	FD	gap			
000014F8				755+* 756+ X 9	DS	0F				
000014F8	E760 8E94 0806		00001094	757 +	VL	v22, V1FUDGE	fudge v22			
000014FE 00001504	E310 5010 0014 E760 1000 2805		00000010 00000000	758+ 759+	LGF VLREPI	R1, V2ADDR F V22, O(0, R1) test	load source address t instruction			
	E760 5028 080E		000014E0	760 +	VST	V22, V109	save v1 output			

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI						
00001510 00001514	07FB			761+ 762+RE9	BR DC	R11 OF	return xl16 expected result			
00001514 00001514 0000151C	08080807 08080807 08080807 08080807			763+ 764	DROP DC	R5 XL16' 0808080708080	0807 0808080708080807'	resul t		
00001524 0000152C	08080807 080807F7 FEFDFCFB FAF9F8F7			765 766	DC	XL16' 0808080708080	07F7 FEFDFCFBFAF9F8F7'	source		
				767 *Doublew	ord					
				768	VRX	VLREPG, 3				
00001538				769+	DS	OFD				
00001538	00001570	00001538		770+	USING		base for test data and		1e	
00001538 0000153C	00001578 000A			771+T10 772+	DC DC	A(X10) H' 10'	address of test routine test number			
0000153E	000A 00			772+ 773+	DC	X' 00'	test number			
0000153E	03			77 4 +	DC	HL1'3'	m3			
00001540	E5D3D9C5 D7C74040			775+	DC	CL8' VLREPG'	instruction name			
00001548	000015A4			776+	DC	A(RE10+16)	address of v2 source			
0000154C	000015B4			777+	DC	A(RE10+32)	address of v3 source			
00001550	0000010			778+	DC	A(16)	result length			
$00001554 \\ 00001558$	00001594 00000000 00000000			779+REA10 780+	DC DS	A(RE10) FD	result address			
00001558	0000000 0000000			780+ 781+V1010	DS DS	XL16	gap V1 output			
00001568	0000000 00000000			701111010	DO	ALIO	VI oucput			
00001570	00000000 00000000			782+ 783+*	DS		gap			
00001578	T700 0T04 0000		00001001	784+X10	DS	OF	0.1			
00001578 0000157E	E760 8E94 0806 E310 5010 0014		00001094 00000010	785+ 786+	VL LGF	v22, V1FUDGE R1, V2ADDR	fudge v22 load source address			
0000157E	E760 1000 3805		00000010	787+		•	instruction			
0000158A	E760 5028 080E		00001560	788 +	VST	V22, V1010	save v1 output			
00001590	07FB		00001000	789+	BR	R11	return			
00001594				790+RE10	DC	0F	xl16 expected result			
00001594				791+		R 5	_	_		
	FFFFFFF FFFF09AA			792	DC	XL16' FFFFFFFFFFF	9AA FFFFFFFFFF09AA'	resul t		
000015A4	FFFFFFF FFFF09AA FFFFFFFF FFFF09AA 01020304 05060708			793	DC	XL16' FFFFFFFFFFF	09AA 0102030405060708'	source		
000015B8				794 795 796+	VRX DS	VLREPG, 3 OFD				
000013B8		000015B8		797+	USING		base for test data and	test routir	1e	
000015B8	000015F8	JUU 1010		798+T11	DC	A(X11)	address of test routine			
000015BC	000B			799+	DC	H'11'	test number			
000015BE	00			800+	DC	X' 00'	•			
000015BF	03			801+	DC DC	HL1'3'	m3			
000015C0 000015C8	E5D3D9C5 D7C74040			802+ 803+	DC	CL8' VLREPG'	instruction name address of v2 source			
000015C8 000015CC	00001624 00001634			804+	DC DC	A(RE11+16) A(RE11+32)	address of v2 source address of v3 source			
000015CC	00001034			805+	DC DC	A(16)	result length			
000015D4	00001614			806+REA11	DC	A(RE11)	result address			
000015D8	0000000 00000000			807 +	DS					
000015E0	00000000 00000000			808+V1011	DS	XL16	gap V1 output			
000015E8 000015F0	00000000 00000000 00000000 00000000			809+ 810+*	DS	FD	gap			
				0101						

	U. 7. U ZVECCOI -	e7-23-VLREP					03 Apr 202	25 15: 41: 04	Page
LOC	OBJECT CODE	ADDR1	ADDR2	STMI					
0015F8				811+X11	DS	0F			
0015F8	E760 8E94 0806		00001094	812+	VL	v22, V1FUDGE	fudge v22		
0015FE	E310 5010 0014		00000010	813+	LGF	R1, V2ADDR	load source address		
001604	E760 1000 3805		0000000	814+			est instruction		
00160A 001610	E760 5028 080E 07FB		000015E0	815+ 816+	VST BR	V22, V1011 R11	save v1 output return		
001614	U/FD			817+RE11	DC DC	OF	xl16 expected result		
001614				818+	DROP	R5	ATTO EXPECTEU TESUTE		
001614	AABB1122 050607	08		819	DC		060708 AABB112205060708'	resul t	
00161C	AABB1122 050607	08							
001624	AABB1122 050607			820	DC	XL16' AABB112205	060708 090A0B0C0D0E0F00'	source	
00162C	O9OAOBOC ODOEOF	00		004					
				821 822	WDW	VI DEDC O			
001638				823+	VRX DS	VLREPG, 3 OFD			
001638		00001638		824+	USI NG		base for test data and	l test routin	ıe.
001638	00001678	33331333		825+T12	DC	A(X12)	address of test routin		-
00163C	000C			826+	DC	H' 12'	test number		
00163E	00			827+	DC	X' 00'			
00163F	03			828+	DC	HL1'3'	m3		
001640	E5D3D9C5 D7C740	40		829+	DC DC	CL8' VLREPG'	instruction name		
001648 00164C	000016A4 000016B4			830+ 831+	DC DC	A(RE12+16) A(RE12+32)	address of v2 source address of v3 source		
00164C 001650	000010B4			832+	DC	A(16)	result length		
001654	00001694			833+REA12	DC	A(RE12)	result address		
001658	0000000 000000	00		834+	DS	FD	gap		
001660	0000000 000000			835+V1012	DS	XL16	V1 output		
001668	00000000 000000			000	D.C.	TIP			
001670	00000000 000000	00		836+ 837+*	DS	FD	gap		
001678				838+X12	DS	0F			
001678	E760 8E94 0806		00001094	839+	VL	v22, V1FUDGE	fudge v22		
	E310 5010 0014		00000010	840+	ĹĠF	R1, V2ADDR	load source address		
	E760 1000 3805		0000000	841+		3 V22, 0(0, R1) to	est instruction		
	E760 5028 080E		00001660	842+		V22, V1012	save v1 output		
001690	07FB			843+	BR	R11	return		
001694				844+RE12	DC DROP	OF R5	xl16 expected result		
001694	FEFDFCFB FAF9F8	01		845+ 846			F9F801 FEFDFCFBFAF9F801	resul t	
	FEFDFCFB FAF9F8			UTU	ь	ALIU ILIDICIDIA	I OI OUT TELDI OF DIAF OF OUT	I CSuI C	
	FEFDFCFB FAF9F8			847	DC	XL16' FEFDFCFBFA	F9F801 090A0B0C0D0E0F00'	source	
	090A0B0C 0D0E0F								
				848					
001GP4	0000000			849 850	DC	F' O' END OF	TARIF		
	0000000			851		F' 0'	IADLE		
~~IODO				852 *	D 0	- 0			
				853 * table	of poir	nters to individ	ual load test		
				854 *	-				
0016BC				855 E7TESTS		OF			
0010BC				856	PTTABI				
0016BC	000010B8			857+TTABLE 858+	DS DC	0F A(T1)			
በበ1ይወር	WWWINDA			0J0+	DС	A(II)			
					DC	A(T2)			
0016C0	00001138 000011B8			859+ 860+	DC DC	A(T2) A(T3)			

000016D0 00001338 863+ DC A(T6) 000016D4 000013B8 864+ DC A(T7) 000016D8 00001438 865+ DC A(T8) 000016D0 000014B8 866+ DC A(T9) 000016E0 00001538 867+ DC A(T11) 000016E2 00001638 869+ DC A(T12) 870+* 870+* 000016F0 0000000 871+ DC A(0) END OF TABLE 000016F4 00000000 872+ DC A(0) 873 000016F4 00000000 874 DC F' 0' END OF TABLE	ASMA Ver.	0. 7. 0 zvector- e7-	23- VLREP					03 Apr 2	2025 15: 41: 04	Page	21
000016D4 000013B8 864+ DC A(T7) 000016D8 00001438 865+ DC A(T8) 000016DC 000014B8 866+ DC A(T9) 000016E0 00001538 867+ DC A(T10) 000016E4 000015B8 868+ DC A(T11) 000016E8 00001638 869+ DC A(T12) 870+* 000016F0 00000000 871+ DC A(0) END OF TABLE 000016F0 00000000 872+ DC A(0) 873 000016F4 00000000 874 DC F' 0' END OF TABLE	LOC	OBJECT CODE	ADDR1	ADDR2	STM						
870+* 000016EC 00000000 871+ DC A(0) END OF TABLE 000016F0 00000000 872+ DC A(0) 873 000016F4 00000000 874 DC F' 0' END OF TABLE	000016CC 000016D0 000016D4 000016D8 000016DC 000016E0 000016E4	00001338 000013B8 00001438 000014B8 00001538			863+ 864+ 865+ 866+ 867+	DC DC DC DC	A(T6) A(T7) A(T8) A(T9) A(T10)				
000016F4 00000000 874 DC F'O' END OF TABLE	000016E8 000016EC 000016F0	0000000			870+* 871+ 872+		A(T12) A(0)	END OF TABLE			
	000016F4 000016F8				874			END OF TABLE			

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI								
		00000016	00000001	924 V22	EQU	22						
		00000017 00000018	00000001 00000001	925 V23 926 V24	EQU EQU	23 24						
		00000019 0000001A	00000001 00000001	927 V25 928 V26	EQU FOU	25 26						
		0000001B	0000001	929 V27	EQU EQU EQU EQU EQU EQU EQU EQU EQU	22 23 24 25 26 27 28 29 30 31						
		0000001C 0000001D	00000001 00000001	930 V28 931 V29	EQU EQU	28 29						
		0000001E 0000001F	$00000001 \\ 00000001$	932 V30 933 V31	EQU EQU	30 31						
		0000011	0000001	934		O1						
				935	END							

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TROW F 0000048C	EGI N	I	00000200	2	154	120	150	151	152												
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0.1 1 00000470		X		18			273														
0.1PSW D 00000460 8 338 340 AILCONT U 00000305 1 240 4 378 242 251 AILCONT U 00000305 1 240 4 378 242 251 AILCONT U 00000305 1 240 4 378 242 251 AILCONT U 00000305 1 240 4 378 242 251 AILCONT U 00000305 1 240 240 4 378 242 251 AILCONT U 00000305 1 240 240 240 240 240 240 240 240 240 240		U		1																	
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ALIANG U 0000030A ALIALESW D 00000478 8 342 344 ALITEST I 00000488 8 183 187 188 190 19001 F 00000280 8 183 187 188 190 19001 F 00000280 8 183 187 188 190 190 10000000 1 344 24 ALIALESW D 00000000 1 344 24 B U 00000000 1 344 25 B U 00000000 1 344 25 B U 00000000 1 345 26 SG U 00000376 9 330 313 314 SGCMD C 0000386 9 330 313 314 SGCMD C 0000386 9 330 313 314 SGCMC I 00000376 9 330 313 314 SGCMC I 00000376 9 330 313 314 SGCMC I 00000386 9 348 316 SGCMC I 00000386 9 348 316 SGCMC I 00000386 9 348 317 SGCMC I 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 00000386 1 000000386 1 00000386 1 000000386 1 000000386 1 000000386 1 000000386 1 000000386 1 000000386 1 00000000 1 00000000 1 00000000 1 00000000		F		4		242	251														
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B U 000000000 1 1 4419 271 B U 001000000 1 1 365 GG I 00000384 4 300 198 283 GGMC C 000003F6 95 331 307 328 305 GGMC I 000003F6 95 331 307 328 305 GGMC I 000003F6 95 331 307 328 305 GGMC I 000003F0 6 328 311 GGMC I 000003F0 8 321 GGMC I 000003F0 8 421 GGMC I 000003F0 8 421 GGMC I 000003F0 8 421 GGMC I 0000004 1 208 227 245 F 000003F0 1 363 RT3 C 00001050 18 399 265 266 267 273 274 275 RT1AME C 00001088 16 384 391 285 RT1AKG U 0000005F 1 381 399 275 RT1AME C 00001044 2 389 275 RT1AME C 00001044 2 389 275 RT1AME C 00001018 3 8357 269 RT1AME C 00001018 3 8357 269 RT1AME C 00001018 3 8357 269 RT1AME C 00001018 3 835 267 RT1AME C 00001018 1 881 114 164 167 187 189 190 191 196 215 216 241 242 280 281 284 I U 0000000 1 881 197 222 223 251 252 282 314 328 540 541 567 568 594 595 622 RT1AME C 00001018 3 835 267 RT1AME C 00001018 3 835 267 RT1AME C 0000000 1 881 197 222 223 251 252 282 314 328 540 541 567 568 594 595 622 RT1AME C 00001018 3 835 267 RT1AME C 0000000 1 881 152 161 162 RT1AME C 0000000 1 881 152 161 162 RT1AME C 0000000 1 881 152 161 162 RT1AME C 0000000 1 883 260 209 226 244 I U 0000000 1 883 265 266 267 704 705 731 732 758 759 786 787 813 814 I U 0000000 1 883 291 292 292 293 543 570 597 625 652 679 707 734 761 789 816 843 I U 0000000 1 883 292 292 292 543 570 597 625 652 679 707 734 761 789 816 843 I U 0000000 1 883 293 265 266 267 278 288 I U 0000000 1 883 293 265 266 267 278 288 I U 0000000 1 885 287 I 885 299 210 213 261 286 524 545 551 572 578 599 606 627 633 654 I 886 299 210 213 261 286 524 545 551 572 578 599 606 627 633 654 I 886 299 210 213 261 286 524 545 551 572 578 599 606 627 633 654 I U 00000000 1 885 287 I RT1AME C C C C C C C C C		U	00010000	1																	
BE		U	0000007	1		271															
SGCM I 000003R6 4 300 198 283	В			1																	
SGCMB C C 000003FF 95 331 314 314 SGCMSG C C 000003FF 95 331 307 328 305 SGMS I 000003FF 95 331 307 328 305 SGMS I 000003FG 6 328 311 SGMS I 000003FG 2 309 306 SGGK I 000003FG 4 324 317 320 SGGK I 000003FG 4 327 303 324 SCMSW F 000003FG 4 327 303 324 SCMSW F 0000003FG 4 327 303 324 SCMSW F 0000003FG 4 327 303 324 SCMSW F 0000003FG 1 363 SCMSW F 00000005 1 8 39 SCMSW F 00000005 1 8 SCMSW F 00000000 1 8 SCMSW		Ť		4		198	283														
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SGRET J 000003BE 4 324 317 320 8 SGSAVE F 000003E4 4 327 303 324 EXTE7 U 000002P4 1 208 227 245 PNAME C 00000008 8 421 269 PNAME C 00001000 1 363 RT3 C 0000105D 18 399 265 266 267 273 274 275 RTILNE C 0000108B 16 334 391 282 RTLING U 000003F 1 391 281 RTMB C 00001044 2 389 275 RTNAME C 00001044 2 389 275 RTNAME C 00001018 3 385 267 0 U 00000001 1 881 114 164 167 187 189 190 191 196 215 216 241 242 280 281 284 RTNUM C 00001018 3 385 267 0 U 00000000 1 881 114 164 167 187 189 190 191 196 215 216 241 242 280 281 284 1 U 0000000 1 882 197 222 223 251 252 282 314 328 540 541 567 568 594 595 622		Ţ																			
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PNAME C 00000008	BGSAVE	F	000003E4	4	327	303	324														
PNAME C 00000008	EXTE7	U	000002D4	1	208	227	245														
AGE RT3 C 00001000 1 363 RTI. RT3 C 0000105D 18 399 265 266 267 273 274 275 RTI. RTLINE C 00001008 16 384 391 282 RTI. RTLNG U 0000003F 1 391 281 RTI. RTMB C 00001044 2 2 389 275 RTNAME C 00001018 3 385 267 267 267 267 267 267 267 267 267 267		Ċ		8																	
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1	PRTNUM	C	00001018	3	385	267															
1	20			1			164	167	187	189	190	191	196	215	216	241	242	280	281	284	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		•		_										~-0	~-0		~ -~	~~~	~~-	~~-	
10	21	II	00000001	1	882							314	328	540	541	567	568	594	595	622	
840 841 10 U 0000000A 1 891 152 161 162 11 U 0000000B 1 892 219 220 543 570 597 625 652 679 707 734 761 789 816 843 12 U 0000000C 1 893 206 209 226 244 13 U 0000000B 1 894 14 U 0000000E 1 895 15 U 0000000F 1 896 235 260 287 288 2 U 00000002 1 883 198 263 264 271 272 280 283 284 301 303 309 310 311 313 319 3 U 00000003 1 884 4 U 00000004 1 885 5 U 00000005 1 886 209 210 213 261 286 524 545 551 572 578 599 606 627 633 654 6 U 00000007 1 888	r I	U	0000001	1	862																
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13		U		1						597	625	652	679	707	734	761	789	816	843		
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14 U 00000000E 1 895 15 U 0000000F 1 896 235 260 287 288 2 U 00000002 1 883 198 263 264 271 272 280 283 284 301 303 309 310 311 313 319 3 U 00000003 1 884 84 84 85 885 </td <td></td> <td>U</td> <td></td> <td>1</td> <td></td>		U		1																	
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324 325 3		_		1						979	280	283	991	201	303	300	210	211	212	210	
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8	8			1	889	150	154	155	150	150											

SMA Ver. 0.7.0		- e7- 23- VLRE								оо пр	1 202	5 15: 41: 04	Page	2
SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFE	RENCE	S							
29	U	00000009	1	890	151	158	159	161						
E1	F	00001114	$\overline{4}$	544	530	531	533							
E10	F	00001594	$ar{4}$	790	776	777	779							
E11	$ar{\mathbf{F}}$	00001614	$ar{4}$	817	803	804	806							
E12	$ar{\mathbf{F}}$	00001694	$ar{4}$	844	830	831	833							
EE2	F	00001194	4	571	557	558	560							
EE3	F	00001214	4	598	584	585	587							
EE4	F	00001294	4	626	612	613	615							
EE5	F	00001314	4	653	639	640	642							
EE6	${f F}$	00001394	4	680	666	667	669							
RE7	${f F}$	00001414	4	708	694	695	697							
EE8	F	00001494	4	735	721	722	724							
EE9	F	00001514	4	762	748	749	751							
EEA1	A	000010D4	4	533										
EEA10	A	00001554	4	779										
EA11	A	000015D4	4	806										
EA12	A	00001654	4	833										
EA2	A	00001154	4	560										
EEA3	A	000011D4	4	587										
EA4	A	00001254	4	615										
EA5	A	000012D4	4	642										
EA6	A	00001354	4	669										
EA7	A	000013D4	4	697										
EA8	A	00001454	4	724										
EA9	A	000014D4	4	751										
EADDR	A	0000001C	4	425	222									
EG2LOW	Ü	000000DD	1	368										
EG2PATT	Ų	AABBCCDD	1	367										
ELEN	A	00000018	4	424	000	004								
PTDWSAV	D	00000398	8	293	280	284								
RPTERROR	Ī	0000032C	4	260	235	007								
PTSAVE	F	00000390	4	290	260	287								
PTSVR5	F	00000394	4	291	261	286								
SKL0001	U	0000004E	1	180	196	107								
SKT0001	C	0000022A	20	177	180	197								
SVOLDPSW	U	00000140	0	116	050									
`1 '10	A	000010B8	4	525 771	858 867									
110	A	00001538	4	771	867									
`11 `12	A A	000015B8 00001638	4	798 825	868 869									
12 2	A A	00001038	4	552	859									
	A A	00001138 000011B8	4	579	860									
.3 [4	A A	00001188	4	607	861									
.4 .5	A A	00001238 000012B8	4	634	862									
.5 [6	A A	00001288	4	661	863									
7	A	00001338 000013B8	4	689	864									
. 7 . 8	A	000013B8	4	716	865									
'9	A	00001438 000014B8	4	743	866									
ESTI NG	F	00001413	4	379	216									
NUM	H	00001004	2	417	215	263								
SUB	A	00000004	4	416	219	~00								
TABLE	F	000016BC	4	857	~10									
0	ĪJ	00001020	1	902										
1	Ü	00000001	1	903	218									
10	Ŭ	00000001 0000000A	1	912	~10									
10														

		VALUE	LENGTH	DEFN	KEILE	RENCE	.													
12	U	000000C	1	914																
13	Ü	0000000C	1	915																
14	Ŭ	0000000E	1	916																
15	Ŭ	000000E	1	917																
16	Ŭ	00000010	1	918																
17	Ü	00000011	1	919																
18	Ū	00000012	$\bar{1}$	920																
19	U	0000013	1	921																
1FUDGE	X	00001094	16	408	218	539	566	593	621	648	675	703	730	757	785	812	839			
101	X	000010E0	16	535	542															
1010	X	00001560	16	781	788															
1011	X	000015E0	16	808	815															
1012	X	00001660	16	835	842															
102	X	00001160	16	562	569															
103	X	000011E0	16	589	596															
104	X	00001260	16	617	624															
105	X	000012E0	16	644	651															
106	X	00001360	16	671	678															
107	X	000013E0	16	699	706															
108 109	X X	00001460 000014E0	16 16	726 753	733 760															
109 10UTPUT	X	000014E0	16	427	223															
2	Ŭ	00000028	10	904	223															
20	Ü	0000002	1	922																
21	Ü	00000014	1	923																
22	Ŭ	00000016	1	924	539	541	542	566	568	569	593	595	596	621	623	624	648	650	651	
~~	· ·	0000010	•	021	675	677	678	703	705	706	730	732	733	757	759	760	785	787	788	
					812	814	815	839	841	842										
23	U	0000017	1	925																
24	U	0000018	1	926																
25	U	00000019	1	927																
26	U	000001A	1	928																
27	U	000001B	1	929																
28	U	000001C	1	930																
29	U	0000001D	1	931																
2ADDR	A	00000010	4	422	540	567	594	622	649	676	704	731	758	786	813	840				
3	U	00000003	1	905																
30	U	0000001E	1	932																
31	Ų	0000001F	1	933																
3ADDR	A	00000014	4	423																
4 5	U	00000004	1	906 907																
6	U	00000005 00000006	1	908																
0 7	U II	00000000	1	909																
8	II	00000007	1	910																
9	Ĭ	00000009	1	911																
0001	Ŭ	0000003 000002A8	1	186	174	187														
1	F	000010F8	4	538	525	10.														
10	F	00001578	4	784	771															
11	F	000015F8	4	811	798															
12	F	00001678	4	838	825															
2	$ar{\mathbf{F}}$	00001178	$\overline{4}$	565	552															
3	F	000011F8	$\bar{4}$	592	579															
4	F	00001278	4	620	607															
5		000012F8	4	647	634															

SYMBOL	ТҮРЕ	VALUE	LENGTH	DEFN	DEEE	RENCE	r c						
						aven C E	<u>ی</u> ن						
	F F F	000013F8 00001478	4 4	702 729	716								
0001	F U	000014F8 000002D0	4 1	756 200	743 192								
E7TST (E7TESTS)	J A	00000000 00000498	5884 4	113	116	118	122	126	377	114			
L2(L' MSGMSG) 1'	R	000004A2	2 4	358	206 305								
64'	F F	0000049C 00000494	4 4 2	356 354	241 191 300								
0'	Н	000004A0	2	357	300								



