LOC	OBJECT CODE	ADDR1	ADDR2	STMT

```
  2 ****************************************************************************
  3 *
  4 *    Zvector E7 instruction tests for VRR-c encoded:
  5 *
  6 *    E770 VESLV  - Vector Element Shift Left Vector
  7 *    E778 VESRLV - Vector Element Shift Right Logical Vector
  8 *    E77A VESRAV - Vector Element Shift Right Arithmetic Vector
  9 *
 10 *        James Wekel April 2025
 11 ****************************************************************************

 13 ****************************************************************************
 14 *
 15 *        basic instruction tests
 16 *
 17 ****************************************************************************
 18 *   This program tests proper functioning of the z/arch E7 VRR-c vector
 19 *   element shift left, shift right logical, shitft right arithmetic
 20 *   instructions where the shift is a vector element.
 21 *
 22 *   Exceptions are not tested.
 23 *
 24 *   PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
 25 *   obvious coding errors.  None of the tests are thorough.  They are
 26 *   NOT designed to test all aspects of any of the instructions.
 27 *
 28 ****************************************************************************
 29 *
 30 *    *Testcase zzvector-e7-28-ShiftVector
 31 *    *
 32 *    *   Zvector E7 instruction tests for VRR-c encoded:
 33 *    *
 34 *    *   E770 VESLV  - Vector Element Shift Left Vector
 35 *    *   E778 VESRLV - Vector Element Shift Right Logical Vector
 36 *    *   E77A VESRAV - Vector Element Shift Right Arithmetic Vector
 37 *    *
 38 *    *   # ------------------------------------------------------------
 39 *    *   #  This tests only the basic function of the instructions.
 40 *    *   #  Exceptions are NOT tested.
 41 *    *   # ------------------------------------------------------------
 42 *    *
 43 *    mainsize    2
 44 *    numcpu      1
 45 *    sysclear
 46 *    archlvl     z/Arch
 47 *
 48 *    loadcore    "$(testpath)/zvector-e7-28-ShiftVector.core" 0x0
 49 *
 50 *    diag8cmd    enable    # (needed for messages to Hercules console)
 51 *    runtest     5
 52 *    diag8cmd    disable   # (reset back to default)
 53 *
 54 *    *Done
 55 *
 56 ****************************************************************************
```

```
      LOC           OBJECT CODE      ADDR1     ADDR2     STMT

                                                         58 *****************************************************************************
                                                         59 *         FCHECK Macro - Is a Facility Bit set?
                                                         60 *
                                                         61 *         If the facility bit is NOT set, an message is issued and
                                                         62 *         the test is skipped.
                                                         63 *
                                                         64 *         Fcheck uses R0, R1 and R2
                                                         65 *
                                                         66 * eg.     FCHECK 134,'vector-packed-decimal'
                                                         67 *****************************************************************************
                                                         68         MACRO
                                                         69         FCHECK &BITNO,&NOTSETMSG
                                                         70 .*                        &BITNO : facility bit number to check
                                                         71 .*                        &NOTSETMSG : 'facility name'
                                                         72         LCLA  &FBBYTE        Facility bit in Byte
                                                         73         LCLA  &FBBIT         Facility bit within Byte
                                                         74
                                                         75         LCLA  &L(8)
                                                         76 &L(1)   SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                         77
                                                         78 &FBBYTE SETA  &BITNO/8
                                                         79 &FBBIT  SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                         80 .*            MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                         81
                                                         82         B     X&SYSNDX
                                                         83 *                                    Fcheck data area
                                                         84 *                                    skip messgae
                                                         85 SKT&SYSNDX DC  C'    Skipping tests: '
                                                         86         DC    C&NOTSETMSG
                                                         87         DC    C' (bit &BITNO) is not installed.'
                                                         88 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                         89 *                                    facility bits
                                                         90         DS    FD               gap
                                                         91 FB&SYSNDX DS  4FD
                                                         92         DS    FD               gap
                                                         93 *
                                                         94 X&SYSNDX EQU *
                                                         95         LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                         96         STFLE FB&SYSNDX           get facility bits
                                                         97
                                                         98         XGR   R0,R0
                                                         99         IC    R0,FB&SYSNDX+&FBBYTE   get fbit byte
                                                        100         N     R0,=F'&FBBIT'          is bit set?
                                                        101         BNZ   XC&SYSNDX
                                                        102 *
                                                        103 * facility bit not set, issue message and exit
                                                        104 *
                                                        105         LA    R0,SKL&SYSNDX          message length
                                                        106         LA    R1,SKT&SYSNDX          message address
                                                        107         BAL   R2,MSG
                                                        108
                                                        109         B     EOJ
                                                        110 XC&SYSNDX EQU *
                                                        111         MEND
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				113	**			
				114	*	Low core PSWs		
				115	**			
		00000000	00003D4B	116	ZVE7TST	START 0		
00000000		00000000		117		USING ZVE7TST,R0		Low core addressability
				118				
		00000140	00000000	119	SVOLDPSW	EQU	ZVE7TST+X'140'	z/Arch Supervisor call old PSW
00000000		00000000	000001A0	121		ORG	ZVE7TST+X'1A0'	z/Architecure RESTART PSW
000001A0	00000001 80000000			122		DC	X'0000000180000000'	
000001A8	00000000 00000200			123		DC	AD(BEGIN)	
000001B0		000001B0	000001D0	125		ORG	ZVE7TST+X'1D0'	z/Architecure PROGRAM CHECK PSW
000001D0	00020001 80000000			126		DC	X'0002000180000000'	
000001D8	00000000 0000DEAD			127		DC	AD(X'DEAD')	
000001E0		000001E0	00000200	129		ORG	ZVE7TST+X'200'	Start of actual test program..
				131	**			
				132	*	The actual "ZVE7TST" program itself...		
				133	**			
				134	*			
				135	*	Architecture Mode: z/Arch		
				136	*	Register Usage:		
				137	*			
				138	*	R0	(work)	
				139	*	R1-4	(work)	
				140	*	R5	Testing control table - current test base	
				141	*	R6-R7	(work)	
				142	*	R8	First base register	
				143	*	R9	Second base register	
				144	*	R10	Third base register	
				145	*	R11	E7TEST call return	
				146	*	R12	E7TESTS register	
				147	*	R13	(work)	
				148	*	R14	Subroutine call	
				149	*	R15	Secondary Subroutine call or work	
				150	*			
				151	**			
00000200		00000200		153		USING	BEGIN,R8	FIRST Base Register
00000200		00001200		154		USING	BEGIN+4096,R9	SECOND Base Register
00000200		00002200		155		USING	BEGIN+8192,R10	THIRD Base Register
00000200	0580			157	BEGIN	BALR	R8,0	Initialize FIRST base register
00000202	0680			158		BCTR	R8,0	Initialize FIRST base register
00000204	0680			159		BCTR	R8,0	Initialize FIRST base register
00000206	4190 8800		00000800	161		LA	R9,2048(,R8)	Initialize SECOND base register
0000020A	4190 9800		00000800	162		LA	R9,2048(,R9)	Initialize SECOND base register
				163				

```
  LOC        OBJECT CODE       ADDR1      ADDR2     STMT

0000020E   41A0 9800                    00000800   164              LA     R10,2048(,R9)    Initalize THIRD base register
00000212   41A0 A800                    00000800   165              LA     R10,2048(,R10)   Initalize THIRD base register
                                                   166
00000216   B600 828C                    0000048C   167              STCTL  R0,R0,CTLR0      Store CR0 to enable AFP
0000021A   9604 828D                    0000048D   168              OI     CTLR0+1,X'04'    Turn on AFP bit
0000021E   9602 828D                    0000048D   169              OI     CTLR0+1,X'02'    Turn on Vector bit
00000222   B700 828C                    0000048C   170              LCTL   R0,R0,CTLR0      Reload updated CR0
                                                   171
                                                   172  *********************************************************************
                                                   173  * Is z/Architecture vector facility installed  (bit 129)
                                                   174  *********************************************************************
                                                   175
                                                   176              FCHECK 129,'z/Architecture vector facility'
00000226   47F0 80A8                    000002A8   177+             B      X0001
                                                   178+*                                             Fcheck data area
                                                   179+*                                             skip messgae
0000022A   40404040 E2928997                       180+SKT0001 DC     C'    Skipping tests: '
0000023E   A961C199 838889A3                       181+         DC     C'z/Architecture vector facility'
0000025C   404D8289 A340F1F2                       182+         DC     C' (bit 129) is not installed.'
           0000004E   00000001                     183+SKL0001 EQU    *-SKT0001
                                                   184+*                                             facility bits
00000278   00000000 00000000                       185+         DS     FD                            gap
00000280   00000000 00000000                       186+FB0001  DS     4FD
000002A0   00000000 00000000                       187+         DS     FD                            gap
                                                   188+*
           000002A8   00000001                     189+X0001   EQU    *
000002A8   4100 0004                    00000004   190+         LA     R0,((X0001-FB0001)/8)-1
000002AC   B2B0 8080                    00000280   191+         STFLE  FB0001                        get facility bits
000002B0   B982 0000                               192+         XGR    R0,R0
000002B4   4300 8090                    00000290   193+         IC     R0,FB0001+16                  get fbit byte
000002B8   5400 8294                    00000494   194+         N      R0,=F'64'                     is bit set?
000002BC   4770 80D0                    000002D0   195+         BNZ    XC0001
                                                   196+*
                                                   197+* facility bit not set, issue message and exit
                                                   198+*
000002C0   4100 004E                    0000004E   199+         LA     R0,SKL0001                    message length
000002C4   4110 802A                    0000022A   200+         LA     R1,SKT0001                    message address
000002C8   4520 81A8                    000003A8   201+         BAL    R2,MSG
000002CC   47F0 8270                    00000470   202+         B      EOJ
           000002D0   00000001                     203+XC0001  EQU    *
```

```
  LOC          OBJECT CODE        ADDR1      ADDR2      STMT

                                                        205  ************************************************************************
                                                        206  *           Do tests in the E7TESTS table
                                                        207  ************************************************************************
                                                        208
000002D0   58C0 8298                          00000498  209           L      R12,=A(E7TESTS)      get table of test addresses
                                                        210
                              000002D4        00000001  211 NEXTE7    EQU    *
000002D4   5850 C000                          00000000  212           L      R5,0(0,R12)          get test address
000002D8   1255                                         213           LTR    R5,R5                 have a test?
000002DA   4780 811E                          0000031E  214           BZ     ENDTEST                 done?
                                                        215
000002DE                        00000000                216           USING  E7TEST,R5
                                                        217
000002DE   4800 5004                          00000004  218           LH     R0,TNUM              save current test number
000002E2   5000 8E04                          00001004  219           ST     R0,TESTING           for easy reference
                                                        220
000002E6   E710 8E94 0006                     00001094  221           VL     V1,V1FUDGE
000002EC   58B0 5000                          00000000  222           L      R11,TSUB             get address of test routine
000002F0   05BB                                         223           BALR   R11,R11              do test
                                                        224
000002F2   E310 501C 0014                     0000001C  225           LGF    R1,READDR            get address of expected result
000002F8   D50F 5028 1000      00000028       00000000  226           CLC    V10UTPUT,0(R1)       valid?
000002FE   4770 810A                          0000030A  227           BNE    FAILMSG                no, issue failed message
                                                        228
00000302   41C0 C004                          00000004  229           LA     R12,4(0,R12)         next test address
00000306   47F0 80D4                          000002D4  230           B      NEXTE7
```

```
   LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  232 ****************************************************************************
                                                  233 * result not as expected:
                                                  234 *        issue message with test number, instruction under test
                                                  235 *               and instruction m4
                                                  236 ****************************************************************************
                              0000030A  00000001  237 FAILMSG  EQU     *
0000030A   45F0 812C                     0000032C  238          BAL    R15,RPTERROR


                                                  240 ****************************************************************************
                                                  241 * continue after a failed test
                                                  242 ****************************************************************************
                              0000030E  00000001  243 FAILCONT EQU     *
0000030E   5800 829C                     0000049C  244          L      R0,=F'1'            set failed test indicator
00000312   5000 8E00                     00001000  245          ST     R0,FAILED
                                                  246
00000316   41C0 C004                     00000004  247          LA     R12,4(0,R12)       next test address
0000031A   47F0 80D4                     000002D4  248          B      NEXTE7


                                                  250 ****************************************************************************
                                                  251 * end of testing; set ending psw
                                                  252 ****************************************************************************
                              0000031E  00000001  253 ENDTEST  EQU     *
0000031E   5810 8E00                     00001000  254          L      R1,FAILED          did a test fail?
00000322   1211                                    255          LTR    R1,R1
00000324   4780 8270                     00000470  256          BZ     EOJ                No, exit
00000328   47F0 8288                     00000488  257          B      FAILTEST           Yes, exit with BAD PSW
```

```
  LOC           OBJECT CODE        ADDR1      ADDR2      STMT

                                                        259 ********************************************************************
                                                        260 *         RPTERROR                   Report instruction test in error
                                                        261 ********************************************************************

0000032C   50F0 8190                          00000390  263 RPTERROR ST    R15,RPTSAVE         Save return address
00000330   5050 8194                          00000394  264          ST    R5,RPTSVR5          Save R5
                                                        265 *
00000334   4820 5004                          00000004  266          LH    R2,TNUM             get test number and convert
00000338   4E20 8E73                          00001073  267          CVD   R2,DECNUM
0000033C   D211 8E5D 8E47     0000105D 00001047         268          MVC   PRT3,EDIT
00000342   DE11 8E5D 8E73     0000105D 00001073         269          ED    PRT3,DECNUM
00000348   D202 8E18 8E6A     00001018 0000106A         270          MVC   PRTNUM(3),PRT3+13   fill in message with test #
                                                        271
0000034E   D207 8E33 5008     00001033 00000008         272          MVC   PRTNAME,OPNAME      fill in message with instruction
                                                        273 *
00000354   E320 5007 0076                     00000007  274          LB    R2,m4               get m4 and convert
0000035A   4E20 8E73                          00001073  275          CVD   R2,DECNUM
0000035E   D211 8E5D 8E47     0000105D 00001047         276          MVC   PRT3,EDIT
00000364   DE11 8E5D 8E73     0000105D 00001073         277          ED    PRT3,DECNUM
0000036A   D201 8E44 8E6B     00001044 0000106B         278          MVC   PRTM4(2),PRT3+14    fill in message with m4 field
                                                        279 *
                                                        280 *         Use Hercules Diagnose for Message to console
                                                        281 *
00000370   9002 8198                          00000398  282          STM   R0,R2,RPTDWSAV      save regs used by MSG
00000374   4100 003F                          0000003F  283          LA    R0,PRTLNG           message length
00000378   4110 8E08                          00001008  284          LA    R1,PRTLINE          messagfe address
0000037C   4520 81A8                          000003A8  285          BAL   R2,MSG              call Hercules console MSG display
00000380   9802 8198                          00000398  286          LM    R0,R2,RPTDWSAV      restore regs


00000384   5850 8194                          00000394  288          L     R5,RPTSVR5          Restore R5
00000388   58F0 8190                          00000390  289          L     R15,RPTSAVE         Restore return address
0000038C   07FF                                         290          BR    R15                 Return to caller

00000390   00000000                                     292 RPTSAVE  DC    F'0'                R15 save area
00000394   00000000                                     293 RPTSVR5  DC    F'0'                R5 save area

00000398   00000000 00000000                            295 RPTDWSAV DC    2D'0'               R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

                                                 297 ****************************************************************************
                                                 298 *           Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                 299 *                 R2 = return address
                                                 300 ****************************************************************************

000003A8   4900 82A0                   000004A0  302 MSG       CH    R0,=H'0'              Do we even HAVE a message?
000003AC   07D2                                  303           BNHR  R2                    No, ignore

000003AE   9002 81E4                   000003E4  305           STM   R0,R2,MSGSAVE         Save registers

000003B2   4900 82A2                   000004A2  307           CH    R0,=AL2(L'MSGMSG)     Message length within limits?
000003B6   47D0 81BE                   000003BE  308           BNH   MSGOK                 Yes, continue
000003BA   4100 005F                   0000005F  309           LA    R0,L'MSGMSG           No, set to maximum

000003BE   1820                                  311 MSGOK     LR    R2,R0                 Copy length to work register
000003C0   0620                                  312           BCTR  R2,0                  Minus-1 for execute
000003C2   4420 81F0                   000003F0  313           EX    R2,MSGMVC             Copy message to O/P buffer

000003C6   4120 200A                   0000000A  315           LA    R2,1+L'MSGCMD(,R2)    Calculate true command length
000003CA   4110 81F6                   000003F6  316           LA    R1,MSGCMD             Point to true command

000003CE   83120008                              318           DC    X'83',X'12',X'0008'   Issue Hercules Diagnose X'008'
000003D2   4780 81DE                   000003DE  319           BZ    MSGRET                Return if successful
                                                 320
000003D6   1222                                  321           LTR   R2,R2                 Is Diag8 Ry (R2) 0?
000003D8   4780 81DE                   000003DE  322           BZ    MSGRET                  an error occurred but coninue
                                                 323
000003DC   0000                                  324           DC    H'0'                  CRASH for debugging purposes

000003DE   9802 81E4                   000003E4  326 MSGRET    LM    R0,R2,MSGSAVE         Restore registers
000003E2   07F2                                  327           BR    R2                    Return to caller


000003E4   00000000 00000000                     329 MSGSAVE   DC    3F'0'                 Registers save area
000003F0   D200 81FF 1000   000003FF   00000000  330 MSGMVC    MVC   MSGMSG(0),0(R1)       Executed instruction

000003F6   D4E2C7D5 D6C8405C                      332 MSGCMD    DC    C'MSGNOH * '          *** HERCULES MESSAGE COMMAND ***
000003FF   40404040 40404040                      333 MSGMSG    DC    CL95' '               The message text to be displayed
                                                 334
```

```
  LOC          OBJECT CODE       ADDR1      ADDR2      STMT

                                                       336 ****************************************************************************
                                                       337 *          Normal completion or Abnormal termination PSWs
                                                       338 ****************************************************************************


00000460    00020001 80000000                          340 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000470    B2B2 8260                      00000460     342 EOJ      LPSWE EOJPSW                Normal completion


00000478    00020001 80000000                          344 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

00000488    B2B2 8278                      00000478     346 FAILTEST LPSWE FAILPSW               Abnormal termination



                                                       348 ****************************************************************************
                                                       349 *          Working Storage
                                                       350 ****************************************************************************


0000048C    00000000                                   352 CTLR0    DS    F                     CR0
00000490    00000000                                   353          DS    F

00000494                                               355          LTORG ,                     Literals pool
00000494    00000040                                   356                =F'64'
00000498    00003C18                                   357                =A(E7TESTS)
0000049C    00000001                                   358                =F'1'
000004A0    0000                                       359                =H'0'
000004A2    005F                                       360                =AL2(L'MSGMSG)
                                                       361
                                                       362 *          some constants
                                                       363
                             00000400    00000001      364 K        EQU   1024                  One KB
                             00001000    00000001      365 PAGE     EQU   (4*K)                 Size of one page
                             00010000    00000001      366 K64      EQU   (64*K)                64 KB
                             00100000    00000001      367 MB       EQU   (K*K)                  1 MB
                                                       368
                             AABBCCDD    00000001      369 REG2PATT EQU   X'AABBCCDD'            Polluted Register pattern
                             000000DD    00000001      370 REG2LOW  EQU         X'DD'           (last byte above)
```

```
  LOC         OBJECT CODE      ADDR1      ADDR2     STMT

                                                    372 *===============================================================================
                                                    373 *
                                                    374 *   NOTE: start data on an address that is easy to display
                                                    375 *         within Hercules
                                                    376 *
                                                    377 *===============================================================================
                                                    378
000004A4                       000004A4   00001000  379          ORG    ZVE7TST+X'1000'
00001000   00000000                                 380 FAILED   DC     F'0'                          some test failed?
00001004   00000000                                 381 TESTING  DC     F'0'                          current test number

                                                    383 *
                                                    384 *          failed message and associated editting
                                                    385 *
00001008   40404040 40404040                        386 PRTLINE  DC     C'          Test # '
00001018   A7A7A7                                   387 PRTNUM   DC     C'xxx'
0000101B   40868189 93858440                        388          DC     c' failed for instruction '
00001033   A7A7A7A7 A7A7A7A7                        389 PRTNAME  DC     CL8'xxxxxxxx'
0000103B   40A689A3 884094F4                        390          DC     C' with m4='
00001044   A7A7                                     391 PRTm4    DC     C'xx'
00001046   4B                                       392          DC     C'.'
                               0000003F   00000001  393 PRTLNG   EQU    *-PRTLINE
```

```
  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

                                                    395 *******************************************************************************
                                                    396 *          TEST failed : message working storge
                                                    397 *******************************************************************************
00001047   40212020 20202020                        398 EDIT      DC     XL18'402120202020202020202020202020202020'
                                                    399
00001059   7E7E7E6E                                 400           DC     C' ===>'
0000105D   40404040 40404040                        401 PRT3      DC     CL18' '
0000106F   4C7E7E7E                                 402           DC     C' <==='
00001073   00000000 00000000                        403 DECNUM    DS     CL16


                                                    405 *******************************************************************************
                                                    406 *          Vector instruction results, pollution and input
                                                    407 *******************************************************************************
00001084                                            408           DS     0F
00001084   00000000 00000000                        409           DS     XL16                                       gap
00001094   FFFFFFFF FFFFFFFF                        410 V1FUDGE   DC     XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'       V1 FUDGE
000010A4   00000000 00000000                        411           DS     XL16
```

```
  LOC          OBJECT CODE      ADDR1      ADDR2     STMT

                                                     413 ****************************************************************************
                                                     414 *          E7TEST DSECT
                                                     415 ****************************************************************************

                                                     417 E7TEST    DSECT ,
00000000  00000000                                   418 TSUB      DC    A(0)              pointer  to test
00000004  0000                                       419 TNUM      DC    H'00'             Test Number
00000006  00                                         420           DC    X'00'
00000007  00                                         421 M4        DC    HL1'00'           m4 used
                                                     422
00000008  40404040 40404040                          423 OPNAME    DC    CL8' '            E7 name
00000010  00000000                                   424 V2ADDR    DC    A(0)              address of v2 source
00000014  00000000                                   425 V3ADDR    DC    A(0)              address of  v3 source
00000018  00000000                                   426 RELEN     DC    A(0)              RESULT LENGTH
0000001C  00000000                                   427 READDR    DC    A(0)              result (expected) address
00000020  00000000 00000000                          428           DS    FD                 gap
00000028  00000000 00000000                          429 V1OUTPUT  DS    XL16              V1 Output
00000038  00000000 00000000                          430           DS    FD                 gap
                                                     431
                                                     432 *          test routine will be here (from VRR-c macro)
                                                     433 *
                                                     434 *          followed by
                                                     435 *              EXPECTED RESULT

                          00000000  00003D4B         437 ZVE7TST   CSECT ,
000010B4                                             438           DS    0F

                                                     440 ****************************************************************************
                                                     441 *     Macros to help build test tables
                                                     442 ****************************************************************************

                                                     444 *
                                                     445 * macro to generate individual test
                                                     446 *
                                                     447           MACRO
                                                     448           VRR_C &INST,&M4
                                                     449 .*                                      &INST   - VRR-c instruction under test
                                                     450 .*                                      &m4     - m4 field
                                                     451
                                                     452           GBLA  &TNUM
                                                     453 &TNUM     SETA  &TNUM+1
                                                     454
                                                     455           DS    0FD
                                                     456           USING *,R5               base for test data and test routine
                                                     457
                                                     458 T&TNUM    DC    A(X&TNUM)           address of test routine
                                                     459           DC    H'&TNUM'           test number
                                                     460           DC    X'00'
                                                     461           DC    HL1'&M4'           m4
                                                     462           DC    CL8'&INST'         instruction name
                                                     463           DC    A(RE&TNUM+16)      address of v2 source
```

```
  LOC          OBJECT CODE       ADDR1     ADDR2      STMT

                                                      464              DC      A(RE&TNUM+32)     address of v3 source
                                                      465              DC      A(16)             result length
                                                      466 REA&TNUM DC        A(RE&TNUM)        result address
                                                      467              DS      FD                gap
                                                      468 V10&TNUM DS        XL16              V1 output
                                                      469              DS      FD                gap
                                                      470 .*
                                                      471 *
                                                      472 X&TNUM      DS      0F
                                                      473              LGF     R1,V2ADDR         load v2 source
                                                      474              VL      v22,0(R1)         use v22 to test decoder
                                                      475
                                                      476              LGF     R1,V3ADDR         load v3 source
                                                      477              VL      v23,0(R1)         use v23 to test decoder
                                                      478
                                                      479              &INST V22,V22,V23,&M4       test instruction (dest is a source)
                                                      480
                                                      481              VST     V22,V10&TNUM       save v1 output
                                                      482              BR      R11               return
                                                      483
                                                      484 RE&TNUM     DC      0F                xl16 expected result
                                                      485
                                                      486              DROP    R5
                                                      487              MEND


                                                      489 *
                                                      490 * macro to generate table of pointers to individual tests
                                                      491 *
                                                      492              MACRO
                                                      493              PTTABLE
                                                      494              GBLA    &TNUM
                                                      495              LCLA    &CUR
                                                      496 &CUR        SETA    1
                                                      497 .*
                                                      498 TTABLE      DS      0F
                                                      499 .LOOP       ANOP
                                                      500 .*
                                                      501              DC      A(T&CUR)
                                                      502 .*
                                                      503 &CUR        SETA    &CUR+1
                                                      504              AIF     (&CUR LE &TNUM).LOOP
                                                      505 *
                                                      506              DC      A(0)               END OF TABLE
                                                      507              DC      A(0)
                                                      508 .*
                                                      509              MEND
```

```
  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

                                                   511 ****************************************************************************
                                                   512 *         E7 VRR-c tests
                                                   513 ****************************************************************************
                                                   514         PRINT DATA
                                                   515
                                                   516 *   E770 VESLV  - Vector Element Shift Left Vector
                                                   517 *   E778 VESRLV - Vector Element Shift Right Logical Vector
                                                   518 *   E77A VESRAV - Vector Element Shift Right Arithmetic Vector
                                                   519 *
                                                   520 *         VRR-c instruction, m4
                                                   521 *             followed by
                                                   522 *               16 byte expected result (V1)
                                                   523 *               16 byte V2 source
                                                   524 *               16 byte V3 source
                                                   525 *
                                                   526 *--------------------------------------------------------------------
                                                   527 *   VESLV  - Vector Element Shift Left Vector
                                                   528 *--------------------------------------------------------------------
                                                   529 *Byte
                                                   530         VRR_C VESLV,0
000010B8                                           531+        DS    0FD
000010B8                        000010B8           532+        USING *,R5             base for test data and test routine
000010B8   000010F8                                533+T1      DC    A(X1)            address of test routine
000010BC   0001                                    534+        DC    H'1'             test number
000010BE   00                                      535+        DC    X'00'
000010BF   00                                      536+        DC    HL1'0'           m4
000010C0   E5C5E2D3 E5404040                        537+        DC    CL8'VESLV'       instruction name
000010C8   00001130                                538+        DC    A(RE1+16)        address of v2 source
000010CC   00001140                                539+        DC    A(RE1+32)        address of v3 source
000010D0   00000010                                540+        DC    A(16)            result length
000010D4   00001120                                541+REA1    DC    A(RE1)           result address
000010D8   00000000 00000000                        542+        DS    FD               gap
000010E0   00000000 00000000                        543+V101    DS    XL16             V1 output
000010E8   00000000 00000000
000010F0   00000000 00000000                        544+        DS    FD               gap
                                                   545+*
000010F8                                           546+X1      DS    0F
000010F8   E310 5010 0014            00000010       547+        LGF   R1,V2ADDR        load v2 source
000010FE   E761 0000 0806            00000000       548+        VL    v22,0(R1)        use v22 to test decoder
00001104   E310 5014 0014            00000014       549+        LGF   R1,V3ADDR        load v3 source
0000110A   E771 0000 0806            00000000       550+        VL    v23,0(R1)        use v23 to test decoder
00001110   E766 7000 0E70                           551+        VESLV V22,V22,V23,0     test instruction (dest is a source)
00001116   E760 5028 080E            000010E0       552+        VST   V22,V101         save v1 output
0000111C   07FB                                    553+        BR    R11              return
00001120                                           554+RE1     DC    0F               xl16 expected result
00001120                                           555+        DROP  R5
00001120   01020408 10204080                        556        DC    XL16'0102040810204080 0102040810204080'    result
00001128   01020408 10204080
00001130   01010101 01010101                        557        DC    XL16'0101010101010101 0101010101010101'    v2
00001138   01010101 01010101
00001140   00010203 04050607                        558        DC    XL16'0001020304050607 08090A0B0C0D0E0F'    v3
00001148   08090A0B 0C0D0E0F
                                                   559
                                                   560         VRR_C VESLV,0
00001150                                           561+        DS    0FD
00001150                        00001150           562+        USING *,R5             base for test data and test routine
```

```
   LOC        OBJECT CODE      ADDR1    ADDR2    STMT

00001150  00001190                            563+T2     DC     A(X2)           address of test routine
00001154  0002                              564+       DC     H'2'            test number
00001156  00                                565+       DC     X'00'
00001157  00                                566+       DC     HL1'0'          m4
00001158  E5C5E2D3 E5404040                 567+       DC     CL8'VESLV'      instruction name
00001160  000011C8                          568+       DC     A(RE2+16)       address of v2 source
00001164  000011D8                          569+       DC     A(RE2+32)       address of v3 source
00001168  00000010                          570+       DC     A(16)           result length
0000116C  000011B8                          571+REA2   DC     A(RE2)          result address
00001170  00000000 00000000                 572+       DS     FD              gap
00001178  00000000 00000000                 573+V102   DS     XL16            V1 output
00001180  00000000 00000000
00001188  00000000 00000000                 574+       DS     FD              gap
                                            575+*
00001190                                    576+X2     DS     0F
00001190  E310 5010 0014          00000010  577+       LGF    R1,V2ADDR       load v2 source
00001196  E761 0000 0806          00000000  578+       VL     v22,0(R1)       use v22 to test decoder
0000119C  E310 5014 0014          00000014  579+       LGF    R1,V3ADDR       load v3 source
000011A2  E771 0000 0806          00000000  580+       VL     v23,0(R1)       use v23 to test decoder
000011A8  E766 7000 0E70                    581+       VESLV  V22,V22,V23,0    test instruction (dest is a source)
000011AE  E760 5028 080E          00001178  582+       VST    V22,V102         save v1 output
000011B4  07FB                              583+       BR     R11             return
000011B8                                    584+RE2    DC     0F              xl16 expected result
000011B8                                    585+       DROP   R5
000011B8  FFFEFCF8 F0E0C080                 586        DC     XL16'FFFEFCF8F0E0C080 FFFEFCF8F0E0C080'    result
000011C0  FFFEFCF8 F0E0C080
000011C8  FFFFFFFF FFFFFFFF                 587        DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v2
000011D0  FFFFFFFF FFFFFFFF
000011D8  00010203 04050607                 588        DC     XL16'0001020304050607 08090A0B0C0D0E0F'    v3
000011E0  08090A0B 0C0D0E0F
                                            589
                                            590        VRR_C  VESLV,0
000011E8                                    591+       DS     0FD
000011E8                       000011E8     592+       USING  *,R5            base for test data and test routine
000011E8  00001228                          593+T3     DC     A(X3)           address of test routine
000011EC  0003                              594+       DC     H'3'            test number
000011EE  00                                595+       DC     X'00'
000011EF  00                                596+       DC     HL1'0'          m4
000011F0  E5C5E2D3 E5404040                 597+       DC     CL8'VESLV'      instruction name
000011F8  00001260                          598+       DC     A(RE3+16)       address of v2 source
000011FC  00001270                          599+       DC     A(RE3+32)       address of v3 source
00001200  00000010                          600+       DC     A(16)           result length
00001204  00001250                          601+REA3   DC     A(RE3)          result address
00001208  00000000 00000000                 602+       DS     FD              gap
00001210  00000000 00000000                 603+V103   DS     XL16            V1 output
00001218  00000000 00000000
00001220  00000000 00000000                 604+       DS     FD              gap
                                            605+*
00001228                                    606+X3     DS     0F
00001228  E310 5010 0014          00000010  607+       LGF    R1,V2ADDR       load v2 source
0000122E  E761 0000 0806          00000000  608+       VL     v22,0(R1)       use v22 to test decoder
00001234  E310 5014 0014          00000014  609+       LGF    R1,V3ADDR       load v3 source
0000123A  E771 0000 0806          00000000  610+       VL     v23,0(R1)       use v23 to test decoder
00001240  E766 7000 0E70                    611+       VESLV  V22,V22,V23,0    test instruction (dest is a source)
00001246  E760 9010 080E          00001210  612+       VST    V22,V103         save v1 output
0000124C  07FB                              613+       BR     R11             return
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001250				614+RE3	DC	0F		xl16 expected result
00001250				615+	DROP	R5		
00001250	01020408 10204080			616	DC	XL16'0102040810204080 0102040810204080'		result
00001258	01020408 10204080							
00001260	01010101 01010101			617	DC	XL16'0101010101010101 0101010101010101'		v2
00001268	01010101 01010101							
00001270	F0F1F2F3 F4F5F6F7			618	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'		v3
00001278	F8F9FAFB FCFDFEFF							
				619				
				620	VRR_C	VESLV,0		
00001280				621+	DS	0FD		
00001280		00001280		622+	USING	*,R5		base for test data and test routine
00001280	000012C0			623+T4	DC	A(X4)		address of test routine
00001284	0004			624+	DC	H'4'		test number
00001286	00			625+	DC	X'00'		
00001287	00			626+	DC	HL1'0'		m4
00001288	E5C5E2D3 E5404040			627+	DC	CL8'VESLV'		instruction name
00001290	000012F8			628+	DC	A(RE4+16)		address of v2 source
00001294	00001308			629+	DC	A(RE4+32)		address of v3 source
00001298	00000010			630+	DC	A(16)		result length
0000129C	000012E8			631+REA4	DC	A(RE4)		result address
000012A0	00000000 00000000			632+	DS	FD		gap
000012A8	00000000 00000000			633+V104	DS	XL16		V1 output
000012B0	00000000 00000000							
000012B8	00000000 00000000			634+	DS	FD		gap
				635+*				
000012C0				636+X4	DS	0F		
000012C0	E310 5010 0014		00000010	637+	LGF	R1,V2ADDR		load v2 source
000012C6	E761 0000 0806		00000000	638+	VL	v22,0(R1)		use v22 to test decoder
000012CC	E310 5014 0014		00000014	639+	LGF	R1,V3ADDR		load v3 source
000012D2	E771 0000 0806		00000000	640+	VL	v23,0(R1)		use v23 to test decoder
000012D8	E766 7000 0E70			641+	VESLV	V22,V22,V23,0		test instruction (dest is a source)
000012DE	E760 5028 080E		000012A8	642+	VST	V22,V104		save v1 output
000012E4	07FB			643+	BR	R11		return
000012E8				644+RE4	DC	0F		xl16 expected result
000012E8				645+	DROP	R5		
000012E8	FFFEFCF8 F0E0C080			646	DC	XL16'FFFEFCF8F0E0C080 FFFEFCF8F0E0C080'		result
000012F0	FFFEFCF8 F0E0C080							
000012F8	FFFFFFFF FFFFFFFF			647	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'		v2
00001300	FFFFFFFF FFFFFFFF							
00001308	F0F1F2F3 F4F5F6F7			648	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'		v3
00001310	F8F9FAFB FCFDFEFF							
				649				
				650	*Halfword			
				651	VRR_C	VESLV,1		
00001318				652+	DS	0FD		
00001318		00001318		653+	USING	*,R5		base for test data and test routine
00001318	00001358			654+T5	DC	A(X5)		address of test routine
0000131C	0005			655+	DC	H'5'		test number
0000131E	00			656+	DC	X'00'		
0000131F	01			657+	DC	HL1'1'		m4
00001320	E5C5E2D3 E5404040			658+	DC	CL8'VESLV'		instruction name
00001328	00001390			659+	DC	A(RE5+16)		address of v2 source
0000132C	000013A0			660+	DC	A(RE5+32)		address of v3 source
00001330	00000010			661+	DC	A(16)		result length
00001334	00001380			662+REA5	DC	A(RE5)		result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001338	00000000 00000000			663+	DS	FD	gap
00001340	00000000 00000000			664+V105	DS	XL16	V1 output
00001348	00000000 00000000						
00001350	00000000 00000000			665+	DS	FD	gap
				666+*			
00001358				667+X5	DS	0F	
00001358	E310 5010 0014		00000010	668+	LGF	R1,V2ADDR	load v2 source
0000135E	E761 0000 0806		00000000	669+	VL	v22,0(R1)	use v22 to test decoder
00001364	E310 5014 0014		00000014	670+	LGF	R1,V3ADDR	load v3 source
0000136A	E771 0000 0806		00000000	671+	VL	v23,0(R1)	use v23 to test decoder
00001370	E766 7000 1E70			672+	VESLV V22,V22,V23,1		test instruction (dest is a source)
00001376	E760 5028 080E		00001340	673+	VST	V22,V105	save v1 output
0000137C	07FB			674+	BR	R11	return
00001380				675+RE5	DC	0F	xl16 expected result
00001380				676+	DROP	R5	
00001380	00010002 00040008			677	DC	XL16'0001000200040008 0010002000400080' result	
00001388	00100020 00400080						
00001390	00010001 00010001			678	DC	XL16'0001000100010001 0001000100010001' v2	
00001398	00010001 00010001						
000013A0	00000001 00020003			679	DC	XL16'0000000100020003 0004000500060007' v3	
000013A8	00040005 00060007						
				680			
				681	VRR_C VESLV,1		
000013B0				682+	DS	0FD	
000013B0		000013B0		683+	USING *,R5		base for test data and test routine
000013B0	000013F0			684+T6	DC	A(X6)	address of test routine
000013B4	0006			685+	DC	H'6'	test number
000013B6	00			686+	DC	X'00'	
000013B7	01			687+	DC	HL1'1'	m4
000013B8	E5C5E2D3 E5404040			688+	DC	CL8'VESLV'	instruction name
000013C0	00001428			689+	DC	A(RE6+16)	address of v2 source
000013C4	00001438			690+	DC	A(RE6+32)	address of v3 source
000013C8	00000010			691+	DC	A(16)	result length
000013CC	00001418			692+REA6	DC	A(RE6)	result address
000013D0	00000000 00000000			693+	DS	FD	gap
000013D8	00000000 00000000			694+V106	DS	XL16	V1 output
000013E0	00000000 00000000						
000013E8	00000000 00000000			695+	DS	FD	gap
				696+*			
000013F0				697+X6	DS	0F	
000013F0	E310 5010 0014		00000010	698+	LGF	R1,V2ADDR	load v2 source
000013F6	E761 0000 0806		00000000	699+	VL	v22,0(R1)	use v22 to test decoder
000013FC	E310 5014 0014		00000014	700+	LGF	R1,V3ADDR	load v3 source
00001402	E771 0000 0806		00000000	701+	VL	v23,0(R1)	use v23 to test decoder
00001408	E766 7000 1E70			702+	VESLV V22,V22,V23,1		test instruction (dest is a source)
0000140E	E760 5028 080E		000013D8	703+	VST	V22,V106	save v1 output
00001414	07FB			704+	BR	R11	return
00001418				705+RE6	DC	0F	xl16 expected result
00001418				706+	DROP	R5	
00001418	01000200 04000800			707	DC	XL16'0100020004000800 1000200040008000' result	
00001420	10002000 40008000						
00001428	00010001 00010001			708	DC	XL16'0001000100010001 0001000100010001' v2	
00001430	00010001 00010001						
00001438	00080009 000A000B			709	DC	XL16'00080009000A000B 000C000D000E000F' v3	
00001440	000C000D 000E000F						
				710			

```
  LOC        OBJECT CODE     ADDR1     ADDR2     STMT


                                                711              VRR_C VESLV,1
00001448                                        712+             DS    0FD
00001448                       00001448         713+             USING *,R5              base for test data and test routine
00001448  00001488                              714+T7           DC    A(X7)              address of test routine
0000144C  0007                                  715+             DC    H'7'               test number
0000144E  00                                    716+             DC    X'00'
0000144F  01                                    717+             DC    HL1'1'             m4
00001450  E5C5E2D3 E5404040                      718+             DC    CL8'VESLV'         instruction name
00001458  000014C0                              719+             DC    A(RE7+16)          address of v2 source
0000145C  000014D0                              720+             DC    A(RE7+32)          address of v3 source
00001460  00000010                              721+             DC    A(16)              result length
00001464  000014B0                              722+REA7         DC    A(RE7)             result address
00001468  00000000 00000000                      723+             DS    FD                 gap
00001470  00000000 00000000                      724+V107         DS    XL16               V1 output
00001478  00000000 00000000
00001480  00000000 00000000                      725+             DS    FD                 gap
                                                726+*
00001488                                        727+X7           DS    0F
00001488  E310 5010 0014                 00000010 728+             LGF   R1,V2ADDR          load v2 source
0000148E  E761 0000 0806                 00000000 729+             VL    v22,0(R1)          use v22 to test decoder
00001494  E310 5014 0014                 00000014 730+             LGF   R1,V3ADDR          load v3 source
0000149A  E771 0000 0806                 00000000 731+             VL    v23,0(R1)          use v23 to test decoder
000014A0  E766 7000 1E70                          732+             VESLV V22,V22,V23,1        test instruction (dest is a source)
000014A6  E760 5028 080E                 00001470 733+             VST   V22,V107            save v1 output
000014AC  07FB                                    734+             BR    R11                return
000014B0                                          735+RE7          DC    0F                 xl16 expected result
000014B0                                          736+             DROP  R5
000014B0  FFFFFFFE FFFCFFF8                        737              DC    XL16'FFFFFFFEFFFCFFF8 FFF0FFE0FFC0FF80'     result
000014B8  FFF0FFE0 FFC0FF80
000014C0  FFFFFFFF FFFFFFFF                        738              DC    XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'     v2
000014C8  FFFFFFFF FFFFFFFF
000014D0  00000001 00020003                        739              DC    XL16'0000000100020003 0004000500060007'     v3
000014D8  00040005 00060007
                                                740
                                                741              VRR_C VESLV,1
000014E0                                        742+             DS    0FD
000014E0                       000014E0         743+             USING *,R5              base for test data and test routine
000014E0  00001520                              744+T8           DC    A(X8)              address of test routine
000014E4  0008                                  745+             DC    H'8'               test number
000014E6  00                                    746+             DC    X'00'
000014E7  01                                    747+             DC    HL1'1'             m4
000014E8  E5C5E2D3 E5404040                      748+             DC    CL8'VESLV'         instruction name
000014F0  00001558                              749+             DC    A(RE8+16)          address of v2 source
000014F4  00001568                              750+             DC    A(RE8+32)          address of v3 source
000014F8  00000010                              751+             DC    A(16)              result length
000014FC  00001548                              752+REA8         DC    A(RE8)             result address
00001500  00000000 00000000                      753+             DS    FD                 gap
00001508  00000000 00000000                      754+V108         DS    XL16               V1 output
00001510  00000000 00000000
00001518  00000000 00000000                      755+             DS    FD                 gap
                                                756+*
00001520                                        757+X8           DS    0F
00001520  E310 5010 0014                 00000010 758+             LGF   R1,V2ADDR          load v2 source
00001526  E761 0000 0806                 00000000 759+             VL    v22,0(R1)          use v22 to test decoder
0000152C  E310 5014 0014                 00000014 760+             LGF   R1,V3ADDR          load v3 source
00001532  E771 0000 0806                 00000000 761+             VL    v23,0(R1)          use v23 to test decoder
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001538	E766 7000 1E70			762+	VESLV	V22,V22,V23,1	test instruction (dest is a source)
0000153E	E760 5028 080E		00001508	763+	VST	V22,V108	save v1 output
00001544	07FB			764+	BR	R11	return
00001548				765+RE8	DC	0F	xl16 expected result
00001548				766+	DROP	R5	
00001548	FF00FE00 FC00F800			767	DC	XL16'FF00FE00FC00F800 F000E000C0008000'	result
00001550	F000E000 C0008000						
00001558	FFFFFFFF FFFFFFFF			768	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00001560	FFFFFFFF FFFFFFFF						
00001568	00080009 000A000B			769	DC	XL16'00080009000A000B 000C000D000E000F'	v3
00001570	000C000D 000E000F						
				770			
				771	VRR_C	VESLV,1	
00001578				772+	DS	0FD	
00001578		00001578		773+	USING	*,R5	base for test data and test routine
00001578	000015B8			774+T9	DC	A(X9)	address of test routine
0000157C	0009			775+	DC	H'9'	test number
0000157E	00			776+	DC	X'00'	
0000157F	01			777+	DC	HL1'1'	m4
00001580	E5C5E2D3 E5404040			778+	DC	CL8'VESLV'	instruction name
00001588	000015F0			779+	DC	A(RE9+16)	address of v2 source
0000158C	00001600			780+	DC	A(RE9+32)	address of v3 source
00001590	00000010			781+	DC	A(16)	result length
00001594	000015E0			782+REA9	DC	A(RE9)	result address
00001598	00000000 00000000			783+	DS	FD	gap
000015A0	00000000 00000000			784+V109	DS	XL16	V1 output
000015A8	00000000 00000000						
000015B0	00000000 00000000			785+	DS	FD	gap
				786+*			
000015B8				787+X9	DS	0F	
000015B8	E310 5010 0014		00000010	788+	LGF	R1,V2ADDR	load v2 source
000015BE	E761 0000 0806		00000000	789+	VL	v22,0(R1)	use v22 to test decoder
000015C4	E310 5014 0014		00000014	790+	LGF	R1,V3ADDR	load v3 source
000015CA	E771 0000 0806		00000000	791+	VL	v23,0(R1)	use v23 to test decoder
000015D0	E766 7000 1E70			792+	VESLV	V22,V22,V23,1	test instruction (dest is a source)
000015D6	E760 5028 080E		000015A0	793+	VST	V22,V109	save v1 output
000015DC	07FB			794+	BR	R11	return
000015E0				795+RE9	DC	0F	xl16 expected result
000015E0				796+	DROP	R5	
000015E0	00010002 00040008			797	DC	XL16'0001000200040008 0010002000400080'	result
000015E8	00100020 00400080						
000015F0	00010001 00010001			798	DC	XL16'0001000100010001 0001000100010001'	v2
000015F8	00010001 00010001						
00001600	F000F001 F002F003			799	DC	XL16'F000F001F002F003 F004F005F006F007'	v3
00001608	F004F005 F006F007						
				800			
				801	VRR_C	VESLV,1	
00001610				802+	DS	0FD	
00001610		00001610		803+	USING	*,R5	base for test data and test routine
00001610	00001650			804+T10	DC	A(X10)	address of test routine
00001614	000A			805+	DC	H'10'	test number
00001616	00			806+	DC	X'00'	
00001617	01			807+	DC	HL1'1'	m4
00001618	E5C5E2D3 E5404040			808+	DC	CL8'VESLV'	instruction name
00001620	00001688			809+	DC	A(RE10+16)	address of v2 source
00001624	00001698			810+	DC	A(RE10+32)	address of v3 source

```
  LOC       OBJECT CODE      ADDR1     ADDR2     STMT

00001628  00000010                               811+      DC      A(16)           result length
0000162C  00001678                               812+REA10  DC      A(RE10)         result address
00001630  00000000 00000000                      813+      DS      FD              gap
00001638  00000000 00000000                      814+V1010  DS      XL16            V1 output
00001640  00000000 00000000
00001648  00000000 00000000                      815+      DS      FD              gap
                                                 816+*
00001650                                         817+X10    DS      0F
00001650  E310 5010 0014              00000010   818+      LGF     R1,V2ADDR       load v2 source
00001656  E761 0000 0806              00000000   819+      VL      v22,0(R1)       use v22 to test decoder
0000165C  E310 5014 0014              00000014   820+      LGF     R1,V3ADDR       load v3 source
00001662  E771 0000 0806              00000000   821+      VL      v23,0(R1)       use v23 to test decoder
00001668  E766 7000 1E70                         822+      VESLV   V22,V22,V23,1    test instruction (dest is a source)
0000166E  E760 5028 080E              00001638   823+      VST     V22,V1010        save v1 output
00001674  07FB                                   824+      BR      R11             return
00001678                                         825+RE10   DC      0F              xl16 expected result
00001678                                         826+      DROP    R5
00001678  FFFFFFFE FFFCFFF8                       827       DC      XL16'FFFFFFFEFFFCFFF8 FFF0FFE0FFC0FF80'     result
00001680  FFF0FFE0 FFC0FF80
00001688  FFFFFFFF FFFFFFFF                       828       DC      XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'     v2
00001690  FFFFFFFF FFFFFFFF
00001698  F000F001 F002F003                       829       DC      XL16'F000F001F002F003 F004F005F006F007'    v3
000016A0  F004F005 F006F007
                                                  830
                                                  831 *Word
                                                  832          VRR_C  VESLV,2
000016A8                                         833+      DS      0FD
000016A8              000016A8                    834+      USING   *,R5            base for test data and test routine
000016A8  000016E8                               835+T11    DC      A(X11)          address of test routine
000016AC  000B                                   836+      DC      H'11'           test number
000016AE  00                                     837+      DC      X'00'
000016AF  02                                     838+      DC      HL1'2'          m4
000016B0  E5C5E2D3 E5404040                       839+      DC      CL8'VESLV'      instruction name
000016B8  00001720                               840+      DC      A(RE11+16)      address of v2 source
000016BC  00001730                               841+      DC      A(RE11+32)      address of v3 source
000016C0  00000010                               842+      DC      A(16)           result length
000016C4  00001710                               843+REA11  DC      A(RE11)         result address
000016C8  00000000 00000000                      844+      DS      FD              gap
000016D0  00000000 00000000                      845+V1011  DS      XL16            V1 output
000016D8  00000000 00000000
000016E0  00000000 00000000                      846+      DS      FD              gap
                                                 847+*
000016E8                                         848+X11    DS      0F
000016E8  E310 5010 0014              00000010   849+      LGF     R1,V2ADDR       load v2 source
000016EE  E761 0000 0806              00000000   850+      VL      v22,0(R1)       use v22 to test decoder
000016F4  E310 5014 0014              00000014   851+      LGF     R1,V3ADDR       load v3 source
000016FA  E771 0000 0806              00000000   852+      VL      v23,0(R1)       use v23 to test decoder
00001700  E766 7000 2E70                         853+      VESLV   V22,V22,V23,2    test instruction (dest is a source)
00001706  E760 5028 080E              000016D0   854+      VST     V22,V1011        save v1 output
0000170C  07FB                                   855+      BR      R11             return
00001710                                         856+RE11   DC      0F              xl16 expected result
00001710                                         857+      DROP    R5
00001710  00000001 00000002                       858       DC      XL16'0000000100000002 0000000400000008'    result
00001718  00000004 00000008
00001720  00000001 00000001                       859       DC      XL16'0000000100000001 0000000100000001'    v2
00001728  00000001 00000001
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001730	00000000 00000001			860	DC	XL16'0000000000000001 0000000200000003'	v3
00001738	00000002 00000003						
				861			
				862	VRR_C	VESLV,2	
00001740				863+	DS	0FD	
00001740		00001740		864+	USING	*,R5	base for test data and test routine
00001740	00001780			865+T12	DC	A(X12)	address of test routine
00001744	000C			866+	DC	H'12'	test number
00001746	00			867+	DC	X'00'	
00001747	02			868+	DC	HL1'2'	m4
00001748	E5C5E2D3 E5404040			869+	DC	CL8'VESLV'	instruction name
00001750	000017B8			870+	DC	A(RE12+16)	address of v2 source
00001754	000017C8			871+	DC	A(RE12+32)	address of v3 source
00001758	00000010			872+	DC	A(16)	result length
0000175C	000017A8			873+REA12	DC	A(RE12)	result address
00001760	00000000 00000000			874+	DS	FD	gap
00001768	00000000 00000000			875+V1012	DS	XL16	V1 output
00001770	00000000 00000000						
00001778	00000000 00000000			876+	DS	FD	gap
				877+*			
00001780				878+X12	DS	0F	
00001780	E310 5010 0014		00000010	879+	LGF	R1,V2ADDR	load v2 source
00001786	E761 0000 0806		00000000	880+	VL	v22,0(R1)	use v22 to test decoder
0000178C	E310 5014 0014		00000014	881+	LGF	R1,V3ADDR	load v3 source
00001792	E771 0000 0806		00000000	882+	VL	v23,0(R1)	use v23 to test decoder
00001798	E766 7000 2E70			883+	VESLV	V22,V22,V23,2	test instruction (dest is a source)
0000179E	E760 5028 080E		00001768	884+	VST	V22,V1012	save v1 output
000017A4	07FB			885+	BR	R11	return
000017A8				886+RE12	DC	0F	xl16 expected result
000017A8				887+	DROP	R5	
000017A8	00000100 00000200			888	DC	XL16'0000010000000200 0000040000000800'	result
000017B0	00000400 00000800						
000017B8	00000001 00000001			889	DC	XL16'0000000100000001 0000000100000001'	v2
000017C0	00000001 00000001						
000017C8	00000008 00000009			890	DC	XL16'0000000800000009 0000000A0000000B'	v3
000017D0	0000000A 0000000B						
				891			
				892	VRR_C	VESLV,2	
000017D8				893+	DS	0FD	
000017D8		000017D8		894+	USING	*,R5	base for test data and test routine
000017D8	00001818			895+T13	DC	A(X13)	address of test routine
000017DC	000D			896+	DC	H'13'	test number
000017DE	00			897+	DC	X'00'	
000017DF	02			898+	DC	HL1'2'	m4
000017E0	E5C5E2D3 E5404040			899+	DC	CL8'VESLV'	instruction name
000017E8	00001850			900+	DC	A(RE13+16)	address of v2 source
000017EC	00001860			901+	DC	A(RE13+32)	address of v3 source
000017F0	00000010			902+	DC	A(16)	result length
000017F4	00001840			903+REA13	DC	A(RE13)	result address
000017F8	00000000 00000000			904+	DS	FD	gap
00001800	00000000 00000000			905+V1013	DS	XL16	V1 output
00001808	00000000 00000000						
00001810	00000000 00000000			906+	DS	FD	gap
				907+*			
00001818				908+X13	DS	0F	
00001818	E310 5010 0014		00000010	909+	LGF	R1,V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000181E	E761 0000 0806		00000000	910+	VL	v22,0(R1)	use v22 to test decoder
00001824	E310 5014 0014		00000014	911+	LGF	R1,V3ADDR	load v3 source
0000182A	E771 0000 0806		00000000	912+	VL	v23,0(R1)	use v23 to test decoder
00001830	E766 7000 2E70			913+	VESLV	V22,V22,V23,2	test instruction (dest is a source)
00001836	E760 5028 080E		00001800	914+	VST	V22,V1013	save v1 output
0000183C	07FB			915+	BR	R11	return
00001840				916+RE13	DC	0F	xl16 expected result
00001840				917+	DROP	R5	
00001840	FFFFFFFF FFFFFFFE			918	DC	XL16'FFFFFFFFFFFFFFFE FFFFFFFCFFFFFFF8'	result
00001848	FFFFFFFC FFFFFFF8						
00001850	FFFFFFFF FFFFFFFF			919	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00001858	FFFFFFFF FFFFFFFF						
00001860	00000000 00000001			920	DC	XL16'0000000000000001 0000000200000003'	v3
00001868	00000002 00000003						
				921			
				922	VRR_C	VESLV,2	
00001870				923+	DS	0FD	
00001870		00001870		924+	USING	*,R5	base for test data and test routine
00001870	000018B0			925+T14	DC	A(X14)	address of test routine
00001874	000E			926+	DC	H'14'	test number
00001876	00			927+	DC	X'00'	
00001877	02			928+	DC	HL1'2'	m4
00001878	E5C5E2D3 E5404040			929+	DC	CL8'VESLV'	instruction name
00001880	000018E8			930+	DC	A(RE14+16)	address of v2 source
00001884	000018F8			931+	DC	A(RE14+32)	address of v3 source
00001888	00000010			932+	DC	A(16)	result length
0000188C	000018D8			933+REA14	DC	A(RE14)	result address
00001890	00000000 00000000			934+	DS	FD	gap
00001898	00000000 00000000			935+V1014	DS	XL16	V1 output
000018A0	00000000 00000000						
000018A8	00000000 00000000			936+	DS	FD	gap
				937+*			
000018B0				938+X14	DS	0F	
000018B0	E310 5010 0014		00000010	939+	LGF	R1,V2ADDR	load v2 source
000018B6	E761 0000 0806		00000000	940+	VL	v22,0(R1)	use v22 to test decoder
000018BC	E310 5014 0014		00000014	941+	LGF	R1,V3ADDR	load v3 source
000018C2	E771 0000 0806		00000000	942+	VL	v23,0(R1)	use v23 to test decoder
000018C8	E766 7000 2E70			943+	VESLV	V22,V22,V23,2	test instruction (dest is a source)
000018CE	E760 5028 080E		00001898	944+	VST	V22,V1014	save v1 output
000018D4	07FB			945+	BR	R11	return
000018D8				946+RE14	DC	0F	xl16 expected result
000018D8				947+	DROP	R5	
000018D8	FFFFFF00 FFFFFE00			948	DC	XL16'FFFFFF00FFFFFE00 FFFFFC00FFFFF800'	result
000018E0	FFFFFC00 FFFFF800						
000018E8	FFFFFFFF FFFFFFFF			949	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
000018F0	FFFFFFFF FFFFFFFF						
000018F8	00000008 00000009			950	DC	XL16'0000000800000009 0000000A0000000B'	v3
00001900	0000000A 0000000B						
				951			
				952	VRR_C	VESLV,2	
00001908				953+	DS	0FD	
00001908		00001908		954+	USING	*,R5	base for test data and test routine
00001908	00001948			955+T15	DC	A(X15)	address of test routine
0000190C	000F			956+	DC	H'15'	test number
0000190E	00			957+	DC	X'00'	
0000190F	02			958+	DC	HL1'2'	m4

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001910	E5C5E2D3 E5404040			959+	DC	CL8'VESLV'		instruction name
00001918	00001980			960+	DC	A(RE15+16)		address of v2 source
0000191C	00001990			961+	DC	A(RE15+32)		address of v3 source
00001920	00000010			962+	DC	A(16)		result length
00001924	00001970			963+REA15	DC	A(RE15)		result address
00001928	00000000 00000000			964+	DS	FD		gap
00001930	00000000 00000000			965+V1015	DS	XL16		V1 output
00001938	00000000 00000000							
00001940	00000000 00000000			966+	DS	FD		gap
				967+*				
00001948				968+X15	DS	0F		
00001948	E310 5010 0014		00000010	969+	LGF	R1,V2ADDR		load v2 source
0000194E	E761 0000 0806		00000000	970+	VL	v22,0(R1)		use v22 to test decoder
00001954	E310 5014 0014		00000014	971+	LGF	R1,V3ADDR		load v3 source
0000195A	E771 0000 0806		00000000	972+	VL	v23,0(R1)		use v23 to test decoder
00001960	E766 7000 2E70			973+	VESLV	V22,V22,V23,2		test instruction (dest is a source)
00001966	E760 5028 080E		00001930	974+	VST	V22,V1015		save v1 output
0000196C	07FB			975+	BR	R11		return
00001970				976+RE15	DC	0F		xl16 expected result
00001970				977+	DROP	R5		
00001970	00000001 00000002			978	DC	XL16'0000000100000002 0000000400000008'	result
00001978	00000004 00000008							
00001980	00000001 00000001			979	DC	XL16'0000000100000001 0000000100000001'	v2
00001988	00000001 00000001							
00001990	F0000000 F0000001			980	DC	XL16'F0000000F0000001 F0000002F0000003'	v3
00001998	F0000002 F0000003							
				981				
				982		VRR_C VESLV,2		
000019A0				983+	DS	0FD		
000019A0		000019A0		984+	USING	*,R5		base for test data and test routine
000019A0	000019E0			985+T16	DC	A(X16)		address of test routine
000019A4	0010			986+	DC	H'16'		test number
000019A6	00			987+	DC	X'00'		
000019A7	02			988+	DC	HL1'2'		m4
000019A8	E5C5E2D3 E5404040			989+	DC	CL8'VESLV'		instruction name
000019B0	00001A18			990+	DC	A(RE16+16)		address of v2 source
000019B4	00001A28			991+	DC	A(RE16+32)		address of v3 source
000019B8	00000010			992+	DC	A(16)		result length
000019BC	00001A08			993+REA16	DC	A(RE16)		result address
000019C0	00000000 00000000			994+	DS	FD		gap
000019C8	00000000 00000000			995+V1016	DS	XL16		V1 output
000019D0	00000000 00000000							
000019D8	00000000 00000000			996+	DS	FD		gap
				997+*				
000019E0				998+X16	DS	0F		
000019E0	E310 5010 0014		00000010	999+	LGF	R1,V2ADDR		load v2 source
000019E6	E761 0000 0806		00000000	1000+	VL	v22,0(R1)		use v22 to test decoder
000019EC	E310 5014 0014		00000014	1001+	LGF	R1,V3ADDR		load v3 source
000019F2	E771 0000 0806		00000000	1002+	VL	v23,0(R1)		use v23 to test decoder
000019F8	E766 7000 2E70			1003+	VESLV	V22,V22,V23,2		test instruction (dest is a source)
000019FE	E760 5028 080E		000019C8	1004+	VST	V22,V1016		save v1 output
00001A04	07FB			1005+	BR	R11		return
00001A08				1006+RE16	DC	0F		xl16 expected result
00001A08				1007+	DROP	R5		
00001A08	FFFFFF00 FFFFFE00			1008	DC	XL16'FFFFFF00FFFFFE00 FFFFFC00FFFFF800'	result
00001A10	FFFFFC00 FFFFF800							

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  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

00001A18  FFFFFFFF FFFFFFFF                         1009       DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v2
00001A20  FFFFFFFF FFFFFFFF
00001A28  F0000008 F0000009                         1010       DC     XL16'F0000008F0000009 F000000AF000000B'   v3
00001A30  F000000A F000000B
                                                    1011
                                                    1012  *Doubleword
                                                    1013       VRR_C  VESLV,3
00001A38                                            1014+      DS     0FD
00001A38                     00001A38               1015+      USING  *,R5                 base for test data and test routine
00001A38  00001A78                                  1016+T17   DC     A(X17)               address of test routine
00001A3C  0011                                      1017+      DC     H'17'                test number
00001A3E  00                                        1018+      DC     X'00'
00001A3F  03                                        1019+      DC     HL1'3'               m4
00001A40  E5C5E2D3 E5404040                         1020+      DC     CL8'VESLV'           instruction name
00001A48  00001AB0                                  1021+      DC     A(RE17+16)           address of v2 source
00001A4C  00001AC0                                  1022+      DC     A(RE17+32)           address of v3 source
00001A50  00000010                                  1023+      DC     A(16)                result length
00001A54  00001AA0                                  1024+REA17 DC     A(RE17)              result address
00001A58  00000000 00000000                         1025+      DS     FD                   gap
00001A60  00000000 00000000                         1026+V1017 DS     XL16                 V1 output
00001A68  00000000 00000000
00001A70  00000000 00000000                         1027+      DS     FD                   gap
                                                    1028+*
00001A78                                            1029+X17   DS     0F
00001A78  E310 5010 0014                 00000010   1030+      LGF    R1,V2ADDR            load v2 source
00001A7E  E761 0000 0806                 00000000   1031+      VL     v22,0(R1)            use v22 to test decoder
00001A84  E310 5014 0014                 00000014   1032+      LGF    R1,V3ADDR            load v3 source
00001A8A  E771 0000 0806                 00000000   1033+      VL     v23,0(R1)            use v23 to test decoder
00001A90  E766 7000 3E70                            1034+      VESLV  V22,V22,V23,3         test instruction (dest is a source)
00001A96  E760 5028 080E                 00001A60   1035+      VST    V22,V1017            save v1 output
00001A9C  07FB                                      1036+      BR     R11                  return
00001AA0                                            1037+RE17  DC     0F                   xl16 expected result
00001AA0                                            1038+      DROP   R5
00001AA0  00000000 00000001                         1039       DC     XL16'0000000000000001 0000000000000002'   result
00001AA8  00000000 00000002
00001AB0  00000000 00000001                         1040       DC     XL16'0000000000000001 0000000000000001'   v2
00001AB8  00000000 00000001
00001AC0  00000000 00000000                         1041       DC     XL16'0000000000000000 0000000000000001'   v3
00001AC8  00000000 00000001
                                                    1042
                                                    1043       VRR_C  VESLV,3
00001AD0                                            1044+      DS     0FD
00001AD0                     00001AD0               1045+      USING  *,R5                 base for test data and test routine
00001AD0  00001B10                                  1046+T18   DC     A(X18)               address of test routine
00001AD4  0012                                      1047+      DC     H'18'                test number
00001AD6  00                                        1048+      DC     X'00'
00001AD7  03                                        1049+      DC     HL1'3'               m4
00001AD8  E5C5E2D3 E5404040                         1050+      DC     CL8'VESLV'           instruction name
00001AE0  00001B48                                  1051+      DC     A(RE18+16)           address of v2 source
00001AE4  00001B58                                  1052+      DC     A(RE18+32)           address of v3 source
00001AE8  00000010                                  1053+      DC     A(16)                result length
00001AEC  00001B38                                  1054+REA18 DC     A(RE18)              result address
00001AF0  00000000 00000000                         1055+      DS     FD                   gap
00001AF8  00000000 00000000                         1056+V1018 DS     XL16                 V1 output
00001B00  00000000 00000000
00001B08  00000000 00000000                         1057+      DS     FD                   gap
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				1058+*			
00001B10				1059+X18	DS	0F	
00001B10	E310 5010 0014		00000010	1060+	LGF	R1,V2ADDR	load v2 source
00001B16	E761 0000 0806		00000000	1061+	VL	v22,0(R1)	use v22 to test decoder
00001B1C	E310 5014 0014		00000014	1062+	LGF	R1,V3ADDR	load v3 source
00001B22	E771 0000 0806		00000000	1063+	VL	v23,0(R1)	use v23 to test decoder
00001B28	E766 7000 3E70			1064+	VESLV	V22,V22,V23,3	test instruction (dest is a source)
00001B2E	E760 5028 080E		00001AF8	1065+	VST	V22,V1018	save v1 output
00001B34	07FB			1066+	BR	R11	return
00001B38				1067+RE18	DC	0F	xl16 expected result
00001B38				1068+	DROP	R5	
00001B38	00000000 00000400			1069	DC	XL16'0000000000000400 0000000000000800'	result
00001B40	00000000 00000800						
00001B48	00000000 00000001			1070	DC	XL16'0000000000000001 0000000000000001'	v2
00001B50	00000000 00000001						
00001B58	00000000 0000000A			1071	DC	XL16'000000000000000A 000000000000000B'	v3
00001B60	00000000 0000000B						
				1072			
				1073	VRR_C	VESLV,3	
00001B68				1074+	DS	0FD	
00001B68		00001B68		1075+	USING	*,R5	base for test data and test routine
00001B68	00001BA8			1076+T19	DC	A(X19)	address of test routine
00001B6C	0013			1077+	DC	H'19'	test number
00001B6E	00			1078+	DC	X'00'	
00001B6F	03			1079+	DC	HL1'3'	m4
00001B70	E5C5E2D3 E5404040			1080+	DC	CL8'VESLV'	instruction name
00001B78	00001BE0			1081+	DC	A(RE19+16)	address of v2 source
00001B7C	00001BF0			1082+	DC	A(RE19+32)	address of v3 source
00001B80	00000010			1083+	DC	A(16)	result length
00001B84	00001BD0			1084+REA19	DC	A(RE19)	result address
00001B88	00000000 00000000			1085+	DS	FD	gap
00001B90	00000000 00000000			1086+V1019	DS	XL16	V1 output
00001B98	00000000 00000000						
00001BA0	00000000 00000000			1087+	DS	FD	gap
				1088+*			
00001BA8				1089+X19	DS	0F	
00001BA8	E310 5010 0014		00000010	1090+	LGF	R1,V2ADDR	load v2 source
00001BAE	E761 0000 0806		00000000	1091+	VL	v22,0(R1)	use v22 to test decoder
00001BB4	E310 5014 0014		00000014	1092+	LGF	R1,V3ADDR	load v3 source
00001BBA	E771 0000 0806		00000000	1093+	VL	v23,0(R1)	use v23 to test decoder
00001BC0	E766 7000 3E70			1094+	VESLV	V22,V22,V23,3	test instruction (dest is a source)
00001BC6	E760 5028 080E		00001B90	1095+	VST	V22,V1019	save v1 output
00001BCC	07FB			1096+	BR	R11	return
00001BD0				1097+RE19	DC	0F	xl16 expected result
00001BD0				1098+	DROP	R5	
00001BD0	00000400 00000000			1099	DC	XL16'0000040000000000 0800000000000000'	result
00001BD8	08000000 00000000						
00001BE0	00000000 00000001			1100	DC	XL16'0000000000000001 0000000000000001'	v2
00001BE8	00000000 00000001						
00001BF0	00000000 0000002A			1101	DC	XL16'000000000000002A 000000000000003B'	v3
00001BF8	00000000 0000003B						
				1102			
				1103	VRR_C	VESLV,3	
00001C00				1104+	DS	0FD	
00001C00		00001C00		1105+	USING	*,R5	base for test data and test routine
00001C00	00001C40			1106+T20	DC	A(X20)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001C04	0014			1107+	DC	H'20'		test number
00001C06	00			1108+	DC	X'00'		
00001C07	03			1109+	DC	HL1'3'		m4
00001C08	E5C5E2D3 E5404040			1110+	DC	CL8'VESLV'		instruction name
00001C10	00001C78			1111+	DC	A(RE20+16)		address of v2 source
00001C14	00001C88			1112+	DC	A(RE20+32)		address of v3 source
00001C18	00000010			1113+	DC	A(16)		result length
00001C1C	00001C68			1114+REA20	DC	A(RE20)		result address
00001C20	00000000 00000000			1115+	DS	FD		gap
00001C28	00000000 00000000			1116+V1020	DS	XL16		V1 output
00001C30	00000000 00000000							
00001C38	00000000 00000000			1117+	DS	FD		gap
				1118+*				
00001C40				1119+X20	DS	0F		
00001C40	E310 5010 0014		00000010	1120+	LGF	R1,V2ADDR		load v2 source
00001C46	E761 0000 0806		00000000	1121+	VL	v22,0(R1)		use v22 to test decoder
00001C4C	E310 5014 0014		00000014	1122+	LGF	R1,V3ADDR		load v3 source
00001C52	E771 0000 0806		00000000	1123+	VL	v23,0(R1)		use v23 to test decoder
00001C58	E766 7000 3E70			1124+	VESLV	V22,V22,V23,3		test instruction (dest is a source)
00001C5E	E760 5028 080E		00001C28	1125+	VST	V22,V1020		save v1 output
00001C64	07FB			1126+	BR	R11		return
00001C68				1127+RE20	DC	0F		xl16 expected result
00001C68				1128+	DROP	R5		
00001C68	FFFFFFFF FFFFFF80			1129	DC	XL16'FFFFFFFFFFFFFF80 FFFFFFFFFFFC0000'		result
00001C70	FFFFFFFF FFFC0000							
00001C78	FFFFFFFF FFFFFFFF			1130	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'		v2
00001C80	FFFFFFFF FFFFFFFF							
00001C88	00000000 00000007			1131	DC	XL16'0000000000000007 0000000000000012'		v3
00001C90	00000000 00000012							
				1132				
				1133	VRR_C	VESLV,3		
00001C98				1134+	DS	0FD		
00001C98		00001C98		1135+	USING	*,R5		base for test data and test routine
00001C98	00001CD8			1136+T21	DC	A(X21)		address of test routine
00001C9C	0015			1137+	DC	H'21'		test number
00001C9E	00			1138+	DC	X'00'		
00001C9F	03			1139+	DC	HL1'3'		m4
00001CA0	E5C5E2D3 E5404040			1140+	DC	CL8'VESLV'		instruction name
00001CA8	00001D10			1141+	DC	A(RE21+16)		address of v2 source
00001CAC	00001D20			1142+	DC	A(RE21+32)		address of v3 source
00001CB0	00000010			1143+	DC	A(16)		result length
00001CB4	00001D00			1144+REA21	DC	A(RE21)		result address
00001CB8	00000000 00000000			1145+	DS	FD		gap
00001CC0	00000000 00000000			1146+V1021	DS	XL16		V1 output
00001CC8	00000000 00000000							
00001CD0	00000000 00000000			1147+	DS	FD		gap
				1148+*				
00001CD8				1149+X21	DS	0F		
00001CD8	E310 5010 0014		00000010	1150+	LGF	R1,V2ADDR		load v2 source
00001CDE	E761 0000 0806		00000000	1151+	VL	v22,0(R1)		use v22 to test decoder
00001CE4	E310 5014 0014		00000014	1152+	LGF	R1,V3ADDR		load v3 source
00001CEA	E771 0000 0806		00000000	1153+	VL	v23,0(R1)		use v23 to test decoder
00001CF0	E766 7000 3E70			1154+	VESLV	V22,V22,V23,3		test instruction (dest is a source)
00001CF6	E760 5028 080E		00001CC0	1155+	VST	V22,V1021		save v1 output
00001CFC	07FB			1156+	BR	R11		return
00001D00				1157+RE21	DC	0F		xl16 expected result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001D00				1158+	DROP	R5		
00001D00	FFFFFFFC 00000000			1159	DC	XL16'FFFFFFFC00000000 FFF8000000000000'	result	
00001D08	FFF80000 00000000							
00001D10	FFFFFFFF FFFFFFFF			1160	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2	
00001D18	FFFFFFFF FFFFFFFF							
00001D20	00000000 00000022			1161	DC	XL16'0000000000000022 0000000000000033'	v3	
00001D28	00000000 00000033							
				1162				
				1163				
				1164	VRR_C	VESLV,3		
00001D30				1165+	DS	0FD		
00001D30		00001D30		1166+	USING	*,R5	base for test data and test routine	
00001D30	00001D70			1167+T22	DC	A(X22)	address of test routine	
00001D34	0016			1168+	DC	H'22'	test number	
00001D36	00			1169+	DC	X'00'		
00001D37	03			1170+	DC	HL1'3'	m4	
00001D38	E5C5E2D3 E5404040			1171+	DC	CL8'VESLV'	instruction name	
00001D40	00001DA8			1172+	DC	A(RE22+16)	address of v2 source	
00001D44	00001DB8			1173+	DC	A(RE22+32)	address of v3 source	
00001D48	00000010			1174+	DC	A(16)	result length	
00001D4C	00001D98			1175+REA22	DC	A(RE22)	result address	
00001D50	00000000 00000000			1176+	DS	FD	gap	
00001D58	00000000 00000000			1177+V1022	DS	XL16	V1 output	
00001D60	00000000 00000000							
00001D68	00000000 00000000			1178+	DS	FD	gap	
				1179+*				
00001D70				1180+X22	DS	0F		
00001D70	E310 5010 0014		00000010	1181+	LGF	R1,V2ADDR	load v2 source	
00001D76	E761 0000 0806		00000000	1182+	VL	v22,0(R1)	use v22 to test decoder	
00001D7C	E310 5014 0014		00000014	1183+	LGF	R1,V3ADDR	load v3 source	
00001D82	E771 0000 0806		00000000	1184+	VL	v23,0(R1)	use v23 to test decoder	
00001D88	E766 7000 3E70			1185+	VESLV	V22,V22,V23,3	test instruction (dest is a source)	
00001D8E	E760 5028 080E		00001D58	1186+	VST	V22,V1022	save v1 output	
00001D94	07FB			1187+	BR	R11	return	
00001D98				1188+RE22	DC	0F	xl16 expected result	
00001D98				1189+	DROP	R5		
00001D98	00000000 00000400			1190	DC	XL16'0000000000000400 0000000000000800'	result	
00001DA0	00000000 00000800							
00001DA8	00000000 00000001			1191	DC	XL16'0000000000000001 0000000000000001'	v2	
00001DB0	00000000 00000001							
00001DB8	F0000000 0000000A			1192	DC	XL16'F00000000000000A F00000000000000B'	v3	
00001DC0	F0000000 0000000B							
				1193				
				1194	VRR_C	VESLV,3		
00001DC8				1195+	DS	0FD		
00001DC8		00001DC8		1196+	USING	*,R5	base for test data and test routine	
00001DC8	00001E08			1197+T23	DC	A(X23)	address of test routine	
00001DCC	0017			1198+	DC	H'23'	test number	
00001DCE	00			1199+	DC	X'00'		
00001DCF	03			1200+	DC	HL1'3'	m4	
00001DD0	E5C5E2D3 E5404040			1201+	DC	CL8'VESLV'	instruction name	
00001DD8	00001E40			1202+	DC	A(RE23+16)	address of v2 source	
00001DDC	00001E50			1203+	DC	A(RE23+32)	address of v3 source	
00001DE0	00000010			1204+	DC	A(16)	result length	
00001DE4	00001E30			1205+REA23	DC	A(RE23)	result address	
00001DE8	00000000 00000000			1206+	DS	FD	gap	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001DF0	00000000 00000000			1207+V1023	DS	XL16	V1 output
00001DF8	00000000 00000000						
00001E00	00000000 00000000			1208+	DS	FD	gap
				1209+*			
00001E08				1210+X23	DS	0F	
00001E08	E310 5010 0014		00000010	1211+	LGF	R1,V2ADDR	load v2 source
00001E0E	E761 0000 0806		00000000	1212+	VL	v22,0(R1)	use v22 to test decoder
00001E14	E310 5014 0014		00000014	1213+	LGF	R1,V3ADDR	load v3 source
00001E1A	E771 0000 0806		00000000	1214+	VL	v23,0(R1)	use v23 to test decoder
00001E20	E766 7000 3E70			1215+	VESLV	V22,V22,V23,3	test instruction (dest is a source)
00001E26	E760 5028 080E		00001DF0	1216+	VST	V22,V1023	save v1 output
00001E2C	07FB			1217+	BR	R11	return
00001E30				1218+RE23	DC	0F	xl16 expected result
00001E30				1219+	DROP	R5	
00001E30	FFFFFFFC 00000000			1220	DC	XL16'FFFFFFFC00000000 FFF8000000000000'	result
00001E38	FFF80000 00000000						
00001E40	FFFFFFFF FFFFFFFF			1221	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00001E48	FFFFFFFF FFFFFFFF						
00001E50	F0000000 00000022			1222	DC	XL16'F000000000000022 F000000000000033'	v3
00001E58	F0000000 00000033						
				1223			

```
  LOC         OBJECT CODE      ADDR1      ADDR2      STMT

                                                     1225 *----------------------------------------------------------------
                                                     1226 *    VESRLV - Vector Element Shift Right Logical Vector
                                                     1227 *----------------------------------------------------------------
                                                     1228 *Byte
                                                     1229           VRR_C VESRLV,0
00001E60                                             1230+          DS    0FD
00001E60                            00001E60         1231+          USING *,R5                base for test data and test routine
00001E60   00001EA0                                  1232+T24       DC    A(X24)              address of test routine
00001E64   0018                                      1233+          DC    H'24'               test number
00001E66   00                                        1234+          DC    X'00'
00001E67   00                                        1235+          DC    HL1'0'              m4
00001E68   E5C5E2D9 D3E54040                          1236+         DC    CL8'VESRLV'         instruction name
00001E70   00001ED8                                  1237+          DC    A(RE24+16)          address of v2 source
00001E74   00001EE8                                  1238+          DC    A(RE24+32)          address of v3 source
00001E78   00000010                                  1239+          DC    A(16)               result length
00001E7C   00001EC8                                  1240+REA24     DC    A(RE24)             result address
00001E80   00000000 00000000                          1241+         DS    FD                  gap
00001E88   00000000 00000000                          1242+V1024    DS    XL16                V1 output
00001E90   00000000 00000000
00001E98   00000000 00000000                          1243+         DS    FD                  gap
                                                     1244+*
00001EA0                                             1245+X24       DS    0F
00001EA0   E310 5010 0014                  00000010  1246+          LGF   R1,V2ADDR           load v2 source
00001EA6   E761 0000 0806                  00000000  1247+          VL    v22,0(R1)           use v22 to test decoder
00001EAC   E310 5014 0014                  00000014  1248+          LGF   R1,V3ADDR           load v3 source
00001EB2   E771 0000 0806                  00000000  1249+          VL    v23,0(R1)           use v23 to test decoder
00001EB8   E766 7000 0E78                            1250+          VESRLV V22,V22,V23,0       test instruction (dest is a source)
00001EBE   E760 5028 080E                  00001E88  1251+          VST   V22,V1024            save v1 output
00001EC4   07FB                                      1252+          BR    R11                 return
00001EC8                                             1253+RE24      DC    0F                  xl16 expected result
00001EC8                                             1254+          DROP  R5
00001EC8   80402010 08040201                          1255         DC    XL16'8040201008040201 8040201008040201'    result
00001ED0   80402010 08040201
00001ED8   80808080 80808080                          1256         DC    XL16'8080808080808080 8080808080808080'    v2
00001EE0   80808080 80808080
00001EE8   00010203 04050607                          1257         DC    XL16'0001020304050607 08090A0B0C0D0E0F'    v3
00001EF0   08090A0B 0C0D0E0F
                                                     1258
                                                     1259           VRR_C VESRLV,0
00001EF8                                             1260+          DS    0FD
00001EF8                            00001EF8         1261+          USING *,R5                base for test data and test routine
00001EF8   00001F38                                  1262+T25       DC    A(X25)              address of test routine
00001EFC   0019                                      1263+          DC    H'25'               test number
00001EFE   00                                        1264+          DC    X'00'
00001EFF   00                                        1265+          DC    HL1'0'              m4
00001F00   E5C5E2D9 D3E54040                          1266+         DC    CL8'VESRLV'         instruction name
00001F08   00001F70                                  1267+          DC    A(RE25+16)          address of v2 source
00001F0C   00001F80                                  1268+          DC    A(RE25+32)          address of v3 source
00001F10   00000010                                  1269+          DC    A(16)               result length
00001F14   00001F60                                  1270+REA25     DC    A(RE25)             result address
00001F18   00000000 00000000                          1271+         DS    FD                  gap
00001F20   00000000 00000000                          1272+V1025    DS    XL16                V1 output
00001F28   00000000 00000000
00001F30   00000000 00000000                          1273+         DS    FD                  gap
                                                     1274+*
00001F38                                             1275+X25       DS    0F
```

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00001F38  E310 5010 0014              00000010  1276+        LGF     R1,V2ADDR           load v2 source
00001F3E  E761 0000 0806              00000000  1277+        VL      v22,0(R1)           use v22 to test decoder
00001F44  E310 5014 0014              00000014  1278+        LGF     R1,V3ADDR           load v3 source
00001F4A  E771 0000 0806              00000000  1279+        VL      v23,0(R1)           use v23 to test decoder
00001F50  E766 7000 0E78                        1280+        VESRLV  V22,V22,V23,0        test instruction (dest is a source)
00001F56  E760 5028 080E              00001F20  1281+        VST     V22,V1025            save v1 output
00001F5C  07FB                                  1282+        BR      R11                 return
00001F60                                        1283+RE25    DC      0F                  xl16 expected result
00001F60                                        1284+        DROP    R5
00001F60  FF7F3F1F 0F070301                     1285         DC      XL16'FF7F3F1F0F070301 FF7F3F1F0F070301'     result
00001F68  FF7F3F1F 0F070301
00001F70  FFFFFFFF FFFFFFFF                     1286         DC      XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'     v2
00001F78  FFFFFFFF FFFFFFFF
00001F80  00010203 04050607                     1287         DC      XL16'0001020304050607 08090A0B0C0D0E0F'     v3
00001F88  08090A0B 0C0D0E0F
                                                1288
                                                1289         VRR_C VESRLV,0
00001F90                                        1290+        DS      0FD
00001F90                            00001F90    1291+        USING   *,R5                base for test data and test routine
00001F90  00001FD0                              1292+T26     DC      A(X26)              address of test routine
00001F94  001A                                  1293+        DC      H'26'               test number
00001F96  00                                    1294+        DC      X'00'
00001F97  00                                    1295+        DC      HL1'0'              m4
00001F98  E5C5E2D9 D3E54040                     1296+        DC      CL8'VESRLV'         instruction name
00001FA0  00002008                              1297+        DC      A(RE26+16)          address of v2 source
00001FA4  00002018                              1298+        DC      A(RE26+32)          address of v3 source
00001FA8  00000010                              1299+        DC      A(16)               result length
00001FAC  00001FF8                              1300+REA26   DC      A(RE26)             result address
00001FB0  00000000 00000000                     1301+        DS      FD                  gap
00001FB8  00000000 00000000                     1302+V1026   DS      XL16                V1 output
00001FC0  00000000 00000000
00001FC8  00000000 00000000                     1303+        DS      FD                  gap
                                                1304+*
00001FD0                                        1305+X26     DS      0F
00001FD0  E310 5010 0014              00000010  1306+        LGF     R1,V2ADDR           load v2 source
00001FD6  E761 0000 0806              00000000  1307+        VL      v22,0(R1)           use v22 to test decoder
00001FDC  E310 5014 0014              00000014  1308+        LGF     R1,V3ADDR           load v3 source
00001FE2  E771 0000 0806              00000000  1309+        VL      v23,0(R1)           use v23 to test decoder
00001FE8  E766 7000 0E78                        1310+        VESRLV  V22,V22,V23,0        test instruction (dest is a source)
00001FEE  E760 5028 080E              00001FB8  1311+        VST     V22,V1026            save v1 output
00001FF4  07FB                                  1312+        BR      R11                 return
00001FF8                                        1313+RE26    DC      0F                  xl16 expected result
00001FF8                                        1314+        DROP    R5
00001FF8  80402010 08040201                     1315         DC      XL16'8040201008040201 8040201008040201'     result
00002000  80402010 08040201
00002008  80808080 80808080                     1316         DC      XL16'8080808080808080 8080808080808080'     v2
00002010  80808080 80808080
00002018  F0F1F2F3 F4F5F6F7                     1317         DC      XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'     v3
00002020  F8F9FAFB FCFDFEFF
                                                1318
                                                1319         VRR_C VESRLV,0
00002028                                        1320+        DS      0FD
00002028                            00002028    1321+        USING   *,R5                base for test data and test routine
00002028  00002068                              1322+T27     DC      A(X27)              address of test routine
0000202C  001B                                  1323+        DC      H'27'               test number
0000202E  00                                    1324+        DC      X'00'
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000202F	00			1325+	DC	HL1'0'	m4
00002030	E5C5E2D9 D3E54040			1326+	DC	CL8'VESRLV'	instruction name
00002038	000020A0			1327+	DC	A(RE27+16)	address of v2 source
0000203C	000020B0			1328+	DC	A(RE27+32)	address of v3 source
00002040	00000010			1329+	DC	A(16)	result length
00002044	00002090			1330+REA27	DC	A(RE27)	result address
00002048	00000000 00000000			1331+	DS	FD	gap
00002050	00000000 00000000			1332+V1027	DS	XL16	V1 output
00002058	00000000 00000000						
00002060	00000000 00000000			1333+	DS	FD	gap
				1334+*			
00002068				1335+X27	DS	0F	
00002068	E310 5010 0014		00000010	1336+	LGF	R1,V2ADDR	load v2 source
0000206E	E761 0000 0806		00000000	1337+	VL	v22,0(R1)	use v22 to test decoder
00002074	E310 5014 0014		00000014	1338+	LGF	R1,V3ADDR	load v3 source
0000207A	E771 0000 0806		00000000	1339+	VL	v23,0(R1)	use v23 to test decoder
00002080	E766 7000 0E78			1340+	VESRLV V22,V22,V23,0		test instruction (dest is a source)
00002086	E760 5028 080E		00002050	1341+	VST	V22,V1027	save v1 output
0000208C	07FB			1342+	BR	R11	return
00002090				1343+RE27	DC	0F	xl16 expected result
00002090				1344+	DROP	R5	
00002090	FF7F3F1F 0F070301			1345	DC	XL16'FF7F3F1F0F070301 FF7F3F1F0F070301'	result
00002098	FF7F3F1F 0F070301						
000020A0	FFFFFFFF FFFFFFFF			1346	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
000020A8	FFFFFFFF FFFFFFFF						
000020B0	F0F1F2F3 F4F5F6F7			1347	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	v3
000020B8	F8F9FAFB FCFDFEFF						
				1348			
				1349 *Halfword			
				1350	VRR_C VESRLV,1		
000020C0				1351+	DS	0FD	
000020C0			000020C0	1352+	USING	*,R5	base for test data and test routine
000020C0	00002100			1353+T28	DC	A(X28)	address of test routine
000020C4	001C			1354+	DC	H'28'	test number
000020C6	00			1355+	DC	X'00'	
000020C7	01			1356+	DC	HL1'1'	m4
000020C8	E5C5E2D9 D3E54040			1357+	DC	CL8'VESRLV'	instruction name
000020D0	00002138			1358+	DC	A(RE28+16)	address of v2 source
000020D4	00002148			1359+	DC	A(RE28+32)	address of v3 source
000020D8	00000010			1360+	DC	A(16)	result length
000020DC	00002128			1361+REA28	DC	A(RE28)	result address
000020E0	00000000 00000000			1362+	DS	FD	gap
000020E8	00000000 00000000			1363+V1028	DS	XL16	V1 output
000020F0	00000000 00000000						
000020F8	00000000 00000000			1364+	DS	FD	gap
				1365+*			
00002100				1366+X28	DS	0F	
00002100	E310 5010 0014		00000010	1367+	LGF	R1,V2ADDR	load v2 source
00002106	E761 0000 0806		00000000	1368+	VL	v22,0(R1)	use v22 to test decoder
0000210C	E310 5014 0014		00000014	1369+	LGF	R1,V3ADDR	load v3 source
00002112	E771 0000 0806		00000000	1370+	VL	v23,0(R1)	use v23 to test decoder
00002118	E766 7000 1E78			1371+	VESRLV V22,V22,V23,1		test instruction (dest is a source)
0000211E	E760 5028 080E		000020E8	1372+	VST	V22,V1028	save v1 output
00002124	07FB			1373+	BR	R11	return
00002128				1374+RE28	DC	0F	xl16 expected result
00002128				1375+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002128	80004000 20001000			1376	DC	XL16'8000400020001000 0800040002000100'		result
00002130	08000400 02000100							
00002138	80008000 80008000			1377	DC	XL16'8000800080008000 8000800080008000'		v2
00002140	80008000 80008000							
00002148	00000001 00020003			1378	DC	XL16'0000000100020003 0004000500060007'		v3
00002150	00040005 00060007							
				1379				
				1380	VRR_C	VESRLV, 1		
00002158				1381+	DS	0FD		
00002158		00002158		1382+	USING	*,R5	base for test data and test routine	
00002158	00002198			1383+T29	DC	A(X29)	address of test routine	
0000215C	001D			1384+	DC	H'29'	test number	
0000215E	00			1385+	DC	X'00'		
0000215F	01			1386+	DC	HL1'1'	m4	
00002160	E5C5E2D9 D3E54040			1387+	DC	CL8'VESRLV'	instruction name	
00002168	000021D0			1388+	DC	A(RE29+16)	address of v2 source	
0000216C	000021E0			1389+	DC	A(RE29+32)	address of v3 source	
00002170	00000010			1390+	DC	A(16)	result length	
00002174	000021C0			1391+REA29	DC	A(RE29)	result address	
00002178	00000000 00000000			1392+	DS	FD	gap	
00002180	00000000 00000000			1393+V1029	DS	XL16	V1 output	
00002188	00000000 00000000							
00002190	00000000 00000000			1394+	DS	FD	gap	
				1395+*				
00002198				1396+X29	DS	0F		
00002198	E310 5010 0014		00000010	1397+	LGF	R1,V2ADDR	load v2 source	
0000219E	E761 0000 0806		00000000	1398+	VL	v22,0(R1)	use v22 to test decoder	
000021A4	E310 5014 0014		00000014	1399+	LGF	R1,V3ADDR	load v3 source	
000021AA	E771 0000 0806		00000000	1400+	VL	v23,0(R1)	use v23 to test decoder	
000021B0	E766 7000 1E78			1401+	VESRLV	V22,V22,V23,1	test instruction (dest is a source)	
000021B6	E760 5028 080E		00002180	1402+	VST	V22,V1029	save v1 output	
000021BC	07FB			1403+	BR	R11	return	
000021C0				1404+RE29	DC	0F	xl16 expected result	
000021C0				1405+	DROP	R5		
000021C0	00800040 00200010			1406	DC	XL16'0080004000200010 0008000400020001'		result
000021C8	00080004 00020001							
000021D0	80008000 80008000			1407	DC	XL16'8000800080008000 8000800080008000'		v2
000021D8	80008000 80008000							
000021E0	00080009 000A000B			1408	DC	XL16'00080009000A000B 000C000D000E000F'		v3
000021E8	000C000D 000E000F							
				1409				
				1410	VRR_C	VESRLV, 1		
000021F0				1411+	DS	0FD		
000021F0		000021F0		1412+	USING	*,R5	base for test data and test routine	
000021F0	00002230			1413+T30	DC	A(X30)	address of test routine	
000021F4	001E			1414+	DC	H'30'	test number	
000021F6	00			1415+	DC	X'00'		
000021F7	01			1416+	DC	HL1'1'	m4	
000021F8	E5C5E2D9 D3E54040			1417+	DC	CL8'VESRLV'	instruction name	
00002200	00002268			1418+	DC	A(RE30+16)	address of v2 source	
00002204	00002278			1419+	DC	A(RE30+32)	address of v3 source	
00002208	00000010			1420+	DC	A(16)	result length	
0000220C	00002258			1421+REA30	DC	A(RE30)	result address	
00002210	00000000 00000000			1422+	DS	FD	gap	
00002218	00000000 00000000			1423+V1030	DS	XL16	V1 output	
00002220	00000000 00000000							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002228	00000000 00000000			1424+	DS	FD	gap
				1425+*			
00002230				1426+X30	DS	0F	
00002230	E310 5010 0014		00000010	1427+	LGF	R1,V2ADDR	load v2 source
00002236	E761 0000 0806		00000000	1428+	VL	v22,0(R1)	use v22 to test decoder
0000223C	E310 5014 0014		00000014	1429+	LGF	R1,V3ADDR	load v3 source
00002242	E771 0000 0806		00000000	1430+	VL	v23,0(R1)	use v23 to test decoder
00002248	E766 7000 1E78			1431+	VESRLV V22,V22,V23,1		test instruction (dest is a source)
0000224E	E760 A018 080E		00002218	1432+	VST	V22,V1030	save v1 output
00002254	07FB			1433+	BR	R11	return
00002258				1434+RE30	DC	0F	xl16 expected result
00002258				1435+	DROP	R5	
00002258	FFFF7FFF 3FFF1FFF			1436	DC	XL16'FFFF7FFF3FFF1FFF 0FFF07FF03FF01FF'	result
00002260	0FFF07FF 03FF01FF						
00002268	FFFFFFFF FFFFFFFF			1437	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00002270	FFFFFFFF FFFFFFFF						
00002278	00000001 00020003			1438	DC	XL16'0000000100020003 0004000500060007'	v3
00002280	00040005 00060007						
				1439			
				1440	VRR_C VESRLV,1		
00002288				1441+	DS	0FD	
00002288		00002288		1442+	USING *,R5		base for test data and test routine
00002288	000022C8			1443+T31	DC	A(X31)	address of test routine
0000228C	001F			1444+	DC	H'31'	test number
0000228E	00			1445+	DC	X'00'	
0000228F	01			1446+	DC	HL1'1'	m4
00002290	E5C5E2D9 D3E54040			1447+	DC	CL8'VESRLV'	instruction name
00002298	00002300			1448+	DC	A(RE31+16)	address of v2 source
0000229C	00002310			1449+	DC	A(RE31+32)	address of v3 source
000022A0	00000010			1450+	DC	A(16)	result length
000022A4	000022F0			1451+REA31	DC	A(RE31)	result address
000022A8	00000000 00000000			1452+	DS	FD	gap
000022B0	00000000 00000000			1453+V1031	DS	XL16	V1 output
000022B8	00000000 00000000						
000022C0	00000000 00000000			1454+	DS	FD	gap
				1455+*			
000022C8				1456+X31	DS	0F	
000022C8	E310 5010 0014		00000010	1457+	LGF	R1,V2ADDR	load v2 source
000022CE	E761 0000 0806		00000000	1458+	VL	v22,0(R1)	use v22 to test decoder
000022D4	E310 5014 0014		00000014	1459+	LGF	R1,V3ADDR	load v3 source
000022DA	E771 0000 0806		00000000	1460+	VL	v23,0(R1)	use v23 to test decoder
000022E0	E766 7000 1E78			1461+	VESRLV V22,V22,V23,1		test instruction (dest is a source)
000022E6	E760 5028 080E		000022B0	1462+	VST	V22,V1031	save v1 output
000022EC	07FB			1463+	BR	R11	return
000022F0				1464+RE31	DC	0F	xl16 expected result
000022F0				1465+	DROP	R5	
000022F0	00FF007F 003F001F			1466	DC	XL16'00FF007F003F001F 000F000700030001'	result
000022F8	000F0007 00030001						
00002300	FFFFFFFF FFFFFFFF			1467	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00002308	FFFFFFFF FFFFFFFF						
00002310	00080009 000A000B			1468	DC	XL16'00080009000A000B 000C000D000E000F'	v3
00002318	000C000D 000E000F						
				1469			
				1470	VRR_C VESRLV,1		
00002320				1471+	DS	0FD	
00002320		00002320		1472+	USING *,R5		base for test data and test routine

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00002320   00002360                              1473+T32     DC      A(X32)             address of test routine
00002324   0020                                  1474+        DC      H'32'              test number
00002326   00                                    1475+        DC      X'00'
00002327   01                                    1476+        DC      HL1'1'             m4
00002328   E5C5E2D9 D3E54040                      1477+        DC      CL8'VESRLV'        instruction name
00002330   00002398                              1478+        DC      A(RE32+16)         address of v2 source
00002334   000023A8                              1479+        DC      A(RE32+32)         address of v3 source
00002338   00000010                              1480+        DC      A(16)              result length
0000233C   00002388                              1481+REA32   DC      A(RE32)            result address
00002340   00000000 00000000                      1482+        DS      FD                 gap
00002348   00000000 00000000                      1483+V1032   DS      XL16               V1 output
00002350   00000000 00000000
00002358   00000000 00000000                      1484+        DS      FD                 gap
                                                  1485+*
00002360                                          1486+X32     DS      0F
00002360   E310 5010 0014            00000010     1487+        LGF     R1,V2ADDR          load v2 source
00002366   E761 0000 0806            00000000     1488+        VL      v22,0(R1)          use v22 to test decoder
0000236C   E310 5014 0014            00000014     1489+        LGF     R1,V3ADDR          load v3 source
00002372   E771 0000 0806            00000000     1490+        VL      v23,0(R1)          use v23 to test decoder
00002378   E766 7000 1E78                         1491+        VESRLV  V22,V22,V23,1       test instruction (dest is a source)
0000237E   E760 5028 080E            00002348     1492+        VST     V22,V1032          save v1 output
00002384   07FB                                   1493+        BR      R11                return
00002388                                          1494+RE32    DC      0F                 xl16 expected result
00002388                                          1495+        DROP    R5
00002388   80004000 20001000                      1496         DC      XL16'8000400020001000 0800040002000100'    result
00002390   08000400 02000100
00002398   80008000 80008000                      1497         DC      XL16'8000800080008000 8000800080008000'    v2
000023A0   80008000 80008000
000023A8   F000F001 F002F003                      1498         DC      XL16'F000F001F002F003 F004F005F006F007'    v3
000023B0   F004F005 F006F007
                                                  1499
                                                  1500         VRR_C   VESRLV,1
000023B8                                          1501+        DS      0FD
000023B8                    000023B8              1502+        USING   *,R5               base for test data and test routine
000023B8   000023F8                              1503+T33     DC      A(X33)             address of test routine
000023BC   0021                                   1504+        DC      H'33'              test number
000023BE   00                                     1505+        DC      X'00'
000023BF   01                                     1506+        DC      HL1'1'             m4
000023C0   E5C5E2D9 D3E54040                      1507+        DC      CL8'VESRLV'        instruction name
000023C8   00002430                              1508+        DC      A(RE33+16)         address of v2 source
000023CC   00002440                              1509+        DC      A(RE33+32)         address of v3 source
000023D0   00000010                              1510+        DC      A(16)              result length
000023D4   00002420                              1511+REA33   DC      A(RE33)            result address
000023D8   00000000 00000000                      1512+        DS      FD                 gap
000023E0   00000000 00000000                      1513+V1033   DS      XL16               V1 output
000023E8   00000000 00000000
000023F0   00000000 00000000                      1514+        DS      FD                 gap
                                                  1515+*
000023F8                                          1516+X33     DS      0F
000023F8   E310 5010 0014            00000010     1517+        LGF     R1,V2ADDR          load v2 source
000023FE   E761 0000 0806            00000000     1518+        VL      v22,0(R1)          use v22 to test decoder
00002404   E310 5014 0014            00000014     1519+        LGF     R1,V3ADDR          load v3 source
0000240A   E771 0000 0806            00000000     1520+        VL      v23,0(R1)          use v23 to test decoder
00002410   E766 7000 1E78                         1521+        VESRLV  V22,V22,V23,1       test instruction (dest is a source)
00002416   E760 5028 080E            000023E0     1522+        VST     V22,V1033          save v1 output
0000241C   07FB                                   1523+        BR      R11                return
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002420				1524+RE33	DC	0F	xl16 expected result	
00002420				1525+	DROP	R5		
00002420	FFFF7FFF 3FFF1FFF			1526	DC	XL16'FFFF7FFF3FFF1FFF 0FFF07FF03FF01FF'		result
00002428	0FFF07FF 03FF01FF							
00002430	FFFFFFFF FFFFFFFF			1527	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'		v2
00002438	FFFFFFFF FFFFFFFF							
00002440	F000F001 F002F003			1528	DC	XL16'F000F001F002F003 F004F005F006F007'		v3
00002448	F004F005 F006F007							
				1529				
				1530 *Word				
				1531	VRR_C	VESRLV, 2		
00002450				1532+	DS	0FD		
00002450		00002450		1533+	USING	*, R5	base for test data and test routine	
00002450	00002490			1534+T34	DC	A(X34)	address of test routine	
00002454	0022			1535+	DC	H'34'	test number	
00002456	00			1536+	DC	X'00'		
00002457	02			1537+	DC	HL1'2'	m4	
00002458	E5C5E2D9 D3E54040			1538+	DC	CL8'VESRLV'	instruction name	
00002460	000024C8			1539+	DC	A(RE34+16)	address of v2 source	
00002464	000024D8			1540+	DC	A(RE34+32)	address of v3 source	
00002468	00000010			1541+	DC	A(16)	result length	
0000246C	000024B8			1542+REA34	DC	A(RE34)	result address	
00002470	00000000 00000000			1543+	DS	FD	gap	
00002478	00000000 00000000			1544+V1034	DS	XL16	V1 output	
00002480	00000000 00000000							
00002488	00000000 00000000			1545+	DS	FD	gap	
				1546+*				
00002490				1547+X34	DS	0F		
00002490	E310 5010 0014		00000010	1548+	LGF	R1, V2ADDR	load v2 source	
00002496	E761 0000 0806		00000000	1549+	VL	v22, 0(R1)	use v22 to test decoder	
0000249C	E310 5014 0014		00000014	1550+	LGF	R1, V3ADDR	load v3 source	
000024A2	E771 0000 0806		00000000	1551+	VL	v23, 0(R1)	use v23 to test decoder	
000024A8	E766 7000 2E78			1552+	VESRLV	V22, V22, V23, 2	test instruction (dest is a source)	
000024AE	E760 5028 080E		00002478	1553+	VST	V22, V1034	save v1 output	
000024B4	07FB			1554+	BR	R11	return	
000024B8				1555+RE34	DC	0F	xl16 expected result	
000024B8				1556+	DROP	R5		
000024B8	80000000 40000000			1557	DC	XL16'8000000040000000 2000000010000000'		result
000024C0	20000000 10000000							
000024C8	80000000 80000000			1558	DC	XL16'8000000080000000 8000000080000000'		v2
000024D0	80000000 80000000							
000024D8	00000000 00000001			1559	DC	XL16'0000000000000001 0000000200000003'		v3
000024E0	00000002 00000003							
				1560				
				1561	VRR_C	VESRLV, 2		
000024E8				1562+	DS	0FD		
000024E8		000024E8		1563+	USING	*, R5	base for test data and test routine	
000024E8	00002528			1564+T35	DC	A(X35)	address of test routine	
000024EC	0023			1565+	DC	H'35'	test number	
000024EE	00			1566+	DC	X'00'		
000024EF	02			1567+	DC	HL1'2'	m4	
000024F0	E5C5E2D9 D3E54040			1568+	DC	CL8'VESRLV'	instruction name	
000024F8	00002560			1569+	DC	A(RE35+16)	address of v2 source	
000024FC	00002570			1570+	DC	A(RE35+32)	address of v3 source	
00002500	00000010			1571+	DC	A(16)	result length	
00002504	00002550			1572+REA35	DC	A(RE35)	result address	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002508	00000000 00000000			1573+	DS	FD	gap
00002510	00000000 00000000			1574+V1035	DS	XL16	V1 output
00002518	00000000 00000000						
00002520	00000000 00000000			1575+	DS	FD	gap
				1576+*			
00002528				1577+X35	DS	0F	
00002528	E310 5010 0014		00000010	1578+	LGF	R1,V2ADDR	load v2 source
0000252E	E761 0000 0806		00000000	1579+	VL	v22,0(R1)	use v22 to test decoder
00002534	E310 5014 0014		00000014	1580+	LGF	R1,V3ADDR	load v3 source
0000253A	E771 0000 0806		00000000	1581+	VL	v23,0(R1)	use v23 to test decoder
00002540	E766 7000 2E78			1582+	VESRLV	V22,V22,V23,2	test instruction (dest is a source)
00002546	E760 5028 080E		00002510	1583+	VST	V22,V1035	save v1 output
0000254C	07FB			1584+	BR	R11	return
00002550				1585+RE35	DC	0F	xl16 expected result
00002550				1586+	DROP	R5	
00002550	00800000 00400000			1587	DC	XL16'0080000000400000 0020000000100000'	result
00002558	00200000 00100000						
00002560	80000000 80000000			1588	DC	XL16'8000000080000000 8000000080000000'	v2
00002568	80000000 80000000						
00002570	00000008 00000009			1589	DC	XL16'0000000800000009 0000000A0000000B'	v3
00002578	0000000A 0000000B						
				1590			
				1591	VRR_C	VESRLV,2	
00002580				1592+	DS	0FD	
00002580		00002580		1593+	USING	*,R5	base for test data and test routine
00002580	000025C0			1594+T36	DC	A(X36)	address of test routine
00002584	0024			1595+	DC	H'36'	test number
00002586	00			1596+	DC	X'00'	
00002587	02			1597+	DC	HL1'2'	m4
00002588	E5C5E2D9 D3E54040			1598+	DC	CL8'VESRLV'	instruction name
00002590	000025F8			1599+	DC	A(RE36+16)	address of v2 source
00002594	00002608			1600+	DC	A(RE36+32)	address of v3 source
00002598	00000010			1601+	DC	A(16)	result length
0000259C	000025E8			1602+REA36	DC	A(RE36)	result address
000025A0	00000000 00000000			1603+	DS	FD	gap
000025A8	00000000 00000000			1604+V1036	DS	XL16	V1 output
000025B0	00000000 00000000						
000025B8	00000000 00000000			1605+	DS	FD	gap
				1606+*			
000025C0				1607+X36	DS	0F	
000025C0	E310 5010 0014		00000010	1608+	LGF	R1,V2ADDR	load v2 source
000025C6	E761 0000 0806		00000000	1609+	VL	v22,0(R1)	use v22 to test decoder
000025CC	E310 5014 0014		00000014	1610+	LGF	R1,V3ADDR	load v3 source
000025D2	E771 0000 0806		00000000	1611+	VL	v23,0(R1)	use v23 to test decoder
000025D8	E766 7000 2E78			1612+	VESRLV	V22,V22,V23,2	test instruction (dest is a source)
000025DE	E760 5028 080E		000025A8	1613+	VST	V22,V1036	save v1 output
000025E4	07FB			1614+	BR	R11	return
000025E8				1615+RE36	DC	0F	xl16 expected result
000025E8				1616+	DROP	R5	
000025E8	FFFFFFFF 7FFFFFFF			1617	DC	XL16'FFFFFFFF7FFFFFFF 3FFFFFFF1FFFFFFF'	result
000025F0	3FFFFFFF 1FFFFFFF						
000025F8	FFFFFFFF FFFFFFFF			1618	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00002600	FFFFFFFF FFFFFFFF						
00002608	00000000 00000001			1619	DC	XL16'0000000000000001 0000000200000003'	v3
00002610	00000002 00000003						
				1620			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				1621		VRR_C VESRLV, 2	
00002618				1622+	DS	0FD	
00002618		00002618		1623+	USING	*, R5	base for test data and test routine
00002618	00002658			1624+T37	DC	A(X37)	address of test routine
0000261C	0025			1625+	DC	H' 37'	test number
0000261E	00			1626+	DC	X' 00'	
0000261F	02			1627+	DC	HL1' 2'	m4
00002620	E5C5E2D9 D3E54040			1628+	DC	CL8' VESRLV'	instruction name
00002628	00002690			1629+	DC	A(RE37+16)	address of v2 source
0000262C	000026A0			1630+	DC	A(RE37+32)	address of v3 source
00002630	00000010			1631+	DC	A(16)	result length
00002634	00002680			1632+REA37	DC	A(RE37)	result address
00002638	00000000 00000000			1633+	DS	FD	gap
00002640	00000000 00000000			1634+V1037	DS	XL16	V1 output
00002648	00000000 00000000						
00002650	00000000 00000000			1635+	DS	FD	gap
				1636+*			
00002658				1637+X37	DS	0F	
00002658	E310 5010 0014		00000010	1638+	LGF	R1, V2ADDR	load v2 source
0000265E	E761 0000 0806		00000000	1639+	VL	v22, 0(R1)	use v22 to test decoder
00002664	E310 5014 0014		00000014	1640+	LGF	R1, V3ADDR	load v3 source
0000266A	E771 0000 0806		00000000	1641+	VL	v23, 0(R1)	use v23 to test decoder
00002670	E766 7000 2E78			1642+		VESRLV V22, V22, V23, 2	test instruction (dest is a source)
00002676	E760 5028 080E		00002640	1643+	VST	V22, V1037	save v1 output
0000267C	07FB			1644+	BR	R11	return
00002680				1645+RE37	DC	0F	xl16 expected result
00002680				1646+	DROP	R5	
00002680	00FFFFFF 007FFFFF			1647	DC	XL16' 00FFFFFF007FFFFF 003FFFFF001FFFFF'	result
00002688	003FFFFF 001FFFFF						
00002690	FFFFFFFF FFFFFFFF			1648	DC	XL16' FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00002698	FFFFFFFF FFFFFFFF						
000026A0	00000008 00000009			1649	DC	XL16' 0000000800000009 0000000A0000000B'	v3
000026A8	0000000A 0000000B						
				1650			
				1651		VRR_C VESRLV, 2	
000026B0				1652+	DS	0FD	
000026B0		000026B0		1653+	USING	*, R5	base for test data and test routine
000026B0	000026F0			1654+T38	DC	A(X38)	address of test routine
000026B4	0026			1655+	DC	H' 38'	test number
000026B6	00			1656+	DC	X' 00'	
000026B7	02			1657+	DC	HL1' 2'	m4
000026B8	E5C5E2D9 D3E54040			1658+	DC	CL8' VESRLV'	instruction name
000026C0	00002728			1659+	DC	A(RE38+16)	address of v2 source
000026C4	00002738			1660+	DC	A(RE38+32)	address of v3 source
000026C8	00000010			1661+	DC	A(16)	result length
000026CC	00002718			1662+REA38	DC	A(RE38)	result address
000026D0	00000000 00000000			1663+	DS	FD	gap
000026D8	00000000 00000000			1664+V1038	DS	XL16	V1 output
000026E0	00000000 00000000						
000026E8	00000000 00000000			1665+	DS	FD	gap
				1666+*			
000026F0				1667+X38	DS	0F	
000026F0	E310 5010 0014		00000010	1668+	LGF	R1, V2ADDR	load v2 source
000026F6	E761 0000 0806		00000000	1669+	VL	v22, 0(R1)	use v22 to test decoder
000026FC	E310 5014 0014		00000014	1670+	LGF	R1, V3ADDR	load v3 source
00002702	E771 0000 0806		00000000	1671+	VL	v23, 0(R1)	use v23 to test decoder

```
  LOC          OBJECT CODE       ADDR1     ADDR2     STMT

00002708  E766 7000 2E78                             1672+            VESRLV V22,V22,V23,2      test instruction (dest is a source)
0000270E  E760 5028 080E                   000026D8  1673+            VST    V22,V1038         save v1 output
00002714  07FB                                       1674+            BR     R11               return
00002718                                             1675+RE38        DC     0F                xl16 expected result
00002718                                             1676+            DROP   R5
00002718  80000000 40000000                          1677             DC     XL16'8000000040000000 2000000010000000'    result
00002720  20000000 10000000
00002728  80000000 80000000                          1678             DC     XL16'8000000080000000 8000000080000000'    v2
00002730  80000000 80000000
00002738  F0000000 F0000001                          1679             DC     XL16'F0000000F0000001 F0000002F0000003'    v3
00002740  F0000002 F0000003
                                                     1680
                                                     1681             VRR_C  VESRLV,2
00002748                                             1682+            DS     0FD
00002748                             00002748        1683+            USING  *,R5              base for test data and test routine
00002748  00002788                                   1684+T39         DC     A(X39)            address of test routine
0000274C  0027                                       1685+            DC     H'39'             test number
0000274E  00                                         1686+            DC     X'00'
0000274F  02                                         1687+            DC     HL1'2'            m4
00002750  E5C5E2D9 D3E54040                          1688+            DC     CL8'VESRLV'       instruction name
00002758  000027C0                                   1689+            DC     A(RE39+16)        address of v2 source
0000275C  000027D0                                   1690+            DC     A(RE39+32)        address of v3 source
00002760  00000010                                   1691+            DC     A(16)             result length
00002764  000027B0                                   1692+REA39       DC     A(RE39)           result address
00002768  00000000 00000000                          1693+            DS     FD                gap
00002770  00000000 00000000                          1694+V1039       DS     XL16              V1 output
00002778  00000000 00000000
00002780  00000000 00000000                          1695+            DS     FD                gap
                                                     1696+*
00002788                                             1697+X39         DS     0F
00002788  E310 5010 0014          00000010           1698+            LGF    R1,V2ADDR         load v2 source
0000278E  E761 0000 0806          00000000           1699+            VL     v22,0(R1)         use v22 to test decoder
00002794  E310 5014 0014          00000014           1700+            LGF    R1,V3ADDR         load v3 source
0000279A  E771 0000 0806          00000000           1701+            VL     v23,0(R1)         use v23 to test decoder
000027A0  E766 7000 2E78                             1702+            VESRLV V22,V22,V23,2       test instruction (dest is a source)
000027A6  E760 5028 080E                   00002770  1703+            VST    V22,V1039          save v1 output
000027AC  07FB                                       1704+            BR     R11               return
000027B0                                             1705+RE39        DC     0F                xl16 expected result
000027B0                                             1706+            DROP   R5
000027B0  00FFFFFF 007FFFFF                          1707             DC     XL16'00FFFFFF007FFFFF 003FFFFF001FFFFF'    result
000027B8  003FFFFF 001FFFFF
000027C0  FFFFFFFF FFFFFFFF                          1708             DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v2
000027C8  FFFFFFFF FFFFFFFF
000027D0  F0000008 F0000009                          1709             DC     XL16'F0000008F0000009 F000000AF000000B'    v3
000027D8  F000000A F000000B
                                                     1710
                                                     1711 *Doubleword
                                                     1712             VRR_C  VESRLV,3
000027E0                                             1713+            DS     0FD
000027E0                             000027E0        1714+            USING  *,R5              base for test data and test routine
000027E0  00002820                                   1715+T40         DC     A(X40)            address of test routine
000027E4  0028                                       1716+            DC     H'40'             test number
000027E6  00                                         1717+            DC     X'00'
000027E7  03                                         1718+            DC     HL1'3'            m4
000027E8  E5C5E2D9 D3E54040                          1719+            DC     CL8'VESRLV'       instruction name
000027F0  00002858                                   1720+            DC     A(RE40+16)        address of v2 source
```

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  LOC        OBJECT CODE      ADDR1      ADDR2      STMT

000027F4   00002868                                 1721+           DC     A(RE40+32)        address of v3 source
000027F8   00000010                                 1722+           DC     A(16)             result length
000027FC   00002848                                 1723+REA40      DC     A(RE40)           result address
00002800   00000000 00000000                        1724+           DS     FD                gap
00002808   00000000 00000000                        1725+V1040      DS     XL16              V1 output
00002810   00000000 00000000
00002818   00000000 00000000                        1726+           DS     FD                gap
                                                    1727+*
00002820                                            1728+X40        DS     0F
00002820   E310 5010 0014              00000010     1729+           LGF    R1,V2ADDR         load v2 source
00002826   E761 0000 0806              00000000     1730+           VL     v22,0(R1)         use v22 to test decoder
0000282C   E310 5014 0014              00000014     1731+           LGF    R1,V3ADDR         load v3 source
00002832   E771 0000 0806              00000000     1732+           VL     v23,0(R1)         use v23 to test decoder
00002838   E766 7000 3E78                           1733+           VESRLV V22,V22,V23,3      test instruction (dest is a source)
0000283E   E760 5028 080E              00002808     1734+           VST    V22,V1040          save v1 output
00002844   07FB                                     1735+           BR     R11               return
00002848                                            1736+RE40       DC     0F                xl16 expected result
00002848                                            1737+           DROP   R5
00002848   80000000 00000000                        1738            DC     XL16'8000000000000000 4000000000000000'     result
00002850   40000000 00000000
00002858   80000000 00000000                        1739            DC     XL16'8000000000000000 8000000000000000'     v2
00002860   80000000 00000000
00002868   00000000 00000000                        1740            DC     XL16'0000000000000000 0000000000000001'     v3
00002870   00000000 00000001
                                                    1741
                                                    1742            VRR_C  VESRLV,3
00002878                                            1743+           DS     0FD
00002878                          00002878          1744+           USING  *,R5             base for test data and test routine
00002878   000028B8                                 1745+T41        DC     A(X41)            address of test routine
0000287C   0029                                     1746+           DC     H'41'             test number
0000287E   00                                       1747+           DC     X'00'
0000287F   03                                       1748+           DC     HL1'3'            m4
00002880   E5C5E2D9 D3E54040                        1749+           DC     CL8'VESRLV'       instruction name
00002888   000028F0                                 1750+           DC     A(RE41+16)        address of v2 source
0000288C   00002900                                 1751+           DC     A(RE41+32)        address of v3 source
00002890   00000010                                 1752+           DC     A(16)             result length
00002894   000028E0                                 1753+REA41      DC     A(RE41)           result address
00002898   00000000 00000000                        1754+           DS     FD                gap
000028A0   00000000 00000000                        1755+V1041      DS     XL16              V1 output
000028A8   00000000 00000000
000028B0   00000000 00000000                        1756+           DS     FD                gap
                                                    1757+*
000028B8                                            1758+X41        DS     0F
000028B8   E310 5010 0014              00000010     1759+           LGF    R1,V2ADDR         load v2 source
000028BE   E761 0000 0806              00000000     1760+           VL     v22,0(R1)         use v22 to test decoder
000028C4   E310 5014 0014              00000014     1761+           LGF    R1,V3ADDR         load v3 source
000028CA   E771 0000 0806              00000000     1762+           VL     v23,0(R1)         use v23 to test decoder
000028D0   E766 7000 3E78                           1763+           VESRLV V22,V22,V23,3      test instruction (dest is a source)
000028D6   E760 5028 080E              000028A0     1764+           VST    V22,V1041          save v1 output
000028DC   07FB                                     1765+           BR     R11               return
000028E0                                            1766+RE41       DC     0F                xl16 expected result
000028E0                                            1767+           DROP   R5
000028E0   00200000 00000000                        1768            DC     XL16'0020000000000000 0010000000000000'     result
000028E8   00100000 00000000
000028F0   80000000 00000000                        1769            DC     XL16'8000000000000000 8000000000000000'     v2
000028F8   80000000 00000000
```

```
  LOC          OBJECT CODE        ADDR1      ADDR2      STMT

00002900    00000000 0000000A                          1770            DC      XL16'000000000000000A 000000000000000B'     v3
00002908    00000000 0000000B

                                                        1771
                                                        1772            VRR_C VESRLV,3
00002910                                                1773+           DS      0FD
00002910                         00002910               1774+           USING *,R5                   base for test data and test routine
00002910    00002950                                    1775+T42        DC      A(X42)                address of test routine
00002914    002A                                        1776+           DC      H'42'                 test number
00002916    00                                          1777+           DC      X'00'
00002917    03                                          1778+           DC      HL1'3'                m4
00002918    E5C5E2D9 D3E54040                           1779+           DC      CL8'VESRLV'           instruction name
00002920    00002988                                    1780+           DC      A(RE42+16)            address of v2 source
00002924    00002998                                    1781+           DC      A(RE42+32)            address of v3 source
00002928    00000010                                    1782+           DC      A(16)                 result length
0000292C    00002978                                    1783+REA42      DC      A(RE42)               result address
00002930    00000000 00000000                           1784+           DS      FD                    gap
00002938    00000000 00000000                           1785+V1042      DS      XL16                  V1 output
00002940    00000000 00000000
00002948    00000000 00000000                           1786+           DS      FD                    gap
                                                        1787+*
00002950                                                1788+X42        DS      0F
00002950    E310 5010 0014                  00000010    1789+           LGF     R1,V2ADDR             load v2 source
00002956    E761 0000 0806                  00000000    1790+           VL      v22,0(R1)             use v22 to test decoder
0000295C    E310 5014 0014                  00000014    1791+           LGF     R1,V3ADDR             load v3 source
00002962    E771 0000 0806                  00000000    1792+           VL      v23,0(R1)             use v23 to test decoder
00002968    E766 7000 3E78                              1793+           VESRLV V22,V22,V23,3           test instruction (dest is a source)
0000296E    E760 5028 080E                  00002938    1794+           VST     V22,V1042              save v1 output
00002974    07FB                                        1795+           BR      R11                   return
00002978                                                1796+RE42       DC      0F                    xl16 expected result
00002978                                                1797+           DROP    R5
00002978    00000000 00200000                           1798            DC      XL16'0000000000200000 0000000000000010'     result
00002980    00000000 00000010
00002988    80000000 00000000                           1799            DC      XL16'8000000000000000 8000000000000000'     v2
00002990    80000000 00000000
00002998    00000000 0000002A                           1800            DC      XL16'000000000000002A 000000000000003B'     v3
000029A0    00000000 0000003B
                                                        1801
                                                        1802            VRR_C VESRLV,3
000029A8                                                1803+           DS      0FD
000029A8                         000029A8               1804+           USING *,R5                   base for test data and test routine
000029A8    000029E8                                    1805+T43        DC      A(X43)                address of test routine
000029AC    002B                                        1806+           DC      H'43'                 test number
000029AE    00                                          1807+           DC      X'00'
000029AF    03                                          1808+           DC      HL1'3'                m4
000029B0    E5C5E2D9 D3E54040                           1809+           DC      CL8'VESRLV'           instruction name
000029B8    00002A20                                    1810+           DC      A(RE43+16)            address of v2 source
000029BC    00002A30                                    1811+           DC      A(RE43+32)            address of v3 source
000029C0    00000010                                    1812+           DC      A(16)                 result length
000029C4    00002A10                                    1813+REA43      DC      A(RE43)               result address
000029C8    00000000 00000000                           1814+           DS      FD                    gap
000029D0    00000000 00000000                           1815+V1043      DS      XL16                  V1 output
000029D8    00000000 00000000
000029E0    00000000 00000000                           1816+           DS      FD                    gap
                                                        1817+*
000029E8                                                1818+X43        DS      0F
000029E8    E310 5010 0014                  00000010    1819+           LGF     R1,V2ADDR             load v2 source
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000029EE	E761 0000 0806		00000000	1820+	VL	v22,0(R1)	use v22 to test decoder
000029F4	E310 5014 0014		00000014	1821+	LGF	R1,V3ADDR	load v3 source
000029FA	E771 0000 0806		00000000	1822+	VL	v23,0(R1)	use v23 to test decoder
00002A00	E766 7000 3E78			1823+	VESRLV V22,V22,V23,3		test instruction (dest is a source)
00002A06	E760 5028 080E		000029D0	1824+	VST	V22,V1043	save v1 output
00002A0C	07FB			1825+	BR	R11	return
00002A10				1826+RE43	DC	0F	xl16 expected result
00002A10				1827+	DROP	R5	
00002A10	01FFFFFF FFFFFFFF			1828	DC	XL16'01FFFFFFFFFFFFFF 00003FFFFFFFFFFF'	result
00002A18	00003FFF FFFFFFFF						
00002A20	FFFFFFFF FFFFFFFF			1829	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00002A28	FFFFFFFF FFFFFFFF						
00002A30	00000000 00000007			1830	DC	XL16'0000000000000007 0000000000000012'	v3
00002A38	00000000 00000012						
				1831			
				1832	VRR_C VESRLV,3		
00002A40				1833+	DS	0FD	
00002A40		00002A40		1834+	USING	*,R5	base for test data and test routine
00002A40	00002A80			1835+T44	DC	A(X44)	address of test routine
00002A44	002C			1836+	DC	H'44'	test number
00002A46	00			1837+	DC	X'00'	
00002A47	03			1838+	DC	HL1'3'	m4
00002A48	E5C5E2D9 D3E54040			1839+	DC	CL8'VESRLV'	instruction name
00002A50	00002AB8			1840+	DC	A(RE44+16)	address of v2 source
00002A54	00002AC8			1841+	DC	A(RE44+32)	address of v3 source
00002A58	00000010			1842+	DC	A(16)	result length
00002A5C	00002AA8			1843+REA44	DC	A(RE44)	result address
00002A60	00000000 00000000			1844+	DS	FD	gap
00002A68	00000000 00000000			1845+V1044	DS	XL16	V1 output
00002A70	00000000 00000000						
00002A78	00000000 00000000			1846+	DS	FD	gap
				1847+*			
00002A80				1848+X44	DS	0F	
00002A80	E310 5010 0014		00000010	1849+	LGF	R1,V2ADDR	load v2 source
00002A86	E761 0000 0806		00000000	1850+	VL	v22,0(R1)	use v22 to test decoder
00002A8C	E310 5014 0014		00000014	1851+	LGF	R1,V3ADDR	load v3 source
00002A92	E771 0000 0806		00000000	1852+	VL	v23,0(R1)	use v23 to test decoder
00002A98	E766 7000 3E78			1853+	VESRLV V22,V22,V23,3		test instruction (dest is a source)
00002A9E	E760 5028 080E		00002A68	1854+	VST	V22,V1044	save v1 output
00002AA4	07FB			1855+	BR	R11	return
00002AA8				1856+RE44	DC	0F	xl16 expected result
00002AA8				1857+	DROP	R5	
00002AA8	00000000 3FFFFFFF			1858	DC	XL16'000000003FFFFFFF 0000000000001FFF'	result
00002AB0	00000000 00001FFF						
00002AB8	FFFFFFFF FFFFFFFF			1859	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00002AC0	FFFFFFFF FFFFFFFF						
00002AC8	00000000 00000022			1860	DC	XL16'0000000000000022 0000000000000033'	v3
00002AD0	00000000 00000033						
				1861			
				1862			
				1863	VRR_C VESRLV,3		
00002AD8				1864+	DS	0FD	
00002AD8		00002AD8		1865+	USING	*,R5	base for test data and test routine
00002AD8	00002B18			1866+T45	DC	A(X45)	address of test routine
00002ADC	002D			1867+	DC	H'45'	test number
00002ADE	00			1868+	DC	X'00'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002ADF	03			1869+	DC	HL1'3'	m4
00002AE0	E5C5E2D9 D3E54040			1870+	DC	CL8'VESRLV'	instruction name
00002AE8	00002B50			1871+	DC	A(RE45+16)	address of v2 source
00002AEC	00002B60			1872+	DC	A(RE45+32)	address of v3 source
00002AF0	00000010			1873+	DC	A(16)	result length
00002AF4	00002B40			1874+REA45	DC	A(RE45)	result address
00002AF8	00000000 00000000			1875+	DS	FD	gap
00002B00	00000000 00000000			1876+V1045	DS	XL16	V1 output
00002B08	00000000 00000000						
00002B10	00000000 00000000			1877+	DS	FD	gap
				1878+*			
00002B18				1879+X45	DS	0F	
00002B18	E310 5010 0014		00000010	1880+	LGF	R1,V2ADDR	load v2 source
00002B1E	E761 0000 0806		00000000	1881+	VL	v22,0(R1)	use v22 to test decoder
00002B24	E310 5014 0014		00000014	1882+	LGF	R1,V3ADDR	load v3 source
00002B2A	E771 0000 0806		00000000	1883+	VL	v23,0(R1)	use v23 to test decoder
00002B30	E766 7000 3E78			1884+	VESRLV V22,V22,V23,3		test instruction (dest is a source)
00002B36	E760 5028 080E		00002B00	1885+	VST	V22,V1045	save v1 output
00002B3C	07FB			1886+	BR	R11	return
00002B40				1887+RE45	DC	0F	xl16 expected result
00002B40				1888+	DROP	R5	
00002B40	00200000 00000000			1889	DC	XL16'0020000000000000 0010000000000000'	result
00002B48	00100000 00000000						
00002B50	80000000 00000000			1890	DC	XL16'8000000000000000 8000000000000000'	v2
00002B58	80000000 00000000						
00002B60	F0000000 0000000A			1891	DC	XL16'F00000000000000A F00000000000000B'	v3
00002B68	F0000000 0000000B						
				1892			
				1893		VRR_C VESRLV,3	
00002B70				1894+	DS	0FD	
00002B70		00002B70		1895+	USING	*,R5	base for test data and test routine
00002B70	00002BB0			1896+T46	DC	A(X46)	address of test routine
00002B74	002E			1897+	DC	H'46'	test number
00002B76	00			1898+	DC	X'00'	
00002B77	03			1899+	DC	HL1'3'	m4
00002B78	E5C5E2D9 D3E54040			1900+	DC	CL8'VESRLV'	instruction name
00002B80	00002BE8			1901+	DC	A(RE46+16)	address of v2 source
00002B84	00002BF8			1902+	DC	A(RE46+32)	address of v3 source
00002B88	00000010			1903+	DC	A(16)	result length
00002B8C	00002BD8			1904+REA46	DC	A(RE46)	result address
00002B90	00000000 00000000			1905+	DS	FD	gap
00002B98	00000000 00000000			1906+V1046	DS	XL16	V1 output
00002BA0	00000000 00000000						
00002BA8	00000000 00000000			1907+	DS	FD	gap
				1908+*			
00002BB0				1909+X46	DS	0F	
00002BB0	E310 5010 0014		00000010	1910+	LGF	R1,V2ADDR	load v2 source
00002BB6	E761 0000 0806		00000000	1911+	VL	v22,0(R1)	use v22 to test decoder
00002BBC	E310 5014 0014		00000014	1912+	LGF	R1,V3ADDR	load v3 source
00002BC2	E771 0000 0806		00000000	1913+	VL	v23,0(R1)	use v23 to test decoder
00002BC8	E766 7000 3E78			1914+	VESRLV V22,V22,V23,3		test instruction (dest is a source)
00002BCE	E760 5028 080E		00002B98	1915+	VST	V22,V1046	save v1 output
00002BD4	07FB			1916+	BR	R11	return
00002BD8				1917+RE46	DC	0F	xl16 expected result
00002BD8				1918+	DROP	R5	
00002BD8	00000000 3FFFFFFF			1919	DC	XL16'000000003FFFFFFF 0000000000001FFF'	result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00002BE0	00000000 00001FFF					
00002BE8	FFFFFFFF FFFFFFFF			1920	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF' v2
00002BF0	FFFFFFFF FFFFFFFF					
00002BF8	F0000000 00000022			1921	DC	XL16'F000000000000022 F000000000000033' v3
00002C00	F0000000 00000033					
				1922		
				1923		

```
  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

                                                    1925 *-------------------------------------------------------------------
                                                    1926 *    VESRAV - Vector Element Shift Right Arithmetic Vector
                                                    1927 *-------------------------------------------------------------------
                                                    1928 *Byte
                                                    1929          VRR_C VESRAV, 0
00002C08                                            1930+         DS    0FD
00002C08                         00002C08           1931+         USING *, R5                  base for test data and test routine
00002C08   00002C48                                 1932+T47      DC    A(X47)                 address of test routine
00002C0C   002F                                     1933+         DC    H'47'                  test number
00002C0E   00                                       1934+         DC    X'00'
00002C0F   00                                       1935+         DC    HL1'0'                 m4
00002C10   E5C5E2D9 C1E54040                         1936+         DC    CL8'VESRAV'            instruction name
00002C18   00002C80                                 1937+         DC    A(RE47+16)             address of v2 source
00002C1C   00002C90                                 1938+         DC    A(RE47+32)             address of v3 source
00002C20   00000010                                 1939+         DC    A(16)                  result length
00002C24   00002C70                                 1940+REA47    DC    A(RE47)                result address
00002C28   00000000 00000000                         1941+         DS    FD                     gap
00002C30   00000000 00000000                         1942+V1047    DS    XL16                   V1 output
00002C38   00000000 00000000
00002C40   00000000 00000000                         1943+         DS    FD                     gap
                                                    1944+*
00002C48                                            1945+X47      DS    0F
00002C48   E310 5010 0014              00000010     1946+         LGF   R1, V2ADDR             load v2 source
00002C4E   E761 0000 0806              00000000     1947+         VL    v22, 0(R1)             use v22 to test decoder
00002C54   E310 5014 0014              00000014     1948+         LGF   R1, V3ADDR             load v3 source
00002C5A   E771 0000 0806              00000000     1949+         VL    v23, 0(R1)             use v23 to test decoder
00002C60   E766 7000 0E7A                            1950+         VESRAV V22, V22, V23, 0      test instruction (dest is a source)
00002C66   E760 5028 080E              00002C30     1951+         VST   V22, V1047              save v1 output
00002C6C   07FB                                     1952+         BR    R11                    return
00002C70                                            1953+RE47    DC    0F                     xl16 expected result
00002C70                                            1954+         DROP  R5
00002C70   40201008 04020100                         1955          DC    XL16'4020100804020100 4020100804020100'      result
00002C78   40201008 04020100
00002C80   40404040 40404040                         1956          DC    XL16'4040404040404040 4040404040404040'      v2
00002C88   40404040 40404040
00002C90   00010203 04050607                         1957          DC    XL16'0001020304050607 08090A0B0C0D0E0F'      v3
00002C98   08090A0B 0C0D0E0F
                                                    1958
                                                    1959          VRR_C VESRAV, 0
00002CA0                                            1960+         DS    0FD
00002CA0                         00002CA0           1961+         USING *, R5                  base for test data and test routine
00002CA0   00002CE0                                 1962+T48      DC    A(X48)                 address of test routine
00002CA4   0030                                     1963+         DC    H'48'                  test number
00002CA6   00                                       1964+         DC    X'00'
00002CA7   00                                       1965+         DC    HL1'0'                 m4
00002CA8   E5C5E2D9 C1E54040                         1966+         DC    CL8'VESRAV'            instruction name
00002CB0   00002D18                                 1967+         DC    A(RE48+16)             address of v2 source
00002CB4   00002D28                                 1968+         DC    A(RE48+32)             address of v3 source
00002CB8   00000010                                 1969+         DC    A(16)                  result length
00002CBC   00002D08                                 1970+REA48    DC    A(RE48)                result address
00002CC0   00000000 00000000                         1971+         DS    FD                     gap
00002CC8   00000000 00000000                         1972+V1048    DS    XL16                   V1 output
00002CD0   00000000 00000000
00002CD8   00000000 00000000                         1973+         DS    FD                     gap
                                                    1974+*
00002CE0                                            1975+X48      DS    0F
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002CE0	E310 5010 0014		00000010	1976+	LGF	R1,V2ADDR	load v2 source
00002CE6	E761 0000 0806		00000000	1977+	VL	v22,0(R1)	use v22 to test decoder
00002CEC	E310 5014 0014		00000014	1978+	LGF	R1,V3ADDR	load v3 source
00002CF2	E771 0000 0806		00000000	1979+	VL	v23,0(R1)	use v23 to test decoder
00002CF8	E766 7000 0E7A			1980+	VESRAV V22,V22,V23,0		test instruction (dest is a source)
00002CFE	E760 5028 080E		00002CC8	1981+	VST	V22,V1048	save v1 output
00002D04	07FB			1982+	BR	R11	return
00002D08				1983+RE48	DC	0F	xl16 expected result
00002D08				1984+	DROP	R5	
00002D08	80C0E0F0 F8FCFEFF			1985	DC	XL16'80C0E0F0F8FCFEFF 80C0E0F0F8FCFEFF'	result
00002D10	80C0E0F0 F8FCFEFF						
00002D18	80808080 80808080			1986	DC	XL16'8080808080808080 8080808080808080'	v2
00002D20	80808080 80808080						
00002D28	00010203 04050607			1987	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	v3
00002D30	08090A0B 0C0D0E0F						
				1988			
				1989	VRR_C VESRAV,0		
00002D38				1990+	DS	0FD	
00002D38		00002D38		1991+	USING *,R5		base for test data and test routine
00002D38	00002D78			1992+T49	DC	A(X49)	address of test routine
00002D3C	0031			1993+	DC	H'49'	test number
00002D3E	00			1994+	DC	X'00'	
00002D3F	00			1995+	DC	HL1'0'	m4
00002D40	E5C5E2D9 C1E54040			1996+	DC	CL8'VESRAV'	instruction name
00002D48	00002DB0			1997+	DC	A(RE49+16)	address of v2 source
00002D4C	00002DC0			1998+	DC	A(RE49+32)	address of v3 source
00002D50	00000010			1999+	DC	A(16)	result length
00002D54	00002DA0			2000+REA49	DC	A(RE49)	result address
00002D58	00000000 00000000			2001+	DS	FD	gap
00002D60	00000000 00000000			2002+V1049	DS	XL16	V1 output
00002D68	00000000 00000000						
00002D70	00000000 00000000			2003+	DS	FD	gap
				2004+*			
00002D78				2005+X49	DS	0F	
00002D78	E310 5010 0014		00000010	2006+	LGF	R1,V2ADDR	load v2 source
00002D7E	E761 0000 0806		00000000	2007+	VL	v22,0(R1)	use v22 to test decoder
00002D84	E310 5014 0014		00000014	2008+	LGF	R1,V3ADDR	load v3 source
00002D8A	E771 0000 0806		00000000	2009+	VL	v23,0(R1)	use v23 to test decoder
00002D90	E766 7000 0E7A			2010+	VESRAV V22,V22,V23,0		test instruction (dest is a source)
00002D96	E760 5028 080E		00002D60	2011+	VST	V22,V1049	save v1 output
00002D9C	07FB			2012+	BR	R11	return
00002DA0				2013+RE49	DC	0F	xl16 expected result
00002DA0				2014+	DROP	R5	
00002DA0	F0F8FCFE FFFFFFFF			2015	DC	XL16'F0F8FCFEFFFFFFFF F8FCFEFFFFFFFFFF'	result
00002DA8	F8FCFEFF FFFFFFFF						
00002DB0	F0F1F2F3 F4F5F6F7			2016	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	v2
00002DB8	F8F9FAFB FCFDFEFF						
00002DC0	00010203 04050607			2017	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	v3
00002DC8	08090A0B 0C0D0E0F						
				2018			
				2019	VRR_C VESRAV,0		
00002DD0				2020+	DS	0FD	
00002DD0		00002DD0		2021+	USING *,R5		base for test data and test routine
00002DD0	00002E10			2022+T50	DC	A(X50)	address of test routine
00002DD4	0032			2023+	DC	H'50'	test number
00002DD6	00			2024+	DC	X'00'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002DD7	00			2025+	DC	HL1'0'	m4	
00002DD8	E5C5E2D9 C1E54040			2026+	DC	CL8'VESRAV'	instruction name	
00002DE0	00002E48			2027+	DC	A(RE50+16)	address of v2 source	
00002DE4	00002E58			2028+	DC	A(RE50+32)	address of v3 source	
00002DE8	00000010			2029+	DC	A(16)	result length	
00002DEC	00002E38			2030+REA50	DC	A(RE50)	result address	
00002DF0	00000000 00000000			2031+	DS	FD	gap	
00002DF8	00000000 00000000			2032+V1050	DS	XL16	V1 output	
00002E00	00000000 00000000							
00002E08	00000000 00000000			2033+	DS	FD	gap	
				2034+*				
00002E10				2035+X50	DS	0F		
00002E10	E310 5010 0014		00000010	2036+	LGF	R1,V2ADDR	load v2 source	
00002E16	E761 0000 0806		00000000	2037+	VL	v22,0(R1)	use v22 to test decoder	
00002E1C	E310 5014 0014		00000014	2038+	LGF	R1,V3ADDR	load v3 source	
00002E22	E771 0000 0806		00000000	2039+	VL	v23,0(R1)	use v23 to test decoder	
00002E28	E766 7000 0E7A			2040+	VESRAV	V22,V22,V23,0	test instruction (dest is a source)	
00002E2E	E760 5028 080E		00002DF8	2041+	VST	V22,V1050	save v1 output	
00002E34	07FB			2042+	BR	R11	return	
00002E38				2043+RE50	DC	0F	xl16 expected result	
00002E38				2044+	DROP	R5		
00002E38	40201008 04020100			2045	DC	XL16'4020100804020100 4020100804020100'	result	
00002E40	40201008 04020100							
00002E48	40404040 40404040			2046	DC	XL16'4040404040404040 4040404040404040'	v2	
00002E50	40404040 40404040							
00002E58	F0F1F2F3 F4F5F6F7			2047	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	v3	
00002E60	F8F9FAFB FCFDFEFF							
				2048				
				2049	VRR_C	VESRAV,0		
00002E68				2050+	DS	0FD		
00002E68		00002E68		2051+	USING	*,R5	base for test data and test routine	
00002E68	00002EA8			2052+T51	DC	A(X51)	address of test routine	
00002E6C	0033			2053+	DC	H'51'	test number	
00002E6E	00			2054+	DC	X'00'		
00002E6F	00			2055+	DC	HL1'0'	m4	
00002E70	E5C5E2D9 C1E54040			2056+	DC	CL8'VESRAV'	instruction name	
00002E78	00002EE0			2057+	DC	A(RE51+16)	address of v2 source	
00002E7C	00002EF0			2058+	DC	A(RE51+32)	address of v3 source	
00002E80	00000010			2059+	DC	A(16)	result length	
00002E84	00002ED0			2060+REA51	DC	A(RE51)	result address	
00002E88	00000000 00000000			2061+	DS	FD	gap	
00002E90	00000000 00000000			2062+V1051	DS	XL16	V1 output	
00002E98	00000000 00000000							
00002EA0	00000000 00000000			2063+	DS	FD	gap	
				2064+*				
00002EA8				2065+X51	DS	0F		
00002EA8	E310 5010 0014		00000010	2066+	LGF	R1,V2ADDR	load v2 source	
00002EAE	E761 0000 0806		00000000	2067+	VL	v22,0(R1)	use v22 to test decoder	
00002EB4	E310 5014 0014		00000014	2068+	LGF	R1,V3ADDR	load v3 source	
00002EBA	E771 0000 0806		00000000	2069+	VL	v23,0(R1)	use v23 to test decoder	
00002EC0	E766 7000 0E7A			2070+	VESRAV	V22,V22,V23,0	test instruction (dest is a source)	
00002EC6	E760 5028 080E		00002E90	2071+	VST	V22,V1051	save v1 output	
00002ECC	07FB			2072+	BR	R11	return	
00002ED0				2073+RE51	DC	0F	xl16 expected result	
00002ED0				2074+	DROP	R5		
00002ED0	F0F8FCFE FFFFFFFF			2075	DC	XL16'F0F8FCFEFFFFFFFF F8FCFEFFFFFFFFFF'	result	

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00002ED8  F8FCFEFF FFFFFFFF
00002EE0  F0F1F2F3 F4F5F6F7            2076            DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'    v2
00002EE8  F8F9FAFB FCFDFEFF
00002EF0  F0F1F2F3 F4F5F6F7            2077            DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'    v3
00002EF8  F8F9FAFB FCFDFEFF
                                       2078
                                       2079
                                       2080  *Halfword
                                       2081            VRR_C VESRAV, 1
00002F00                               2082+           DS    0FD
00002F00                     00002F00  2083+           USING *, R5                  base for test data and test routine
00002F00  00002F40                     2084+T52        DC    A(X52)                 address of test routine
00002F04  0034                         2085+           DC    H'52'                  test number
00002F06  00                           2086+           DC    X'00'
00002F07  01                           2087+           DC    HL1'1'                 m4
00002F08  E5C5E2D9 C1E54040            2088+           DC    CL8'VESRAV'            instruction name
00002F10  00002F78                     2089+           DC    A(RE52+16)             address of v2 source
00002F14  00002F88                     2090+           DC    A(RE52+32)             address of v3 source
00002F18  00000010                     2091+           DC    A(16)                  result length
00002F1C  00002F68                     2092+REA52      DC    A(RE52)                result address
00002F20  00000000 00000000            2093+           DS    FD                     gap
00002F28  00000000 00000000            2094+V1052      DS    XL16                   V1 output
00002F30  00000000 00000000
00002F38  00000000 00000000            2095+           DS    FD                     gap
                                       2096+*
00002F40                               2097+X52        DS    0F
00002F40  E310 5010 0014      00000010 2098+           LGF   R1, V2ADDR             load v2 source
00002F46  E761 0000 0806      00000000 2099+           VL    v22, 0(R1)             use v22 to test decoder
00002F4C  E310 5014 0014      00000014 2100+           LGF   R1, V3ADDR             load v3 source
00002F52  E771 0000 0806      00000000 2101+           VL    v23, 0(R1)             use v23 to test decoder
00002F58  E766 7000 1E7A               2102+           VESRAV V22, V22, V23, 1       test instruction (dest is a source)
00002F5E  E760 5028 080E      00002F28 2103+           VST   V22, V1052             save v1 output
00002F64  07FB                         2104+           BR    R11                    return
00002F68                               2105+RE52       DC    0F                     xl16 expected result
00002F68                               2106+           DROP  R5
00002F68  40002000 10000800            2107            DC    XL16'4000200010000800 0400020001000080'    result
00002F70  04000200 01000080
00002F78  40004000 40004000            2108            DC    XL16'4000400040004000 4000400040004000'    v2
00002F80  40004000 40004000
00002F88  00000001 00020003            2109            DC    XL16'0000000100020003 0004000500060007'    v3
00002F90  00040005 00060007
                                       2110
                                       2111            VRR_C VESRAV, 1
00002F98                               2112+           DS    0FD
00002F98                     00002F98  2113+           USING *, R5                  base for test data and test routine
00002F98  00002FD8                     2114+T53        DC    A(X53)                 address of test routine
00002F9C  0035                         2115+           DC    H'53'                  test number
00002F9E  00                           2116+           DC    X'00'
00002F9F  01                           2117+           DC    HL1'1'                 m4
00002FA0  E5C5E2D9 C1E54040            2118+           DC    CL8'VESRAV'            instruction name
00002FA8  00003010                     2119+           DC    A(RE53+16)             address of v2 source
00002FAC  00003020                     2120+           DC    A(RE53+32)             address of v3 source
00002FB0  00000010                     2121+           DC    A(16)                  result length
00002FB4  00003000                     2122+REA53      DC    A(RE53)                result address
00002FB8  00000000 00000000            2123+           DS    FD                     gap
00002FC0  00000000 00000000            2124+V1053      DS    XL16                   V1 output
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002FC8	00000000 00000000						
00002FD0	00000000 00000000			2125+	DS	FD	gap
				2126+*			
00002FD8				2127+X53	DS	0F	
00002FD8	E310 5010 0014		00000010	2128+	LGF	R1,V2ADDR	load v2 source
00002FDE	E761 0000 0806		00000000	2129+	VL	v22,0(R1)	use v22 to test decoder
00002FE4	E310 5014 0014		00000014	2130+	LGF	R1,V3ADDR	load v3 source
00002FEA	E771 0000 0806		00000000	2131+	VL	v23,0(R1)	use v23 to test decoder
00002FF0	E766 7000 1E7A			2132+	VESRAV V22,V22,V23,1		test instruction (dest is a source)
00002FF6	E760 5028 080E		00002FC0	2133+	VST	V22,V1053	save v1 output
00002FFC	07FB			2134+	BR	R11	return
00003000				2135+RE53	DC	0F	xl16 expected result
00003000				2136+	DROP	R5	
00003000	8000C000 E000F000			2137	DC	XL16'8000C000E000F000 F800FC00FE00FF00'	result
00003008	F800FC00 FE00FF00						
00003010	80008000 80008000			2138	DC	XL16'8000800080008000 8000800080008000'	v2
00003018	80008000 80008000						
00003020	00000001 00020003			2139	DC	XL16'0000000100020003 0004000500060007'	v3
00003028	00040005 00060007						
				2140			
00003030				2141	VRR_C VESRAV,1		
00003030				2142+	DS	0FD	
00003030		00003030		2143+	USING *,R5		base for test data and test routine
00003030	00003070			2144+T54	DC	A(X54)	address of test routine
00003034	0036			2145+	DC	H'54'	test number
00003036	00			2146+	DC	X'00'	
00003037	01			2147+	DC	HL1'1'	m4
00003038	E5C5E2D9 C1E54040			2148+	DC	CL8'VESRAV'	instruction name
00003040	000030A8			2149+	DC	A(RE54+16)	address of v2 source
00003044	000030B8			2150+	DC	A(RE54+32)	address of v3 source
00003048	00000010			2151+	DC	A(16)	result length
0000304C	00003098			2152+REA54	DC	A(RE54)	result address
00003050	00000000 00000000			2153+	DS	FD	gap
00003058	00000000 00000000			2154+V1054	DS	XL16	V1 output
00003060	00000000 00000000						
00003068	00000000 00000000			2155+	DS	FD	gap
				2156+*			
00003070				2157+X54	DS	0F	
00003070	E310 5010 0014		00000010	2158+	LGF	R1,V2ADDR	load v2 source
00003076	E761 0000 0806		00000000	2159+	VL	v22,0(R1)	use v22 to test decoder
0000307C	E310 5014 0014		00000014	2160+	LGF	R1,V3ADDR	load v3 source
00003082	E771 0000 0806		00000000	2161+	VL	v23,0(R1)	use v23 to test decoder
00003088	E766 7000 1E7A			2162+	VESRAV V22,V22,V23,1		test instruction (dest is a source)
0000308E	E760 5028 080E		00003058	2163+	VST	V22,V1054	save v1 output
00003094	07FB			2164+	BR	R11	return
00003098				2165+RE54	DC	0F	xl16 expected result
00003098				2166+	DROP	R5	
00003098	FF80FFC0 FFE0FFF0			2167	DC	XL16'FF80FFC0FFE0FFF0 FFF8FFFCFFFEFFFF'	result
000030A0	FFF8FFFC FFFEFFFF						
000030A8	80008000 80008000			2168	DC	XL16'8000800080008000 8000800080008000'	v2
000030B0	80008000 80008000						
000030B8	00080009 000A000B			2169	DC	XL16'00080009000A000B 000C000D000E000F'	v3
000030C0	000C000D 000E000F						
				2170			
				2171	VRR_C VESRAV,1		
000030C8				2172+	DS	0FD	

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  LOC        OBJECT CODE      ADDR1     ADDR2      STMT

000030C8                     000030C8             2173+             USING  *,R5                base for test data and test routine
000030C8  00003108                                2174+T55    DC     A(X55)              address of test routine
000030CC  0037                                    2175+       DC     H'55'               test number
000030CE  00                                      2176+       DC     X'00'
000030CF  01                                      2177+       DC     HL1'1'              m4
000030D0  E5C5E2D9 C1E54040                        2178+       DC     CL8'VESRAV'         instruction name
000030D8  00003140                                2179+       DC     A(RE55+16)          address of v2 source
000030DC  00003150                                2180+       DC     A(RE55+32)          address of v3 source
000030E0  00000010                                2181+       DC     A(16)               result length
000030E4  00003130                                2182+REA55  DC     A(RE55)             result address
000030E8  00000000 00000000                        2183+       DS     FD                  gap
000030F0  00000000 00000000                        2184+V1055  DS     XL16                V1 output
000030F8  00000000 00000000
00003100  00000000 00000000                        2185+       DS     FD                  gap
                                                   2186+*
00003108                                           2187+X55    DS     0F
00003108  E310 5010 0014              00000010     2188+       LGF    R1,V2ADDR           load v2 source
0000310E  E761 0000 0806              00000000     2189+       VL     v22,0(R1)           use v22 to test decoder
00003114  E310 5014 0014              00000014     2190+       LGF    R1,V3ADDR           load v3 source
0000311A  E771 0000 0806              00000000     2191+       VL     v23,0(R1)           use v23 to test decoder
00003120  E766 7000 1E7A                           2192+       VESRAV V22,V22,V23,1        test instruction (dest is a source)
00003126  E760 5028 080E              000030F0     2193+       VST    V22,V1055            save v1 output
0000312C  07FB                                     2194+       BR     R11                 return
00003130                                           2195+RE55   DC     0F                  xl16 expected result
00003130                                           2196+       DROP   R5
00003130  F0F1F979 FD3DFEDE                        2197        DC     XL16'F0F1F979FD3DFEDE FF8FFFD7FFF3FFFD'    result
00003138  FF8FFFD7 FFF3FFFD
00003140  F0F1F2F3 F4F5F6F7                        2198        DC     XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'    v2
00003148  F8F9FAFB FCFDFEFF
00003150  00000001 00020003                        2199        DC     XL16'0000000100020003 0004000500060007'   v3
00003158  00040005 00060007
                                                   2200
                                                   2201        VRR_C  VESRAV,1
00003160                                           2202+       DS     0FD
00003160                     00003160             2203+       USING  *,R5                base for test data and test routine
00003160  000031A0                                2204+T56    DC     A(X56)              address of test routine
00003164  0038                                    2205+       DC     H'56'               test number
00003166  00                                      2206+       DC     X'00'
00003167  01                                      2207+       DC     HL1'1'              m4
00003168  E5C5E2D9 C1E54040                        2208+       DC     CL8'VESRAV'         instruction name
00003170  000031D8                                2209+       DC     A(RE56+16)          address of v2 source
00003174  000031E8                                2210+       DC     A(RE56+32)          address of v3 source
00003178  00000010                                2211+       DC     A(16)               result length
0000317C  000031C8                                2212+REA56  DC     A(RE56)             result address
00003180  00000000 00000000                        2213+       DS     FD                  gap
00003188  00000000 00000000                        2214+V1056  DS     XL16                V1 output
00003190  00000000 00000000
00003198  00000000 00000000                        2215+       DS     FD                  gap
                                                   2216+*
000031A0                                           2217+X56    DS     0F
000031A0  E310 5010 0014              00000010     2218+       LGF    R1,V2ADDR           load v2 source
000031A6  E761 0000 0806              00000000     2219+       VL     v22,0(R1)           use v22 to test decoder
000031AC  E310 5014 0014              00000014     2220+       LGF    R1,V3ADDR           load v3 source
000031B2  E771 0000 0806              00000000     2221+       VL     v23,0(R1)           use v23 to test decoder
000031B8  E766 7000 1E7A                           2222+       VESRAV V22,V22,V23,1        test instruction (dest is a source)
000031BE  E760 5028 080E              00003188     2223+       VST    V22,V1056            save v1 output
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000031C4	07FB			2224+	BR	R11		return
000031C8				2225+RE56	DC	0F		xl16 expected result
000031C8				2226+	DROP	R5		
000031C8	FFF0FFF9 FFFDFFFE			2227	DC	XL16'FFF0FFF9FFFDFFFE FFFFFFFFFFFFFFFF'		result
000031D0	FFFFFFFF FFFFFFFF							
000031D8	F0F1F2F3 F4F5F6F7			2228	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'		v2
000031E0	F8F9FAFB FCFDFEFF							
000031E8	00080009 000A000B			2229	DC	XL16'00080009000A000B 000C000D000E000F'		v3
000031F0	000C000D 000E000F							
				2230				
				2231	VRR_C	VESRAV, 1		
000031F8				2232+	DS	0FD		
000031F8		000031F8		2233+	USING	*,R5		base for test data and test routine
000031F8	00003238			2234+T57	DC	A(X57)		address of test routine
000031FC	0039			2235+	DC	H'57'		test number
000031FE	00			2236+	DC	X'00'		
000031FF	01			2237+	DC	HL1'1'		m4
00003200	E5C5E2D9 C1E54040			2238+	DC	CL8'VESRAV'		instruction name
00003208	00003270			2239+	DC	A(RE57+16)		address of v2 source
0000320C	00003280			2240+	DC	A(RE57+32)		address of v3 source
00003210	00000010			2241+	DC	A(16)		result length
00003214	00003260			2242+REA57	DC	A(RE57)		result address
00003218	00000000 00000000			2243+	DS	FD		gap
00003220	00000000 00000000			2244+V1057	DS	XL16		V1 output
00003228	00000000 00000000							
00003230	00000000 00000000			2245+	DS	FD		gap
				2246+*				
00003238				2247+X57	DS	0F		
00003238	E310 5010 0014		00000010	2248+	LGF	R1, V2ADDR		load v2 source
0000323E	E761 0000 0806		00000000	2249+	VL	v22, 0(R1)		use v22 to test decoder
00003244	E310 5014 0014		00000014	2250+	LGF	R1, V3ADDR		load v3 source
0000324A	E771 0000 0806		00000000	2251+	VL	v23, 0(R1)		use v23 to test decoder
00003250	E766 7000 1E7A			2252+	VESRAV	V22, V22, V23, 1		test instruction (dest is a source)
00003256	E760 5028 080E		00003220	2253+	VST	V22, V1057		save v1 output
0000325C	07FB			2254+	BR	R11		return
00003260				2255+RE57	DC	0F		xl16 expected result
00003260				2256+	DROP	R5		
00003260	8000C000 E000F000			2257	DC	XL16'8000C000E000F000 F800FC00FE00FF00'		result
00003268	F800FC00 FE00FF00							
00003270	80008000 80008000			2258	DC	XL16'8000800080008000 8000800080008000'		v2
00003278	80008000 80008000							
00003280	F000F001 F002F003			2259	DC	XL16'F000F001F002F003 F004F005F006F007'		v3
00003288	F004F005 F006F007							
				2260				
				2261	VRR_C	VESRAV, 1		
00003290				2262+	DS	0FD		
00003290		00003290		2263+	USING	*,R5		base for test data and test routine
00003290	000032D0			2264+T58	DC	A(X58)		address of test routine
00003294	003A			2265+	DC	H'58'		test number
00003296	00			2266+	DC	X'00'		
00003297	01			2267+	DC	HL1'1'		m4
00003298	E5C5E2D9 C1E54040			2268+	DC	CL8'VESRAV'		instruction name
000032A0	00003308			2269+	DC	A(RE58+16)		address of v2 source
000032A4	00003318			2270+	DC	A(RE58+32)		address of v3 source
000032A8	00000010			2271+	DC	A(16)		result length
000032AC	000032F8			2272+REA58	DC	A(RE58)		result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000032B0	00000000 00000000			2273+	DS	FD	gap
000032B8	00000000 00000000			2274+V1058	DS	XL16	V1 output
000032C0	00000000 00000000						
000032C8	00000000 00000000			2275+	DS	FD	gap
				2276+*			
000032D0				2277+X58	DS	0F	
000032D0	E310 5010 0014		00000010	2278+	LGF	R1,V2ADDR	load v2 source
000032D6	E761 0000 0806		00000000	2279+	VL	v22,0(R1)	use v22 to test decoder
000032DC	E310 5014 0014		00000014	2280+	LGF	R1,V3ADDR	load v3 source
000032E2	E771 0000 0806		00000000	2281+	VL	v23,0(R1)	use v23 to test decoder
000032E8	E766 7000 1E7A			2282+	VESRAV V22,V22,V23,1		test instruction (dest is a source)
000032EE	E760 5028 080E		000032B8	2283+	VST	V22,V1058	save v1 output
000032F4	07FB			2284+	BR	R11	return
000032F8				2285+RE58	DC	0F	xl16 expected result
000032F8				2286+	DROP	R5	
000032F8	F0F1F979 FD3DFEDE			2287	DC	XL16'F0F1F979FD3DFEDE FF8FFFD7FFF3FFFD' result	
00003300	FF8FFFD7 FFF3FFFD						
00003308	F0F1F2F3 F4F5F6F7			2288	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF' v2	
00003310	F8F9FAFB FCFDFEFF						
00003318	F000F001 F002F003			2289	DC	XL16'F000F001F002F003 F004F005F006F007' v3	
00003320	F004F005 F006F007						
				2290			
				2291 *Word			
				2292	VRR_C VESRAV,2		
00003328				2293+	DS	0FD	
00003328		00003328		2294+	USING *,R5		base for test data and test routine
00003328	00003368			2295+T59	DC	A(X59)	address of test routine
0000332C	003B			2296+	DC	H'59'	test number
0000332E	00			2297+	DC	X'00'	
0000332F	02			2298+	DC	HL1'2'	m4
00003330	E5C5E2D9 C1E54040			2299+	DC	CL8'VESRAV'	instruction name
00003338	000033A0			2300+	DC	A(RE59+16)	address of v2 source
0000333C	000033B0			2301+	DC	A(RE59+32)	address of v3 source
00003340	00000010			2302+	DC	A(16)	result length
00003344	00003390			2303+REA59	DC	A(RE59)	result address
00003348	00000000 00000000			2304+	DS	FD	gap
00003350	00000000 00000000			2305+V1059	DS	XL16	V1 output
00003358	00000000 00000000						
00003360	00000000 00000000			2306+	DS	FD	gap
				2307+*			
00003368				2308+X59	DS	0F	
00003368	E310 5010 0014		00000010	2309+	LGF	R1,V2ADDR	load v2 source
0000336E	E761 0000 0806		00000000	2310+	VL	v22,0(R1)	use v22 to test decoder
00003374	E310 5014 0014		00000014	2311+	LGF	R1,V3ADDR	load v3 source
0000337A	E771 0000 0806		00000000	2312+	VL	v23,0(R1)	use v23 to test decoder
00003380	E766 7000 2E7A			2313+	VESRAV V22,V22,V23,2		test instruction (dest is a source)
00003386	E760 5028 080E		00003350	2314+	VST	V22,V1059	save v1 output
0000338C	07FB			2315+	BR	R11	return
00003390				2316+RE59	DC	0F	xl16 expected result
00003390				2317+	DROP	R5	
00003390	40000000 20000000			2318	DC	XL16'4000000020000000 1000000008000000' result	
00003398	10000000 08000000						
000033A0	40000000 40000000			2319	DC	XL16'4000000040000000 4000000040000000' v2	
000033A8	40000000 40000000						
000033B0	00000000 00000001			2320	DC	XL16'0000000000000001 0000000200000003' v3	
000033B8	00000002 00000003						

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 LOC        OBJECT CODE        ADDR1    ADDR2    STMT

                                                2321
                                                2322           VRR_C VESRAV,2
000033C0                                        2323+          DS    0FD
000033C0                      000033C0          2324+          USING *,R5              base for test data and test routine
000033C0    00003400                            2325+T60       DC    A(X60)             address of test routine
000033C4    003C                                2326+          DC    H'60'              test number
000033C6    00                                  2327+          DC    X'00'
000033C7    02                                  2328+          DC    HL1'2'             m4
000033C8    E5C5E2D9 C1E54040                   2329+          DC    CL8'VESRAV'        instruction name
000033D0    00003438                            2330+          DC    A(RE60+16)         address of v2 source
000033D4    00003448                            2331+          DC    A(RE60+32)         address of v3 source
000033D8    00000010                            2332+          DC    A(16)              result length
000033DC    00003428                            2333+REA60     DC    A(RE60)            result address
000033E0    00000000 00000000                   2334+          DS    FD                 gap
000033E8    00000000 00000000                   2335+V1060     DS    XL16               V1 output
000033F0    00000000 00000000
000033F8    00000000 00000000                   2336+          DS    FD                 gap
                                                2337+*
00003400                                        2338+X60       DS    0F
00003400    E310 5010 0014              00000010 2339+         LGF   R1,V2ADDR          load v2 source
00003406    E761 0000 0806              00000000 2340+         VL    v22,0(R1)          use v22 to test decoder
0000340C    E310 5014 0014              00000014 2341+         LGF   R1,V3ADDR          load v3 source
00003412    E771 0000 0806              00000000 2342+         VL    v23,0(R1)          use v23 to test decoder
00003418    E766 7000 2E7A                       2343+         VESRAV V22,V22,V23,2      test instruction (dest is a source)
0000341E    E760 5028 080E              000033E8 2344+         VST   V22,V1060          save v1 output
00003424    07FB                                 2345+         BR    R11                return
00003428                                         2346+RE60     DC    0F                 xl16 expected result
00003428                                         2347+         DROP  R5
00003428    80000000 C0000000                    2348          DC    XL16'80000000C0000000 E0000000F0000000'    result
00003430    E0000000 F0000000
00003438    80000000 80000000                    2349          DC    XL16'8000000080000000 8000000080000000'    v2
00003440    80000000 80000000
00003448    00000000 00000001                    2350          DC    XL16'0000000000000001 0000000200000003'    v3
00003450    00000002 00000003
                                                 2351
                                                 2352          VRR_C VESRAV,2
00003458                                         2353+         DS    0FD
00003458                      00003458           2354+         USING *,R5              base for test data and test routine
00003458    00003498                             2355+T61      DC    A(X61)             address of test routine
0000345C    003D                                 2356+         DC    H'61'              test number
0000345E    00                                   2357+         DC    X'00'
0000345F    02                                   2358+         DC    HL1'2'             m4
00003460    E5C5E2D9 C1E54040                    2359+         DC    CL8'VESRAV'        instruction name
00003468    000034D0                             2360+         DC    A(RE61+16)         address of v2 source
0000346C    000034E0                             2361+         DC    A(RE61+32)         address of v3 source
00003470    00000010                             2362+         DC    A(16)              result length
00003474    000034C0                             2363+REA61    DC    A(RE61)            result address
00003478    00000000 00000000                    2364+         DS    FD                 gap
00003480    00000000 00000000                    2365+V1061    DS    XL16               V1 output
00003488    00000000 00000000
00003490    00000000 00000000                    2366+         DS    FD                 gap
                                                 2367+*
00003498                                         2368+X61      DS    0F
00003498    E310 5010 0014              00000010 2369+         LGF   R1,V2ADDR          load v2 source
0000349E    E761 0000 0806              00000000 2370+         VL    v22,0(R1)          use v22 to test decoder
000034A4    E310 5014 0014              00000014 2371+         LGF   R1,V3ADDR          load v3 source
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000034AA	E771 0000 0806		00000000	2372+	VL	v23,0(R1)	use v23 to test decoder
000034B0	E766 7000 2E7A			2373+	VESRAV V22,V22,V23,2		test instruction (dest is a source)
000034B6	E760 5028 080E		00003480	2374+	VST	V22,V1061	save v1 output
000034BC	07FB			2375+	BR	R11	return
000034C0				2376+RE61	DC	0F	xl16 expected result
000034C0				2377+	DROP	R5	
000034C0	FF800000 FFC00000			2378	DC	XL16'FF800000FFC00000 FFE00000FFF00000'	result
000034C8	FFE00000 FFF00000						
000034D0	80000000 80000000			2379	DC	XL16'8000000080000000 8000000080000000'	v2
000034D8	80000000 80000000						
000034E0	00000008 00000009			2380	DC	XL16'0000000800000009 0000000A0000000B'	v3
000034E8	0000000A 0000000B						
				2381			
				2382	VRR_C VESRAV,2		
000034F0				2383+	DS	0FD	
000034F0		000034F0		2384+	USING *,R5		base for test data and test routine
000034F0	00003530			2385+T62	DC	A(X62)	address of test routine
000034F4	003E			2386+	DC	H'62'	test number
000034F6	00			2387+	DC	X'00'	
000034F7	02			2388+	DC	HL1'2'	m4
000034F8	E5C5E2D9 C1E54040			2389+	DC	CL8'VESRAV'	instruction name
00003500	00003568			2390+	DC	A(RE62+16)	address of v2 source
00003504	00003578			2391+	DC	A(RE62+32)	address of v3 source
00003508	00000010			2392+	DC	A(16)	result length
0000350C	00003558			2393+REA62	DC	A(RE62)	result address
00003510	00000000 00000000			2394+	DS	FD	gap
00003518	00000000 00000000			2395+V1062	DS	XL16	V1 output
00003520	00000000 00000000						
00003528	00000000 00000000			2396+	DS	FD	gap
				2397+*			
00003530				2398+X62	DS	0F	
00003530	E310 5010 0014		00000010	2399+	LGF	R1,V2ADDR	load v2 source
00003536	E761 0000 0806		00000000	2400+	VL	v22,0(R1)	use v22 to test decoder
0000353C	E310 5014 0014		00000014	2401+	LGF	R1,V3ADDR	load v3 source
00003542	E771 0000 0806		00000000	2402+	VL	v23,0(R1)	use v23 to test decoder
00003548	E766 7000 2E7A			2403+	VESRAV V22,V22,V23,2		test instruction (dest is a source)
0000354E	E760 5028 080E		00003518	2404+	VST	V22,V1062	save v1 output
00003554	07FB			2405+	BR	R11	return
00003558				2406+RE62	DC	0F	xl16 expected result
00003558				2407+	DROP	R5	
00003558	F0F1F2F3 FA7AFB7B			2408	DC	XL16'F0F1F2F3FA7AFB7B FE3E7EBEFF9FBFDF'	result
00003560	FE3E7EBE FF9FBFDF						
00003568	F0F1F2F3 F4F5F6F7			2409	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	v2
00003570	F8F9FAFB FCFDFEFF						
00003578	00000000 00000001			2410	DC	XL16'0000000000000001 0000000200000003'	v3
00003580	00000002 00000003						
				2411			
				2412	VRR_C VESRAV,2		
00003588				2413+	DS	0FD	
00003588		00003588		2414+	USING *,R5		base for test data and test routine
00003588	000035C8			2415+T63	DC	A(X63)	address of test routine
0000358C	003F			2416+	DC	H'63'	test number
0000358E	00			2417+	DC	X'00'	
0000358F	02			2418+	DC	HL1'2'	m4
00003590	E5C5E2D9 C1E54040			2419+	DC	CL8'VESRAV'	instruction name
00003598	00003600			2420+	DC	A(RE63+16)	address of v2 source

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

0000359C   00003610                              2421+         DC     A(RE63+32)          address of v3 source
000035A0   00000010                              2422+         DC     A(16)              result length
000035A4   000035F0                              2423+REA63    DC     A(RE63)            result address
000035A8   00000000 00000000                     2424+         DS     FD                 gap
000035B0   00000000 00000000                     2425+V1063    DS     XL16               V1 output
000035B8   00000000 00000000
000035C0   00000000 00000000                     2426+         DS     FD                 gap
                                                 2427+*
000035C8                                         2428+X63      DS     0F
000035C8   E310 5010 0014             00000010   2429+         LGF    R1,V2ADDR          load v2 source
000035CE   E761 0000 0806             00000000   2430+         VL     v22,0(R1)          use v22 to test decoder
000035D4   E310 5014 0014             00000014   2431+         LGF    R1,V3ADDR          load v3 source
000035DA   E771 0000 0806             00000000   2432+         VL     v23,0(R1)          use v23 to test decoder
000035E0   E766 7000 2E7A                        2433+         VESRAV V22,V22,V23,2       test instruction (dest is a source)
000035E6   E760 5028 080E             000035B0   2434+         VST    V22,V1063          save v1 output
000035EC   07FB                                  2435+         BR     R11                return
000035F0                                         2436+RE63     DC     0F                 xl16 expected result
000035F0                                         2437+         DROP   R5
000035F0   FFF0F1F2 FFFA7AFB                      2438          DC     XL16'FFF0F1F2FFFA7AFB FFFE3E7EFFFF9FBF'     result
000035F8   FFFE3E7E FFFF9FBF
00003600   F0F1F2F3 F4F5F6F7                      2439          DC     XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'     v2
00003608   F8F9FAFB FCFDFEFF
00003610   00000008 00000009                      2440          DC     XL16'0000000800000009 0000000A0000000B'     v3
00003618   0000000A 0000000B
                                                 2441
                                                 2442          VRR_C  VESRAV,2
00003620                                         2443+         DS     0FD
00003620                             00003620    2444+         USING  *,R5               base for test data and test routine
00003620   00003660                              2445+T64      DC     A(X64)             address of test routine
00003624   0040                                  2446+         DC     H'64'              test number
00003626   00                                    2447+         DC     X'00'
00003627   02                                    2448+         DC     HL1'2'             m4
00003628   E5C5E2D9 C1E54040                      2449+         DC     CL8'VESRAV'        instruction name
00003630   00003698                              2450+         DC     A(RE64+16)         address of v2 source
00003634   000036A8                              2451+         DC     A(RE64+32)         address of v3 source
00003638   00000010                              2452+         DC     A(16)              result length
0000363C   00003688                              2453+REA64    DC     A(RE64)            result address
00003640   00000000 00000000                     2454+         DS     FD                 gap
00003648   00000000 00000000                     2455+V1064    DS     XL16               V1 output
00003650   00000000 00000000
00003658   00000000 00000000                     2456+         DS     FD                 gap
                                                 2457+*
00003660                                         2458+X64      DS     0F
00003660   E310 5010 0014             00000010   2459+         LGF    R1,V2ADDR          load v2 source
00003666   E761 0000 0806             00000000   2460+         VL     v22,0(R1)          use v22 to test decoder
0000366C   E310 5014 0014             00000014   2461+         LGF    R1,V3ADDR          load v3 source
00003672   E771 0000 0806             00000000   2462+         VL     v23,0(R1)          use v23 to test decoder
00003678   E766 7000 2E7A                        2463+         VESRAV V22,V22,V23,2       test instruction (dest is a source)
0000367E   E760 5028 080E             00003648   2464+         VST    V22,V1064          save v1 output
00003684   07FB                                  2465+         BR     R11                return
00003688                                         2466+RE64     DC     0F                 xl16 expected result
00003688                                         2467+         DROP   R5
00003688   80000000 C0000000                      2468          DC     XL16'80000000C0000000 E0000000F0000000'     result
00003690   E0000000 F0000000
00003698   80000000 80000000                      2469          DC     XL16'8000000080000000 8000000080000000'     v2
000036A0   80000000 80000000
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000036A8	F0000000 F0000001			2470	DC	XL16'F0000000F0000001 F0000002F0000003'	v3
000036B0	F0000002 F0000003						
				2471			
				2472	VRR_C	VESRAV, 2	
000036B8				2473+	DS	0FD	
000036B8		000036B8		2474+	USING	*, R5	base for test data and test routine
000036B8	000036F8			2475+T65	DC	A(X65)	address of test routine
000036BC	0041			2476+	DC	H'65'	test number
000036BE	00			2477+	DC	X'00'	
000036BF	02			2478+	DC	HL1'2'	m4
000036C0	E5C5E2D9 C1E54040			2479+	DC	CL8'VESRAV'	instruction name
000036C8	00003730			2480+	DC	A(RE65+16)	address of v2 source
000036CC	00003740			2481+	DC	A(RE65+32)	address of v3 source
000036D0	00000010			2482+	DC	A(16)	result length
000036D4	00003720			2483+REA65	DC	A(RE65)	result address
000036D8	00000000 00000000			2484+	DS	FD	gap
000036E0	00000000 00000000			2485+V1065	DS	XL16	V1 output
000036E8	00000000 00000000						
000036F0	00000000 00000000			2486+	DS	FD	gap
				2487+*			
000036F8				2488+X65	DS	0F	
000036F8	E310 5010 0014		00000010	2489+	LGF	R1, V2ADDR	load v2 source
000036FE	E761 0000 0806		00000000	2490+	VL	v22, 0(R1)	use v22 to test decoder
00003704	E310 5014 0014		00000014	2491+	LGF	R1, V3ADDR	load v3 source
0000370A	E771 0000 0806		00000000	2492+	VL	v23, 0(R1)	use v23 to test decoder
00003710	E766 7000 2E7A			2493+	VESRAV	V22, V22, V23, 2	test instruction (dest is a source)
00003716	E760 5028 080E		000036E0	2494+	VST	V22, V1065	save v1 output
0000371C	07FB			2495+	BR	R11	return
00003720				2496+RE65	DC	0F	xl16 expected result
00003720				2497+	DROP	R5	
00003720	FFF0F1F2 FFFA7AFB			2498	DC	XL16'FFF0F1F2FFFA7AFB FFFE3E7EFFFF9FBF'	result
00003728	FFFE3E7E FFFF9FBF						
00003730	F0F1F2F3 F4F5F6F7			2499	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	v2
00003738	F8F9FAFB FCFDFEFF						
00003740	F0000008 F0000009			2500	DC	XL16'F0000008F0000009 F000000AF000000B'	v3
00003748	F000000A F000000B						
				2501			
				2502			
				2503	*Doubleword		
				2504	VRR_C	VESRAV, 3	
00003750				2505+	DS	0FD	
00003750		00003750		2506+	USING	*, R5	base for test data and test routine
00003750	00003790			2507+T66	DC	A(X66)	address of test routine
00003754	0042			2508+	DC	H'66'	test number
00003756	00			2509+	DC	X'00'	
00003757	03			2510+	DC	HL1'3'	m4
00003758	E5C5E2D9 C1E54040			2511+	DC	CL8'VESRAV'	instruction name
00003760	000037C8			2512+	DC	A(RE66+16)	address of v2 source
00003764	000037D8			2513+	DC	A(RE66+32)	address of v3 source
00003768	00000010			2514+	DC	A(16)	result length
0000376C	000037B8			2515+REA66	DC	A(RE66)	result address
00003770	00000000 00000000			2516+	DS	FD	gap
00003778	00000000 00000000			2517+V1066	DS	XL16	V1 output
00003780	00000000 00000000						
00003788	00000000 00000000			2518+	DS	FD	gap
				2519+*			

```
  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

00003790                                        2520+X66     DS     0F
00003790  E310 5010 0014              00000010  2521+        LGF    R1,V2ADDR          load v2 source
00003796  E761 0000 0806              00000000  2522+        VL     v22,0(R1)          use v22 to test decoder
0000379C  E310 5014 0014              00000014  2523+        LGF    R1,V3ADDR          load v3 source
000037A2  E771 0000 0806              00000000  2524+        VL     v23,0(R1)          use v23 to test decoder
000037A8  E766 7000 3E7A                        2525+        VESRAV V22,V22,V23,3       test instruction (dest is a source)
000037AE  E760 5028 080E              00003778  2526+        VST    V22,V1066          save v1 output
000037B4  07FB                                  2527+        BR     R11                return
000037B8                                        2528+RE66    DC     0F                 xl16 expected result
000037B8                                        2529+        DROP   R5
000037B8  40000000 00000000                     2530         DC     XL16'400000000000000 2000000000000000'   result
000037C0  20000000 00000000
000037C8  40000000 00000000                     2531         DC     XL16'400000000000000 4000000000000000'   v2
000037D0  40000000 00000000
000037D8  00000000 00000000                     2532         DC     XL16'000000000000000 0000000000000001'   v3
000037E0  00000000 00000001
                                                2533
                                                2534         VRR_C  VESRAV,3
000037E8                                        2535+        DS     0FD
000037E8                      000037E8          2536+        USING  *,R5               base for test data and test routine
000037E8  00003828                              2537+T67     DC     A(X67)             address of test routine
000037EC  0043                                  2538+        DC     H'67'              test number
000037EE  00                                    2539+        DC     X'00'
000037EF  03                                    2540+        DC     HL1'3'             m4
000037F0  E5C5E2D9 C1E54040                     2541+        DC     CL8'VESRAV'        instruction name
000037F8  00003860                              2542+        DC     A(RE67+16)         address of v2 source
000037FC  00003870                              2543+        DC     A(RE67+32)         address of v3 source
00003800  00000010                              2544+        DC     A(16)              result length
00003804  00003850                              2545+REA67   DC     A(RE67)            result address
00003808  00000000 00000000                     2546+        DS     FD                 gap
00003810  00000000 00000000                     2547+V1067   DS     XL16               V1 output
00003818  00000000 00000000
00003820  00000000 00000000                     2548+        DS     FD                 gap
                                                2549+*
00003828                                        2550+X67     DS     0F
00003828  E310 5010 0014              00000010  2551+        LGF    R1,V2ADDR          load v2 source
0000382E  E761 0000 0806              00000000  2552+        VL     v22,0(R1)          use v22 to test decoder
00003834  E310 5014 0014              00000014  2553+        LGF    R1,V3ADDR          load v3 source
0000383A  E771 0000 0806              00000000  2554+        VL     v23,0(R1)          use v23 to test decoder
00003840  E766 7000 3E7A                        2555+        VESRAV V22,V22,V23,3       test instruction (dest is a source)
00003846  E760 5028 080E              00003810  2556+        VST    V22,V1067          save v1 output
0000384C  07FB                                  2557+        BR     R11                return
00003850                                        2558+RE67    DC     0F                 xl16 expected result
00003850                                        2559+        DROP   R5
00003850  80000000 00000000                     2560         DC     XL16'800000000000000 C000000000000000'   result
00003858  C0000000 00000000
00003860  80000000 00000000                     2561         DC     XL16'800000000000000 8000000000000000'   v2
00003868  80000000 00000000
00003870  00000000 00000000                     2562         DC     XL16'000000000000000 0000000000000001'   v3
00003878  00000000 00000001
                                                2563
                                                2564         VRR_C  VESRAV,3
00003880                                        2565+        DS     0FD
00003880                      00003880          2566+        USING  *,R5               base for test data and test routine
00003880  000038C0                              2567+T68     DC     A(X68)             address of test routine
00003884  0044                                  2568+        DC     H'68'              test number
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00003886  00                                      2569+          DC     X'00'
00003887  03                                      2570+          DC     HL1'3'                    m4
00003888  E5C5E2D9 C1E54040                        2571+          DC     CL8'VESRAV'               instruction name
00003890  000038F8                                 2572+          DC     A(RE68+16)                address of v2 source
00003894  00003908                                 2573+          DC     A(RE68+32)                address of v3 source
00003898  00000010                                 2574+          DC     A(16)                     result length
0000389C  000038E8                                 2575+REA68     DC     A(RE68)                   result address
000038A0  00000000 00000000                        2576+          DS     FD                        gap
000038A8  00000000 00000000                        2577+V1068     DS     XL16                      V1 output
000038B0  00000000 00000000
000038B8  00000000 00000000                        2578+          DS     FD                        gap
                                                   2579+*
000038C0                                           2580+X68       DS     0F
000038C0  E310 5010 0014               00000010    2581+          LGF    R1,V2ADDR                 load v2 source
000038C6  E761 0000 0806               00000000    2582+          VL     v22,0(R1)                 use v22 to test decoder
000038CC  E310 5014 0014               00000014    2583+          LGF    R1,V3ADDR                 load v3 source
000038D2  E771 0000 0806               00000000    2584+          VL     v23,0(R1)                 use v23 to test decoder
000038D8  E766 7000 3E7A                           2585+          VESRAV V22,V22,V23,3              test instruction (dest is a source)
000038DE  E760 5028 080E               000038A8    2586+          VST    V22,V1068                 save v1 output
000038E4  07FB                                     2587+          BR     R11                       return
000038E8                                           2588+RE68      DC     0F                        xl16 expected result
000038E8                                           2589+          DROP   R5
000038E8  FFE00000 00000000                        2590           DC     XL16'FFE0000000000000 FFF0000000000000'   result
000038F0  FFF00000 00000000
000038F8  80000000 00000000                        2591           DC     XL16'8000000000000000 8000000000000000'   v2
00003900  80000000 00000000
00003908  00000000 0000000A                        2592           DC     XL16'000000000000000A 000000000000000B'   v3
00003910  00000000 0000000B
                                                   2593
                                                   2594           VRR_C  VESRAV,3
00003918                                           2595+          DS     0FD
00003918                       00003918            2596+          USING  *,R5                      base for test data and test routine
00003918  00003958                                 2597+T69       DC     A(X69)                    address of test routine
0000391C  0045                                     2598+          DC     H'69'                     test number
0000391E  00                                       2599+          DC     X'00'
0000391F  03                                       2600+          DC     HL1'3'                    m4
00003920  E5C5E2D9 C1E54040                        2601+          DC     CL8'VESRAV'               instruction name
00003928  00003990                                 2602+          DC     A(RE69+16)                address of v2 source
0000392C  000039A0                                 2603+          DC     A(RE69+32)                address of v3 source
00003930  00000010                                 2604+          DC     A(16)                     result length
00003934  00003980                                 2605+REA69     DC     A(RE69)                   result address
00003938  00000000 00000000                        2606+          DS     FD                        gap
00003940  00000000 00000000                        2607+V1069     DS     XL16                      V1 output
00003948  00000000 00000000
00003950  00000000 00000000                        2608+          DS     FD                        gap
                                                   2609+*
00003958                                           2610+X69       DS     0F
00003958  E310 5010 0014               00000010    2611+          LGF    R1,V2ADDR                 load v2 source
0000395E  E761 0000 0806               00000000    2612+          VL     v22,0(R1)                 use v22 to test decoder
00003964  E310 5014 0014               00000014    2613+          LGF    R1,V3ADDR                 load v3 source
0000396A  E771 0000 0806               00000000    2614+          VL     v23,0(R1)                 use v23 to test decoder
00003970  E766 7000 3E7A                           2615+          VESRAV V22,V22,V23,3              test instruction (dest is a source)
00003976  E760 5028 080E               00003940    2616+          VST    V22,V1069                 save v1 output
0000397C  07FB                                     2617+          BR     R11                       return
00003980                                           2618+RE69      DC     0F                        xl16 expected result
00003980                                           2619+          DROP   R5
```

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  LOC          OBJECT CODE       ADDR1     ADDR2      STMT

00003980  FFFFFFFF FFE00000                           2620        DC     XL16'FFFFFFFFFFE00000 FFFFFFFFFFFFFFF0'     result
00003988  FFFFFFFF FFFFFFF0
00003990  80000000 00000000                           2621        DC     XL16'8000000000000000 8000000000000000'     v2
00003998  80000000 00000000
000039A0  00000000 0000002A                           2622        DC     XL16'000000000000002A 000000000000003B'     v3
000039A8  00000000 0000003B
                                                      2623
                                                      2624        VRR_C  VESRAV, 3
000039B0                                              2625+       DS     0FD
000039B0                         000039B0             2626+       USING  *,R5                   base for test data and test routine
000039B0  000039F0                                    2627+T70    DC     A(X70)                 address of test routine
000039B4  0046                                        2628+       DC     H'70'                  test number
000039B6  00                                          2629+       DC     X'00'
000039B7  03                                          2630+       DC     HL1'3'                 m4
000039B8  E5C5E2D9 C1E54040                           2631+       DC     CL8'VESRAV'            instruction name
000039C0  00003A28                                    2632+       DC     A(RE70+16)             address of v2 source
000039C4  00003A38                                    2633+       DC     A(RE70+32)             address of v3 source
000039C8  00000010                                    2634+       DC     A(16)                  result length
000039CC  00003A18                                    2635+REA70  DC     A(RE70)                result address
000039D0  00000000 00000000                           2636+       DS     FD                     gap
000039D8  00000000 00000000                           2637+V1070  DS     XL16                   V1 output
000039E0  00000000 00000000
000039E8  00000000 00000000                           2638+       DS     FD                     gap
                                                      2639+*
000039F0                                              2640+X70    DS     0F
000039F0  E310 5010 0014                   00000010   2641+       LGF    R1,V2ADDR              load v2 source
000039F6  E761 0000 0806                   00000000   2642+       VL     v22,0(R1)              use v22 to test decoder
000039FC  E310 5014 0014                   00000014   2643+       LGF    R1,V3ADDR              load v3 source
00003A02  E771 0000 0806                   00000000   2644+       VL     v23,0(R1)              use v23 to test decoder
00003A08  E766 7000 3E7A                              2645+       VESRAV V22,V22,V23,3           test instruction (dest is a source)
00003A0E  E760 5028 080E                   000039D8   2646+       VST    V22,V1070              save v1 output
00003A14  07FB                                        2647+       BR     R11                    return
00003A18                                              2648+RE70   DC     0F                     xl16 expected result
00003A18                                              2649+       DROP   R5
00003A18  FFE1E3E5 E7E9EBED                           2650        DC     XL16'FFE1E3E5E7E9EBED FFFFFE3E7EBEFF3F'     result
00003A20  FFFFFE3E 7EBEFF3F
00003A28  F0F1F2F3 F4F5F6F7                           2651        DC     XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'     v2
00003A30  F8F9FAFB FCFDFEFF
00003A38  00000000 00000007                           2652        DC     XL16'0000000000000007 0000000000000012'     v3
00003A40  00000000 00000012
                                                      2653
                                                      2654        VRR_C  VESRAV, 3
00003A48                                              2655+       DS     0FD
00003A48                         00003A48             2656+       USING  *,R5                   base for test data and test routine
00003A48  00003A88                                    2657+T71    DC     A(X71)                 address of test routine
00003A4C  0047                                        2658+       DC     H'71'                  test number
00003A4E  00                                          2659+       DC     X'00'
00003A4F  03                                          2660+       DC     HL1'3'                 m4
00003A50  E5C5E2D9 C1E54040                           2661+       DC     CL8'VESRAV'            instruction name
00003A58  00003AC0                                    2662+       DC     A(RE71+16)             address of v2 source
00003A5C  00003AD0                                    2663+       DC     A(RE71+32)             address of v3 source
00003A60  00000010                                    2664+       DC     A(16)                  result length
00003A64  00003AB0                                    2665+REA71  DC     A(RE71)                result address
00003A68  00000000 00000000                           2666+       DS     FD                     gap
00003A70  00000000 00000000                           2667+V1071  DS     XL16                   V1 output
00003A78  00000000 00000000
```

```
   LOC          OBJECT CODE       ADDR1      ADDR2      STMT

00003A80   00000000 00000000                           2668+         DS     FD              gap
                                                        2669+*
00003A88                                                2670+X71      DS     0F
00003A88   E310 5010 0014                   00000010    2671+         LGF    R1,V2ADDR       load v2 source
00003A8E   E761 0000 0806                   00000000    2672+         VL     v22,0(R1)       use v22 to test decoder
00003A94   E310 5014 0014                   00000014    2673+         LGF    R1,V3ADDR       load v3 source
00003A9A   E771 0000 0806                   00000000    2674+         VL     v23,0(R1)       use v23 to test decoder
00003AA0   E766 7000 3E7A                               2675+         VESRAV V22,V22,V23,3    test instruction (dest is a source)
00003AA6   E760 5028 080E                   00003A70    2676+         VST    V22,V1071       save v1 output
00003AAC   07FB                                         2677+         BR     R11             return
00003AB0                                                2678+RE71     DC     0F              xl16 expected result
00003AB0                                                2679+         DROP   R5
00003AB0   FFFFFFFF FC3C7CBC                             2680         DC     XL16'FFFFFFFFFC3C7CBC FFFFFFFFFFFFFF1F'    result
00003AB8   FFFFFFFF FFFFFF1F
00003AC0   F0F1F2F3 F4F5F6F7                             2681         DC     XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'    v2
00003AC8   F8F9FAFB FCFDFEFF
00003AD0   00000000 00000022                             2682         DC     XL16'0000000000000022 0000000000000033'   v3
00003AD8   00000000 00000033
                                                         2683
                                                         2684
00003AE0                                                 2685         VRR_C  VESRAV,3
00003AE0                                                 2686+        DS     0FD
00003AE0                            00003AE0             2687+        USING  *,R5            base for test data and test routine
00003AE0   00003B20                                      2688+T72     DC     A(X72)          address of test routine
00003AE4   0048                                          2689+        DC     H'72'           test number
00003AE6   00                                            2690+        DC     X'00'
00003AE7   03                                            2691+        DC     HL1'3'          m4
00003AE8   E5C5E2D9 C1E54040                              2692+        DC     CL8'VESRAV'     instruction name
00003AF0   00003B58                                      2693+        DC     A(RE72+16)      address of v2 source
00003AF4   00003B68                                      2694+        DC     A(RE72+32)      address of v3 source
00003AF8   00000010                                      2695+        DC     A(16)           result length
00003AFC   00003B48                                      2696+REA72   DC     A(RE72)         result address
00003B00   00000000 00000000                             2697+        DS     FD              gap
00003B08   00000000 00000000                             2698+V1072   DS     XL16            V1 output
00003B10   00000000 00000000
00003B18   00000000 00000000                             2699+        DS     FD              gap
                                                         2700+*
00003B20                                                 2701+X72     DS     0F
00003B20   E310 5010 0014                   00000010     2702+        LGF    R1,V2ADDR       load v2 source
00003B26   E761 0000 0806                   00000000     2703+        VL     v22,0(R1)       use v22 to test decoder
00003B2C   E310 5014 0014                   00000014     2704+        LGF    R1,V3ADDR       load v3 source
00003B32   E771 0000 0806                   00000000     2705+        VL     v23,0(R1)       use v23 to test decoder
00003B38   E766 7000 3E7A                                2706+        VESRAV V22,V22,V23,3    test instruction (dest is a source)
00003B3E   E760 5028 080E                   00003B08     2707+        VST    V22,V1072       save v1 output
00003B44   07FB                                          2708+        BR     R11             return
00003B48                                                 2709+RE72    DC     0F              xl16 expected result
00003B48                                                 2710+        DROP   R5
00003B48   FFE00000 00000000                              2711        DC     XL16'FFE0000000000000 FFF0000000000000'   result
00003B50   FFF00000 00000000
00003B58   80000000 00000000                              2712        DC     XL16'8000000000000000 8000000000000000'   v2
00003B60   80000000 00000000
00003B68   F0000000 0000000A                              2713        DC     XL16'F00000000000000A F00000000000000B'   v3
00003B70   F0000000 0000000B
                                                          2714
                                                          2715        VRR_C  VESRAV,3
00003B78                                                  2716+       DS     0FD
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003B78		00003B78		2717+		USING *,R5	base for test data and test routine
00003B78	00003BB8			2718+T73	DC	A(X73)	address of test routine
00003B7C	0049			2719+	DC	H'73'	test number
00003B7E	00			2720+	DC	X'00'	
00003B7F	03			2721+	DC	HL1'3'	m4
00003B80	E5C5E2D9 C1E54040			2722+	DC	CL8'VESRAV'	instruction name
00003B88	00003BF0			2723+	DC	A(RE73+16)	address of v2 source
00003B8C	00003C00			2724+	DC	A(RE73+32)	address of v3 source
00003B90	00000010			2725+	DC	A(16)	result length
00003B94	00003BE0			2726+REA73	DC	A(RE73)	result address
00003B98	00000000 00000000			2727+	DS	FD	gap
00003BA0	00000000 00000000			2728+V1073	DS	XL16	V1 output
00003BA8	00000000 00000000						
00003BB0	00000000 00000000			2729+	DS	FD	gap
				2730+*			
00003BB8				2731+X73	DS	0F	
00003BB8	E310 5010 0014		00000010	2732+	LGF	R1,V2ADDR	load v2 source
00003BBE	E761 0000 0806		00000000	2733+	VL	v22,0(R1)	use v22 to test decoder
00003BC4	E310 5014 0014		00000014	2734+	LGF	R1,V3ADDR	load v3 source
00003BCA	E771 0000 0806		00000000	2735+	VL	v23,0(R1)	use v23 to test decoder
00003BD0	E766 7000 3E7A			2736+	VESRAV V22,V22,V23,3		test instruction (dest is a source)
00003BD6	E760 5028 080E		00003BA0	2737+	VST	V22,V1073	save v1 output
00003BDC	07FB			2738+	BR	R11	return
00003BE0				2739+RE73	DC	0F	xl16 expected result
00003BE0				2740+	DROP	R5	
00003BE0	FFFFFFFF FC3C7CBC			2741	DC	XL16'FFFFFFFFFC3C7CBC FFFFFFFFFFFFFF1F'	result
00003BE8	FFFFFFFF FFFFFF1F						
00003BF0	F0F1F2F3 F4F5F6F7			2742	DC	XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	v2
00003BF8	F8F9FAFB FCFDFEFF						
00003C00	F0000000 00000022			2743	DC	XL16'F000000000000022 F000000000000033'	v3
00003C08	F0000000 00000033						
				2744			
				2745			
				2746			
				2747			
00003C10	00000000			2748	DC	F'0'	END OF TABLE
00003C14	00000000			2749	DC	F'0'	
				2750 *			
				2751 * table of pointers to individual load test			
				2752 *			
00003C18				2753 E7TESTS	DS	0F	
				2754		PTTABLE	
00003C18				2755+TTABLE	DS	0F	
00003C18	000010B8			2756+	DC	A(T1)	
00003C1C	00001150			2757+	DC	A(T2)	
00003C20	000011E8			2758+	DC	A(T3)	
00003C24	00001280			2759+	DC	A(T4)	
00003C28	00001318			2760+	DC	A(T5)	
00003C2C	000013B0			2761+	DC	A(T6)	
00003C30	00001448			2762+	DC	A(T7)	
00003C34	000014E0			2763+	DC	A(T8)	
00003C38	00001578			2764+	DC	A(T9)	
00003C3C	00001610			2765+	DC	A(T10)	
00003C40	000016A8			2766+	DC	A(T11)	
00003C44	00001740			2767+	DC	A(T12)	
00003C48	000017D8			2768+	DC	A(T13)	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00003C4C	00001870			2769+	DC	A(T14)
00003C50	00001908			2770+	DC	A(T15)
00003C54	000019A0			2771+	DC	A(T16)
00003C58	00001A38			2772+	DC	A(T17)
00003C5C	00001AD0			2773+	DC	A(T18)
00003C60	00001B68			2774+	DC	A(T19)
00003C64	00001C00			2775+	DC	A(T20)
00003C68	00001C98			2776+	DC	A(T21)
00003C6C	00001D30			2777+	DC	A(T22)
00003C70	00001DC8			2778+	DC	A(T23)
00003C74	00001E60			2779+	DC	A(T24)
00003C78	00001EF8			2780+	DC	A(T25)
00003C7C	00001F90			2781+	DC	A(T26)
00003C80	00002028			2782+	DC	A(T27)
00003C84	000020C0			2783+	DC	A(T28)
00003C88	00002158			2784+	DC	A(T29)
00003C8C	000021F0			2785+	DC	A(T30)
00003C90	00002288			2786+	DC	A(T31)
00003C94	00002320			2787+	DC	A(T32)
00003C98	000023B8			2788+	DC	A(T33)
00003C9C	00002450			2789+	DC	A(T34)
00003CA0	000024E8			2790+	DC	A(T35)
00003CA4	00002580			2791+	DC	A(T36)
00003CA8	00002618			2792+	DC	A(T37)
00003CAC	000026B0			2793+	DC	A(T38)
00003CB0	00002748			2794+	DC	A(T39)
00003CB4	000027E0			2795+	DC	A(T40)
00003CB8	00002878			2796+	DC	A(T41)
00003CBC	00002910			2797+	DC	A(T42)
00003CC0	000029A8			2798+	DC	A(T43)
00003CC4	00002A40			2799+	DC	A(T44)
00003CC8	00002AD8			2800+	DC	A(T45)
00003CCC	00002B70			2801+	DC	A(T46)
00003CD0	00002C08			2802+	DC	A(T47)
00003CD4	00002CA0			2803+	DC	A(T48)
00003CD8	00002D38			2804+	DC	A(T49)
00003CDC	00002DD0			2805+	DC	A(T50)
00003CE0	00002E68			2806+	DC	A(T51)
00003CE4	00002F00			2807+	DC	A(T52)
00003CE8	00002F98			2808+	DC	A(T53)
00003CEC	00003030			2809+	DC	A(T54)
00003CF0	000030C8			2810+	DC	A(T55)
00003CF4	00003160			2811+	DC	A(T56)
00003CF8	000031F8			2812+	DC	A(T57)
00003CFC	00003290			2813+	DC	A(T58)
00003D00	00003328			2814+	DC	A(T59)
00003D04	000033C0			2815+	DC	A(T60)
00003D08	00003458			2816+	DC	A(T61)
00003D0C	000034F0			2817+	DC	A(T62)
00003D10	00003588			2818+	DC	A(T63)
00003D14	00003620			2819+	DC	A(T64)
00003D18	000036B8			2820+	DC	A(T65)
00003D1C	00003750			2821+	DC	A(T66)
00003D20	000037E8			2822+	DC	A(T67)
00003D24	00003880			2823+	DC	A(T68)
00003D28	00003918			2824+	DC	A(T69)

```
  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

00003D2C  000039B0                              2825+          DC      A(T70)
00003D30  00003A48                              2826+          DC      A(T71)
00003D34  00003AE0                              2827+          DC      A(T72)
00003D38  00003B78                              2828+          DC      A(T73)
                                                2829+*
00003D3C  00000000                              2830+          DC      A(0)              END OF TABLE
00003D40  00000000                              2831+          DC      A(0)
                                                2832
00003D44  00000000                              2833           DC      F'0'      END OF TABLE
00003D48  00000000                              2834           DC      F'0'
```

```
  LOC        OBJECT CODE      ADDR1      ADDR2      STMT

                                                    2836 ****************************************************************************
                                                    2837 *          Register equates
                                                    2838 ****************************************************************************

                             00000000   00000001    2840 R0       EQU   0
                             00000001   00000001    2841 R1       EQU   1
                             00000002   00000001    2842 R2       EQU   2
                             00000003   00000001    2843 R3       EQU   3
                             00000004   00000001    2844 R4       EQU   4
                             00000005   00000001    2845 R5       EQU   5
                             00000006   00000001    2846 R6       EQU   6
                             00000007   00000001    2847 R7       EQU   7
                             00000008   00000001    2848 R8       EQU   8
                             00000009   00000001    2849 R9       EQU   9
                             0000000A   00000001    2850 R10      EQU   10
                             0000000B   00000001    2851 R11      EQU   11
                             0000000C   00000001    2852 R12      EQU   12
                             0000000D   00000001    2853 R13      EQU   13
                             0000000E   00000001    2854 R14      EQU   14
                             0000000F   00000001    2855 R15      EQU   15


                                                    2857 ****************************************************************************
                                                    2858 *          Register equates
                                                    2859 ****************************************************************************

                             00000000   00000001    2861 V0       EQU   0
                             00000001   00000001    2862 V1       EQU   1
                             00000002   00000001    2863 V2       EQU   2
                             00000003   00000001    2864 V3       EQU   3
                             00000004   00000001    2865 V4       EQU   4
                             00000005   00000001    2866 V5       EQU   5
                             00000006   00000001    2867 V6       EQU   6
                             00000007   00000001    2868 V7       EQU   7
                             00000008   00000001    2869 V8       EQU   8
                             00000009   00000001    2870 V9       EQU   9
                             0000000A   00000001    2871 V10      EQU   10
                             0000000B   00000001    2872 V11      EQU   11
                             0000000C   00000001    2873 V12      EQU   12
                             0000000D   00000001    2874 V13      EQU   13
                             0000000E   00000001    2875 V14      EQU   14
                             0000000F   00000001    2876 V15      EQU   15
                             00000010   00000001    2877 V16      EQU   16
                             00000011   00000001    2878 V17      EQU   17
                             00000012   00000001    2879 V18      EQU   18
                             00000013   00000001    2880 V19      EQU   19
                             00000014   00000001    2881 V20      EQU   20
                             00000015   00000001    2882 V21      EQU   21
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LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                          00000016  00000001  2883 V22      EQU    22
                          00000017  00000001  2884 V23      EQU    23
                          00000018  00000001  2885 V24      EQU    24
                          00000019  00000001  2886 V25      EQU    25
                          0000001A  00000001  2887 V26      EQU    26
                          0000001B  00000001  2888 V27      EQU    27
                          0000001C  00000001  2889 V28      EQU    28
                          0000001D  00000001  2890 V29      EQU    29
                          0000001E  00000001  2891 V30      EQU    30
                          0000001F  00000001  2892 V31      EQU    31
                                              2893
                                              2894          END
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES											
BEGIN	I	00000200	2	157	123	153	154	155								
CTLR0	F	0000048C	4	352	167	168	169	170								
DECNUM	C	00001073	16	403	267	269	275	277								
E7TEST	4	00000000	64	417	216											
E7TESTS	F	00003C18	4	2753	209											
EDIT	X	00001047	18	398	268	276										
ENDTEST	U	0000031E	1	253	214											
EOJ	I	00000470	4	342	202	256										
EOJPSW	D	00000460	8	340	342											
FAILCONT	U	0000030E	1	243												
FAILED	F	00001000	4	380	245	254										
FAILMSG	U	0000030A	1	237	227											
FAILPSW	D	00000478	8	344	346											
FAILTEST	I	00000488	4	346	257											
FB0001	F	00000280	8	186	190	191	193									
IMAGE	1	00000000	15692	0												
K	U	00000400	1	364	365	366	367									
K64	U	00010000	1	366												
M4	U	00000007	1	421	274											
MB	U	00100000	1	367												
MSG	I	000003A8	4	302	201	285										
MSGCMD	C	000003F6	9	332	315	316										
MSGMSG	C	000003FF	95	333	309	330	307									
MSGMVC	I	000003F0	6	330	313											
MSGOK	I	000003BE	2	311	308											
MSGRET	I	000003DE	4	326	319	322										
MSGSAVE	F	000003E4	4	329	305	326										
NEXTE7	U	000002D4	1	211	230	248										
OPNAME	C	00000008	8	423	272											
PAGE	U	00001000	1	365												
PRT3	C	0000105D	18	401	268	269	270	276	277	278						
PRTLINE	C	00001008	16	386	393	284										
PRTLNG	U	0000003F	1	393	283											
PRTM4	C	00001044	2	391	278											
PRTNAME	C	00001033	8	389	272											
PRTNUM	C	00001018	3	387	270											
R0	U	00000000	1	2840	117	167	170	190	192	193	194	199	218	219	244	245	282
					283	286	302	305	307	309	311	326				
R1	U	00000001	1	2841	200	225	226	254	255	284	316	330	547	548	549	550	577
					578	579	580	607	608	609	610	637	638	639	640	668	669
					670	671	698	699	700	701	728	729	730	731	758	759	760
					761	788	789	790	791	818	819	820	821	849	850	851	852
					879	880	881	882	909	910	911	912	939	940	941	942	969
					970	971	972	999	1000	1001	1002	1030	1031	1032	1033	1060	1061
					1062	1063	1090	1091	1092	1093	1120	1121	1122	1123	1150	1151	1152
					1153	1181	1182	1183	1184	1211	1212	1213	1214	1246	1247	1248	1249
					1276	1277	1278	1279	1306	1307	1308	1309	1336	1337	1338	1339	1367
					1368	1369	1370	1397	1398	1399	1400	1427	1428	1429	1430	1457	1458
					1459	1460	1487	1488	1489	1490	1517	1518	1519	1520	1548	1549	1550
					1551	1578	1579	1580	1581	1608	1609	1610	1611	1638	1639	1640	1641
					1668	1669	1670	1671	1698	1699	1700	1701	1729	1730	1731	1732	1759
					1760	1761	1762	1789	1790	1791	1792	1819	1820	1821	1822	1849	1850
					1851	1852	1880	1881	1882	1883	1910	1911	1912	1913	1946	1947	1948
					1949	1976	1977	1978	1979	2006	2007	2008	2009	2036	2037	2038	2039
					2066	2067	2068	2069	2098	2099	2100	2101	2128	2129	2130	2131	2158
					2159	2160	2161	2188	2189	2190	2191	2218	2219	2220	2221	2248	2249

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					2250 2251 2278 2279 2280 2281 2309 2310 2311 2312 2339 2340 2341
					2342 2369 2370 2371 2372 2399 2400 2401 2402 2429 2430 2431 2432
					2459 2460 2461 2462 2489 2490 2491 2492 2521 2522 2523 2524 2551
					2552 2553 2554 2581 2582 2583 2584 2611 2612 2613 2614 2641 2642
					2643 2644 2671 2672 2673 2674 2702 2703 2704 2705 2732 2733 2734
					2735
R10	U	0000000A	1	2850	155 164 165
R11	U	0000000B	1	2851	222 223 553 583 613 643 674 704 734 764 794 824 855
					885 915 945 975 1005 1036 1066 1096 1126 1156 1187 1217 1252
					1282 1312 1342 1373 1403 1433 1463 1493 1523 1554 1584 1614 1644
					1674 1704 1735 1765 1795 1825 1855 1886 1916 1952 1982 2012 2042
					2072 2104 2134 2164 2194 2224 2254 2284 2315 2345 2375 2405 2435
					2465 2495 2527 2557 2587 2617 2647 2677 2708 2738
R12	U	0000000C	1	2852	209 212 229 247
R13	U	0000000D	1	2853	
R14	U	0000000E	1	2854	
R15	U	0000000F	1	2855	238 263 289 290
R2	U	00000002	1	2842	201 266 267 274 275 282 285 286 303 305 311 312 313
					315 321 326 327
R3	U	00000003	1	2843	
R4	U	00000004	1	2844	
R5	U	00000005	1	2845	212 213 216 264 288 532 555 562 585 592 615 622 645
					653 676 683 706 713 736 743 766 773 796 803 826 834
					857 864 887 894 917 924 947 954 977 984 1007 1015 1038
					1045 1068 1075 1098 1105 1128 1135 1158 1166 1189 1196 1219 1231
					1254 1261 1284 1291 1314 1321 1344 1352 1375 1382 1405 1412 1435
					1442 1465 1472 1495 1502 1525 1533 1556 1563 1586 1593 1616 1623
					1646 1653 1676 1683 1706 1714 1737 1744 1767 1774 1797 1804 1827
					1834 1857 1865 1888 1895 1918 1931 1954 1961 1984 1991 2014 2021
					2044 2051 2074 2083 2106 2113 2136 2143 2166 2173 2196 2203 2226
					2233 2256 2263 2286 2294 2317 2324 2347 2354 2377 2384 2407 2414
					2437 2444 2467 2474 2497 2506 2529 2536 2559 2566 2589 2596 2619
					2626 2649 2656 2679 2687 2710 2717 2740
R6	U	00000006	1	2846	
R7	U	00000007	1	2847	
R8	U	00000008	1	2848	153 157 158 159 161
R9	U	00000009	1	2849	154 161 162 164
RE1	F	00001120	4	554	538 539 541
RE10	F	00001678	4	825	809 810 812
RE11	F	00001710	4	856	840 841 843
RE12	F	000017A8	4	886	870 871 873
RE13	F	00001840	4	916	900 901 903
RE14	F	000018D8	4	946	930 931 933
RE15	F	00001970	4	976	960 961 963
RE16	F	00001A08	4	1006	990 991 993
RE17	F	00001AA0	4	1037	1021 1022 1024
RE18	F	00001B38	4	1067	1051 1052 1054
RE19	F	00001BD0	4	1097	1081 1082 1084
RE2	F	000011B8	4	584	568 569 571
RE20	F	00001C68	4	1127	1111 1112 1114
RE21	F	00001D00	4	1157	1141 1142 1144
RE22	F	00001D98	4	1188	1172 1173 1175
RE23	F	00001E30	4	1218	1202 1203 1205
RE24	F	00001EC8	4	1253	1237 1238 1240
RE25	F	00001F60	4	1283	1267 1268 1270
RE26	F	00001FF8	4	1313	1297 1298 1300

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
RE27	F	00002090	4	1343	1327	1328	1330
RE28	F	00002128	4	1374	1358	1359	1361
RE29	F	000021C0	4	1404	1388	1389	1391
RE3	F	00001250	4	614	598	599	601
RE30	F	00002258	4	1434	1418	1419	1421
RE31	F	000022F0	4	1464	1448	1449	1451
RE32	F	00002388	4	1494	1478	1479	1481
RE33	F	00002420	4	1524	1508	1509	1511
RE34	F	000024B8	4	1555	1539	1540	1542
RE35	F	00002550	4	1585	1569	1570	1572
RE36	F	000025E8	4	1615	1599	1600	1602
RE37	F	00002680	4	1645	1629	1630	1632
RE38	F	00002718	4	1675	1659	1660	1662
RE39	F	000027B0	4	1705	1689	1690	1692
RE4	F	000012E8	4	644	628	629	631
RE40	F	00002848	4	1736	1720	1721	1723
RE41	F	000028E0	4	1766	1750	1751	1753
RE42	F	00002978	4	1796	1780	1781	1783
RE43	F	00002A10	4	1826	1810	1811	1813
RE44	F	00002AA8	4	1856	1840	1841	1843
RE45	F	00002B40	4	1887	1871	1872	1874
RE46	F	00002BD8	4	1917	1901	1902	1904
RE47	F	00002C70	4	1953	1937	1938	1940
RE48	F	00002D08	4	1983	1967	1968	1970
RE49	F	00002DA0	4	2013	1997	1998	2000
RE5	F	00001380	4	675	659	660	662
RE50	F	00002E38	4	2043	2027	2028	2030
RE51	F	00002ED0	4	2073	2057	2058	2060
RE52	F	00002F68	4	2105	2089	2090	2092
RE53	F	00003000	4	2135	2119	2120	2122
RE54	F	00003098	4	2165	2149	2150	2152
RE55	F	00003130	4	2195	2179	2180	2182
RE56	F	000031C8	4	2225	2209	2210	2212
RE57	F	00003260	4	2255	2239	2240	2242
RE58	F	000032F8	4	2285	2269	2270	2272
RE59	F	00003390	4	2316	2300	2301	2303
RE6	F	00001418	4	705	689	690	692
RE60	F	00003428	4	2346	2330	2331	2333
RE61	F	000034C0	4	2376	2360	2361	2363
RE62	F	00003558	4	2406	2390	2391	2393
RE63	F	000035F0	4	2436	2420	2421	2423
RE64	F	00003688	4	2466	2450	2451	2453
RE65	F	00003720	4	2496	2480	2481	2483
RE66	F	000037B8	4	2528	2512	2513	2515
RE67	F	00003850	4	2558	2542	2543	2545
RE68	F	000038E8	4	2588	2572	2573	2575
RE69	F	00003980	4	2618	2602	2603	2605
RE7	F	000014B0	4	735	719	720	722
RE70	F	00003A18	4	2648	2632	2633	2635
RE71	F	00003AB0	4	2678	2662	2663	2665
RE72	F	00003B48	4	2709	2693	2694	2696
RE73	F	00003BE0	4	2739	2723	2724	2726
RE8	F	00001548	4	765	749	750	752
RE9	F	000015E0	4	795	779	780	782
REA1	A	000010D4	4	541			
REA10	A	0000162C	4	812			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA11	A	000016C4	4	843	
REA12	A	0000175C	4	873	
REA13	A	000017F4	4	903	
REA14	A	0000188C	4	933	
REA15	A	00001924	4	963	
REA16	A	000019BC	4	993	
REA17	A	00001A54	4	1024	
REA18	A	00001AEC	4	1054	
REA19	A	00001B84	4	1084	
REA2	A	0000116C	4	571	
REA20	A	00001C1C	4	1114	
REA21	A	00001CB4	4	1144	
REA22	A	00001D4C	4	1175	
REA23	A	00001DE4	4	1205	
REA24	A	00001E7C	4	1240	
REA25	A	00001F14	4	1270	
REA26	A	00001FAC	4	1300	
REA27	A	00002044	4	1330	
REA28	A	000020DC	4	1361	
REA29	A	00002174	4	1391	
REA3	A	00001204	4	601	
REA30	A	0000220C	4	1421	
REA31	A	000022A4	4	1451	
REA32	A	0000233C	4	1481	
REA33	A	000023D4	4	1511	
REA34	A	0000246C	4	1542	
REA35	A	00002504	4	1572	
REA36	A	0000259C	4	1602	
REA37	A	00002634	4	1632	
REA38	A	000026CC	4	1662	
REA39	A	00002764	4	1692	
REA4	A	0000129C	4	631	
REA40	A	000027FC	4	1723	
REA41	A	00002894	4	1753	
REA42	A	0000292C	4	1783	
REA43	A	000029C4	4	1813	
REA44	A	00002A5C	4	1843	
REA45	A	00002AF4	4	1874	
REA46	A	00002B8C	4	1904	
REA47	A	00002C24	4	1940	
REA48	A	00002CBC	4	1970	
REA49	A	00002D54	4	2000	
REA5	A	00001334	4	662	
REA50	A	00002DEC	4	2030	
REA51	A	00002E84	4	2060	
REA52	A	00002F1C	4	2092	
REA53	A	00002FB4	4	2122	
REA54	A	0000304C	4	2152	
REA55	A	000030E4	4	2182	
REA56	A	0000317C	4	2212	
REA57	A	00003214	4	2242	
REA58	A	000032AC	4	2272	
REA59	A	00003344	4	2303	
REA6	A	000013CC	4	692	
REA60	A	000033DC	4	2333	
REA61	A	00003474	4	2363	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA62	A	0000350C	4	2393		
REA63	A	000035A4	4	2423		
REA64	A	0000363C	4	2453		
REA65	A	000036D4	4	2483		
REA66	A	0000376C	4	2515		
REA67	A	00003804	4	2545		
REA68	A	0000389C	4	2575		
REA69	A	00003934	4	2605		
REA7	A	00001464	4	722		
REA70	A	000039CC	4	2635		
REA71	A	00003A64	4	2665		
REA72	A	00003AFC	4	2696		
REA73	A	00003B94	4	2726		
REA8	A	000014FC	4	752		
REA9	A	00001594	4	782		
READDR	A	0000001C	4	427	225	
REG2LOW	U	000000DD	1	370		
REG2PATT	U	AABBCCDD	1	369		
RELEN	A	00000018	4	426		
RPTDWSAV	D	00000398	8	295	282	286
RPTERROR	I	0000032C	4	263	238	
RPTSAVE	F	00000390	4	292	263	289
RPTSVR5	F	00000394	4	293	264	288
SKL0001	U	0000004E	1	183	199	
SKT0001	C	0000022A	20	180	183	200
SVOLDPSW	U	00000140	0	119		
T1	A	000010B8	4	533	2756	
T10	A	00001610	4	804	2765	
T11	A	000016A8	4	835	2766	
T12	A	00001740	4	865	2767	
T13	A	000017D8	4	895	2768	
T14	A	00001870	4	925	2769	
T15	A	00001908	4	955	2770	
T16	A	000019A0	4	985	2771	
T17	A	00001A38	4	1016	2772	
T18	A	00001AD0	4	1046	2773	
T19	A	00001B68	4	1076	2774	
T2	A	00001150	4	563	2757	
T20	A	00001C00	4	1106	2775	
T21	A	00001C98	4	1136	2776	
T22	A	00001D30	4	1167	2777	
T23	A	00001DC8	4	1197	2778	
T24	A	00001E60	4	1232	2779	
T25	A	00001EF8	4	1262	2780	
T26	A	00001F90	4	1292	2781	
T27	A	00002028	4	1322	2782	
T28	A	000020C0	4	1353	2783	
T29	A	00002158	4	1383	2784	
T3	A	000011E8	4	593	2758	
T30	A	000021F0	4	1413	2785	
T31	A	00002288	4	1443	2786	
T32	A	00002320	4	1473	2787	
T33	A	000023B8	4	1503	2788	
T34	A	00002450	4	1534	2789	
T35	A	000024E8	4	1564	2790	
T36	A	00002580	4	1594	2791	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
T37	A	00002618	4	1624	2792	
T38	A	000026B0	4	1654	2793	
T39	A	00002748	4	1684	2794	
T4	A	00001280	4	623	2759	
T40	A	000027E0	4	1715	2795	
T41	A	00002878	4	1745	2796	
T42	A	00002910	4	1775	2797	
T43	A	000029A8	4	1805	2798	
T44	A	00002A40	4	1835	2799	
T45	A	00002AD8	4	1866	2800	
T46	A	00002B70	4	1896	2801	
T47	A	00002C08	4	1932	2802	
T48	A	00002CA0	4	1962	2803	
T49	A	00002D38	4	1992	2804	
T5	A	00001318	4	654	2760	
T50	A	00002DD0	4	2022	2805	
T51	A	00002E68	4	2052	2806	
T52	A	00002F00	4	2084	2807	
T53	A	00002F98	4	2114	2808	
T54	A	00003030	4	2144	2809	
T55	A	000030C8	4	2174	2810	
T56	A	00003160	4	2204	2811	
T57	A	000031F8	4	2234	2812	
T58	A	00003290	4	2264	2813	
T59	A	00003328	4	2295	2814	
T6	A	000013B0	4	684	2761	
T60	A	000033C0	4	2325	2815	
T61	A	00003458	4	2355	2816	
T62	A	000034F0	4	2385	2817	
T63	A	00003588	4	2415	2818	
T64	A	00003620	4	2445	2819	
T65	A	000036B8	4	2475	2820	
T66	A	00003750	4	2507	2821	
T67	A	000037E8	4	2537	2822	
T68	A	00003880	4	2567	2823	
T69	A	00003918	4	2597	2824	
T7	A	00001448	4	714	2762	
T70	A	000039B0	4	2627	2825	
T71	A	00003A48	4	2657	2826	
T72	A	00003AE0	4	2688	2827	
T73	A	00003B78	4	2718	2828	
T8	A	000014E0	4	744	2763	
T9	A	00001578	4	774	2764	
TESTING	F	00001004	4	381	219	
TNUM	H	00000004	2	419	218	266
TSUB	A	00000000	4	418	222	
TTABLE	F	00003C18	4	2755		
V0	U	00000000	1	2861		
V1	U	00000001	1	2862	221	
V10	U	0000000A	1	2871		
V11	U	0000000B	1	2872		
V12	U	0000000C	1	2873		
V13	U	0000000D	1	2874		
V14	U	0000000E	1	2875		
V15	U	0000000F	1	2876		
V16	U	00000010	1	2877		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V17	U	00000011	1	2878	
V18	U	00000012	1	2879	
V19	U	00000013	1	2880	
V1FUDGE	X	00001094	16	410	221
V101	X	000010E0	16	543	552
V1010	X	00001638	16	814	823
V1011	X	000016D0	16	845	854
V1012	X	00001768	16	875	884
V1013	X	00001800	16	905	914
V1014	X	00001898	16	935	944
V1015	X	00001930	16	965	974
V1016	X	000019C8	16	995	1004
V1017	X	00001A60	16	1026	1035
V1018	X	00001AF8	16	1056	1065
V1019	X	00001B90	16	1086	1095
V102	X	00001178	16	573	582
V1020	X	00001C28	16	1116	1125
V1021	X	00001CC0	16	1146	1155
V1022	X	00001D58	16	1177	1186
V1023	X	00001DF0	16	1207	1216
V1024	X	00001E88	16	1242	1251
V1025	X	00001F20	16	1272	1281
V1026	X	00001FB8	16	1302	1311
V1027	X	00002050	16	1332	1341
V1028	X	000020E8	16	1363	1372
V1029	X	00002180	16	1393	1402
V103	X	00001210	16	603	612
V1030	X	00002218	16	1423	1432
V1031	X	000022B0	16	1453	1462
V1032	X	00002348	16	1483	1492
V1033	X	000023E0	16	1513	1522
V1034	X	00002478	16	1544	1553
V1035	X	00002510	16	1574	1583
V1036	X	000025A8	16	1604	1613
V1037	X	00002640	16	1634	1643
V1038	X	000026D8	16	1664	1673
V1039	X	00002770	16	1694	1703
V104	X	000012A8	16	633	642
V1040	X	00002808	16	1725	1734
V1041	X	000028A0	16	1755	1764
V1042	X	00002938	16	1785	1794
V1043	X	000029D0	16	1815	1824
V1044	X	00002A68	16	1845	1854
V1045	X	00002B00	16	1876	1885
V1046	X	00002B98	16	1906	1915
V1047	X	00002C30	16	1942	1951
V1048	X	00002CC8	16	1972	1981
V1049	X	00002D60	16	2002	2011
V105	X	00001340	16	664	673
V1050	X	00002DF8	16	2032	2041
V1051	X	00002E90	16	2062	2071
V1052	X	00002F28	16	2094	2103
V1053	X	00002FC0	16	2124	2133
V1054	X	00003058	16	2154	2163
V1055	X	000030F0	16	2184	2193
V1056	X	00003188	16	2214	2223

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V1057	X	00003220	16	2244	2253												
V1058	X	000032B8	16	2274	2283												
V1059	X	00003350	16	2305	2314												
V106	X	000013D8	16	694	703												
V1060	X	000033E8	16	2335	2344												
V1061	X	00003480	16	2365	2374												
V1062	X	00003518	16	2395	2404												
V1063	X	000035B0	16	2425	2434												
V1064	X	00003648	16	2455	2464												
V1065	X	000036E0	16	2485	2494												
V1066	X	00003778	16	2517	2526												
V1067	X	00003810	16	2547	2556												
V1068	X	000038A8	16	2577	2586												
V1069	X	00003940	16	2607	2616												
V107	X	00001470	16	724	733												
V1070	X	000039D8	16	2637	2646												
V1071	X	00003A70	16	2667	2676												
V1072	X	00003B08	16	2698	2707												
V1073	X	00003BA0	16	2728	2737												
V108	X	00001508	16	754	763												
V109	X	000015A0	16	784	793												
V10UTPUT	X	00000028	16	429	226												
V2	U	00000002	1	2863													
V20	U	00000014	1	2881													
V21	U	00000015	1	2882													
V22	U	00000016	1	2883	548	551	552	578	581	582	608	611	612	638	641	642	669
					672	673	699	702	703	729	732	733	759	762	763	789	792
					793	819	822	823	850	853	854	880	883	884	910	913	914
					940	943	944	970	973	974	1000	1003	1004	1031	1034	1035	1061
					1064	1065	1091	1094	1095	1121	1124	1125	1151	1154	1155	1182	1185
					1186	1212	1215	1216	1247	1250	1251	1277	1280	1281	1307	1310	1311
					1337	1340	1341	1368	1371	1372	1398	1401	1402	1428	1431	1432	1458
					1461	1462	1488	1491	1492	1518	1521	1522	1549	1552	1553	1579	1582
					1583	1609	1612	1613	1639	1642	1643	1669	1672	1673	1699	1702	1703
					1730	1733	1734	1760	1763	1764	1790	1793	1794	1820	1823	1824	1850
					1853	1854	1881	1884	1885	1911	1914	1915	1947	1950	1951	1977	1980
					1981	2007	2010	2011	2037	2040	2041	2067	2070	2071	2099	2102	2103
					2129	2132	2133	2159	2162	2163	2189	2192	2193	2219	2222	2223	2249
					2252	2253	2279	2282	2283	2310	2313	2314	2340	2343	2344	2370	2373
					2374	2400	2403	2404	2430	2433	2434	2460	2463	2464	2490	2493	2494
					2522	2525	2526	2552	2555	2556	2582	2585	2586	2612	2615	2616	2642
					2645	2646	2672	2675	2676	2703	2706	2707	2733	2736	2737		
V23	U	00000017	1	2884	550	551	580	581	610	611	640	641	671	672	701	702	731
					732	761	762	791	792	821	822	852	853	882	883	912	913
					942	943	972	973	1002	1003	1033	1034	1063	1064	1093	1094	1123
					1124	1153	1154	1184	1185	1214	1215	1249	1250	1279	1280	1309	1310
					1339	1340	1370	1371	1400	1401	1430	1431	1460	1461	1490	1491	1520
					1521	1551	1552	1581	1582	1611	1612	1641	1642	1671	1672	1701	1702
					1732	1733	1762	1763	1792	1793	1822	1823	1852	1853	1883	1884	1913
					1914	1949	1950	1979	1980	2009	2010	2039	2040	2069	2070	2101	2102
					2131	2132	2161	2162	2191	2192	2221	2222	2251	2252	2281	2282	2312
					2313	2342	2343	2372	2373	2402	2403	2432	2433	2462	2463	2492	2493
					2524	2525	2554	2555	2584	2585	2614	2615	2644	2645	2674	2675	2705
					2706	2735	2736										
V24	U	00000018	1	2885													
V25	U	00000019	1	2886													

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V26	U	0000001A	1	2887	
V27	U	0000001B	1	2888	
V28	U	0000001C	1	2889	
V29	U	0000001D	1	2890	
V2ADDR	A	00000010	4	424	547 577 607 637 668 698 728 758 788 818 849 879 909
					939 969 999 1030 1060 1090 1120 1150 1181 1211 1246 1276 1306
					1336 1367 1397 1427 1457 1487 1517 1548 1578 1608 1638 1668 1698
					1729 1759 1789 1819 1849 1880 1910 1946 1976 2006 2036 2066 2098
					2128 2158 2188 2218 2248 2278 2309 2339 2369 2399 2429 2459 2489
					2521 2551 2581 2611 2641 2671 2702 2732
V3	U	00000003	1	2864	
V30	U	0000001E	1	2891	
V31	U	0000001F	1	2892	
V3ADDR	A	00000014	4	425	549 579 609 639 670 700 730 760 790 820 851 881 911
					941 971 1001 1032 1062 1092 1122 1152 1183 1213 1248 1278 1308
					1338 1369 1399 1429 1459 1489 1519 1550 1580 1610 1640 1670 1700
					1731 1761 1791 1821 1851 1882 1912 1948 1978 2008 2038 2068 2100
					2130 2160 2190 2220 2250 2280 2311 2341 2371 2401 2431 2461 2491
					2523 2553 2583 2613 2643 2673 2704 2734
V4	U	00000004	1	2865	
V5	U	00000005	1	2866	
V6	U	00000006	1	2867	
V7	U	00000007	1	2868	
V8	U	00000008	1	2869	
V9	U	00000009	1	2870	
X0001	U	000002A8	1	189	177 190
X1	F	000010F8	4	546	533
X10	F	00001650	4	817	804
X11	F	000016E8	4	848	835
X12	F	00001780	4	878	865
X13	F	00001818	4	908	895
X14	F	000018B0	4	938	925
X15	F	00001948	4	968	955
X16	F	000019E0	4	998	985
X17	F	00001A78	4	1029	1016
X18	F	00001B10	4	1059	1046
X19	F	00001BA8	4	1089	1076
X2	F	00001190	4	576	563
X20	F	00001C40	4	1119	1106
X21	F	00001CD8	4	1149	1136
X22	F	00001D70	4	1180	1167
X23	F	00001E08	4	1210	1197
X24	F	00001EA0	4	1245	1232
X25	F	00001F38	4	1275	1262
X26	F	00001FD0	4	1305	1292
X27	F	00002068	4	1335	1322
X28	F	00002100	4	1366	1353
X29	F	00002198	4	1396	1383
X3	F	00001228	4	606	593
X30	F	00002230	4	1426	1413
X31	F	000022C8	4	1456	1443
X32	F	00002360	4	1486	1473
X33	F	000023F8	4	1516	1503
X34	F	00002490	4	1547	1534
X35	F	00002528	4	1577	1564
X36	F	000025C0	4	1607	1594

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES					
X37	F	00002658	4	1637	1624					
X38	F	000026F0	4	1667	1654					
X39	F	00002788	4	1697	1684					
X4	F	000012C0	4	636	623					
X40	F	00002820	4	1728	1715					
X41	F	000028B8	4	1758	1745					
X42	F	00002950	4	1788	1775					
X43	F	000029E8	4	1818	1805					
X44	F	00002A80	4	1848	1835					
X45	F	00002B18	4	1879	1866					
X46	F	00002BB0	4	1909	1896					
X47	F	00002C48	4	1945	1932					
X48	F	00002CE0	4	1975	1962					
X49	F	00002D78	4	2005	1992					
X5	F	00001358	4	667	654					
X50	F	00002E10	4	2035	2022					
X51	F	00002EA8	4	2065	2052					
X52	F	00002F40	4	2097	2084					
X53	F	00002FD8	4	2127	2114					
X54	F	00003070	4	2157	2144					
X55	F	00003108	4	2187	2174					
X56	F	000031A0	4	2217	2204					
X57	F	00003238	4	2247	2234					
X58	F	000032D0	4	2277	2264					
X59	F	00003368	4	2308	2295					
X6	F	000013F0	4	697	684					
X60	F	00003400	4	2338	2325					
X61	F	00003498	4	2368	2355					
X62	F	00003530	4	2398	2385					
X63	F	000035C8	4	2428	2415					
X64	F	00003660	4	2458	2445					
X65	F	000036F8	4	2488	2475					
X66	F	00003790	4	2520	2507					
X67	F	00003828	4	2550	2537					
X68	F	000038C0	4	2580	2567					
X69	F	00003958	4	2610	2597					
X7	F	00001488	4	727	714					
X70	F	000039F0	4	2640	2627					
X71	F	00003A88	4	2670	2657					
X72	F	00003B20	4	2701	2688					
X73	F	00003BB8	4	2731	2718					
X8	F	00001520	4	757	744					
X9	F	000015B8	4	787	774					
XC0001	U	000002D0	1	203	195					
ZVE7TST	J	00000000	15692	116	119	121	125	129	379	117
=A(E7TESTS)	A	00000498	4	357	209					
=AL2(L'MSGMSG)	R	000004A2	2	360	307					
=F'1'	F	0000049C	4	358	244					
=F'64'	F	00000494	4	356	194					
=H'0'	H	000004A0	2	359	302					

MACRO	DEFN	REFERENCES															
FCHECK	69	176															
PTTABLE	493	2754															
VRR_C	448	530	560	590	620	651	681	711	741	771	801	832	862	892	922	952	982	1013
		1043	1073	1103	1133	1164	1194	1229	1259	1289	1319	1350	1380	1410	1440	1470	1500	1531
		1561	1591	1621	1651	1681	1712	1742	1772	1802	1832	1863	1893	1929	1959	1989	2019	2049
		2081	2111	2141	2171	2201	2231	2261	2292	2322	2352	2382	2412	2442	2472	2504	2534	2564
		2594	2624	2654	2685	2715												

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    DESC       SYMBOL    SIZE       POS          ADDR

Entry: 0

Image      IMAGE    15692   0000-3D4B   0000-3D4B
   Region            15692   0000-3D4B   0000-3D4B
     CSECT   ZVE7TST  15692   0000-3D4B   0000-3D4B
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       STMT   FILE NAME

1   /home/tn529/sharedvfp/tests/zvector-e7-28-ShiftVector.asm

** NO ERRORS FOUND **