```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     2 ************************************************************************
                                                     3 *
                                                     4 *   Zvector E7 instruction tests for VRR-a encoded:
                                                     5 *
                                                     6 *   E75C VISTR  - Vector Isolate String
                                                     7 *
                                                     8 *        James Wekel February 2025
                                                     9 ************************************************************************


                                                    11 ************************************************************************
                                                    12 *
                                                    13 *        basic instruction tests
                                                    14 *
                                                    15 ************************************************************************
                                                    16 *  This program tests proper functioning of the z/arch E7 VRR-a
                                                    17 *  Vector Isolate String instruction.
                                                    18 *  Exceptions are not tested.
                                                    19 *
                                                    20 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                    21 *  obvious coding errors.  None of the tests are thorough.  They are
                                                    22 *  NOT designed to test all aspects of any of the instructions.
                                                    23 *
                                                    24 ************************************************************************
                                                    25 *
                                                    26 *    *Testcase zvector-e7-08-VISTR
                                                    27 *    *
                                                    28 *    *   Zvector E7 instruction tests for VRR-a encoded:
                                                    29 *    *
                                                    30 *    *   E75C VISTR  - Vector Isolate String
                                                    31 *    *
                                                    32 *    *   # ---------------------------------------------------------
                                                    33 *    *   #  This tests only the basic function of the instruction.
                                                    34 *    *   #  Exceptions are NOT tested.
                                                    35 *    *   # ---------------------------------------------------------
                                                    36 *    *
                                                    37 *    mainsize    2
                                                    38 *    numcpu      1
                                                    39 *    sysclear
                                                    40 *    archlvl     z/Arch
                                                    41 *
                                                    42 *    loadcore    "$(testpath)/zvector-e7-08-VISTR.core" 0x0
                                                    43 *
                                                    44 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                    45 *    runtest     10        #
                                                    46 *    diag8cmd    disable   # (reset back to default)
                                                    47 *
                                                    48 *    *Done
                                                    49 *
                                                    50 ************************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    52 ************************************************************************
                                                    53 *        FCHECK Macro - Is a Facility Bit set?
                                                    54 *
                                                    55 *        If the facility bit is NOT set, an message is issued and
                                                    56 *        the test is skipped.
                                                    57 *
                                                    58 *        Fcheck uses R0, R1 and R2
                                                    59 *
                                                    60 * eg.    FCHECK 134,'vector-packed-decimal'
                                                    61 ************************************************************************
                                                    62          MACRO
                                                    63          FCHECK &BITNO,&NOTSETMSG
                                                    64 .*                      &BITNO : facility bit number to check
                                                    65 .*                      &NOTSETMSG : 'facility name'
                                                    66          LCLA  &FBBYTE           Facility bit in Byte
                                                    67          LCLA  &FBBIT            Facility bit within Byte
                                                    68
                                                    69          LCLA  &L(8)
                                                    70 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                    71
                                                    72 &FBBYTE  SETA  &BITNO/8
                                                    73 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                    74 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                    75
                                                    76          B     X&SYSNDX
                                                    77 *                                       Fcheck data area
                                                    78 *                                       skip messgae
                                                    79 SKT&SYSNDX DC  C'    Skipping tests: '
                                                    80          DC    C&NOTSETMSG
                                                    81          DC    C' (bit &BITNO) is not installed.'
                                                    82 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                    83 *                                       facility bits
                                                    84          DS    FD                       gap
                                                    85 FB&SYSNDX DS   4FD
                                                    86          DS    FD                       gap
                                                    87 *
                                                    88 X&SYSNDX EQU *
                                                    89          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                    90          STFLE FB&SYSNDX                get facility bits
                                                    91
                                                    92          XGR   R0,R0
                                                    93          IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                    94          N     R0,=F'&FBBIT'            is bit set?
                                                    95          BNZ   XC&SYSNDX
                                                    96 *
                                                    97 * facility bit not set, issue message and exit
                                                    98 *
                                                    99          LA    R0,SKL&SYSNDX            message length
                                                   100          LA    R1,SKT&SYSNDX            message address
                                                   101          BAL   R2,MSG
                                                   102
                                                   103          B     EOJ
                                                   104 XC&SYSNDX EQU *
                                                   105          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     107 ************************************************************************
                                                     108 *        Low core PSWs
                                                     109 ************************************************************************
                               00000000  00002B5F    110 ZVE7TST  START 0
00000000                       00000000              111          USING ZVE7TST,R0            Low core addressability
                                                     112
                               00000140  00000000    113 SVOLDPSW EQU   ZVE7TST+X'140'        z/Arch Supervisor call old PSW

00000000                       00000000  000001A0    115          ORG   ZVE7TST+X'1A0'       z/Architecure RESTART PSW
000001A0  00000001 80000000                          116          DC    X'0000000180000000'
000001A8  00000000 00000200                          117          DC    AD(BEGIN)

000001B0                       000001B0  000001D0    119          ORG   ZVE7TST+X'1D0'       z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                          120          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                          121          DC    AD(X'DEAD')

000001E0                       000001E0  00000200    123          ORG   ZVE7TST+X'200'       Start of actual test program...

                                                     125 ************************************************************************
                                                     126 *                The actual "ZVE7TST" program itself...
                                                     127 ************************************************************************
                                                     128 *
                                                     129 *  Architecture Mode: z/Arch
                                                     130 *  Register Usage:
                                                     131 *
                                                     132 *    R0       (work)
                                                     133 *    R1-4     (work)
                                                     134 *    R5       Testing control table - current test base
                                                     135 *    R6-R7    (work)
                                                     136 *    R8       First base register
                                                     137 *    R9       Second base register
                                                     138 *    R10      Third base register
                                                     139 *    R11      E7TEST call return
                                                     140 *    R12      E7TESTS register
                                                     141 *    R13      (work)
                                                     142 *    R14      Subroutine call
                                                     143 *    R15      Secondary Subroutine call or work
                                                     144 *
                                                     145 ************************************************************************

00000200                       00000200              147          USING BEGIN,R8          FIRST Base Register
00000200                       00001200              148          USING BEGIN+4096,R9     SECOND Base Register
00000200                       00002200              149          USING BEGIN+8192,R10    THIRD Base Register

00000200  0580                                       151 BEGIN    BALR  R8,0              Initalize FIRST base register
00000202  0680                                       152          BCTR  R8,0              Initalize FIRST base register
00000204  0680                                       153          BCTR  R8,0              Initalize FIRST base register

00000206  4190 8800                    00000800      155          LA    R9,2048(,R8)      Initalize SECOND base register
0000020A  4190 9800                    00000800      156          LA    R9,2048(,R9)      Initalize SECOND base register
                                                     157
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000020E  41A0 9800                    00000800   158          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                    00000800   159          LA    R10,2048(,R10)   Initalize THIRD base register
                                                  160
00000216  B600 8354                    00000554   161          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 8355                    00000555   162          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 8355                    00000555   163          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 8354                    00000554   164          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                  165
                                                  166 ********************************************************************
                                                  167 * Is z/Architecture vector facility installed  (bit 129)
                                                  168 ********************************************************************
                                                  169
                                                  170          FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                    000002A8  171+         B     X0001
                                                  172+*                                  Fcheck data area
                                                  173+*                                  skip messgae
0000022A  40404040 E2928997                       174+SKT0001  DC    C'    Skipping tests: '
0000023E  A961C199 838889A3                       175+         DC    C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                       176+         DC    C' (bit 129) is not installed.'
                          0000004E  00000001      177+SKL0001  EQU   *-SKT0001
                                                  178+*                                  facility bits
00000278  00000000 00000000                       179+         DS    FD               gap
00000280  00000000 00000000                       180+FB0001   DS    4FD
000002A0  00000000 00000000                       181+         DS    FD               gap
                                                  182+*
                          000002A8  00000001      183+X0001    EQU   *
000002A8  4100 0004                    00000004   184+         LA    R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                    00000280   185+         STFLE FB0001           get facility bits
000002B0  B982 0000                               186+         XGR   R0,R0
000002B4  4300 8090                    00000290   187+         IC    R0,FB0001+16     get fbit byte
000002B8  5400 8368                    00000568   188+         N     R0,=F'64'        is bit set?
000002BC  4770 80D0                    000002D0   189+         BNZ   XC0001
                                                  190+*
                                                  191+* facility bit not set, issue message and exit
                                                  192+*
000002C0  4100 004E                    0000004E   193+         LA    R0,SKL0001       message length
000002C4  4110 802A                    0000022A   194+         LA    R1,SKT0001       message address
000002C8  4520 8270                    00000470   195+         BAL   R2,MSG
000002CC  47F0 8338                    00000538   196+         B     EOJ
                          000002D0  00000001      197+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    199 ********************************************************************************
                                                    200 *               Do tests in the E7TESTS table
                                                    201 ********************************************************************************
                                                    202
000002D0  58C0 836C                       0000056C  203           L     R12,=A(E7TESTS)          get table of test addresses
                                                    204
                                000002D4  00000001  205 NEXTE7    EQU   *
000002D4  5850 C000                       00000000  206           L     R5,0(0,R12)              get test address
000002D8  1255                                      207           LTR   R5,R5                       have a test?
000002DA  4780 8228                       00000428  208           BZ    ENDTEST                        done?
                                                    209
000002DE                        00000000            210           USING E7TEST,R5
                                                    211
000002DE  4800 5004                       00000004  212           LH    R0,TNUM                  save current test number
000002E2  5000 8E04                       00001004  213           ST    R0,TESTING               for easy reference
                                                    214
000002E6  E760 8EF8 0806                  000010F8  215           VL    V22,V1FUDGE              using V22 as v1 for instruction
000002EC  58B0 5000                       00000000  216           L     R11,TSUB                 get address of test routine
000002F0  05BB                                      217           BALR  R11,R11                  do test
                                                    218
000002F2  E310 500A 0076                  0000000A  219           LB    R1,CCMASK                (failure CC mask)
000002F8  8910 0004                       00000004  220           SLL   R1,4                     (shift to BC instr CC position)
000002FC  4410 8118                       00000318  221           EX    R1,TESTCC                fail if...
                                                    222
                                00000300  00000001  223 TESTREST EQU   *
00000300  E310 5030 0014                  00000030  224           LGF   R1,READDR                get address of expected result
00000306  D50F 5040 1000        00000040  00000000  225           CLC   V1OUTPUT,0(R1)           valid?
0000030C  4770 81B0                       000003B0  226           BNE   FAILMSG                     no, issue failed message
                                                    227
00000310  41C0 C004                       00000004  228           LA    R12,4(0,R12)             next test address
00000314  47F0 80D4                       000002D4  229           B     NEXTE7
                                                    230
00000318  4700 811C                       0000031C  231 TESTCC    BC    0,CCMSG                  (unexpected condition code?)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    233 ********************************************************************************
                                                    234 * cc was not as expected
                                                    235 ********************************************************************************
                               0000031C  00000001   236 CCMSG    EQU   *
                                                    237 *
                                                    238 * is CS set by test?
                                                    239 *
0000031C  E310 5008 0076                 00000008   240          LB    R1,M5                    Get M5
00000322  E310 8360 0080                 00000560   241          NG    R1,=D'1'                   issolate CS
00000328  4780 8100                      00000300   242          BZ    TESTREST                     not set?
                                                    243 *
                                                    244 * extract CC from extracted PSW
                                                    245 *
0000032C  5810 500C                      0000000C   246          L     R1,CCPSW
00000330  8810 000C                      0000000C   247          SRL   R1,12
00000334  5410 8370                      00000570   248          N     R1,=XL4'3'
00000338  4210 5014                      00000014   249          STC   R1,CCFOUND               save cc
                                                    250 *
                                                    251 * FILL IN MESSAGE
                                                    252 *
0000033C  4820 5004                      00000004   253          LH    R2,TNUM                  get test number and convert
00000340  4E20 8ED6                      000010D6   254          CVD   R2,DECNUM
00000344  D211 8EC0 8EAA  000010C0       000010AA   255          MVC   PRT3,EDIT
0000034A  DE11 8EC0 8ED6  000010C0       000010D6   256          ED    PRT3,DECNUM
00000350  D202 8E65 8ECD  00001065       000010CD   257          MVC   CCPRTNUM(3),PRT3+13      fill in message with test #
                                                    258
00000356  D207 8E82 5015  00001082       00000015   259          MVC   CCPRTNAME,OPNAME         fill in message with instruction
                                                    260
0000035C  B982 0022                                 261          XGR   R2,R2                    get CC as U8
00000360  4320 5009                      00000009   262          IC    R2,CC
00000364  4E20 8ED6                      000010D6   263          CVD   R2,DECNUM                and convert
00000368  D211 8EC0 8EAA  000010C0       000010AA   264          MVC   PRT3,EDIT
0000036E  DE11 8EC0 8ED6  000010C0       000010D6   265          ED    PRT3,DECNUM
00000374  D200 8E98 8ECF  00001098       000010CF   266          MVC   CCPRTEXP(1),PRT3+15      fill in message with CC field
                                                    267
0000037A  B982 0022                                 268          XGR   R2,R2                    get CCFOUND as U8
0000037E  4320 5014                      00000014   269          IC    R2,CCFOUND
00000382  4E20 8ED6                      000010D6   270          CVD   R2,DECNUM                and convert
00000386  D211 8EC0 8EAA  000010C0       000010AA   271          MVC   PRT3,EDIT
0000038C  DE11 8EC0 8ED6  000010C0       000010D6   272          ED    PRT3,DECNUM
00000392  D200 8EA8 8ECF  000010A8       000010CF   273          MVC   CCPRTGOT(1),PRT3+15      fill in message with ccfound
                                                    274
00000398  4100 0055                      00000055   275          LA    R0,CCPRTLNG              message length
0000039C  4110 8E55                      00001055   276          LA    R1,CCPRTLINE             messagfe address
000003A0  45F0 8236                      00000436   277          BAL   R15,RPTERROR
                                                    278
000003A4  5800 8374                      00000574   279          L     R0,=F'1'                 set failed test indicator
000003A8  5000 8E00                      00001000   280          ST    R0,FAILED
                                                    281
000003AC  47F0 8100                      00000300   282          B     TESTREST
                                                    283
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    285 ************************************************************************
                                                    286 * result not as expected:
                                                    287 *        issue message with test number, instruction under test
                                                    288 *              and instruction M3, M5
                                                    289 ************************************************************************
                                 000003B0  00000001 290 FAILMSG  EQU   *
000003B0  4820 5004                        00000004 291          LH    R2,TNUM              get test number and convert
000003B4  4E20 8ED6                        000010D6 292          CVD   R2,DECNUM
000003B8  D211 8EC0 8EAA       000010C0   000010AA 293          MVC   PRT3,EDIT
000003BE  DE11 8EC0 8ED6       000010C0   000010D6 294          ED    PRT3,DECNUM
000003C4  D202 8E18 8ECD       00001018   000010CD 295          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    296
000003CA  D207 8E33 5015       00001033   00000015 297          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    298
000003D0  B982 0022                                 299          XGR   R2,R2                get M3 as U8
000003D4  4320 5007                        00000007 300          IC    R2,M3
000003D8  4E20 8ED6                        000010D6 301          CVD   R2,DECNUM            and convert
000003DC  D211 8EC0 8EAA       000010C0   000010AA 302          MVC   PRT3,EDIT
000003E2  DE11 8EC0 8ED6       000010C0   000010D6 303          ED    PRT3,DECNUM
000003E8  D202 8E44 8ECD       00001044   000010CD 304          MVC   PRTM3(3),PRT3+13     fill in message with M3 field
                                                    305
000003EE  B982 0022                                 306          XGR   R2,R2                get M5 as U8
000003F2  4320 5008                        00000008 307          IC    R2,M5
000003F6  4E20 8ED6                        000010D6 308          CVD   R2,DECNUM            and convert
000003FA  D211 8EC0 8EAA       000010C0   000010AA 309          MVC   PRT3,EDIT
00000400  DE11 8EC0 8ED6       000010C0   000010D6 310          ED    PRT3,DECNUM
00000406  D202 8E51 8ECD       00001051   000010CD 311          MVC   PRTM5(3),PRT3+13     fill in message with M5 field
                                                    312
0000040C  4100 004D                        0000004D 313          LA    R0,PRTLNG            message length
00000410  4110 8E08                        00001008 314          LA    R1,PRTLINE           messagfe address
00000414  45F0 8236                        00000436 315          BAL   R15,RPTERROR

                                                    317 ************************************************************************
                                                    318 * continue after a failed test
                                                    319 ************************************************************************
                                 00000418  00000001 320 FAILCONT EQU   *
00000418  5800 8374                        00000574 321          L     R0,=F'1'               set failed test indicator
0000041C  5000 8E00                        00001000 322          ST    R0,FAILED
                                                    323
00000420  41C0 C004                        00000004 324          LA    R12,4(0,R12)           next test address
00000424  47F0 80D4                        000002D4 325          B     NEXTE7


                                                    327 ************************************************************************
                                                    328 * end of testing; set ending psw
                                                    329 ************************************************************************
                                 00000428  00000001 330 ENDTEST  EQU   *
00000428  5810 8E00                        00001000 331          L     R1,FAILED              did a test fail?
0000042C  1211                                      332          LTR   R1,R1
0000042E  4780 8338                        00000538 333          BZ    EOJ                    No, exit
00000432  47F0 8350                        00000550 334          B     FAILTEST               Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    336 ************************************************************************
                                                    337 *        RPTERROR          Report instruction test in error
                                                    338 *                             R0 = MESSGAE LENGTH
                                                    339 *                             R1 = ADDRESS OF MESSAGE
                                                    340 ************************************************************************

00000436  50F0 8254                 00000454       342 RPTERROR ST    R15,RPTSAVE          Save return address
0000043A  5050 8258                 00000458       343          ST    R5,RPTSVR5           Save R5
                                                    344 *
                                                    345 *        Use Hercules Diagnose for Message to console
                                                    346 *
0000043E  9002 8260                 00000460       347          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000442  4520 8270                 00000470       348          BAL   R2,MSG               call Hercules console MSG display
00000446  9802 8260                 00000460       349          LM    R0,R2,RPTDWSAV       restore regs

0000044A  5850 8258                 00000458       351          L     R5,RPTSVR5           Restore R5
0000044E  58F0 8254                 00000454       352          L     R15,RPTSAVE          Restore return address
00000452  07FF                                     353          BR    R15                  Return to caller

00000454  00000000                                 355 RPTSAVE  DC    F'0'                 R15 save area
00000458  00000000                                 356 RPTSVR5  DC    F'0'                 R5 save area

00000460  00000000 00000000                        358 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call

                                                    360 ************************************************************************
                                                    361 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    362 *                R2 = return address
                                                    363 ************************************************************************

00000470  4900 8378                 00000578       365 MSG      CH    R0,=H'0'             Do we even HAVE a message?
00000474  07D2                                     366          BNHR  R2                   No, ignore

00000476  9002 82AC                 000004AC       368          STM   R0,R2,MSGSAVE        Save registers

0000047A  4900 837A                 0000057A       370          CH    R0,=AL2(L'MSGMSG)    Message length within limits?
0000047E  47D0 8286                 00000486       371          BNH   MSGOK                Yes, continue
00000482  4100 005F                 0000005F       372          LA    R0,L'MSGMSG          No, set to maximum

00000486  1820                                     374 MSGOK    LR    R2,R0                Copy length to work register
00000488  0620                                     375          BCTR  R2,0                 Minus-1 for execute
0000048A  4420 82B8                 000004B8       376          EX    R2,MSGMVC            Copy message to O/P buffer

0000048E  4120 200A                 0000000A       378          LA    R2,1+L'MSGCMD(,R2)   Calculate true command length
00000492  4110 82BE                 000004BE       379          LA    R1,MSGCMD            Point to true command

00000496  83120008                                 381          DC    X'83',X'12',X'0008'  Issue Hercules Diagnose X'008'
0000049A  4780 82A6                 000004A6       382          BZ    MSGRET               Return if successful
                                                    383
0000049E  1222                                     384          LTR   R2,R2                Is Diag8 Ry (R2) 0?
000004A0  4780 82A6                 000004A6       385          BZ    MSGRET                 an error occurred but coninue
                                                    386
000004A4  0000                                     387          DC    H'0'                 CRASH for debugging purposes

000004A6  9802 82AC                 000004AC       389 MSGRET   LM    R0,R2,MSGSAVE        Restore registers
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000004AA  07F2                                      390          BR    R2                    Return to caller


000004AC  00000000 00000000                         392 MSGSAVE  DC    3F'0'                 Registers save area
000004B8  D200 82C7 1000      000004C7  00000000    393 MSGMVC   MVC   MSGMSG(0),0(R1)       Executed instruction

000004BE  D4E2C7D5 D6C8405C                         395 MSGCMD   DC    C'MSGNOH * '          *** HERCULES MESSAGE COMMAND ***
000004C7  40404040 40404040                         396 MSGMSG   DC    CL95' '               The message text to be displayed
                                                    397
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     399 ********************************************************************************
                                                     400 *        Normal completion or Abnormal termination PSWs
                                                     401 ********************************************************************************

00000528  00020001 80000000                          403 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
00000538  B2B2 8328                    00000528      405 EOJ      LPSWE EOJPSW                   Normal completion

00000540  00020001 80000000                          407 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
00000550  B2B2 8340                    00000540      409 FAILTEST LPSWE FAILPSW                  Abnormal termination

                                                     411 ********************************************************************************
                                                     412 *        Working Storage
                                                     413 ********************************************************************************

00000554  00000000                                   415 CTLR0    DS    F                        CR0
00000558  00000000                                   416          DS    F

00000560                                             418          LTORG ,                        Literals pool
00000560  00000000 00000001                          419                =D'1'
00000568  00000040                                   420                =F'64'
0000056C  00002AB4                                   421                =A(E7TESTS)
00000570  00000003                                   422                =XL4'3'
00000574  00000001                                   423                =F'1'
00000578  0000                                       424                =H'0'
0000057A  005F                                       425                =AL2(L'MSGMSG)
                                                     426
                                                     427 *        some constants
                                                     428
                          00000400  00000001        429 K        EQU   1024                     One KB
                          00001000  00000001        430 PAGE     EQU   (4*K)                    Size of one page
                          00010000  00000001        431 K64      EQU   (64*K)                   64 KB
                          00100000  00000001        432 MB       EQU   (K*K)                     1 MB
                                                     433
                          AABBCCDD  00000001        434 REG2PATT EQU   X'AABBCCDD'              Polluted Register pattern
                          000000DD  00000001        435 REG2LOW  EQU         X'DD'             (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    437 *=========================================================================
                                                    438 *
                                                    439 *  NOTE: start data on an address that is easy to display
                                                    440 *        within Hercules
                                                    441 *
                                                    442 *=========================================================================
                                                    443
0000057C                      0000057C  00001000    444          ORG   ZVE7TST+X'1000'
00001000  00000000                                  445 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                  446 TESTING  DC    F'0'                    current test number

                                                    448 ************************************************************************
                                                    449 *        TEST failed : result messgae
                                                    450 ************************************************************************
                                                    451 *
                                                    452 *        failed message and associated editting
                                                    453 *
00001008  40404040 40404040                         454 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                    455 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                         456          DC    C' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                         457 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 8840D4F3                         458          DC    C' with M3='
00001044  A7A7A7                                    459 PRTM3    DC    C'xxx'
00001047  6B                                        460          DC    C','
00001048  40A689A3 8840D4F5                         461          DC    C' with M5='
00001051  A7A7A7                                    462 PRTM5    DC    C'xxx'
00001054  4B                                        463          DC    C'.'
                              0000004D  00000001    464 PRTLNG   EQU   *-PRTLINE
                                                    465
                                                    466 ************************************************************************
                                                    467 *        TEST failed : CC message
                                                    468 ************************************************************************
                                                    469 *
                                                    470 *        failed message and associated editting
                                                    471 *
00001055  40404040 40404040                         472 CCPRTLINE DC   C'         Test # '
00001065  A7A7A7                                    473 CCPRTNUM DC    C'xxx'
00001068  40A69996 95874083                         474          DC    c' wrong cc for instruction '
00001082  A7A7A7A7 A7A7A7A7                         475 CCPRTNAME DC    CL8'xxxxxxxx'
0000108A  4085A797 8583A385                         476          DC    C' expected: cc='
00001098  A7                                        477 CCPRTEXP DC    C'x'
00001099  6B                                        478          DC    C','
0000109A  40998583 8589A585                         479          DC    C' received: cc='
000010A8  A7                                        480 CCPRTGOT DC    C'x'
000010A9  4B                                        481          DC    C'.'
                              00000055  00000001    482 CCPRTLNG   EQU   *-CCPRTLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    484 ************************************************************************
                                                    485 *        TEST failed : message working storge
                                                    486 ************************************************************************
000010AA  40212020 20202020                         487 EDIT     DC    XL18'40212020202020202020202020202020'
                                                    488
000010BC  7E7E7E6E                                  489          DC    C'===>'
000010C0  40404040 40404040                         490 PRT3     DC    CL18' '
000010D2  4C7E7E7E                                  491          DC    C'<==='
000010D6  00000000 00000000                         492 DECNUM   DS    CL16


                                                    494 ************************************************************************
                                                    495 *        Vector instruction results, pollution and input
                                                    496 ************************************************************************
000010E8                                            497          DS    0F
000010E8  00000000 00000000                         498          DS    XL16                                    gap
000010F8  FFFFFFFF FFFFFFFF                         499 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
00001108  00000000 00000000                         500          DS    XL16


                                                    502 ************************************************************************
                                                    503 *        E7TEST DSECT
                                                    504 ************************************************************************


                                                    506 E7TEST   DSECT ,
00000000  00000000                                  507 TSUB     DC    A(0)                      pointer  to test
00000004  0000                                      508 TNUM     DC    H'00'                     Test Number
00000006  00                                        509          DC    X'00'
00000007  00                                        510 M3       DC    HL1'00'                   M3 used
00000008  00                                        511 M5       DC    HL1'00'                   M5 used
00000009  00                                        512 CC       DC    HL1'00'                   cc expected
0000000A  00                                        513 CCMASK   DC    HL1'00'                   not expected CC mask
                                                    514 *
                                                    515 *        CC extrtaction
                                                    516 *
0000000C  00000000 00000000                         517 CCPSW    DS    2F                        extract PSW after test (has CC)
00000014  00                                        518 CCFOUND  DS    X                         extracted cc
                                                    519
00000015  40404040 40404040                         520 OPNAME   DC    CL8' '                    E7 name
00000020  00000000                                  521 V1ADDR   DC    A(0)                      address of v1 result
00000024  00000000                                  522 V2ADDR   DC    A(0)                      address of v2 source
00000028  00000000                                  523 V3ADDR   DC    A(0)                      address of v3 source
0000002C  00000000                                  524 RELEN    DC    A(0)                      RESULT LENGTH
00000030  00000000                                  525 READDR   DC    A(0)                      result (expected) address
00000038  00000000 00000000                         526          DS    FD                           gap
00000040  00000000 00000000                         527 V1OUTPUT DS    XL16                      V1 Output
00000050  00000000 00000000                         528          DS    FD                           gap
                                                    529
                                                    530 *        test routine will be here (from VRR-a macro)
                                                    531 *
                                                    532 *        followed by
                                                    533 *              EXPECTED RESULT
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                              00000000  00002B5F    535 ZVE7TST  CSECT ,
00001118                                            536          DS    0F


                                                    538 ************************************************************************
                                                    539 *     Macros to help build test tables
                                                    540 ************************************************************************


                                                    542 *
                                                    543 * macro to generate individual test
                                                    544 *
                                                    545          MACRO
                                                    546          VRR_A &INST,&M3,&M5,&CC
                                                    547 .*                                 &INST   - VRR-a instruction under test
                                                    548 .*                                 &M3     - M3 field - element size
                                                    549 .*                                 &M5     - M5 field - CS
                                                    550 .*                                 &CC     - expected CC
                                                    551
                                                    552          LCLA  &XCC(4)  &XCC has mask values for FAILED condition codes
                                                    553 &XCC(1)  SETA  7                  CC != 0
                                                    554 &XCC(2)  SETA  11                 CC != 1
                                                    555 &XCC(3)  SETA  13                 CC != 2
                                                    556 &XCC(4)  SETA  14                 CC != 3
                                                    557
                                                    558          GBLA  &TNUM
                                                    559 &TNUM    SETA  &TNUM+1
                                                    560
                                                    561          DS    0FD
                                                    562          USING *,R5               base for test data and test routine
                                                    563
                                                    564 T&TNUM   DC    A(X&TNUM)          address of test routine
                                                    565          DC    H'&TNUM'           test number
                                                    566          DC    X'00'
                                                    567          DC    HL1'&M3'                M3 used
                                                    568          DC    HL1'&M5'                M5 used
                                                    569          DC    HL1'&CC'           CC
                                                    570          DC    HL1'&XCC(&CC+1)'   CC failed mask
                                                    571
                                                    572          DS    2F                 extracted PSW after test (has CC)
                                                    573          DC    X'FF'              extracted CC, if test failed
                                                    574
                                                    575          DC    CL8'&INST'         instruction name
                                                    576          DC    A(RE&TNUM)         address of v1 result
                                                    577          DC    A(RE&TNUM+16)      address of v2 source
                                                    578          DC    A(RE&TNUM+32)      address of v3 source
                                                    579          DC    A(16)              result length
                                                    580 REA&TNUM DC    A(RE&TNUM)         result address
                                                    581          DS    FD                 gap
                                                    582 V1O&TNUM DS    XL16               V1 output
                                                    583          DS    FD                 gap
                                                    584 .*
                                                    585 *
                                                    586 X&TNUM   DS    0F
                                                    587          LA   R1,V1FUDGE         load v21 fudge
                                                    588          VL    v21,0(R1)
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      589
                                                      590          LGF   R1,V2ADDR          load v2 source
                                                      591          VL    v22,0(R1)          use v21 to test decoder
                                                      592
                                                      593          &INST V21,V22,&M3,&M5           test instruction
                                                      594
                                                      595          EPSW  R2,R0              extract psw
                                                      596          ST    R2,CCPSW              to save CC
                                                      597
                                                      598          VST   V21,V1O&TNUM       save v1 output
                                                      599
                                                      600          BR    R11                return
                                                      601
                                                      602 RE&TNUM  DC    0F                 V1 for this test
                                                      603
                                                      604          DROP  R5
                                                      605          MEND
                                                      607 *
                                                      608 * macro to generate table of pointers to individual tests
                                                      609 *
                                                      610          MACRO
                                                      611          PTTABLE
                                                      612          GBLA  &TNUM
                                                      613          LCLA  &CUR
                                                      614 &CUR     SETA  1
                                                      615 .*
                                                      616 TTABLE   DS    0F
                                                      617 .LOOP    ANOP
                                                      618 .*
                                                      619          DC    A(T&CUR)                 test address
                                                      620 .*
                                                      621 &CUR     SETA  &CUR+1
                                                      622          AIF   (&CUR LE &TNUM).LOOP
                                                      623 *
                                                      624          DC    A(0)                     end of table
                                                      625          DC    A(0)                     end of table
                                                      626 .*
                                                      627          MEND
                                                      628
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      630 ************************************************************************
                                                      631 *        E7 VRR-a tests
                                                      632 ************************************************************************
                                                      633          PRINT DATA
                                                      634 *
                                                      635 *
                                                      636 *   E75C VISTR  - Vector Isolate String
                                                      637 *
                                                      638 *        VRR-a instruction,
                                                      639 *              M3,                    element size
                                                      640 *              M5,                    CS
                                                      641 *              CC                     expected condition code
                                                      642 *
                                                      643 *              followed by
                                                      644 *                 16 byte V1 result
                                                      645 *                 16 byte V2 source
                                                      646
                                                      647 *-----------------------------------------------------------------
                                                      648 * VISTR  - Vector Isolate String
                                                      649 *-----------------------------------------------------------------
                                                      650
                                                      651 *-----------------------------------------------------------------
                                                      652 * case 0 -  simple debug                                  CS=1
                                                      653 *-----------------------------------------------------------------
                                                      654 *byte
                                                      655          VRR_A VISTR,0,1,0
00001118                                              656+         DS    0FD
00001118                          00001118            657+         USING *,R5             base for test data and test routine
00001118  00001170                                    658+T1       DC    A(X1)            address of test routine
0000111C  0001                                        659+         DC    H'1'             test number
0000111E  00                                          660+         DC    X'00'
0000111F  00                                          661+         DC    HL1'0'                M3 used
00001120  01                                          662+         DC    HL1'1'                M5 used
00001121  00                                          663+         DC    HL1'0'           CC
00001122  07                                          664+         DC    HL1'7'           CC failed mask
00001124  00000000 00000000                           665+         DS    2F               extracted PSW after test (has CC)
0000112C  FF                                          666+         DC    X'FF'            extracted CC, if test failed
0000112D  E5C9E2E3 D9404040                           667+         DC    CL8'VISTR'       instruction name
00001138  0000119C                                    668+         DC    A(RE1)           address of v1 result
0000113C  000011AC                                    669+         DC    A(RE1+16)        address of v2 source
00001140  000011BC                                    670+         DC    A(RE1+32)        address of v3 source
00001144  00000010                                    671+         DC    A(16)            result length
00001148  0000119C                                    672+REA1     DC    A(RE1)           result address
00001150  00000000 00000000                           673+         DS    FD               gap
00001158  00000000 00000000                           674+V1O1     DS    XL16             V1 output
00001160  00000000 00000000
00001168  00000000 00000000                           675+         DS    FD               gap
                                                      676+*
00001170                                              677+X1       DS    0F
00001170  4110 8EF8                     000010F8      678+         LA    R1,V1FUDGE      load v21 fudge
00001174  E751 0000 0806                00000000      679+         VL    v21,0(R1)
0000117A  E310 5024 0014                00000024      680+         LGF   R1,V2ADDR        load v2 source
00001180  E761 0000 0806                00000000      681+         VL    v22,0(R1)        use v21 to test decoder
00001186  E756 0010 0C5C                              682+         VISTR V21,V22,0,1              test instruction
0000118C  B98D 0020                                   683+         EPSW  R2,R0            extract psw
00001190  5020 500C                     0000000C      684+         ST    R2,CCPSW            to save CC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001194  E750 5040 080E                 00001158   685+         VST   V21,V1O1           save v1 output
0000119A  07FB                                      686+         BR    R11               return
0000119C                                            687+RE1      DC    0F                V1 for this test
0000119C                                            688+         DROP  R5
0000119C  00000000 00000000                         689          DC    XL16'00000000 00000000 00000000 00000000'   V1
000011A4  00000000 00000000
000011AC  00000000 00000000                         690          DC    XL16'00000000 00000000 00000000 00000000'   v2
000011B4  00000000 00000000
                                                    691
                                                    692          VRR_A VISTR,0,1,0
000011C0                                            693+         DS    0FD
000011C0                    000011C0                694+         USING *,R5              base for test data and test routine
000011C0  00001218                                  695+T2       DC    A(X2)             address of test routine
000011C4  0002                                      696+         DC    H'2'              test number
000011C6  00                                        697+         DC    X'00'
000011C7  00                                        698+         DC    HL1'0'                 M3 used
000011C8  01                                        699+         DC    HL1'1'                 M5 used
000011C9  00                                        700+         DC    HL1'0'            CC
000011CA  07                                        701+         DC    HL1'7'            CC failed mask
000011CC  00000000 00000000                         702+         DS    2F                extracted PSW after test (has CC)
000011D4  FF                                        703+         DC    X'FF'             extracted CC, if test failed
000011D5  E5C9E2E3 D9404040                         704+         DC    CL8'VISTR'        instruction name
000011E0  00001244                                  705+         DC    A(RE2)            address of v1 result
000011E4  00001254                                  706+         DC    A(RE2+16)         address of v2 source
000011E8  00001264                                  707+         DC    A(RE2+32)         address of v3 source
000011EC  00000010                                  708+         DC    A(16)             result length
000011F0  00001244                                  709+REA2     DC    A(RE2)            result address
000011F8  00000000 00000000                         710+         DS    FD                gap
00001200  00000000 00000000                         711+V1O2     DS    XL16              V1 output
00001208  00000000 00000000
00001210  00000000 00000000                         712+         DS    FD                gap
                                                    713+*
00001218                                            714+X2       DS    0F
00001218  4110 8EF8                      000010F8   715+         LA    R1,V1FUDGE       load v21 fudge
0000121C  E751 0000 0806                 00000000   716+         VL    v21,0(R1)
00001222  E310 5024 0014                 00000024   717+         LGF   R1,V2ADDR         load v2 source
00001228  E761 0000 0806                 00000000   718+         VL    v22,0(R1)         use v21 to test decoder
0000122E  E756 0010 0C5C                            719+         VISTR V21,V22,0,1               test instruction
00001234  B98D 0020                                 720+         EPSW  R2,R0             extract psw
00001238  5020 500C                      0000000C   721+         ST    R2,CCPSW             to save CC
0000123C  E750 9000 080E                 00001200   722+         VST   V21,V1O2          save v1 output
00001242  07FB                                      723+         BR    R11               return
00001244                                            724+RE2      DC    0F                V1 for this test
00001244                                            725+         DROP  R5
00001244  01020304 00000000                         726          DC    XL16'01020304 00000000 00000000 00000000'   V1
0000124C  00000000 00000000
00001254  01020304 00000000                         727          DC    XL16'01020304 00000000 0FFFFFFF FFFFFFFF'   v2
0000125C  0FFFFFFF FFFFFFFF
                                                    728
                                                    729          VRR_A VISTR,0,1,3
00001268                                            730+         DS    0FD
00001268                    00001268                731+         USING *,R5              base for test data and test routine
00001268  000012C0                                  732+T3       DC    A(X3)             address of test routine
0000126C  0003                                      733+         DC    H'3'              test number
0000126E  00                                        734+         DC    X'00'
0000126F  00                                        735+         DC    HL1'0'                 M3 used
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001270  01                                      736+         DC    HL1'1'                  M5 used
00001271  03                                      737+         DC    HL1'3'                CC
00001272  0E                                      738+         DC    HL1'14'               CC failed mask
00001274  00000000 00000000                       739+         DS    2F                    extracted PSW after test (has CC)
0000127C  FF                                      740+         DC    X'FF'                 extracted CC, if test failed
0000127D  E5C9E2E3 D9404040                       741+         DC    CL8'VISTR'            instruction name
00001288  000012EC                                742+         DC    A(RE3)                address of v1 result
0000128C  000012FC                                743+         DC    A(RE3+16)             address of v2 source
00001290  0000130C                                744+         DC    A(RE3+32)             address of v3 source
00001294  00000010                                745+         DC    A(16)                 result length
00001298  000012EC                                746+REA3     DC    A(RE3)                result address
000012A0  00000000 00000000                       747+         DS    FD                    gap
000012A8  00000000 00000000                       748+V1O3     DS    XL16                  V1 output
000012B0  00000000 00000000
000012B8  00000000 00000000                       749+         DS    FD                    gap
                                                  750+*
000012C0                                          751+X3       DS    0F
000012C0  4110 8EF8                    000010F8   752+         LA    R1,V1FUDGE          load v21 fudge
000012C4  E751 0000 0806               00000000   753+         VL    v21,0(R1)
000012CA  E310 5024 0014               00000024   754+         LGF   R1,V2ADDR            load v2 source
000012D0  E761 0000 0806               00000000   755+         VL    v22,0(R1)           use v21 to test decoder
000012D6  E756 0010 0C5C                          756+         VISTR V21,V22,0,1                 test instruction
000012DC  B98D 0020                               757+         EPSW  R2,R0               extract psw
000012E0  5020 500C                    0000000C   758+         ST    R2,CCPSW               to save CC
000012E4  E750 5040 080E               000012A8   759+         VST   V21,V1O3            save v1 output
000012EA  07FB                                    760+         BR    R11                 return
000012EC                                          761+RE3      DC    0F                      V1 for this test
000012EC                                          762+         DROP  R5
000012EC  01020304 05060708                       763          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v1
000012F4  090A0B0C 0D0E0F10
000012FC  01020304 05060708                       764          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v2
00001304  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    766 *halfword
                                                    767          VRR_A VISTR,1,1,0
00001310                                            768+         DS    0FD
00001310                      00001310              769+         USING *,R5              base for test data and test routine
00001310  00001368                                  770+T4       DC    A(X4)             address of test routine
00001314  0004                                      771+         DC    H'4'              test number
00001316  00                                        772+         DC    X'00'
00001317  01                                        773+         DC    HL1'1'                 M3 used
00001318  01                                        774+         DC    HL1'1'                 M5 used
00001319  00                                        775+         DC    HL1'0'            CC
0000131A  07                                        776+         DC    HL1'7'            CC failed mask
0000131C  00000000 00000000                         777+         DS    2F                extracted PSW after test (has CC)
00001324  FF                                        778+         DC    X'FF'             extracted CC, if test failed
00001325  E5C9E2E3 D9404040                         779+         DC    CL8'VISTR'        instruction name
00001330  00001394                                  780+         DC    A(RE4)            address of v1 result
00001334  000013A4                                  781+         DC    A(RE4+16)         address of v2 source
00001338  000013B4                                  782+         DC    A(RE4+32)         address of v3 source
0000133C  00000010                                  783+         DC    A(16)             result length
00001340  00001394                                  784+REA4     DC    A(RE4)            result address
00001348  00000000 00000000                         785+         DS    FD                gap
00001350  00000000 00000000                         786+V1O4     DS    XL16              V1 output
00001358  00000000 00000000
00001360  00000000 00000000                         787+         DS    FD                gap
                                                    788+*
00001368                                            789+X4       DS    0F
00001368  4110 8EF8                     000010F8    790+         LA    R1,V1FUDGE        load v21 fudge
0000136C  E751 0000 0806                00000000    791+         VL    v21,0(R1)
00001372  E310 5024 0014                00000024    792+         LGF   R1,V2ADDR         load v2 source
00001378  E761 0000 0806                00000000    793+         VL    v22,0(R1)         use v21 to test decoder
0000137E  E756 0010 1C5C                            794+         VISTR V21,V22,1,1             test instruction
00001384  B98D 0020                                 795+         EPSW  R2,R0             extract psw
00001388  5020 500C                     0000000C    796+         ST    R2,CCPSW             to save CC
0000138C  E750 5040 080E                00001350    797+         VST   V21,V1O4          save v1 output
00001392  07FB                                      798+         BR    R11               return
00001394                                            799+RE4      DC    0F                V1 for this test
00001394                                            800+         DROP  R5
00001394  00000000 00000000                         801          DC    XL16'00000000 00000000 00000000 00000000'   V1
0000139C  00000000 00000000
000013A4  00000000 00000000                         802          DC    XL16'00000000 00000000 00000000 00000000'   v2
000013AC  00000000 00000000
                                                    803
                                                    804          VRR_A VISTR,1,1,0
000013B8                                            805+         DS    0FD
000013B8                      000013B8              806+         USING *,R5              base for test data and test routine
000013B8  00001410                                  807+T5       DC    A(X5)             address of test routine
000013BC  0005                                      808+         DC    H'5'              test number
000013BE  00                                        809+         DC    X'00'
000013BF  01                                        810+         DC    HL1'1'                 M3 used
000013C0  01                                        811+         DC    HL1'1'                 M5 used
000013C1  00                                        812+         DC    HL1'0'            CC
000013C2  07                                        813+         DC    HL1'7'            CC failed mask
000013C4  00000000 00000000                         814+         DS    2F                extracted PSW after test (has CC)
000013CC  FF                                        815+         DC    X'FF'             extracted CC, if test failed
000013CD  E5C9E2E3 D9404040                         816+         DC    CL8'VISTR'        instruction name
000013D8  0000143C                                  817+         DC    A(RE5)            address of v1 result
000013DC  0000144C                                  818+         DC    A(RE5+16)         address of v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000013E0  0000145C                                 819+          DC    A(RE5+32)           address of v3 source
000013E4  00000010                                 820+          DC    A(16)               result length
000013E8  0000143C                                 821+REA5      DC    A(RE5)              result address
000013F0  00000000 00000000                        822+          DS    FD                  gap
000013F8  00000000 00000000                        823+V1O5      DS    XL16                V1 output
00001400  00000000 00000000
00001408  00000000 00000000                        824+          DS    FD                  gap
                                                   825+*
00001410                                           826+X5        DS    0F
00001410  4110 8EF8                      000010F8  827+          LA    R1,V1FUDGE        load v21 fudge
00001414  E751 0000 0806                 00000000  828+          VL    v21,0(R1)
0000141A  E310 5024 0014                 00000024  829+          LGF   R1,V2ADDR          load v2 source
00001420  E761 0000 0806                 00000000  830+          VL    v22,0(R1)          use v21 to test decoder
00001426  E756 0010 1C5C                           831+          VISTR V21,V22,1,1                test instruction
0000142C  B98D 0020                                832+          EPSW  R2,R0              extract psw
00001430  5020 500C                      0000000C  833+          ST    R2,CCPSW              to save CC
00001434  E750 5040 080E                 000013F8  834+          VST   V21,V1O5           save v1 output
0000143A  07FB                                     835+          BR    R11                return
0000143C                                           836+RE5       DC    0F                 V1 for this test
0000143C                                           837+          DROP  R5
0000143C  10203040 00000000                        838           DC    XL16'01020304 00000000 00000000 000000000'  V1
00001444  00000000 00000000
0000144C  10203040 00000000                        839           DC    XL16'01020304 00000000 0FFFFFFF FFFFFFFF'  v2
00001454  FFFFFFFF FFFFFFFF
                                                   840
                                                   841           VRR_A VISTR,1,1,3
00001460                                           842+          DS    0FD
00001460                         00001460          843+          USING *,R5               base for test data and test routine
00001460  000014B8                                 844+T6        DC    A(X6)              address of test routine
00001464  0006                                     845+          DC    H'6'               test number
00001466  00                                       846+          DC    X'00'
00001467  01                                       847+          DC    HL1'1'                  M3 used
00001468  01                                       848+          DC    HL1'1'                  M5 used
00001469  03                                       849+          DC    HL1'3'             CC
0000146A  0E                                       850+          DC    HL1'14'            CC failed mask
0000146C  00000000 00000000                        851+          DS    2F                 extracted PSW after test (has CC)
00001474  FF                                       852+          DC    X'FF'              extracted CC, if test failed
00001475  E5C9E2E3 D9404040                       853+          DC    CL8'VISTR'         instruction name
00001480  000014E4                                 854+          DC    A(RE6)             address of v1 result
00001484  000014F4                                 855+          DC    A(RE6+16)          address of v2 source
00001488  00001504                                 856+          DC    A(RE6+32)          address of v3 source
0000148C  00000010                                 857+          DC    A(16)              result length
00001490  000014E4                                 858+REA6      DC    A(RE6)             result address
00001498  00000000 00000000                        859+          DS    FD                 gap
000014A0  00000000 00000000                        860+V1O6      DS    XL16               V1 output
000014A8  00000000 00000000
000014B0  00000000 00000000                        861+          DS    FD                 gap
                                                   862+*
000014B8                                           863+X6        DS    0F
000014B8  4110 8EF8                      000010F8  864+          LA    R1,V1FUDGE        load v21 fudge
000014BC  E751 0000 0806                 00000000  865+          VL    v21,0(R1)
000014C2  E310 5024 0014                 00000024  866+          LGF   R1,V2ADDR          load v2 source
000014C8  E761 0000 0806                 00000000  867+          VL    v22,0(R1)          use v21 to test decoder
000014CE  E756 0010 1C5C                           868+          VISTR V21,V22,1,1                test instruction
000014D4  B98D 0020                                869+          EPSW  R2,R0              extract psw
000014D8  5020 500C                      0000000C  870+          ST    R2,CCPSW              to save CC
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000014DC  E750 5040 080E                  000014A0   871+         VST   V21,V1O6           save v1 output
000014E2  07FB                                       872+         BR    R11                return
000014E4                                             873+RE6      DC    0F                 V1 for this test
000014E4                                             874+         DROP  R5
000014E4  01020304 05060708                          875          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v1
000014EC  090A0B0C 0D0E0F10
000014F4  01020304 05060708                          876          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v2
000014FC  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    878 *word
                                                    879          VRR_A VISTR,2,1,0
00001508                                            880+         DS    0FD
00001508                      00001508              881+         USING *,R5              base for test data and test routine
00001508  00001560                                  882+T7       DC    A(X7)             address of test routine
0000150C  0007                                      883+         DC    H'7'              test number
0000150E  00                                        884+         DC    X'00'
0000150F  02                                        885+         DC    HL1'2'                 M3 used
00001510  01                                        886+         DC    HL1'1'                 M5 used
00001511  00                                        887+         DC    HL1'0'            CC
00001512  07                                        888+         DC    HL1'7'            CC failed mask
00001514  00000000 00000000                         889+         DS    2F                extracted PSW after test (has CC)
0000151C  FF                                        890+         DC    X'FF'             extracted CC, if test failed
0000151D  E5C9E2E3 D9404040                         891+         DC    CL8'VISTR'        instruction name
00001528  0000158C                                  892+         DC    A(RE7)            address of v1 result
0000152C  0000159C                                  893+         DC    A(RE7+16)         address of v2 source
00001530  000015AC                                  894+         DC    A(RE7+32)         address of v3 source
00001534  00000010                                  895+         DC    A(16)             result length
00001538  0000158C                                  896+REA7     DC    A(RE7)            result address
00001540  00000000 00000000                         897+         DS    FD                gap
00001548  00000000 00000000                         898+V1O7     DS    XL16              V1 output
00001550  00000000 00000000
00001558  00000000 00000000                         899+         DS    FD                gap
                                                    900+*
00001560                                            901+X7       DS    0F
00001560  4110 8EF8                     000010F8    902+         LA    R1,V1FUDGE        load v21 fudge
00001564  E751 0000 0806                00000000    903+         VL    v21,0(R1)
0000156A  E310 5024 0014                00000024    904+         LGF   R1,V2ADDR         load v2 source
00001570  E761 0000 0806                00000000    905+         VL    v22,0(R1)         use v21 to test decoder
00001576  E756 0010 2C5C                            906+         VISTR V21,V22,2,1               test instruction
0000157C  B98D 0020                                 907+         EPSW  R2,R0             extract psw
00001580  5020 500C                     0000000C    908+         ST    R2,CCPSW             to save CC
00001584  E750 5040 080E                00001548    909+         VST   V21,V1O7          save v1 output
0000158A  07FB                                      910+         BR    R11               return
0000158C                                            911+RE7      DC    0F                V1 for this test
0000158C                                            912+         DROP  R5
0000158C  00000000 00000000                         913          DC    XL16'00000000 00000000 00000000 00000000'   V1
00001594  00000000 00000000
0000159C  00000000 00000000                         914          DC    XL16'00000000 00000000 00000000 00000000'   v2
000015A4  00000000 00000000
                                                    915
                                                    916          VRR_A VISTR,2,1,0
000015B0                                            917+         DS    0FD
000015B0                      000015B0              918+         USING *,R5              base for test data and test routine
000015B0  00001608                                  919+T8       DC    A(X8)             address of test routine
000015B4  0008                                      920+         DC    H'8'              test number
000015B6  00                                        921+         DC    X'00'
000015B7  02                                        922+         DC    HL1'2'                 M3 used
000015B8  01                                        923+         DC    HL1'1'                 M5 used
000015B9  00                                        924+         DC    HL1'0'            CC
000015BA  07                                        925+         DC    HL1'7'            CC failed mask
000015BC  00000000 00000000                         926+         DS    2F                extracted PSW after test (has CC)
000015C4  FF                                        927+         DC    X'FF'             extracted CC, if test failed
000015C5  E5C9E2E3 D9404040                         928+         DC    CL8'VISTR'        instruction name
000015D0  00001634                                  929+         DC    A(RE8)            address of v1 result
000015D4  00001644                                  930+         DC    A(RE8+16)         address of v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000015D8  00001654                                 931+          DC    A(RE8+32)           address of v3 source
000015DC  00000010                                 932+          DC    A(16)               result length
000015E0  00001634                                 933+REA8      DC    A(RE8)              result address
000015E8  00000000 00000000                        934+          DS    FD                  gap
000015F0  00000000 00000000                        935+V1O8      DS    XL16                V1 output
000015F8  00000000 00000000
00001600  00000000 00000000                        936+          DS    FD                  gap
                                                   937+*
00001608                                           938+X8        DS    0F
00001608  4110 8EF8                      000010F8  939+          LA    R1,V1FUDGE        load v21 fudge
0000160C  E751 0000 0806                 00000000  940+          VL    v21,0(R1)
00001612  E310 5024 0014                 00000024  941+          LGF   R1,V2ADDR          load v2 source
00001618  E761 0000 0806                 00000000  942+          VL    v22,0(R1)          use v21 to test decoder
0000161E  E756 0010 2C5C                           943+          VISTR V21,V22,2,1                test instruction
00001624  B98D 0020                                944+          EPSW  R2,R0              extract psw
00001628  5020 500C                      0000000C  945+          ST    R2,CCPSW              to save CC
0000162C  E750 5040 080E                 000015F0  946+          VST   V21,V1O8           save v1 output
00001632  07FB                                     947+          BR    R11                return
00001634                                           948+RE8       DC    0F                 V1 for this test
00001634                                           949+          DROP  R5
00001634  10203040 00000000                        950           DC    XL16'01020304 00000000 00000000 000000000'  V1
0000163C  00000000 00000000
00001644  10203040 00000000                        951           DC    XL16'01020304 00000000 0FFFFFFF FFFFFFFF'  v2
0000164C  FFFFFFFF FFFFFFFF
                                                   952
                                                   953           VRR_A VISTR,2,1,3
00001658                                           954+          DS    0FD
00001658                         00001658          955+          USING *,R5               base for test data and test routine
00001658  000016B0                                 956+T9        DC    A(X9)              address of test routine
0000165C  0009                                     957+          DC    H'9'               test number
0000165E  00                                       958+          DC    X'00'
0000165F  02                                       959+          DC    HL1'2'                  M3 used
00001660  01                                       960+          DC    HL1'1'                  M5 used
00001661  03                                       961+          DC    HL1'3'             CC
00001662  0E                                       962+          DC    HL1'14'            CC failed mask
00001664  00000000 00000000                        963+          DS    2F                 extracted PSW after test (has CC)
0000166C  FF                                       964+          DC    X'FF'              extracted CC, if test failed
0000166D  E5C9E2E3 D9404040                        965+          DC    CL8'VISTR'         instruction name
00001678  000016DC                                 966+          DC    A(RE9)             address of v1 result
0000167C  000016EC                                 967+          DC    A(RE9+16)          address of v2 source
00001680  000016FC                                 968+          DC    A(RE9+32)          address of v3 source
00001684  00000010                                 969+          DC    A(16)              result length
00001688  000016DC                                 970+REA9      DC    A(RE9)             result address
00001690  00000000 00000000                        971+          DS    FD                 gap
00001698  00000000 00000000                        972+V1O9      DS    XL16               V1 output
000016A0  00000000 00000000
000016A8  00000000 00000000                        973+          DS    FD                 gap
                                                   974+*
000016B0                                           975+X9        DS    0F
000016B0  4110 8EF8                      000010F8  976+          LA    R1,V1FUDGE        load v21 fudge
000016B4  E751 0000 0806                 00000000  977+          VL    v21,0(R1)
000016BA  E310 5024 0014                 00000024  978+          LGF   R1,V2ADDR          load v2 source
000016C0  E761 0000 0806                 00000000  979+          VL    v22,0(R1)          use v21 to test decoder
000016C6  E756 0010 2C5C                           980+          VISTR V21,V22,2,1                test instruction
000016CC  B98D 0020                                981+          EPSW  R2,R0              extract psw
000016D0  5020 500C                      0000000C  982+          ST    R2,CCPSW              to save CC
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000016D4  E750 5040 080E                  00001698   983+         VST   V21,V1O9           save v1 output
000016DA  07FB                                       984+         BR    R11                return
000016DC                                             985+RE9      DC    0F                 V1 for this test
000016DC                                             986+         DROP  R5
000016DC  01020304 05060708                          987          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v1
000016E4  090A0B0C 0D0E0F10
000016EC  01020304 05060708                          988          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v2
000016F4  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    990 *-------------------------------------------------------------------
                                                    991 * case 1 -  more options                                    CS=1
                                                    992 *-------------------------------------------------------------------
                                                    993 *byte
                                                    994          VRR_A VISTR,0,1,3
00001700                                            995+         DS    0FD
00001700                      00001700              996+         USING *,R5              base for test data and test routine
00001700  00001758                                  997+T10      DC    A(X10)            address of test routine
00001704  000A                                      998+         DC    H'10'             test number
00001706  00                                        999+         DC    X'00'
00001707  00                                       1000+         DC    HL1'0'                 M3 used
00001708  01                                       1001+         DC    HL1'1'                 M5 used
00001709  03                                       1002+         DC    HL1'3'            CC
0000170A  0E                                       1003+         DC    HL1'14'           CC failed mask
0000170C  00000000 00000000                        1004+         DS    2F                extracted PSW after test (has CC)
00001714  FF                                       1005+         DC    X'FF'             extracted CC, if test failed
00001715  E5C9E2E3 D9404040                        1006+         DC    CL8'VISTR'        instruction name
00001720  00001784                                 1007+         DC    A(RE10)           address of v1 result
00001724  00001794                                 1008+         DC    A(RE10+16)        address of v2 source
00001728  000017A4                                 1009+         DC    A(RE10+32)        address of v3 source
0000172C  00000010                                 1010+         DC    A(16)             result length
00001730  00001784                                 1011+REA10    DC    A(RE10)           result address
00001738  00000000 00000000                        1012+         DS    FD                gap
00001740  00000000 00000000                        1013+V1O10    DS    XL16              V1 output
00001748  00000000 00000000
00001750  00000000 00000000                        1014+         DS    FD                gap
                                                   1015+*
00001758                                           1016+X10      DS    0F
00001758  4110 8EF8                      000010F8  1017+         LA    R1,V1FUDGE      load v21 fudge
0000175C  E751 0000 0806                 00000000  1018+         VL    v21,0(R1)
00001762  E310 5024 0014                 00000024  1019+         LGF   R1,V2ADDR        load v2 source
00001768  E761 0000 0806                 00000000  1020+         VL    v22,0(R1)         use v21 to test decoder
0000176E  E756 0010 0C5C                           1021+         VISTR V21,V22,0,1               test instruction
00001774  B98D 0020                                1022+         EPSW  R2,R0             extract psw
00001778  5020 500C                      0000000C  1023+         ST    R2,CCPSW             to save CC
0000177C  E750 5040 080E                 00001740  1024+         VST   V21,V1O10         save v1 output
00001782  07FB                                     1025+         BR    R11               return
00001784                                           1026+RE10     DC    0F                V1 for this test
00001784                                           1027+         DROP  R5
00001784  01020304 05060708                        1028          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v1
0000178C  090A0B0C 0D0E0F10
00001794  01020304 05060708                        1029          DC    XL16'01020304 05060708 090A0B0C 0D0E0F10'   v2
0000179C  090A0B0C 0D0E0F10
                                                   1030
                                                   1031          VRR_A VISTR,0,1,0
000017A8                                           1032+         DS    0FD
000017A8                      000017A8             1033+         USING *,R5              base for test data and test routine
000017A8  00001800                                 1034+T11      DC    A(X11)            address of test routine
000017AC  000B                                     1035+         DC    H'11'             test number
000017AE  00                                       1036+         DC    X'00'
000017AF  00                                       1037+         DC    HL1'0'                 M3 used
000017B0  01                                       1038+         DC    HL1'1'                 M5 used
000017B1  00                                       1039+         DC    HL1'0'            CC
000017B2  07                                       1040+         DC    HL1'7'            CC failed mask
000017B4  00000000 00000000                        1041+         DS    2F                extracted PSW after test (has CC)
000017BC  FF                                       1042+         DC    X'FF'             extracted CC, if test failed
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000017BD  E5C9E2E3 D9404040                        1043+          DC    CL8'VISTR'          instruction name
000017C8  0000182C                                 1044+          DC    A(RE11)             address of v1 result
000017CC  0000183C                                 1045+          DC    A(RE11+16)          address of v2 source
000017D0  0000184C                                 1046+          DC    A(RE11+32)          address of v3 source
000017D4  00000010                                 1047+          DC    A(16)               result length
000017D8  0000182C                                 1048+REA11     DC    A(RE11)             result address
000017E0  00000000 00000000                        1049+          DS    FD                  gap
000017E8  00000000 00000000                        1050+V1O11     DS    XL16                V1 output
000017F0  00000000 00000000
000017F8  00000000 00000000                        1051+          DS    FD                  gap
                                                   1052+*
00001800                                           1053+X11       DS    0F
00001800  4110 8EF8                      000010F8  1054+          LA    R1,V1FUDGE         load v21 fudge
00001804  E751 0000 0806                 00000000  1055+          VL    v21,0(R1)
0000180A  E310 5024 0014                 00000024  1056+          LGF   R1,V2ADDR           load v2 source
00001810  E761 0000 0806                 00000000  1057+          VL    v22,0(R1)           use v21 to test decoder
00001816  E756 0010 0C5C                           1058+          VISTR V21,V22,0,1                 test instruction
0000181C  B98D 0020                                1059+          EPSW  R2,R0               extract psw
00001820  5020 500C                      0000000C  1060+          ST    R2,CCPSW               to save CC
00001824  E750 5040 080E                 000017E8  1061+          VST   V21,V1O11           save v1 output
0000182A  07FB                                     1062+          BR    R11                 return
0000182C                                           1063+RE11      DC    0F                  V1 for this test
0000182C                                           1064+          DROP  R5
0000182C  01020304 05060708                        1065           DC    XL16'01020304 05060708 090A0B0C 0D0E0F00'   v1
00001834  090A0B0C 0D0E0F00
0000183C  01020304 05060708                        1066           DC    XL16'01020304 05060708 090A0B0C 0D0E0F00'   v2
00001844  090A0B0C 0D0E0F00
                                                   1067
                                                   1068           VRR_A VISTR,0,1,0
00001850                                           1069+          DS    0FD
00001850                       00001850            1070+          USING *,R5                base for test data and test routine
00001850  000018A8                                 1071+T12       DC    A(X12)              address of test routine
00001854  000C                                     1072+          DC    H'12'               test number
00001856  00                                       1073+          DC    X'00'
00001857  00                                       1074+          DC    HL1'0'                    M3 used
00001858  01                                       1075+          DC    HL1'1'                    M5 used
00001859  00                                       1076+          DC    HL1'0'              CC
0000185A  07                                       1077+          DC    HL1'7'              CC failed mask
0000185C  00000000 00000000                        1078+          DS    2F                  extracted PSW after test (has CC)
00001864  FF                                       1079+          DC    X'FF'               extracted CC, if test failed
00001865  E5C9E2E3 D9404040                        1080+          DC    CL8'VISTR'          instruction name
00001870  000018D4                                 1081+          DC    A(RE12)             address of v1 result
00001874  000018E4                                 1082+          DC    A(RE12+16)          address of v2 source
00001878  000018F4                                 1083+          DC    A(RE12+32)          address of v3 source
0000187C  00000010                                 1084+          DC    A(16)               result length
00001880  000018D4                                 1085+REA12     DC    A(RE12)             result address
00001888  00000000 00000000                        1086+          DS    FD                  gap
00001890  00000000 00000000                        1087+V1O12     DS    XL16                V1 output
00001898  00000000 00000000
000018A0  00000000 00000000                        1088+          DS    FD                  gap
                                                   1089+*
000018A8                                           1090+X12       DS    0F
000018A8  4110 8EF8                      000010F8  1091+          LA    R1,V1FUDGE         load v21 fudge
000018AC  E751 0000 0806                 00000000  1092+          VL    v21,0(R1)
000018B2  E310 5024 0014                 00000024  1093+          LGF   R1,V2ADDR           load v2 source
000018B8  E761 0000 0806                 00000000  1094+          VL    v22,0(R1)           use v21 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000018BE  E756 0010 0C5C                         1095+         VISTR V21,V22,0,1               test instruction
000018C4  B98D 0020                              1096+         EPSW  R2,R0               extract psw
000018C8  5020 500C                 0000000C     1097+         ST    R2,CCPSW               to save CC
000018CC  E750 5040 080E            00001890     1098+         VST   V21,V1O12           save v1 output
000018D2  07FB                                   1099+         BR    R11                 return
000018D4                                         1100+RE12     DC    0F                  V1 for this test
000018D4                                         1101+         DROP  R5
000018D4  01020304 05060708                      1102          DC    XL16'01020304 05060708 090A0B0C 0D000000'   v1
000018DC  090A0B0C 0D000000
000018E4  01020304 05060708                      1103          DC    XL16'01020304 05060708 090A0B0C 0D000F10'   v2
000018EC  090A0B0C 0D000F10
                                                 1104
                                                 1105          VRR_A VISTR,0,1,0
000018F8                                         1106+         DS    0FD
000018F8                    000018F8             1107+         USING *,R5                base base for test data and test routine
000018F8  00001950                               1108+T13      DC    A(X13)              address of test routine
000018FC  000D                                   1109+         DC    H'13'               test number
000018FE  00                                     1110+         DC    X'00'
000018FF  00                                     1111+         DC    HL1'0'                   M3 used
00001900  01                                     1112+         DC    HL1'1'                   M5 used
00001901  00                                     1113+         DC    HL1'0'              CC
00001902  07                                     1114+         DC    HL1'7'              CC failed mask
00001904  00000000 00000000                      1115+         DS    2F                  extracted PSW after test (has CC)
0000190C  FF                                     1116+         DC    X'FF'               extracted CC, if test failed
0000190D  E5C9E2E3 D9404040                      1117+         DC    CL8'VISTR'          instruction name
00001918  0000197C                               1118+         DC    A(RE13)             address of v1 result
0000191C  0000198C                               1119+         DC    A(RE13+16)          address of v2 source
00001920  0000199C                               1120+         DC    A(RE13+32)          address of v3 source
00001924  00000010                               1121+         DC    A(16)               result length
00001928  0000197C                               1122+REA13    DC    A(RE13)             result address
00001930  00000000 00000000                      1123+         DS    FD                  gap
00001938  00000000 00000000                      1124+V1O13    DS    XL16                V1 output
00001940  00000000 00000000
00001948  00000000 00000000                      1125+         DS    FD                  gap
                                                 1126+*
00001950                                         1127+X13      DS    0F
00001950  4110 8EF8                 000010F8     1128+         LA    R1,V1FUDGE         load v21 fudge
00001954  E751 0000 0806            00000000     1129+         VL    v21,0(R1)
0000195A  E310 5024 0014            00000024     1130+         LGF   R1,V2ADDR           load v2 source
00001960  E761 0000 0806            00000000     1131+         VL    v22,0(R1)           use v21 to test decoder
00001966  E756 0010 0C5C                         1132+         VISTR V21,V22,0,1               test instruction
0000196C  B98D 0020                              1133+         EPSW  R2,R0               extract psw
00001970  5020 500C                 0000000C     1134+         ST    R2,CCPSW               to save CC
00001974  E750 5040 080E            00001938     1135+         VST   V21,V1O13           save v1 output
0000197A  07FB                                   1136+         BR    R11                 return
0000197C                                         1137+RE13     DC    0F                  V1 for this test
0000197C                                         1138+         DROP  R5
0000197C  01020304 05060708                      1139          DC    XL16'01020304 05060708 090A0B0C 00000000'   v1
00001984  090A0B0C 00000000
0000198C  01020304 05060708                      1140          DC    XL16'01020304 05060708 090A0B0C 000E0F10'   v2
00001994  090A0B0C 000E0F10
                                                 1141
                                                 1142          VRR_A VISTR,0,1,0
000019A0                                         1143+         DS    0FD
000019A0                    000019A0             1144+         USING *,R5                base base for test data and test routine
000019A0  000019F8                               1145+T14      DC    A(X14)              address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000019A4  000E                                     1146+          DC    H'14'              test number
000019A6  00                                       1147+          DC    X'00'
000019A7  00                                       1148+          DC    HL1'0'                  M3 used
000019A8  01                                       1149+          DC    HL1'1'                  M5 used
000019A9  00                                       1150+          DC    HL1'0'             CC
000019AA  07                                       1151+          DC    HL1'7'             CC failed mask
000019AC  00000000 00000000                        1152+          DS    2F                 extracted PSW after test (has CC)
000019B4  FF                                       1153+          DC    X'FF'              extracted CC, if test failed
000019B5  E5C9E2E3 D9404040                        1154+          DC    CL8'VISTR'         instruction name
000019C0  00001A24                                 1155+          DC    A(RE14)            address of v1 result
000019C4  00001A34                                 1156+          DC    A(RE14+16)         address of v2 source
000019C8  00001A44                                 1157+          DC    A(RE14+32)         address of v3 source
000019CC  00000010                                 1158+          DC    A(16)              result length
000019D0  00001A24                                 1159+REA14     DC    A(RE14)            result address
000019D8  00000000 00000000                        1160+          DS    FD                 gap
000019E0  00000000 00000000                        1161+V1O14     DS    XL16               V1 output
000019E8  00000000 00000000
000019F0  00000000 00000000                        1162+          DS    FD                 gap
                                                   1163+*
000019F8                                           1164+X14       DS    0F
000019F8  4110 8EF8                      000010F8  1165+          LA    R1,V1FUDGE        load v21 fudge
000019FC  E751 0000 0806                 00000000  1166+          VL    v21,0(R1)
00001A02  E310 5024 0014                 00000024  1167+          LGF   R1,V2ADDR          load v2 source
00001A08  E761 0000 0806                 00000000  1168+          VL    v22,0(R1)          use v21 to test decoder
00001A0E  E756 0010 0C5C                           1169+          VISTR V21,V22,0,1                test instruction
00001A14  B98D 0020                                1170+          EPSW  R2,R0              extract psw
00001A18  5020 500C                      0000000C  1171+          ST    R2,CCPSW                to save CC
00001A1C  E750 5040 080E                 000019E0  1172+          VST   V21,V1O14          save v1 output
00001A22  07FB                                     1173+          BR    R11                return
00001A24                                           1174+RE14      DC    0F                 V1 for this test
00001A24                                           1175+          DROP  R5
00001A24  01020304 05060708                        1176           DC    XL16'01020304 05060708 090A0B00 00000000'   v1
00001A2C  090A0B00 00000000
00001A34  01020304 05060708                        1177           DC    XL16'01020304 05060708 090A0B00 0D0E0F10'   v2
00001A3C  090A0B00 0D0E0F10
                                                   1178
                                                   1179           VRR_A VISTR,0,1,0
00001A48                                           1180+          DS    0FD
00001A48                           00001A48        1181+          USING *,R5               base for test data and test routine
00001A48  00001AA0                                 1182+T15       DC    A(X15)             address of test routine
00001A4C  000F                                     1183+          DC    H'15'              test number
00001A4E  00                                       1184+          DC    X'00'
00001A4F  00                                       1185+          DC    HL1'0'                  M3 used
00001A50  01                                       1186+          DC    HL1'1'                  M5 used
00001A51  00                                       1187+          DC    HL1'0'             CC
00001A52  07                                       1188+          DC    HL1'7'             CC failed mask
00001A54  00000000 00000000                        1189+          DS    2F                 extracted PSW after test (has CC)
00001A5C  FF                                       1190+          DC    X'FF'              extracted CC, if test failed
00001A5D  E5C9E2E3 D9404040                        1191+          DC    CL8'VISTR'         instruction name
00001A68  00001ACC                                 1192+          DC    A(RE15)            address of v1 result
00001A6C  00001ADC                                 1193+          DC    A(RE15+16)         address of v2 source
00001A70  00001AEC                                 1194+          DC    A(RE15+32)         address of v3 source
00001A74  00000010                                 1195+          DC    A(16)              result length
00001A78  00001ACC                                 1196+REA15     DC    A(RE15)            result address
00001A80  00000000 00000000                        1197+          DS    FD                 gap
00001A88  00000000 00000000                        1198+V1O15     DS    XL16               V1 output
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001A90  00000000 00000000
00001A98  00000000 00000000                         1199+         DS    FD                  gap
                                                    1200+*
00001AA0                                            1201+X15      DS    0F
00001AA0  4110 8EF8                       000010F8  1202+         LA    R1,V1FUDGE         load v21 fudge
00001AA4  E751 0000 0806                  00000000  1203+         VL    v21,0(R1)
00001AAA  E310 5024 0014                  00000024  1204+         LGF   R1,V2ADDR           load v2 source
00001AB0  E761 0000 0806                  00000000  1205+         VL    v22,0(R1)           use v21 to test decoder
00001AB6  E756 0010 0C5C                            1206+         VISTR V21,V22,0,1                test instruction
00001ABC  B98D 0020                                 1207+         EPSW  R2,R0               extract psw
00001AC0  5020 500C                       0000000C  1208+         ST    R2,CCPSW               to save CC
00001AC4  E750 5040 080E                  00001A88  1209+         VST   V21,V1O15           save v1 output
00001ACA  07FB                                      1210+         BR    R11                 return
00001ACC                                            1211+RE15     DC    0F                  V1 for this test
00001ACC                                            1212+         DROP  R5
00001ACC  01020304 05060708                         1213          DC    XL16'01020304 05060708 090A0000 00000000'   v1
00001AD4  090A0000 00000000
00001ADC  01020304 05060708                         1214          DC    XL16'01020304 05060708 090A000C 0D0E0F10'   v2
00001AE4  090A000C 0D0E0F10
                                                    1215
                                                    1216          VRR_A VISTR,0,1,0
00001AF0                                            1217+         DS    0FD
00001AF0                  00001AF0                  1218+         USING *,R5                base for test data and test routine
00001AF0  00001B48                                  1219+T16      DC    A(X16)              address of test routine
00001AF4  0010                                      1220+         DC    H'16'               test number
00001AF6  00                                        1221+         DC    X'00'
00001AF7  00                                        1222+         DC    HL1'0'                   M3 used
00001AF8  01                                        1223+         DC    HL1'1'                   M5 used
00001AF9  00                                        1224+         DC    HL1'0'              CC
00001AFA  07                                        1225+         DC    HL1'7'              CC failed mask
00001AFC  00000000 00000000                         1226+         DS    2F                  extracted PSW after test (has CC)
00001B04  FF                                        1227+         DC    X'FF'               extracted CC, if test failed
00001B05  E5C9E2E3 D9404040                         1228+         DC    CL8'VISTR'          instruction name
00001B10  00001B74                                  1229+         DC    A(RE16)             address of v1 result
00001B14  00001B84                                  1230+         DC    A(RE16+16)          address of v2 source
00001B18  00001B94                                  1231+         DC    A(RE16+32)          address of v3 source
00001B1C  00000010                                  1232+         DC    A(16)               result length
00001B20  00001B74                                  1233+REA16    DC    A(RE16)             result address
00001B28  00000000 00000000                         1234+         DS    FD                  gap
00001B30  00000000 00000000                         1235+V1O16    DS    XL16                V1 output
00001B38  00000000 00000000
00001B40  00000000 00000000                         1236+         DS    FD                  gap
                                                    1237+*
00001B48                                            1238+X16      DS    0F
00001B48  4110 8EF8                       000010F8  1239+         LA    R1,V1FUDGE         load v21 fudge
00001B4C  E751 0000 0806                  00000000  1240+         VL    v21,0(R1)
00001B52  E310 5024 0014                  00000024  1241+         LGF   R1,V2ADDR           load v2 source
00001B58  E761 0000 0806                  00000000  1242+         VL    v22,0(R1)           use v21 to test decoder
00001B5E  E756 0010 0C5C                            1243+         VISTR V21,V22,0,1                test instruction
00001B64  B98D 0020                                 1244+         EPSW  R2,R0               extract psw
00001B68  5020 500C                       0000000C  1245+         ST    R2,CCPSW               to save CC
00001B6C  E750 5040 080E                  00001B30  1246+         VST   V21,V1O16           save v1 output
00001B72  07FB                                      1247+         BR    R11                 return
00001B74                                            1248+RE16     DC    0F                  V1 for this test
00001B74                                            1249+         DROP  R5
00001B74  01020304 05060708                         1250          DC    XL16'01020304 05060708 09000000 00000000'   v1
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001B7C  09000000 00000000
00001B84  01020304 05060708                        1251          DC    XL16'01020304 05060708 09000B0C 0D0E0F10'   v2
00001B8C  09000B0C 0D0E0F10
                                                   1252
                                                   1253          VRR_A VISTR,0,1,0
00001B98                                           1254+         DS    0FD
00001B98                     00001B98              1255+         USING *,R5                base for test data and test routine
00001B98  00001BF0                                 1256+T17      DC    A(X17)              address of test routine
00001B9C  0011                                     1257+         DC    H'17'               test number
00001B9E  00                                       1258+         DC    X'00'
00001B9F  00                                       1259+         DC    HL1'0'                   M3 used
00001BA0  01                                       1260+         DC    HL1'1'                   M5 used
00001BA1  00                                       1261+         DC    HL1'0'              CC
00001BA2  07                                       1262+         DC    HL1'7'              CC failed mask
00001BA4  00000000 00000000                        1263+         DS    2F                  extracted PSW after test (has CC)
00001BAC  FF                                       1264+         DC    X'FF'               extracted CC, if test failed
00001BAD  E5C9E2E3 D9404040                        1265+         DC    CL8'VISTR'          instruction name
00001BB8  00001C1C                                 1266+         DC    A(RE17)             address of v1 result
00001BBC  00001C2C                                 1267+         DC    A(RE17+16)          address of v2 source
00001BC0  00001C3C                                 1268+         DC    A(RE17+32)          address of v3 source
00001BC4  00000010                                 1269+         DC    A(16)               result length
00001BC8  00001C1C                                 1270+REA17    DC    A(RE17)             result address
00001BD0  00000000 00000000                        1271+         DS    FD                  gap
00001BD8  00000000 00000000                        1272+V1O17    DS    XL16                V1 output
00001BE0  00000000 00000000
00001BE8  00000000 00000000                        1273+         DS    FD                  gap
                                                   1274+*
00001BF0                                           1275+X17      DS    0F
00001BF0  4110 8EF8                       000010F8 1276+         LA    R1,V1FUDGE        load v21 fudge
00001BF4  E751 0000 0806                  00000000 1277+         VL    v21,0(R1)
00001BFA  E310 5024 0014                  00000024 1278+         LGF   R1,V2ADDR          load v2 source
00001C00  E761 0000 0806                  00000000 1279+         VL    v22,0(R1)           use v21 to test decoder
00001C06  E756 0010 0C5C                           1280+         VISTR V21,V22,0,1                test instruction
00001C0C  B98D 0020                                1281+         EPSW  R2,R0               extract psw
00001C10  5020 500C                       0000000C 1282+         ST    R2,CCPSW               to save CC
00001C14  E750 5040 080E                  00001BD8 1283+         VST   V21,V1O17           save v1 output
00001C1A  07FB                                     1284+         BR    R11                 return
00001C1C                                           1285+RE17     DC    0F                  V1 for this test
00001C1C                                           1286+         DROP  R5
00001C1C  01020304 05060708                        1287          DC    XL16'01020304 05060708 00000000 00000000'   v1
00001C24  00000000 00000000
00001C2C  01020304 05060708                        1288          DC    XL16'01020304 05060708 000A0B0C 0D0E0F10'   v2
00001C34  000A0B0C 0D0E0F10
                                                   1289
                                                   1290          VRR_A VISTR,0,1,0
00001C40                                           1291+         DS    0FD
00001C40                     00001C40              1292+         USING *,R5                base for test data and test routine
00001C40  00001C98                                 1293+T18      DC    A(X18)              address of test routine
00001C44  0012                                     1294+         DC    H'18'               test number
00001C46  00                                       1295+         DC    X'00'
00001C47  00                                       1296+         DC    HL1'0'                   M3 used
00001C48  01                                       1297+         DC    HL1'1'                   M5 used
00001C49  00                                       1298+         DC    HL1'0'              CC
00001C4A  07                                       1299+         DC    HL1'7'              CC failed mask
00001C4C  00000000 00000000                        1300+         DS    2F                  extracted PSW after test (has CC)
00001C54  FF                                       1301+         DC    X'FF'               extracted CC, if test failed
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001C55  E5C9E2E3 D9404040                        1302+          DC    CL8'VISTR'          instruction name
00001C60  00001CC4                                 1303+          DC    A(RE18)             address of v1 result
00001C64  00001CD4                                 1304+          DC    A(RE18+16)          address of v2 source
00001C68  00001CE4                                 1305+          DC    A(RE18+32)          address of v3 source
00001C6C  00000010                                 1306+          DC    A(16)               result length
00001C70  00001CC4                                 1307+REA18     DC    A(RE18)             result address
00001C78  00000000 00000000                        1308+          DS    FD                  gap
00001C80  00000000 00000000                        1309+V1O18     DS    XL16                V1 output
00001C88  00000000 00000000
00001C90  00000000 00000000                        1310+          DS    FD                  gap
                                                   1311+*
00001C98                                           1312+X18       DS    0F
00001C98  4110 8EF8                      000010F8  1313+          LA    R1,V1FUDGE         load v21 fudge
00001C9C  E751 0000 0806                 00000000  1314+          VL    v21,0(R1)
00001CA2  E310 5024 0014                 00000024  1315+          LGF   R1,V2ADDR           load v2 source
00001CA8  E761 0000 0806                 00000000  1316+          VL    v22,0(R1)           use v21 to test decoder
00001CAE  E756 0010 0C5C                           1317+          VISTR V21,V22,0,1                 test instruction
00001CB4  B98D 0020                                1318+          EPSW  R2,R0               extract psw
00001CB8  5020 500C                      0000000C  1319+          ST    R2,CCPSW               to save CC
00001CBC  E750 5040 080E                 00001C80  1320+          VST   V21,V1O18           save v1 output
00001CC2  07FB                                     1321+          BR    R11                 return
00001CC4                                           1322+RE18      DC    0F                  V1 for this test
00001CC4                                           1323+          DROP  R5
00001CC4  01020304 05060700                        1324           DC    XL16'01020304 05060700 00000000 00000000'   v1
00001CCC  00000000 00000000
00001CD4  01020304 05060700                        1325           DC    XL16'01020304 05060700 090A0B0C 0D0E0F10'   v2
00001CDC  090A0B0C 0D0E0F10
                                                   1326
                                                   1327           VRR_A VISTR,0,1,0
00001CE8                                           1328+          DS    0FD
00001CE8                           00001CE8        1329+          USING *,R5                base for test data and test routine
00001CE8  00001D40                                 1330+T19       DC    A(X19)              address of test routine
00001CEC  0013                                     1331+          DC    H'19'               test number
00001CEE  00                                       1332+          DC    X'00'
00001CEF  00                                       1333+          DC    HL1'0'                   M3 used
00001CF0  01                                       1334+          DC    HL1'1'                   M5 used
00001CF1  00                                       1335+          DC    HL1'0'              CC
00001CF2  07                                       1336+          DC    HL1'7'              CC failed mask
00001CF4  00000000 00000000                        1337+          DS    2F                  extracted PSW after test (has CC)
00001CFC  FF                                       1338+          DC    X'FF'               extracted CC, if test failed
00001CFD  E5C9E2E3 D9404040                        1339+          DC    CL8'VISTR'          instruction name
00001D08  00001D6C                                 1340+          DC    A(RE19)             address of v1 result
00001D0C  00001D7C                                 1341+          DC    A(RE19+16)          address of v2 source
00001D10  00001D8C                                 1342+          DC    A(RE19+32)          address of v3 source
00001D14  00000010                                 1343+          DC    A(16)               result length
00001D18  00001D6C                                 1344+REA19     DC    A(RE19)             result address
00001D20  00000000 00000000                        1345+          DS    FD                  gap
00001D28  00000000 00000000                        1346+V1O19     DS    XL16                V1 output
00001D30  00000000 00000000
00001D38  00000000 00000000                        1347+          DS    FD                  gap
                                                   1348+*
00001D40                                           1349+X19       DS    0F
00001D40  4110 8EF8                      000010F8  1350+          LA    R1,V1FUDGE         load v21 fudge
00001D44  E751 0000 0806                 00000000  1351+          VL    v21,0(R1)
00001D4A  E310 5024 0014                 00000024  1352+          LGF   R1,V2ADDR           load v2 source
00001D50  E761 0000 0806                 00000000  1353+          VL    v22,0(R1)           use v21 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001D56  E756 0010 0C5C                           1354+         VISTR V21,V22,0,1               test instruction
00001D5C  B98D 0020                                1355+         EPSW  R2,R0               extract psw
00001D60  5020 500C                     0000000C   1356+         ST    R2,CCPSW               to save CC
00001D64  E750 5040 080E                00001D28   1357+         VST   V21,V1O19           save v1 output
00001D6A  07FB                                     1358+         BR    R11                 return
00001D6C                                           1359+RE19     DC    0F                  V1 for this test
00001D6C                                           1360+         DROP  R5
00001D6C  01020304 05060000                        1361          DC    XL16'01020304 05060000 00000000 00000000'   v1
00001D74  00000000 00000000
00001D7C  01020304 05060008                        1362          DC    XL16'01020304 05060008 090A0B0C 0D0E0F10'   v2
00001D84  090A0B0C 0D0E0F10
                                                   1363
                                                   1364          VRR_A VISTR,0,1,0
00001D90                                           1365+         DS    0FD
00001D90                  00001D90                 1366+         USING *,R5                base for test data and test routine
00001D90  00001DE8                                 1367+T20      DC    A(X20)              address of test routine
00001D94  0014                                     1368+         DC    H'20'               test number
00001D96  00                                       1369+         DC    X'00'
00001D97  00                                       1370+         DC    HL1'0'                   M3 used
00001D98  01                                       1371+         DC    HL1'1'                   M5 used
00001D99  00                                       1372+         DC    HL1'0'              CC
00001D9A  07                                       1373+         DC    HL1'7'              CC failed mask
00001D9C  00000000 00000000                        1374+         DS    2F                  extracted PSW after test (has CC)
00001DA4  FF                                       1375+         DC    X'FF'               extracted CC, if test failed
00001DA5  E5C9E2E3 D9404040                        1376+         DC    CL8'VISTR'          instruction name
00001DB0  00001E14                                 1377+         DC    A(RE20)             address of v1 result
00001DB4  00001E24                                 1378+         DC    A(RE20+16)          address of v2 source
00001DB8  00001E34                                 1379+         DC    A(RE20+32)          address of v3 source
00001DBC  00000010                                 1380+         DC    A(16)               result length
00001DC0  00001E14                                 1381+REA20    DC    A(RE20)             result address
00001DC8  00000000 00000000                        1382+         DS    FD                  gap
00001DD0  00000000 00000000                        1383+V1O20    DS    XL16                V1 output
00001DD8  00000000 00000000
00001DE0  00000000 00000000                        1384+         DS    FD                  gap
                                                   1385+*
00001DE8                                           1386+X20      DS    0F
00001DE8  4110 8EF8                     000010F8   1387+         LA    R1,V1FUDGE         load v21 fudge
00001DEC  E751 0000 0806                00000000   1388+         VL    v21,0(R1)
00001DF2  E310 5024 0014                00000024   1389+         LGF   R1,V2ADDR           load v2 source
00001DF8  E761 0000 0806                00000000   1390+         VL    v22,0(R1)           use v21 to test decoder
00001DFE  E756 0010 0C5C                           1391+         VISTR V21,V22,0,1               test instruction
00001E04  B98D 0020                                1392+         EPSW  R2,R0               extract psw
00001E08  5020 500C                     0000000C   1393+         ST    R2,CCPSW               to save CC
00001E0C  E750 5040 080E                00001DD0   1394+         VST   V21,V1O20           save v1 output
00001E12  07FB                                     1395+         BR    R11                 return
00001E14                                           1396+RE20     DC    0F                  V1 for this test
00001E14                                           1397+         DROP  R5
00001E14  01020304 05000000                        1398          DC    XL16'01020304 05000000 00000000 00000000'   v1
00001E1C  00000000 00000000
00001E24  01020304 05000708                        1399          DC    XL16'01020304 05000708 090A0B0C 0D0E0F10'   v2
00001E2C  090A0B0C 0D0E0F10
                                                   1400
                                                   1401          VRR_A VISTR,0,1,0
00001E38                                           1402+         DS    0FD
00001E38                  00001E38                 1403+         USING *,R5                base for test data and test routine
00001E38  00001E90                                 1404+T21      DC    A(X21)              address of test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001E3C  0015                                    1405+          DC    H'21'              test number
00001E3E  00                                      1406+          DC    X'00'
00001E3F  00                                      1407+          DC    HL1'0'                  M3 used
00001E40  01                                      1408+          DC    HL1'1'                  M5 used
00001E41  00                                      1409+          DC    HL1'0'             CC
00001E42  07                                      1410+          DC    HL1'7'             CC failed mask
00001E44  00000000 00000000                       1411+          DS    2F                 extracted PSW after test (has CC)
00001E4C  FF                                      1412+          DC    X'FF'              extracted CC, if test failed
00001E4D  E5C9E2E3 D9404040                       1413+          DC    CL8'VISTR'         instruction name
00001E58  00001EBC                                1414+          DC    A(RE21)            address of v1 result
00001E5C  00001ECC                                1415+          DC    A(RE21+16)         address of v2 source
00001E60  00001EDC                                1416+          DC    A(RE21+32)         address of v3 source
00001E64  00000010                                1417+          DC    A(16)              result length
00001E68  00001EBC                                1418+REA21     DC    A(RE21)            result address
00001E70  00000000 00000000                       1419+          DS    FD                 gap
00001E78  00000000 00000000                       1420+V1O21     DS    XL16               V1 output
00001E80  00000000 00000000
00001E88  00000000 00000000                       1421+          DS    FD                 gap
                                                  1422+*
00001E90                                          1423+X21       DS    0F
00001E90  4110 8EF8                  000010F8     1424+          LA    R1,V1FUDGE        load v21 fudge
00001E94  E751 0000 0806             00000000     1425+          VL    v21,0(R1)
00001E9A  E310 5024 0014             00000024     1426+          LGF   R1,V2ADDR          load v2 source
00001EA0  E761 0000 0806             00000000     1427+          VL    v22,0(R1)          use v21 to test decoder
00001EA6  E756 0010 0C5C                          1428+          VISTR V21,V22,0,1                test instruction
00001EAC  B98D 0020                               1429+          EPSW  R2,R0              extract psw
00001EB0  5020 500C                  0000000C     1430+          ST    R2,CCPSW                to save CC
00001EB4  E750 5040 080E             00001E78     1431+          VST   V21,V1O21          save v1 output
00001EBA  07FB                                    1432+          BR    R11                return
00001EBC                                          1433+RE21      DC    0F                 V1 for this test
00001EBC                                          1434+          DROP  R5
00001EBC  01020304 00000000                       1435           DC    XL16'01020304 00000000 00000000 00000000'   v1
00001EC4  00000000 00000000
00001ECC  01020304 00060708                       1436           DC    XL16'01020304 00060708 090A0B0C 0D0E0F10'   v2
00001ED4  090A0B0C 0D0E0F10
                                                  1437
                                                  1438           VRR_A VISTR,0,1,0
00001EE0                                          1439+          DS    0FD
00001EE0                       00001EE0           1440+          USING *,R5               base for test data and test routine
00001EE0  00001F38                                1441+T22       DC    A(X22)             address of test routine
00001EE4  0016                                    1442+          DC    H'22'              test number
00001EE6  00                                      1443+          DC    X'00'
00001EE7  00                                      1444+          DC    HL1'0'                  M3 used
00001EE8  01                                      1445+          DC    HL1'1'                  M5 used
00001EE9  00                                      1446+          DC    HL1'0'             CC
00001EEA  07                                      1447+          DC    HL1'7'             CC failed mask
00001EEC  00000000 00000000                       1448+          DS    2F                 extracted PSW after test (has CC)
00001EF4  FF                                      1449+          DC    X'FF'              extracted CC, if test failed
00001EF5  E5C9E2E3 D9404040                       1450+          DC    CL8'VISTR'         instruction name
00001F00  00001F64                                1451+          DC    A(RE22)            address of v1 result
00001F04  00001F74                                1452+          DC    A(RE22+16)         address of v2 source
00001F08  00001F84                                1453+          DC    A(RE22+32)         address of v3 source
00001F0C  00000010                                1454+          DC    A(16)              result length
00001F10  00001F64                                1455+REA22     DC    A(RE22)            result address
00001F18  00000000 00000000                       1456+          DS    FD                 gap
00001F20  00000000 00000000                       1457+V1O22     DS    XL16               V1 output
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001F28  00000000 00000000
00001F30  00000000 00000000                        1458+         DS    FD                  gap
                                                   1459+*
00001F38                                           1460+X22      DS    0F
00001F38  4110 8EF8                      000010F8  1461+          LA    R1,V1FUDGE         load v21 fudge
00001F3C  E751 0000 0806                 00000000  1462+          VL    v21,0(R1)
00001F42  E310 5024 0014                 00000024  1463+          LGF   R1,V2ADDR           load v2 source
00001F48  E761 0000 0806                 00000000  1464+          VL    v22,0(R1)           use v21 to test decoder
00001F4E  E756 0010 0C5C                           1465+          VISTR V21,V22,0,1                 test instruction
00001F54  B98D 0020                                1466+          EPSW  R2,R0               extract psw
00001F58  5020 500C                      0000000C  1467+          ST    R2,CCPSW               to save CC
00001F5C  E750 5040 080E                 00001F20  1468+          VST   V21,V1O22           save v1 output
00001F62  07FB                                     1469+          BR    R11                 return
00001F64                                           1470+RE22     DC    0F                  V1 for this test
00001F64                                           1471+          DROP  R5
00001F64  01020300 00000000                        1472           DC    XL16'01020300 00000000 00000000 00000000'   v1
00001F6C  00000000 00000000
00001F74  01020300 05060708                        1473           DC    XL16'01020300 05060708 090A0B0C 0D0E0F10'   v2
00001F7C  090A0B0C 0D0E0F10
                                                   1474
                                                   1475           VRR_A VISTR,0,1,0
00001F88                                           1476+          DS    0FD
00001F88                 00001F88                  1477+          USING *,R5                base for test data and test routine
00001F88  00001FE0                                 1478+T23      DC    A(X23)              address of test routine
00001F8C  0017                                     1479+          DC    H'23'               test number
00001F8E  00                                       1480+          DC    X'00'
00001F8F  00                                       1481+          DC    HL1'0'                    M3 used
00001F90  01                                       1482+          DC    HL1'1'                    M5 used
00001F91  00                                       1483+          DC    HL1'0'              CC
00001F92  07                                       1484+          DC    HL1'7'              CC failed mask
00001F94  00000000 00000000                        1485+          DS    2F                  extracted PSW after test (has CC)
00001F9C  FF                                       1486+          DC    X'FF'               extracted CC, if test failed
00001F9D  E5C9E2E3 D9404040                        1487+          DC    CL8'VISTR'          instruction name
00001FA8  0000200C                                 1488+          DC    A(RE23)             address of v1 result
00001FAC  0000201C                                 1489+          DC    A(RE23+16)          address of v2 source
00001FB0  0000202C                                 1490+          DC    A(RE23+32)          address of v3 source
00001FB4  00000010                                 1491+          DC    A(16)               result length
00001FB8  0000200C                                 1492+REA23    DC    A(RE23)             result address
00001FC0  00000000 00000000                        1493+          DS    FD                  gap
00001FC8  00000000 00000000                        1494+V1O23    DS    XL16                V1 output
00001FD0  00000000 00000000
00001FD8  00000000 00000000                        1495+          DS    FD                  gap
                                                   1496+*
00001FE0                                           1497+X23      DS    0F
00001FE0  4110 8EF8                      000010F8  1498+          LA    R1,V1FUDGE         load v21 fudge
00001FE4  E751 0000 0806                 00000000  1499+          VL    v21,0(R1)
00001FEA  E310 5024 0014                 00000024  1500+          LGF   R1,V2ADDR           load v2 source
00001FF0  E761 0000 0806                 00000000  1501+          VL    v22,0(R1)           use v21 to test decoder
00001FF6  E756 0010 0C5C                           1502+          VISTR V21,V22,0,1                 test instruction
00001FFC  B98D 0020                                1503+          EPSW  R2,R0               extract psw
00002000  5020 500C                      0000000C  1504+          ST    R2,CCPSW               to save CC
00002004  E750 5040 080E                 00001FC8  1505+          VST   V21,V1O23           save v1 output
0000200A  07FB                                     1506+          BR    R11                 return
0000200C                                           1507+RE23     DC    0F                  V1 for this test
0000200C                                           1508+          DROP  R5
0000200C  01020000 00000000                        1509           DC    XL16'01020000 00000000 00000000 00000000'   v1
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002014  00000000 00000000
0000201C  01020004 05060708                        1510          DC    XL16'01020004 05060708 090A0B0C 0D0E0F10'   v2
00002024  090A0B0C 0D0E0F10
                                                   1511
                                                   1512          VRR_A VISTR,0,1,0
00002030                                           1513+         DS    0FD
00002030                     00002030              1514+         USING *,R5               base for test data and test routine
00002030  00002088                                 1515+T24      DC    A(X24)             address of test routine
00002034  0018                                     1516+         DC    H'24'              test number
00002036  00                                       1517+         DC    X'00'
00002037  00                                       1518+         DC    HL1'0'                  M3 used
00002038  01                                       1519+         DC    HL1'1'                  M5 used
00002039  00                                       1520+         DC    HL1'0'             CC
0000203A  07                                       1521+         DC    HL1'7'             CC failed mask
0000203C  00000000 00000000                        1522+         DS    2F                 extracted PSW after test (has CC)
00002044  FF                                       1523+         DC    X'FF'              extracted CC, if test failed
00002045  E5C9E2E3 D9404040                        1524+         DC    CL8'VISTR'         instruction name
00002050  000020B4                                 1525+         DC    A(RE24)            address of v1 result
00002054  000020C4                                 1526+         DC    A(RE24+16)         address of v2 source
00002058  000020D4                                 1527+         DC    A(RE24+32)         address of v3 source
0000205C  00000010                                 1528+         DC    A(16)              result length
00002060  000020B4                                 1529+REA24    DC    A(RE24)            result address
00002068  00000000 00000000                        1530+         DS    FD                 gap
00002070  00000000 00000000                        1531+V1O24    DS    XL16               V1 output
00002078  00000000 00000000
00002080  00000000 00000000                        1532+         DS    FD                 gap
                                                   1533+*
00002088                                           1534+X24      DS    0F
00002088  4110 8EF8                     000010F8   1535+         LA    R1,V1FUDGE       load v21 fudge
0000208C  E751 0000 0806                00000000   1536+         VL    v21,0(R1)
00002092  E310 5024 0014                00000024   1537+         LGF   R1,V2ADDR         load v2 source
00002098  E761 0000 0806                00000000   1538+         VL    v22,0(R1)          use v21 to test decoder
0000209E  E756 0010 0C5C                           1539+         VISTR V21,V22,0,1                test instruction
000020A4  B98D 0020                                1540+         EPSW  R2,R0              extract psw
000020A8  5020 500C                     0000000C   1541+         ST    R2,CCPSW              to save CC
000020AC  E750 5040 080E                00002070   1542+         VST   V21,V1O24          save v1 output
000020B2  07FB                                     1543+         BR    R11                return
000020B4                                           1544+RE24     DC    0F                 V1 for this test
000020B4                                           1545+         DROP  R5
000020B4  01000000 00000000                        1546          DC    XL16'01000000 00000000 00000000 00000000'   v1
000020BC  00000000 00000000
000020C4  01000304 05060708                        1547          DC    XL16'01000304 05060708 090A0B0C 0D0E0F10'   v2
000020CC  090A0B0C 0D0E0F10
                                                   1548
                                                   1549          VRR_A VISTR,0,1,0
000020D8                                           1550+         DS    0FD
000020D8                     000020D8              1551+         USING *,R5               base for test data and test routine
000020D8  00002130                                 1552+T25      DC    A(X25)             address of test routine
000020DC  0019                                     1553+         DC    H'25'              test number
000020DE  00                                       1554+         DC    X'00'
000020DF  00                                       1555+         DC    HL1'0'                  M3 used
000020E0  01                                       1556+         DC    HL1'1'                  M5 used
000020E1  00                                       1557+         DC    HL1'0'             CC
000020E2  07                                       1558+         DC    HL1'7'             CC failed mask
000020E4  00000000 00000000                        1559+         DS    2F                 extracted PSW after test (has CC)
000020EC  FF                                       1560+         DC    X'FF'              extracted CC, if test failed
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000020ED  E5C9E2E3 D9404040                        1561+          DC    CL8'VISTR'          instruction name
000020F8  0000215C                                 1562+          DC    A(RE25)             address of v1 result
000020FC  0000216C                                 1563+          DC    A(RE25+16)          address of v2 source
00002100  0000217C                                 1564+          DC    A(RE25+32)          address of v3 source
00002104  00000010                                 1565+          DC    A(16)               result length
00002108  0000215C                                 1566+REA25     DC    A(RE25)             result address
00002110  00000000 00000000                        1567+          DS    FD                  gap
00002118  00000000 00000000                        1568+V1O25     DS    XL16                V1 output
00002120  00000000 00000000
00002128  00000000 00000000                        1569+          DS    FD                  gap
                                                   1570+*
00002130                                           1571+X25       DS    0F
00002130  4110 8EF8                       000010F8 1572+          LA    R1,V1FUDGE         load v21 fudge
00002134  E751 0000 0806                  00000000 1573+          VL    v21,0(R1)
0000213A  E310 5024 0014                  00000024 1574+          LGF   R1,V2ADDR           load v2 source
00002140  E761 0000 0806                  00000000 1575+          VL    v22,0(R1)           use v21 to test decoder
00002146  E756 0010 0C5C                           1576+          VISTR V21,V22,0,1                 test instruction
0000214C  B98D 0020                                1577+          EPSW  R2,R0               extract psw
00002150  5020 500C                       0000000C 1578+          ST    R2,CCPSW               to save CC
00002154  E750 5040 080E                  00002118 1579+          VST   V21,V1O25           save v1 output
0000215A  07FB                                     1580+          BR    R11                 return
0000215C                                           1581+RE25      DC    0F                  V1 for this test
0000215C                                           1582+          DROP  R5
0000215C  00000000 00000000                        1583           DC    XL16'00000000 00000000 00000000 00000000'   v1
00002164  00000000 00000000
0000216C  00020304 05060708                        1584           DC    XL16'00020304 05060708 090A0B0C 0D0E0F10'   v2
00002174  090A0B0C 0D0E0F10
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   1586 *halfword
                                                   1587          VRR_A VISTR,1,1,3
00002180                                           1588+         DS    0FD
00002180                       00002180            1589+         USING *,R5              base for test data and test routine
00002180  000021D8                                 1590+T26      DC    A(X26)            address of test routine
00002184  001A                                     1591+         DC    H'26'             test number
00002186  00                                       1592+         DC    X'00'
00002187  01                                       1593+         DC    HL1'1'                 M3 used
00002188  01                                       1594+         DC    HL1'1'                 M5 used
00002189  03                                       1595+         DC    HL1'3'            CC
0000218A  0E                                       1596+         DC    HL1'14'           CC failed mask
0000218C  00000000 00000000                        1597+         DS    2F                extracted PSW after test (has CC)
00002194  FF                                       1598+         DC    X'FF'             extracted CC, if test failed
00002195  E5C9E2E3 D9404040                       1599+         DC    CL8'VISTR'        instruction name
000021A0  00002204                                 1600+         DC    A(RE26)           address of v1 result
000021A4  00002214                                 1601+         DC    A(RE26+16)        address of v2 source
000021A8  00002224                                 1602+         DC    A(RE26+32)        address of v3 source
000021AC  00000010                                 1603+         DC    A(16)             result length
000021B0  00002204                                 1604+REA26    DC    A(RE26)           result address
000021B8  00000000 00000000                        1605+         DS    FD                gap
000021C0  00000000 00000000                        1606+V1O26    DS    XL16              V1 output
000021C8  00000000 00000000
000021D0  00000000 00000000                        1607+         DS    FD                gap
                                                   1608+*
000021D8                                           1609+X26      DS    0F
000021D8  4110 8EF8                     000010F8   1610+         LA    R1,V1FUDGE        load v21 fudge
000021DC  E751 0000 0806                00000000   1611+         VL    v21,0(R1)
000021E2  E310 5024 0014                00000024   1612+         LGF   R1,V2ADDR         load v2 source
000021E8  E761 0000 0806                00000000   1613+         VL    v22,0(R1)         use v21 to test decoder
000021EE  E756 0010 1C5C                           1614+         VISTR V21,V22,1,1               test instruction
000021F4  B98D 0020                                1615+         EPSW  R2,R0             extract psw
000021F8  5020 500C                     0000000C   1616+         ST    R2,CCPSW             to save CC
000021FC  E750 5040 080E                000021C0   1617+         VST   V21,V1O26         save v1 output
00002202  07FB                                     1618+         BR    R11               return
00002204                                           1619+RE26     DC    0F                V1 for this test
00002204                                           1620+         DROP  R5
00002204  88888888 77777777                        1621          DC    XL16'88888888 77777777 66666666 55555555'   v2
0000220C  66666666 55555555
00002214  88888888 77777777                        1622          DC    XL16'88888888 77777777 66666666 55555555'   v2
0000221C  66666666 55555555
                                                   1623
                                                   1624          VRR_A VISTR,1,1,0
00002228                                           1625+         DS    0FD
00002228                       00002228            1626+         USING *,R5              base for test data and test routine
00002228  00002280                                 1627+T27      DC    A(X27)            address of test routine
0000222C  001B                                     1628+         DC    H'27'             test number
0000222E  00                                       1629+         DC    X'00'
0000222F  01                                       1630+         DC    HL1'1'                 M3 used
00002230  01                                       1631+         DC    HL1'1'                 M5 used
00002231  00                                       1632+         DC    HL1'0'            CC
00002232  07                                       1633+         DC    HL1'7'            CC failed mask
00002234  00000000 00000000                        1634+         DS    2F                extracted PSW after test (has CC)
0000223C  FF                                       1635+         DC    X'FF'             extracted CC, if test failed
0000223D  E5C9E2E3 D9404040                        1636+         DC    CL8'VISTR'        instruction name
00002248  000022AC                                 1637+         DC    A(RE27)           address of v1 result
0000224C  000022BC                                 1638+         DC    A(RE27+16)        address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002250  000022CC                                1639+          DC    A(RE27+32)          address of v3 source
00002254  00000010                                1640+          DC    A(16)               result length
00002258  000022AC                                1641+REA27     DC    A(RE27)             result address
00002260  00000000 00000000                       1642+          DS    FD                  gap
00002268  00000000 00000000                       1643+V1O27     DS    XL16                V1 output
00002270  00000000 00000000
00002278  00000000 00000000                       1644+          DS    FD                  gap
                                                  1645+*
00002280                                          1646+X27       DS    0F
00002280  4110 8EF8                     000010F8  1647+          LA    R1,V1FUDGE        load v21 fudge
00002284  E751 0000 0806                00000000  1648+          VL    v21,0(R1)
0000228A  E310 5024 0014                00000024  1649+          LGF   R1,V2ADDR          load v2 source
00002290  E761 0000 0806                00000000  1650+          VL    v22,0(R1)          use v21 to test decoder
00002296  E756 0010 1C5C                          1651+          VISTR V21,V22,1,1                test instruction
0000229C  B98D 0020                               1652+          EPSW  R2,R0              extract psw
000022A0  5020 500C                     0000000C  1653+          ST    R2,CCPSW              to save CC
000022A4  E750 5040 080E                00002268  1654+          VST   V21,V1O27          save v1 output
000022AA  07FB                                    1655+          BR    R11                return
000022AC                                          1656+RE27      DC    0F                 V1 for this test
000022AC                                          1657+          DROP  R5
000022AC  88888888 77777777                       1658           DC    XL16'88888888 77777777 66666666 55550000'   v2
000022B4  66666666 55550000
000022BC  88888888 77777777                       1659           DC    XL16'88888888 77777777 66666666 55550000'   v2
000022C4  66666666 55550000
                                                  1660
                                                  1661           VRR_A VISTR,1,1,0
000022D0                                          1662+          DS    0FD
000022D0                        000022D0          1663+          USING *,R5               base for test data and test routine
000022D0  00002328                                1664+T28       DC    A(X28)             address of test routine
000022D4  001C                                    1665+          DC    H'28'              test number
000022D6  00                                      1666+          DC    X'00'
000022D7  01                                      1667+          DC    HL1'1'                  M3 used
000022D8  01                                      1668+          DC    HL1'1'                  M5 used
000022D9  00                                      1669+          DC    HL1'0'             CC
000022DA  07                                      1670+          DC    HL1'7'             CC failed mask
000022DC  00000000 00000000                       1671+          DS    2F                 extracted PSW after test (has CC)
000022E4  FF                                      1672+          DC    X'FF'              extracted CC, if test failed
000022E5  E5C9E2E3 D9404040                       1673+          DC    CL8'VISTR'         instruction name
000022F0  00002354                                1674+          DC    A(RE28)            address of v1 result
000022F4  00002364                                1675+          DC    A(RE28+16)         address of v2 source
000022F8  00002374                                1676+          DC    A(RE28+32)         address of v3 source
000022FC  00000010                                1677+          DC    A(16)              result length
00002300  00002354                                1678+REA28     DC    A(RE28)            result address
00002308  00000000 00000000                       1679+          DS    FD                 gap
00002310  00000000 00000000                       1680+V1O28     DS    XL16               V1 output
00002318  00000000 00000000
00002320  00000000 00000000                       1681+          DS    FD                 gap
                                                  1682+*
00002328                                          1683+X28       DS    0F
00002328  4110 8EF8                     000010F8  1684+          LA    R1,V1FUDGE        load v21 fudge
0000232C  E751 0000 0806                00000000  1685+          VL    v21,0(R1)
00002332  E310 5024 0014                00000024  1686+          LGF   R1,V2ADDR          load v2 source
00002338  E761 0000 0806                00000000  1687+          VL    v22,0(R1)          use v21 to test decoder
0000233E  E756 0010 1C5C                          1688+          VISTR V21,V22,1,1                test instruction
00002344  B98D 0020                               1689+          EPSW  R2,R0              extract psw
00002348  5020 500C                     0000000C  1690+          ST    R2,CCPSW              to save CC
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000234C  E750 5040 080E                 00002310  1691+          VST   V21,V1O28          save v1 output
00002352  07FB                                     1692+          BR    R11               return
00002354                                           1693+RE28      DC    0F                V1 for this test
00002354                                           1694+          DROP  R5
00002354  88888888 77777777                        1695           DC    XL16'88888888 77777777 66666666 00000000'   v2
0000235C  66666666 00000000
00002364  88888888 77777777                        1696           DC    XL16'88888888 77777777 66666666 00005555'   v2
0000236C  66666666 00005555
                                                   1697
                                                   1698           VRR_A VISTR,1,1,0
00002378                                           1699+          DS    0FD
00002378                   00002378                1700+          USING *,R5              base for test data and test routine
00002378  000023D0                                 1701+T29       DC    A(X29)            address of test routine
0000237C  001D                                     1702+          DC    H'29'             test number
0000237E  00                                       1703+          DC    X'00'
0000237F  01                                       1704+          DC    HL1'1'                 M3 used
00002380  01                                       1705+          DC    HL1'1'                 M5 used
00002381  00                                       1706+          DC    HL1'0'            CC
00002382  07                                       1707+          DC    HL1'7'            CC failed mask
00002384  00000000 00000000                        1708+          DS    2F                extracted PSW after test (has CC)
0000238C  FF                                       1709+          DC    X'FF'             extracted CC, if test failed
0000238D  E5C9E2E3 D9404040                        1710+          DC    CL8'VISTR'        instruction name
00002398  000023FC                                 1711+          DC    A(RE29)           address of v1 result
0000239C  0000240C                                 1712+          DC    A(RE29+16)        address of v2 source
000023A0  0000241C                                 1713+          DC    A(RE29+32)        address of v3 source
000023A4  00000010                                 1714+          DC    A(16)             result length
000023A8  000023FC                                 1715+REA29     DC    A(RE29)           result address
000023B0  00000000 00000000                        1716+          DS    FD                gap
000023B8  00000000 00000000                        1717+V1O29     DS    XL16              V1 output
000023C0  00000000 00000000
000023C8  00000000 00000000                        1718+          DS    FD                gap
                                                   1719+*
000023D0                                           1720+X29       DS    0F
000023D0  4110 8EF8                      000010F8  1721+          LA    R1,V1FUDGE       load v21 fudge
000023D4  E751 0000 0806                 00000000  1722+          VL    v21,0(R1)
000023DA  E310 5024 0014                 00000024  1723+          LGF   R1,V2ADDR          load v2 source
000023E0  E761 0000 0806                 00000000  1724+          VL    v22,0(R1)         use v21 to test decoder
000023E6  E756 0010 1C5C                           1725+          VISTR V21,V22,1,1               test instruction
000023EC  B98D 0020                                1726+          EPSW  R2,R0             extract psw
000023F0  5020 500C                      0000000C  1727+          ST    R2,CCPSW             to save CC
000023F4  E750 5040 080E                 000023B8  1728+          VST   V21,V1O29           save v1 output
000023FA  07FB                                     1729+          BR    R11               return
000023FC                                           1730+RE29      DC    0F                V1 for this test
000023FC                                           1731+          DROP  R5
000023FC  88888888 77777777                        1732           DC    XL16'88888888 77777777 66660000 00000000'   v2
00002404  66660000 00000000
0000240C  88888888 77777777                        1733           DC    XL16'88888888 77777777 66660000 55555555'   v2
00002414  66660000 55555555
                                                   1734
                                                   1735           VRR_A VISTR,1,1,0
00002420                                           1736+          DS    0FD
00002420                   00002420                1737+          USING *,R5              base for test data and test routine
00002420  00002478                                 1738+T30       DC    A(X30)            address of test routine
00002424  001E                                     1739+          DC    H'30'             test number
00002426  00                                       1740+          DC    X'00'
00002427  01                                       1741+          DC    HL1'1'                 M3 used
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002428  01                                       1742+         DC    HL1'1'                 M5 used
00002429  00                                       1743+         DC    HL1'0'              CC
0000242A  07                                       1744+         DC    HL1'7'              CC failed mask
0000242C  00000000 00000000                        1745+         DS    2F                  extracted PSW after test (has CC)
00002434  FF                                       1746+         DC    X'FF'               extracted CC, if test failed
00002435  E5C9E2E3 D9404040                        1747+         DC    CL8'VISTR'          instruction name
00002440  000024A4                                 1748+         DC    A(RE30)             address of v1 result
00002444  000024B4                                 1749+         DC    A(RE30+16)          address of v2 source
00002448  000024C4                                 1750+         DC    A(RE30+32)          address of v3 source
0000244C  00000010                                 1751+         DC    A(16)               result length
00002450  000024A4                                 1752+REA30    DC    A(RE30)             result address
00002458  00000000 00000000                        1753+         DS    FD                  gap
00002460  00000000 00000000                        1754+V1O30    DS    XL16                V1 output
00002468  00000000 00000000
00002470  00000000 00000000                        1755+         DS    FD                  gap
                                                   1756+*
00002478                                           1757+X30      DS    0F
00002478  4110 8EF8                      000010F8  1758+         LA    R1,V1FUDGE        load v21 fudge
0000247C  E751 0000 0806                 00000000  1759+         VL    v21,0(R1)
00002482  E310 5024 0014                 00000024  1760+         LGF   R1,V2ADDR          load v2 source
00002488  E761 0000 0806                 00000000  1761+         VL    v22,0(R1)          use v21 to test decoder
0000248E  E756 0010 1C5C                           1762+         VISTR V21,V22,1,1                test instruction
00002494  B98D 0020                                1763+         EPSW  R2,R0              extract psw
00002498  5020 500C                      0000000C  1764+         ST    R2,CCPSW              to save CC
0000249C  E750 5040 080E                 00002460  1765+         VST   V21,V1O30          save v1 output
000024A2  07FB                                     1766+         BR    R11                return
000024A4                                           1767+RE30     DC    0F                 V1 for this test
000024A4                                           1768+         DROP  R5
000024A4  88888888 77777777                       1769          DC    XL16'88888888 77777777 00000000 00000000'   v2
000024AC  00000000 00000000
000024B4  88888888 77777777                       1770          DC    XL16'88888888 77777777 00006666 55555555'   v2
000024BC  00006666 55555555
                                                   1771
                                                   1772          VRR_A VISTR,1,1,0
000024C8                                           1773+         DS    0FD
000024C8                       000024C8            1774+         USING *,R5               base for test data and test routine
000024C8  00002520                                 1775+T31      DC    A(X31)             address of test routine
000024CC  001F                                     1776+         DC    H'31'              test number
000024CE  00                                       1777+         DC    X'00'
000024CF  01                                       1778+         DC    HL1'1'                 M3 used
000024D0  01                                       1779+         DC    HL1'1'                 M5 used
000024D1  00                                       1780+         DC    HL1'0'              CC
000024D2  07                                       1781+         DC    HL1'7'              CC failed mask
000024D4  00000000 00000000                        1782+         DS    2F                  extracted PSW after test (has CC)
000024DC  FF                                       1783+         DC    X'FF'               extracted CC, if test failed
000024DD  E5C9E2E3 D9404040                        1784+         DC    CL8'VISTR'          instruction name
000024E8  0000254C                                 1785+         DC    A(RE31)             address of v1 result
000024EC  0000255C                                 1786+         DC    A(RE31+16)          address of v2 source
000024F0  0000256C                                 1787+         DC    A(RE31+32)          address of v3 source
000024F4  00000010                                 1788+         DC    A(16)               result length
000024F8  0000254C                                 1789+REA31    DC    A(RE31)             result address
00002500  00000000 00000000                        1790+         DS    FD                  gap
00002508  00000000 00000000                        1791+V1O31    DS    XL16                V1 output
00002510  00000000 00000000
00002518  00000000 00000000                        1792+         DS    FD                  gap
                                                   1793+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002520                                           1794+X31      DS    0F
00002520  4110 8EF8                      000010F8  1795+          LA    R1,V1FUDGE         load v21 fudge
00002524  E751 0000 0806                 00000000  1796+          VL    v21,0(R1)
0000252A  E310 5024 0014                 00000024  1797+          LGF   R1,V2ADDR           load v2 source
00002530  E761 0000 0806                 00000000  1798+          VL    v22,0(R1)           use v21 to test decoder
00002536  E756 0010 1C5C                           1799+          VISTR V21,V22,1,1                test instruction
0000253C  B98D 0020                                1800+          EPSW  R2,R0               extract psw
00002540  5020 500C                      0000000C  1801+          ST    R2,CCPSW               to save CC
00002544  E750 5040 080E                 00002508  1802+          VST   V21,V1O31           save v1 output
0000254A  07FB                                     1803+          BR    R11                 return
0000254C                                           1804+RE31     DC    0F                  V1 for this test
0000254C                                           1805+          DROP  R5
0000254C  88888888 77770000                        1806           DC    XL16'88888888 77770000 00000000 00000000'   v2
00002554  00000000 00000000
0000255C  88888888 77770000                        1807           DC    XL16'88888888 77770000 66666666 55555555'   v2
00002564  66666666 55555555
                                                   1808
                                                   1809           VRR_A VISTR,1,1,0
00002570                                           1810+          DS    0FD
00002570                         00002570          1811+          USING *,R5                base for test data and test routine
00002570  000025C8                                 1812+T32      DC    A(X32)              address of test routine
00002574  0020                                     1813+          DC    H'32'               test number
00002576  00                                       1814+          DC    X'00'
00002577  01                                       1815+          DC    HL1'1'                   M3 used
00002578  01                                       1816+          DC    HL1'1'                   M5 used
00002579  00                                       1817+          DC    HL1'0'              CC
0000257A  07                                       1818+          DC    HL1'7'              CC failed mask
0000257C  00000000 00000000                        1819+          DS    2F                  extracted PSW after test (has CC)
00002584  FF                                       1820+          DC    X'FF'               extracted CC, if test failed
00002585  E5C9E2E3 D9404040                       1821+          DC    CL8'VISTR'          instruction name
00002590  000025F4                                 1822+          DC    A(RE32)             address of v1 result
00002594  00002604                                 1823+          DC    A(RE32+16)          address of v2 source
00002598  00002614                                 1824+          DC    A(RE32+32)          address of v3 source
0000259C  00000010                                 1825+          DC    A(16)               result length
000025A0  000025F4                                 1826+REA32    DC    A(RE32)             result address
000025A8  00000000 00000000                        1827+          DS    FD                  gap
000025B0  00000000 00000000                        1828+V1O32    DS    XL16                V1 output
000025B8  00000000 00000000
000025C0  00000000 00000000                        1829+          DS    FD                  gap
                                                   1830+*
000025C8                                           1831+X32      DS    0F
000025C8  4110 8EF8                      000010F8  1832+          LA    R1,V1FUDGE         load v21 fudge
000025CC  E751 0000 0806                 00000000  1833+          VL    v21,0(R1)
000025D2  E310 5024 0014                 00000024  1834+          LGF   R1,V2ADDR           load v2 source
000025D8  E761 0000 0806                 00000000  1835+          VL    v22,0(R1)           use v21 to test decoder
000025DE  E756 0010 1C5C                           1836+          VISTR V21,V22,1,1                test instruction
000025E4  B98D 0020                                1837+          EPSW  R2,R0               extract psw
000025E8  5020 500C                      0000000C  1838+          ST    R2,CCPSW               to save CC
000025EC  E750 5040 080E                 000025B0  1839+          VST   V21,V1O32           save v1 output
000025F2  07FB                                     1840+          BR    R11                 return
000025F4                                           1841+RE32     DC    0F                  V1 for this test
000025F4                                           1842+          DROP  R5
000025F4  88888888 00000000                        1843           DC    XL16'88888888 00000000 00000000 00000000'   v2
000025FC  00000000 00000000
00002604  88888888 00007777                        1844           DC    XL16'88888888 00007777 66666666 55555555'   v2
0000260C  66666666 55555555
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1845
                                                    1846          VRR_A VISTR,1,1,0
00002618                                            1847+         DS    0FD
00002618                      00002618              1848+         USING *,R5              base for test data and test routine
00002618  00002670                                  1849+T33      DC    A(X33)            address of test routine
0000261C  0021                                      1850+         DC    H'33'             test number
0000261E  00                                        1851+         DC    X'00'
0000261F  01                                        1852+         DC    HL1'1'                 M3 used
00002620  01                                        1853+         DC    HL1'1'                 M5 used
00002621  00                                        1854+         DC    HL1'0'            CC
00002622  07                                        1855+         DC    HL1'7'            CC failed mask
00002624  00000000 00000000                         1856+         DS    2F                extracted PSW after test (has CC)
0000262C  FF                                        1857+         DC    X'FF'             extracted CC, if test failed
0000262D  E5C9E2E3 D9404040                         1858+         DC    CL8'VISTR'        instruction name
00002638  0000269C                                  1859+         DC    A(RE33)           address of v1 result
0000263C  000026AC                                  1860+         DC    A(RE33+16)        address of v2 source
00002640  000026BC                                  1861+         DC    A(RE33+32)        address of v3 source
00002644  00000010                                  1862+         DC    A(16)             result length
00002648  0000269C                                  1863+REA33    DC    A(RE33)           result address
00002650  00000000 00000000                         1864+         DS    FD                gap
00002658  00000000 00000000                         1865+V1O33    DS    XL16              V1 output
00002660  00000000 00000000
00002668  00000000 00000000                         1866+         DS    FD                gap
                                                    1867+*
00002670                                            1868+X33      DS    0F
00002670  4110 8EF8                       000010F8  1869+         LA    R1,V1FUDGE        load v21 fudge
00002674  E751 0000 0806                  00000000  1870+         VL    v21,0(R1)
0000267A  E310 5024 0014                  00000024  1871+         LGF   R1,V2ADDR         load v2 source
00002680  E761 0000 0806                  00000000  1872+         VL    v22,0(R1)         use v21 to test decoder
00002686  E756 0010 1C5C                            1873+         VISTR V21,V22,1,1               test instruction
0000268C  B98D 0020                                 1874+         EPSW  R2,R0             extract psw
00002690  5020 500C                       0000000C  1875+         ST    R2,CCPSW             to save CC
00002694  E750 5040 080E                  00002658  1876+         VST   V21,V1O33         save v1 output
0000269A  07FB                                      1877+         BR    R11               return
0000269C                                            1878+RE33     DC    0F                V1 for this test
0000269C                                            1879+         DROP  R5
0000269C  88880000 00000000                         1880          DC    XL16'88880000 00000000 00000000 00000000'   v2
000026A4  00000000 00000000
000026AC  88880000 77777777                         1881          DC    XL16'88880000 77777777 66666666 55555555'   v2
000026B4  66666666 55555555
                                                    1882
                                                    1883          VRR_A VISTR,1,1,0
000026C0                                            1884+         DS    0FD
000026C0                      000026C0              1885+         USING *,R5              base for test data and test routine
000026C0  00002718                                  1886+T34      DC    A(X34)            address of test routine
000026C4  0022                                      1887+         DC    H'34'             test number
000026C6  00                                        1888+         DC    X'00'
000026C7  01                                        1889+         DC    HL1'1'                 M3 used
000026C8  01                                        1890+         DC    HL1'1'                 M5 used
000026C9  00                                        1891+         DC    HL1'0'            CC
000026CA  07                                        1892+         DC    HL1'7'            CC failed mask
000026CC  00000000 00000000                         1893+         DS    2F                extracted PSW after test (has CC)
000026D4  FF                                        1894+         DC    X'FF'             extracted CC, if test failed
000026D5  E5C9E2E3 D9404040                         1895+         DC    CL8'VISTR'        instruction name
000026E0  00002744                                  1896+         DC    A(RE34)           address of v1 result
000026E4  00002754                                  1897+         DC    A(RE34+16)        address of v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000026E8  00002764                                1898+          DC    A(RE34+32)          address of v3 source
000026EC  00000010                                1899+          DC    A(16)               result length
000026F0  00002744                                1900+REA34     DC    A(RE34)             result address
000026F8  00000000 00000000                       1901+          DS    FD                  gap
00002700  00000000 00000000                       1902+V1O34     DS    XL16                V1 output
00002708  00000000 00000000
00002710  00000000 00000000                       1903+          DS    FD                  gap
                                                  1904+*
00002718                                          1905+X34       DS    0F
00002718  4110 8EF8                     000010F8  1906+          LA    R1,V1FUDGE        load v21 fudge
0000271C  E751 0000 0806                00000000  1907+          VL    v21,0(R1)
00002722  E310 5024 0014                00000024  1908+          LGF   R1,V2ADDR          load v2 source
00002728  E761 0000 0806                00000000  1909+          VL    v22,0(R1)          use v21 to test decoder
0000272E  E756 0010 1C5C                          1910+          VISTR V21,V22,1,1                test instruction
00002734  B98D 0020                               1911+          EPSW  R2,R0              extract psw
00002738  5020 500C                     0000000C  1912+          ST    R2,CCPSW              to save CC
0000273C  E750 5040 080E                00002700  1913+          VST   V21,V1O34          save v1 output
00002742  07FB                                    1914+          BR    R11                return
00002744                                          1915+RE34      DC    0F                 V1 for this test
00002744                                          1916+          DROP  R5
00002744  00000000 00000000                       1917           DC    XL16'00000000 00000000 00000000 00000000'   v2
0000274C  00000000 00000000
00002754  00008888 77777777                       1918           DC    XL16'00008888 77777777 66666666 55555555'   v2
0000275C  66666666 55555555
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   1920 *word
                                                   1921          VRR_A VISTR,2,1,3
00002768                                           1922+         DS    0FD
00002768                     00002768              1923+         USING *,R5              base for test data and test routine
00002768  000027C0                                 1924+T35      DC    A(X35)            address of test routine
0000276C  0023                                     1925+         DC    H'35'             test number
0000276E  00                                       1926+         DC    X'00'
0000276F  02                                       1927+         DC    HL1'2'                 M3 used
00002770  01                                       1928+         DC    HL1'1'                 M5 used
00002771  03                                       1929+         DC    HL1'3'            CC
00002772  0E                                       1930+         DC    HL1'14'           CC failed mask
00002774  00000000 00000000                        1931+         DS    2F                extracted PSW after test (has CC)
0000277C  FF                                       1932+         DC    X'FF'             extracted CC, if test failed
0000277D  E5C9E2E3 D9404040                        1933+         DC    CL8'VISTR'        instruction name
00002788  000027EC                                 1934+         DC    A(RE35)           address of v1 result
0000278C  000027FC                                 1935+         DC    A(RE35+16)        address of v2 source
00002790  0000280C                                 1936+         DC    A(RE35+32)        address of v3 source
00002794  00000010                                 1937+         DC    A(16)             result length
00002798  000027EC                                 1938+REA35    DC    A(RE35)           result address
000027A0  00000000 00000000                        1939+         DS    FD                gap
000027A8  00000000 00000000                        1940+V1O35    DS    XL16              V1 output
000027B0  00000000 00000000
000027B8  00000000 00000000                        1941+         DS    FD                gap
                                                   1942+*
000027C0                                           1943+X35      DS    0F
000027C0  4110 8EF8                     000010F8   1944+         LA    R1,V1FUDGE        load v21 fudge
000027C4  E751 0000 0806                00000000   1945+         VL    v21,0(R1)
000027CA  E310 5024 0014                00000024   1946+         LGF   R1,V2ADDR         load v2 source
000027D0  E761 0000 0806                00000000   1947+         VL    v22,0(R1)         use v21 to test decoder
000027D6  E756 0010 2C5C                           1948+         VISTR V21,V22,2,1               test instruction
000027DC  B98D 0020                                1949+         EPSW  R2,R0             extract psw
000027E0  5020 500C                     0000000C   1950+         ST    R2,CCPSW             to save CC
000027E4  E750 5040 080E                000027A8   1951+         VST   V21,V1O35         save v1 output
000027EA  07FB                                     1952+         BR    R11               return
000027EC                                           1953+RE35     DC    0F                V1 for this test
000027EC                                           1954+         DROP  R5
000027EC  AAAAAAAA BBBBBBBB                        1955          DC    XL16'AAAAAAAA BBBBBBBB CCCCCCCC DDDDDDDD'   v2
000027F4  CCCCCCCC DDDDDDDD
000027FC  AAAAAAAA BBBBBBBB                        1956          DC    XL16'AAAAAAAA BBBBBBBB CCCCCCCC DDDDDDDD'   v2
00002804  CCCCCCCC DDDDDDDD
                                                   1957
                                                   1958          VRR_A VISTR,2,1,0
00002810                                           1959+         DS    0FD
00002810                     00002810              1960+         USING *,R5              base for test data and test routine
00002810  00002868                                 1961+T36      DC    A(X36)            address of test routine
00002814  0024                                     1962+         DC    H'36'             test number
00002816  00                                       1963+         DC    X'00'
00002817  02                                       1964+         DC    HL1'2'                 M3 used
00002818  01                                       1965+         DC    HL1'1'                 M5 used
00002819  00                                       1966+         DC    HL1'0'            CC
0000281A  07                                       1967+         DC    HL1'7'            CC failed mask
0000281C  00000000 00000000                        1968+         DS    2F                extracted PSW after test (has CC)
00002824  FF                                       1969+         DC    X'FF'             extracted CC, if test failed
00002825  E5C9E2E3 D9404040                        1970+         DC    CL8'VISTR'        instruction name
00002830  00002894                                 1971+         DC    A(RE36)           address of v1 result
00002834  000028A4                                 1972+         DC    A(RE36+16)        address of v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002838  000028B4                          1973+          DC    A(RE36+32)          address of v3 source
0000283C  00000010                          1974+          DC    A(16)               result length
00002840  00002894                          1975+REA36     DC    A(RE36)             result address
00002848  00000000 00000000                 1976+          DS    FD                  gap
00002850  00000000 00000000                 1977+V1O36     DS    XL16                V1 output
00002858  00000000 00000000
00002860  00000000 00000000                 1978+          DS    FD                  gap
                                            1979+*
00002868                                    1980+X36       DS    0F
00002868  4110 8EF8                 000010F8 1981+          LA    R1,V1FUDGE        load v21 fudge
0000286C  E751 0000 0806            00000000 1982+          VL    v21,0(R1)
00002872  E310 5024 0014            00000024 1983+          LGF   R1,V2ADDR          load v2 source
00002878  E761 0000 0806            00000000 1984+          VL    v22,0(R1)          use v21 to test decoder
0000287E  E756 0010 2C5C                     1985+          VISTR V21,V22,2,1                test instruction
00002884  B98D 0020                          1986+          EPSW  R2,R0              extract psw
00002888  5020 500C                 0000000C 1987+          ST    R2,CCPSW              to save CC
0000288C  E750 5040 080E            00002850 1988+          VST   V21,V1O36          save v1 output
00002892  07FB                               1989+          BR    R11                return
00002894                                     1990+RE36      DC    0F                 V1 for this test
00002894                                     1991+          DROP  R5
00002894  AAAAAAAA BBBBBBBB                  1992           DC    XL16'AAAAAAAA BBBBBBBB CCCCCCCC 00000000'   v2
0000289C  CCCCCCCC 00000000
000028A4  AAAAAAAA BBBBBBBB                  1993           DC    XL16'AAAAAAAA BBBBBBBB CCCCCCCC 00000000'   v2
000028AC  CCCCCCCC 00000000
                                             1994
                                             1995            VRR_A VISTR,2,1,0
000028B8                                     1996+          DS    0FD
000028B8                    000028B8         1997+          USING *,R5               base for test data and test routine
000028B8  00002910                           1998+T37       DC    A(X37)             address of test routine
000028BC  0025                               1999+          DC    H'37'              test number
000028BE  00                                 2000+          DC    X'00'
000028BF  02                                 2001+          DC    HL1'2'                  M3 used
000028C0  01                                 2002+          DC    HL1'1'                  M5 used
000028C1  00                                 2003+          DC    HL1'0'             CC
000028C2  07                                 2004+          DC    HL1'7'             CC failed mask
000028C4  00000000 00000000                  2005+          DS    2F                 extracted PSW after test (has CC)
000028CC  FF                                 2006+          DC    X'FF'              extracted CC, if test failed
000028CD  E5C9E2E3 D9404040                  2007+          DC    CL8'VISTR'         instruction name
000028D8  0000293C                           2008+          DC    A(RE37)            address of v1 result
000028DC  0000294C                           2009+          DC    A(RE37+16)         address of v2 source
000028E0  0000295C                           2010+          DC    A(RE37+32)         address of v3 source
000028E4  00000010                           2011+          DC    A(16)              result length
000028E8  0000293C                           2012+REA37     DC    A(RE37)            result address
000028F0  00000000 00000000                  2013+          DS    FD                 gap
000028F8  00000000 00000000                  2014+V1O37     DS    XL16               V1 output
00002900  00000000 00000000
00002908  00000000 00000000                  2015+          DS    FD                 gap
                                             2016+*
00002910                                     2017+X37       DS    0F
00002910  4110 8EF8                 000010F8 2018+          LA    R1,V1FUDGE        load v21 fudge
00002914  E751 0000 0806            00000000 2019+          VL    v21,0(R1)
0000291A  E310 5024 0014            00000024 2020+          LGF   R1,V2ADDR          load v2 source
00002920  E761 0000 0806            00000000 2021+          VL    v22,0(R1)          use v21 to test decoder
00002926  E756 0010 2C5C                     2022+          VISTR V21,V22,2,1                test instruction
0000292C  B98D 0020                          2023+          EPSW  R2,R0              extract psw
00002930  5020 500C                 0000000C 2024+          ST    R2,CCPSW              to save CC
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002934  E750 5040 080E                 000028F8  2025+          VST   V21,V1O37           save v1 output
0000293A  07FB                                     2026+          BR    R11                 return
0000293C                                           2027+RE37      DC    0F                  V1 for this test
0000293C                                           2028+          DROP  R5
0000293C  AAAAAAAA BBBBBBBB                        2029           DC    XL16'AAAAAAAA BBBBBBBB 00000000 00000000'   v2
00002944  00000000 00000000
0000294C  AAAAAAAA BBBBBBBB                        2030           DC    XL16'AAAAAAAA BBBBBBBB 00000000 DDDDDDDD'   v2
00002954  00000000 DDDDDDDD
                                                   2031
                                                   2032           VRR_A VISTR,2,1,0
00002960                                           2033+          DS    0FD
00002960                    00002960               2034+          USING *,R5                base for test data and test routine
00002960  000029B8                                 2035+T38       DC    A(X38)              address of test routine
00002964  0026                                     2036+          DC    H'38'               test number
00002966  00                                       2037+          DC    X'00'
00002967  02                                       2038+          DC    HL1'2'                   M3 used
00002968  01                                       2039+          DC    HL1'1'                   M5 used
00002969  00                                       2040+          DC    HL1'0'              CC
0000296A  07                                       2041+          DC    HL1'7'              CC failed mask
0000296C  00000000 00000000                        2042+          DS    2F                  extracted PSW after test (has CC)
00002974  FF                                       2043+          DC    X'FF'               extracted CC, if test failed
00002975  E5C9E2E3 D9404040                        2044+          DC    CL8'VISTR'          instruction name
00002980  000029E4                                 2045+          DC    A(RE38)             address of v1 result
00002984  000029F4                                 2046+          DC    A(RE38+16)          address of v2 source
00002988  00002A04                                 2047+          DC    A(RE38+32)          address of v3 source
0000298C  00000010                                 2048+          DC    A(16)               result length
00002990  000029E4                                 2049+REA38     DC    A(RE38)             result address
00002998  00000000 00000000                        2050+          DS    FD                  gap
000029A0  00000000 00000000                        2051+V1O38     DS    XL16                V1 output
000029A8  00000000 00000000
000029B0  00000000 00000000                        2052+          DS    FD                  gap
                                                   2053+*
000029B8                                           2054+X38       DS    0F
000029B8  4110 8EF8                     000010F8   2055+          LA    R1,V1FUDGE        load v21 fudge
000029BC  E751 0000 0806                00000000   2056+          VL    v21,0(R1)
000029C2  E310 5024 0014                00000024   2057+          LGF   R1,V2ADDR           load v2 source
000029C8  E761 0000 0806                00000000   2058+          VL    v22,0(R1)           use v21 to test decoder
000029CE  E756 0010 2C5C                           2059+          VISTR V21,V22,2,1                 test instruction
000029D4  B98D 0020                                2060+          EPSW  R2,R0               extract psw
000029D8  5020 500C                     0000000C   2061+          ST    R2,CCPSW               to save CC
000029DC  E750 5040 080E                000029A0   2062+          VST   V21,V1O38           save v1 output
000029E2  07FB                                     2063+          BR    R11                 return
000029E4                                           2064+RE38      DC    0F                  V1 for this test
000029E4                                           2065+          DROP  R5
000029E4  AAAAAAAA 00000000                        2066           DC    XL16'AAAAAAAA 00000000 00000000 00000000'   v2
000029EC  00000000 00000000
000029F4  AAAAAAAA 00000000                        2067           DC    XL16'AAAAAAAA 00000000 CCCCCCCC DDDDDDDD'   v2
000029FC  CCCCCCCC DDDDDDDD
                                                   2068
                                                   2069           VRR_A VISTR,2,1,0
00002A08                                           2070+          DS    0FD
00002A08                    00002A08               2071+          USING *,R5                base for test data and test routine
00002A08  00002A60                                 2072+T39       DC    A(X39)              address of test routine
00002A0C  0027                                     2073+          DC    H'39'               test number
00002A0E  00                                       2074+          DC    X'00'
00002A0F  02                                       2075+          DC    HL1'2'                   M3 used
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002A10  01                                       2076+          DC    HL1'1'                 M5 used
00002A11  00                                       2077+          DC    HL1'0'              CC
00002A12  07                                       2078+          DC    HL1'7'              CC failed mask
00002A14  00000000 00000000                        2079+          DS    2F                  extracted PSW after test (has CC)
00002A1C  FF                                       2080+          DC    X'FF'               extracted CC, if test failed
00002A1D  E5C9E2E3 D9404040                        2081+          DC    CL8'VISTR'          instruction name
00002A28  00002A8C                                 2082+          DC    A(RE39)             address of v1 result
00002A2C  00002A9C                                 2083+          DC    A(RE39+16)          address of v2 source
00002A30  00002AAC                                 2084+          DC    A(RE39+32)          address of v3 source
00002A34  00000010                                 2085+          DC    A(16)               result length
00002A38  00002A8C                                 2086+REA39     DC    A(RE39)             result address
00002A40  00000000 00000000                        2087+          DS    FD                  gap
00002A48  00000000 00000000                        2088+V1O39     DS    XL16                V1 output
00002A50  00000000 00000000
00002A58  00000000 00000000                        2089+          DS    FD                  gap
                                                   2090+*
00002A60                                           2091+X39       DS    0F
00002A60  4110 8EF8                      000010F8  2092+          LA    R1,V1FUDGE        load v21 fudge
00002A64  E751 0000 0806                 00000000  2093+          VL    v21,0(R1)
00002A6A  E310 5024 0014                 00000024  2094+          LGF   R1,V2ADDR          load v2 source
00002A70  E761 0000 0806                 00000000  2095+          VL    v22,0(R1)          use v21 to test decoder
00002A76  E756 0010 2C5C                           2096+          VISTR V21,V22,2,1                test instruction
00002A7C  B98D 0020                                2097+          EPSW  R2,R0              extract psw
00002A80  5020 500C                      0000000C  2098+          ST    R2,CCPSW              to save CC
00002A84  E750 5040 080E                 00002A48  2099+          VST   V21,V1O39          save v1 output
00002A8A  07FB                                     2100+          BR    R11                return
00002A8C                                           2101+RE39      DC    0F                      V1 for this test
00002A8C                                           2102+          DROP  R5
00002A8C  00000000 00000000                        2103           DC    XL16'00000000 00000000 00000000 00000000'   v2
00002A94  00000000 00000000
00002A9C  00000000 BBBBBBBB                        2104           DC    XL16'00000000 BBBBBBBB CCCCCCCC DDDDDDDD'   v2
00002AA4  CCCCCCCC DDDDDDDD
                                                   2105
                                                   2106
                                                   2107
00002AAC  00000000                                 2108           DC    F'0'     END OF TABLE
00002AB0  00000000                                 2109           DC    F'0'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2111 *
                                                   2112 * table of pointers to individual tests
                                                   2113 *
00002AB4                                           2114 E7TESTS  DS    0F
                                                   2115          PTTABLE
00002AB4                                           2116+TTABLE   DS    0F
00002AB4  00001118                                 2117+         DC    A(T1)                    test address
00002AB8  000011C0                                 2118+         DC    A(T2)                    test address
00002ABC  00001268                                 2119+         DC    A(T3)                    test address
00002AC0  00001310                                 2120+         DC    A(T4)                    test address
00002AC4  000013B8                                 2121+         DC    A(T5)                    test address
00002AC8  00001460                                 2122+         DC    A(T6)                    test address
00002ACC  00001508                                 2123+         DC    A(T7)                    test address
00002AD0  000015B0                                 2124+         DC    A(T8)                    test address
00002AD4  00001658                                 2125+         DC    A(T9)                    test address
00002AD8  00001700                                 2126+         DC    A(T10)                   test address
00002ADC  000017A8                                 2127+         DC    A(T11)                   test address
00002AE0  00001850                                 2128+         DC    A(T12)                   test address
00002AE4  000018F8                                 2129+         DC    A(T13)                   test address
00002AE8  000019A0                                 2130+         DC    A(T14)                   test address
00002AEC  00001A48                                 2131+         DC    A(T15)                   test address
00002AF0  00001AF0                                 2132+         DC    A(T16)                   test address
00002AF4  00001B98                                 2133+         DC    A(T17)                   test address
00002AF8  00001C40                                 2134+         DC    A(T18)                   test address
00002AFC  00001CE8                                 2135+         DC    A(T19)                   test address
00002B00  00001D90                                 2136+         DC    A(T20)                   test address
00002B04  00001E38                                 2137+         DC    A(T21)                   test address
00002B08  00001EE0                                 2138+         DC    A(T22)                   test address
00002B0C  00001F88                                 2139+         DC    A(T23)                   test address
00002B10  00002030                                 2140+         DC    A(T24)                   test address
00002B14  000020D8                                 2141+         DC    A(T25)                   test address
00002B18  00002180                                 2142+         DC    A(T26)                   test address
00002B1C  00002228                                 2143+         DC    A(T27)                   test address
00002B20  000022D0                                 2144+         DC    A(T28)                   test address
00002B24  00002378                                 2145+         DC    A(T29)                   test address
00002B28  00002420                                 2146+         DC    A(T30)                   test address
00002B2C  000024C8                                 2147+         DC    A(T31)                   test address
00002B30  00002570                                 2148+         DC    A(T32)                   test address
00002B34  00002618                                 2149+         DC    A(T33)                   test address
00002B38  000026C0                                 2150+         DC    A(T34)                   test address
00002B3C  00002768                                 2151+         DC    A(T35)                   test address
00002B40  00002810                                 2152+         DC    A(T36)                   test address
00002B44  000028B8                                 2153+         DC    A(T37)                   test address
00002B48  00002960                                 2154+         DC    A(T38)                   test address
00002B4C  00002A08                                 2155+         DC    A(T39)                   test address
                                                   2156+*
00002B50  00000000                                 2157+         DC    A(0)                     end of table
00002B54  00000000                                 2158+         DC    A(0)                     end of table
                                                   2159
00002B58  00000000                                 2160          DC    F'0'     END OF TABLE
00002B5C  00000000                                 2161          DC    F'0'
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     2163 ********************************************************************************
                                                     2164 *        Register equates
                                                     2165 ********************************************************************************

                                00000000  00000001  2167 R0       EQU   0
                                00000001  00000001  2168 R1       EQU   1
                                00000002  00000001  2169 R2       EQU   2
                                00000003  00000001  2170 R3       EQU   3
                                00000004  00000001  2171 R4       EQU   4
                                00000005  00000001  2172 R5       EQU   5
                                00000006  00000001  2173 R6       EQU   6
                                00000007  00000001  2174 R7       EQU   7
                                00000008  00000001  2175 R8       EQU   8
                                00000009  00000001  2176 R9       EQU   9
                                0000000A  00000001  2177 R10      EQU   10
                                0000000B  00000001  2178 R11      EQU   11
                                0000000C  00000001  2179 R12      EQU   12
                                0000000D  00000001  2180 R13      EQU   13
                                0000000E  00000001  2181 R14      EQU   14
                                0000000F  00000001  2182 R15      EQU   15


                                                     2184 ********************************************************************************
                                                     2185 *        Register equates
                                                     2186 ********************************************************************************


                              00000000  00000001  2188 V0       EQU   0
                              00000001  00000001  2189 V1       EQU   1
                              00000002  00000001  2190 V2       EQU   2
                              00000003  00000001  2191 V3       EQU   3
                              00000004  00000001  2192 V4       EQU   4
                              00000005  00000001  2193 V5       EQU   5
                              00000006  00000001  2194 V6       EQU   6
                              00000007  00000001  2195 V7       EQU   7
                              00000008  00000001  2196 V8       EQU   8
                              00000009  00000001  2197 V9       EQU   9
                              0000000A  00000001  2198 V10      EQU   10
                              0000000B  00000001  2199 V11      EQU   11
                              0000000C  00000001  2200 V12      EQU   12
                              0000000D  00000001  2201 V13      EQU   13
                              0000000E  00000001  2202 V14      EQU   14
                              0000000F  00000001  2203 V15      EQU   15
                              00000010  00000001  2204 V16      EQU   16
                              00000011  00000001  2205 V17      EQU   17
                              00000012  00000001  2206 V18      EQU   18
                              00000013  00000001  2207 V19      EQU   19
                              00000014  00000001  2208 V20      EQU   20
                              00000015  00000001  2209 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001  2210 V22       EQU   22
                                00000017  00000001  2211 V23       EQU   23
                                00000018  00000001  2212 V24       EQU   24
                                00000019  00000001  2213 V25       EQU   25
                                0000001A  00000001  2214 V26       EQU   26
                                0000001B  00000001  2215 V27       EQU   27
                                0000001C  00000001  2216 V28       EQU   28
                                0000001D  00000001  2217 V29       EQU   29
                                0000001E  00000001  2218 V30       EQU   30
                                0000001F  00000001  2219 V31       EQU   31
                                                    2220
                                                    2221           END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	151	117 147 148 149
CC	U	00000009	1	512	262
CCFOUND	X	00000014	1	518	249 269
CCMASK	U	0000000A	1	513	219
CCMSG	U	0000031C	1	236	231
CCPRTEXP	C	00001098	1	477	266
CCPRTGOT	C	000010A8	1	480	273
CCPRTLINE	C	00001055	16	472	482 276
CCPRTLNG	U	00000055	1	482	275
CCPRTNAME	C	00001082	8	475	259
CCPRTNUM	C	00001065	3	473	257
CCPSW	F	0000000C	4	517	246 684 721 758 796 833 870 908 945 982 1023 1060 1097 1134 1171 1208 1245 1282 1319 1356 1393 1430 1467 1504 1541 1578 1616 1653 1690 1727 1764 1801 1838 1875 1912 1950 1987 2024 2061 2098
CTLR0	F	00000554	4	415	161 162 163 164
DECNUM	C	000010D6	16	492	254 256 263 265 270 272 292 294 301 303 308 310
E7TEST	4	00000000	88	506	210
E7TESTS	F	00002AB4	4	2114	203
EDIT	X	000010AA	18	487	255 264 271 293 302 309
ENDTEST	U	00000428	1	330	208
EOJ	I	00000538	4	405	196 333
EOJPSW	D	00000528	8	403	405
FAILCONT	U	00000418	1	320	
FAILED	F	00001000	4	445	280 322 331
FAILMSG	U	000003B0	1	290	226
FAILPSW	D	00000540	8	407	409
FAILTEST	I	00000550	4	409	334
FB0001	F	00000280	8	180	184 185 187
IMAGE	1	00000000	11104	0	
K	U	00000400	1	429	430 431 432
K64	U	00010000	1	431	
M3	U	00000007	1	510	300
M5	U	00000008	1	511	240 307
MB	U	00100000	1	432	
MSG	I	00000470	4	365	195 348
MSGCMD	C	000004BE	9	395	378 379
MSGMSG	C	000004C7	95	396	372 393 370
MSGMVC	I	000004B8	6	393	376
MSGOK	I	00000486	2	374	371
MSGRET	I	000004A6	4	389	382 385
MSGSAVE	F	000004AC	4	392	368 389
NEXTE7	U	000002D4	1	205	229 325
OPNAME	C	00000015	8	520	259 297
PAGE	U	00001000	1	430	
PRT3	C	000010C0	18	490	255 256 257 264 265 266 271 272 273 293 294 295 302 303 304 309 310 311
PRTLINE	C	00001008	16	454	464 314
PRTLNG	U	0000004D	1	464	313
PRTM3	C	00001044	3	459	304
PRTM5	C	00001051	3	462	311
PRTNAME	C	00001033	8	457	297
PRTNUM	C	00001018	3	455	295
R0	U	00000000	1	2167	111 161 164 184 186 187 188 193 212 213 275 279 280 313 321 322 347 349 365 368 370 372 374 389 683 720 757 795 832 869 907 944 981 1022 1059 1096 1133 1170 1207

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					1244 1281 1318 1355 1392 1429 1466 1503 1540 1577 1615 1652 1689
					1726 1763 1800 1837 1874 1911 1949 1986 2023 2060 2097
R1	U	00000001	1	2168	194 219 220 221 224 225 240 241 246 247 248 249 276
					314 331 332 379 393 678 679 680 681 715 716 717 718
					752 753 754 755 790 791 792 793 827 828 829 830 864
					865 866 867 902 903 904 905 939 940 941 942 976 977
					978 979 1017 1018 1019 1020 1054 1055 1056 1057 1091 1092 1093
					1094 1128 1129 1130 1131 1165 1166 1167 1168 1202 1203 1204 1205
					1239 1240 1241 1242 1276 1277 1278 1279 1313 1314 1315 1316 1350
					1351 1352 1353 1387 1388 1389 1390 1424 1425 1426 1427 1461 1462
					1463 1464 1498 1499 1500 1501 1535 1536 1537 1538 1572 1573 1574
					1575 1610 1611 1612 1613 1647 1648 1649 1650 1684 1685 1686 1687
					1721 1722 1723 1724 1758 1759 1760 1761 1795 1796 1797 1798 1832
					1833 1834 1835 1869 1870 1871 1872 1906 1907 1908 1909 1944 1945
					1946 1947 1981 1982 1983 1984 2018 2019 2020 2021 2055 2056 2057
					2058 2092 2093 2094 2095
R10	U	0000000A	1	2177	149 158 159
R11	U	0000000B	1	2178	216 217 686 723 760 798 835 872 910 947 984 1025 1062
					1099 1136 1173 1210 1247 1284 1321 1358 1395 1432 1469 1506 1543
					1580 1618 1655 1692 1729 1766 1803 1840 1877 1914 1952 1989 2026
					2063 2100
R12	U	0000000C	1	2179	203 206 228 324
R13	U	0000000D	1	2180	
R14	U	0000000E	1	2181	
R15	U	0000000F	1	2182	277 315 342 352 353
R2	U	00000002	1	2169	195 253 254 261 262 263 268 269 270 291 292 299 300
					301 306 307 308 347 348 349 366 368 374 375 376 378
					384 389 390 683 684 720 721 757 758 795 796 832 833
					869 870 907 908 944 945 981 982 1022 1023 1059 1060 1096
					1097 1133 1134 1170 1171 1207 1208 1244 1245 1281 1282 1318 1319
					1355 1356 1392 1393 1429 1430 1466 1467 1503 1504 1540 1541 1577
					1578 1615 1616 1652 1653 1689 1690 1726 1727 1763 1764 1800 1801
					1837 1838 1874 1875 1911 1912 1949 1950 1986 1987 2023 2024 2060
					2061 2097 2098
R3	U	00000003	1	2170	
R4	U	00000004	1	2171	
R5	U	00000005	1	2172	206 207 210 343 351 657 688 694 725 731 762 769 800
					806 837 843 874 881 912 918 949 955 986 996 1027 1033
					1064 1070 1101 1107 1138 1144 1175 1181 1212 1218 1249 1255 1286
					1292 1323 1329 1360 1366 1397 1403 1434 1440 1471 1477 1508 1514
					1545 1551 1582 1589 1620 1626 1657 1663 1694 1700 1731 1737 1768
					1774 1805 1811 1842 1848 1879 1885 1916 1923 1954 1960 1991 1997
					2028 2034 2065 2071 2102
R6	U	00000006	1	2173	
R7	U	00000007	1	2174	
R8	U	00000008	1	2175	147 151 152 153 155
R9	U	00000009	1	2176	148 155 156 158
RE1	F	0000119C	4	687	668 669 670 672
RE10	F	00001784	4	1026	1007 1008 1009 1011
RE11	F	0000182C	4	1063	1044 1045 1046 1048
RE12	F	000018D4	4	1100	1081 1082 1083 1085
RE13	F	0000197C	4	1137	1118 1119 1120 1122
RE14	F	00001A24	4	1174	1155 1156 1157 1159
RE15	F	00001ACC	4	1211	1192 1193 1194 1196
RE16	F	00001B74	4	1248	1229 1230 1231 1233
RE17	F	00001C1C	4	1285	1266 1267 1268 1270

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE18	F	00001CC4	4	1322	1303	1304	1305	1307
RE19	F	00001D6C	4	1359	1340	1341	1342	1344
RE2	F	00001244	4	724	705	706	707	709
RE20	F	00001E14	4	1396	1377	1378	1379	1381
RE21	F	00001EBC	4	1433	1414	1415	1416	1418
RE22	F	00001F64	4	1470	1451	1452	1453	1455
RE23	F	0000200C	4	1507	1488	1489	1490	1492
RE24	F	000020B4	4	1544	1525	1526	1527	1529
RE25	F	0000215C	4	1581	1562	1563	1564	1566
RE26	F	00002204	4	1619	1600	1601	1602	1604
RE27	F	000022AC	4	1656	1637	1638	1639	1641
RE28	F	00002354	4	1693	1674	1675	1676	1678
RE29	F	000023FC	4	1730	1711	1712	1713	1715
RE3	F	000012EC	4	761	742	743	744	746
RE30	F	000024A4	4	1767	1748	1749	1750	1752
RE31	F	0000254C	4	1804	1785	1786	1787	1789
RE32	F	000025F4	4	1841	1822	1823	1824	1826
RE33	F	0000269C	4	1878	1859	1860	1861	1863
RE34	F	00002744	4	1915	1896	1897	1898	1900
RE35	F	000027EC	4	1953	1934	1935	1936	1938
RE36	F	00002894	4	1990	1971	1972	1973	1975
RE37	F	0000293C	4	2027	2008	2009	2010	2012
RE38	F	000029E4	4	2064	2045	2046	2047	2049
RE39	F	00002A8C	4	2101	2082	2083	2084	2086
RE4	F	00001394	4	799	780	781	782	784
RE5	F	0000143C	4	836	817	818	819	821
RE6	F	000014E4	4	873	854	855	856	858
RE7	F	0000158C	4	911	892	893	894	896
RE8	F	00001634	4	948	929	930	931	933
RE9	F	000016DC	4	985	966	967	968	970
REA1	A	00001148	4	672				
REA10	A	00001730	4	1011				
REA11	A	000017D8	4	1048				
REA12	A	00001880	4	1085				
REA13	A	00001928	4	1122				
REA14	A	000019D0	4	1159				
REA15	A	00001A78	4	1196				
REA16	A	00001B20	4	1233				
REA17	A	00001BC8	4	1270				
REA18	A	00001C70	4	1307				
REA19	A	00001D18	4	1344				
REA2	A	000011F0	4	709				
REA20	A	00001DC0	4	1381				
REA21	A	00001E68	4	1418				
REA22	A	00001F10	4	1455				
REA23	A	00001FB8	4	1492				
REA24	A	00002060	4	1529				
REA25	A	00002108	4	1566				
REA26	A	000021B0	4	1604				
REA27	A	00002258	4	1641				
REA28	A	00002300	4	1678				
REA29	A	000023A8	4	1715				
REA3	A	00001298	4	746				
REA30	A	00002450	4	1752				
REA31	A	000024F8	4	1789				
REA32	A	000025A0	4	1826				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA33	A	00002648	4	1863		
REA34	A	000026F0	4	1900		
REA35	A	00002798	4	1938		
REA36	A	00002840	4	1975		
REA37	A	000028E8	4	2012		
REA38	A	00002990	4	2049		
REA39	A	00002A38	4	2086		
REA4	A	00001340	4	784		
REA5	A	000013E8	4	821		
REA6	A	00001490	4	858		
REA7	A	00001538	4	896		
REA8	A	000015E0	4	933		
REA9	A	00001688	4	970		
READDR	A	00000030	4	525	224	
REG2LOW	U	000000DD	1	435		
REG2PATT	U	AABBCCDD	1	434		
RELEN	A	0000002C	4	524		
RPTDWSAV	D	00000460	8	358	347	349
RPTERROR	I	00000436	4	342	277	315
RPTSAVE	F	00000454	4	355	342	352
RPTSVR5	F	00000458	4	356	343	351
SKL0001	U	0000004E	1	177	193	
SKT0001	C	0000022A	20	174	177	194
SVOLDPSW	U	00000140	0	113		
T1	A	00001118	4	658	2117	
T10	A	00001700	4	997	2126	
T11	A	000017A8	4	1034	2127	
T12	A	00001850	4	1071	2128	
T13	A	000018F8	4	1108	2129	
T14	A	000019A0	4	1145	2130	
T15	A	00001A48	4	1182	2131	
T16	A	00001AF0	4	1219	2132	
T17	A	00001B98	4	1256	2133	
T18	A	00001C40	4	1293	2134	
T19	A	00001CE8	4	1330	2135	
T2	A	000011C0	4	695	2118	
T20	A	00001D90	4	1367	2136	
T21	A	00001E38	4	1404	2137	
T22	A	00001EE0	4	1441	2138	
T23	A	00001F88	4	1478	2139	
T24	A	00002030	4	1515	2140	
T25	A	000020D8	4	1552	2141	
T26	A	00002180	4	1590	2142	
T27	A	00002228	4	1627	2143	
T28	A	000022D0	4	1664	2144	
T29	A	00002378	4	1701	2145	
T3	A	00001268	4	732	2119	
T30	A	00002420	4	1738	2146	
T31	A	000024C8	4	1775	2147	
T32	A	00002570	4	1812	2148	
T33	A	00002618	4	1849	2149	
T34	A	000026C0	4	1886	2150	
T35	A	00002768	4	1924	2151	
T36	A	00002810	4	1961	2152	
T37	A	000028B8	4	1998	2153	
T38	A	00002960	4	2035	2154	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T39	A	00002A08	4	2072	2155
T4	A	00001310	4	770	2120
T5	A	000013B8	4	807	2121
T6	A	00001460	4	844	2122
T7	A	00001508	4	882	2123
T8	A	000015B0	4	919	2124
T9	A	00001658	4	956	2125
TESTCC	I	00000318	4	231	221
TESTING	F	00001004	4	446	213
TESTREST	U	00000300	1	223	242 282
TNUM	H	00000004	2	508	212 253 291
TSUB	A	00000000	4	507	216
TTABLE	F	00002AB4	4	2116	
V0	U	00000000	1	2188	
V1	U	00000001	1	2189	
V10	U	0000000A	1	2198	
V11	U	0000000B	1	2199	
V12	U	0000000C	1	2200	
V13	U	0000000D	1	2201	
V14	U	0000000E	1	2202	
V15	U	0000000F	1	2203	
V16	U	00000010	1	2204	
V17	U	00000011	1	2205	
V18	U	00000012	1	2206	
V19	U	00000013	1	2207	
V1ADDR	A	00000020	4	521	
V1FUDGE	X	000010F8	16	499	215 678 715 752 790 827 864 902 939 976 1017 1054 1091 1128 1165 1202 1239 1276 1313 1350 1387 1424 1461 1498 1535 1572 1610 1647 1684 1721 1758 1795 1832 1869 1906 1944 1981 2018 2055 2092
V1O1	X	00001158	16	674	685
V1O10	X	00001740	16	1013	1024
V1O11	X	000017E8	16	1050	1061
V1O12	X	00001890	16	1087	1098
V1O13	X	00001938	16	1124	1135
V1O14	X	000019E0	16	1161	1172
V1O15	X	00001A88	16	1198	1209
V1O16	X	00001B30	16	1235	1246
V1O17	X	00001BD8	16	1272	1283
V1O18	X	00001C80	16	1309	1320
V1O19	X	00001D28	16	1346	1357
V1O2	X	00001200	16	711	722
V1O20	X	00001DD0	16	1383	1394
V1O21	X	00001E78	16	1420	1431
V1O22	X	00001F20	16	1457	1468
V1O23	X	00001FC8	16	1494	1505
V1O24	X	00002070	16	1531	1542
V1O25	X	00002118	16	1568	1579
V1O26	X	000021C0	16	1606	1617
V1O27	X	00002268	16	1643	1654
V1O28	X	00002310	16	1680	1691
V1O29	X	000023B8	16	1717	1728
V1O3	X	000012A8	16	748	759
V1O30	X	00002460	16	1754	1765
V1O31	X	00002508	16	1791	1802
V1O32	X	000025B0	16	1828	1839

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1033	X	00002658	16	1865	1876
V1034	X	00002700	16	1902	1913
V1035	X	000027A8	16	1940	1951
V1036	X	00002850	16	1977	1988
V1037	X	000028F8	16	2014	2025
V1038	X	000029A0	16	2051	2062
V1039	X	00002A48	16	2088	2099
V104	X	00001350	16	786	797
V105	X	000013F8	16	823	834
V106	X	000014A0	16	860	871
V107	X	00001548	16	898	909
V108	X	000015F0	16	935	946
V109	X	00001698	16	972	983
V10OUTPUT	X	00000040	16	527	225
V2	U	00000002	1	2190	
V20	U	00000014	1	2208	
V21	U	00000015	1	2209	679 682 685 716 719 722 753 756 759 791 794 797 828 831 834 865 868 871 903 906 909 940 943 946 977 980 983 1018 1021 1024 1055 1058 1061 1092 1095 1098 1129 1132 1135 1166 1169 1172 1203 1206 1209 1240 1243 1246 1277 1280 1283 1314 1317 1320 1351 1354 1357 1388 1391 1394 1425 1428 1431 1462 1465 1468 1499 1502 1505 1536 1539 1542 1573 1576 1579 1611 1614 1617 1648 1651 1654 1685 1688 1691 1722 1725 1728 1759 1762 1765 1796 1799 1802 1833 1836 1839 1870 1873 1876 1907 1910 1913 1945 1948 1951 1982 1985 1988 2019 2022 2025 2056 2059 2062 2093 2096 2099
V22	U	00000016	1	2210	215 681 682 718 719 755 756 793 794 830 831 867 868 905 906 942 943 979 980 1020 1021 1057 1058 1094 1095 1131 1132 1168 1169 1205 1206 1242 1243 1279 1280 1316 1317 1353 1354 1390 1391 1427 1428 1464 1465 1501 1502 1538 1539 1575 1576 1613 1614 1650 1651 1687 1688 1724 1725 1761 1762 1798 1799 1835 1836 1872 1873 1909 1910 1947 1948 1984 1985 2021 2022 2058 2059 2095 2096
V23	U	00000017	1	2211	
V24	U	00000018	1	2212	
V25	U	00000019	1	2213	
V26	U	0000001A	1	2214	
V27	U	0000001B	1	2215	
V28	U	0000001C	1	2216	
V29	U	0000001D	1	2217	
V2ADDR	A	00000024	4	522	680 717 754 792 829 866 904 941 978 1019 1056 1093 1130 1167 1204 1241 1278 1315 1352 1389 1426 1463 1500 1537 1574 1612 1649 1686 1723 1760 1797 1834 1871 1908 1946 1983 2020 2057 2094
V3	U	00000003	1	2191	
V30	U	0000001E	1	2218	
V31	U	0000001F	1	2219	
V3ADDR	A	00000028	4	523	
V4	U	00000004	1	2192	
V5	U	00000005	1	2193	
V6	U	00000006	1	2194	
V7	U	00000007	1	2195	
V8	U	00000008	1	2196	
V9	U	00000009	1	2197	
X0001	U	000002A8	1	183	171 184
X1	F	00001170	4	677	658
X10	F	00001758	4	1016	997
X11	F	00001800	4	1053	1034

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X12	F	000018A8	4	1090	1071
X13	F	00001950	4	1127	1108
X14	F	000019F8	4	1164	1145
X15	F	00001AA0	4	1201	1182
X16	F	00001B48	4	1238	1219
X17	F	00001BF0	4	1275	1256
X18	F	00001C98	4	1312	1293
X19	F	00001D40	4	1349	1330
X2	F	00001218	4	714	695
X20	F	00001DE8	4	1386	1367
X21	F	00001E90	4	1423	1404
X22	F	00001F38	4	1460	1441
X23	F	00001FE0	4	1497	1478
X24	F	00002088	4	1534	1515
X25	F	00002130	4	1571	1552
X26	F	000021D8	4	1609	1590
X27	F	00002280	4	1646	1627
X28	F	00002328	4	1683	1664
X29	F	000023D0	4	1720	1701
X3	F	000012C0	4	751	732
X30	F	00002478	4	1757	1738
X31	F	00002520	4	1794	1775
X32	F	000025C8	4	1831	1812
X33	F	00002670	4	1868	1849
X34	F	00002718	4	1905	1886
X35	F	000027C0	4	1943	1924
X36	F	00002868	4	1980	1961
X37	F	00002910	4	2017	1998
X38	F	000029B8	4	2054	2035
X39	F	00002A60	4	2091	2072
X4	F	00001368	4	789	770
X5	F	00001410	4	826	807
X6	F	000014B8	4	863	844
X7	F	00001560	4	901	882
X8	F	00001608	4	938	919
X9	F	000016B0	4	975	956
XC0001	U	000002D0	1	197	189
ZVE7TST	J	00000000	11104	110	113 115 119 123 444 111
=A(E7TESTS)	A	0000056C	4	421	203
=AL2(L'MSGMSG)	R	0000057A	2	425	370
=D'1'	D	00000560	8	419	241
=F'1'	F	00000574	4	423	279 321
=F'64'	F	00000568	4	420	188
=H'0'	H	00000578	2	424	365
=XL4'3'	X	00000570	4	422	248

```
 MACRO    DEFN  REFERENCES

FCHECK     63    170
PTTABLE   611   2115
VRR_A     546    655    692    729    767    804    841    879    916    953    994   1031   1068   1105   1142   1179   1216   1253
               1290   1327   1364   1401   1438   1475   1512   1549   1587   1624   1661   1698   1735   1772   1809   1846   1883
               1921   1958   1995   2032   2069
```

```
   DESC      SYMBOL    SIZE      POS         ADDR

Entry: 0

Image       IMAGE     11104  0000-2B5F  0000-2B5F
  Region              11104  0000-2B5F  0000-2B5F
    CSECT   ZVE7TST   11104  0000-2B5F  0000-2B5F
```

```
   STMT                          FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e7-08-VISTR.asm

** NO ERRORS FOUND **
```