

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 *     Zvector E7 instruction tests for VRR-b encoded:
				5 *
				6 *     E795 VPKLS   - Vector Pack Logical Saturate
				7 *     E797 VPKS    - Vector Pack Saturate
				8 *     E7F8 VCEQ    - Vector Compare Equal
				9 *     E7F9 VCHL    - Vector Compare High Logical
				10 *    E7FB VCH     - Vector Compare High
				11 *
				12 *           James Wekel March 2025
				13 *****
				15 *****
				16 *
				17 *           basic instruction tests
				18 *
				19 *****
				20 *     This program tests proper functioning of the z/arch E7 VRR-b
				21 *     Pack Logical Saturate, Pack Saturate, Compare, Compare Equal,
				22 *     Compare High Logical instructions.
				23 *     Exceptions are not tested.
				24 *
				25 *     PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				26 *     obvious coding errors. None of the tests are thorough. They are
				27 *     NOT designed to test all aspects of any of the instructions.
				28 *
				29 *****
				30 *
				31 *     *Testcase zvector-e7-16-PackCompare
				32 *     *
				33 *     *     Zvector E7 instruction tests for VRR-b encoded:
				34 *     *
				35 *     *     E795 VPKLS   - Vector Pack Logical Saturate
				36 *     *     E797 VPKS    - Vector Pack Saturate
				37 *     *     E7F8 VCEQ    - Vector Compare Equal
				38 *     *     E7F9 VCHL    - Vector Compare High Logical
				39 *     *     E7FB VCH     - Vector Compare High
				40 *     *
				41 *     *     # -----
				42 *     *     #     This tests only the basic function of the instruction.
				43 *     *     #     Exceptions are NOT tested.
				44 *     *     # -----
				45 *     *
				46 *     main size     2
				47 *     numcpu       1
				48 *     sysclear
				49 *     archlvl      z/Arch
				50 *     *
				51 *     loadcore     "\$(testpath)/zvector-e7-16-PackCompare.core" 0x0
				52 *     *
				53 *     diag8cmd    enable    # (needed for messages to Hercules console)
				54 *     runtest     5
				55 *     diag8cmd    disable   # (reset back to default)
				56 *     *

	<b>57</b>	*	<b>*Done</b>
	<b>58</b>	*	
	<b>59</b>	*	
	<b>60</b>	* * * * *	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
62				*****
63				* FCHECK Macro - Is a Facility Bit set?
64				*
65				* If the facility bit is NOT set, an message is issued and
66				* the test is skipped.
67				*
68				* Fcheck uses R0, R1 and R2
69				*
70				* eg. FCHECK 134, 'vector-packed-decimal'
71				*****
72				MACRO
73				FCHECK &BITNO, &NOTSETMSG
74	.	*		&BITNO : facility bit number to check
75	.	*		&NOTSETMSG : 'facility name'
76				LCLA &FBBYTE Facility bit in Byte
77				LCLA &FBBIT Facility bit within Byte
78				
79				LCLA &L(8)
80	&L(1)			SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
81				
82	&FBBYTE	SETA	&BITNO/8	
83	&FBBIT	SETA	&L((&BITNO-(&FBBYTE*8))+1)	
84	.	*	MNOTE	0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
85				
86			B	X&SYSNDX
87	*			Fcheck data area
88	*			skip messgae
89	SKT&SYSNDX DC	C'		Skipping tests: '
90		DC		C&NOTSETMSG
91		DC		C' (bit &BITNO) is not installed.'
92	SKL&SYSNDX EQU	*		- SKT&SYSNDX
93	*			facility bits
94		DS	FD	gap
95	FB&SYSNDX DS		4FD	
96		DS	FD	gap
97	*			
98	X&SYSNDX EQU	*		
99		LA		R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
100		STFLE		FB&SYSNDX get facility bits
101				
102		XGR		R0, R0
103		IC		R0, FB&SYSNDX+&FBBYTE get fbit byte
104		N		R0, =F' &FBBIT' is bit set?
105		BNZ		XC&SYSNDX
106	*			
107	*			facility bit not set, issue message and exit
108	*			
109		LA		R0, SKL&SYSNDX message length
110		LA		R1, SKT&SYSNDX message address
111		BAL		R2, MSG
112				
113		B		EOJ
114	XC&SYSNDX EQU	*		
115				MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				117	*****
				118	* Low core PSWs
				119	*****
00000000		00000000	00009D6F	120	ZVE7TST START 0
		00000000		121	USING ZVE7TST, R0 Low core addressability
		00000140	00000000	122	
				123	SVOLDPSW EQU ZVE7TST+X' 140' z/Arch Supervisor call old PSW
00000000		00000000	000001A0	125	ORG ZVE7TST+X' 1A0' z/Architecture RESTART PSW
000001A0	00000001 80000000			126	DC X' 0000000180000000'
000001A8	00000000 00000200			127	DC AD(BEGIN)
000001B0		000001B0	000001D0	129	ORG ZVE7TST+X' 1D0' z/Architecture PROGRAM CHECK PSW
000001D0	00020001 80000000			130	DC X' 0002000180000000'
000001D8	00000000 0000DEAD			131	DC AD(X' DEAD')
000001E0		000001E0	00000200	133	ORG ZVE7TST+X' 200' Start of actual test program..
				135	*****
				136	* The actual "ZVE7TST" program itself...
				137	*****
				138	*
				139	* Architecture Mode: z/Arch
				140	* Register Usage:
				141	*
				142	* R0 (work)
				143	* R1- 4 (work)
				144	* R5 Testing control table - current test base
				145	* R6- R7 (work)
				146	* R8 First base register
				147	* R9 Second base register
				148	* R10 Third base register
				149	* R11 E7TEST call return
				150	* R12 E7TESTS register
				151	* R13 (work)
				152	* R14 Subroutine call
				153	* R15 Secondary Subroutine call or work
				154	*
				155	*****
00000200		00000200		157	USING BEGIN, R8 FIRST Base Register
00000200		00001200		158	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		159	USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			161	BEGIN BALR R8, 0 Inititalize FIRST base register
00000202	0680			162	BCTR R8, 0 Inititalize FIRST base register
00000204	0680			163	BCTR R8, 0 Inititalize FIRST base register
00000206	4190 8800		00000800	165	LA R9, 2048(, R8) Inititalize SECOND base register
0000020A	4190 9800		00000800	166	LA R9, 2048(, R9) Inititalize SECOND base register
				167	





LOC	OBJECT CODE			ADDR1	ADDR2	STMT	
						243	*****
						244	* cc was not as expected
						245	*****
				0000031C	00000001	246	CCMSG EQU *
						247	*
						248	* is CS set by test?
						249	*
0000031C	E310	5008	0076		00000008	250	LB R1, M5 Get M5
00000322	E310	8360	0080		00000560	251	NG R1, =D' 1' isolate CS
00000328	4780	8100			00000300	252	BZ TESTREST not set?
						253	*
						254	* extract CC from extracted PSW
						255	*
0000032C	5810	500C			0000000C	256	L R1, CCPSW
00000330	8810	000C			0000000C	257	SRL R1, 12
00000334	5410	8370			00000570	258	N R1, =XL4' 3'
00000338	4210	5014			00000014	259	STC R1, CCFOUND save cc
						260	*
						261	* FILL IN MESSAGE
						262	*
0000033C	4820	5004			00000004	263	LH R2, TNUM get test number and convert
00000340	4E20	8ED6			000010D6	264	CVD R2, DECNUM
00000344	D211	8EC0	8EAA	000010C0	000010AA	265	MVC PRT3, EDIT
0000034A	DE11	8EC0	8ED6	000010C0	000010D6	266	ED PRT3, DECNUM
00000350	D202	8E65	8ECD	00001065	000010CD	267	MVC CCPRTNUM(3), PRT3+13 fill in message with test #
						268	
00000356	D207	8E82	5015	00001082	00000015	269	MVC CCPRTNAME, OPNAME fill in message with instruction
						270	
0000035C	B982	0022				271	XGR R2, R2 get CC as U8
00000360	4320	5009			00000009	272	IC R2, CC
00000364	4E20	8ED6			000010D6	273	CVD R2, DECNUM and convert
00000368	D211	8EC0	8EAA	000010C0	000010AA	274	MVC PRT3, EDIT
0000036E	DE11	8EC0	8ED6	000010C0	000010D6	275	ED PRT3, DECNUM
00000374	D200	8E98	8ECF	00001098	000010CF	276	MVC CCPRTEXP(1), PRT3+15 fill in message with CC field
						277	
0000037A	B982	0022				278	XGR R2, R2 get CCFOUND as U8
0000037E	4320	5014			00000014	279	IC R2, CCFOUND
00000382	4E20	8ED6			000010D6	280	CVD R2, DECNUM and convert
00000386	D211	8EC0	8EAA	000010C0	000010AA	281	MVC PRT3, EDIT
0000038C	DE11	8EC0	8ED6	000010C0	000010D6	282	ED PRT3, DECNUM
00000392	D200	8EA8	8ECF	000010A8	000010CF	283	MVC CCPRTGOT(1), PRT3+15 fill in message with ccfound
						284	
00000398	4100	0055			00000055	285	LA R0, CCPRTLNG message length
0000039C	4110	8E55			00001055	286	LA R1, CCPRTLNE messagfe address
000003A0	45F0	8236			00000436	287	BAL R15, RPTERROR
						288	
000003A4	5800	8374			00000574	289	L R0, =F' 1' set failed test indicator
000003A8	5000	8E00			00001000	290	ST R0, FAILED
						291	
000003AC	47F0	8100			00000300	292	B TESTREST
						293	



LOC	OBJECT	CODE	ADDR1	ADDR2	STMT	
					295	*****
					296	* result not as expected:
					297	* issue message with test number, instruction under test
					298	* and instruction m4, m5
					299	*****
			000003B0	00000001	300	FAILMSG EQU *
000003B0	4820	5004		00000004	301	LH R2, TNUM get test number and convert
000003B4	4E20	8ED6		000010D6	302	CVD R2, DECNUM
000003B8	D211	8EC0 8EAA	000010C0	000010AA	303	MVC PRT3, EDIT
000003BE	DE11	8EC0 8ED6	000010C0	000010D6	304	ED PRT3, DECNUM
000003C4	D202	8E18 8ECD	00001018	000010CD	305	MVC PRTNUM(3), PRT3+13 fill in message with test #
					306	
000003CA	D207	8E33 5015	00001033	00000015	307	MVC PRTNAME, OPNAME fill in message with instruction
					308	
000003D0	B982	0022			309	XGR R2, R2 get M4 as U8
000003D4	4320	5007		00000007	310	IC R2, M4
000003D8	4E20	8ED6		000010D6	311	CVD R2, DECNUM and convert
000003DC	D211	8EC0 8EAA	000010C0	000010AA	312	MVC PRT3, EDIT
000003E2	DE11	8EC0 8ED6	000010C0	000010D6	313	ED PRT3, DECNUM
000003E8	D202	8E44 8ECD	00001044	000010CD	314	MVC PRTM4(3), PRT3+13 fill in message with M4 field
					315	
000003EE	B982	0022			316	XGR R2, R2 get M5 as U8
000003F2	4320	5008		00000008	317	IC R2, M5
000003F6	4E20	8ED6		000010D6	318	CVD R2, DECNUM and convert
000003FA	D211	8EC0 8EAA	000010C0	000010AA	319	MVC PRT3, EDIT
00000400	DE11	8EC0 8ED6	000010C0	000010D6	320	ED PRT3, DECNUM
00000406	D202	8E51 8ECD	00001051	000010CD	321	MVC PRTM5(3), PRT3+13 fill in message with M5 field
					322	
0000040C	4100	004D		0000004D	323	LA R0, PRTLNG message length
00000410	4110	8E08		00001008	324	LA R1, PRTLNE messagfe address
00000414	45F0	8236		00000436	325	BAL R15, RPTERROR
					327	*****
					328	* continue after a failed test
					329	*****
			00000418	00000001	330	FAILCONT EQU *
00000418	5800	8374		00000574	331	L R0, =F' 1' set failed test indicator
0000041C	5000	8E00		00001000	332	ST R0, FAILED
					333	
00000420	41C0	C004		00000004	334	LA R12, 4(0, R12) next test address
00000424	47F0	80D4		000002D4	335	B NEXTE7
					337	*****
					338	* end of testing; set ending psr
					339	*****
			00000428	00000001	340	ENDTEST EQU *
00000428	5810	8E00		00001000	341	L R1, FAILED did a test fail?
0000042C	1211				342	LTR R1, R1
0000042E	4780	8338		00000538	343	BZ EOJ No, exit
00000432	47F0	8350		00000550	344	B FAILTEST Yes, exit with BAD PSW



LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				346	*****			
				347	*	RPTERROR	Report instruction test in error	
				348	*		R0 = MESSGAE LENGTH	
				349	*		R1 = ADDRESS OF MESSAGE	
				350	*****			
00000436	50F0 8254		00000454	352	RPTERROR	ST	R15, RPTSAVE	Save return address
0000043A	5050 8258		00000458	353		ST	R5, RPTSVR5	Save R5
				354	*			
				355	*	Use Hercules Diagnose for Message to console		
				356	*			
0000043E	9002 8260		00000460	357		STM	R0, R2, RPTDWSAV	save regs used by MSG
00000442	4520 8270		00000470	358		BAL	R2, MSG	call Hercules console MSG display
00000446	9802 8260		00000460	359		LM	R0, R2, RPTDWSAV	restore regs
0000044A	5850 8258		00000458	361		L	R5, RPTSVR5	Restore R5
0000044E	58F0 8254		00000454	362		L	R15, RPTSAVE	Restore return address
00000452	07FF			363		BR	R15	Return to caller
00000454	00000000			365	RPTSAVE	DC	F' 0'	R15 save area
00000458	00000000			366	RPTSVR5	DC	F' 0'	R5 save area
00000460	00000000 00000000			368	RPTDWSAV	DC	2D' 0'	R0-R2 save area for MSG call
				370	*****			
				371	*	Issue HERCULES MESSAGE pointed to by R1, length in R0		
				372	*	R2 = return address		
				373	*****			
00000470	4900 8378		00000578	375	MSG	CH	R0, =H' 0'	Do we even HAVE a message?
00000474	07D2			376		BNHR	R2	No, ignore
00000476	9002 82AC		000004AC	378		STM	R0, R2, MSGSAVE	Save registers
0000047A	4900 837A		0000057A	380		CH	R0, =AL2(L' MSGMSG)	Message length within limits?
0000047E	47D0 8286		00000486	381		BNH	MSGOK	Yes, continue
00000482	4100 005F		0000005F	382		LA	R0, L' MSGMSG	No, set to maximum
00000486	1820			384	MSGOK	LR	R2, R0	Copy length to work register
00000488	0620			385		BCTR	R2, 0	Minus-1 for execute
0000048A	4420 82B8		000004B8	386		EX	R2, MSGMVC	Copy message to O/P buffer
0000048E	4120 200A		0000000A	388		LA	R2, 1+L' MSGCMD(, R2)	Calculate true command length
00000492	4110 82BE		000004BE	389		LA	R1, MSGCMD	Point to true command
00000496	83120008			391		DC	X' 83' , X' 12' , X' 0008'	Issue Hercules Diagnose X' 008'
0000049A	4780 82A6		000004A6	392		BZ	MSGRET	Return if successful
				393				
0000049E	1222			394		LTR	R2, R2	Is Diag8 Ry (R2) 0?
000004A0	4780 82A6		000004A6	395		BZ	MSGRET	an error occurred but coninue
				396				
000004A4	0000			397		DC	H' 0'	CRASH for debugging purposes
000004A6	9802 82AC		000004AC	399	MSGRET	LM	R0, R2, MSGSAVE	Restore registers



LOC	OBJECT	CODE	ADDR1	ADDR2	STMT	
					409	*****
					410	* Normal completion or Abnormal termination PSWs
					411	*****
00000528	00020001	80000000			413	E0JPSW DC OD' 0' , X' 0002000180000000' , AD(0)
00000538	B2B2	8328		00000528	415	E0J LPSWE E0JPSW Normal completion
00000540	00020001	80000000			417	FAILPSW DC OD' 0' , X' 0002000180000000' , AD(X' BAD' )
00000550	B2B2	8340		00000540	419	FAILTEST LPSWE FAILPSW Abnormal termination
					421	*****
					422	* Working Storage
					423	*****
00000554	00000000				425	CTLRO DS F CRO
00000558	00000000				426	DS F
00000560					428	LTORG , Literals pool
00000560	00000000	00000001			429	=D' 1'
00000568	00000040				430	=F' 64'
0000056C	00009AA0				431	=A(E7TESTS)
00000570	00000003				432	=XL4' 3'
00000574	00000001				433	=F' 1'
00000578	0000				434	=H' 0'
0000057A	005F				435	=AL2(L' MSGMSG)
					436	
					437	* some constants
					438	
			00000400	00000001	439	K EQU 1024 One KB
			00001000	00000001	440	PAGE EQU (4*K) Size of one page
			00010000	00000001	441	K64 EQU (64*K) 64 KB
			00100000	00000001	442	MB EQU (K*K) 1 MB
					443	
			AABBCCDD	00000001	444	REG2PATT EQU X' AABBCCDD' Polluted Register pattern
			000000DD	00000001	445	REG2LOW EQU X' DD' (last byte above)

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT
					447 *=====
					448 *
					449 * NOTE: start data on an address that is easy to display
					450 * within Hercules
					451 *
					452 *=====
					453
0000057C			0000057C	00001000	454 ORG ZVE7TST+X' 1000'
00001000	00000000				455 FAILED DC F' 0' some test failed?
00001004	00000000				456 TESTING DC F' 0' current test number
					458 *****
					459 * TEST failed : result messgae
					460 *****
					461 *
					462 * failed message and associated editting
					463 *
00001008	40404040	40404040			464 PRTLIN DC C' Test # '
00001018	A7A7A7				465 PRTNUM DC C' xxx'
0000101B	40868189	93858440			466 DC C' failed for instruction '
00001033	A7A7A7A7	A7A7A7A7			467 PRTNAME DC CL8' xxxxxxxx'
0000103B	40A689A3	884094F4			468 DC C' with m4='
00001044	A7A7A7				469 PRTM4 DC C' xxx'
00001047	6B				470 DC C' , '
00001048	40A689A3	884094F5			471 DC C' with m5='
00001051	A7A7A7				472 PRTM5 DC C' xxx'
00001054	4B				473 DC C' . '
			0000004D	00000001	474 PRTLNG EQU *- PRTLIN
					475
					476 *****
					477 * TEST failed : CC message
					478 *****
					479 *
					480 * failed message and associated editting
					481 *
00001055	40404040	40404040			482 CCPRTLIN DC C' Test # '
00001065	A7A7A7				483 CCPRTNUM DC C' xxx'
00001068	40A69996	95874083			484 DC c' wrong cc for instruction '
00001082	A7A7A7A7	A7A7A7A7			485 CCPRTNAME DC CL8' xxxxxxxx'
0000108A	4085A797	8583A385			486 DC C' expected: cc='
00001098	A7				487 CCPRTEXP DC C' x'
00001099	6B				488 DC C' , '
0000109A	40998583	8589A585			489 DC C' received: cc='
000010A8	A7				490 CCPRTGOT DC C' x'
000010A9	4B				491 DC C' . '
			00000055	00000001	492 CCPRTLNG EQU *- CCPRTLIN

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				494 *****
				495 * TEST failed : message working storge
				496 *****
000010AA	40212020	20202020		497 EDIT DC XL18' 4021202020202020202020202020202020'
				498
000010BC	7E7E7E6E			499 DC C' ==>'
000010C0	40404040	40404040		500 PRT3 DC CL18' '
000010D2	4C7E7E7E			501 DC C' <==='
000010D6	00000000	00000000		502 DECNUM DS CL16
				504 *****
				505 * Vector instruction results, pollution and input
				506 *****
000010E8				507 DS 0F
000010E8	00000000	00000000		508 DS XL16
000010F8	FFFFFFFF	FFFFFFFF		509 V1FUDGE DC XL16' FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF' V1 FUDGE
00001108	00000000	00000000		510 DS XL16
				512 *****
				513 * E7TEST DSECT
				514 *****
				516 E7TEST DSECT ,
00000000	00000000			517 TSUB DC A(0) pointer to test
00000004	0000			518 TNUM DC H' 00' Test Number
00000006	00			519 DC X' 00'
00000007	00			520 M4 DC HL1' 00' m4 used
00000008	00			521 M5 DC HL1' 00' m5 used
00000009	00			522 CC DC HL1' 00' cc expected
0000000A	00			523 CCMASK DC HL1' 00' not expected CC mask
				524 *
				525 * CC extrtaction
				526 *
0000000C	00000000	00000000		527 CCPSW DS 2F extract PSW after test (has CC)
00000014	00			528 CCFOUND DS X extracted cc
				529
00000015	40404040	40404040		530 OPNAME DC CL8' ' E7 name
00000020	00000000			531 V1ADDR DC A(0) address of v1 result
00000024	00000000			532 V2ADDR DC A(0) address of v2 source
00000028	00000000			533 V3ADDR DC A(0) address of v3 source
0000002C	00000000			534 RELEN DC A(0) RESULT LENGTH
00000030	00000000			535 READDR DC A(0) result (expected) address
00000038	00000000	00000000		536 DS 2FD gap
00000048	00000000	00000000		537 V1OUTPUT DS XL16 V1 Output
00000058	00000000	00000000		538 DS 2FD gap
				539
				540 * test routine will be here (from VRR-b macro)
				541 *
				542 * followed by
				543 * EXPECTED RESULT

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
00001118		00000000	00009D6F	545 ZVE7TST CSECT , 546 DS OF	
				548 *****	
				549 * Macros to help build test tables	
				550 *****	
				552 *	
				553 * macro to generate individual test	
				554 *	
				555 MACRO	
				556 VRR_B &INST, &M4, &CC	
				557 . *	&INST - VRR-b instruction under test
				558 . *	&M4 - m4 field - element size
				559 . *	&CC - expected CC
				560	
				561 LCLA &XCC(4) &XCC has mask values for FAILED condition codes	
				562 &XCC(1) SETA 7 CC != 0	
				563 &XCC(2) SETA 11 CC != 1	
				564 &XCC(3) SETA 13 CC != 2	
				565 &XCC(4) SETA 14 CC != 3	
				566	
				567 GBLA &TNUM	
				568 &TNUM SETA &TNUM+1	
				569	
				570 DS OFD	
				571 USING *, R5	base for test data and test routine
				572	
				573 T&TNUM DC A(X&TNUM)	address of test routine
				574 DC H' &TNUM	test number
				575 DC X' 00'	
				576 DC HL1' &M4'	m4 used
				577 DC HL1' 1'	m5 used
				578 DC HL1' &CC'	CC
				579 DC HL1' &XCC(&CC+1)'	CC failed mask
				580	
				581 DS 2F	extracted PSW after test (has CC)
				582 DC X' FF'	extracted CC, if test failed
				583	
				584 DC CL8' &INST'	instruction name
				585 DC A(RE&TNUM)	address of v1 result
				586 DC A(RE&TNUM+16)	address of v2 source
				587 DC A(RE&TNUM+32)	address of v3 source
				588 DC A(16)	result length
				589 REA&TNUM DC A(RE&TNUM)	result address
				590 DS 2FD	gap
				591 V10&TNUM DS XL16	V1 output
				592 DS 2FD	gap
				593 . *	
				594 *	
				595 X&TNUM DS OF	
				596 LGF R1, V2ADDR	load v2 source
				597 VL v22, 0(R1)	use v21 to test decoder
				598 LGF R1, V3ADDR	load v3 source





LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				638	*****
				639	* E7 VRR-b tests
				640	*****
				641	PRINT DATA
				642	*
				643	*
				644	* E795 VPKLS - Vector Pack Logical Saturate
				645	* E797 VPKS - Vector Pack Saturate
				646	* E7F8 VCEQ - Vector Compare Equal
				647	* E7F9 VCHL - Vector Compare High Logical
				648	* E7FB VCH - Vector Compare High
				649	*
				650	* VRR-b instruction,
				651	* M, element size
				652	* CC expected condition code
				653	*
				654	* followed by
				655	* 16 byte V1 result
				656	* 16 byte V2 source
				657	* 16 byte V3 source
				658	*
				659	* NOTE: M5 is preset to 1; Condition Code Set (CS)
				660	*
				661	* -----
				662	* VPKLS - Vector Pack Logical Saturate
				663	* -----
				664	* cc=0: No saturation
				665	* cc=1: At least one but not all elements saturated
				666	* cc=3: Saturation on all elements
				667	* -----
				668	* case - simple cc debug
				669	* -----
				670	* Halfword
				671	VRR_B VPKLS, 1, 0
00001118				672+	DS OFD
00001118		00001118		673+	USING *, R5
00001118	00001180			674+T1	DC A(X1)
0000111C	0001			675+	DC H' 1'
0000111E	00			676+	DC X' 00'
0000111F	01			677+	DC HL1' 1'
00001120	01			678+	DC HL1' 1'
00001121	00			679+	DC HL1' 0'
00001122	07			680+	DC HL1' 7'
00001124	00000000	00000000		681+	DS 2F
0000112C	FF			682+	DC X' FF'
0000112D	E5D7D2D3	E2404040		683+	DC CL8' VPKLS'
00001138	000011B0			684+	DC A(RE1)
0000113C	000011C0			685+	DC A(RE1+16)
00001140	000011D0			686+	DC A(RE1+32)
00001144	00000010			687+	DC A(16)
00001148	000011B0			688+REA1	DC A(RE1)
00001150	00000000	00000000		689+	DS 2FD
00001158	00000000	00000000			
00001160	00000000	00000000		690+V101	DS XL16
00001168	00000000	00000000			
00001170	00000000	00000000		691+	DS 2FD

base for test data and test routine  
address of test routine  
test number

m4 used  
m5 used

CC  
CC failed mask  
extracted PSW after test (has CC)  
extracted CC, if test failed

instruction name  
address of v1 result  
address of v2 source  
address of v3 source  
result length  
result address

gap  
V1 output  
gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001178	00000000 00000000			692+*			
00001180				693+X1	DS	0F	
00001180	E310 5024 0014		00000024	694+	LGF	R1, V2ADDR	load v2 source
00001186	E761 0000 0806		00000000	695+	VL	v22, 0(R1)	use v21 to test decoder
0000118C	E310 5028 0014		00000028	696+	LGF	R1, V3ADDR	load v3 source
00001192	E771 0000 0806		00000000	697+	VL	v23, 0(R1)	use v22 to test decoder
00001198	E756 7010 1E95			698+	VPKLS	V21, V22, V23, 1, 1	test instruction
0000119E	B98D 0020			699+	EPSW	R2, R0	extract psw
000011A2	5020 500C		0000000C	700+	ST	R2, CCPSW	to save CC
000011A6	E750 5048 080E		00001160	701+	VST	V21, V101	save v1 output
000011AC	07FB			702+	BR	R11	return
000011B0				703+RE1	DC	0F	V1 for this test
000011B0				704+	DROP	R5	
000011B0	00000000 00000000			705	DC	XL16' 0000000000000000 0000000000000000'	result
000011B8	00000000 00000000						
000011C0	00000000 00000000			706	DC	XL16' 0000000000000000 0000000000000000'	v2
000011C8	00000000 00000000						
000011D0	00000000 00000000			707	DC	XL16' 0000000000000000 0000000000000000'	v3
000011D8	00000000 00000000						
				708			
				709	VRR_B	VPKLS, 1, 1	
000011E0				710+	DS	0FD	
000011E0		000011E0		711+	USING	*, R5	base for test data and test routine
000011E0	00001248			712+T2	DC	A(X2)	address of test routine
000011E4	0002			713+	DC	H' 2'	test number
000011E6	00			714+	DC	X' 00'	
000011E7	01			715+	DC	HL1' 1'	m4 used
000011E8	01			716+	DC	HL1' 1'	m5 used
000011E9	01			717+	DC	HL1' 1'	CC
000011EA	0B			718+	DC	HL1' 11'	CC failed mask
000011EC	00000000 00000000			719+	DS	2F	extracted PSW after test (has CC)
000011F4	FF			720+	DC	X' FF'	extracted CC, if test failed
000011F5	E5D7D2D3 E2404040			721+	DC	CL8' VPKLS'	instruction name
00001200	00001278			722+	DC	A(RE2)	address of v1 result
00001204	00001288			723+	DC	A(RE2+16)	address of v2 source
00001208	00001298			724+	DC	A(RE2+32)	address of v3 source
0000120C	00000010			725+	DC	A(16)	result length
00001210	00001278			726+REA2	DC	A(RE2)	result address
00001218	00000000 00000000			727+	DS	2FD	gap
00001220	00000000 00000000						
00001228	00000000 00000000			728+V102	DS	XL16	V1 output
00001230	00000000 00000000						
00001238	00000000 00000000			729+	DS	2FD	gap
00001240	00000000 00000000						
				730+*			
00001248				731+X2	DS	0F	
00001248	E310 5024 0014		00000024	732+	LGF	R1, V2ADDR	load v2 source
0000124E	E761 0000 0806		00000000	733+	VL	v22, 0(R1)	use v21 to test decoder
00001254	E310 5028 0014		00000028	734+	LGF	R1, V3ADDR	load v3 source
0000125A	E771 0000 0806		00000000	735+	VL	v23, 0(R1)	use v22 to test decoder
00001260	E756 7010 1E95			736+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001266	B98D 0020			737+	EPSW	R2, R0	extract psw
0000126A	5020 500C		0000000C	738+	ST	R2, CCPSW	to save CC
0000126E	E750 9028 080E		00001228	739+	VST	V21, V102	save v1 output
00001274	07FB			740+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001278				741+RE2	DC	0F	V1 for this test
00001278				742+	DROP	R5	
00001278	00000000 00000000			743	DC	XL16' 0000000000000000 0000000000000000'	result
00001280	FFFFFFFF FFFFFFFF						
00001288	00000000 00000000			744	DC	XL16' 0000000000000000 0000000000000000'	v2
00001290	00000000 00000000						
00001298	FFFFFFFF FFFFFFFF			745	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
000012A0	FFFFFFFF FFFFFFFF						
				746			
				747	VRR_B	VPKLS, 1, 3	
000012A8				748+	DS	0FD	
000012A8		000012A8		749+	USING	*, R5	base for test data and test routine
000012A8	00001310			750+T3	DC	A(X3)	address of test routine
000012AC	0003			751+	DC	H' 3'	test number
000012AE	00			752+	DC	X' 00'	
000012AF	01			753+	DC	HL1' 1'	m4 used
000012B0	01			754+	DC	HL1' 1'	m5 used
000012B1	03			755+	DC	HL1' 3'	CC
000012B2	0E			756+	DC	HL1' 14'	CC failed mask
000012B4	00000000 00000000			757+	DS	2F	extracted PSW after test (has CC)
000012BC	FF			758+	DC	X' FF'	extracted CC, if test failed
000012BD	E5D7D2D3 E2404040			759+	DC	CL8' VPKLS'	instruction name
000012C8	00001340			760+	DC	A(RE3)	address of v1 result
000012CC	00001350			761+	DC	A(RE3+16)	address of v2 source
000012D0	00001360			762+	DC	A(RE3+32)	address of v3 source
000012D4	00000010			763+	DC	A(16)	result length
000012D8	00001340			764+REA3	DC	A(RE3)	result address
000012E0	00000000 00000000			765+	DS	2FD	gap
000012E8	00000000 00000000						
000012F0	00000000 00000000			766+V103	DS	XL16	V1 output
000012F8	00000000 00000000						
00001300	00000000 00000000			767+	DS	2FD	gap
00001308	00000000 00000000						
				768+*			
00001310				769+X3	DS	0F	
00001310	E310 5024 0014		00000024	770+	LGF	R1, V2ADDR	load v2 source
00001316	E761 0000 0806		00000000	771+	VL	v22, 0(R1)	use v21 to test decoder
0000131C	E310 5028 0014		00000028	772+	LGF	R1, V3ADDR	load v3 source
00001322	E771 0000 0806		00000000	773+	VL	v23, 0(R1)	use v22 to test decoder
00001328	E756 7010 1E95			774+	VPKLS	V21, V22, V23, 1, 1	test instruction
0000132E	B98D 0020			775+	EPSW	R2, R0	extract psw
00001332	5020 500C		0000000C	776+	ST	R2, CCPSW	to save CC
00001336	E750 5048 080E		000012F0	777+	VST	V21, V103	save v1 output
0000133C	07FB			778+	BR	R11	return
00001340				779+RE3	DC	0F	V1 for this test
00001340				780+	DROP	R5	
00001340	FFFFFFFF FFFFFFFF			781	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00001348	FFFFFFFF FFFFFFFF						
00001350	FFFFFFFF FFFFFFFF			782	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00001358	FFFFFFFF FFFFFFFF						
00001360	FFFFFFFF FFFFFFFF			783	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00001368	FFFFFFFF FFFFFFFF						
				784			
				785 *Word			
				786	VRR_B	VPKLS, 2, 0	
00001370				787+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001370		00001370		788+	USING *, R5	base for test data and test routine
00001370	000013D8			789+T4	DC A(X4)	address of test routine
00001374	0004			790+	DC H' 4'	test number
00001376	00			791+	DC X' 00'	
00001377	02			792+	DC HL1' 2'	m4 used
00001378	01			793+	DC HL1' 1'	m5 used
00001379	00			794+	DC HL1' 0'	CC
0000137A	07			795+	DC HL1' 7'	CC failed mask
0000137C	00000000 00000000			796+	DS 2F	extracted PSW after test (has CC)
00001384	FF			797+	DC X' FF'	extracted CC, if test failed
00001385	E5D7D2D3 E2404040			798+	DC CL8' VPKLS'	instruction name
00001390	00001408			799+	DC A(RE4)	address of v1 result
00001394	00001418			800+	DC A(RE4+16)	address of v2 source
00001398	00001428			801+	DC A(RE4+32)	address of v3 source
0000139C	00000010			802+	DC A(16)	result length
000013A0	00001408			803+REA4	DC A(RE4)	result address
000013A8	00000000 00000000			804+	DS 2FD	gap
000013B0	00000000 00000000					
000013B8	00000000 00000000			805+V104	DS XL16	V1 output
000013C0	00000000 00000000					
000013C8	00000000 00000000			806+	DS 2FD	gap
000013D0	00000000 00000000					
				807+*		
000013D8				808+X4	DS 0F	
000013D8	E310 5024 0014		00000024	809+	LGF R1, V2ADDR	load v2 source
000013DE	E761 0000 0806		00000000	810+	VL v22, 0(R1)	use v21 to test decoder
000013E4	E310 5028 0014		00000028	811+	LGF R1, V3ADDR	load v3 source
000013EA	E771 0000 0806		00000000	812+	VL v23, 0(R1)	use v22 to test decoder
000013F0	E756 7010 2E95			813+	VPKLS V21, V22, V23, 2, 1	test instruction
000013F6	B98D 0020			814+	EPSW R2, R0	extract psw
000013FA	5020 500C		0000000C	815+	ST R2, CCPSW	to save CC
000013FE	E750 5048 080E		000013B8	816+	VST V21, V104	save v1 output
00001404	07FB			817+	BR R11	return
00001408				818+RE4	DC 0F	V1 for this test
00001408				819+	DROP R5	
00001408	00000000 00000000			820	DC XL16' 0000000000000000 0000000000000000'	result
00001410	00000000 00000000					
00001418	00000000 00000000			821	DC XL16' 0000000000000000 0000000000000000'	v2
00001420	00000000 00000000					
00001428	00000000 00000000			822	DC XL16' 0000000000000000 0000000000000000'	v3
00001430	00000000 00000000					
				823		
				824	VRR_B VPKLS, 2, 1	
00001438				825+	DS 0FD	
00001438		00001438		826+	USING *, R5	base for test data and test routine
00001438	000014A0			827+T5	DC A(X5)	address of test routine
0000143C	0005			828+	DC H' 5'	test number
0000143E	00			829+	DC X' 00'	
0000143F	02			830+	DC HL1' 2'	m4 used
00001440	01			831+	DC HL1' 1'	m5 used
00001441	01			832+	DC HL1' 1'	CC
00001442	0B			833+	DC HL1' 11'	CC failed mask
00001444	00000000 00000000			834+	DS 2F	extracted PSW after test (has CC)
0000144C	FF			835+	DC X' FF'	extracted CC, if test failed
0000144D	E5D7D2D3 E2404040			836+	DC CL8' VPKLS'	instruction name
00001458	000014D0			837+	DC A(RE5)	address of v1 result



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000145C	000014E0			838+	DC	A(RE5+16)	address of v2 source
00001460	000014F0			839+	DC	A(RE5+32)	address of v3 source
00001464	00000010			840+	DC	A(16)	result length
00001468	000014D0			841+REA5	DC	A(RE5)	result address
00001470	00000000 00000000			842+	DS	2FD	gap
00001478	00000000 00000000						
00001480	00000000 00000000			843+V105	DS	XL16	V1 output
00001488	00000000 00000000						
00001490	00000000 00000000			844+	DS	2FD	gap
00001498	00000000 00000000						
				845+*			
000014A0				846+X5	DS	0F	
000014A0	E310 5024 0014		00000024	847+	LGF	R1, V2ADDR	load v2 source
000014A6	E761 0000 0806		00000000	848+	VL	v22, 0(R1)	use v21 to test decoder
000014AC	E310 5028 0014		00000028	849+	LGF	R1, V3ADDR	load v3 source
000014B2	E771 0000 0806		00000000	850+	VL	v23, 0(R1)	use v22 to test decoder
000014B8	E756 7010 2E95			851+	VPKLS	V21, V22, V23, 2, 1	test instruction
000014BE	B98D 0020			852+	EPSW	R2, R0	extract psw
000014C2	5020 500C		0000000C	853+	ST	R2, CCPSW	to save CC
000014C6	E750 5048 080E		00001480	854+	VST	V21, V105	save v1 output
000014CC	07FB			855+	BR	R11	return
000014D0				856+RE5	DC	0F	V1 for this test
000014D0				857+	DROP	R5	
000014D0	00000000 00000000			858	DC	XL16' 0000000000000000 FFFFFFFF'	result
000014D8	FFFFFFFF FFFFFFFF						
000014E0	00000000 00000000			859	DC	XL16' 0000000000000000 0000000000000000'	v2
000014E8	00000000 00000000						
000014F0	FFFFFFFF FFFFFFFF			860	DC	XL16' FFFFFFFF'	v3
000014F8	FFFFFFFF FFFFFFFF						
				861			
				862	VRR_B	VPKLS, 2, 3	
00001500				863+	DS	0FD	
00001500		00001500		864+	USING	*, R5	base for test data and test routine
00001500	00001568			865+T6	DC	A(X6)	address of test routine
00001504	0006			866+	DC	H' 6'	test number
00001506	00			867+	DC	X' 00'	
00001507	02			868+	DC	HL1' 2'	m4 used
00001508	01			869+	DC	HL1' 1'	m5 used
00001509	03			870+	DC	HL1' 3'	CC
0000150A	0E			871+	DC	HL1' 14'	CC failed mask
0000150C	00000000 00000000			872+	DS	2F	extracted PSW after test (has CC)
00001514	FF			873+	DC	X' FF'	extracted CC, if test failed
00001515	E5D7D2D3 E2404040			874+	DC	CL8' VPKLS'	instruction name
00001520	00001598			875+	DC	A(RE6)	address of v1 result
00001524	000015A8			876+	DC	A(RE6+16)	address of v2 source
00001528	000015B8			877+	DC	A(RE6+32)	address of v3 source
0000152C	00000010			878+	DC	A(16)	result length
00001530	00001598			879+REA6	DC	A(RE6)	result address
00001538	00000000 00000000			880+	DS	2FD	gap
00001540	00000000 00000000						
00001548	00000000 00000000			881+V106	DS	XL16	V1 output
00001550	00000000 00000000						
00001558	00000000 00000000			882+	DS	2FD	gap
00001560	00000000 00000000						
				883+*			
00001568				884+X6	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001568	E310 5024 0014		00000024	885+	LGF	R1, V2ADDR	load v2 source
0000156E	E761 0000 0806		00000000	886+	VL	v22, 0(R1)	use v21 to test decoder
00001574	E310 5028 0014		00000028	887+	LGF	R1, V3ADDR	load v3 source
0000157A	E771 0000 0806		00000000	888+	VL	v23, 0(R1)	use v22 to test decoder
00001580	E756 7010 2E95			889+	VPKLS	V21, V22, V23, 2, 1	test instruction
00001586	B98D 0020			890+	EPSW	R2, R0	extract psw
0000158A	5020 500C		0000000C	891+	ST	R2, CCPSW	to save CC
0000158E	E750 5048 080E		00001548	892+	VST	V21, V106	save v1 output
00001594	07FB			893+	BR	R11	return
00001598				894+RE6	DC	0F	V1 for this test
00001598				895+	DROP	R5	
00001598	FFFFFFFF FFFFFFFF			896	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000015A0	FFFFFFFF FFFFFFFF						
000015A8	FFFFFFFF FFFFFFFF			897	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
000015B0	FFFFFFFF FFFFFFFF						
000015B8	FFFFFFFF FFFFFFFF			898	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
000015C0	FFFFFFFF FFFFFFFF						
				899			
				900 *DoubleWord			
				901	VRR_B	VPKLS, 3, 0	
000015C8				902+	DS	0FD	
000015C8		000015C8		903+	USING	*, R5	base for test data and test routine
000015C8	00001630			904+T7	DC	A(X7)	address of test routine
000015CC	0007			905+	DC	H' 7'	test number
000015CE	00			906+	DC	X' 00'	
000015CF	03			907+	DC	HL1' 3'	m4 used
000015D0	01			908+	DC	HL1' 1'	m5 used
000015D1	00			909+	DC	HL1' 0'	CC
000015D2	07			910+	DC	HL1' 7'	CC failed mask
000015D4	00000000 00000000			911+	DS	2F	extracted PSW after test (has CC)
000015DC	FF			912+	DC	X' FF'	extracted CC, if test failed
000015DD	E5D7D2D3 E2404040			913+	DC	CL8' VPKLS'	instruction name
000015E8	00001660			914+	DC	A(RE7)	address of v1 result
000015EC	00001670			915+	DC	A(RE7+16)	address of v2 source
000015F0	00001680			916+	DC	A(RE7+32)	address of v3 source
000015F4	00000010			917+	DC	A(16)	result length
000015F8	00001660			918+REA7	DC	A(RE7)	result address
00001600	00000000 00000000			919+	DS	2FD	gap
00001608	00000000 00000000						
00001610	00000000 00000000			920+V107	DS	XL16	V1 output
00001618	00000000 00000000						
00001620	00000000 00000000			921+	DS	2FD	gap
00001628	00000000 00000000						
				922+*			
00001630				923+X7	DS	0F	
00001630	E310 5024 0014		00000024	924+	LGF	R1, V2ADDR	load v2 source
00001636	E761 0000 0806		00000000	925+	VL	v22, 0(R1)	use v21 to test decoder
0000163C	E310 5028 0014		00000028	926+	LGF	R1, V3ADDR	load v3 source
00001642	E771 0000 0806		00000000	927+	VL	v23, 0(R1)	use v22 to test decoder
00001648	E756 7010 3E95			928+	VPKLS	V21, V22, V23, 3, 1	test instruction
0000164E	B98D 0020			929+	EPSW	R2, R0	extract psw
00001652	5020 500C		0000000C	930+	ST	R2, CCPSW	to save CC
00001656	E750 5048 080E		00001610	931+	VST	V21, V107	save v1 output
0000165C	07FB			932+	BR	R11	return
00001660				933+RE7	DC	0F	V1 for this test
00001660				934+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001660	00000000 00000000			935	DC	XL16' 0000000000000000 0000000000000000'	result
00001668	00000000 00000000						
00001670	00000000 00000000			936	DC	XL16' 0000000000000000 0000000000000000'	v2
00001678	00000000 00000000						
00001680	00000000 00000000			937	DC	XL16' 0000000000000000 0000000000000000'	v3
00001688	00000000 00000000						
				938			
				939	VRR_B	VPKLS, 3, 1	
00001690				940+	DS	0FD	
00001690		00001690		941+	USING	*, R5	base for test data and test routine
00001690	000016F8			942+T8	DC	A(X8)	address of test routine
00001694	0008			943+	DC	H' 8'	test number
00001696	00			944+	DC	X' 00'	
00001697	03			945+	DC	HL1' 3'	m4 used
00001698	01			946+	DC	HL1' 1'	m5 used
00001699	01			947+	DC	HL1' 1'	CC
0000169A	0B			948+	DC	HL1' 11'	CC failed mask
0000169C	00000000 00000000			949+	DS	2F	extracted PSW after test (has CC)
000016A4	FF			950+	DC	X' FF'	extracted CC, if test failed
000016A5	E5D7D2D3 E2404040			951+	DC	CL8' VPKLS'	instruction name
000016B0	00001728			952+	DC	A(RE8)	address of v1 result
000016B4	00001738			953+	DC	A(RE8+16)	address of v2 source
000016B8	00001748			954+	DC	A(RE8+32)	address of v3 source
000016BC	00000010			955+	DC	A(16)	result length
000016C0	00001728			956+REA8	DC	A(RE8)	result address
000016C8	00000000 00000000			957+	DS	2FD	gap
000016D0	00000000 00000000						
000016D8	00000000 00000000			958+V108	DS	XL16	V1 output
000016E0	00000000 00000000						
000016E8	00000000 00000000			959+	DS	2FD	gap
000016F0	00000000 00000000						
				960+*			
000016F8				961+X8	DS	0F	
000016F8	E310 5024 0014		00000024	962+	LGF	R1, V2ADDR	load v2 source
000016FE	E761 0000 0806		00000000	963+	VL	v22, 0(R1)	use v21 to test decoder
00001704	E310 5028 0014		00000028	964+	LGF	R1, V3ADDR	load v3 source
0000170A	E771 0000 0806		00000000	965+	VL	v23, 0(R1)	use v22 to test decoder
00001710	E756 7010 3E95			966+	VPKLS	V21, V22, V23, 3, 1	test instruction
00001716	B98D 0020			967+	EPSW	R2, R0	extract psw
0000171A	5020 500C		0000000C	968+	ST	R2, CCPSW	to save CC
0000171E	E750 5048 080E		000016D8	969+	VST	V21, V108	save v1 output
00001724	07FB			970+	BR	R11	return
00001728				971+RE8	DC	0F	V1 for this test
00001728				972+	DROP	R5	
00001728	00000000 00000000			973	DC	XL16' 0000000000000000 FFFFFFFFFFFFFFFFFF'	result
00001730	FFFFFFFF FFFFFFFF						
00001738	00000000 00000000			974	DC	XL16' 0000000000000000 0000000000000000'	v2
00001740	00000000 00000000						
00001748	FFFFFFFF FFFFFFFF			975	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00001750	FFFFFFFF FFFFFFFF						
				976			
				977	VRR_B	VPKLS, 3, 3	
00001758				978+	DS	0FD	
00001758		00001758		979+	USING	*, R5	base for test data and test routine
00001758	000017C0			980+T9	DC	A(X9)	address of test routine
0000175C	0009			981+	DC	H' 9'	test number



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000175E	00			982+	DC	X' 00'	
0000175F	03			983+	DC	HL1' 3'	m4 used
00001760	01			984+	DC	HL1' 1'	m5 used
00001761	03			985+	DC	HL1' 3'	CC
00001762	0E			986+	DC	HL1' 14'	CC failed mask
00001764	00000000 00000000			987+	DS	2F	extracted PSW after test (has CC)
0000176C	FF			988+	DC	X' FF'	extracted CC, if test failed
0000176D	E5D7D2D3 E2404040			989+	DC	CL8' VPKLS'	instruction name
00001778	000017F0			990+	DC	A(RE9)	address of v1 result
0000177C	00001800			991+	DC	A(RE9+16)	address of v2 source
00001780	00001810			992+	DC	A(RE9+32)	address of v3 source
00001784	00000010			993+	DC	A(16)	result length
00001788	000017F0			994+REA9	DC	A(RE9)	result address
00001790	00000000 00000000			995+	DS	2FD	gap
00001798	00000000 00000000						
000017A0	00000000 00000000			996+V109	DS	XL16	V1 output
000017A8	00000000 00000000						
000017B0	00000000 00000000			997+	DS	2FD	gap
000017B8	00000000 00000000						
				998+*			
000017C0				999+X9	DS	0F	
000017C0	E310 5024 0014		00000024	1000+	LGF	R1, V2ADDR	load v2 source
000017C6	E761 0000 0806		00000000	1001+	VL	v22, 0(R1)	use v21 to test decoder
000017CC	E310 5028 0014		00000028	1002+	LGF	R1, V3ADDR	load v3 source
000017D2	E771 0000 0806		00000000	1003+	VL	v23, 0(R1)	use v22 to test decoder
000017D8	E756 7010 3E95			1004+	VPKLS	V21, V22, V23, 3, 1	test instruction
000017DE	B98D 0020			1005+	EPSW	R2, R0	extract psw
000017E2	5020 500C		0000000C	1006+	ST	R2, CCPSW	to save CC
000017E6	E750 5048 080E		000017A0	1007+	VST	V21, V109	save v1 output
000017EC	07FB			1008+	BR	R11	return
000017F0				1009+RE9	DC	0F	V1 for this test
000017F0				1010+	DROP	R5	
000017F0	FFFFFFFF FFFFFFFF			1011	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000017F8	FFFFFFFF FFFFFFFF						
00001800	FFFFFFFF FFFFFFFF			1012	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00001808	FFFFFFFF FFFFFFFF						
00001810	FFFFFFFF FFFFFFFF			1013	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00001818	FFFFFFFF FFFFFFFF						
				1014			
				1015	*	-----	
				1016	*	case - general	
				1017	*	-----	
				1018	*	Halfword	
				1019		VRR_B VPKLS, 1, 0	
00001820				1020+	DS	0FD	
00001820		00001820		1021+	USING	*, R5	base for test data and test routine
00001820	00001888			1022+T10	DC	A(X10)	address of test routine
00001824	000A			1023+	DC	H' 10'	test number
00001826	00			1024+	DC	X' 00'	
00001827	01			1025+	DC	HL1' 1'	m4 used
00001828	01			1026+	DC	HL1' 1'	m5 used
00001829	00			1027+	DC	HL1' 0'	CC
0000182A	07			1028+	DC	HL1' 7'	CC failed mask
0000182C	00000000 00000000			1029+	DS	2F	extracted PSW after test (has CC)
00001834	FF			1030+	DC	X' FF'	extracted CC, if test failed
00001835	E5D7D2D3 E2404040			1031+	DC	CL8' VPKLS'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001840	000018B8			1032+	DC	A(RE10)	address of v1 result
00001844	000018C8			1033+	DC	A(RE10+16)	address of v2 source
00001848	000018D8			1034+	DC	A(RE10+32)	address of v3 source
0000184C	00000010			1035+	DC	A(16)	result length
00001850	000018B8			1036+REA10	DC	A(RE10)	result address
00001858	00000000 00000000			1037+	DS	2FD	gap
00001860	00000000 00000000						
00001868	00000000 00000000			1038+V1010	DS	XL16	V1 output
00001870	00000000 00000000						
00001878	00000000 00000000			1039+	DS	2FD	gap
00001880	00000000 00000000						
00001888				1040+*			
00001888	E310 5024 0014		00000024	1041+X10	DS	0F	
0000188E	E761 0000 0806		00000000	1042+	LGF	R1, V2ADDR	load v2 source
00001894	E310 5028 0014		00000028	1043+	VL	v22, 0(R1)	use v21 to test decoder
0000189A	E771 0000 0806		00000000	1044+	LGF	R1, V3ADDR	load v3 source
000018A0	E756 7010 1E95			1045+	VL	v23, 0(R1)	use v22 to test decoder
000018A6	B98D 0020			1046+	VPKLS	V21, V22, V23, 1, 1	test instruction
000018AA	5020 500C		0000000C	1047+	EPSW	R2, R0	extract psw
000018AE	E750 5048 080E		00001868	1048+	ST	R2, CCPSW	to save CC
000018B4	07FB			1049+	VST	V21, V1010	save v1 output
000018B8				1050+	BR	R11	return
000018B8				1051+RE10	DC	0F	V1 for this test
000018B8				1052+	DROP	R5	
000018B8	11335577 99BBDDFF			1053	DC	XL16' 1133557799BBDDFF FEFDFCFBFAF9F8F7'	result
000018C0	FEFDFCFB FAF9F8F7						
000018C8	00110033 00550077			1054	DC	XL16' 0011003300550077 009900BB00DD00FF'	v2
000018D0	009900BB 00DD00FF						
000018D8	00FE00FD 00FC00FB			1055	DC	XL16' 00FE00FD00FC00FB 00FA00F900F800F7'	v3
000018E0	00FA00F9 00F800F7						
000018E8				1056			
000018E8		000018E8		1057	VRR_B	VPKLS, 1, 0	
000018E8	00001950			1058+	DS	0FD	
000018EC	000B			1059+	USING	*, R5	base for test data and test routine
000018EE	00			1060+T11	DC	A(X11)	address of test routine
000018EF	01			1061+	DC	H' 11'	test number
000018F0	01			1062+	DC	X' 00'	
000018F1	00			1063+	DC	HL1' 1'	m4 used
000018F2	07			1064+	DC	HL1' 1'	m5 used
000018F4	00000000 00000000			1065+	DC	HL1' 0'	CC
000018FC	FF			1066+	DC	HL1' 7'	CC failed mask
000018FD	E5D7D2D3 E2404040			1067+	DS	2F	extracted PSW after test (has CC)
00001908	00001980			1068+	DC	X' FF'	extracted CC, if test failed
0000190C	00001990			1069+	DC	CL8' VPKLS'	instruction name
00001910	000019A0			1070+	DC	A(RE11)	address of v1 result
00001914	00000010			1071+	DC	A(RE11+16)	address of v2 source
00001918	00001980			1072+	DC	A(RE11+32)	address of v3 source
00001920	00000000 00000000			1073+	DC	A(16)	result length
00001928	00000000 00000000			1074+REA11	DC	A(RE11)	result address
00001930	00000000 00000000			1075+	DS	2FD	gap
00001938	00000000 00000000						
00001940	00000000 00000000			1076+V1011	DS	XL16	V1 output
00001948	00000000 00000000						
				1077+	DS	2FD	gap
				1078+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001950				1079+X11	DS	0F	
00001950	E310 5024 0014		00000024	1080+	LGF	R1, V2ADDR	load v2 source
00001956	E761 0000 0806		00000000	1081+	VL	v22, 0(R1)	use v21 to test decoder
0000195C	E310 5028 0014		00000028	1082+	LGF	R1, V3ADDR	load v3 source
00001962	E771 0000 0806		00000000	1083+	VL	v23, 0(R1)	use v22 to test decoder
00001968	E756 7010 1E95			1084+	VPKLS	V21, V22, V23, 1, 1	test instruction
0000196E	B98D 0020			1085+	EPSW	R2, R0	extract psw
00001972	5020 500C		0000000C	1086+	ST	R2, CCPSW	to save CC
00001976	E750 5048 080E		00001930	1087+	VST	V21, V1011	save v1 output
0000197C	07FB			1088+	BR	R11	return
00001980				1089+RE11	DC	0F	V1 for this test
00001980				1090+	DROP	R5	
00001980	FEFDFCFB FAF9F8F7			1091	DC	XL16' FEFDFCFBFAF9F8F7 1133557799BBDDFF'	result
00001988	11335577 99BBDDFF						
00001990	00FE00FD 00FC00FB			1092	DC	XL16' 00FE00FD00FC00FB 00FA00F900F800F7'	v2
00001998	00FA00F9 00F800F7						
000019A0	00110033 00550077			1093	DC	XL16' 0011003300550077 009900BB00DD00FF'	v3
000019A8	009900BB 00DD00FF						
				1094			
000019B0				1095	VRR_B	VPKLS, 1, 1	
000019B0		000019B0		1096+	DS	0FD	
000019B0	00001A18			1097+	USING	*, R5	base for test data and test routine
000019B4	000C			1098+T12	DC	A(X12)	address of test routine
000019B6	00			1099+	DC	H' 12'	test number
000019B7	01			1100+	DC	X' 00'	
000019B8	01			1101+	DC	HL1' 1'	m4 used
000019B8	01			1102+	DC	HL1' 1'	m5 used
000019B9	01			1103+	DC	HL1' 1'	CC
000019BA	0B			1104+	DC	HL1' 11'	CC failed mask
000019BC	00000000 00000000			1105+	DS	2F	extracted PSW after test (has CC)
000019C4	FF			1106+	DC	X' FF'	extracted CC, if test failed
000019C5	E5D7D2D3 E2404040			1107+	DC	CL8' VPKLS'	instruction name
000019D0	00001A48			1108+	DC	A(RE12)	address of v1 result
000019D4	00001A58			1109+	DC	A(RE12+16)	address of v2 source
000019D8	00001A68			1110+	DC	A(RE12+32)	address of v3 source
000019DC	00000010			1111+	DC	A(16)	result length
000019E0	00001A48			1112+REA12	DC	A(RE12)	result address
000019E8	00000000 00000000			1113+	DS	2FD	gap
000019F0	00000000 00000000						
000019F8	00000000 00000000			1114+V1012	DS	XL16	V1 output
00001A00	00000000 00000000						
00001A08	00000000 00000000			1115+	DS	2FD	gap
00001A10	00000000 00000000						
				1116+*			
00001A18				1117+X12	DS	0F	
00001A18	E310 5024 0014		00000024	1118+	LGF	R1, V2ADDR	load v2 source
00001A1E	E761 0000 0806		00000000	1119+	VL	v22, 0(R1)	use v21 to test decoder
00001A24	E310 5028 0014		00000028	1120+	LGF	R1, V3ADDR	load v3 source
00001A2A	E771 0000 0806		00000000	1121+	VL	v23, 0(R1)	use v22 to test decoder
00001A30	E756 7010 1E95			1122+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001A36	B98D 0020			1123+	EPSW	R2, R0	extract psw
00001A3A	5020 500C		0000000C	1124+	ST	R2, CCPSW	to save CC
00001A3E	E750 5048 080E		000019F8	1125+	VST	V21, V1012	save v1 output
00001A44	07FB			1126+	BR	R11	return
00001A48				1127+RE12	DC	0F	V1 for this test
00001A48				1128+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001A48	01FFFFFF FFFFFFFF			1129	DC	XL16' 01FFFFFFF	result
00001A50	11335577 99BBDDFF						
00001A58	00010203 04050607			1130	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001A60	08090A0B 0C0D0E0F						
00001A68	00110033 00550077			1131	DC	XL16' 0011003300550077 009900BB00DD00FF'	v3
00001A70	009900BB 00DD00FF						
				1132			
				1133	VRR_B	VPKLS, 1, 1	
00001A78				1134+	DS	0FD	
00001A78		00001A78		1135+	USING	*, R5	base for test data and test routine
00001A78	00001AE0			1136+T13	DC	A(X13)	address of test routine
00001A7C	000D			1137+	DC	H' 13'	test number
00001A7E	00			1138+	DC	X' 00'	
00001A7F	01			1139+	DC	HL1' 1'	m4 used
00001A80	01			1140+	DC	HL1' 1'	m5 used
00001A81	01			1141+	DC	HL1' 1'	CC
00001A82	0B			1142+	DC	HL1' 11'	CC failed mask
00001A84	00000000 00000000			1143+	DS	2F	extracted PSW after test (has CC)
00001A8C	FF			1144+	DC	X' FF'	extracted CC, if test failed
00001A8D	E5D7D2D3 E2404040			1145+	DC	CL8' VPKLS'	instruction name
00001A98	00001B10			1146+	DC	A(RE13)	address of v1 result
00001A9C	00001B20			1147+	DC	A(RE13+16)	address of v2 source
00001AA0	00001B30			1148+	DC	A(RE13+32)	address of v3 source
00001AA4	00000010			1149+	DC	A(16)	result length
00001AA8	00001B10			1150+REA13	DC	A(RE13)	result address
00001AB0	00000000 00000000			1151+	DS	2FD	gap
00001AB8	00000000 00000000						
00001AC0	00000000 00000000			1152+V1013	DS	XL16	V1 output
00001AC8	00000000 00000000						
00001AD0	00000000 00000000			1153+	DS	2FD	gap
00001AD8	00000000 00000000						
				1154+*			
00001AE0				1155+X13	DS	0F	
00001AE0	E310 5024 0014		00000024	1156+	LGF	R1, V2ADDR	load v2 source
00001AE6	E761 0000 0806		00000000	1157+	VL	v22, 0(R1)	use v21 to test decoder
00001AEC	E310 5028 0014		00000028	1158+	LGF	R1, V3ADDR	load v3 source
00001AF2	E771 0000 0806		00000000	1159+	VL	v23, 0(R1)	use v22 to test decoder
00001AF8	E756 7010 1E95			1160+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001AFE	B98D 0020			1161+	EPSW	R2, R0	extract psw
00001B02	5020 500C		0000000C	1162+	ST	R2, CCPSW	to save CC
00001B06	E750 5048 080E		00001AC0	1163+	VST	V21, V1013	save v1 output
00001B0C	07FB			1164+	BR	R11	return
00001B10				1165+RE13	DC	0F	V1 for this test
00001B10				1166+	DROP	R5	
00001B10	11335577 99BBDDFF			1167	DC	XL16' 1133557799BBDDFF 01FFFFFFF	result
00001B18	01FFFFFF FFFFFFFF						
00001B20	00110033 00550077			1168	DC	XL16' 0011003300550077 009900BB00DD00FF'	v2
00001B28	009900BB 00DD00FF						
00001B30	00010203 04050607			1169	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00001B38	08090A0B 0C0D0E0F						
				1170			
				1171	VRR_B	VPKLS, 1, 3	
00001B40				1172+	DS	0FD	
00001B40		00001B40		1173+	USING	*, R5	base for test data and test routine
00001B40	00001BA8			1174+T14	DC	A(X14)	address of test routine
00001B44	000E			1175+	DC	H' 14'	test number



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001B46	00			1176+	DC	X' 00'	
00001B47	01			1177+	DC	HL1' 1'	m4 used
00001B48	01			1178+	DC	HL1' 1'	m5 used
00001B49	03			1179+	DC	HL1' 3'	CC
00001B4A	0E			1180+	DC	HL1' 14'	CC failed mask
00001B4C	00000000	00000000		1181+	DS	2F	extracted PSW after test (has CC)
00001B54	FF			1182+	DC	X' FF'	extracted CC, if test failed
00001B55	E5D7D2D3	E2404040		1183+	DC	CL8' VPKLS'	instruction name
00001B60	00001BD8			1184+	DC	A(RE14)	address of v1 result
00001B64	00001BE8			1185+	DC	A(RE14+16)	address of v2 source
00001B68	00001BF8			1186+	DC	A(RE14+32)	address of v3 source
00001B6C	00000010			1187+	DC	A(16)	result length
00001B70	00001BD8			1188+REA14	DC	A(RE14)	result address
00001B78	00000000	00000000		1189+	DS	2FD	gap
00001B80	00000000	00000000					
00001B88	00000000	00000000		1190+V1014	DS	XL16	V1 output
00001B90	00000000	00000000					
00001B98	00000000	00000000		1191+	DS	2FD	gap
00001BA0	00000000	00000000					
00001BA8				1192+*			
00001BA8	E310 5024 0014		00000024	1193+X14	DS	0F	
00001BAE	E761 0000 0806		00000000	1194+	LGF	R1, V2ADDR	load v2 source
00001BB4	E310 5028 0014		00000028	1195+	VL	v22, 0(R1)	use v21 to test decoder
00001BBA	E771 0000 0806		00000000	1196+	LGF	R1, V3ADDR	load v3 source
00001BC0	E756 7010 1E95			1197+	VL	v23, 0(R1)	use v22 to test decoder
00001BC6	B98D 0020			1198+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001BCA	5020 500C		0000000C	1199+	EPSW	R2, R0	extract psw
00001BCE	E750 5048 080E		00001B88	1200+	ST	R2, CCPSW	to save CC
00001BD4	07FB			1201+	VST	V21, V1014	save v1 output
00001BD8				1202+	BR	R11	return
00001BD8				1203+RE14	DC	0F	V1 for this test
00001BD8	FFFFFFFF	FFFFFFFF		1204+	DROP	R5	
00001BD8	FFFFFFFF	FFFFFFFF		1205	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00001BE0	FFFFFFFF	FFFFFFFF					
00001BE8	01110133	01550177		1206	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00001BF0	019901BB	01DD01FF					
00001BF8	01010203	04050607		1207	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
00001C00	08090A0B	0C0D0E0F					
00001C08				1208			
00001C08				1209	VRR_B	VPKLS, 1, 3	
00001C08		00001C08		1210+	DS	0FD	
00001C08	00001C70			1211+	USING	*, R5	base for test data and test routine
00001C0C	000F			1212+T15	DC	A(X15)	address of test routine
00001C0E	00			1213+	DC	H' 15'	test number
00001C0F	01			1214+	DC	X' 00'	
00001C10	01			1215+	DC	HL1' 1'	m4 used
00001C11	03			1216+	DC	HL1' 1'	m5 used
00001C12	0E			1217+	DC	HL1' 3'	CC
00001C14	00000000	00000000		1218+	DC	HL1' 14'	CC failed mask
00001C1C	FF			1219+	DS	2F	extracted PSW after test (has CC)
00001C1D	E5D7D2D3	E2404040		1220+	DC	X' FF'	extracted CC, if test failed
00001C28	00001CA0			1221+	DC	CL8' VPKLS'	instruction name
00001C2C	00001CB0			1222+	DC	A(RE15)	address of v1 result
00001C30	00001CC0			1223+	DC	A(RE15+16)	address of v2 source
00001C34	00000010			1224+	DC	A(RE15+32)	address of v3 source
				1225+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001C38	00001CA0			1226+REA15	DC	A(RE15)	result address
00001C40	00000000 00000000			1227+	DS	2FD	gap
00001C48	00000000 00000000						
00001C50	00000000 00000000			1228+V1015	DS	XL16	V1 output
00001C58	00000000 00000000						
00001C60	00000000 00000000			1229+	DS	2FD	gap
00001C68	00000000 00000000						
				1230+*			
00001C70				1231+X15	DS	0F	
00001C70	E310 5024 0014		00000024	1232+	LGF	R1, V2ADDR	load v2 source
00001C76	E761 0000 0806		00000000	1233+	VL	v22, 0(R1)	use v21 to test decoder
00001C7C	E310 5028 0014		00000028	1234+	LGF	R1, V3ADDR	load v3 source
00001C82	E771 0000 0806		00000000	1235+	VL	v23, 0(R1)	use v22 to test decoder
00001C88	E756 7010 1E95			1236+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001C8E	B98D 0020			1237+	EPSW	R2, R0	extract psw
00001C92	5020 500C		0000000C	1238+	ST	R2, CCPSW	to save CC
00001C96	E750 5048 080E		00001C50	1239+	VST	V21, V1015	save v1 output
00001C9C	07FB			1240+	BR	R11	return
00001CA0				1241+RE15	DC	0F	V1 for this test
00001CA0				1242+	DROP	R5	
00001CA0	FFFFFFFF FFFFFFFF			1243	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00001CA8	FFFFFFFF FFFFFFFF						
00001CB0	01010203 04050607			1244	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
00001CB8	08090A0B 0C0D0E0F						
00001CC0	01110133 01550177			1245	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00001CC8	019901BB 01DD01FF						
				1246			
				1247 *Word			
				1248	VRR_B	VPKLS, 2, 0	
00001CD0				1249+	DS	0FD	
00001CD0		00001CD0		1250+	USING	*, R5	base for test data and test routine
00001CD0	00001D38			1251+T16	DC	A(X16)	address of test routine
00001CD4	0010			1252+	DC	H' 16'	test number
00001CD6	00			1253+	DC	X' 00'	
00001CD7	02			1254+	DC	HL1' 2'	m4 used
00001CD8	01			1255+	DC	HL1' 1'	m5 used
00001CD9	00			1256+	DC	HL1' 0'	CC
00001CDA	07			1257+	DC	HL1' 7'	CC failed mask
00001CDC	00000000 00000000			1258+	DS	2F	extracted PSW after test (has CC)
00001CE4	FF			1259+	DC	X' FF'	extracted CC, if test failed
00001CE5	E5D7D2D3 E2404040			1260+	DC	CL8' VPKLS'	instruction name
00001CF0	00001D68			1261+	DC	A(RE16)	address of v1 result
00001CF4	00001D78			1262+	DC	A(RE16+16)	address of v2 source
00001CF8	00001D88			1263+	DC	A(RE16+32)	address of v3 source
00001CFC	00000010			1264+	DC	A(16)	result length
00001D00	00001D68			1265+REA16	DC	A(RE16)	result address
00001D08	00000000 00000000			1266+	DS	2FD	gap
00001D10	00000000 00000000						
00001D18	00000000 00000000			1267+V1016	DS	XL16	V1 output
00001D20	00000000 00000000						
00001D28	00000000 00000000			1268+	DS	2FD	gap
00001D30	00000000 00000000						
				1269+*			
00001D38				1270+X16	DS	0F	
00001D38	E310 5024 0014		00000024	1271+	LGF	R1, V2ADDR	load v2 source
00001D3E	E761 0000 0806		00000000	1272+	VL	v22, 0(R1)	use v21 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001D44	E310 5028 0014		00000028	1273+	LGF	R1, V3ADDR	load v3 source
00001D4A	E771 0000 0806		00000000	1274+	VL	v23, 0(R1)	use v22 to test decoder
00001D50	E756 7010 2E95			1275+	VPKLS	V21, V22, V23, 2, 1	test instruction
00001D56	B98D 0020			1276+	EPSW	R2, R0	extract psw
00001D5A	5020 500C		0000000C	1277+	ST	R2, CCPSW	to save CC
00001D5E	E750 5048 080E		00001D18	1278+	VST	V21, V1016	save v1 output
00001D64	07FB			1279+	BR	R11	return
00001D68				1280+RE16	DC	0F	V1 for this test
00001D68				1281+	DROP	R5	
00001D68	11335577 99BBDDFF			1282	DC	XL16' 1133557799BBDDFF FEFDFCFBFAF9F8F7'	result t
00001D70	FEFDFCFB FAF9F8F7						
00001D78	00001133 00005577			1283	DC	XL16' 0000113300005577 000099BB0000DDFF'	v2
00001D80	000099BB 0000DDFF						
00001D88	0000FEFD 0000FCFB			1284	DC	XL16' 0000FEFD0000FCFB 0000FAF90000F8F7'	v3
00001D90	0000FAF9 0000F8F7						
				1285			
				1286	VRR_B	VPKLS, 2, 0	
00001D98				1287+	DS	0FD	
00001D98		00001D98		1288+	USING	*, R5	base for test data and test routine
00001D98	00001E00			1289+T17	DC	A(X17)	address of test routine
00001D9C	0011			1290+	DC	H' 17'	test number
00001D9E	00			1291+	DC	X' 00'	
00001D9F	02			1292+	DC	HL1' 2'	m4 used
00001DA0	01			1293+	DC	HL1' 1'	m5 used
00001DA1	00			1294+	DC	HL1' 0'	CC
00001DA2	07			1295+	DC	HL1' 7'	CC failed mask
00001DA4	00000000 00000000			1296+	DS	2F	extracted PSW after test (has CC)
00001DAC	FF			1297+	DC	X' FF'	extracted CC, if test failed
00001DAD	E5D7D2D3 E2404040			1298+	DC	CL8' VPKLS'	instruction name
00001DB8	00001E30			1299+	DC	A(RE17)	address of v1 result
00001DBC	00001E40			1300+	DC	A(RE17+16)	address of v2 source
00001DC0	00001E50			1301+	DC	A(RE17+32)	address of v3 source
00001DC4	00000010			1302+	DC	A(16)	result length
00001DC8	00001E30			1303+REA17	DC	A(RE17)	result address
00001DD0	00000000 00000000			1304+	DS	2FD	gap
00001DD8	00000000 00000000						
00001DE0	00000000 00000000			1305+V1017	DS	XL16	V1 output
00001DE8	00000000 00000000						
00001DF0	00000000 00000000			1306+	DS	2FD	gap
00001DF8	00000000 00000000						
				1307+*			
00001E00				1308+X17	DS	0F	
00001E00	E310 5024 0014		00000024	1309+	LGF	R1, V2ADDR	load v2 source
00001E06	E761 0000 0806		00000000	1310+	VL	v22, 0(R1)	use v21 to test decoder
00001E0C	E310 5028 0014		00000028	1311+	LGF	R1, V3ADDR	load v3 source
00001E12	E771 0000 0806		00000000	1312+	VL	v23, 0(R1)	use v22 to test decoder
00001E18	E756 7010 2E95			1313+	VPKLS	V21, V22, V23, 2, 1	test instruction
00001E1E	B98D 0020			1314+	EPSW	R2, R0	extract psw
00001E22	5020 500C		0000000C	1315+	ST	R2, CCPSW	to save CC
00001E26	E750 5048 080E		00001DE0	1316+	VST	V21, V1017	save v1 output
00001E2C	07FB			1317+	BR	R11	return
00001E30				1318+RE17	DC	0F	V1 for this test
00001E30				1319+	DROP	R5	
00001E30	FEFDFCFB FAF9F8F7			1320	DC	XL16' FEFDFCFBFAF9F8F7 1133557799BBDDFF'	result t
00001E38	11335577 99BBDDFF						
00001E40	0000FEFD 0000FCFB			1321	DC	XL16' 0000FEFD0000FCFB 0000FAF90000F8F7'	v2



LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001E48	0000FAF9	0000F8F7						
00001E50	00001133	00005577		1322	DC	XL16'	0000113300005577 000099BB0000DDFF'	v3
00001E58	000099BB	0000DDFF						
				1323				
				1324	VRR_B	VPKLS, 2, 1		
00001E60				1325+	DS	0FD		
00001E60		00001E60		1326+	USING	*, R5	base for test data and test routine	
00001E60	00001EC8			1327+T18	DC	A(X18)	address of test routine	
00001E64	0012			1328+	DC	H' 18'	test number	
00001E66	00			1329+	DC	X' 00'		
00001E67	02			1330+	DC	HL1' 2'	m4 used	
00001E68	01			1331+	DC	HL1' 1'	m5 used	
00001E69	01			1332+	DC	HL1' 1'	CC	
00001E6A	0B			1333+	DC	HL1' 11'	CC failed mask	
00001E6C	00000000	00000000		1334+	DS	2F	extracted PSW after test (has CC)	
00001E74	FF			1335+	DC	X' FF'	extracted CC, if test failed	
00001E75	E5D7D2D3	E2404040		1336+	DC	CL8' VPKLS'	instruction name	
00001E80	00001EF8			1337+	DC	A(RE18)	address of v1 result	
00001E84	00001F08			1338+	DC	A(RE18+16)	address of v2 source	
00001E88	00001F18			1339+	DC	A(RE18+32)	address of v3 source	
00001E8C	00000010			1340+	DC	A(16)	result length	
00001E90	00001EF8			1341+REA18	DC	A(RE18)	result address	
00001E98	00000000	00000000		1342+	DS	2FD	gap	
00001EA0	00000000	00000000						
00001EA8	00000000	00000000		1343+V1018	DS	XL16	V1 output	
00001EB0	00000000	00000000						
00001EB8	00000000	00000000		1344+	DS	2FD	gap	
00001EC0	00000000	00000000						
				1345+*				
00001EC8				1346+X18	DS	0F		
00001EC8	E310 5024 0014		00000024	1347+	LGF	R1, V2ADDR	load v2 source	
00001ECE	E761 0000 0806		00000000	1348+	VL	v22, 0(R1)	use v21 to test decoder	
00001ED4	E310 5028 0014		00000028	1349+	LGF	R1, V3ADDR	load v3 source	
00001EDA	E771 0000 0806		00000000	1350+	VL	v23, 0(R1)	use v22 to test decoder	
00001EE0	E756 7010 2E95			1351+	VPKLS	V21, V22, V23, 2, 1	test instruction	
00001EE6	B98D 0020			1352+	EPSW	R2, R0	extract psw	
00001EEA	5020 500C		0000000C	1353+	ST	R2, CCPSW	to save CC	
00001EEE	E750 5048 080E		00001EA8	1354+	VST	V21, V1018	save v1 output	
00001EF4	07FB			1355+	BR	R11	return	
00001EF8				1356+RE18	DC	0F	V1 for this test	
00001EF8				1357+	DROP	R5		
00001EF8	1203FFFF	FFFFFFFF		1358	DC	XL16' 1203FFFFFFFFFFFFFFFF 1133557799BBDDFF'	result t	
00001F00	11335577	99BBDDFF						
00001F08	00001203	04050607		1359	DC	XL16' 0000120304050607 08090A0B0C0D0E0F'	v2	
00001F10	08090A0B	0C0D0E0F						
00001F18	00001133	00005577		1360	DC	XL16' 0000113300005577 000099BB0000DDFF'	v3	
00001F20	000099BB	0000DDFF						
				1361				
				1362	VRR_B	VPKLS, 2, 1		
00001F28				1363+	DS	0FD		
00001F28		00001F28		1364+	USING	*, R5	base for test data and test routine	
00001F28	00001F90			1365+T19	DC	A(X19)	address of test routine	
00001F2C	0013			1366+	DC	H' 19'	test number	
00001F2E	00			1367+	DC	X' 00'		
00001F2F	02			1368+	DC	HL1' 2'	m4 used	
00001F30	01			1369+	DC	HL1' 1'	m5 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001F31	01			1370+	DC	HL1' 1'	CC
00001F32	0B			1371+	DC	HL1' 11'	CC failed mask
00001F34	00000000 00000000			1372+	DS	2F	extracted PSW after test (has CC)
00001F3C	FF			1373+	DC	X' FF'	extracted CC, if test failed
00001F3D	E5D7D2D3 E2404040			1374+	DC	CL8' VPKLS'	instruction name
00001F48	00001FC0			1375+	DC	A(RE19)	address of v1 result
00001F4C	00001FD0			1376+	DC	A(RE19+16)	address of v2 source
00001F50	00001FE0			1377+	DC	A(RE19+32)	address of v3 source
00001F54	00000010			1378+	DC	A(16)	result length
00001F58	00001FC0			1379+REA19	DC	A(RE19)	result address
00001F60	00000000 00000000			1380+	DS	2FD	gap
00001F68	00000000 00000000						
00001F70	00000000 00000000			1381+V1019	DS	XL16	V1 output
00001F78	00000000 00000000						
00001F80	00000000 00000000			1382+	DS	2FD	gap
00001F88	00000000 00000000						
				1383+*			
00001F90				1384+X19	DS	0F	
00001F90	E310 5024 0014		00000024	1385+	LGF	R1, V2ADDR	load v2 source
00001F96	E761 0000 0806		00000000	1386+	VL	v22, 0(R1)	use v21 to test decoder
00001F9C	E310 5028 0014		00000028	1387+	LGF	R1, V3ADDR	load v3 source
00001FA2	E771 0000 0806		00000000	1388+	VL	v23, 0(R1)	use v22 to test decoder
00001FA8	E756 7010 2E95			1389+	VPKLS	V21, V22, V23, 2, 1	test instruction
00001FAE	B98D 0020			1390+	EPSW	R2, R0	extract psw
00001FB2	5020 500C		0000000C	1391+	ST	R2, CCPSW	to save CC
00001FB6	E750 5048 080E		00001F70	1392+	VST	V21, V1019	save v1 output
00001FBC	07FB			1393+	BR	R11	return
00001FC0				1394+RE19	DC	0F	V1 for this test
00001FC0				1395+	DROP	R5	
00001FC0	11335577 99BBDDFF			1396	DC	XL16' 1133557799BBDDFF 1203FFFFFFFFFFFFFF'	result
00001FC8	1203FFFF FFFFFFFF						
00001FD0	00001133 00005577			1397	DC	XL16' 0000113300005577 000099BB0000DDFF'	v2
00001FD8	000099BB 0000DDFF						
00001FE0	00001203 04050607			1398	DC	XL16' 0000120304050607 08090A0B0C0D0E0F'	v3
00001FE8	08090A0B 0C0D0E0F						
				1399			
00001FF0				1400	VRR_B	VPKLS, 2, 3	
00001FF0		00001FF0		1401+	DS	0FD	
00001FF0	00002058			1402+	USING	*, R5	base for test data and test routine
00001FF4	0014			1403+T20	DC	A(X20)	address of test routine
00001FF6	00			1404+	DC	H' 20'	test number
00001FF7	02			1405+	DC	X' 00'	
00001FF8	01			1406+	DC	HL1' 2'	m4 used
00001FF9	03			1407+	DC	HL1' 1'	m5 used
00001FFA	0E			1408+	DC	HL1' 3'	CC
00001FFC	00000000 00000000			1409+	DC	HL1' 14'	CC failed mask
00002004	FF			1410+	DS	2F	extracted PSW after test (has CC)
00002005	E5D7D2D3 E2404040			1411+	DC	X' FF'	extracted CC, if test failed
00002010	00002088			1412+	DC	CL8' VPKLS'	instruction name
00002014	00002098			1413+	DC	A(RE20)	address of v1 result
00002018	000020A8			1414+	DC	A(RE20+16)	address of v2 source
0000201C	00000010			1415+	DC	A(RE20+32)	address of v3 source
00002020	00002088			1416+	DC	A(16)	result length
00002028	00000000 00000000			1417+REA20	DC	A(RE20)	result address
00002030	00000000 00000000			1418+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002038	00000000 00000000			1419+V1020	DS	XL16	V1 output
00002040	00000000 00000000						
00002048	00000000 00000000			1420+	DS	2FD	gap
00002050	00000000 00000000						
				1421+*			
00002058				1422+X20	DS	0F	
00002058	E310 5024 0014		00000024	1423+	LGF	R1, V2ADDR	load v2 source
0000205E	E761 0000 0806		00000000	1424+	VL	v22, 0(R1)	use v21 to test decoder
00002064	E310 5028 0014		00000028	1425+	LGF	R1, V3ADDR	load v3 source
0000206A	E771 0000 0806		00000000	1426+	VL	v23, 0(R1)	use v22 to test decoder
00002070	E756 7010 2E95			1427+	VPKLS	V21, V22, V23, 2, 1	test instruction
00002076	B98D 0020			1428+	EPSW	R2, R0	extract psw
0000207A	5020 500C		0000000C	1429+	ST	R2, CCPSW	to save CC
0000207E	E750 5048 080E		00002038	1430+	VST	V21, V1020	save v1 output
00002084	07FB			1431+	BR	R11	return
00002088				1432+RE20	DC	0F	V1 for this test
00002088				1433+	DROP	R5	
00002088	FFFFFFFF FFFFFFFF			1434	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00002090	FFFFFFFF FFFFFFFF						
00002098	01110133 01550177			1435	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
000020A0	019901BB 01DD01FF						
000020A8	01010203 04050607			1436	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
000020B0	08090A0B 0C0D0E0F						
				1437			
				1438	VRR_B	VPKLS, 2, 3	
000020B8				1439+	DS	0FD	
000020B8		000020B8		1440+	USING	*, R5	base for test data and test routine
000020B8	00002120			1441+T21	DC	A(X21)	address of test routine
000020BC	0015			1442+	DC	H' 21'	test number
000020BE	00			1443+	DC	X' 00'	
000020BF	02			1444+	DC	HL1' 2'	m4 used
000020C0	01			1445+	DC	HL1' 1'	m5 used
000020C1	03			1446+	DC	HL1' 3'	CC
000020C2	0E			1447+	DC	HL1' 14'	CC failed mask
000020C4	00000000 00000000			1448+	DS	2F	extracted PSW after test (has CC)
000020CC	FF			1449+	DC	X' FF'	extracted CC, if test failed
000020CD	E5D7D2D3 E2404040			1450+	DC	CL8' VPKLS'	instruction name
000020D8	00002150			1451+	DC	A(RE21)	address of v1 result
000020DC	00002160			1452+	DC	A(RE21+16)	address of v2 source
000020E0	00002170			1453+	DC	A(RE21+32)	address of v3 source
000020E4	00000010			1454+	DC	A(16)	result length
000020E8	00002150			1455+REA21	DC	A(RE21)	result address
000020F0	00000000 00000000			1456+	DS	2FD	gap
000020F8	00000000 00000000						
00002100	00000000 00000000			1457+V1021	DS	XL16	V1 output
00002108	00000000 00000000						
00002110	00000000 00000000			1458+	DS	2FD	gap
00002118	00000000 00000000						
				1459+*			
00002120				1460+X21	DS	0F	
00002120	E310 5024 0014		00000024	1461+	LGF	R1, V2ADDR	load v2 source
00002126	E761 0000 0806		00000000	1462+	VL	v22, 0(R1)	use v21 to test decoder
0000212C	E310 5028 0014		00000028	1463+	LGF	R1, V3ADDR	load v3 source
00002132	E771 0000 0806		00000000	1464+	VL	v23, 0(R1)	use v22 to test decoder
00002138	E756 7010 2E95			1465+	VPKLS	V21, V22, V23, 2, 1	test instruction
0000213E	B98D 0020			1466+	EPSW	R2, R0	extract psw

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002142	5020 500C		0000000C	1467+	ST	R2, CCPSW	to save CC	
00002146	E750 5048 080E		00002100	1468+	VST	V21, V1021	save v1 output	
0000214C	07FB			1469+	BR	R11	return	
00002150				1470+RE21	DC	0F	V1 for this test	
00002150				1471+	DROP	R5		
00002150	FFFFFFFF FFFFFFFF			1472	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00002158	FFFFFFFF FFFFFFFF							
00002160	01010203 04050607			1473	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2	
00002168	08090A0B 0C0D0E0F							
00002170	01110133 01550177			1474	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3	
00002178	019901BB 01DD01FF							
				1475				
				1476 *Doubleword				
				1477	VRR_B	VPKLS, 3, 0		
00002180				1478+	DS	0FD		
00002180		00002180		1479+	USING	*, R5	base for test data and test routine	
00002180	000021E8			1480+T22	DC	A(X22)	address of test routine	
00002184	0016			1481+	DC	H' 22'	test number	
00002186	00			1482+	DC	X' 00'		
00002187	03			1483+	DC	HL1' 3'	m4 used	
00002188	01			1484+	DC	HL1' 1'	m5 used	
00002189	00			1485+	DC	HL1' 0'	CC	
0000218A	07			1486+	DC	HL1' 7'	CC failed mask	
0000218C	00000000 00000000			1487+	DS	2F	extracted PSW after test (has CC)	
00002194	FF			1488+	DC	X' FF'	extracted CC, if test failed	
00002195	E5D7D2D3 E2404040			1489+	DC	CL8' VPKLS'	instruction name	
000021A0	00002218			1490+	DC	A(RE22)	address of v1 result	
000021A4	00002228			1491+	DC	A(RE22+16)	address of v2 source	
000021A8	00002238			1492+	DC	A(RE22+32)	address of v3 source	
000021AC	00000010			1493+	DC	A(16)	result length	
000021B0	00002218			1494+REA22	DC	A(RE22)	result address	
000021B8	00000000 00000000			1495+	DS	2FD	gap	
000021C0	00000000 00000000							
000021C8	00000000 00000000			1496+V1022	DS	XL16	V1 output	
000021D0	00000000 00000000							
000021D8	00000000 00000000			1497+	DS	2FD	gap	
000021E0	00000000 00000000							
				1498+*				
000021E8				1499+X22	DS	0F		
000021E8	E310 5024 0014		00000024	1500+	LGF	R1, V2ADDR	load v2 source	
000021EE	E761 0000 0806		00000000	1501+	VL	v22, 0(R1)	use v21 to test decoder	
000021F4	E310 5028 0014		00000028	1502+	LGF	R1, V3ADDR	load v3 source	
000021FA	E771 0000 0806		00000000	1503+	VL	v23, 0(R1)	use v22 to test decoder	
00002200	E756 7010 3E95			1504+	VPKLS	V21, V22, V23, 3, 1	test instruction	
00002206	B98D 0020			1505+	EPSW	R2, R0	extract psw	
0000220A	5020 500C		0000000C	1506+	ST	R2, CCPSW	to save CC	
0000220E	E750 5048 080E		000021C8	1507+	VST	V21, V1022	save v1 output	
00002214	07FB			1508+	BR	R11	return	
00002218				1509+RE22	DC	0F	V1 for this test	
00002218				1510+	DROP	R5		
00002218	11335577 99BBDDFF			1511	DC	XL16' 1133557799BBDDFF FEFDFCFBFAF9F8F7'	result t	
00002220	FEFDFCFB FAF9F8F7							
00002228	00000000 11335577			1512	DC	XL16' 0000000011335577 0000000099BBDDFF'	v2	
00002230	00000000 99BBDDFF							
00002238	00000000 FEFDFCFB			1513	DC	XL16' 00000000FEFDFCFB 00000000FAF9F8F7'	v3	
00002240	00000000 FAF9F8F7							



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				1514			
				1515	VRR_B	VPKLS, 3, 0	
00002248				1516+	DS	0FD	
00002248		00002248		1517+	USING	*, R5	base for test data and test routine
00002248	000022B0			1518+T23	DC	A(X23)	address of test routine
0000224C	0017			1519+	DC	H' 23'	test number
0000224E	00			1520+	DC	X' 00'	
0000224F	03			1521+	DC	HL1' 3'	m4 used
00002250	01			1522+	DC	HL1' 1'	m5 used
00002251	00			1523+	DC	HL1' 0'	CC
00002252	07			1524+	DC	HL1' 7'	CC failed mask
00002254	00000000 00000000			1525+	DS	2F	extracted PSW after test (has CC)
0000225C	FF			1526+	DC	X' FF'	extracted CC, if test failed
0000225D	E5D7D2D3 E2404040			1527+	DC	CL8' VPKLS'	instruction name
00002268	000022E0			1528+	DC	A(RE23)	address of v1 result
0000226C	000022F0			1529+	DC	A(RE23+16)	address of v2 source
00002270	00002300			1530+	DC	A(RE23+32)	address of v3 source
00002274	00000010			1531+	DC	A(16)	result length
00002278	000022E0			1532+REA23	DC	A(RE23)	result address
00002280	00000000 00000000			1533+	DS	2FD	gap
00002288	00000000 00000000						
00002290	00000000 00000000			1534+V1023	DS	XL16	V1 output
00002298	00000000 00000000						
000022A0	00000000 00000000			1535+	DS	2FD	gap
000022A8	00000000 00000000						
				1536+*			
000022B0				1537+X23	DS	0F	
000022B0	E310 5024 0014		00000024	1538+	LGF	R1, V2ADDR	load v2 source
000022B6	E761 0000 0806		00000000	1539+	VL	v22, 0(R1)	use v21 to test decoder
000022BC	E310 5028 0014		00000028	1540+	LGF	R1, V3ADDR	load v3 source
000022C2	E771 0000 0806		00000000	1541+	VL	v23, 0(R1)	use v22 to test decoder
000022C8	E756 7010 3E95			1542+	VPKLS	V21, V22, V23, 3, 1	test instruction
000022CE	B98D 0020			1543+	EPSW	R2, R0	extract psw
000022D2	5020 500C		0000000C	1544+	ST	R2, CCPSW	to save CC
000022D6	E750 5048 080E		00002290	1545+	VST	V21, V1023	save v1 output
000022DC	07FB			1546+	BR	R11	return
000022E0				1547+RE23	DC	0F	V1 for this test
000022E0				1548+	DROP	R5	
000022E0	FEFDFCFB FAF9F8F7			1549	DC	XL16' FEFDFCFBFAF9F8F7 1133557799BBDDFF'	result t
000022E8	11335577 99BBDDFF						
000022F0	00000000 FEFDFCFB			1550	DC	XL16' 00000000FEFDFCFB 00000000FAF9F8F7'	v2
000022F8	00000000 FAF9F8F7						
00002300	00000000 11335577			1551	DC	XL16' 0000000011335577 0000000099BBDDFF'	v3
00002308	00000000 99BBDDFF						
				1552			
				1553	VRR_B	VPKLS, 3, 1	
00002310				1554+	DS	0FD	
00002310		00002310		1555+	USING	*, R5	base for test data and test routine
00002310	00002378			1556+T24	DC	A(X24)	address of test routine
00002314	0018			1557+	DC	H' 24'	test number
00002316	00			1558+	DC	X' 00'	
00002317	03			1559+	DC	HL1' 3'	m4 used
00002318	01			1560+	DC	HL1' 1'	m5 used
00002319	01			1561+	DC	HL1' 1'	CC
0000231A	0B			1562+	DC	HL1' 11'	CC failed mask
0000231C	00000000 00000000			1563+	DS	2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002324	FF			1564+	DC	X' FF'	extracted CC, if test failed
00002325	E5D7D2D3 E2404040			1565+	DC	CL8' VPKLS'	instruction name
00002330	000023A8			1566+	DC	A(RE24)	address of v1 result
00002334	000023B8			1567+	DC	A(RE24+16)	address of v2 source
00002338	000023C8			1568+	DC	A(RE24+32)	address of v3 source
0000233C	00000010			1569+	DC	A(16)	result length
00002340	000023A8			1570+REA24	DC	A(RE24)	result address
00002348	00000000 00000000			1571+	DS	2FD	gap
00002350	00000000 00000000						
00002358	00000000 00000000			1572+V1024	DS	XL16	V1 output
00002360	00000000 00000000						
00002368	00000000 00000000			1573+	DS	2FD	gap
00002370	00000000 00000000						
00002378				1574+*			
00002378	E310 5024 0014		00000024	1575+X24	DS	0F	
0000237E	E761 0000 0806		00000000	1576+	LGF	R1, V2ADDR	load v2 source
00002384	E310 5028 0014		00000028	1577+	VL	v22, 0(R1)	use v21 to test decoder
0000238A	E771 0000 0806		00000000	1578+	LGF	R1, V3ADDR	load v3 source
00002390	E756 7010 3E95			1579+	VL	v23, 0(R1)	use v22 to test decoder
00002396	B98D 0020			1580+	VPKLS	V21, V22, V23, 3, 1	test instruction
0000239A	5020 500C		0000000C	1581+	EPSW	R2, R0	extract psw
0000239E	E750 5048 080E		00002358	1582+	ST	R2, CCPSW	to save CC
000023A4	07FB			1583+	VST	V21, V1024	save v1 output
000023A8				1584+	BR	R11	return
000023A8				1585+RE24	DC	0F	V1 for this test
000023A8				1586+	DROP	R5	
000023A8	FEFDFCFB FAF9F8F7			1587	DC	XL16' FEFDFCFBFAF9F8F7 FFFFFFFFFFFFFFFFFF'	result t
000023B0	FFFFFFFF FFFFFFFF						
000023B8	00000000 FEFDFCFB			1588	DC	XL16' 00000000FEFDFCFB 00000000FAF9F8F7'	v2
000023C0	00000000 FAF9F8F7						
000023C8	00001133 00005577			1589	DC	XL16' 0000113300005577 000099BB0000DDFF'	v3
000023D0	000099BB 0000DDFF						
000023D8				1590			
000023D8				1591	VRR_B	VPKLS, 3, 1	
000023D8		000023D8		1592+	DS	0FD	
000023D8	00002440			1593+	USING	*, R5	base for test data and test routine
000023DC	0019			1594+T25	DC	A(X25)	address of test routine
000023DE	00			1595+	DC	H' 25'	test number
000023DF	03			1596+	DC	X' 00'	
000023E0	01			1597+	DC	HL1' 3'	m4 used
000023E1	01			1598+	DC	HL1' 1'	m5 used
000023E2	0B			1599+	DC	HL1' 1'	CC
000023E4	00000000 00000000			1600+	DC	HL1' 11'	CC failed mask
000023EC	FF			1601+	DS	2F	extracted PSW after test (has CC)
000023ED	E5D7D2D3 E2404040			1602+	DC	X' FF'	extracted CC, if test failed
000023F8	00002470			1603+	DC	CL8' VPKLS'	instruction name
000023FC	00002480			1604+	DC	A(RE25)	address of v1 result
00002400	00002490			1605+	DC	A(RE25+16)	address of v2 source
00002404	00000010			1606+	DC	A(RE25+32)	address of v3 source
00002408	00002470			1607+	DC	A(16)	result length
00002410	00000000 00000000			1608+REA25	DC	A(RE25)	result address
00002418	00000000 00000000			1609+	DS	2FD	gap
00002420	00000000 00000000			1610+V1025	DS	XL16	V1 output
00002428	00000000 00000000						
00002430	00000000 00000000			1611+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002438	00000000 00000000			1612+*				
00002440				1613+X25	DS	0F		
00002440	E310 5024 0014		00000024	1614+	LGF	R1, V2ADDR	load v2 source	
00002446	E761 0000 0806		00000000	1615+	VL	v22, 0(R1)	use v21 to test decoder	
0000244C	E310 5028 0014		00000028	1616+	LGF	R1, V3ADDR	load v3 source	
00002452	E771 0000 0806		00000000	1617+	VL	v23, 0(R1)	use v22 to test decoder	
00002458	E756 7010 3E95			1618+	VPKLS	V21, V22, V23, 3, 1	test instruction	
0000245E	B98D 0020			1619+	EPSW	R2, R0	extract psw	
00002462	5020 500C		0000000C	1620+	ST	R2, CCPSW	to save CC	
00002466	E750 5048 080E		00002420	1621+	VST	V21, V1025	save v1 output	
0000246C	07FB			1622+	BR	R11	return	
00002470				1623+RE25	DC	0F	V1 for this test	
00002470				1624+	DROP	R5		
00002470	FFFFFFFF FFFFFFFF			1625	DC	XL16' FFFFFFFFFFFFFFFFFF FEFD FCFBFAF9F8F7'	result t	
00002478	FEFD FCFB FAF9F8F7							
00002480	00001133 00005577			1626	DC	XL16' 0000113300005577 000099BB0000DDFF'	v2	
00002488	000099BB 0000DDFF							
00002490	00000000 FEFD FCFB			1627	DC	XL16' 00000000FEFD FCFB 00000000FAF9F8F7'	v3	
00002498	00000000 FAF9F8F7							
				1628				
000024A0				1629	VRR_B	VPKLS, 3, 3		
000024A0		000024A0		1630+	DS	0FD		
000024A0	00002508			1631+	USING	*, R5	base for test data and test routine	
000024A4	001A			1632+T26	DC	A(X26)	address of test routine	
000024A6	00			1633+	DC	H' 26'	test number	
000024A7	03			1634+	DC	X' 00'		
000024A8	01			1635+	DC	HL1' 3'	m4 used	
000024A9	03			1636+	DC	HL1' 1'	m5 used	
000024AA	0E			1637+	DC	HL1' 3'	CC	
000024AC	00000000 00000000			1638+	DC	HL1' 14'	CC failed mask	
000024B4	FF			1639+	DS	2F	extracted PSW after test (has CC)	
000024B5	E5D7D2D3 E2404040			1640+	DC	X' FF'	extracted CC, if test failed	
000024C0	00002538			1641+	DC	CL8' VPKLS'	instruction name	
000024C4	00002548			1642+	DC	A(RE26)	address of v1 result	
000024C8	00002558			1643+	DC	A(RE26+16)	address of v2 source	
000024CC	00000010			1644+	DC	A(RE26+32)	address of v3 source	
000024D0	00002538			1645+	DC	A(16)	result length	
000024D8	00000000 00000000			1646+REA26	DC	A(RE26)	result address	
000024E0	00000000 00000000			1647+	DS	2FD	gap	
000024E8	00000000 00000000			1648+V1026	DS	XL16	V1 output	
000024F0	00000000 00000000							
000024F8	00000000 00000000			1649+	DS	2FD	gap	
00002500	00000000 00000000							
				1650+*				
00002508				1651+X26	DS	0F		
00002508	E310 5024 0014		00000024	1652+	LGF	R1, V2ADDR	load v2 source	
0000250E	E761 0000 0806		00000000	1653+	VL	v22, 0(R1)	use v21 to test decoder	
00002514	E310 5028 0014		00000028	1654+	LGF	R1, V3ADDR	load v3 source	
0000251A	E771 0000 0806		00000000	1655+	VL	v23, 0(R1)	use v22 to test decoder	
00002520	E756 7010 3E95			1656+	VPKLS	V21, V22, V23, 3, 1	test instruction	
00002526	B98D 0020			1657+	EPSW	R2, R0	extract psw	
0000252A	5020 500C		0000000C	1658+	ST	R2, CCPSW	to save CC	
0000252E	E750 5048 080E		000024E8	1659+	VST	V21, V1026	save v1 output	
00002534	07FB			1660+	BR	R11	return	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002538				1661+RE26	DC	0F	V1 for this test
00002538				1662+	DROP	R5	
00002538	FFFFFFFF FFFFFFFF			1663	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00002540	FFFFFFFF FFFFFFFF						
00002548	01110133 01550177			1664	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00002550	019901BB 01DD01FF						
00002558	01010203 04050607			1665	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
00002560	08090A0B 0C0D0E0F						
				1666			
00002568				1667	VRR_B	VPKLS, 3, 3	
00002568		00002568		1668+	DS	0FD	
00002568	000025D0			1669+	USING	*, R5	base for test data and test routine
0000256C	001B			1670+T27	DC	A(X27)	address of test routine
0000256E	00			1671+	DC	H' 27'	test number
0000256F	03			1672+	DC	X' 00'	
00002570	01			1673+	DC	HL1' 3'	m4 used
00002571	03			1674+	DC	HL1' 1'	m5 used
00002572	0E			1675+	DC	HL1' 3'	CC
00002574	00000000 00000000			1676+	DC	HL1' 14'	CC failed mask
0000257C	FF			1677+	DS	2F	extracted PSW after test (has CC)
0000257D	E5D7D2D3 E2404040			1678+	DC	X' FF'	extracted CC, if test failed
00002588	00002600			1679+	DC	CL8' VPKLS'	instruction name
0000258C	00002610			1680+	DC	A(RE27)	address of v1 result
00002590	00002620			1681+	DC	A(RE27+16)	address of v2 source
00002594	00000010			1682+	DC	A(RE27+32)	address of v3 source
00002598	00002600			1683+	DC	A(16)	result length
000025A0	00000000 00000000			1684+REA27	DC	A(RE27)	result address
000025A8	00000000 00000000			1685+	DS	2FD	gap
000025B0	00000000 00000000			1686+V1027	DS	XL16	V1 output
000025B8	00000000 00000000						
000025C0	00000000 00000000			1687+	DS	2FD	gap
000025C8	00000000 00000000						
				1688+*			
000025D0				1689+X27	DS	0F	
000025D0	E310 5024 0014		00000024	1690+	LGF	R1, V2ADDR	load v2 source
000025D6	E761 0000 0806		00000000	1691+	VL	v22, 0(R1)	use v21 to test decoder
000025DC	E310 5028 0014		00000028	1692+	LGF	R1, V3ADDR	load v3 source
000025E2	E771 0000 0806		00000000	1693+	VL	v23, 0(R1)	use v22 to test decoder
000025E8	E756 7010 3E95			1694+	VPKLS	V21, V22, V23, 3, 1	test instruction
000025EE	B98D 0020			1695+	EPSW	R2, R0	extract psw
000025F2	5020 500C		0000000C	1696+	ST	R2, CCPSW	to save CC
000025F6	E750 5048 080E		000025B0	1697+	VST	V21, V1027	save v1 output
000025FC	07FB			1698+	BR	R11	return
00002600				1699+RE27	DC	0F	V1 for this test
00002600				1700+	DROP	R5	
00002600	FFFFFFFF FFFFFFFF			1701	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00002608	FFFFFFFF FFFFFFFF						
00002610	01010203 04050607			1702	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
00002618	08090A0B 0C0D0E0F						
00002620	01110133 01550177			1703	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00002628	019901BB 01DD01FF						
				1704			
				1705 *			
				1706 *	VPKS	- Vector Pack Saturate	
				1707 *			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1708 * cc=0: No saturation	
				1709 * cc=1: At least one but not all elements saturated	
				1710 * cc=3: Saturation on all elements	
				1711 *-----	
				1712 * case - simple cc debug	
				1713 *-----	
				1714 *Hal fword	
				1715 VRR_B VPKS, 1, 0	
00002630				1716+ DS OFD	
00002630		00002630		1717+ USING *, R5	base for test data and test routine
00002630	00002698			1718+T28 DC A(X28)	address of test routine
00002634	001C			1719+ DC H' 28'	test number
00002636	00			1720+ DC X' 00'	
00002637	01			1721+ DC HL1' 1'	m4 used
00002638	01			1722+ DC HL1' 1'	m5 used
00002639	00			1723+ DC HL1' 0'	CC
0000263A	07			1724+ DC HL1' 7'	CC failed mask
0000263C	00000000	00000000		1725+ DS 2F	extracted PSW after test (has CC)
00002644	FF			1726+ DC X' FF'	extracted CC, if test failed
00002645	E5D7D2E2	40404040		1727+ DC CL8' VPKS'	instruction name
00002650	000026C8			1728+ DC A(RE28)	address of v1 result
00002654	000026D8			1729+ DC A(RE28+16)	address of v2 source
00002658	000026E8			1730+ DC A(RE28+32)	address of v3 source
0000265C	00000010			1731+ DC A(16)	result length
00002660	000026C8			1732+REA28 DC A(RE28)	result address
00002668	00000000	00000000		1733+ DS 2FD	gap
00002670	00000000	00000000			
00002678	00000000	00000000		1734+V1028 DS XL16	V1 output
00002680	00000000	00000000			
00002688	00000000	00000000		1735+ DS 2FD	gap
00002690	00000000	00000000			
				1736+*	
00002698				1737+X28 DS OF	
00002698	E310 5024 0014		00000024	1738+ LGF R1, V2ADDR	load v2 source
0000269E	E761 0000 0806		00000000	1739+ VL v22, 0(R1)	use v21 to test decoder
000026A4	E310 5028 0014		00000028	1740+ LGF R1, V3ADDR	load v3 source
000026AA	E771 0000 0806		00000000	1741+ VL v23, 0(R1)	use v22 to test decoder
000026B0	E756 7010 1E97			1742+ VPKS V21, V22, V23, 1, 1	test instruction
000026B6	B98D 0020			1743+ EPSW R2, R0	extract psw
000026BA	5020 500C		0000000C	1744+ ST R2, CCPSW	to save CC
000026BE	E750 5048 080E		00002678	1745+ VST V21, V1028	save v1 output
000026C4	07FB			1746+ BR R11	return
000026C8				1747+RE28 DC OF	V1 for this test
000026C8				1748+ DROP R5	
000026C8	00000000	00000000		1749 DC XL16' 0000000000000000 0000000000000000'	result t
000026D0	00000000	00000000			
000026D8	00000000	00000000		1750 DC XL16' 0000000000000000 0000000000000000'	v2
000026E0	00000000	00000000			
000026E8	00000000	00000000		1751 DC XL16' 0000000000000000 0000000000000000'	v3
000026F0	00000000	00000000			
				1752	
				1753 VRR_B VPKS, 1, 1	
000026F8				1754+ DS OFD	
000026F8		000026F8		1755+ USING *, R5	base for test data and test routine
000026F8	00002760			1756+T29 DC A(X29)	address of test routine
000026FC	001D			1757+ DC H' 29'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000026FE	00			1758+	DC	X' 00'	
000026FF	01			1759+	DC	HL1' 1'	m4 used
00002700	01			1760+	DC	HL1' 1'	m5 used
00002701	01			1761+	DC	HL1' 1'	CC
00002702	0B			1762+	DC	HL1' 11'	CC failed mask
00002704	00000000 00000000			1763+	DS	2F	extracted PSW after test (has CC)
0000270C	FF			1764+	DC	X' FF'	extracted CC, if test failed
0000270D	E5D7D2E2 40404040			1765+	DC	CL8' VPKS'	instruction name
00002718	00002790			1766+	DC	A(RE29)	address of v1 result
0000271C	000027A0			1767+	DC	A(RE29+16)	address of v2 source
00002720	000027B0			1768+	DC	A(RE29+32)	address of v3 source
00002724	00000010			1769+	DC	A(16)	result length
00002728	00002790			1770+REA29	DC	A(RE29)	result address
00002730	00000000 00000000			1771+	DS	2FD	gap
00002738	00000000 00000000						
00002740	00000000 00000000			1772+V1029	DS	XL16	V1 output
00002748	00000000 00000000						
00002750	00000000 00000000			1773+	DS	2FD	gap
00002758	00000000 00000000						
				1774+*			
00002760				1775+X29	DS	0F	
00002760	E310 5024 0014		00000024	1776+	LGF	R1, V2ADDR	load v2 source
00002766	E761 0000 0806		00000000	1777+	VL	v22, 0(R1)	use v21 to test decoder
0000276C	E310 5028 0014		00000028	1778+	LGF	R1, V3ADDR	load v3 source
00002772	E771 0000 0806		00000000	1779+	VL	v23, 0(R1)	use v22 to test decoder
00002778	E756 7010 1E97			1780+	VPKS	V21, V22, V23, 1, 1	test instruction
0000277E	B98D 0020			1781+	EPSW	R2, R0	extract psw
00002782	5020 500C		0000000C	1782+	ST	R2, CCPSW	to save CC
00002786	E750 5048 080E		00002740	1783+	VST	V21, V1029	save v1 output
0000278C	07FB			1784+	BR	R11	return
00002790				1785+RE29	DC	0F	V1 for this test
00002790				1786+	DROP	R5	
00002790	00000000 00000000			1787	DC	XL16' 0000000000000000 7F7F7F7F80808080'	result t
00002798	7F7F7F7F 80808080						
000027A0	00000000 00000000			1788	DC	XL16' 0000000000000000 0000000000000000'	v2
000027A8	00000000 00000000						
000027B0	0FFF0FFF 0FFF0FFF			1789	DC	XL16' 0FFF0FFF0FFF0FFF 8FFF8FFF8FFF8FFF'	v3
000027B8	8FFF8FFF 8FFF8FFF						
				1790			
				1791	VRR_B	VPKS, 1, 3	
000027C0				1792+	DS	0FD	
000027C0		000027C0		1793+	USING	*, R5	base for test data and test routine
000027C0	00002828			1794+T30	DC	A(X30)	address of test routine
000027C4	001E			1795+	DC	H' 30'	test number
000027C6	00			1796+	DC	X' 00'	
000027C7	01			1797+	DC	HL1' 1'	m4 used
000027C8	01			1798+	DC	HL1' 1'	m5 used
000027C9	03			1799+	DC	HL1' 3'	CC
000027CA	0E			1800+	DC	HL1' 14'	CC failed mask
000027CC	00000000 00000000			1801+	DS	2F	extracted PSW after test (has CC)
000027D4	FF			1802+	DC	X' FF'	extracted CC, if test failed
000027D5	E5D7D2E2 40404040			1803+	DC	CL8' VPKS'	instruction name
000027E0	00002858			1804+	DC	A(RE30)	address of v1 result
000027E4	00002868			1805+	DC	A(RE30+16)	address of v2 source
000027E8	00002878			1806+	DC	A(RE30+32)	address of v3 source
000027EC	00000010			1807+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000027F0	00002858			1808+REA30	DC	A(RE30)	result address
000027F8	00000000 00000000			1809+	DS	2FD	gap
00002800	00000000 00000000						
00002808	00000000 00000000			1810+V1030	DS	XL16	V1 output
00002810	00000000 00000000						
00002818	00000000 00000000			1811+	DS	2FD	gap
00002820	00000000 00000000						
				1812+*			
00002828				1813+X30	DS	0F	
00002828	E310 5024 0014		00000024	1814+	LGF	R1, V2ADDR	load v2 source
0000282E	E761 0000 0806		00000000	1815+	VL	v22, 0(R1)	use v21 to test decoder
00002834	E310 5028 0014		00000028	1816+	LGF	R1, V3ADDR	load v3 source
0000283A	E771 0000 0806		00000000	1817+	VL	v23, 0(R1)	use v22 to test decoder
00002840	E756 7010 1E97			1818+	VPKS	V21, V22, V23, 1, 1	test instruction
00002846	B98D 0020			1819+	EPSW	R2, R0	extract psw
0000284A	5020 500C		0000000C	1820+	ST	R2, CCPSW	to save CC
0000284E	E750 5048 080E		00002808	1821+	VST	V21, V1030	save v1 output
00002854	07FB			1822+	BR	R11	return
00002858				1823+RE30	DC	0F	V1 for this test
00002858				1824+	DROP	R5	
00002858	7F7F7F7F 80808080			1825	DC	XL16' 7F7F7F7F80808080 7F7F7F7F80808080'	result
00002860	7F7F7F7F 80808080						
00002868	0FFF0FFF 0FFF0FFF			1826	DC	XL16' 0FFF0FFF0FFF0FFF 8FFF8FFF8FFF8FFF'	v2
00002870	8FFF8FFF 8FFF8FFF						
00002878	0FFF0FFF 0FFF0FFF			1827	DC	XL16' 0FFF0FFF0FFF0FFF 8FFF8FFF8FFF8FFF'	v3
00002880	8FFF8FFF 8FFF8FFF						
				1828			
				1829 *Word			
				1830	VRR_B	VPKS, 2, 0	
00002888				1831+	DS	0FD	
00002888		00002888		1832+	USING	*, R5	base for test data and test routine
00002888	000028F0			1833+T31	DC	A(X31)	address of test routine
0000288C	001F			1834+	DC	H' 31'	test number
0000288E	00			1835+	DC	X' 00'	
0000288F	02			1836+	DC	HL1' 2'	m4 used
00002890	01			1837+	DC	HL1' 1'	m5 used
00002891	00			1838+	DC	HL1' 0'	CC
00002892	07			1839+	DC	HL1' 7'	CC failed mask
00002894	00000000 00000000			1840+	DS	2F	extracted PSW after test (has CC)
0000289C	FF			1841+	DC	X' FF'	extracted CC, if test failed
0000289D	E5D7D2E2 40404040			1842+	DC	CL8' VPKS'	instruction name
000028A8	00002920			1843+	DC	A(RE31)	address of v1 result
000028AC	00002930			1844+	DC	A(RE31+16)	address of v2 source
000028B0	00002940			1845+	DC	A(RE31+32)	address of v3 source
000028B4	00000010			1846+	DC	A(16)	result length
000028B8	00002920			1847+REA31	DC	A(RE31)	result address
000028C0	00000000 00000000			1848+	DS	2FD	gap
000028C8	00000000 00000000						
000028D0	00000000 00000000			1849+V1031	DS	XL16	V1 output
000028D8	00000000 00000000						
000028E0	00000000 00000000			1850+	DS	2FD	gap
000028E8	00000000 00000000						
				1851+*			
000028F0				1852+X31	DS	0F	
000028F0	E310 5024 0014		00000024	1853+	LGF	R1, V2ADDR	load v2 source
000028F6	E761 0000 0806		00000000	1854+	VL	v22, 0(R1)	use v21 to test decoder



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000028FC	E310 5028 0014		00000028	1855+	LGF	R1, V3ADDR	load v3 source
00002902	E771 0000 0806		00000000	1856+	VL	v23, 0(R1)	use v22 to test decoder
00002908	E756 7010 2E97			1857+	VPKS	V21, V22, V23, 2, 1	test instruction
0000290E	B98D 0020			1858+	EPSW	R2, R0	extract psw
00002912	5020 500C		0000000C	1859+	ST	R2, CCPSW	to save CC
00002916	E750 5048 080E		000028D0	1860+	VST	V21, V1031	save v1 output
0000291C	07FB			1861+	BR	R11	return
00002920				1862+RE31	DC	0F	V1 for this test
00002920				1863+	DROP	R5	
00002920	00000000 00000000			1864	DC	XL16' 0000000000000000 0000000000000000'	result t
00002928	00000000 00000000						
00002930	00000000 00000000			1865	DC	XL16' 0000000000000000 0000000000000000'	v2
00002938	00000000 00000000						
00002940	00000000 00000000			1866	DC	XL16' 0000000000000000 0000000000000000'	v3
00002948	00000000 00000000						
				1867			
				1868	VRR_B	VPKS, 2, 1	
00002950				1869+	DS	0FD	
00002950		00002950		1870+	USING	*, R5	base for test data and test routine
00002950	000029B8			1871+T32	DC	A(X32)	address of test routine
00002954	0020			1872+	DC	H' 32'	test number
00002956	00			1873+	DC	X' 00'	
00002957	02			1874+	DC	HL1' 2'	m4 used
00002958	01			1875+	DC	HL1' 1'	m5 used
00002959	01			1876+	DC	HL1' 1'	CC
0000295A	0B			1877+	DC	HL1' 11'	CC failed mask
0000295C	00000000 00000000			1878+	DS	2F	extracted PSW after test (has CC)
00002964	FF			1879+	DC	X' FF'	extracted CC, if test failed
00002965	E5D7D2E2 40404040			1880+	DC	CL8' VPKS'	instruction name
00002970	000029E8			1881+	DC	A(RE32)	address of v1 result
00002974	000029F8			1882+	DC	A(RE32+16)	address of v2 source
00002978	00002A08			1883+	DC	A(RE32+32)	address of v3 source
0000297C	00000010			1884+	DC	A(16)	result length
00002980	000029E8			1885+REA32	DC	A(RE32)	result address
00002988	00000000 00000000			1886+	DS	2FD	gap
00002990	00000000 00000000						
00002998	00000000 00000000			1887+V1032	DS	XL16	V1 output
000029A0	00000000 00000000						
000029A8	00000000 00000000			1888+	DS	2FD	gap
000029B0	00000000 00000000						
				1889+*			
000029B8				1890+X32	DS	0F	
000029B8	E310 5024 0014		00000024	1891+	LGF	R1, V2ADDR	load v2 source
000029BE	E761 0000 0806		00000000	1892+	VL	v22, 0(R1)	use v21 to test decoder
000029C4	E310 5028 0014		00000028	1893+	LGF	R1, V3ADDR	load v3 source
000029CA	E771 0000 0806		00000000	1894+	VL	v23, 0(R1)	use v22 to test decoder
000029D0	E756 7010 2E97			1895+	VPKS	V21, V22, V23, 2, 1	test instruction
000029D6	B98D 0020			1896+	EPSW	R2, R0	extract psw
000029DA	5020 500C		0000000C	1897+	ST	R2, CCPSW	to save CC
000029DE	E750 5048 080E		00002998	1898+	VST	V21, V1032	save v1 output
000029E4	07FB			1899+	BR	R11	return
000029E8				1900+RE32	DC	0F	V1 for this test
000029E8				1901+	DROP	R5	
000029E8	00000000 00000000			1902	DC	XL16' 0000000000000000 7FFF7FFF80008000'	result t
000029F0	7FFF7FFF 80008000						
000029F8	00000000 00000000			1903	DC	XL16' 0000000000000000 0000000000000000'	v2



LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002A00	00000000	00000000						
00002A08	0000FFFF	0000FFFF		1904	DC	XL16' 0000FFFF0000FFFF	8FFF8FFF8FFF8FFF'	v3
00002A10	8FFF8FFF	8FFF8FFF						
				1905				
				1906	VRR_B	VPKS, 2, 3		
00002A18				1907+	DS	0FD		
00002A18		00002A18		1908+	USING	*, R5	base for test data and test routine	
00002A18	00002A80			1909+T33	DC	A(X33)	address of test routine	
00002A1C	0021			1910+	DC	H' 33'	test number	
00002A1E	00			1911+	DC	X' 00'		
00002A1F	02			1912+	DC	HL1' 2'	m4 used	
00002A20	01			1913+	DC	HL1' 1'	m5 used	
00002A21	03			1914+	DC	HL1' 3'	CC	
00002A22	0E			1915+	DC	HL1' 14'	CC failed mask	
00002A24	00000000	00000000		1916+	DS	2F	extracted PSW after test (has CC)	
00002A2C	FF			1917+	DC	X' FF'	extracted CC, if test failed	
00002A2D	E5D7D2E2	40404040		1918+	DC	CL8' VPKS'	instruction name	
00002A38	00002AB0			1919+	DC	A(RE33)	address of v1 result	
00002A3C	00002AC0			1920+	DC	A(RE33+16)	address of v2 source	
00002A40	00002AD0			1921+	DC	A(RE33+32)	address of v3 source	
00002A44	00000010			1922+	DC	A(16)	result length	
00002A48	00002AB0			1923+REA33	DC	A(RE33)	result address	
00002A50	00000000	00000000		1924+	DS	2FD	gap	
00002A58	00000000	00000000						
00002A60	00000000	00000000		1925+V1033	DS	XL16	V1 output	
00002A68	00000000	00000000						
00002A70	00000000	00000000		1926+	DS	2FD	gap	
00002A78	00000000	00000000						
				1927+*				
00002A80				1928+X33	DS	0F		
00002A80	E310 5024 0014		00000024	1929+	LGF	R1, V2ADDR	load v2 source	
00002A86	E761 0000 0806		00000000	1930+	VL	v22, 0(R1)	use v21 to test decoder	
00002A8C	E310 5028 0014		00000028	1931+	LGF	R1, V3ADDR	load v3 source	
00002A92	E771 0000 0806		00000000	1932+	VL	v23, 0(R1)	use v22 to test decoder	
00002A98	E756 7010 2E97			1933+	VPKS	V21, V22, V23, 2, 1	test instruction	
00002A9E	B98D 0020			1934+	EPSW	R2, R0	extract psw	
00002AA2	5020 500C		0000000C	1935+	ST	R2, CCPSW	to save CC	
00002AA6	E750 5048 080E		00002A60	1936+	VST	V21, V1033	save v1 output	
00002AAC	07FB			1937+	BR	R11	return	
00002AB0				1938+RE33	DC	0F	V1 for this test	
00002AB0				1939+	DROP	R5		
00002AB0	7FFF7FFF	80008000		1940	DC	XL16' 7FFF7FFF80008000	7FFF7FFF80008000'	result
00002AB8	7FFF7FFF	80008000						
00002AC0	0000FFFF	0000FFFF		1941	DC	XL16' 0000FFFF0000FFFF	8FFF8FFF8FFF8FFF'	v2
00002AC8	8FFF8FFF	8FFF8FFF						
00002AD0	0000FFFF	0000FFFF		1942	DC	XL16' 0000FFFF0000FFFF	8FFF8FFF8FFF8FFF'	v3
00002AD8	8FFF8FFF	8FFF8FFF						
				1943				
				1944 *DoubleWord				
				1945	VRR_B	VPKS, 3, 0		
00002AE0				1946+	DS	0FD		
00002AE0		00002AE0		1947+	USING	*, R5	base for test data and test routine	
00002AE0	00002B48			1948+T34	DC	A(X34)	address of test routine	
00002AE4	0022			1949+	DC	H' 34'	test number	
00002AE6	00			1950+	DC	X' 00'		
00002AE7	03			1951+	DC	HL1' 3'	m4 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002AE8	01			1952+	DC	HL1' 1'	m5 used
00002AE9	00			1953+	DC	HL1' 0'	CC
00002AEA	07			1954+	DC	HL1' 7'	CC failed mask
00002AEC	00000000	00000000		1955+	DS	2F	extracted PSW after test (has CC)
00002AF4	FF			1956+	DC	X' FF'	extracted CC, if test failed
00002AF5	E5D7D2E2	40404040		1957+	DC	CL8' VPKS'	instruction name
00002B00	00002B78			1958+	DC	A(RE34)	address of v1 result
00002B04	00002B88			1959+	DC	A(RE34+16)	address of v2 source
00002B08	00002B98			1960+	DC	A(RE34+32)	address of v3 source
00002B0C	00000010			1961+	DC	A(16)	result length
00002B10	00002B78			1962+REA34	DC	A(RE34)	result address
00002B18	00000000	00000000		1963+	DS	2FD	gap
00002B20	00000000	00000000					
00002B28	00000000	00000000		1964+V1034	DS	XL16	V1 output
00002B30	00000000	00000000					
00002B38	00000000	00000000		1965+	DS	2FD	gap
00002B40	00000000	00000000					
00002B48				1966+*			
00002B48	E310 5024 0014		00000024	1967+X34	DS	0F	
00002B4E	E761 0000 0806		00000000	1968+	LGF	R1, V2ADDR	load v2 source
00002B54	E310 5028 0014		00000028	1969+	VL	v22, 0(R1)	use v21 to test decoder
00002B5A	E771 0000 0806		00000000	1970+	LGF	R1, V3ADDR	load v3 source
00002B60	E756 7010 3E97			1971+	VL	v23, 0(R1)	use v22 to test decoder
00002B66	B98D 0020			1972+	VPKS	V21, V22, V23, 3, 1	test instruction
00002B6A	5020 500C		0000000C	1973+	EPSW	R2, R0	extract psw
00002B6E	E750 5048 080E		00002B28	1974+	ST	R2, CCPSW	to save CC
00002B74	07FB			1975+	VST	V21, V1034	save v1 output
00002B78				1976+	BR	R11	return
00002B78				1977+RE34	DC	0F	V1 for this test
00002B78				1978+	DROP	R5	
00002B78	00000000	00000000		1979	DC	XL16' 0000000000000000 0000000000000000'	result
00002B80	00000000	00000000					
00002B88	00000000	00000000		1980	DC	XL16' 0000000000000000 0000000000000000'	v2
00002B90	00000000	00000000					
00002B98	00000000	00000000		1981	DC	XL16' 0000000000000000 0000000000000000'	v3
00002BA0	00000000	00000000					
00002BA8				1982			
00002BA8				1983	VRR_B	VPKS, 3, 1	
00002BA8		00002BA8		1984+	DS	0FD	
00002BA8	00002C10			1985+	USING	*, R5	base for test data and test routine
00002BAC	0023			1986+T35	DC	A(X35)	address of test routine
00002BAE	00			1987+	DC	H' 35'	test number
00002BAF	03			1988+	DC	X' 00'	
00002BB0	01			1989+	DC	HL1' 3'	m4 used
00002BB1	01			1990+	DC	HL1' 1'	m5 used
00002BB2	0B			1991+	DC	HL1' 1'	CC
00002BB4	00000000	00000000		1992+	DC	HL1' 11'	CC failed mask
00002BBC	FF			1993+	DS	2F	extracted PSW after test (has CC)
00002BB4	FF			1994+	DC	X' FF'	extracted CC, if test failed
00002BB8	E5D7D2E2	40404040		1995+	DC	CL8' VPKS'	instruction name
00002BC8	00002C40			1996+	DC	A(RE35)	address of v1 result
00002BCC	00002C50			1997+	DC	A(RE35+16)	address of v2 source
00002BD0	00002C60			1998+	DC	A(RE35+32)	address of v3 source
00002BD4	00000010			1999+	DC	A(16)	result length
00002BD8	00002C40			2000+REA35	DC	A(RE35)	result address
00002BE0	00000000	00000000		2001+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002BE8	00000000	00000000						
00002BF0	00000000	00000000		2002+V1035	DS	XL16	V1 output	
00002BF8	00000000	00000000						
00002C00	00000000	00000000		2003+	DS	2FD	gap	
00002C08	00000000	00000000						
00002C10				2004+*				
00002C10	E310 5024 0014		00000024	2005+X35	DS	0F		
00002C16	E761 0000 0806		00000000	2006+	LGF	R1, V2ADDR	load v2 source	
00002C1C	E310 5028 0014		00000028	2007+	VL	v22, 0(R1)	use v21 to test decoder	
00002C22	E771 0000 0806		00000000	2008+	LGF	R1, V3ADDR	load v3 source	
00002C28	E756 7010 3E97		00000000	2009+	VL	v23, 0(R1)	use v22 to test decoder	
00002C2E	B98D 0020			2010+	VPKS	V21, V22, V23, 3, 1	test instruction	
00002C32	5020 500C		0000000C	2011+	EPSW	R2, R0	extract psw	
00002C36	E750 5048 080E		00002BF0	2012+	ST	R2, CCPSW	to save CC	
00002C3C	07FB			2013+	VST	V21, V1035	save v1 output	
00002C40				2014+	BR	R11	return	
00002C40				2015+RE35	DC	0F	V1 for this test	
00002C40	00000000	7FFFFFFF		2016+	DROP	R5		
00002C48	7FFFFFFF	80000000		2017	DC	XL16' 0000000007FFFFFFF 7FFFFFFF80000000'	result t	
00002C50	00000000	00000000		2018	DC	XL16' 0000000000000000 0FFFFFFFFFFFFFFFFF'	v2	
00002C58	0FFFFFFFFF	FFFFFFFF						
00002C60	00000000	FFFFFFFF		2019	DC	XL16' 00000000FFFFFFFF 8FFFFFFFFFFFFFFFFF'	v3	
00002C68	8FFFFFFFFF	FFFFFFFF						
00002C70				2020				
00002C70			00002C70	2021	VRR_B	VPKS, 3, 3		
00002C70	00002CD8			2022+	DS	0FD		
00002C74	0024			2023+	USING	*, R5	base for test data and test routine	
00002C76	00			2024+T36	DC	A(X36)	address of test routine	
00002C77	03			2025+	DC	H' 36'	test number	
00002C78	01			2026+	DC	X' 00'		
00002C79	03			2027+	DC	HL1' 3'	m4 used	
00002C7A	0E			2028+	DC	HL1' 1'	m5 used	
00002C7C	00000000	00000000		2029+	DC	HL1' 3'	CC	
00002C84	FF			2030+	DC	HL1' 14'	CC failed mask	
00002C85	E5D7D2E2 40404040			2031+	DS	2F	extracted PSW after test (has CC)	
00002C90	00002D08			2032+	DC	X' FF'	extracted CC, if test failed	
00002C94	00002D18			2033+	DC	CL8' VPKS'	instruction name	
00002C98	00002D28			2034+	DC	A(RE36)	address of v1 result	
00002C9C	00000010			2035+	DC	A(RE36+16)	address of v2 source	
00002CA0	00002D08			2036+	DC	A(RE36+32)	address of v3 source	
00002CA8	00000000	00000000		2037+	DC	A(16)	result length	
00002CB0	00000000	00000000		2038+REA36	DC	A(RE36)	result address	
00002CB8	00000000	00000000		2039+	DS	2FD	gap	
00002CC0	00000000	00000000						
00002CC8	00000000	00000000		2040+V1036	DS	XL16	V1 output	
00002CD0	00000000	00000000						
00002CD8				2041+	DS	2FD	gap	
00002CD8	E310 5024 0014		00000024	2042+*				
00002CDE	E761 0000 0806		00000000	2043+X36	DS	0F		
00002CE4	E310 5028 0014		00000028	2044+	LGF	R1, V2ADDR	load v2 source	
00002CEA	E771 0000 0806		00000000	2045+	VL	v22, 0(R1)	use v21 to test decoder	
00002CF0	E756 7010 3E97			2046+	LGF	R1, V3ADDR	load v3 source	
				2047+	VL	v23, 0(R1)	use v22 to test decoder	
				2048+	VPKS	V21, V22, V23, 3, 1	test instruction	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002CF6	B98D 0020			2049+	EPSW	R2, R0	extract psw	
00002CFA	5020 500C		0000000C	2050+	ST	R2, CCPSW	to save CC	
00002CFE	E750 5048 080E		00002CB8	2051+	VST	V21, V1036	save v1 output	
00002D04	07FB			2052+	BR	R11	return	
00002D08				2053+RE36	DC	0F	V1 for this test	
00002D08				2054+	DROP	R5		
00002D08	7FFFFFFF 80000000			2055	DC	XL16' 7FFFFFFF80000000 7FFFFFFF80000000'	result t	
00002D10	7FFFFFFF 80000000							
00002D18	000000FF FFFFFFFF			2056	DC	XL16' 000000FFFFFFFF 8FFFFFFFFFFFFFFFFF'	v2	
00002D20	8FFFFFFFF FFFFFFFF							
00002D28	000000FF FFFFFFFF			2057	DC	XL16' 000000FFFFFFFF 8FFFFFFFFFFFFFFFFF'	v3	
00002D30	8FFFFFFFF FFFFFFFF							
				2058				
				2059 *				
				2060 * case - general				
				2061 *				
				2062 *Hal fword				
00002D38				2063	VRR_B	VPKS, 1, 0		
00002D38		00002D38		2064+	DS	0FD		
00002D38	00002DA0			2065+	USING	*, R5	base for test data and test routine	
00002D3C	0025			2066+T37	DC	A(X37)	address of test routine	
00002D3E	00			2067+	DC	H' 37'	test number	
00002D3F	01			2068+	DC	X' 00'		
00002D40	01			2069+	DC	HL1' 1'	m4 used	
00002D41	00			2070+	DC	HL1' 1'	m5 used	
00002D42	07			2071+	DC	HL1' 0'	CC	
00002D44	00000000 00000000			2072+	DC	HL1' 7'	CC failed mask	
00002D4C	FF			2073+	DS	2F	extracted PSW after test (has CC)	
00002D4D	E5D7D2E2 40404040			2074+	DC	X' FF'	extracted CC, if test failed	
00002D58	00002DD0			2075+	DC	CL8' VPKS'	instruction name	
00002D5C	00002DE0			2076+	DC	A(RE37)	address of v1 result	
00002D60	00002DF0			2077+	DC	A(RE37+16)	address of v2 source	
00002D64	00000010			2078+	DC	A(RE37+32)	address of v3 source	
00002D68	00002DD0			2079+	DC	A(16)	result length	
00002D70	00000000 00000000			2080+REA37	DC	A(RE37)	result address	
00002D78	00000000 00000000			2081+	DS	2FD	gap	
00002D80	00000000 00000000			2082+V1037	DS	XL16	V1 output	
00002D88	00000000 00000000							
00002D90	00000000 00000000			2083+	DS	2FD	gap	
00002D98	00000000 00000000							
00002DA0				2084+*				
00002DA0	E310 5024 0014		00000024	2085+X37	DS	0F		
00002DA6	E761 0000 0806		00000000	2086+	LGF	R1, V2ADDR	load v2 source	
00002DAC	E310 5028 0014		00000028	2087+	VL	v22, 0(R1)	use v21 to test decoder	
00002DB2	E771 0000 0806		00000000	2088+	LGF	R1, V3ADDR	load v3 source	
00002DB8	E756 7010 1E97			2089+	VL	v23, 0(R1)	use v22 to test decoder	
00002DBE	B98D 0020			2090+	VPKS	V21, V22, V23, 1, 1	test instruction	
00002DC2	5020 500C		0000000C	2091+	EPSW	R2, R0	extract psw	
00002DC6	E750 5048 080E		00002D80	2092+	ST	R2, CCPSW	to save CC	
00002DCC	07FB			2093+	VST	V21, V1037	save v1 output	
00002DD0				2094+	BR	R11	return	
00002DD0				2095+RE37	DC	0F	V1 for this test	
00002DD0	11335577 22446608			2096+	DROP	R5		
00002DD8	FEFDFCFB FAF9F8F7			2097	DC	XL16' 1133557722446608 FEFDFCFBFAF9F8F7'	result t	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002DE0	00110033 00550077			2098	DC	XL16' 0011003300550077 0022004400660008'	v2	
00002DE8	00220044 00660008							
00002DF0	FFFEFFFD FFFCFFFB			2099	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3	
00002DF8	FFFAFF9 FFF8FFF7							
				2100				
00002E00				2101	VRR_B	VPKS, 1, 0		
00002E00		00002E00		2102+	DS	0FD		
00002E00	00002E68			2103+	USING	*, R5	base for test data and test routine	
00002E04	0026			2104+T38	DC	A(X38)	address of test routine	
00002E06	00			2105+	DC	H' 38'	test number	
00002E07	01			2106+	DC	X' 00'		
00002E08	01			2107+	DC	HL1' 1'	m4 used	
00002E09	00			2108+	DC	HL1' 1'	m5 used	
00002E0A	07			2109+	DC	HL1' 0'	CC	
00002E0C	00000000 00000000			2110+	DC	HL1' 7'	CC failed mask	
00002E14	FF			2111+	DS	2F	extracted PSW after test (has CC)	
00002E15	E5D7D2E2 40404040			2112+	DC	X' FF'	extracted CC, if test failed	
00002E20	00002E98			2113+	DC	CL8' VPKS'	instruction name	
00002E24	00002EA8			2114+	DC	A(RE38)	address of v1 result	
00002E28	00002EB8			2115+	DC	A(RE38+16)	address of v2 source	
00002E2C	00000010			2116+	DC	A(RE38+32)	address of v3 source	
00002E30	00002E98			2117+	DC	A(16)	result length	
00002E38	00000000 00000000			2118+REA38	DC	A(RE38)	result address	
00002E40	00000000 00000000			2119+	DS	2FD	gap	
00002E48	00000000 00000000			2120+V1038	DS	XL16	V1 output	
00002E50	00000000 00000000							
00002E58	00000000 00000000			2121+	DS	2FD	gap	
00002E60	00000000 00000000							
				2122+*				
00002E68				2123+X38	DS	0F		
00002E68	E310 5024 0014		00000024	2124+	LGF	R1, V2ADDR	load v2 source	
00002E6E	E761 0000 0806		00000000	2125+	VL	v22, 0(R1)	use v21 to test decoder	
00002E74	E310 5028 0014		00000028	2126+	LGF	R1, V3ADDR	load v3 source	
00002E7A	E771 0000 0806		00000000	2127+	VL	v23, 0(R1)	use v22 to test decoder	
00002E80	E756 7010 1E97			2128+	VPKS	V21, V22, V23, 1, 1	test instruction	
00002E86	B98D 0020			2129+	EPSW	R2, R0	extract psw	
00002E8A	5020 500C		0000000C	2130+	ST	R2, CCPSW	to save CC	
00002E8E	E750 5048 080E		00002E48	2131+	VST	V21, V1038	save v1 output	
00002E94	07FB			2132+	BR	R11	return	
00002E98				2133+RE38	DC	0F	V1 for this test	
00002E98				2134+	DROP	R5		
00002E98	FEFDFCFB FAF9F8F7			2135	DC	XL16' FEFDFCFBFAF9F8F7 1133557722446608'	result t	
00002EA0	11335577 22446608							
00002EA8	FFFEFFFD FFFCFFFB			2136	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2	
00002EB0	FFFAFF9 FFF8FFF7							
00002EB8	00110033 00550077			2137	DC	XL16' 0011003300550077 0022004400660008'	v3	
00002EC0	00220044 00660008							
				2138				
00002EC8				2139	VRR_B	VPKS, 1, 1		
00002EC8		00002EC8		2140+	DS	0FD		
00002EC8	00002F30			2141+	USING	*, R5	base for test data and test routine	
00002ECC	0027			2142+T39	DC	A(X39)	address of test routine	
00002ECE	00			2143+	DC	H' 39'	test number	
00002ECF	01			2144+	DC	X' 00'		
				2145+	DC	HL1' 1'	m4 used	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002ED0	01			2146+	DC	HL1' 1'	m5 used
00002ED1	01			2147+	DC	HL1' 1'	CC
00002ED2	0B			2148+	DC	HL1' 11'	CC failed mask
00002ED4	00000000 00000000			2149+	DS	2F	extracted PSW after test (has CC)
00002EDC	FF			2150+	DC	X' FF'	extracted CC, if test failed
00002EDD	E5D7D2E2 40404040			2151+	DC	CL8' VPKS'	instruction name
00002EE8	00002F60			2152+	DC	A(RE39)	address of v1 result
00002EEC	00002F70			2153+	DC	A(RE39+16)	address of v2 source
00002EF0	00002F80			2154+	DC	A(RE39+32)	address of v3 source
00002EF4	00000010			2155+	DC	A(16)	result length
00002EF8	00002F60			2156+REA39	DC	A(RE39)	result address
00002F00	00000000 00000000			2157+	DS	2FD	gap
00002F08	00000000 00000000						
00002F10	00000000 00000000			2158+V1039	DS	XL16	V1 output
00002F18	00000000 00000000						
00002F20	00000000 00000000			2159+	DS	2FD	gap
00002F28	00000000 00000000						
00002F30				2160+*			
00002F30	E310 5024 0014		00000024	2161+X39	DS	0F	
00002F36	E761 0000 0806		00000000	2162+	LGF	R1, V2ADDR	load v2 source
00002F3C	E310 5028 0014		00000028	2163+	VL	v22, 0(R1)	use v21 to test decoder
00002F42	E771 0000 0806		00000000	2164+	LGF	R1, V3ADDR	load v3 source
00002F48	E756 7010 1E97			2165+	VL	v23, 0(R1)	use v22 to test decoder
00002F4E	B98D 0020			2166+	VPKS	V21, V22, V23, 1, 1	test instruction
00002F52	5020 500C		0000000C	2167+	EPSW	R2, R0	extract psw
00002F56	E750 5048 080E		00002F10	2168+	ST	R2, CCPSW	to save CC
00002F5C	07FB			2169+	VST	V21, V1039	save v1 output
00002F60				2170+	BR	R11	return
00002F60				2171+RE39	DC	0F	V1 for this test
00002F60				2172+	DROP	R5	
00002F60	017F7F7F 7F7F7F80			2173	DC	XL16' 017F7F7F7F7F7F80 1133557722446600'	result
00002F68	11335577 22446600						
00002F70	00010203 04050607			2174	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v2
00002F78	08090A0B 0C0DFE0F						
00002F80	00110033 00550077			2175	DC	XL16' 0011003300550077 0022004400660000'	v3
00002F88	00220044 00660000						
00002F90				2176			
00002F90				2177	VRR_B	VPKS, 1, 1	
00002F90		00002F90		2178+	DS	0FD	
00002F90	00002FF8			2179+	USING	*, R5	base for test data and test routine
00002F94	0028			2180+T40	DC	A(X40)	address of test routine
00002F96	00			2181+	DC	H' 40'	test number
00002F97	01			2182+	DC	X' 00'	
00002F98	01			2183+	DC	HL1' 1'	m4 used
00002F98	01			2184+	DC	HL1' 1'	m5 used
00002F99	01			2185+	DC	HL1' 1'	CC
00002F9A	0B			2186+	DC	HL1' 11'	CC failed mask
00002F9C	00000000 00000000			2187+	DS	2F	extracted PSW after test (has CC)
00002FA4	FF			2188+	DC	X' FF'	extracted CC, if test failed
00002FA5	E5D7D2E2 40404040			2189+	DC	CL8' VPKS'	instruction name
00002FB0	00003028			2190+	DC	A(RE40)	address of v1 result
00002FB4	00003038			2191+	DC	A(RE40+16)	address of v2 source
00002FB8	00003048			2192+	DC	A(RE40+32)	address of v3 source
00002FBC	00000010			2193+	DC	A(16)	result length
00002FC0	00003028			2194+REA40	DC	A(RE40)	result address
00002FC8	00000000 00000000			2195+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002FD0	00000000 00000000						
00002FD8	00000000 00000000			2196+V1040	DS	XL16	V1 output
00002FE0	00000000 00000000						
00002FE8	00000000 00000000			2197+	DS	2FD	gap
00002FF0	00000000 00000000						
00002FF8				2198+*			
00002FF8	E310 5024 0014		00000024	2199+X40	DS	0F	
00002FFE	E761 0000 0806		00000000	2200+	LGF	R1, V2ADDR	load v2 source
00003004	E310 5028 0014		00000028	2201+	VL	v22, 0(R1)	use v21 to test decoder
0000300A	E771 0000 0806		00000000	2202+	LGF	R1, V3ADDR	load v3 source
00003010	E756 7010 1E97			2203+	VL	v23, 0(R1)	use v22 to test decoder
00003016	B98D 0020			2204+	VPKS	V21, V22, V23, 1, 1	test instruction
0000301A	5020 500C		0000000C	2205+	EPSW	R2, R0	extract psw
0000301E	E750 5048 080E		00002FD8	2206+	ST	R2, CCPSW	to save CC
00003024	07FB			2207+	VST	V21, V1040	save v1 output
00003028				2208+	BR	R11	return
00003028				2209+RE40	DC	0F	V1 for this test
00003028				2210+	DROP	R5	
00003028	11335577 22446600			2211	DC	XL16' 1133557722446600 017F7F7F7F7F7F80'	result
00003030	017F7F7F 7F7F7F80						
00003038	00110033 00550077			2212	DC	XL16' 0011003300550077 0022004400660000'	v2
00003040	00220044 00660000						
00003048	00010203 04050607			2213	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v3
00003050	08090A0B 0C0DFE0F						
00003058				2214			
00003058				2215	VRR_B	VPKS, 1, 3	
00003058		00003058		2216+	DS	0FD	
00003058	000030C0			2217+	USING	*, R5	base for test data and test routine
0000305C	0029			2218+T41	DC	A(X41)	address of test routine
0000305E	00			2219+	DC	H' 41'	test number
0000305F	01			2220+	DC	X' 00'	
00003060	01			2221+	DC	HL1' 1'	m4 used
00003061	03			2222+	DC	HL1' 1'	m5 used
00003062	0E			2223+	DC	HL1' 3'	CC
00003064	00000000 00000000			2224+	DC	HL1' 14'	CC failed mask
0000306C	FF			2225+	DS	2F	extracted PSW after test (has CC)
0000306D	E5D7D2E2 40404040			2226+	DC	X' FF'	extracted CC, if test failed
00003078	000030F0			2227+	DC	CL8' VPKS'	instruction name
0000307C	00003100			2228+	DC	A(RE41)	address of v1 result
00003080	00003110			2229+	DC	A(RE41+16)	address of v2 source
00003084	00000010			2230+	DC	A(RE41+32)	address of v3 source
00003088	000030F0			2231+	DC	A(16)	result length
00003090	00000000 00000000			2232+REA41	DC	A(RE41)	result address
00003098	00000000 00000000			2233+	DS	2FD	gap
000030A0	00000000 00000000			2234+V1041	DS	XL16	V1 output
000030A8	00000000 00000000						
000030B0	00000000 00000000			2235+	DS	2FD	gap
000030B8	00000000 00000000						
000030C0				2236+*			
000030C0	E310 5024 0014		00000024	2237+X41	DS	0F	
000030C6	E761 0000 0806		00000000	2238+	LGF	R1, V2ADDR	load v2 source
000030CC	E310 5028 0014		00000028	2239+	VL	v22, 0(R1)	use v21 to test decoder
000030D2	E771 0000 0806		00000000	2240+	LGF	R1, V3ADDR	load v3 source
000030D8	E756 7010 1E97			2241+	VL	v23, 0(R1)	use v22 to test decoder
				2242+	VPKS	V21, V22, V23, 1, 1	test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000030DE	B98D 0020			2243+	EPSW	R2, R0	extract psw
000030E2	5020 500C		0000000C	2244+	ST	R2, CCPSW	to save CC
000030E6	E750 5048 080E		000030A0	2245+	VST	V21, V1041	save v1 output
000030EC	07FB			2246+	BR	R11	return
000030F0				2247+RE41	DC	0F	V1 for this test
000030F0				2248+	DROP	R5	
000030F0	7F7F7F7F 7F7F7F7F			2249	DC	XL16' 7F7F7F7F7F7F7F7F 7F7F7F7F7F7F7F7F'	result t
000030F8	7F7F7F7F 7F7F7F7F						
00003100	01110133 01550177			2250	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00003108	019901BB 01DD01FF						
00003110	01010203 04050607			2251	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
00003118	08090A0B 0C0D0E0F						
				2252			
				2253	VRR_B	VPKS, 1, 3	
00003120				2254+	DS	0FD	
00003120		00003120		2255+	USING	*, R5	base for test data and test routine
00003120	00003188			2256+T42	DC	A(X42)	address of test routine
00003124	002A			2257+	DC	H' 42'	test number
00003126	00			2258+	DC	X' 00'	
00003127	01			2259+	DC	HL1' 1'	m4 used
00003128	01			2260+	DC	HL1' 1'	m5 used
00003129	03			2261+	DC	HL1' 3'	CC
0000312A	0E			2262+	DC	HL1' 14'	CC failed mask
0000312C	00000000 00000000			2263+	DS	2F	extracted PSW after test (has CC)
00003134	FF			2264+	DC	X' FF'	extracted CC, if test failed
00003135	E5D7D2E2 40404040			2265+	DC	CL8' VPKS'	instruction name
00003140	000031B8			2266+	DC	A(RE42)	address of v1 result
00003144	000031C8			2267+	DC	A(RE42+16)	address of v2 source
00003148	000031D8			2268+	DC	A(RE42+32)	address of v3 source
0000314C	00000010			2269+	DC	A(16)	result length
00003150	000031B8			2270+REA42	DC	A(RE42)	result address
00003158	00000000 00000000			2271+	DS	2FD	gap
00003160	00000000 00000000						
00003168	00000000 00000000			2272+V1042	DS	XL16	V1 output
00003170	00000000 00000000						
00003178	00000000 00000000			2273+	DS	2FD	gap
00003180	00000000 00000000						
				2274+*			
00003188				2275+X42	DS	0F	
00003188	E310 5024 0014		00000024	2276+	LGF	R1, V2ADDR	load v2 source
0000318E	E761 0000 0806		00000000	2277+	VL	v22, 0(R1)	use v21 to test decoder
00003194	E310 5028 0014		00000028	2278+	LGF	R1, V3ADDR	load v3 source
0000319A	E771 0000 0806		00000000	2279+	VL	v23, 0(R1)	use v22 to test decoder
000031A0	E756 7010 1E97			2280+	VPKS	V21, V22, V23, 1, 1	test instruction
000031A6	B98D 0020			2281+	EPSW	R2, R0	extract psw
000031AA	5020 500C		0000000C	2282+	ST	R2, CCPSW	to save CC
000031AE	E750 5048 080E		00003168	2283+	VST	V21, V1042	save v1 output
000031B4	07FB			2284+	BR	R11	return
000031B8				2285+RE42	DC	0F	V1 for this test
000031B8				2286+	DROP	R5	
000031B8	7F7F7F7F 7F7F7F7F			2287	DC	XL16' 7F7F7F7F7F7F7F7F 7F7F7F7F7F7F7F7F'	result t
000031C0	7F7F7F7F 7F7F7F7F						
000031C8	01010203 04050607			2288	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
000031D0	08090A0B 0C0D0E0F						
000031D8	01110133 01550177			2289	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
000031E0	019901BB 01DD01FF						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				2290			
				2291	VRR_B	VPKS, 1, 3	
000031E8				2292+	DS	0FD	
000031E8		000031E8		2293+	USING	*, R5	base for test data and test routine
000031E8	00003250			2294+T43	DC	A(X43)	address of test routine
000031EC	002B			2295+	DC	H' 43'	test number
000031EE	00			2296+	DC	X' 00'	
000031EF	01			2297+	DC	HL1' 1'	m4 used
000031F0	01			2298+	DC	HL1' 1'	m5 used
000031F1	03			2299+	DC	HL1' 3'	CC
000031F2	0E			2300+	DC	HL1' 14'	CC failed mask
000031F4	00000000	00000000		2301+	DS	2F	extracted PSW after test (has CC)
000031FC	FF			2302+	DC	X' FF'	extracted CC, if test failed
000031FD	E5D7D2E2	40404040		2303+	DC	CL8' VPKS'	instruction name
00003208	00003280			2304+	DC	A(RE43)	address of v1 result
0000320C	00003290			2305+	DC	A(RE43+16)	address of v2 source
00003210	000032A0			2306+	DC	A(RE43+32)	address of v3 source
00003214	00000010			2307+	DC	A(16)	result length
00003218	00003280			2308+REA43	DC	A(RE43)	result address
00003220	00000000	00000000		2309+	DS	2FD	gap
00003228	00000000	00000000					
00003230	00000000	00000000		2310+V1043	DS	XL16	V1 output
00003238	00000000	00000000					
00003240	00000000	00000000		2311+	DS	2FD	gap
00003248	00000000	00000000					
				2312+*			
00003250				2313+X43	DS	0F	
00003250	E310 5024 0014		00000024	2314+	LGF	R1, V2ADDR	load v2 source
00003256	E761 0000 0806		00000000	2315+	VL	v22, 0(R1)	use v21 to test decoder
0000325C	E310 5028 0014		00000028	2316+	LGF	R1, V3ADDR	load v3 source
00003262	E771 0000 0806		00000000	2317+	VL	v23, 0(R1)	use v22 to test decoder
00003268	E756 7010 1E97			2318+	VPKS	V21, V22, V23, 1, 1	test instruction
0000326E	B98D 0020			2319+	EPSW	R2, R0	extract psw
00003272	5020 500C		0000000C	2320+	ST	R2, CCPSW	to save CC
00003276	E750 5048 080E		00003230	2321+	VST	V21, V1043	save v1 output
0000327C	07FB			2322+	BR	R11	return
00003280				2323+RE43	DC	0F	V1 for this test
00003280				2324+	DROP	R5	
00003280	80808080	80808080		2325	DC	XL16' 8080808080808080 8080808080808080'	result t
00003288	80808080	80808080					
00003290	F111F133	F155F177		2326	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v2
00003298	F199F1BB	F1DDF1FF					
000032A0	F101F203	F405F607		2327	DC	XL16' F101F203F405F607 F809FAFBFCFDFF0F'	v3
000032A8	F809FAFB	FCFDFF0F					
				2328			
				2329	VRR_B	VPKS, 1, 3	
000032B0				2330+	DS	0FD	
000032B0		000032B0		2331+	USING	*, R5	base for test data and test routine
000032B0	00003318			2332+T44	DC	A(X44)	address of test routine
000032B4	002C			2333+	DC	H' 44'	test number
000032B6	00			2334+	DC	X' 00'	
000032B7	01			2335+	DC	HL1' 1'	m4 used
000032B8	01			2336+	DC	HL1' 1'	m5 used
000032B9	03			2337+	DC	HL1' 3'	CC
000032BA	0E			2338+	DC	HL1' 14'	CC failed mask
000032BC	00000000	00000000		2339+	DS	2F	extracted PSW after test (has CC)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000032C4	FF			2340+	DC	X' FF'	extracted CC, if test failed
000032C5	E5D7D2E2 40404040			2341+	DC	CL8' VPKS'	instruction name
000032D0	00003348			2342+	DC	A(RE44)	address of v1 result
000032D4	00003358			2343+	DC	A(RE44+16)	address of v2 source
000032D8	00003368			2344+	DC	A(RE44+32)	address of v3 source
000032DC	00000010			2345+	DC	A(16)	result length
000032E0	00003348			2346+REA44	DC	A(RE44)	result address
000032E8	00000000 00000000			2347+	DS	2FD	gap
000032F0	00000000 00000000						
000032F8	00000000 00000000			2348+V1044	DS	XL16	V1 output
00003300	00000000 00000000						
00003308	00000000 00000000			2349+	DS	2FD	gap
00003310	00000000 00000000						
00003318				2350+*			
00003318	E310 5024 0014			2351+X44	DS	0F	
0000331E	E761 0000 0806		00000024	2352+	LGF	R1, V2ADDR	load v2 source
00003324	E310 5028 0014		00000000	2353+	VL	v22, 0(R1)	use v21 to test decoder
0000332A	E771 0000 0806		00000028	2354+	LGF	R1, V3ADDR	load v3 source
00003330	E756 7010 1E97		00000000	2355+	VL	v23, 0(R1)	use v22 to test decoder
00003336	B98D 0020			2356+	VPKS	V21, V22, V23, 1, 1	test instruction
0000333A	5020 500C		0000000C	2357+	EPSW	R2, R0	extract psw
0000333E	E750 5048 080E		000032F8	2358+	ST	R2, CCPSW	to save CC
00003344	07FB			2359+	VST	V21, V1044	save v1 output
00003348				2360+	BR	R11	return
00003348				2361+RE44	DC	0F	V1 for this test
00003348				2362+	DROP	R5	
00003348	80808080 80808080			2363	DC	XL16' 8080808080808080 8080808080808080'	result t
00003350	80808080 80808080						
00003358	F101F203 F405F607			2364	DC	XL16' F101F203F405F607 F809FAFBFCFDFE0F'	v2
00003360	F809FAFB FCFDFE0F						
00003368	F111F133 F155F177			2365	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v3
00003370	F199F1BB F1DDF1FF						
				2366			
				2367 *Word			
				2368	VRR_B	VPKS, 2, 0	
00003378				2369+	DS	0FD	
00003378		00003378		2370+	USING	*, R5	base for test data and test routine
00003378	000033E0			2371+T45	DC	A(X45)	address of test routine
0000337C	002D			2372+	DC	H' 45'	test number
0000337E	00			2373+	DC	X' 00'	
0000337F	02			2374+	DC	HL1' 2'	m4 used
00003380	01			2375+	DC	HL1' 1'	m5 used
00003381	00			2376+	DC	HL1' 0'	CC
00003382	07			2377+	DC	HL1' 7'	CC failed mask
00003384	00000000 00000000			2378+	DS	2F	extracted PSW after test (has CC)
0000338C	FF			2379+	DC	X' FF'	extracted CC, if test failed
0000338D	E5D7D2E2 40404040			2380+	DC	CL8' VPKS'	instruction name
00003398	00003410			2381+	DC	A(RE45)	address of v1 result
0000339C	00003420			2382+	DC	A(RE45+16)	address of v2 source
000033A0	00003430			2383+	DC	A(RE45+32)	address of v3 source
000033A4	00000010			2384+	DC	A(16)	result length
000033A8	00003410			2385+REA45	DC	A(RE45)	result address
000033B0	00000000 00000000			2386+	DS	2FD	gap
000033B8	00000000 00000000						
000033C0	00000000 00000000			2387+V1045	DS	XL16	V1 output
000033C8	00000000 00000000						



LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000033D0	00000000 00000000			2388+	DS	2FD	gap	
000033D8	00000000 00000000							
000033E0				2389+*				
000033E0	E310 5024 0014		00000024	2390+X45	DS	0F		
000033E6	E761 0000 0806		00000000	2391+	LGF	R1, V2ADDR	load v2 source	
000033EC	E310 5028 0014		00000028	2392+	VL	v22, 0(R1)	use v21 to test decoder	
000033F2	E771 0000 0806		00000000	2393+	LGF	R1, V3ADDR	load v3 source	
000033F8	E756 7010 2E97			2394+	VL	v23, 0(R1)	use v22 to test decoder	
000033FE	B98D 0020			2395+	VPKS	V21, V22, V23, 2, 1	test instruction	
00003402	5020 500C		0000000C	2396+	EPSW	R2, R0	extract psw	
00003406	E750 5048 080E		000033C0	2397+	ST	R2, CCPSW	to save CC	
0000340C	07FB			2398+	VST	V21, V1045	save v1 output	
00003410				2399+	BR	R11	return	
00003410				2400+RE45	DC	0F	V1 for this test	
00003410	11335577 22446688			2401+	DROP	R5		
00003418	FEFDFCFB FAF9F8F7			2402	DC	XL16' 1133557722446688 FEFDFCFBFAF9F8F7'	result t	
00003420	00001133 00005577			2403	DC	XL16' 0000113300005577 0000224400006688'	v2	
00003428	00002244 00006688							
00003430	FFFFFFFD FFFFCFB			2404	DC	XL16' FFFFFFFDFFFFFFFCFB FFFFAF9FFFFFFF8F7'	v3	
00003438	FFFFFFAF9 FFFFF8F7							
00003440				2405				
00003440		00003440		2406	VRR_B	VPKS, 2, 0		
00003440	000034A8			2407+	DS	0FD		
00003444	002E			2408+	USING	*, R5	base for test data and test routine	
00003446	00			2409+T46	DC	A(X46)	address of test routine	
00003447	02			2410+	DC	H' 46'	test number	
00003448	01			2411+	DC	X' 00'		
00003449	00			2412+	DC	HL1' 2'	m4 used	
0000344A	07			2413+	DC	HL1' 1'	m5 used	
0000344C	00000000 00000000			2414+	DC	HL1' 0'	CC	
00003454	FF			2415+	DC	HL1' 7'	CC failed mask	
00003455	E5D7D2E2 40404040			2416+	DS	2F	extracted PSW after test (has CC)	
00003460	000034D8			2417+	DC	X' FF'	extracted CC, if test failed	
00003464	000034E8			2418+	DC	CL8' VPKS'	instruction name	
00003468	000034F8			2419+	DC	A(RE46)	address of v1 result	
0000346C	00000010			2420+	DC	A(RE46+16)	address of v2 source	
00003470	000034D8			2421+	DC	A(RE46+32)	address of v3 source	
00003478	00000000 00000000			2422+	DC	A(16)	result length	
00003480	00000000 00000000			2423+REA46	DC	A(RE46)	result address	
00003488	00000000 00000000			2424+	DS	2FD	gap	
00003490	00000000 00000000			2425+V1046	DS	XL16	V1 output	
00003498	00000000 00000000			2426+	DS	2FD	gap	
000034A0	00000000 00000000							
000034A8				2427+*				
000034A8	E310 5024 0014		00000024	2428+X46	DS	0F		
000034AE	E761 0000 0806		00000000	2429+	LGF	R1, V2ADDR	load v2 source	
000034B4	E310 5028 0014		00000028	2430+	VL	v22, 0(R1)	use v21 to test decoder	
000034BA	E771 0000 0806		00000000	2431+	LGF	R1, V3ADDR	load v3 source	
000034C0	E756 7010 2E97			2432+	VL	v23, 0(R1)	use v22 to test decoder	
000034C6	B98D 0020			2433+	VPKS	V21, V22, V23, 2, 1	test instruction	
000034CA	5020 500C		0000000C	2434+	EPSW	R2, R0	extract psw	
000034CE	E750 5048 080E		00003488	2435+	ST	R2, CCPSW	to save CC	
				2436+	VST	V21, V1046	save v1 output	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000034D4	07FB			2437+	BR	R11	return
000034D8				2438+RE46	DC	0F	V1 for this test
000034D8				2439+	DROP	R5	
000034D8	FEFDFCFB FAF9F8F7			2440	DC	XL16' FEFDFCFBFAF9F8F7	1133557722446688' result t
000034E0	11335577 22446688						
000034E8	FFFFFFFD FFFFCFB			2441	DC	XL16' FFFFFFFDFFFFFFCFB	FFFFFFFAF9FFFFFFF8F7' v2
000034F0	FFFFFFAF9 FFFFF8F7						
000034F8	00001133 00005577			2442	DC	XL16' 0000113300005577	0000224400006688' v3
00003500	00002244 00006688						
				2443			
				2444	VRR_B	VPKS, 2, 1	
00003508				2445+	DS	0FD	
00003508		00003508		2446+	USING	*, R5	base for test data and test routine
00003508	00003570			2447+T47	DC	A(X47)	address of test routine
0000350C	002F			2448+	DC	H' 47'	test number
0000350E	00			2449+	DC	X' 00'	
0000350F	02			2450+	DC	HL1' 2'	m4 used
00003510	01			2451+	DC	HL1' 1'	m5 used
00003511	01			2452+	DC	HL1' 1'	CC
00003512	0B			2453+	DC	HL1' 11'	CC failed mask
00003514	00000000 00000000			2454+	DS	2F	extracted PSW after test (has CC)
0000351C	FF			2455+	DC	X' FF'	extracted CC, if test failed
0000351D	E5D7D2E2 40404040			2456+	DC	CL8' VPKS'	instruction name
00003528	000035A0			2457+	DC	A(RE47)	address of v1 result
0000352C	000035B0			2458+	DC	A(RE47+16)	address of v2 source
00003530	000035C0			2459+	DC	A(RE47+32)	address of v3 source
00003534	00000010			2460+	DC	A(16)	result length
00003538	000035A0			2461+REA47	DC	A(RE47)	result address
00003540	00000000 00000000			2462+	DS	2FD	gap
00003548	00000000 00000000						
00003550	00000000 00000000			2463+V1047	DS	XL16	V1 output
00003558	00000000 00000000						
00003560	00000000 00000000			2464+	DS	2FD	gap
00003568	00000000 00000000						
				2465+*			
00003570				2466+X47	DS	0F	
00003570	E310 5024 0014		00000024	2467+	LGF	R1, V2ADDR	load v2 source
00003576	E761 0000 0806		00000000	2468+	VL	v22, 0(R1)	use v21 to test decoder
0000357C	E310 5028 0014		00000028	2469+	LGF	R1, V3ADDR	load v3 source
00003582	E771 0000 0806		00000000	2470+	VL	v23, 0(R1)	use v22 to test decoder
00003588	E756 7010 2E97			2471+	VPKS	V21, V22, V23, 2, 1	test instruction
0000358E	B98D 0020			2472+	EPSW	R2, R0	extract psw
00003592	5020 500C		0000000C	2473+	ST	R2, CCPSW	to save CC
00003596	E750 5048 080E		00003550	2474+	VST	V21, V1047	save v1 output
0000359C	07FB			2475+	BR	R11	return
000035A0				2476+RE47	DC	0F	V1 for this test
000035A0				2477+	DROP	R5	
000035A0	12037FFF 7FFF7FFF			2478	DC	XL16' 12037FFF7FFF7FFF	1133557719BB2DFF' result t
000035A8	11335577 19BB2DFF						
000035B0	00001203 04050607			2479	DC	XL16' 0000120304050607	08090A0B0C0D0E0F' v2
000035B8	08090A0B 0C0D0E0F						
000035C0	00001133 00005577			2480	DC	XL16' 0000113300005577	000019BB00002DFF' v3
000035C8	000019BB 00002DFF						
				2481			
				2482	VRR_B	VPKS, 2, 1	
000035D0				2483+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000035D0		000035D0		2484+	USING *, R5	base for test data and test routine
000035D0	00003638			2485+T48	DC A(X48)	address of test routine
000035D4	0030			2486+	DC H' 48'	test number
000035D6	00			2487+	DC X' 00'	
000035D7	02			2488+	DC HL1' 2'	m4 used
000035D8	01			2489+	DC HL1' 1'	m5 used
000035D9	01			2490+	DC HL1' 1'	CC
000035DA	0B			2491+	DC HL1' 11'	CC failed mask
000035DC	00000000 00000000			2492+	DS 2F	extracted PSW after test (has CC)
000035E4	FF			2493+	DC X' FF'	extracted CC, if test failed
000035E5	E5D7D2E2 40404040			2494+	DC CL8' VPKS'	instruction name
000035F0	00003668			2495+	DC A(RE48)	address of v1 result
000035F4	00003678			2496+	DC A(RE48+16)	address of v2 source
000035F8	00003688			2497+	DC A(RE48+32)	address of v3 source
000035FC	00000010			2498+	DC A(16)	result length
00003600	00003668			2499+REA48	DC A(RE48)	result address
00003608	00000000 00000000			2500+	DS 2FD	gap
00003610	00000000 00000000					
00003618	00000000 00000000			2501+V1048	DS XL16	V1 output
00003620	00000000 00000000					
00003628	00000000 00000000			2502+	DS 2FD	gap
00003630	00000000 00000000					
				2503+*		
00003638				2504+X48	DS 0F	
00003638	E310 5024 0014		00000024	2505+	LGF R1, V2ADDR	load v2 source
0000363E	E761 0000 0806		00000000	2506+	VL v22, 0(R1)	use v21 to test decoder
00003644	E310 5028 0014		00000028	2507+	LGF R1, V3ADDR	load v3 source
0000364A	E771 0000 0806		00000000	2508+	VL v23, 0(R1)	use v22 to test decoder
00003650	E756 7010 2E97			2509+	VPKS V21, V22, V23, 2, 1	test instruction
00003656	B98D 0020			2510+	EPSW R2, R0	extract psw
0000365A	5020 500C		0000000C	2511+	ST R2, CCPSW	to save CC
0000365E	E750 5048 080E		00003618	2512+	VST V21, V1048	save v1 output
00003664	07FB			2513+	BR R11	return
00003668				2514+RE48	DC 0F	V1 for this test
00003668				2515+	DROP R5	
00003668	11335577 19BB2DFF			2516	DC XL16' 1133557719BB2DFF 12037FFF7FFF7FFF'	result t
00003670	12037FFF 7FFF7FFF					
00003678	00001133 00005577			2517	DC XL16' 0000113300005577 000019BB00002DFF'	v2
00003680	000019BB 00002DFF					
00003688	00001203 04050607			2518	DC XL16' 0000120304050607 08090A0B0C0D0E0F'	v3
00003690	08090A0B 0C0D0E0F					
				2519		
00003698				2520	VRR_B VPKS, 2, 3	
00003698		00003698		2521+	DS 0FD	
00003698	00003700			2522+	USING *, R5	base for test data and test routine
0000369C	0031			2523+T49	DC A(X49)	address of test routine
0000369E	00			2524+	DC H' 49'	test number
0000369F	02			2525+	DC X' 00'	
000036A0	01			2526+	DC HL1' 2'	m4 used
000036A1	03			2527+	DC HL1' 1'	m5 used
000036A2	0E			2528+	DC HL1' 3'	CC
000036A4	00000000 00000000			2529+	DC HL1' 14'	CC failed mask
000036AC	FF			2530+	DS 2F	extracted PSW after test (has CC)
000036AD	E5D7D2E2 40404040			2531+	DC X' FF'	extracted CC, if test failed
000036B8	00003730			2532+	DC CL8' VPKS'	instruction name
				2533+	DC A(RE49)	address of v1 result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000036BC	00003740			2534+	DC	A(RE49+16)	address of v2 source
000036C0	00003750			2535+	DC	A(RE49+32)	address of v3 source
000036C4	00000010			2536+	DC	A(16)	result length
000036C8	00003730			2537+REA49	DC	A(RE49)	result address
000036D0	00000000 00000000			2538+	DS	2FD	gap
000036D8	00000000 00000000						
000036E0	00000000 00000000			2539+V1049	DS	XL16	V1 output
000036E8	00000000 00000000						
000036F0	00000000 00000000			2540+	DS	2FD	gap
000036F8	00000000 00000000						
				2541+*			
00003700				2542+X49	DS	0F	
00003700	E310 5024 0014		00000024	2543+	LGF	R1, V2ADDR	load v2 source
00003706	E761 0000 0806		00000000	2544+	VL	v22, 0(R1)	use v21 to test decoder
0000370C	E310 5028 0014		00000028	2545+	LGF	R1, V3ADDR	load v3 source
00003712	E771 0000 0806		00000000	2546+	VL	v23, 0(R1)	use v22 to test decoder
00003718	E756 7010 2E97			2547+	VPKS	V21, V22, V23, 2, 1	test instruction
0000371E	B98D 0020			2548+	EPSW	R2, R0	extract psw
00003722	5020 500C		0000000C	2549+	ST	R2, CCPSW	to save CC
00003726	E750 5048 080E		000036E0	2550+	VST	V21, V1049	save v1 output
0000372C	07FB			2551+	BR	R11	return
00003730				2552+RE49	DC	0F	V1 for this test
00003730				2553+	DROP	R5	
00003730	7FFF7FFF 7FFF7FFF			2554	DC	XL16' 7FFF7FFF7FFF7FFF 7FFF7FFF7FFF7FFF'	result
00003738	7FFF7FFF 7FFF7FFF						
00003740	01110133 01550177			2555	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00003748	019901BB 01DD01FF						
00003750	01010203 04050607			2556	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
00003758	08090A0B 0C0D0E0F						
				2557			
00003760				2558	VRR_B	VPKS, 2, 3	
00003760		00003760		2559+	DS	0FD	
00003760	000037C8			2560+	USING	*, R5	base for test data and test routine
00003764	0032			2561+T50	DC	A(X50)	address of test routine
00003766	00			2562+	DC	H' 50'	test number
00003767	02			2563+	DC	X' 00'	
00003768	01			2564+	DC	HL1' 2'	m4 used
00003768	01			2565+	DC	HL1' 1'	m5 used
00003769	03			2566+	DC	HL1' 3'	CC
0000376A	0E			2567+	DC	HL1' 14'	CC failed mask
0000376C	00000000 00000000			2568+	DS	2F	extracted PSW after test (has CC)
00003774	FF			2569+	DC	X' FF'	extracted CC, if test failed
00003775	E5D7D2E2 40404040			2570+	DC	CL8' VPKS'	instruction name
00003780	000037F8			2571+	DC	A(RE50)	address of v1 result
00003784	00003808			2572+	DC	A(RE50+16)	address of v2 source
00003788	00003818			2573+	DC	A(RE50+32)	address of v3 source
0000378C	00000010			2574+	DC	A(16)	result length
00003790	000037F8			2575+REA50	DC	A(RE50)	result address
00003798	00000000 00000000			2576+	DS	2FD	gap
000037A0	00000000 00000000						
000037A8	00000000 00000000			2577+V1050	DS	XL16	V1 output
000037B0	00000000 00000000						
000037B8	00000000 00000000			2578+	DS	2FD	gap
000037C0	00000000 00000000						
				2579+*			
000037C8				2580+X50	DS	0F	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000037C8	E310 5024 0014		00000024	2581+	LGF	R1, V2ADDR	load v2 source
000037CE	E761 0000 0806		00000000	2582+	VL	v22, 0(R1)	use v21 to test decoder
000037D4	E310 5028 0014		00000028	2583+	LGF	R1, V3ADDR	load v3 source
000037DA	E771 0000 0806		00000000	2584+	VL	v23, 0(R1)	use v22 to test decoder
000037E0	E756 7010 2E97			2585+	VPKS	V21, V22, V23, 2, 1	test instruction
000037E6	B98D 0020			2586+	EPSW	R2, R0	extract psw
000037EA	5020 500C		0000000C	2587+	ST	R2, CCPSW	to save CC
000037EE	E750 5048 080E		000037A8	2588+	VST	V21, V1050	save v1 output
000037F4	07FB			2589+	BR	R11	return
000037F8				2590+RE50	DC	0F	V1 for this test
000037F8				2591+	DROP	R5	
000037F8	7FFF7FFF 7FFF7FFF			2592	DC	XL16' 7FFF7FFF7FFF7FFF 7FFF7FFF7FFF7FFF'	result t
00003800	7FFF7FFF 7FFF7FFF						
00003808	01010203 04050607			2593	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
00003810	08090A0B 0C0D0E0F						
00003818	01110133 01550177			2594	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00003820	019901BB 01DD01FF						
00003828				2595			
00003828				2596	VRR_B	VPKS, 2, 3	
00003828		00003828		2597+	DS	0FD	
00003828	00003890			2598+	USING	*, R5	base for test data and test routine
0000382C	0033			2599+T51	DC	A(X51)	address of test routine
0000382E	00			2600+	DC	H' 51'	test number
0000382F	02			2601+	DC	X' 00'	
00003830	01			2602+	DC	HL1' 2'	m4 used
00003831	03			2603+	DC	HL1' 1'	m5 used
00003832	0E			2604+	DC	HL1' 3'	CC
00003832	0E			2605+	DC	HL1' 14'	CC failed mask
00003834	00000000 00000000			2606+	DS	2F	extracted PSW after test (has CC)
0000383C	FF			2607+	DC	X' FF'	extracted CC, if test failed
0000383D	E5D7D2E2 40404040			2608+	DC	CL8' VPKS'	instruction name
00003848	000038C0			2609+	DC	A(RE51)	address of v1 result
0000384C	000038D0			2610+	DC	A(RE51+16)	address of v2 source
00003850	000038E0			2611+	DC	A(RE51+32)	address of v3 source
00003854	00000010			2612+	DC	A(16)	result length
00003858	000038C0			2613+REA51	DC	A(RE51)	result address
00003860	00000000 00000000			2614+	DS	2FD	gap
00003868	00000000 00000000						
00003870	00000000 00000000			2615+V1051	DS	XL16	V1 output
00003878	00000000 00000000						
00003880	00000000 00000000			2616+	DS	2FD	gap
00003888	00000000 00000000						
00003890				2617+*			
00003890	E310 5024 0014		00000024	2618+X51	DS	0F	
00003896	E761 0000 0806		00000000	2619+	LGF	R1, V2ADDR	load v2 source
0000389C	E310 5028 0014		00000028	2620+	VL	v22, 0(R1)	use v21 to test decoder
000038A2	E771 0000 0806		00000000	2621+	LGF	R1, V3ADDR	load v3 source
000038A8	E756 7010 2E97			2622+	VL	v23, 0(R1)	use v22 to test decoder
000038AE	B98D 0020			2623+	VPKS	V21, V22, V23, 2, 1	test instruction
000038B2	5020 500C		0000000C	2624+	EPSW	R2, R0	extract psw
000038B6	E750 5048 080E		00003870	2625+	ST	R2, CCPSW	to save CC
000038BC	07FB			2626+	VST	V21, V1051	save v1 output
000038C0				2627+	BR	R11	return
000038C0				2628+RE51	DC	0F	V1 for this test
000038C0				2629+	DROP	R5	
000038C0	80008000 80008000			2630	DC	XL16' 8000800080008000 8000800080008000'	result t



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000038C8	80008000 80008000						
000038D0	F111F133 F155F177			2631	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v2
000038D8	F199F1BB F1DDF1FF						
000038E0	F101F203 F405F607			2632	DC	XL16' F101F203F405F607 F809FAFBFCFDFE0F'	v3
000038E8	F809FAFB FCFDFE0F						
				2633			
				2634	VRR_B	VPKS, 2, 3	
000038F0				2635+	DS	0FD	
000038F0		000038F0		2636+	USING	*, R5	base for test data and test routine
000038F0	00003958			2637+T52	DC	A(X52)	address of test routine
000038F4	0034			2638+	DC	H' 52'	test number
000038F6	00			2639+	DC	X' 00'	
000038F7	02			2640+	DC	HL1' 2'	m4 used
000038F8	01			2641+	DC	HL1' 1'	m5 used
000038F9	03			2642+	DC	HL1' 3'	CC
000038FA	0E			2643+	DC	HL1' 14'	CC failed mask
000038FC	00000000 00000000			2644+	DS	2F	extracted PSW after test (has CC)
00003904	FF			2645+	DC	X' FF'	extracted CC, if test failed
00003905	E5D7D2E2 40404040			2646+	DC	CL8' VPKS'	instruction name
00003910	00003988			2647+	DC	A(RE52)	address of v1 result
00003914	00003998			2648+	DC	A(RE52+16)	address of v2 source
00003918	000039A8			2649+	DC	A(RE52+32)	address of v3 source
0000391C	00000010			2650+	DC	A(16)	result length
00003920	00003988			2651+REA52	DC	A(RE52)	result address
00003928	00000000 00000000			2652+	DS	2FD	gap
00003930	00000000 00000000						
00003938	00000000 00000000			2653+V1052	DS	XL16	V1 output
00003940	00000000 00000000						
00003948	00000000 00000000			2654+	DS	2FD	gap
00003950	00000000 00000000						
				2655+*			
00003958				2656+X52	DS	0F	
00003958	E310 5024 0014		00000024	2657+	LGF	R1, V2ADDR	load v2 source
0000395E	E761 0000 0806		00000000	2658+	VL	v22, 0(R1)	use v21 to test decoder
00003964	E310 5028 0014		00000028	2659+	LGF	R1, V3ADDR	load v3 source
0000396A	E771 0000 0806		00000000	2660+	VL	v23, 0(R1)	use v22 to test decoder
00003970	E756 7010 2E97			2661+	VPKS	V21, V22, V23, 2, 1	test instruction
00003976	B98D 0020			2662+	EPSW	R2, R0	extract psw
0000397A	5020 500C		0000000C	2663+	ST	R2, CCPSW	to save CC
0000397E	E750 5048 080E		00003938	2664+	VST	V21, V1052	save v1 output
00003984	07FB			2665+	BR	R11	return
00003988				2666+RE52	DC	0F	V1 for this test
00003988				2667+	DROP	R5	
00003988	80008000 80008000			2668	DC	XL16' 8000800080008000 8000800080008000'	result t
00003990	80008000 80008000						
00003998	F101F203 F405F607			2669	DC	XL16' F101F203F405F607 F809FAFBFCFDFE0F'	v2
000039A0	F809FAFB FCFDFE0F						
000039A8	F111F133 F155F177			2670	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v3
000039B0	F199F1BB F1DDF1FF						
				2671			
				2672 *Doubleword			
				2673	VRR_B	VPKS, 3, 0	
000039B8				2674+	DS	0FD	
000039B8		000039B8		2675+	USING	*, R5	base for test data and test routine
000039B8	00003A20			2676+T53	DC	A(X53)	address of test routine
000039BC	0035			2677+	DC	H' 53'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000039BE	00			2678+	DC	X' 00'		
000039BF	03			2679+	DC	HL1' 3'	m4 used	
000039C0	01			2680+	DC	HL1' 1'	m5 used	
000039C1	00			2681+	DC	HL1' 0'	CC	
000039C2	07			2682+	DC	HL1' 7'	CC failed mask	
000039C4	00000000	00000000		2683+	DS	2F	extracted PSW after test (has CC)	
000039CC	FF			2684+	DC	X' FF'	extracted CC, if test failed	
000039CD	E5D7D2E2	40404040		2685+	DC	CL8' VPKS'	instruction name	
000039D8	00003A50			2686+	DC	A(RE53)	address of v1 result	
000039DC	00003A60			2687+	DC	A(RE53+16)	address of v2 source	
000039E0	00003A70			2688+	DC	A(RE53+32)	address of v3 source	
000039E4	00000010			2689+	DC	A(16)	result length	
000039E8	00003A50			2690+REA53	DC	A(RE53)	result address	
000039F0	00000000	00000000		2691+	DS	2FD	gap	
000039F8	00000000	00000000						
00003A00	00000000	00000000		2692+V1053	DS	XL16	V1 output	
00003A08	00000000	00000000						
00003A10	00000000	00000000		2693+	DS	2FD	gap	
00003A18	00000000	00000000						
00003A20				2694+*				
00003A20	E310 5024 0014		00000024	2695+X53	DS	0F		
00003A26	E761 0000 0806		00000000	2696+	LGF	R1, V2ADDR	load v2 source	
00003A2C	E310 5028 0014		00000028	2697+	VL	v22, 0(R1)	use v21 to test decoder	
00003A32	E771 0000 0806		00000000	2698+	LGF	R1, V3ADDR	load v3 source	
00003A38	E756 7010 3E97		00000000	2699+	VL	v23, 0(R1)	use v22 to test decoder	
00003A3E	B98D 0020			2700+	VPKS	V21, V22, V23, 3, 1	test instruction	
00003A42	5020 500C		0000000C	2701+	EPSW	R2, R0	extract psw	
00003A46	E750 5048 080E		00003A00	2702+	ST	R2, CCPSW	to save CC	
00003A4C	07FB			2703+	VST	V21, V1053	save v1 output	
00003A50				2704+	BR	R11	return	
00003A50				2705+RE53	DC	0F	V1 for this test	
00003A50	11335577 22446688			2706+	DROP	R5		
00003A58	FEFDFCFB FAF9F8F7			2707	DC	XL16' 1133557722446688 FEFDFCFBFAF9F8F7'	result t	
00003A60	00000000 11335577			2708	DC	XL16' 0000000011335577 0000000022446688'	v2	
00003A68	00000000 22446688							
00003A70	FFFFFFFF FEFDFCFB			2709	DC	XL16' FFFFFFFFFFEFDFCFB FFFFFFFFFFAF9F8F7'	v3	
00003A78	FFFFFFFF FAF9F8F7							
00003A80				2710				
00003A80				2711	VRR_B	VPKS, 3, 0		
00003A80	00003AE8	00003A80		2712+	DS	0FD		
00003A80	0036			2713+	USING	*, R5	base for test data and test routine	
00003A84	0036			2714+T54	DC	A(X54)	address of test routine	
00003A86	00			2715+	DC	H' 54'	test number	
00003A86	00			2716+	DC	X' 00'		
00003A87	03			2717+	DC	HL1' 3'	m4 used	
00003A88	01			2718+	DC	HL1' 1'	m5 used	
00003A89	00			2719+	DC	HL1' 0'	CC	
00003A8A	07			2720+	DC	HL1' 7'	CC failed mask	
00003A8C	00000000	00000000		2721+	DS	2F	extracted PSW after test (has CC)	
00003A94	FF			2722+	DC	X' FF'	extracted CC, if test failed	
00003A95	E5D7D2E2	40404040		2723+	DC	CL8' VPKS'	instruction name	
00003AA0	00003B18			2724+	DC	A(RE54)	address of v1 result	
00003AA4	00003B28			2725+	DC	A(RE54+16)	address of v2 source	
00003AA8	00003B38			2726+	DC	A(RE54+32)	address of v3 source	
00003AAC	00000010			2727+	DC	A(16)	result length	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003AB0	00003B18			2728+REA54	DC	A(RE54)	result address
00003AB8	00000000 00000000			2729+	DS	2FD	gap
00003AC0	00000000 00000000						
00003AC8	00000000 00000000			2730+V1054	DS	XL16	V1 output
00003AD0	00000000 00000000						
00003AD8	00000000 00000000			2731+	DS	2FD	gap
00003AE0	00000000 00000000						
				2732+*			
00003AE8				2733+X54	DS	0F	
00003AE8	E310 5024 0014		00000024	2734+	LGF	R1, V2ADDR	load v2 source
00003AEE	E761 0000 0806		00000000	2735+	VL	v22, 0(R1)	use v21 to test decoder
00003AF4	E310 5028 0014		00000028	2736+	LGF	R1, V3ADDR	load v3 source
00003AFA	E771 0000 0806		00000000	2737+	VL	v23, 0(R1)	use v22 to test decoder
00003B00	E756 7010 3E97			2738+	VPKS	V21, V22, V23, 3, 1	test instruction
00003B06	B98D 0020			2739+	EPSW	R2, R0	extract psw
00003B0A	5020 500C		0000000C	2740+	ST	R2, CCPSW	to save CC
00003B0E	E750 5048 080E		00003AC8	2741+	VST	V21, V1054	save v1 output
00003B14	07FB			2742+	BR	R11	return
00003B18				2743+RE54	DC	0F	V1 for this test
00003B18				2744+	DROP	R5	
00003B18	FEFDFCFB FAF9F8F7			2745	DC	XL16' FEFDFCFBFAF9F8F7 1133557722446688 '	result
00003B20	11335577 22446688						
00003B28	FFFFFFFF FEFDFCFB			2746	DC	XL16' FFFFFFFFFFEFDFCFB FFFFFFFFFFAF9F8F7'	v2
00003B30	FFFFFFFF FAF9F8F7						
00003B38	00000000 11335577			2747	DC	XL16' 0000000011335577 0000000022446688'	v3
00003B40	00000000 22446688						
				2748			
				2749	VRR_B	VPKS, 3, 1	
00003B48				2750+	DS	0FD	
00003B48		00003B48		2751+	USING	*, R5	base for test data and test routine
00003B48	00003BB0			2752+T55	DC	A(X55)	address of test routine
00003B4C	0037			2753+	DC	H' 55'	test number
00003B4E	00			2754+	DC	X' 00'	
00003B4F	03			2755+	DC	HL1' 3'	m4 used
00003B50	01			2756+	DC	HL1' 1'	m5 used
00003B51	01			2757+	DC	HL1' 1'	CC
00003B52	0B			2758+	DC	HL1' 11'	CC failed mask
00003B54	00000000 00000000			2759+	DS	2F	extracted PSW after test (has CC)
00003B5C	FF			2760+	DC	X' FF'	extracted CC, if test failed
00003B5D	E5D7D2E2 40404040			2761+	DC	CL8' VPKS'	instruction name
00003B68	00003BE0			2762+	DC	A(RE55)	address of v1 result
00003B6C	00003BF0			2763+	DC	A(RE55+16)	address of v2 source
00003B70	00003C00			2764+	DC	A(RE55+32)	address of v3 source
00003B74	00000010			2765+	DC	A(16)	result length
00003B78	00003BE0			2766+REA55	DC	A(RE55)	result address
00003B80	00000000 00000000			2767+	DS	2FD	gap
00003B88	00000000 00000000						
00003B90	00000000 00000000			2768+V1055	DS	XL16	V1 output
00003B98	00000000 00000000						
00003BA0	00000000 00000000			2769+	DS	2FD	gap
00003BA8	00000000 00000000						
				2770+*			
00003BB0				2771+X55	DS	0F	
00003BB0	E310 5024 0014		00000024	2772+	LGF	R1, V2ADDR	load v2 source
00003BB6	E761 0000 0806		00000000	2773+	VL	v22, 0(R1)	use v21 to test decoder
00003BBC	E310 5028 0014		00000028	2774+	LGF	R1, V3ADDR	load v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00003BC2	E771 0000 0806		00000000	2775+	VL	v23, 0(R1)	use v22 to test decoder	
00003BC8	E756 7010 3E97			2776+	VPKS	V21, V22, V23, 3, 1	test instruction	
00003BCE	B98D 0020			2777+	EPSW	R2, R0	extract psw	
00003BD2	5020 500C		0000000C	2778+	ST	R2, CCPSW	to save CC	
00003BD6	E750 5048 080E		00003B90	2779+	VST	V21, V1055	save v1 output	
00003BDC	07FB			2780+	BR	R11	return	
00003BE0				2781+RE55	DC	0F	V1 for this test	
00003BE0				2782+	DROP	R5		
00003BE0	12030405 7FFFFFFF			2783	DC	XL16' 120304057FFFFFFF 1133557719BB2DFF'	result t	
00003BE8	11335577 19BB2DFF							
00003BF0	00000000 12030405			2784	DC	XL16' 0000000012030405 08090A0B0C0D0E0F'	v2	
00003BF8	08090A0B 0C0D0E0F							
00003C00	00000000 11335577			2785	DC	XL16' 0000000011335577 0000000019BB2DFF'	v3	
00003C08	00000000 19BB2DFF							
				2786				
				2787	VRR_B	VPKS, 3, 1		
00003C10				2788+	DS	0FD		
00003C10		00003C10		2789+	USING	*, R5	base for test data and test routine	
00003C10	00003C78			2790+T56	DC	A(X56)	address of test routine	
00003C14	0038			2791+	DC	H' 56'	test number	
00003C16	00			2792+	DC	X' 00'		
00003C17	03			2793+	DC	HL1' 3'	m4 used	
00003C18	01			2794+	DC	HL1' 1'	m5 used	
00003C19	01			2795+	DC	HL1' 1'	CC	
00003C1A	0B			2796+	DC	HL1' 11'	CC failed mask	
00003C1C	00000000 00000000			2797+	DS	2F	extracted PSW after test (has CC)	
00003C24	FF			2798+	DC	X' FF'	extracted CC, if test failed	
00003C25	E5D7D2E2 40404040			2799+	DC	CL8' VPKS'	instruction name	
00003C30	00003CA8			2800+	DC	A(RE56)	address of v1 result	
00003C34	00003CB8			2801+	DC	A(RE56+16)	address of v2 source	
00003C38	00003CC8			2802+	DC	A(RE56+32)	address of v3 source	
00003C3C	00000010			2803+	DC	A(16)	result length	
00003C40	00003CA8			2804+REA56	DC	A(RE56)	result address	
00003C48	00000000 00000000			2805+	DS	2FD	gap	
00003C50	00000000 00000000							
00003C58	00000000 00000000			2806+V1056	DS	XL16	V1 output	
00003C60	00000000 00000000							
00003C68	00000000 00000000			2807+	DS	2FD	gap	
00003C70	00000000 00000000							
				2808+*				
00003C78				2809+X56	DS	0F		
00003C78	E310 5024 0014		00000024	2810+	LGF	R1, V2ADDR	load v2 source	
00003C7E	E761 0000 0806		00000000	2811+	VL	v22, 0(R1)	use v21 to test decoder	
00003C84	E310 5028 0014		00000028	2812+	LGF	R1, V3ADDR	load v3 source	
00003C8A	E771 0000 0806		00000000	2813+	VL	v23, 0(R1)	use v22 to test decoder	
00003C90	E756 7010 3E97			2814+	VPKS	V21, V22, V23, 3, 1	test instruction	
00003C96	B98D 0020			2815+	EPSW	R2, R0	extract psw	
00003C9A	5020 500C		0000000C	2816+	ST	R2, CCPSW	to save CC	
00003C9E	E750 5048 080E		00003C58	2817+	VST	V21, V1056	save v1 output	
00003CA4	07FB			2818+	BR	R11	return	
00003CA8				2819+RE56	DC	0F	V1 for this test	
00003CA8				2820+	DROP	R5		
00003CA8	11335577 19BB2DFF			2821	DC	XL16' 1133557719BB2DFF 120304057FFFFFFF'	result t	
00003CB0	12030405 7FFFFFFF							
00003CB8	00000000 11335577			2822	DC	XL16' 0000000011335577 0000000019BB2DFF'	v2	
00003CC0	00000000 19BB2DFF							



LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00003CC8	00000000 12030405			2823	DC	XL16' 0000000012030405 08090A0B0C0D0E0F'	v3		
00003CD0	08090A0B 0C0D0E0F								
				2824					
00003CD8				2825	VRR_B	VPKS, 3, 3			
00003CD8		00003CD8		2826+	DS	0FD			
00003CD8	00003D40			2827+	USING	*, R5	base for test data and test routine		
00003CDC	0039			2828+T57	DC	A(X57)	address of test routine		
00003CDE	00			2829+	DC	H' 57'	test number		
00003CDF	03			2830+	DC	X' 00'			
00003CE0	01			2831+	DC	HL1' 3'	m4 used		
00003CE1	03			2832+	DC	HL1' 1'	m5 used		
00003CE2	0E			2833+	DC	HL1' 3'	CC		
00003CE4	00000000 00000000			2834+	DC	HL1' 14'	CC failed mask		
00003CEC	FF			2835+	DS	2F	extracted PSW after test (has CC)		
00003CED	E5D7D2E2 40404040			2836+	DC	X' FF'	extracted CC, if test failed		
00003CF8	00003D70			2837+	DC	CL8' VPKS'	instruction name		
00003CFC	00003D80			2838+	DC	A(RE57)	address of v1 result		
00003D00	00003D90			2839+	DC	A(RE57+16)	address of v2 source		
00003D04	00000010			2840+	DC	A(RE57+32)	address of v3 source		
00003D08	00003D70			2841+	DC	A(16)	result length		
00003D10	00000000 00000000			2842+REA57	DC	A(RE57)	result address		
00003D18	00000000 00000000			2843+	DS	2FD	gap		
00003D20	00000000 00000000			2844+V1057	DS	XL16	V1 output		
00003D28	00000000 00000000								
00003D30	00000000 00000000			2845+	DS	2FD	gap		
00003D38	00000000 00000000								
				2846+*					
00003D40				2847+X57	DS	0F			
00003D40	E310 5024 0014		00000024	2848+	LGF	R1, V2ADDR	load v2 source		
00003D46	E761 0000 0806		00000000	2849+	VL	v22, 0(R1)	use v21 to test decoder		
00003D4C	E310 5028 0014		00000028	2850+	LGF	R1, V3ADDR	load v3 source		
00003D52	E771 0000 0806		00000000	2851+	VL	v23, 0(R1)	use v22 to test decoder		
00003D58	E756 7010 3E97			2852+	VPKS	V21, V22, V23, 3, 1	test instruction		
00003D5E	B98D 0020			2853+	EPSW	R2, R0	extract psw		
00003D62	5020 500C		0000000C	2854+	ST	R2, CCPSW	to save CC		
00003D66	E750 5048 080E		00003D20	2855+	VST	V21, V1057	save v1 output		
00003D6C	07FB			2856+	BR	R11	return		
00003D70				2857+RE57	DC	0F	V1 for this test		
00003D70				2858+	DROP	R5			
00003D70	7FFFFFFF 7FFFFFFF			2859	DC	XL16' 7FFFFFFF7FFFFFFF 7FFFFFFF7FFFFFFF'	result t		
00003D78	7FFFFFFF 7FFFFFFF								
00003D80	01110133 01550177			2860	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2		
00003D88	019901BB 01DD01FF								
00003D90	01010203 04050607			2861	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3		
00003D98	08090A0B 0C0D0E0F								
				2862					
00003DA0				2863	VRR_B	VPKS, 3, 3			
00003DA0		00003DA0		2864+	DS	0FD			
00003DA0	00003E08			2865+	USING	*, R5	base for test data and test routine		
00003DA4	003A			2866+T58	DC	A(X58)	address of test routine		
00003DA6	00			2867+	DC	H' 58'	test number		
00003DA7	03			2868+	DC	X' 00'			
00003DA8	01			2869+	DC	HL1' 3'	m4 used		
00003DA8	01			2870+	DC	HL1' 1'	m5 used		
00003DA9	03			2871+	DC	HL1' 3'	CC		



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003DAA	0E			2872+	DC	HL1' 14'	CC failed mask
00003DAC	00000000 00000000			2873+	DS	2F	extracted PSW after test (has CC)
00003DB4	FF			2874+	DC	X' FF'	extracted CC, if test failed
00003DB5	E5D7D2E2 40404040			2875+	DC	CL8' VPKS'	instruction name
00003DC0	00003E38			2876+	DC	A(RE58)	address of v1 result
00003DC4	00003E48			2877+	DC	A(RE58+16)	address of v2 source
00003DC8	00003E58			2878+	DC	A(RE58+32)	address of v3 source
00003DCC	00000010			2879+	DC	A(16)	result length
00003DD0	00003E38			2880+REA58	DC	A(RE58)	result address
00003DD8	00000000 00000000			2881+	DS	2FD	gap
00003DE0	00000000 00000000						
00003DE8	00000000 00000000			2882+V1058	DS	XL16	V1 output
00003DF0	00000000 00000000						
00003DF8	00000000 00000000			2883+	DS	2FD	gap
00003E00	00000000 00000000						
00003E08				2884+*			
00003E08	E310 5024 0014		00000024	2885+X58	DS	0F	
00003E0E	E761 0000 0806		00000000	2886+	LGF	R1, V2ADDR	load v2 source
00003E14	E310 5028 0014		00000028	2887+	VL	v22, 0(R1)	use v21 to test decoder
00003E1A	E771 0000 0806		00000000	2888+	LGF	R1, V3ADDR	load v3 source
00003E20	E756 7010 3E97			2889+	VL	v23, 0(R1)	use v22 to test decoder
00003E26	B98D 0020			2890+	VPKS	V21, V22, V23, 3, 1	test instruction
00003E2A	5020 500C		0000000C	2891+	EPSW	R2, R0	extract psw
00003E2E	E750 5048 080E		00003DE8	2892+	ST	R2, CCPSW	to save CC
00003E34	07FB			2893+	VST	V21, V1058	save v1 output
00003E38				2894+	BR	R11	return
00003E38				2895+RE58	DC	0F	V1 for this test
00003E38				2896+	DROP	R5	
00003E38	7FFFFFFF 7FFFFFFF			2897	DC	XL16' 7FFFFFFF7FFFFFFF 7FFFFFFF7FFFFFFF'	result t
00003E40	7FFFFFFF 7FFFFFFF						
00003E48	01010203 04050607			2898	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
00003E50	08090A0B 0C0D0E0F						
00003E58	01110133 01550177			2899	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00003E60	019901BB 01DD01FF						
00003E68				2900			
00003E68		00003E68		2901	VRR_B	VPKS, 3, 3	
00003E68	00003ED0			2902+	DS	0FD	
00003E6C	003B			2903+	USING	*, R5	base for test data and test routine
00003E6E	00			2904+T59	DC	A(X59)	address of test routine
00003E6F	03			2905+	DC	H' 59'	test number
00003E70	01			2906+	DC	X' 00'	
00003E71	03			2907+	DC	HL1' 3'	m4 used
00003E72	0E			2908+	DC	HL1' 1'	m5 used
00003E74	00000000 00000000			2909+	DC	HL1' 3'	CC
00003E7C	FF			2910+	DC	HL1' 14'	CC failed mask
00003E7D	E5D7D2E2 40404040			2911+	DS	2F	extracted PSW after test (has CC)
00003E88	00003F00			2912+	DC	X' FF'	extracted CC, if test failed
00003E8C	00003F10			2913+	DC	CL8' VPKS'	instruction name
00003E90	00003F20			2914+	DC	A(RE59)	address of v1 result
00003E94	00000010			2915+	DC	A(RE59+16)	address of v2 source
00003E98	00003F00			2916+	DC	A(RE59+32)	address of v3 source
00003EA0	00000000 00000000			2917+	DC	A(16)	result length
00003EA8	00000000 00000000			2918+REA59	DC	A(RE59)	result address
00003EB0	00000000 00000000			2919+	DS	2FD	gap
				2920+V1059	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00003EB8	00000000	00000000						
00003EC0	00000000	00000000		2921+	DS	2FD	gap	
00003EC8	00000000	00000000						
				2922+*				
00003ED0				2923+X59	DS	0F		
00003ED0	E310 5024 0014		00000024	2924+	LGF	R1, V2ADDR	load v2 source	
00003ED6	E761 0000 0806		00000000	2925+	VL	v22, 0(R1)	use v21 to test decoder	
00003EDC	E310 5028 0014		00000028	2926+	LGF	R1, V3ADDR	load v3 source	
00003EE2	E771 0000 0806		00000000	2927+	VL	v23, 0(R1)	use v22 to test decoder	
00003EE8	E756 7010 3E97			2928+	VPKS	V21, V22, V23, 3, 1	test instruction	
00003EEE	B98D 0020			2929+	EPSW	R2, R0	extract psw	
00003EF2	5020 500C		0000000C	2930+	ST	R2, CCPSW	to save CC	
00003EF6	E750 5048 080E		00003EB0	2931+	VST	V21, V1059	save v1 output	
00003EFC	07FB			2932+	BR	R11	return	
00003F00				2933+RE59	DC	0F	V1 for this test	
00003F00				2934+	DROP	R5		
00003F00	80000000	80000000		2935	DC	XL16' 8000000080000000 8000000080000000'	result t	
00003F08	80000000	80000000						
00003F10	F111F133 F155F177			2936	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v2	
00003F18	F199F1BB F1DDF1FF							
00003F20	F101F203 F405F607			2937	DC	XL16' F101F203F405F607 F809FAFBFCDFE0F'	v3	
00003F28	F809FAFB FCDFE0F							
				2938				
00003F30				2939	VRR_B	VPKS, 3, 3		
00003F30		00003F30		2940+	DS	0FD		
00003F30	00003F98			2941+	USING	*, R5	base for test data and test routine	
00003F34	003C			2942+T60	DC	A(X60)	address of test routine	
00003F36	00			2943+	DC	H' 60'	test number	
00003F37	03			2944+	DC	X' 00'		
00003F38	01			2945+	DC	HL1' 3'	m4 used	
00003F39	03			2946+	DC	HL1' 1'	m5 used	
00003F3A	0E			2947+	DC	HL1' 3'	CC	
00003F3C	00000000 00000000			2948+	DC	HL1' 14'	CC failed mask	
00003F44	FF			2949+	DS	2F	extracted PSW after test (has CC)	
00003F45	E5D7D2E2 40404040			2950+	DC	X' FF'	extracted CC, if test failed	
00003F50	00003FC8			2951+	DC	CL8' VPKS'	instruction name	
00003F54	00003FD8			2952+	DC	A(RE60)	address of v1 result	
00003F58	00003FE8			2953+	DC	A(RE60+16)	address of v2 source	
00003F5C	00000010			2954+	DC	A(RE60+32)	address of v3 source	
00003F60	00003FC8			2955+	DC	A(16)	result length	
00003F68	00000000 00000000			2956+REA60	DC	A(RE60)	result address	
00003F70	00000000 00000000			2957+	DS	2FD	gap	
00003F78	00000000 00000000			2958+V1060	DS	XL16	V1 output	
00003F80	00000000 00000000							
00003F88	00000000 00000000			2959+	DS	2FD	gap	
00003F90	00000000 00000000							
				2960+*				
00003F98				2961+X60	DS	0F		
00003F98	E310 5024 0014		00000024	2962+	LGF	R1, V2ADDR	load v2 source	
00003F9E	E761 0000 0806		00000000	2963+	VL	v22, 0(R1)	use v21 to test decoder	
00003FA4	E310 5028 0014		00000028	2964+	LGF	R1, V3ADDR	load v3 source	
00003FAA	E771 0000 0806		00000000	2965+	VL	v23, 0(R1)	use v22 to test decoder	
00003FB0	E756 7010 3E97			2966+	VPKS	V21, V22, V23, 3, 1	test instruction	
00003FB6	B98D 0020			2967+	EPSW	R2, R0	extract psw	
00003FBA	5020 500C		0000000C	2968+	ST	R2, CCPSW	to save CC	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003FBE	E750 5048 080E		00003F78	2969+	VST	V21, V1060	save v1 output
00003FC4	07FB			2970+	BR	R11	return
00003FC8				2971+RE60	DC	0F	V1 for this test
00003FC8				2972+	DROP	R5	
00003FC8	80000000 80000000			2973	DC	XL16' 8000000080000000 8000000080000000'	result t
00003FD0	80000000 80000000						
00003FD8	F101F203 F405F607			2974	DC	XL16' F101F203F405F607 F809FAFBFCDFE0F'	v2
00003FE0	F809FAFB FCFDFE0F						
00003FE8	F111F133 F155F177			2975	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v3
00003FF0	F199F1BB F1DDF1FF						
				2976			
				2977 *			
				2978 *	VCEQ	- Vector Compare Equal	
				2979 *			
				2980 *	cc=0:	All elements equal	
				2981 *	cc=1:	At least one, but not all elements equal	
				2982 *	cc=3:	No element equal	
				2983 *			
				2984 *	case -	simple cc debug	
				2985 *			
				2986 *	Byte		
				2987	VRR_B	VCEQ, 0, 0	
00003FF8				2988+	DS	0FD	
00003FF8		00003FF8		2989+	USING	*, R5	base for test data and test routine
00003FF8	00004060			2990+T61	DC	A(X61)	address of test routine
00003FFC	003D			2991+	DC	H' 61'	test number
00003FFE	00			2992+	DC	X' 00'	
00003FFF	00			2993+	DC	HL1' 0'	m4 used
00004000	01			2994+	DC	HL1' 1'	m5 used
00004001	00			2995+	DC	HL1' 0'	CC
00004002	07			2996+	DC	HL1' 7'	CC failed mask
00004004	00000000 00000000			2997+	DS	2F	extracted PSW after test (has CC)
0000400C	FF			2998+	DC	X' FF'	extracted CC, if test failed
0000400D	E5C3C5D8 40404040			2999+	DC	CL8' VCEQ'	instruction name
00004018	00004090			3000+	DC	A(RE61)	address of v1 result
0000401C	000040A0			3001+	DC	A(RE61+16)	address of v2 source
00004020	000040B0			3002+	DC	A(RE61+32)	address of v3 source
00004024	00000010			3003+	DC	A(16)	result length
00004028	00004090			3004+REA61	DC	A(RE61)	result address
00004030	00000000 00000000			3005+	DS	2FD	gap
00004038	00000000 00000000						
00004040	00000000 00000000			3006+V1061	DS	XL16	V1 output
00004048	00000000 00000000						
00004050	00000000 00000000			3007+	DS	2FD	gap
00004058	00000000 00000000						
				3008+*			
00004060				3009+X61	DS	0F	
00004060	E310 5024 0014		00000024	3010+	LGF	R1, V2ADDR	load v2 source
00004066	E761 0000 0806		00000000	3011+	VL	v22, 0(R1)	use v21 to test decoder
0000406C	E310 5028 0014		00000028	3012+	LGF	R1, V3ADDR	load v3 source
00004072	E771 0000 0806		00000000	3013+	VL	v23, 0(R1)	use v22 to test decoder
00004078	E756 7010 0EF8			3014+	VCEQ	V21, V22, V23, 0, 1	test instruction
0000407E	B98D 0020			3015+	EPSW	R2, R0	extract psw
00004082	5020 500C		0000000C	3016+	ST	R2, CCPSW	to save CC
00004086	E750 5048 080E		00004040	3017+	VST	V21, V1061	save v1 output
0000408C	07FB			3018+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004090				3019+RE61	DC	0F	V1 for this test
00004090				3020+	DROP	R5	
00004090	FFFFFFFF FFFFFFFF			3021	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00004098	FFFFFFFF FFFFFFFF						
000040A0	00000000 00000000			3022	DC	XL16' 0000000000000000 0000000000000000'	v2
000040A8	00000000 00000000						
000040B0	00000000 00000000			3023	DC	XL16' 0000000000000000 0000000000000000'	v3
000040B8	00000000 00000000						
				3024			
000040C0				3025	VRR_B	VCEQ, 0, 1	
000040C0		000040C0		3026+	DS	0FD	
000040C0	00004128			3027+	USING	*, R5	base for test data and test routine
000040C4	003E			3028+T62	DC	A(X62)	address of test routine
000040C6	00			3029+	DC	H' 62'	test number
000040C7	00			3030+	DC	X' 00'	
000040C8	01			3031+	DC	HL1' 0'	m4 used
000040C9	01			3032+	DC	HL1' 1'	m5 used
000040CA	0B			3033+	DC	HL1' 1'	CC
000040CC	00000000 00000000			3034+	DC	HL1' 11'	CC failed mask
000040D4	FF			3035+	DS	2F	extracted PSW after test (has CC)
000040D5	E5C3C5D8 40404040			3036+	DC	X' FF'	extracted CC, if test failed
000040E0	00004158			3037+	DC	CL8' VCEQ'	instruction name
000040E4	00004168			3038+	DC	A(RE62)	address of v1 result
000040E8	00004178			3039+	DC	A(RE62+16)	address of v2 source
000040EC	00000010			3040+	DC	A(RE62+32)	address of v3 source
000040F0	00004158			3041+	DC	A(16)	result length
000040F8	00000000 00000000			3042+REA62	DC	A(RE62)	result address
00004100	00000000 00000000			3043+	DS	2FD	gap
00004108	00000000 00000000			3044+V1062	DS	XL16	V1 output
00004110	00000000 00000000						
00004118	00000000 00000000			3045+	DS	2FD	gap
00004120	00000000 00000000						
				3046+*			
00004128				3047+X62	DS	0F	
00004128	E310 5024 0014		00000024	3048+	LGF	R1, V2ADDR	load v2 source
0000412E	E761 0000 0806		00000000	3049+	VL	v22, 0(R1)	use v21 to test decoder
00004134	E310 5028 0014		00000028	3050+	LGF	R1, V3ADDR	load v3 source
0000413A	E771 0000 0806		00000000	3051+	VL	v23, 0(R1)	use v22 to test decoder
00004140	E756 7010 0EF8			3052+	VCEQ	V21, V22, V23, 0, 1	test instruction
00004146	B98D 0020			3053+	EPSW	R2, R0	extract psw
0000414A	5020 500C		0000000C	3054+	ST	R2, CCPSW	to save CC
0000414E	E750 5048 080E		00004108	3055+	VST	V21, V1062	save v1 output
00004154	07FB			3056+	BR	R11	return
00004158				3057+RE62	DC	0F	V1 for this test
00004158				3058+	DROP	R5	
00004158	FFFFFFFF FFFFFFFF			3059	DC	XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result
00004160	00000000 FFFFFFFF						
00004168	00000000 00000000			3060	DC	XL16' 0000000000000000 0000000000000000'	v2
00004170	00000000 00000000						
00004178	00000000 00000000			3061	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00004180	8FFF8FFF 00000000						
				3062			
00004188				3063	VRR_B	VCEQ, 0, 3	
00004188		00004188		3064+	DS	0FD	
				3065+	USING	*, R5	base for test data and test routine



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004188	000041F0			3066+T63	DC	A(X63)	address of test routine
0000418C	003F			3067+	DC	H' 63'	test number
0000418E	00			3068+	DC	X' 00'	
0000418F	00			3069+	DC	HL1' 0'	m4 used
00004190	01			3070+	DC	HL1' 1'	m5 used
00004191	03			3071+	DC	HL1' 3'	CC
00004192	0E			3072+	DC	HL1' 14'	CC failed mask
00004194	00000000 00000000			3073+	DS	2F	extracted PSW after test (has CC)
0000419C	FF			3074+	DC	X' FF'	extracted CC, if test failed
0000419D	E5C3C5D8 40404040			3075+	DC	CL8' VCEQ'	instruction name
000041A8	00004220			3076+	DC	A(RE63)	address of v1 result
000041AC	00004230			3077+	DC	A(RE63+16)	address of v2 source
000041B0	00004240			3078+	DC	A(RE63+32)	address of v3 source
000041B4	00000010			3079+	DC	A(16)	result length
000041B8	00004220			3080+REA63	DC	A(RE63)	result address
000041C0	00000000 00000000			3081+	DS	2FD	gap
000041C8	00000000 00000000						
000041D0	00000000 00000000			3082+V1063	DS	XL16	V1 output
000041D8	00000000 00000000						
000041E0	00000000 00000000			3083+	DS	2FD	gap
000041E8	00000000 00000000						
000041F0				3084+*			
000041F0	E310 5024 0014			3085+X63	DS	0F	
000041F6	E761 0000 0806		00000024	3086+	LGF	R1, V2ADDR	load v2 source
000041FC	E310 5028 0014		00000000	3087+	VL	v22, 0(R1)	use v21 to test decoder
00004202	E771 0000 0806		00000028	3088+	LGF	R1, V3ADDR	load v3 source
00004208	E756 7010 0EF8		00000000	3089+	VL	v23, 0(R1)	use v22 to test decoder
0000420E	B98D 0020			3090+	VCEQ	V21, V22, V23, 0, 1	test instruction
00004212	5020 500C			3091+	EPSW	R2, R0	extract psw
00004216	E750 5048 080E		0000000C	3092+	ST	R2, CCPSW	to save CC
0000421C	07FB		000041D0	3093+	VST	V21, V1063	save v1 output
00004220				3094+	BR	R11	return
00004220				3095+RE63	DC	0F	V1 for this test
00004220				3096+	DROP	R5	
00004220	00000000 00000000			3097	DC	XL16' 0000000000000000 0000000000000000'	result t
00004228	00000000 00000000						
00004230	FFFFFFFF FFFFFFFF			3098	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00004238	FFFFFFFF FFFFFFFF						
00004240	00000000 00000000			3099	DC	XL16' 0000000000000000 0000000000000000'	v3
00004248	00000000 00000000						
				3100			
				3101 *Halfword			
				3102	VRR_B	VCEQ, 1, 0	
00004250				3103+	DS	0FD	
00004250		00004250		3104+	USING	*, R5	base for test data and test routine
00004250	000042B8			3105+T64	DC	A(X64)	address of test routine
00004254	0040			3106+	DC	H' 64'	test number
00004256	00			3107+	DC	X' 00'	
00004257	01			3108+	DC	HL1' 1'	m4 used
00004258	01			3109+	DC	HL1' 1'	m5 used
00004259	00			3110+	DC	HL1' 0'	CC
0000425A	07			3111+	DC	HL1' 7'	CC failed mask
0000425C	00000000 00000000			3112+	DS	2F	extracted PSW after test (has CC)
00004264	FF			3113+	DC	X' FF'	extracted CC, if test failed
00004265	E5C3C5D8 40404040			3114+	DC	CL8' VCEQ'	instruction name
00004270	000042E8			3115+	DC	A(RE64)	address of v1 result



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004274	000042F8			3116+	DC	A(RE64+16)	address of v2 source
00004278	00004308			3117+	DC	A(RE64+32)	address of v3 source
0000427C	00000010			3118+	DC	A(16)	result length
00004280	000042E8			3119+REA64	DC	A(RE64)	result address
00004288	00000000 00000000			3120+	DS	2FD	gap
00004290	00000000 00000000						
00004298	00000000 00000000			3121+V1064	DS	XL16	V1 output
000042A0	00000000 00000000						
000042A8	00000000 00000000			3122+	DS	2FD	gap
000042B0	00000000 00000000						
				3123+*			
000042B8				3124+X64	DS	0F	
000042B8	E310 5024 0014		00000024	3125+	LGF	R1, V2ADDR	load v2 source
000042BE	E761 0000 0806		00000000	3126+	VL	v22, 0(R1)	use v21 to test decoder
000042C4	E310 5028 0014		00000028	3127+	LGF	R1, V3ADDR	load v3 source
000042CA	E771 0000 0806		00000000	3128+	VL	v23, 0(R1)	use v22 to test decoder
000042D0	E756 7010 1EF8			3129+	VCEQ	V21, V22, V23, 1, 1	test instruction
000042D6	B98D 0020			3130+	EPSW	R2, R0	extract psw
000042DA	5020 500C		0000000C	3131+	ST	R2, CCPSW	to save CC
000042DE	E750 5048 080E		00004298	3132+	VST	V21, V1064	save v1 output
000042E4	07FB			3133+	BR	R11	return
000042E8				3134+RE64	DC	0F	V1 for this test
000042E8				3135+	DROP	R5	
000042E8	FFFFFFFF FFFFFFFF			3136	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000042F0	FFFFFFFF FFFFFFFF						
000042F8	00000000 00000000			3137	DC	XL16' 0000000000000000 0000000000000000'	v2
00004300	00000000 00000000						
00004308	00000000 00000000			3138	DC	XL16' 0000000000000000 0000000000000000'	v3
00004310	00000000 00000000						
				3139			
00004318				3140	VRR_B	VCEQ, 1, 1	
00004318		00004318		3141+	DS	0FD	
00004318	00004380			3142+	USING	*, R5	base for test data and test routine
0000431C	0041			3143+T65	DC	A(X65)	address of test routine
0000431E	00			3144+	DC	H' 65'	test number
0000431F	01			3145+	DC	X' 00'	
00004320	01			3146+	DC	HL1' 1'	m4 used
00004321	01			3147+	DC	HL1' 1'	m5 used
00004322	0B			3148+	DC	HL1' 1'	CC
00004322	0B			3149+	DC	HL1' 11'	CC failed mask
00004324	00000000 00000000			3150+	DS	2F	extracted PSW after test (has CC)
0000432C	FF			3151+	DC	X' FF'	extracted CC, if test failed
0000432D	E5C3C5D8 40404040			3152+	DC	CL8' VCEQ'	instruction name
00004338	000043B0			3153+	DC	A(RE65)	address of v1 result
0000433C	000043C0			3154+	DC	A(RE65+16)	address of v2 source
00004340	000043D0			3155+	DC	A(RE65+32)	address of v3 source
00004344	00000010			3156+	DC	A(16)	result length
00004348	000043B0			3157+REA65	DC	A(RE65)	result address
00004350	00000000 00000000			3158+	DS	2FD	gap
00004358	00000000 00000000						
00004360	00000000 00000000			3159+V1065	DS	XL16	V1 output
00004368	00000000 00000000						
00004370	00000000 00000000			3160+	DS	2FD	gap
00004378	00000000 00000000						
				3161+*			
00004380				3162+X65	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004380	E310 5024 0014		00000024	3163+	LGF	R1, V2ADDR	load v2 source
00004386	E761 0000 0806		00000000	3164+	VL	v22, 0(R1)	use v21 to test decoder
0000438C	E310 5028 0014		00000028	3165+	LGF	R1, V3ADDR	load v3 source
00004392	E771 0000 0806		00000000	3166+	VL	v23, 0(R1)	use v22 to test decoder
00004398	E756 7010 1EF8			3167+	VCEQ	V21, V22, V23, 1, 1	test instruction
0000439E	B98D 0020			3168+	EPSW	R2, R0	extract psw
000043A2	5020 500C		0000000C	3169+	ST	R2, CCPSW	to save CC
000043A6	E750 5048 080E		00004360	3170+	VST	V21, V1065	save v1 output
000043AC	07FB			3171+	BR	R11	return
000043B0				3172+RE65	DC	0F	V1 for this test
000043B0				3173+	DROP	R5	
000043B0	FFFFFFFF FFFFFFFF			3174	DC	XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result t
000043B8	00000000 FFFFFFFF						
000043C0	00000000 00000000			3175	DC	XL16' 0000000000000000 0000000000000000'	v2
000043C8	00000000 00000000						
000043D0	00000000 00000000			3176	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
000043D8	8FFF8FFF 00000000						
000043E0				3177			
000043E0				3178	VRR_B	VCEQ, 1, 3	
000043E0		000043E0		3179+	DS	0FD	
000043E0	00004448			3180+	USING	*, R5	base for test data and test routine
000043E4	0042			3181+T66	DC	A(X66)	address of test routine
000043E6	00			3182+	DC	H' 66'	test number
000043E7	01			3183+	DC	X' 00'	
000043E8	01			3184+	DC	HL1' 1'	m4 used
000043E9	03			3185+	DC	HL1' 1'	m5 used
000043EA	0E			3186+	DC	HL1' 3'	CC
000043EC	00000000 00000000			3187+	DC	HL1' 14'	CC failed mask
000043F4	FF			3188+	DS	2F	extracted PSW after test (has CC)
000043F5	E5C3C5D8 40404040			3189+	DC	X' FF'	extracted CC, if test failed
00004400	00004478			3190+	DC	CL8' VCEQ'	instruction name
00004404	00004488			3191+	DC	A(RE66)	address of v1 result
00004408	00004498			3192+	DC	A(RE66+16)	address of v2 source
0000440C	00000010			3193+	DC	A(RE66+32)	address of v3 source
00004410	00004478			3194+	DC	A(16)	result length
00004418	00000000 00000000			3195+REA66	DC	A(RE66)	result address
00004420	00000000 00000000			3196+	DS	2FD	gap
00004428	00000000 00000000			3197+V1066	DS	XL16	V1 output
00004430	00000000 00000000						
00004438	00000000 00000000			3198+	DS	2FD	gap
00004440	00000000 00000000						
00004448				3199+*			
00004448	E310 5024 0014		00000024	3200+X66	DS	0F	
0000444E	E761 0000 0806		00000000	3201+	LGF	R1, V2ADDR	load v2 source
00004454	E310 5028 0014		00000028	3202+	VL	v22, 0(R1)	use v21 to test decoder
0000445A	E771 0000 0806		00000000	3203+	LGF	R1, V3ADDR	load v3 source
00004460	E756 7010 1EF8			3204+	VL	v23, 0(R1)	use v22 to test decoder
00004466	B98D 0020			3205+	VCEQ	V21, V22, V23, 1, 1	test instruction
0000446A	5020 500C		0000000C	3206+	EPSW	R2, R0	extract psw
0000446E	E750 5048 080E		00004428	3207+	ST	R2, CCPSW	to save CC
00004474	07FB			3208+	VST	V21, V1066	save v1 output
00004478				3209+	BR	R11	return
00004478				3210+RE66	DC	0F	V1 for this test
00004478				3211+	DROP	R5	
00004478	00000000 00000000			3212	DC	XL16' 0000000000000000 0000000000000000'	result t

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004480	00000000 00000000						
00004488	FFFFFFFF FFFFFFFF			3213	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00004490	FFFFFFFF FFFFFFFF						
00004498	00000000 00000000			3214	DC	XL16' 0000000000000000 0000000000000000'	v3
000044A0	00000000 00000000						
				3215			
				3216	*Word		
				3217	VRR_B	VCEQ, 2, 0	
000044A8				3218+	DS	0FD	
000044A8		000044A8		3219+	USING	*, R5	base for test data and test routine
000044A8	00004510			3220+T67	DC	A(X67)	address of test routine
000044AC	0043			3221+	DC	H' 67'	test number
000044AE	00			3222+	DC	X' 00'	
000044AF	02			3223+	DC	HL1' 2'	m4 used
000044B0	01			3224+	DC	HL1' 1'	m5 used
000044B1	00			3225+	DC	HL1' 0'	CC
000044B2	07			3226+	DC	HL1' 7'	CC failed mask
000044B4	00000000 00000000			3227+	DS	2F	extracted PSW after test (has CC)
000044BC	FF			3228+	DC	X' FF'	extracted CC, if test failed
000044BD	E5C3C5D8 40404040			3229+	DC	CL8' VCEQ'	instruction name
000044C8	00004540			3230+	DC	A(RE67)	address of v1 result
000044CC	00004550			3231+	DC	A(RE67+16)	address of v2 source
000044D0	00004560			3232+	DC	A(RE67+32)	address of v3 source
000044D4	00000010			3233+	DC	A(16)	result length
000044D8	00004540			3234+REA67	DC	A(RE67)	result address
000044E0	00000000 00000000			3235+	DS	2FD	gap
000044E8	00000000 00000000						
000044F0	00000000 00000000			3236+V1067	DS	XL16	V1 output
000044F8	00000000 00000000						
00004500	00000000 00000000			3237+	DS	2FD	gap
00004508	00000000 00000000						
				3238+*			
00004510				3239+X67	DS	0F	
00004510	E310 5024 0014		00000024	3240+	LGF	R1, V2ADDR	load v2 source
00004516	E761 0000 0806		00000000	3241+	VL	v22, 0(R1)	use v21 to test decoder
0000451C	E310 5028 0014		00000028	3242+	LGF	R1, V3ADDR	load v3 source
00004522	E771 0000 0806		00000000	3243+	VL	v23, 0(R1)	use v22 to test decoder
00004528	E756 7010 2EF8			3244+	VCEQ	V21, V22, V23, 2, 1	test instruction
0000452E	B98D 0020			3245+	EPSW	R2, R0	extract psw
00004532	5020 500C		0000000C	3246+	ST	R2, CCPSW	to save CC
00004536	E750 5048 080E		000044F0	3247+	VST	V21, V1067	save v1 output
0000453C	07FB			3248+	BR	R11	return
00004540				3249+RE67	DC	0F	V1 for this test
00004540				3250+	DROP	R5	
00004540	FFFFFFFF FFFFFFFF			3251	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00004548	FFFFFFFF FFFFFFFF						
00004550	00000000 00000000			3252	DC	XL16' 0000000000000000 0000000000000000'	v2
00004558	00000000 00000000						
00004560	00000000 00000000			3253	DC	XL16' 0000000000000000 0000000000000000'	v3
00004568	00000000 00000000						
				3254			
				3255	VRR_B	VCEQ, 2, 1	
00004570				3256+	DS	0FD	
00004570		00004570		3257+	USING	*, R5	base for test data and test routine
00004570	000045D8			3258+T68	DC	A(X68)	address of test routine
00004574	0044			3259+	DC	H' 68'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004576	00			3260+	DC	X' 00'	
00004577	02			3261+	DC	HL1' 2'	m4 used
00004578	01			3262+	DC	HL1' 1'	m5 used
00004579	01			3263+	DC	HL1' 1'	CC
0000457A	0B			3264+	DC	HL1' 11'	CC failed mask
0000457C	00000000 00000000			3265+	DS	2F	extracted PSW after test (has CC)
00004584	FF			3266+	DC	X' FF'	extracted CC, if test failed
00004585	E5C3C5D8 40404040			3267+	DC	CL8' VCEQ'	instruction name
00004590	00004608			3268+	DC	A(RE68)	address of v1 result
00004594	00004618			3269+	DC	A(RE68+16)	address of v2 source
00004598	00004628			3270+	DC	A(RE68+32)	address of v3 source
0000459C	00000010			3271+	DC	A(16)	result length
000045A0	00004608			3272+REA68	DC	A(RE68)	result address
000045A8	00000000 00000000			3273+	DS	2FD	gap
000045B0	00000000 00000000						
000045B8	00000000 00000000			3274+V1068	DS	XL16	V1 output
000045C0	00000000 00000000						
000045C8	00000000 00000000			3275+	DS	2FD	gap
000045D0	00000000 00000000						
				3276+*			
000045D8				3277+X68	DS	0F	
000045D8	E310 5024 0014		00000024	3278+	LGF	R1, V2ADDR	load v2 source
000045DE	E761 0000 0806		00000000	3279+	VL	v22, 0(R1)	use v21 to test decoder
000045E4	E310 5028 0014		00000028	3280+	LGF	R1, V3ADDR	load v3 source
000045EA	E771 0000 0806		00000000	3281+	VL	v23, 0(R1)	use v22 to test decoder
000045F0	E756 7010 2EF8			3282+	VCEQ	V21, V22, V23, 2, 1	test instruction
000045F6	B98D 0020			3283+	EPSW	R2, R0	extract psw
000045FA	5020 500C		0000000C	3284+	ST	R2, CCPSW	to save CC
000045FE	E750 5048 080E		000045B8	3285+	VST	V21, V1068	save v1 output
00004604	07FB			3286+	BR	R11	return
00004608				3287+RE68	DC	0F	V1 for this test
00004608				3288+	DROP	R5	
00004608	FFFFFFFF FFFFFFFF			3289	DC	XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result t
00004610	00000000 FFFFFFFF						
00004618	00000000 00000000			3290	DC	XL16' 0000000000000000 0000000000000000'	v2
00004620	00000000 00000000						
00004628	00000000 00000000			3291	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00004630	8FFF8FFF 00000000						
				3292			
				3293	VRR_B	VCEQ, 2, 3	
00004638				3294+	DS	0FD	
00004638		00004638		3295+	USING	*, R5	base for test data and test routine
00004638	000046A0			3296+T69	DC	A(X69)	address of test routine
0000463C	0045			3297+	DC	H' 69'	test number
0000463E	00			3298+	DC	X' 00'	
0000463F	02			3299+	DC	HL1' 2'	m4 used
00004640	01			3300+	DC	HL1' 1'	m5 used
00004641	03			3301+	DC	HL1' 3'	CC
00004642	0E			3302+	DC	HL1' 14'	CC failed mask
00004644	00000000 00000000			3303+	DS	2F	extracted PSW after test (has CC)
0000464C	FF			3304+	DC	X' FF'	extracted CC, if test failed
0000464D	E5C3C5D8 40404040			3305+	DC	CL8' VCEQ'	instruction name
00004658	000046D0			3306+	DC	A(RE69)	address of v1 result
0000465C	000046E0			3307+	DC	A(RE69+16)	address of v2 source
00004660	000046F0			3308+	DC	A(RE69+32)	address of v3 source
00004664	00000010			3309+	DC	A(16)	result length



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004668	000046D0			3310+REA69	DC	A(RE69)	result address
00004670	00000000 00000000			3311+	DS	2FD	gap
00004678	00000000 00000000						
00004680	00000000 00000000			3312+V1069	DS	XL16	V1 output
00004688	00000000 00000000						
00004690	00000000 00000000			3313+	DS	2FD	gap
00004698	00000000 00000000						
				3314+*			
000046A0				3315+X69	DS	0F	
000046A0	E310 5024 0014		00000024	3316+	LGF	R1, V2ADDR	load v2 source
000046A6	E761 0000 0806		00000000	3317+	VL	v22, 0(R1)	use v21 to test decoder
000046AC	E310 5028 0014		00000028	3318+	LGF	R1, V3ADDR	load v3 source
000046B2	E771 0000 0806		00000000	3319+	VL	v23, 0(R1)	use v22 to test decoder
000046B8	E756 7010 2EF8			3320+	VCEQ	V21, V22, V23, 2, 1	test instruction
000046BE	B98D 0020			3321+	EPSW	R2, R0	extract psw
000046C2	5020 500C		0000000C	3322+	ST	R2, CCPSW	to save CC
000046C6	E750 5048 080E		00004680	3323+	VST	V21, V1069	save v1 output
000046CC	07FB			3324+	BR	R11	return
000046D0				3325+RE69	DC	0F	V1 for this test
000046D0				3326+	DROP	R5	
000046D0	00000000 00000000			3327	DC	XL16' 0000000000000000 0000000000000000'	result
000046D8	00000000 00000000						
000046E0	FFFFFFFF FFFFFFFF			3328	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
000046E8	FFFFFFFF FFFFFFFF						
000046F0	00000000 00000000			3329	DC	XL16' 0000000000000000 0000000000000000'	v3
000046F8	00000000 00000000						
				3330			
				3331 *Doubleword			
				3332	VRR_B	VCEQ, 3, 0	
00004700				3333+	DS	0FD	
00004700		00004700		3334+	USING	*, R5	base for test data and test routine
00004700	00004768			3335+T70	DC	A(X70)	address of test routine
00004704	0046			3336+	DC	H' 70'	test number
00004706	00			3337+	DC	X' 00'	
00004707	03			3338+	DC	HL1' 3'	m4 used
00004708	01			3339+	DC	HL1' 1'	m5 used
00004709	00			3340+	DC	HL1' 0'	CC
0000470A	07			3341+	DC	HL1' 7'	CC failed mask
0000470C	00000000 00000000			3342+	DS	2F	extracted PSW after test (has CC)
00004714	FF			3343+	DC	X' FF'	extracted CC, if test failed
00004715	E5C3C5D8 40404040			3344+	DC	CL8' VCEQ'	instruction name
00004720	00004798			3345+	DC	A(RE70)	address of v1 result
00004724	000047A8			3346+	DC	A(RE70+16)	address of v2 source
00004728	000047B8			3347+	DC	A(RE70+32)	address of v3 source
0000472C	00000010			3348+	DC	A(16)	result length
00004730	00004798			3349+REA70	DC	A(RE70)	result address
00004738	00000000 00000000			3350+	DS	2FD	gap
00004740	00000000 00000000						
00004748	00000000 00000000			3351+V1070	DS	XL16	V1 output
00004750	00000000 00000000						
00004758	00000000 00000000			3352+	DS	2FD	gap
00004760	00000000 00000000						
				3353+*			
00004768				3354+X70	DS	0F	
00004768	E310 5024 0014		00000024	3355+	LGF	R1, V2ADDR	load v2 source
0000476E	E761 0000 0806		00000000	3356+	VL	v22, 0(R1)	use v21 to test decoder



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004774	E310 5028 0014		00000028	3357+	LGF	R1, V3ADDR	load v3 source
0000477A	E771 0000 0806		00000000	3358+	VL	v23, 0(R1)	use v22 to test decoder
00004780	E756 7010 3EF8			3359+	VCEQ	V21, V22, V23, 3, 1	test instruction
00004786	B98D 0020			3360+	EPSW	R2, R0	extract psw
0000478A	5020 500C		0000000C	3361+	ST	R2, CCPSW	to save CC
0000478E	E750 5048 080E		00004748	3362+	VST	V21, V1070	save v1 output
00004794	07FB			3363+	BR	R11	return
00004798				3364+RE70	DC	0F	V1 for this test
00004798				3365+	DROP	R5	
00004798	FFFFFFFF FFFFFFFF			3366	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000047A0	FFFFFFFF FFFFFFFF						
000047A8	00000000 00000000			3367	DC	XL16' 0000000000000000 0000000000000000'	v2
000047B0	00000000 00000000						
000047B8	00000000 00000000			3368	DC	XL16' 0000000000000000 0000000000000000'	v3
000047C0	00000000 00000000						
				3369			
				3370	VRR_B	VCEQ, 3, 1	
000047C8				3371+	DS	0FD	
000047C8		000047C8		3372+	USING	*, R5	base for test data and test routine
000047C8	00004830			3373+T71	DC	A(X71)	address of test routine
000047CC	0047			3374+	DC	H' 71'	test number
000047CE	00			3375+	DC	X' 00'	
000047CF	03			3376+	DC	HL1' 3'	m4 used
000047D0	01			3377+	DC	HL1' 1'	m5 used
000047D1	01			3378+	DC	HL1' 1'	CC
000047D2	0B			3379+	DC	HL1' 11'	CC failed mask
000047D4	00000000 00000000			3380+	DS	2F	extracted PSW after test (has CC)
000047DC	FF			3381+	DC	X' FF'	extracted CC, if test failed
000047DD	E5C3C5D8 40404040			3382+	DC	CL8' VCEQ'	instruction name
000047E8	00004860			3383+	DC	A(RE71)	address of v1 result
000047EC	00004870			3384+	DC	A(RE71+16)	address of v2 source
000047F0	00004880			3385+	DC	A(RE71+32)	address of v3 source
000047F4	00000010			3386+	DC	A(16)	result length
000047F8	00004860			3387+REA71	DC	A(RE71)	result address
00004800	00000000 00000000			3388+	DS	2FD	gap
00004808	00000000 00000000						
00004810	00000000 00000000			3389+V1071	DS	XL16	V1 output
00004818	00000000 00000000						
00004820	00000000 00000000			3390+	DS	2FD	gap
00004828	00000000 00000000						
				3391+*			
00004830				3392+X71	DS	0F	
00004830	E310 5024 0014		00000024	3393+	LGF	R1, V2ADDR	load v2 source
00004836	E761 0000 0806		00000000	3394+	VL	v22, 0(R1)	use v21 to test decoder
0000483C	E310 5028 0014		00000028	3395+	LGF	R1, V3ADDR	load v3 source
00004842	E771 0000 0806		00000000	3396+	VL	v23, 0(R1)	use v22 to test decoder
00004848	E756 7010 3EF8			3397+	VCEQ	V21, V22, V23, 3, 1	test instruction
0000484E	B98D 0020			3398+	EPSW	R2, R0	extract psw
00004852	5020 500C		0000000C	3399+	ST	R2, CCPSW	to save CC
00004856	E750 5048 080E		00004810	3400+	VST	V21, V1071	save v1 output
0000485C	07FB			3401+	BR	R11	return
00004860				3402+RE71	DC	0F	V1 for this test
00004860				3403+	DROP	R5	
00004860	FFFFFFFF FFFFFFFF			3404	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result t
00004868	00000000 00000000						
00004870	00000000 00000000			3405	DC	XL16' 0000000000000000 0000000000000000'	v2

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004878	00000000	00000000					
00004880	00000000	00000000		3406	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00004888	8FFF8FFF	00000000					
				3407			
				3408	VRR_B	VCEQ, 3, 3	
00004890				3409+	DS	0FD	
00004890		00004890		3410+	USING	*, R5	base for test data and test routine
00004890	000048F8			3411+T72	DC	A(X72)	address of test routine
00004894	0048			3412+	DC	H' 72'	test number
00004896	00			3413+	DC	X' 00'	
00004897	03			3414+	DC	HL1' 3'	m4 used
00004898	01			3415+	DC	HL1' 1'	m5 used
00004899	03			3416+	DC	HL1' 3'	CC
0000489A	0E			3417+	DC	HL1' 14'	CC failed mask
0000489C	00000000	00000000		3418+	DS	2F	extracted PSW after test (has CC)
000048A4	FF			3419+	DC	X' FF'	extracted CC, if test failed
000048A5	E5C3C5D8	40404040		3420+	DC	CL8' VCEQ'	instruction name
000048B0	00004928			3421+	DC	A(RE72)	address of v1 result
000048B4	00004938			3422+	DC	A(RE72+16)	address of v2 source
000048B8	00004948			3423+	DC	A(RE72+32)	address of v3 source
000048BC	00000010			3424+	DC	A(16)	result length
000048C0	00004928			3425+REA72	DC	A(RE72)	result address
000048C8	00000000	00000000		3426+	DS	2FD	gap
000048D0	00000000	00000000					
000048D8	00000000	00000000		3427+V1072	DS	XL16	V1 output
000048E0	00000000	00000000					
000048E8	00000000	00000000		3428+	DS	2FD	gap
000048F0	00000000	00000000					
				3429+*			
000048F8				3430+X72	DS	0F	
000048F8	E310 5024 0014		00000024	3431+	LGF	R1, V2ADDR	load v2 source
000048FE	E761 0000 0806		00000000	3432+	VL	v22, 0(R1)	use v21 to test decoder
00004904	E310 5028 0014		00000028	3433+	LGF	R1, V3ADDR	load v3 source
0000490A	E771 0000 0806		00000000	3434+	VL	v23, 0(R1)	use v22 to test decoder
00004910	E756 7010 3EF8			3435+	VCEQ	V21, V22, V23, 3, 1	test instruction
00004916	B98D 0020			3436+	EPSW	R2, R0	extract psw
0000491A	5020 500C		0000000C	3437+	ST	R2, CCPSW	to save CC
0000491E	E750 5048 080E		000048D8	3438+	VST	V21, V1072	save v1 output
00004924	07FB			3439+	BR	R11	return
00004928				3440+RE72	DC	0F	V1 for this test
00004928				3441+	DROP	R5	
00004928	00000000	00000000		3442	DC	XL16' 0000000000000000 0000000000000000'	result t
00004930	00000000	00000000					
00004938	FFFFFFFF	FFFFFFFF		3443	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00004940	FFFFFFFF	FFFFFFFF					
00004948	00000000	00000000		3444	DC	XL16' 0000000000000000 0000000000000000'	v3
00004950	00000000	00000000					
				3445			
				3446	*-----		
				3447	* case -	general	
				3448	*-----		
				3449	*Byte		
				3450	VRR_B	VCEQ, 0, 0	
00004958				3451+	DS	0FD	
00004958		00004958		3452+	USING	*, R5	base for test data and test routine
00004958	000049C0			3453+T73	DC	A(X73)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000495C	0049			3454+	DC	H' 73'	test number
0000495E	00			3455+	DC	X' 00'	
0000495F	00			3456+	DC	HL1' 0'	m4 used
00004960	01			3457+	DC	HL1' 1'	m5 used
00004961	00			3458+	DC	HL1' 0'	CC
00004962	07			3459+	DC	HL1' 7'	CC failed mask
00004964	00000000	00000000		3460+	DS	2F	extracted PSW after test (has CC)
0000496C	FF			3461+	DC	X' FF'	extracted CC, if test failed
0000496D	E5C3C5D8	40404040		3462+	DC	CL8' VCEQ'	instruction name
00004978	000049F0			3463+	DC	A(RE73)	address of v1 result
0000497C	00004A00			3464+	DC	A(RE73+16)	address of v2 source
00004980	00004A10			3465+	DC	A(RE73+32)	address of v3 source
00004984	00000010			3466+	DC	A(16)	result length
00004988	000049F0			3467+REA73	DC	A(RE73)	result address
00004990	00000000	00000000		3468+	DS	2FD	gap
00004998	00000000	00000000					
000049A0	00000000	00000000		3469+V1073	DS	XL16	V1 output
000049A8	00000000	00000000					
000049B0	00000000	00000000		3470+	DS	2FD	gap
000049B8	00000000	00000000					
000049C0				3471+*			
000049C0	E310 5024 0014		00000024	3472+X73	DS	0F	
000049C6	E761 0000 0806		00000000	3473+	LGF	R1, V2ADDR	load v2 source
000049CC	E310 5028 0014		00000028	3474+	VL	v22, 0(R1)	use v21 to test decoder
000049D2	E771 0000 0806		00000000	3475+	LGF	R1, V3ADDR	load v3 source
000049D8	E756 7010 0EF8		00000000	3476+	VL	v23, 0(R1)	use v22 to test decoder
000049DE	B98D 0020			3477+	VCEQ	V21, V22, V23, 0, 1	test instruction
000049E2	5020 500C		0000000C	3478+	EPSW	R2, R0	extract psw
000049E6	E750 5048 080E		000049A0	3479+	ST	R2, CCPSW	to save CC
000049EC	07FB			3480+	VST	V21, V1073	save v1 output
000049F0				3481+	BR	R11	return
000049F0				3482+RE73	DC	0F	V1 for this test
000049F0	FFFFFFFF FFFFFFFF			3483+	DROP	R5	
000049F0	FFFFFFFF FFFFFFFF			3484	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000049F8	FFFFFFFF FFFFFFFF						
00004A00	00110033 00550077			3485	DC	XL16' 0011003300550077 0022004400660008'	v2
00004A08	00220044 00660008						
00004A10	00110033 00550077			3486	DC	XL16' 0011003300550077 0022004400660008'	v3
00004A18	00220044 00660008						
00004A20				3487			
00004A20				3488	VRR_B	VCEQ, 0, 0	
00004A20		00004A20		3489+	DS	0FD	
00004A20	00004A88			3490+	USING	*, R5	base for test data and test routine
00004A24	004A			3491+T74	DC	A(X74)	address of test routine
00004A26	00			3492+	DC	H' 74'	test number
00004A27	00			3493+	DC	X' 00'	
00004A28	01			3494+	DC	HL1' 0'	m4 used
00004A29	00			3495+	DC	HL1' 1'	m5 used
00004A2A	07			3496+	DC	HL1' 0'	CC
00004A2C	00000000	00000000		3497+	DC	HL1' 7'	CC failed mask
00004A34	FF			3498+	DS	2F	extracted PSW after test (has CC)
00004A35	E5C3C5D8	40404040		3499+	DC	X' FF'	extracted CC, if test failed
00004A40	00004AB8			3500+	DC	CL8' VCEQ'	instruction name
00004A44	00004AC8			3501+	DC	A(RE74)	address of v1 result
00004A48	00004AD8			3502+	DC	A(RE74+16)	address of v2 source
				3503+	DC	A(RE74+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004A4C	00000010			3504+	DC	A(16)	result length
00004A50	00004AB8			3505+REA74	DC	A(RE74)	result address
00004A58	00000000 00000000			3506+	DS	2FD	gap
00004A60	00000000 00000000						
00004A68	00000000 00000000			3507+V1074	DS	XL16	V1 output
00004A70	00000000 00000000						
00004A78	00000000 00000000			3508+	DS	2FD	gap
00004A80	00000000 00000000						
				3509+*			
00004A88				3510+X74	DS	0F	
00004A88	E310 5024 0014		00000024	3511+	LGF	R1, V2ADDR	load v2 source
00004A8E	E761 0000 0806		00000000	3512+	VL	v22, 0(R1)	use v21 to test decoder
00004A94	E310 5028 0014		00000028	3513+	LGF	R1, V3ADDR	load v3 source
00004A9A	E771 0000 0806		00000000	3514+	VL	v23, 0(R1)	use v22 to test decoder
00004AA0	E756 7010 0EF8			3515+	VCEQ	V21, V22, V23, 0, 1	test instruction
00004AA6	B98D 0020			3516+	EPSW	R2, R0	extract psw
00004AAA	5020 500C		0000000C	3517+	ST	R2, CCPSW	to save CC
00004AAE	E750 5048 080E		00004A68	3518+	VST	V21, V1074	save v1 output
00004AB4	07FB			3519+	BR	R11	return
00004AB8				3520+RE74	DC	0F	V1 for this test
00004AB8				3521+	DROP	R5	
00004AB8	FFFFFFFF FFFFFFFF			3522	DC	XL16' FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF'	result
00004AC0	FFFFFFFF FFFFFFFF						
00004AC8	FFFEFFFD FFFCFFFB			3523	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00004AD0	FFFAFFF9 FFF8FFF7						
00004AD8	FFFEFFFD FFFCFFFB			3524	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00004AE0	FFFAFFF9 FFF8FFF7						
				3525			
				3526	VRR_B	VCEQ, 0, 1	
00004AE8				3527+	DS	0FD	
00004AE8		00004AE8		3528+	USING	*, R5	base for test data and test routine
00004AE8	00004B50			3529+T75	DC	A(X75)	address of test routine
00004AEC	004B			3530+	DC	H' 75'	test number
00004AEE	00			3531+	DC	X' 00'	
00004AEF	00			3532+	DC	HL1' 0'	m4 used
00004AF0	01			3533+	DC	HL1' 1'	m5 used
00004AF1	01			3534+	DC	HL1' 1'	CC
00004AF2	0B			3535+	DC	HL1' 11'	CC failed mask
00004AF4	00000000 00000000			3536+	DS	2F	extracted PSW after test (has CC)
00004AFC	FF			3537+	DC	X' FF'	extracted CC, if test failed
00004AFD	E5C3C5D8 40404040			3538+	DC	CL8' VCEQ'	instruction name
00004B08	00004B80			3539+	DC	A(RE75)	address of v1 result
00004B0C	00004B90			3540+	DC	A(RE75+16)	address of v2 source
00004B10	00004BA0			3541+	DC	A(RE75+32)	address of v3 source
00004B14	00000010			3542+	DC	A(16)	result length
00004B18	00004B80			3543+REA75	DC	A(RE75)	result address
00004B20	00000000 00000000			3544+	DS	2FD	gap
00004B28	00000000 00000000						
00004B30	00000000 00000000			3545+V1075	DS	XL16	V1 output
00004B38	00000000 00000000						
00004B40	00000000 00000000			3546+	DS	2FD	gap
00004B48	00000000 00000000						
				3547+*			
00004B50				3548+X75	DS	0F	
00004B50	E310 5024 0014		00000024	3549+	LGF	R1, V2ADDR	load v2 source
00004B56	E761 0000 0806		00000000	3550+	VL	v22, 0(R1)	use v21 to test decoder



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004B5C	E310 5028 0014		00000028	3551+	LGF	R1, V3ADDR	load v3 source
00004B62	E771 0000 0806		00000000	3552+	VL	v23, 0(R1)	use v22 to test decoder
00004B68	E756 7010 0EF8			3553+	VCEQ	V21, V22, V23, 0, 1	test instruction
00004B6E	B98D 0020			3554+	EPSW	R2, R0	extract psw
00004B72	5020 500C		0000000C	3555+	ST	R2, CCPSW	to save CC
00004B76	E750 5048 080E		00004B30	3556+	VST	V21, V1075	save v1 output
00004B7C	07FB			3557+	BR	R11	return
00004B80				3558+RE75	DC	0F	V1 for this test
00004B80				3559+	DROP	R5	
00004B80	FF000000 00000000			3560	DC	XL16' FF00000000000000 FFFFFFFF'	result t
00004B88	FFFFFFFF FFFFFFFF						
00004B90	00010203 04050607			3561	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v2
00004B98	08090A0B 0C0DFE0F						
00004BA0	00110033 00550077			3562	DC	XL16' 0011003300550077 08090A0B0C0DFE0F'	v3
00004BA8	08090A0B 0C0DFE0F						
				3563			
00004BB0				3564	VRR_B	VCEQ, 0, 1	
00004BB0		00004BB0		3565+	DS	0FD	
00004BB0	00004C18			3566+	USING	*, R5	base for test data and test routine
00004BB4	004C			3567+T76	DC	A(X76)	address of test routine
00004BB6	00			3568+	DC	H' 76'	test number
00004BB7	00			3569+	DC	X' 00'	
00004BB8	01			3570+	DC	HL1' 0'	m4 used
00004BB8	01			3571+	DC	HL1' 1'	m5 used
00004BB9	01			3572+	DC	HL1' 1'	CC
00004BBA	0B			3573+	DC	HL1' 11'	CC failed mask
00004BBC	00000000 00000000			3574+	DS	2F	extracted PSW after test (has CC)
00004BC4	FF			3575+	DC	X' FF'	extracted CC, if test failed
00004BC5	E5C3C5D8 40404040			3576+	DC	CL8' VCEQ'	instruction name
00004BD0	00004C48			3577+	DC	A(RE76)	address of v1 result
00004BD4	00004C58			3578+	DC	A(RE76+16)	address of v2 source
00004BD8	00004C68			3579+	DC	A(RE76+32)	address of v3 source
00004BDC	00000010			3580+	DC	A(16)	result length
00004BE0	00004C48			3581+REA76	DC	A(RE76)	result address
00004BE8	00000000 00000000			3582+	DS	2FD	gap
00004BF0	00000000 00000000						
00004BF8	00000000 00000000			3583+V1076	DS	XL16	V1 output
00004C00	00000000 00000000						
00004C08	00000000 00000000			3584+	DS	2FD	gap
00004C10	00000000 00000000						
				3585+*			
00004C18				3586+X76	DS	0F	
00004C18	E310 5024 0014		00000024	3587+	LGF	R1, V2ADDR	load v2 source
00004C1E	E761 0000 0806		00000000	3588+	VL	v22, 0(R1)	use v21 to test decoder
00004C24	E310 5028 0014		00000028	3589+	LGF	R1, V3ADDR	load v3 source
00004C2A	E771 0000 0806		00000000	3590+	VL	v23, 0(R1)	use v22 to test decoder
00004C30	E756 7010 0EF8			3591+	VCEQ	V21, V22, V23, 0, 1	test instruction
00004C36	B98D 0020			3592+	EPSW	R2, R0	extract psw
00004C3A	5020 500C		0000000C	3593+	ST	R2, CCPSW	to save CC
00004C3E	E750 5048 080E		00004BF8	3594+	VST	V21, V1076	save v1 output
00004C44	07FB			3595+	BR	R11	return
00004C48				3596+RE76	DC	0F	V1 for this test
00004C48				3597+	DROP	R5	
00004C48	FFFFFFFF FFFFFFFF			3598	DC	XL16' FFFFFFFF'	result t
00004C50	FF000000 00000000						
00004C58	08090A0B 0C0DFE0F			3599	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v2

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00004C60	00010203 04050607							
00004C68	08090A0B 0C0DFE0F			3600	DC	XL16' 08090A0B0C0DFE0F	0011003300550077'	v3
00004C70	00110033 00550077							
				3601				
				3602	VRR_B	VCEQ, 0, 3		
00004C78				3603+	DS	0FD		
00004C78		00004C78		3604+	USING	*, R5		base for test data and test routine
00004C78	00004CE0			3605+T77	DC	A(X77)		address of test routine
00004C7C	004D			3606+	DC	H' 77'		test number
00004C7E	00			3607+	DC	X' 00'		
00004C7F	00			3608+	DC	HL1' 0'		m4 used
00004C80	01			3609+	DC	HL1' 1'		m5 used
00004C81	03			3610+	DC	HL1' 3'		CC
00004C82	0E			3611+	DC	HL1' 14'		CC failed mask
00004C84	00000000 00000000			3612+	DS	2F		extracted PSW after test (has CC)
00004C8C	FF			3613+	DC	X' FF'		extracted CC, if test failed
00004C8D	E5C3C5D8 40404040			3614+	DC	CL8' VCEQ'		instruction name
00004C98	00004D10			3615+	DC	A(RE77)		address of v1 result
00004C9C	00004D20			3616+	DC	A(RE77+16)		address of v2 source
00004CA0	00004D30			3617+	DC	A(RE77+32)		address of v3 source
00004CA4	00000010			3618+	DC	A(16)		result length
00004CA8	00004D10			3619+REA77	DC	A(RE77)		result address
00004CB0	00000000 00000000			3620+	DS	2FD		gap
00004CB8	00000000 00000000							
00004CC0	00000000 00000000			3621+V1077	DS	XL16		V1 output
00004CC8	00000000 00000000							
00004CD0	00000000 00000000			3622+	DS	2FD		gap
00004CD8	00000000 00000000							
				3623+*				
00004CE0				3624+X77	DS	0F		
00004CE0	E310 5024 0014		00000024	3625+	LGF	R1, V2ADDR		load v2 source
00004CE6	E761 0000 0806		00000000	3626+	VL	v22, 0(R1)		use v21 to test decoder
00004CEC	E310 5028 0014		00000028	3627+	LGF	R1, V3ADDR		load v3 source
00004CF2	E771 0000 0806		00000000	3628+	VL	v23, 0(R1)		use v22 to test decoder
00004CF8	E756 7010 0EF8			3629+	VCEQ	V21, V22, V23, 0, 1		test instruction
00004CFE	B98D 0020			3630+	EPSW	R2, R0		extract psw
00004D02	5020 500C		0000000C	3631+	ST	R2, CCPSW		to save CC
00004D06	E750 5048 080E		00004CC0	3632+	VST	V21, V1077		save v1 output
00004D0C	07FB			3633+	BR	R11		return
00004D10				3634+RE77	DC	0F		V1 for this test
00004D10				3635+	DROP	R5		
00004D10	00000000 00000000			3636	DC	XL16' 0000000000000000 0000000000000000'		result t
00004D18	00000000 00000000							
00004D20	01110133 01550177			3637	DC	XL16' 0111013301550177 019901BB01DD01FF'		v2
00004D28	019901BB 01DD01FF							
00004D30	00010203 04050607			3638	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'		v3
00004D38	08090A0B 0C0D0E0F							
				3639				
				3640	VRR_B	VCEQ, 0, 3		
00004D40				3641+	DS	0FD		
00004D40		00004D40		3642+	USING	*, R5		base for test data and test routine
00004D40	00004DA8			3643+T78	DC	A(X78)		address of test routine
00004D44	004E			3644+	DC	H' 78'		test number
00004D46	00			3645+	DC	X' 00'		
00004D47	00			3646+	DC	HL1' 0'		m4 used
00004D48	01			3647+	DC	HL1' 1'		m5 used

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004D49	03			3648+	DC	HL1' 3'	CC
00004D4A	0E			3649+	DC	HL1' 14'	CC failed mask
00004D4C	00000000 00000000			3650+	DS	2F	extracted PSW after test (has CC)
00004D54	FF			3651+	DC	X' FF'	extracted CC, if test failed
00004D55	E5C3C5D8 40404040			3652+	DC	CL8' VCEQ'	instruction name
00004D60	00004DD8			3653+	DC	A(RE78)	address of v1 result
00004D64	00004DE8			3654+	DC	A(RE78+16)	address of v2 source
00004D68	00004DF8			3655+	DC	A(RE78+32)	address of v3 source
00004D6C	00000010			3656+	DC	A(16)	result length
00004D70	00004DD8			3657+REA78	DC	A(RE78)	result address
00004D78	00000000 00000000			3658+	DS	2FD	gap
00004D80	00000000 00000000						
00004D88	00000000 00000000			3659+V1078	DS	XL16	V1 output
00004D90	00000000 00000000						
00004D98	00000000 00000000			3660+	DS	2FD	gap
00004DA0	00000000 00000000						
				3661+*			
00004DA8				3662+X78	DS	0F	
00004DA8	E310 5024 0014		00000024	3663+	LGF	R1, V2ADDR	load v2 source
00004DAE	E761 0000 0806		00000000	3664+	VL	v22, 0(R1)	use v21 to test decoder
00004DB4	E310 5028 0014		00000028	3665+	LGF	R1, V3ADDR	load v3 source
00004DBA	E771 0000 0806		00000000	3666+	VL	v23, 0(R1)	use v22 to test decoder
00004DC0	E756 7010 0EF8			3667+	VCEQ	V21, V22, V23, 0, 1	test instruction
00004DC6	B98D 0020			3668+	EPSW	R2, R0	extract psw
00004DCA	5020 500C		0000000C	3669+	ST	R2, CCPSW	to save CC
00004DCE	E750 5048 080E		00004D88	3670+	VST	V21, V1078	save v1 output
00004DD4	07FB			3671+	BR	R11	return
00004DD8				3672+RE78	DC	0F	V1 for this test
00004DD8				3673+	DROP	R5	
00004DD8	00000000 00000000			3674	DC	XL16' 0000000000000000 0000000000000000'	result t
00004DE0	00000000 00000000						
00004DE8	00010203 04050607			3675	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00004DF0	08090A0B 0C0D0E0F						
00004DF8	01110133 01550177			3676	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00004E00	019901BB 01DD01FF						
				3677			
				3678 *Hal fword			
				3679	VRR_B	VCEQ, 1, 0	
00004E08				3680+	DS	0FD	
00004E08		00004E08		3681+	USING	*, R5	base for test data and test routine
00004E08	00004E70			3682+T79	DC	A(X79)	address of test routine
00004E0C	004F			3683+	DC	H' 79'	test number
00004E0E	00			3684+	DC	X' 00'	
00004E0F	01			3685+	DC	HL1' 1'	m4 used
00004E10	01			3686+	DC	HL1' 1'	m5 used
00004E11	00			3687+	DC	HL1' 0'	CC
00004E12	07			3688+	DC	HL1' 7'	CC failed mask
00004E14	00000000 00000000			3689+	DS	2F	extracted PSW after test (has CC)
00004E1C	FF			3690+	DC	X' FF'	extracted CC, if test failed
00004E1D	E5C3C5D8 40404040			3691+	DC	CL8' VCEQ'	instruction name
00004E28	00004EA0			3692+	DC	A(RE79)	address of v1 result
00004E2C	00004EB0			3693+	DC	A(RE79+16)	address of v2 source
00004E30	00004EC0			3694+	DC	A(RE79+32)	address of v3 source
00004E34	00000010			3695+	DC	A(16)	result length
00004E38	00004EA0			3696+REA79	DC	A(RE79)	result address
00004E40	00000000 00000000			3697+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004E48	00000000 00000000						
00004E50	00000000 00000000			3698+V1079	DS	XL16	V1 output
00004E58	00000000 00000000						
00004E60	00000000 00000000			3699+	DS	2FD	gap
00004E68	00000000 00000000						
00004E70				3700+*			
00004E70	E310 5024 0014		00000024	3701+X79	DS	0F	
00004E76	E761 0000 0806		00000000	3702+	LGF	R1, V2ADDR	load v2 source
00004E7C	E310 5028 0014		00000028	3703+	VL	v22, 0(R1)	use v21 to test decoder
00004E82	E771 0000 0806		00000000	3704+	LGF	R1, V3ADDR	load v3 source
00004E88	E756 7010 1EF8			3705+	VL	v23, 0(R1)	use v22 to test decoder
00004E8E	B98D 0020			3706+	VCEQ	V21, V22, V23, 1, 1	test instruction
00004E92	5020 500C		0000000C	3707+	EPSW	R2, R0	extract psw
00004E96	E750 5048 080E		00004E50	3708+	ST	R2, CCPSW	to save CC
00004E9C	07FB			3709+	VST	V21, V1079	save v1 output
00004EA0				3710+	BR	R11	return
00004EA0				3711+RE79	DC	0F	V1 for this test
00004EA0	FFFFFFFF FFFFFFFF			3712+	DROP	R5	
00004EA8	FFFFFFFF FFFFFFFF			3713	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00004EB0	00110033 00550077			3714	DC	XL16' 0011003300550077 0022004400660008'	v2
00004EB8	00220044 00660008						
00004EC0	00110033 00550077			3715	DC	XL16' 0011003300550077 0022004400660008'	v3
00004EC8	00220044 00660008						
00004ED0				3716			
00004ED0		00004ED0		3717	VRR_B	VCEQ, 1, 0	
00004ED0	00004F38			3718+	DS	0FD	
00004ED4	0050			3719+	USING	*, R5	base for test data and test routine
00004ED6	00			3720+T80	DC	A(X80)	address of test routine
00004ED7	01			3721+	DC	H' 80'	test number
00004ED8	01			3722+	DC	X' 00'	
00004ED9	00			3723+	DC	HL1' 1'	m4 used
00004EDA	07			3724+	DC	HL1' 1'	m5 used
00004EDC	00000000 00000000			3725+	DC	HL1' 0'	CC
00004EE4	FF			3726+	DC	HL1' 7'	CC failed mask
00004EE5	E5C3C5D8 40404040			3727+	DS	2F	extracted PSW after test (has CC)
00004EF0	00004F68			3728+	DC	X' FF'	extracted CC, if test failed
00004EF4	00004F78			3729+	DC	CL8' VCEQ'	instruction name
00004EF8	00004F88			3730+	DC	A(RE80)	address of v1 result
00004EFC	00000010			3731+	DC	A(RE80+16)	address of v2 source
00004F00	00004F68			3732+	DC	A(RE80+32)	address of v3 source
00004F08	00000000 00000000			3733+	DC	A(16)	result length
00004F10	00000000 00000000			3734+REA80	DC	A(RE80)	result address
00004F18	00000000 00000000			3735+	DS	2FD	gap
00004F20	00000000 00000000						
00004F28	00000000 00000000			3736+V1080	DS	XL16	V1 output
00004F30	00000000 00000000						
00004F38				3737+	DS	2FD	gap
00004F38				3738+*			
00004F38	E310 5024 0014		00000024	3739+X80	DS	0F	
00004F3E	E761 0000 0806		00000000	3740+	LGF	R1, V2ADDR	load v2 source
00004F44	E310 5028 0014		00000028	3741+	VL	v22, 0(R1)	use v21 to test decoder
00004F4A	E771 0000 0806		00000000	3742+	LGF	R1, V3ADDR	load v3 source
00004F50	E756 7010 1EF8			3743+	VL	v23, 0(R1)	use v22 to test decoder
				3744+	VCEQ	V21, V22, V23, 1, 1	test instruction



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004F56	B98D 0020			3745+	EPSW	R2, R0	extract psw
00004F5A	5020 500C		0000000C	3746+	ST	R2, CCPSW	to save CC
00004F5E	E750 5048 080E		00004F18	3747+	VST	V21, V1080	save v1 output
00004F64	07FB			3748+	BR	R11	return
00004F68				3749+RE80	DC	0F	V1 for this test
00004F68				3750+	DROP	R5	
00004F68	FFFFFFFF FFFFFFFF			3751	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00004F70	FFFFFFFF FFFFFFFF						
00004F78	FFFEFFFD FFFCFFFB			3752	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00004F80	FFFAFFF9 FFF8FFF7						
00004F88	FFFEFFFD FFFCFFFB			3753	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00004F90	FFFAFFF9 FFF8FFF7						
				3754			
				3755	VRR_B	VCEQ, 1, 1	
00004F98				3756+	DS	0FD	
00004F98		00004F98		3757+	USING	*, R5	base for test data and test routine
00004F98	00005000			3758+T81	DC	A(X81)	address of test routine
00004F9C	0051			3759+	DC	H' 81'	test number
00004F9E	00			3760+	DC	X' 00'	
00004F9F	01			3761+	DC	HL1' 1'	m4 used
00004FA0	01			3762+	DC	HL1' 1'	m5 used
00004FA1	01			3763+	DC	HL1' 1'	CC
00004FA2	0B			3764+	DC	HL1' 11'	CC failed mask
00004FA4	00000000 00000000			3765+	DS	2F	extracted PSW after test (has CC)
00004FAC	FF			3766+	DC	X' FF'	extracted CC, if test failed
00004FAD	E5C3C5D8 40404040			3767+	DC	CL8' VCEQ'	instruction name
00004FB8	00005030			3768+	DC	A(RE81)	address of v1 result
00004FBC	00005040			3769+	DC	A(RE81+16)	address of v2 source
00004FC0	00005050			3770+	DC	A(RE81+32)	address of v3 source
00004FC4	00000010			3771+	DC	A(16)	result length
00004FC8	00005030			3772+REA81	DC	A(RE81)	result address
00004FD0	00000000 00000000			3773+	DS	2FD	gap
00004FD8	00000000 00000000						
00004FE0	00000000 00000000			3774+V1081	DS	XL16	V1 output
00004FE8	00000000 00000000						
00004FF0	00000000 00000000			3775+	DS	2FD	gap
00004FF8	00000000 00000000						
				3776+*			
00005000				3777+X81	DS	0F	
00005000	E310 5024 0014		00000024	3778+	LGF	R1, V2ADDR	load v2 source
00005006	E761 0000 0806		00000000	3779+	VL	v22, 0(R1)	use v21 to test decoder
0000500C	E310 5028 0014		00000028	3780+	LGF	R1, V3ADDR	load v3 source
00005012	E771 0000 0806		00000000	3781+	VL	v23, 0(R1)	use v22 to test decoder
00005018	E756 7010 1EF8			3782+	VCEQ	V21, V22, V23, 1, 1	test instruction
0000501E	B98D 0020			3783+	EPSW	R2, R0	extract psw
00005022	5020 500C		0000000C	3784+	ST	R2, CCPSW	to save CC
00005026	E750 5048 080E		00004FE0	3785+	VST	V21, V1081	save v1 output
0000502C	07FB			3786+	BR	R11	return
00005030				3787+RE81	DC	0F	V1 for this test
00005030				3788+	DROP	R5	
00005030	FFFF0000 00000000			3789	DC	XL16' FFFF000000000000 FFFFFFFFFFFFFFFFFF'	result
00005038	FFFFFFFF FFFFFFFF						
00005040	00010203 04050607			3790	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v2
00005048	08090A0B 0C0DFE0F						
00005050	00010033 00550077			3791	DC	XL16' 0001003300550077 08090A0B0C0DFE0F'	v3
00005058	08090A0B 0C0DFE0F						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				3792			
				3793	VRR_B	VCEQ, 1, 1	
00005060				3794+	DS	0FD	
00005060		00005060		3795+	USING	*, R5	base for test data and test routine
00005060	000050C8			3796+T82	DC	A(X82)	address of test routine
00005064	0052			3797+	DC	H' 82'	test number
00005066	00			3798+	DC	X' 00'	
00005067	01			3799+	DC	HL1' 1'	m4 used
00005068	01			3800+	DC	HL1' 1'	m5 used
00005069	01			3801+	DC	HL1' 1'	CC
0000506A	0B			3802+	DC	HL1' 11'	CC failed mask
0000506C	00000000 00000000			3803+	DS	2F	extracted PSW after test (has CC)
00005074	FF			3804+	DC	X' FF'	extracted CC, if test failed
00005075	E5C3C5D8 40404040			3805+	DC	CL8' VCEQ'	instruction name
00005080	000050F8			3806+	DC	A(RE82)	address of v1 result
00005084	00005108			3807+	DC	A(RE82+16)	address of v2 source
00005088	00005118			3808+	DC	A(RE82+32)	address of v3 source
0000508C	00000010			3809+	DC	A(16)	result length
00005090	000050F8			3810+REA82	DC	A(RE82)	result address
00005098	00000000 00000000			3811+	DS	2FD	gap
000050A0	00000000 00000000						
000050A8	00000000 00000000			3812+V1082	DS	XL16	V1 output
000050B0	00000000 00000000						
000050B8	00000000 00000000			3813+	DS	2FD	gap
000050C0	00000000 00000000						
				3814+*			
000050C8				3815+X82	DS	0F	
000050C8	E310 5024 0014		00000024	3816+	LGF	R1, V2ADDR	load v2 source
000050CE	E761 0000 0806		00000000	3817+	VL	v22, 0(R1)	use v21 to test decoder
000050D4	E310 5028 0014		00000028	3818+	LGF	R1, V3ADDR	load v3 source
000050DA	E771 0000 0806		00000000	3819+	VL	v23, 0(R1)	use v22 to test decoder
000050E0	E756 7010 1EF8			3820+	VCEQ	V21, V22, V23, 1, 1	test instruction
000050E6	B98D 0020			3821+	EPSW	R2, R0	extract psw
000050EA	5020 500C		0000000C	3822+	ST	R2, CCPSW	to save CC
000050EE	E750 5048 080E		000050A8	3823+	VST	V21, V1082	save v1 output
000050F4	07FB			3824+	BR	R11	return
000050F8				3825+RE82	DC	0F	V1 for this test
000050F8				3826+	DROP	R5	
000050F8	FFFFFFFF FFFFFFFF			3827	DC	XL16' FFFFFFFFFFFFFFFFFF 000000000000FFFF'	result t
00005100	00000000 0000FFFF						
00005108	08090A0B 0C0DFE0F			3828	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v2
00005110	00010203 04050607						
00005118	08090A0B 0C0DFE0F			3829	DC	XL16' 08090A0B0C0DFE0F 0011003300550607'	v3
00005120	00110033 00550607						
				3830			
				3831	VRR_B	VCEQ, 1, 3	
00005128				3832+	DS	0FD	
00005128		00005128		3833+	USING	*, R5	base for test data and test routine
00005128	00005190			3834+T83	DC	A(X83)	address of test routine
0000512C	0053			3835+	DC	H' 83'	test number
0000512E	00			3836+	DC	X' 00'	
0000512F	01			3837+	DC	HL1' 1'	m4 used
00005130	01			3838+	DC	HL1' 1'	m5 used
00005131	03			3839+	DC	HL1' 3'	CC
00005132	0E			3840+	DC	HL1' 14'	CC failed mask
00005134	00000000 00000000			3841+	DS	2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000513C	FF			3842+	DC	X' FF'	extracted CC, if test failed
0000513D	E5C3C5D8 40404040			3843+	DC	CL8' VCEQ'	instruction name
00005148	000051C0			3844+	DC	A(RE83)	address of v1 result
0000514C	000051D0			3845+	DC	A(RE83+16)	address of v2 source
00005150	000051E0			3846+	DC	A(RE83+32)	address of v3 source
00005154	00000010			3847+	DC	A(16)	result length
00005158	000051C0			3848+REA83	DC	A(RE83)	result address
00005160	00000000 00000000			3849+	DS	2FD	gap
00005168	00000000 00000000						
00005170	00000000 00000000			3850+V1083	DS	XL16	V1 output
00005178	00000000 00000000						
00005180	00000000 00000000			3851+	DS	2FD	gap
00005188	00000000 00000000						
00005190				3852+*			
00005190	E310 5024 0014		00000024	3853+X83	DS	0F	
00005196	E761 0000 0806		00000000	3854+	LGF	R1, V2ADDR	load v2 source
0000519C	E310 5028 0014		00000028	3855+	VL	v22, 0(R1)	use v21 to test decoder
000051A2	E771 0000 0806		00000000	3856+	LGF	R1, V3ADDR	load v3 source
000051A8	E756 7010 1EF8			3857+	VL	v23, 0(R1)	use v22 to test decoder
000051AE	B98D 0020			3858+	VCEQ	V21, V22, V23, 1, 1	test instruction
000051B2	5020 500C		0000000C	3859+	EPSW	R2, R0	extract psw
000051B6	E750 5048 080E		00005170	3860+	ST	R2, CCPSW	to save CC
000051BC	07FB			3861+	VST	V21, V1083	save v1 output
000051C0				3862+	BR	R11	return
000051C0				3863+RE83	DC	0F	V1 for this test
000051C0	00000000 00000000			3864+	DROP	R5	
000051C8	00000000 00000000			3865	DC	XL16' 0000000000000000 0000000000000000'	result
000051D0	01110133 01550177			3866	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
000051D8	019901BB 01DD01FF						
000051E0	00010203 04050607			3867	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
000051E8	08090A0B 0C0D0E0F						
000051F0				3868			
000051F0				3869	VRR_B	VCEQ, 1, 3	
000051F0	00005258	000051F0		3870+	DS	0FD	
000051F0				3871+	USING	*, R5	base for test data and test routine
000051F4	0054			3872+T84	DC	A(X84)	address of test routine
000051F6	00			3873+	DC	H' 84'	test number
000051F7	01			3874+	DC	X' 00'	
000051F8	01			3875+	DC	HL1' 1'	m4 used
000051F9	03			3876+	DC	HL1' 1'	m5 used
000051FA	0E			3877+	DC	HL1' 3'	CC
000051FC	00000000 00000000			3878+	DC	HL1' 14'	CC failed mask
00005204	FF			3879+	DS	2F	extracted PSW after test (has CC)
00005205	E5C3C5D8 40404040			3880+	DC	X' FF'	extracted CC, if test failed
00005210	00005288			3881+	DC	CL8' VCEQ'	instruction name
00005214	00005298			3882+	DC	A(RE84)	address of v1 result
00005218	000052A8			3883+	DC	A(RE84+16)	address of v2 source
0000521C	00000010			3884+	DC	A(RE84+32)	address of v3 source
00005220	00005288			3885+	DC	A(16)	result length
00005228	00000000 00000000			3886+REA84	DC	A(RE84)	result address
00005230	00000000 00000000			3887+	DS	2FD	gap
00005238	00000000 00000000			3888+V1084	DS	XL16	V1 output
00005240	00000000 00000000						
00005248	00000000 00000000			3889+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005250	00000000 00000000			3890+*			
00005258				3891+X84	DS	0F	
00005258	E310 5024 0014		00000024	3892+	LGF	R1, V2ADDR	load v2 source
0000525E	E761 0000 0806		00000000	3893+	VL	v22, 0(R1)	use v21 to test decoder
00005264	E310 5028 0014		00000028	3894+	LGF	R1, V3ADDR	load v3 source
0000526A	E771 0000 0806		00000000	3895+	VL	v23, 0(R1)	use v22 to test decoder
00005270	E756 7010 1EF8			3896+	VCEQ	V21, V22, V23, 1, 1	test instruction
00005276	B98D 0020			3897+	EPSW	R2, R0	extract psw
0000527A	5020 500C		0000000C	3898+	ST	R2, CCPSW	to save CC
0000527E	E750 5048 080E		00005238	3899+	VST	V21, V1084	save v1 output
00005284	07FB			3900+	BR	R11	return
00005288				3901+RE84	DC	0F	V1 for this test
00005288				3902+	DROP	R5	
00005288	00000000 00000000			3903	DC	XL16' 0000000000000000 0000000000000000'	result t
00005290	00000000 00000000						
00005298	00010203 04050607			3904	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000052A0	08090A0B 0C0D0E0F						
000052A8	01110133 01550177			3905	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
000052B0	019901BB 01DD01FF						
				3906			
				3907 *Word			
				3908	VRR_B	VCEQ, 2, 0	
000052B8				3909+	DS	0FD	
000052B8		000052B8		3910+	USING	*, R5	base for test data and test routine
000052B8	00005320			3911+T85	DC	A(X85)	address of test routine
000052BC	0055			3912+	DC	H' 85'	test number
000052BE	00			3913+	DC	X' 00'	
000052BF	02			3914+	DC	HL1' 2'	m4 used
000052C0	01			3915+	DC	HL1' 1'	m5 used
000052C1	00			3916+	DC	HL1' 0'	CC
000052C2	07			3917+	DC	HL1' 7'	CC failed mask
000052C4	00000000 00000000			3918+	DS	2F	extracted PSW after test (has CC)
000052CC	FF			3919+	DC	X' FF'	extracted CC, if test failed
000052CD	E5C3C5D8 40404040			3920+	DC	CL8' VCEQ'	instruction name
000052D8	00005350			3921+	DC	A(RE85)	address of v1 result
000052DC	00005360			3922+	DC	A(RE85+16)	address of v2 source
000052E0	00005370			3923+	DC	A(RE85+32)	address of v3 source
000052E4	00000010			3924+	DC	A(16)	result length
000052E8	00005350			3925+REA85	DC	A(RE85)	result address
000052F0	00000000 00000000			3926+	DS	2FD	gap
000052F8	00000000 00000000						
00005300	00000000 00000000			3927+V1085	DS	XL16	V1 output
00005308	00000000 00000000						
00005310	00000000 00000000			3928+	DS	2FD	gap
00005318	00000000 00000000						
				3929+*			
00005320				3930+X85	DS	0F	
00005320	E310 5024 0014		00000024	3931+	LGF	R1, V2ADDR	load v2 source
00005326	E761 0000 0806		00000000	3932+	VL	v22, 0(R1)	use v21 to test decoder
0000532C	E310 5028 0014		00000028	3933+	LGF	R1, V3ADDR	load v3 source
00005332	E771 0000 0806		00000000	3934+	VL	v23, 0(R1)	use v22 to test decoder
00005338	E756 7010 2EF8			3935+	VCEQ	V21, V22, V23, 2, 1	test instruction
0000533E	B98D 0020			3936+	EPSW	R2, R0	extract psw
00005342	5020 500C		0000000C	3937+	ST	R2, CCPSW	to save CC
00005346	E750 5048 080E		00005300	3938+	VST	V21, V1085	save v1 output



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000534C	07FB			3939+	BR	R11	return
00005350				3940+RE85	DC	0F	V1 for this test
00005350				3941+	DROP	R5	
00005350	FFFFFFFF FFFFFFFF			3942	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005358	FFFFFFFF FFFFFFFF						
00005360	00110033 00550077			3943	DC	XL16' 0011003300550077 0022004400660008'	v2
00005368	00220044 00660008						
00005370	00110033 00550077			3944	DC	XL16' 0011003300550077 0022004400660008'	v3
00005378	00220044 00660008						
				3945			
				3946	VRR_B	VCEQ, 2, 0	
00005380				3947+	DS	0FD	
00005380		00005380		3948+	USING	*, R5	base for test data and test routine
00005380	000053E8			3949+T86	DC	A(X86)	address of test routine
00005384	0056			3950+	DC	H' 86'	test number
00005386	00			3951+	DC	X' 00'	
00005387	02			3952+	DC	HL1' 2'	m4 used
00005388	01			3953+	DC	HL1' 1'	m5 used
00005389	00			3954+	DC	HL1' 0'	CC
0000538A	07			3955+	DC	HL1' 7'	CC failed mask
0000538C	00000000 00000000			3956+	DS	2F	extracted PSW after test (has CC)
00005394	FF			3957+	DC	X' FF'	extracted CC, if test failed
00005395	E5C3C5D8 40404040			3958+	DC	CL8' VCEQ'	instruction name
000053A0	00005418			3959+	DC	A(RE86)	address of v1 result
000053A4	00005428			3960+	DC	A(RE86+16)	address of v2 source
000053A8	00005438			3961+	DC	A(RE86+32)	address of v3 source
000053AC	00000010			3962+	DC	A(16)	result length
000053B0	00005418			3963+REA86	DC	A(RE86)	result address
000053B8	00000000 00000000			3964+	DS	2FD	gap
000053C0	00000000 00000000						
000053C8	00000000 00000000			3965+V1086	DS	XL16	V1 output
000053D0	00000000 00000000						
000053D8	00000000 00000000			3966+	DS	2FD	gap
000053E0	00000000 00000000						
				3967+*			
000053E8				3968+X86	DS	0F	
000053E8	E310 5024 0014		00000024	3969+	LGF	R1, V2ADDR	load v2 source
000053EE	E761 0000 0806		00000000	3970+	VL	v22, 0(R1)	use v21 to test decoder
000053F4	E310 5028 0014		00000028	3971+	LGF	R1, V3ADDR	load v3 source
000053FA	E771 0000 0806		00000000	3972+	VL	v23, 0(R1)	use v22 to test decoder
00005400	E756 7010 2EF8			3973+	VCEQ	V21, V22, V23, 2, 1	test instruction
00005406	B98D 0020			3974+	EPSW	R2, R0	extract psw
0000540A	5020 500C		0000000C	3975+	ST	R2, CCPSW	to save CC
0000540E	E750 5048 080E		000053C8	3976+	VST	V21, V1086	save v1 output
00005414	07FB			3977+	BR	R11	return
00005418				3978+RE86	DC	0F	V1 for this test
00005418				3979+	DROP	R5	
00005418	FFFFFFFF FFFFFFFF			3980	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005420	FFFFFFFF FFFFFFFF						
00005428	FFFEFFFD FFFCFFFB			3981	DC	XL16' FFFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00005430	FFFAFFF9 FFF8FFF7						
00005438	FFFEFFFD FFFCFFFB			3982	DC	XL16' FFFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00005440	FFFAFFF9 FFF8FFF7						
				3983			
				3984	VRR_B	VCEQ, 2, 1	
00005448				3985+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00005448		00005448		3986+	USING *, R5	base for test data and test routine
00005448	000054B0			3987+T87	DC A(X87)	address of test routine
0000544C	0057			3988+	DC H' 87'	test number
0000544E	00			3989+	DC X' 00'	
0000544F	02			3990+	DC HL1' 2'	m4 used
00005450	01			3991+	DC HL1' 1'	m5 used
00005451	01			3992+	DC HL1' 1'	CC
00005452	0B			3993+	DC HL1' 11'	CC failed mask
00005454	00000000 00000000			3994+	DS 2F	extracted PSW after test (has CC)
0000545C	FF			3995+	DC X' FF'	extracted CC, if test failed
0000545D	E5C3C5D8 40404040			3996+	DC CL8' VCEQ'	instruction name
00005468	000054E0			3997+	DC A(RE87)	address of v1 result
0000546C	000054F0			3998+	DC A(RE87+16)	address of v2 source
00005470	00005500			3999+	DC A(RE87+32)	address of v3 source
00005474	00000010			4000+	DC A(16)	result length
00005478	000054E0			4001+REA87	DC A(RE87)	result address
00005480	00000000 00000000			4002+	DS 2FD	gap
00005488	00000000 00000000					
00005490	00000000 00000000			4003+V1087	DS XL16	V1 output
00005498	00000000 00000000					
000054A0	00000000 00000000			4004+	DS 2FD	gap
000054A8	00000000 00000000					
				4005+*		
000054B0				4006+X87	DS 0F	
000054B0	E310 5024 0014		00000024	4007+	LGF R1, V2ADDR	load v2 source
000054B6	E761 0000 0806		00000000	4008+	VL v22, 0(R1)	use v21 to test decoder
000054BC	E310 5028 0014		00000028	4009+	LGF R1, V3ADDR	load v3 source
000054C2	E771 0000 0806		00000000	4010+	VL v23, 0(R1)	use v22 to test decoder
000054C8	E756 7010 2EF8			4011+	VCEQ V21, V22, V23, 2, 1	test instruction
000054CE	B98D 0020			4012+	EPSW R2, R0	extract psw
000054D2	5020 500C		0000000C	4013+	ST R2, CCPSW	to save CC
000054D6	E750 5048 080E		00005490	4014+	VST V21, V1087	save v1 output
000054DC	07FB			4015+	BR R11	return
000054E0				4016+RE87	DC 0F	V1 for this test
000054E0				4017+	DROP R5	
000054E0	FFFFFFFF 00000000			4018	DC XL16' FFFFFFFF00000000 FFFFFFFF' result t	
000054E8	FFFFFFFF FFFFFFFF					
000054F0	00010203 04050607			4019	DC XL16' 0001020304050607 08090A0B0C0DFE0F'	v2
000054F8	08090A0B 0C0DFE0F					
00005500	00010203 00550077			4020	DC XL16' 0001020300550077 08090A0B0C0DFE0F'	v3
00005508	08090A0B 0C0DFE0F					
				4021		
				4022	VRR_B VCEQ, 2, 1	
00005510				4023+	DS 0FD	
00005510		00005510		4024+	USING *, R5	base for test data and test routine
00005510	00005578			4025+T88	DC A(X88)	address of test routine
00005514	0058			4026+	DC H' 88'	test number
00005516	00			4027+	DC X' 00'	
00005517	02			4028+	DC HL1' 2'	m4 used
00005518	01			4029+	DC HL1' 1'	m5 used
00005519	01			4030+	DC HL1' 1'	CC
0000551A	0B			4031+	DC HL1' 11'	CC failed mask
0000551C	00000000 00000000			4032+	DS 2F	extracted PSW after test (has CC)
00005524	FF			4033+	DC X' FF'	extracted CC, if test failed
00005525	E5C3C5D8 40404040			4034+	DC CL8' VCEQ'	instruction name
00005530	000055A8			4035+	DC A(RE88)	address of v1 result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005534	000055B8			4036+	DC	A(RE88+16)	address of v2 source
00005538	000055C8			4037+	DC	A(RE88+32)	address of v3 source
0000553C	00000010			4038+	DC	A(16)	result length
00005540	000055A8			4039+REA88	DC	A(RE88)	result address
00005548	00000000 00000000			4040+	DS	2FD	gap
00005550	00000000 00000000						
00005558	00000000 00000000			4041+V1088	DS	XL16	V1 output
00005560	00000000 00000000						
00005568	00000000 00000000			4042+	DS	2FD	gap
00005570	00000000 00000000						
				4043+*			
00005578				4044+X88	DS	0F	
00005578	E310 5024 0014		00000024	4045+	LGF	R1, V2ADDR	load v2 source
0000557E	E761 0000 0806		00000000	4046+	VL	v22, 0(R1)	use v21 to test decoder
00005584	E310 5028 0014		00000028	4047+	LGF	R1, V3ADDR	load v3 source
0000558A	E771 0000 0806		00000000	4048+	VL	v23, 0(R1)	use v22 to test decoder
00005590	E756 7010 2EF8			4049+	VCEQ	V21, V22, V23, 2, 1	test instruction
00005596	B98D 0020			4050+	EPSW	R2, R0	extract psw
0000559A	5020 500C		0000000C	4051+	ST	R2, CCPSW	to save CC
0000559E	E750 5048 080E		00005558	4052+	VST	V21, V1088	save v1 output
000055A4	07FB			4053+	BR	R11	return
000055A8				4054+RE88	DC	0F	V1 for this test
000055A8				4055+	DROP	R5	
000055A8	FFFFFFFF FFFFFFFF			4056	DC	XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result
000055B0	00000000 FFFFFFFF						
000055B8	08090A0B 0C0DFE0F			4057	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v2
000055C0	00010203 04050607						
000055C8	08090A0B 0C0DFE0F			4058	DC	XL16' 08090A0B0C0DFE0F 0011003304050607'	v3
000055D0	00110033 04050607						
				4059			
000055D8				4060	VRR_B	VCEQ, 2, 3	
000055D8		000055D8		4061+	DS	0FD	
000055D8	00005640			4062+	USING	*, R5	base for test data and test routine
000055DC	0059			4063+T89	DC	A(X89)	address of test routine
000055DE	00			4064+	DC	H' 89'	test number
000055DF	02			4065+	DC	X' 00'	
000055E0	01			4066+	DC	HL1' 2'	m4 used
000055E1	03			4067+	DC	HL1' 1'	m5 used
000055E2	0E			4068+	DC	HL1' 3'	CC
000055E4	00000000 00000000			4069+	DC	HL1' 14'	CC failed mask
000055EC	FF			4070+	DS	2F	extracted PSW after test (has CC)
000055ED	E5C3C5D8 40404040			4071+	DC	X' FF'	extracted CC, if test failed
000055F8	00005670			4072+	DC	CL8' VCEQ'	instruction name
000055FC	00005680			4073+	DC	A(RE89)	address of v1 result
00005600	00005690			4074+	DC	A(RE89+16)	address of v2 source
00005604	00000010			4075+	DC	A(RE89+32)	address of v3 source
00005608	00005670			4076+	DC	A(16)	result length
00005610	00000000 00000000			4077+REA89	DC	A(RE89)	result address
00005618	00000000 00000000			4078+	DS	2FD	gap
00005620	00000000 00000000			4079+V1089	DS	XL16	V1 output
00005628	00000000 00000000						
00005630	00000000 00000000			4080+	DS	2FD	gap
00005638	00000000 00000000						
				4081+*			
00005640				4082+X89	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005640	E310 5024 0014		00000024	4083+	LGF	R1, V2ADDR	load v2 source
00005646	E761 0000 0806		00000000	4084+	VL	v22, 0(R1)	use v21 to test decoder
0000564C	E310 5028 0014		00000028	4085+	LGF	R1, V3ADDR	load v3 source
00005652	E771 0000 0806		00000000	4086+	VL	v23, 0(R1)	use v22 to test decoder
00005658	E756 7010 2EF8			4087+	VCEQ	V21, V22, V23, 2, 1	test instruction
0000565E	B98D 0020			4088+	EPSW	R2, R0	extract psw
00005662	5020 500C		0000000C	4089+	ST	R2, CCPSW	to save CC
00005666	E750 5048 080E		00005620	4090+	VST	V21, V1089	save v1 output
0000566C	07FB			4091+	BR	R11	return
00005670				4092+RE89	DC	0F	V1 for this test
00005670				4093+	DROP	R5	
00005670	00000000 00000000			4094	DC	XL16' 0000000000000000 0000000000000000'	result t
00005678	00000000 00000000						
00005680	01110133 01550177			4095	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00005688	019901BB 01DD01FF						
00005690	00010203 04050607			4096	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00005698	08090A0B 0C0D0E0F						
000056A0				4097			
000056A0				4098	VRR_B	VCEQ, 2, 3	
000056A0		000056A0		4099+	DS	0FD	
000056A0	00005708			4100+	USING	*, R5	base for test data and test routine
000056A4	005A			4101+T90	DC	A(X90)	address of test routine
000056A6	00			4102+	DC	H' 90'	test number
000056A7	02			4103+	DC	X' 00'	
000056A8	01			4104+	DC	HL1' 2'	m4 used
000056A9	03			4105+	DC	HL1' 1'	m5 used
000056AA	0E			4106+	DC	HL1' 3'	CC
000056AC	00000000 00000000			4107+	DC	HL1' 14'	CC failed mask
000056B4	FF			4108+	DS	2F	extracted PSW after test (has CC)
000056B5	E5C3C5D8 40404040			4109+	DC	X' FF'	extracted CC, if test failed
000056C0	00005738			4110+	DC	CL8' VCEQ'	instruction name
000056C4	00005748			4111+	DC	A(RE90)	address of v1 result
000056C8	00005758			4112+	DC	A(RE90+16)	address of v2 source
000056CC	00000010			4113+	DC	A(RE90+32)	address of v3 source
000056D0	00005738			4114+	DC	A(16)	result length
000056D8	00000000 00000000			4115+REA90	DC	A(RE90)	result address
000056E0	00000000 00000000			4116+	DS	2FD	gap
000056E8	00000000 00000000			4117+V1090	DS	XL16	V1 output
000056F0	00000000 00000000						
000056F8	00000000 00000000			4118+	DS	2FD	gap
00005700	00000000 00000000						
00005708				4119+*			
00005708	E310 5024 0014		00000024	4120+X90	DS	0F	
0000570E	E761 0000 0806		00000000	4121+	LGF	R1, V2ADDR	load v2 source
00005714	E310 5028 0014		00000028	4122+	VL	v22, 0(R1)	use v21 to test decoder
0000571A	E771 0000 0806		00000000	4123+	LGF	R1, V3ADDR	load v3 source
00005720	E756 7010 2EF8			4124+	VL	v23, 0(R1)	use v22 to test decoder
00005726	B98D 0020			4125+	VCEQ	V21, V22, V23, 2, 1	test instruction
0000572A	5020 500C		0000000C	4126+	EPSW	R2, R0	extract psw
0000572E	E750 5048 080E		000056E8	4127+	ST	R2, CCPSW	to save CC
00005734	07FB			4128+	VST	V21, V1090	save v1 output
00005738				4129+	BR	R11	return
00005738				4130+RE90	DC	0F	V1 for this test
00005738				4131+	DROP	R5	
00005738	00000000 00000000			4132	DC	XL16' 0000000000000000 0000000000000000'	result t



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005740	00000000	00000000					
00005748	00010203	04050607		4133	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00005750	08090A0B	0C0D0E0F					
00005758	01110133	01550177		4134	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00005760	019901BB	01DD01FF					
				4135			
				4136	*Doubleword		
				4137	VRR_B	VCEQ, 3, 0	
00005768				4138+	DS	0FD	
00005768		00005768		4139+	USING	*, R5	base for test data and test routine
00005768	000057D0			4140+T91	DC	A(X91)	address of test routine
0000576C	005B			4141+	DC	H' 91'	test number
0000576E	00			4142+	DC	X' 00'	
0000576F	03			4143+	DC	HL1' 3'	m4 used
00005770	01			4144+	DC	HL1' 1'	m5 used
00005771	00			4145+	DC	HL1' 0'	CC
00005772	07			4146+	DC	HL1' 7'	CC failed mask
00005774	00000000	00000000		4147+	DS	2F	extracted PSW after test (has CC)
0000577C	FF			4148+	DC	X' FF'	extracted CC, if test failed
0000577D	E5C3C5D8	40404040		4149+	DC	CL8' VCEQ'	instruction name
00005788	00005800			4150+	DC	A(RE91)	address of v1 result
0000578C	00005810			4151+	DC	A(RE91+16)	address of v2 source
00005790	00005820			4152+	DC	A(RE91+32)	address of v3 source
00005794	00000010			4153+	DC	A(16)	result length
00005798	00005800			4154+REA91	DC	A(RE91)	result address
000057A0	00000000	00000000		4155+	DS	2FD	gap
000057A8	00000000	00000000					
000057B0	00000000	00000000		4156+V1091	DS	XL16	V1 output
000057B8	00000000	00000000					
000057C0	00000000	00000000		4157+	DS	2FD	gap
000057C8	00000000	00000000					
				4158+*			
000057D0				4159+X91	DS	0F	
000057D0	E310 5024 0014		00000024	4160+	LGF	R1, V2ADDR	load v2 source
000057D6	E761 0000 0806		00000000	4161+	VL	v22, 0(R1)	use v21 to test decoder
000057DC	E310 5028 0014		00000028	4162+	LGF	R1, V3ADDR	load v3 source
000057E2	E771 0000 0806		00000000	4163+	VL	v23, 0(R1)	use v22 to test decoder
000057E8	E756 7010 3EF8			4164+	VCEQ	V21, V22, V23, 3, 1	test instruction
000057EE	B98D 0020			4165+	EPSW	R2, R0	extract psw
000057F2	5020 500C		0000000C	4166+	ST	R2, CCPSW	to save CC
000057F6	E750 5048 080E		000057B0	4167+	VST	V21, V1091	save v1 output
000057FC	07FB			4168+	BR	R11	return
00005800				4169+RE91	DC	0F	V1 for this test
00005800				4170+	DROP	R5	
00005800	FFFFFFFF	FFFFFFFF		4171	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00005808	FFFFFFFF	FFFFFFFF					
00005810	00110033	00550077		4172	DC	XL16' 0011003300550077 0022004400660008'	v2
00005818	00220044	00660008					
00005820	00110033	00550077		4173	DC	XL16' 0011003300550077 0022004400660008'	v3
00005828	00220044	00660008					
				4174			
				4175	VRR_B	VCEQ, 3, 0	
00005830				4176+	DS	0FD	
00005830		00005830		4177+	USING	*, R5	base for test data and test routine
00005830	00005898			4178+T92	DC	A(X92)	address of test routine
00005834	005C			4179+	DC	H' 92'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005836	00			4180+	DC	X' 00'	
00005837	03			4181+	DC	HL1' 3'	m4 used
00005838	01			4182+	DC	HL1' 1'	m5 used
00005839	00			4183+	DC	HL1' 0'	CC
0000583A	07			4184+	DC	HL1' 7'	CC failed mask
0000583C	00000000	00000000		4185+	DS	2F	extracted PSW after test (has CC)
00005844	FF			4186+	DC	X' FF'	extracted CC, if test failed
00005845	E5C3C5D8	40404040		4187+	DC	CL8' VCEQ'	instruction name
00005850	000058C8			4188+	DC	A(RE92)	address of v1 result
00005854	000058D8			4189+	DC	A(RE92+16)	address of v2 source
00005858	000058E8			4190+	DC	A(RE92+32)	address of v3 source
0000585C	00000010			4191+	DC	A(16)	result length
00005860	000058C8			4192+REA92	DC	A(RE92)	result address
00005868	00000000	00000000		4193+	DS	2FD	gap
00005870	00000000	00000000					
00005878	00000000	00000000		4194+V1092	DS	XL16	V1 output
00005880	00000000	00000000					
00005888	00000000	00000000		4195+	DS	2FD	gap
00005890	00000000	00000000					
00005898				4196+*			
00005898	E310 5024 0014		00000024	4197+X92	DS	0F	
0000589E	E761 0000 0806		00000000	4198+	LGF	R1, V2ADDR	load v2 source
000058A4	E310 5028 0014		00000028	4199+	VL	v22, 0(R1)	use v21 to test decoder
000058AA	E771 0000 0806		00000000	4200+	LGF	R1, V3ADDR	load v3 source
000058B0	E756 7010 3EF8			4201+	VL	v23, 0(R1)	use v22 to test decoder
000058B6	B98D 0020			4202+	VCEQ	V21, V22, V23, 3, 1	test instruction
000058BA	5020 500C		0000000C	4203+	EPSW	R2, R0	extract psw
000058BE	E750 5048 080E		00005878	4204+	ST	R2, CCPSW	to save CC
000058C4	07FB			4205+	VST	V21, V1092	save v1 output
000058C8				4206+	BR	R11	return
000058C8				4207+RE92	DC	0F	V1 for this test
000058C8				4208+	DROP	R5	
000058C8	FFFFFFFF FFFFFFFF			4209	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000058D0	FFFFFFFF FFFFFFFF						
000058D8	FFFEFFFD FFFCFFFB			4210	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
000058E0	FFFAFFF9 FFF8FFF7						
000058E8	FFFEFFFD FFFCFFFB			4211	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
000058F0	FFFAFFF9 FFF8FFF7						
000058F8				4212			
000058F8				4213	VRR_B	VCEQ, 3, 1	
000058F8	00005960	000058F8		4214+	DS	0FD	
000058FC	005D			4215+	USING	*, R5	base for test data and test routine
000058FE	00			4216+T93	DC	A(X93)	address of test routine
000058FF	03			4217+	DC	H' 93'	test number
00005900	01			4218+	DC	X' 00'	
00005901	01			4219+	DC	HL1' 3'	m4 used
00005902	0B			4220+	DC	HL1' 1'	m5 used
00005904	00000000	00000000		4221+	DC	HL1' 1'	CC
0000590C	FF			4222+	DC	HL1' 11'	CC failed mask
0000590D	E5C3C5D8	40404040		4223+	DS	2F	extracted PSW after test (has CC)
00005918	00005990			4224+	DC	X' FF'	extracted CC, if test failed
0000591C	000059A0			4225+	DC	CL8' VCEQ'	instruction name
00005920	000059B0			4226+	DC	A(RE93)	address of v1 result
00005924	00000010			4227+	DC	A(RE93+16)	address of v2 source
				4228+	DC	A(RE93+32)	address of v3 source
				4229+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005928	00005990			4230+REA93	DC	A(RE93)	result address
00005930	00000000 00000000			4231+	DS	2FD	gap
00005938	00000000 00000000						
00005940	00000000 00000000			4232+V1093	DS	XL16	V1 output
00005948	00000000 00000000						
00005950	00000000 00000000			4233+	DS	2FD	gap
00005958	00000000 00000000						
				4234+*			
00005960				4235+X93	DS	0F	
00005960	E310 5024 0014		00000024	4236+	LGF	R1, V2ADDR	load v2 source
00005966	E761 0000 0806		00000000	4237+	VL	v22, 0(R1)	use v21 to test decoder
0000596C	E310 5028 0014		00000028	4238+	LGF	R1, V3ADDR	load v3 source
00005972	E771 0000 0806		00000000	4239+	VL	v23, 0(R1)	use v22 to test decoder
00005978	E756 7010 3EF8			4240+	VCEQ	V21, V22, V23, 3, 1	test instruction
0000597E	B98D 0020			4241+	EPSW	R2, R0	extract psw
00005982	5020 500C		0000000C	4242+	ST	R2, CCPSW	to save CC
00005986	E750 5048 080E		00005940	4243+	VST	V21, V1093	save v1 output
0000598C	07FB			4244+	BR	R11	return
00005990				4245+RE93	DC	0F	V1 for this test
00005990				4246+	DROP	R5	
00005990	00000000 00000000			4247	DC	XL16' 0000000000000000 FFFFFFFF'	result
00005998	FFFFFFFF FFFFFFFF						
000059A0	00010203 04050607			4248	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v2
000059A8	08090A0B 0C0DFE0F						
000059B0	00110033 00550077			4249	DC	XL16' 0011003300550077 08090A0B0C0DFE0F'	v3
000059B8	08090A0B 0C0DFE0F						
				4250			
000059C0				4251	VRR_B	VCEQ, 3, 1	
000059C0		000059C0		4252+	DS	0FD	
000059C0	00005A28			4253+	USING	*, R5	base for test data and test routine
000059C4	005E			4254+T94	DC	A(X94)	address of test routine
000059C6	00			4255+	DC	H' 94'	test number
000059C7	03			4256+	DC	X' 00'	
000059C8	01			4257+	DC	HL1' 3'	m4 used
000059C9	01			4258+	DC	HL1' 1'	m5 used
000059CA	0B			4259+	DC	HL1' 1'	CC
000059CC	00000000 00000000			4260+	DC	HL1' 11'	CC failed mask
000059D4	FF			4261+	DS	2F	extracted PSW after test (has CC)
000059D5	E5C3C5D8 40404040			4262+	DC	X' FF'	extracted CC, if test failed
000059E0	00005A58			4263+	DC	CL8' VCEQ'	instruction name
000059E4	00005A68			4264+	DC	A(RE94)	address of v1 result
000059E8	00005A78			4265+	DC	A(RE94+16)	address of v2 source
000059EC	00000010			4266+	DC	A(RE94+32)	address of v3 source
000059F0	00005A58			4267+	DC	A(16)	result length
000059F8	00000000 00000000			4268+REA94	DC	A(RE94)	result address
00005A00	00000000 00000000			4269+	DS	2FD	gap
00005A08	00000000 00000000			4270+V1094	DS	XL16	V1 output
00005A10	00000000 00000000						
00005A18	00000000 00000000			4271+	DS	2FD	gap
00005A20	00000000 00000000						
				4272+*			
00005A28				4273+X94	DS	0F	
00005A28	E310 5024 0014		00000024	4274+	LGF	R1, V2ADDR	load v2 source
00005A2E	E761 0000 0806		00000000	4275+	VL	v22, 0(R1)	use v21 to test decoder
00005A34	E310 5028 0014		00000028	4276+	LGF	R1, V3ADDR	load v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005A3A	E771 0000 0806		00000000	4277+	VL	v23, 0(R1)	use v22 to test decoder
00005A40	E756 7010 3EF8			4278+	VCEQ	V21, V22, V23, 3, 1	test instruction
00005A46	B98D 0020			4279+	EPSW	R2, R0	extract psw
00005A4A	5020 500C		0000000C	4280+	ST	R2, CCPSW	to save CC
00005A4E	E750 5048 080E		00005A08	4281+	VST	V21, V1094	save v1 output
00005A54	07FB			4282+	BR	R11	return
00005A58				4283+RE94	DC	0F	V1 for this test
00005A58				4284+	DROP	R5	
00005A58	FFFFFFFF FFFFFFFF			4285	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result t
00005A60	00000000 00000000						
00005A68	08090A0B 0C0DFE0F			4286	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v2
00005A70	00010203 04050607						
00005A78	08090A0B 0C0DFE0F			4287	DC	XL16' 08090A0B0C0DFE0F 0011003300550077'	v3
00005A80	00110033 00550077						
				4288			
				4289	VRR_B	VCEQ, 3, 3	
00005A88				4290+	DS	0FD	
00005A88		00005A88		4291+	USING	*, R5	base for test data and test routine
00005A88	00005AF0			4292+T95	DC	A(X95)	address of test routine
00005A8C	005F			4293+	DC	H' 95'	test number
00005A8E	00			4294+	DC	X' 00'	
00005A8F	03			4295+	DC	HL1' 3'	m4 used
00005A90	01			4296+	DC	HL1' 1'	m5 used
00005A91	03			4297+	DC	HL1' 3'	CC
00005A92	0E			4298+	DC	HL1' 14'	CC failed mask
00005A94	00000000 00000000			4299+	DS	2F	extracted PSW after test (has CC)
00005A9C	FF			4300+	DC	X' FF'	extracted CC, if test failed
00005A9D	E5C3C5D8 40404040			4301+	DC	CL8' VCEQ'	instruction name
00005AA8	00005B20			4302+	DC	A(RE95)	address of v1 result
00005AAC	00005B30			4303+	DC	A(RE95+16)	address of v2 source
00005AB0	00005B40			4304+	DC	A(RE95+32)	address of v3 source
00005AB4	00000010			4305+	DC	A(16)	result length
00005AB8	00005B20			4306+REA95	DC	A(RE95)	result address
00005AC0	00000000 00000000			4307+	DS	2FD	gap
00005AC8	00000000 00000000						
00005AD0	00000000 00000000			4308+V1095	DS	XL16	V1 output
00005AD8	00000000 00000000						
00005AE0	00000000 00000000			4309+	DS	2FD	gap
00005AE8	00000000 00000000						
				4310+*			
00005AF0				4311+X95	DS	0F	
00005AF0	E310 5024 0014		00000024	4312+	LGF	R1, V2ADDR	load v2 source
00005AF6	E761 0000 0806		00000000	4313+	VL	v22, 0(R1)	use v21 to test decoder
00005AFC	E310 5028 0014		00000028	4314+	LGF	R1, V3ADDR	load v3 source
00005B02	E771 0000 0806		00000000	4315+	VL	v23, 0(R1)	use v22 to test decoder
00005B08	E756 7010 3EF8			4316+	VCEQ	V21, V22, V23, 3, 1	test instruction
00005B0E	B98D 0020			4317+	EPSW	R2, R0	extract psw
00005B12	5020 500C		0000000C	4318+	ST	R2, CCPSW	to save CC
00005B16	E750 5048 080E		00005AD0	4319+	VST	V21, V1095	save v1 output
00005B1C	07FB			4320+	BR	R11	return
00005B20				4321+RE95	DC	0F	V1 for this test
00005B20				4322+	DROP	R5	
00005B20	00000000 00000000			4323	DC	XL16' 0000000000000000 0000000000000000'	result t
00005B28	00000000 00000000						
00005B30	01110133 01550177			4324	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00005B38	019901BB 01DD01FF						



LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00005B40	00010203 04050607			4325	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3		
00005B48	08090A0B 0C0D0E0F								
				4326					
				4327	VRR_B	VCEQ, 3, 3			
00005B50				4328+	DS	0FD			
00005B50		00005B50		4329+	USING	*, R5	base for test data and test routine		
00005B50	00005BB8			4330+T96	DC	A(X96)	address of test routine		
00005B54	0060			4331+	DC	H' 96'	test number		
00005B56	00			4332+	DC	X' 00'			
00005B57	03			4333+	DC	HL1' 3'	m4 used		
00005B58	01			4334+	DC	HL1' 1'	m5 used		
00005B59	03			4335+	DC	HL1' 3'	CC		
00005B5A	0E			4336+	DC	HL1' 14'	CC failed mask		
00005B5C	00000000 00000000			4337+	DS	2F	extracted PSW after test (has CC)		
00005B64	FF			4338+	DC	X' FF'	extracted CC, if test failed		
00005B65	E5C3C5D8 40404040			4339+	DC	CL8' VCEQ'	instruction name		
00005B70	00005BE8			4340+	DC	A(RE96)	address of v1 result		
00005B74	00005BF8			4341+	DC	A(RE96+16)	address of v2 source		
00005B78	00005C08			4342+	DC	A(RE96+32)	address of v3 source		
00005B7C	00000010			4343+	DC	A(16)	result length		
00005B80	00005BE8			4344+REA96	DC	A(RE96)	result address		
00005B88	00000000 00000000			4345+	DS	2FD	gap		
00005B90	00000000 00000000								
00005B98	00000000 00000000			4346+V1096	DS	XL16	V1 output		
00005BA0	00000000 00000000								
00005BA8	00000000 00000000			4347+	DS	2FD	gap		
00005BB0	00000000 00000000								
				4348+*					
00005BB8				4349+X96	DS	0F			
00005BB8	E310 5024 0014		00000024	4350+	LGF	R1, V2ADDR	load v2 source		
00005BBE	E761 0000 0806		00000000	4351+	VL	v22, 0(R1)	use v21 to test decoder		
00005BC4	E310 5028 0014		00000028	4352+	LGF	R1, V3ADDR	load v3 source		
00005BCA	E771 0000 0806		00000000	4353+	VL	v23, 0(R1)	use v22 to test decoder		
00005BD0	E756 7010 3EF8			4354+	VCEQ	V21, V22, V23, 3, 1	test instruction		
00005BD6	B98D 0020			4355+	EPSW	R2, R0	extract psw		
00005BDA	5020 500C		0000000C	4356+	ST	R2, CCPSW	to save CC		
00005BDE	E750 5048 080E		00005B98	4357+	VST	V21, V1096	save v1 output		
00005BE4	07FB			4358+	BR	R11	return		
00005BE8				4359+RE96	DC	0F	V1 for this test		
00005BE8				4360+	DROP	R5			
00005BE8	00000000 00000000			4361	DC	XL16' 0000000000000000 0000000000000000'	result t		
00005BF0	00000000 00000000								
00005BF8	00010203 04050607			4362	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2		
00005C00	08090A0B 0C0D0E0F								
00005C08	01110133 01550177			4363	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3		
00005C10	019901BB 01DD01FF								
				4364					
				4365	*	-----			
				4366	*	VCHL - Vector Compare High Logical			
				4367	*	-----			
				4368	*	cc=0: All elements high			
				4369	*	cc=1: Some elements high			
				4370	*	cc=3: No element high			
				4371	*	-----			
				4372	*	case - simple cc debug			
				4373	*	-----			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				4374 *Byte		
				4375	VRR_B VCHL, 0, 0	
00005C18				4376+	DS 0FD	
00005C18		00005C18		4377+	USING *, R5	base for test data and test routine
00005C18	00005C80			4378+T97	DC A(X97)	address of test routine
00005C1C	0061			4379+	DC H' 97'	test number
00005C1E	00			4380+	DC X' 00'	
00005C1F	00			4381+	DC HL1' 0'	m4 used
00005C20	01			4382+	DC HL1' 1'	m5 used
00005C21	00			4383+	DC HL1' 0'	CC
00005C22	07			4384+	DC HL1' 7'	CC failed mask
00005C24	00000000 00000000			4385+	DS 2F	extracted PSW after test (has CC)
00005C2C	FF			4386+	DC X' FF'	extracted CC, if test failed
00005C2D	E5C3C8D3 40404040			4387+	DC CL8' VCHL'	instruction name
00005C38	00005CB0			4388+	DC A(RE97)	address of v1 result
00005C3C	00005CC0			4389+	DC A(RE97+16)	address of v2 source
00005C40	00005CD0			4390+	DC A(RE97+32)	address of v3 source
00005C44	00000010			4391+	DC A(16)	result length
00005C48	00005CB0			4392+REA97	DC A(RE97)	result address
00005C50	00000000 00000000			4393+	DS 2FD	gap
00005C58	00000000 00000000					
00005C60	00000000 00000000			4394+V1097	DS XL16	V1 output
00005C68	00000000 00000000					
00005C70	00000000 00000000			4395+	DS 2FD	gap
00005C78	00000000 00000000					
				4396+*		
00005C80				4397+X97	DS 0F	
00005C80	E310 5024 0014		00000024	4398+	LGF R1, V2ADDR	load v2 source
00005C86	E761 0000 0806		00000000	4399+	VL v22, 0(R1)	use v21 to test decoder
00005C8C	E310 5028 0014		00000028	4400+	LGF R1, V3ADDR	load v3 source
00005C92	E771 0000 0806		00000000	4401+	VL v23, 0(R1)	use v22 to test decoder
00005C98	E756 7010 0EF9			4402+	VCHL V21, V22, V23, 0, 1	test instruction
00005C9E	B98D 0020			4403+	EPSW R2, R0	extract psw
00005CA2	5020 500C		0000000C	4404+	ST R2, CCPSW	to save CC
00005CA6	E750 5048 080E		00005C60	4405+	VST V21, V1097	save v1 output
00005CAC	07FB			4406+	BR R11	return
00005CB0				4407+RE97	DC 0F	V1 for this test
00005CB0				4408+	DROP R5	
00005CB0	FFFFFFFF FFFFFFFF			4409	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005CB8	FFFFFFFF FFFFFFFF					
00005CC0	FFFFFFFF FFFFFFFF			4410	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00005CC8	FFFFFFFF FFFFFFFF					
00005CD0	00000000 00000000			4411	DC XL16' 0000000000000000 0000000000000000'	v3
00005CD8	00000000 00000000					
				4412		
00005CE0				4413	VRR_B VCHL, 0, 1	
00005CE0		00005CE0		4414+	DS 0FD	
00005CE0	00005D48			4415+	USING *, R5	base for test data and test routine
00005CE4	0062			4416+T98	DC A(X98)	address of test routine
00005CE6	00			4417+	DC H' 98'	test number
00005CE7	00			4418+	DC X' 00'	
00005CE8	01			4419+	DC HL1' 0'	m4 used
00005CE9	01			4420+	DC HL1' 1'	m5 used
00005CEA	0B			4421+	DC HL1' 1'	CC
00005CEC	00000000 00000000			4422+	DC HL1' 11'	CC failed mask
				4423+	DS 2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005CF4	FF			4424+	DC	X' FF'	extracted CC, if test failed
00005CF5	E5C3C8D3 40404040			4425+	DC	CL8' VCHL'	instruction name
00005D00	00005D78			4426+	DC	A(RE98)	address of v1 result
00005D04	00005D88			4427+	DC	A(RE98+16)	address of v2 source
00005D08	00005D98			4428+	DC	A(RE98+32)	address of v3 source
00005D0C	00000010			4429+	DC	A(16)	result length
00005D10	00005D78			4430+REA98	DC	A(RE98)	result address
00005D18	00000000 00000000			4431+	DS	2FD	gap
00005D20	00000000 00000000						
00005D28	00000000 00000000			4432+V1098	DS	XL16	V1 output
00005D30	00000000 00000000						
00005D38	00000000 00000000			4433+	DS	2FD	gap
00005D40	00000000 00000000						
00005D48				4434+*			
00005D48	E310 5024 0014			4435+X98	DS	0F	
00005D4E	E761 0000 0806		00000024	4436+	LGF	R1, V2ADDR	load v2 source
00005D54	E310 5028 0014		00000000	4437+	VL	v22, 0(R1)	use v21 to test decoder
00005D5A	E771 0000 0806		00000028	4438+	LGF	R1, V3ADDR	load v3 source
00005D60	E756 7010 0EF9		00000000	4439+	VL	v23, 0(R1)	use v22 to test decoder
00005D66	B98D 0020			4440+	VCHL	V21, V22, V23, 0, 1	test instruction
00005D6A	5020 500C		0000000C	4441+	EPSW	R2, R0	extract psw
00005D6E	E750 5048 080E		00005D28	4442+	ST	R2, CCPSW	to save CC
00005D74	07FB			4443+	VST	V21, V1098	save v1 output
00005D78				4444+	BR	R11	return
00005D78				4445+RE98	DC	0F	V1 for this test
00005D78				4446+	DROP	R5	
00005D78	00000000 00000000			4447	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result
00005D80	FFFFFFFF 00000000						
00005D88	00000000 00000000			4448	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v2
00005D90	8FFF8FFF 00000000						
00005D98	00000000 00000000			4449	DC	XL16' 0000000000000000 0000000000000000'	v3
00005DA0	00000000 00000000						
00005DA8				4450			
00005DA8				4451	VRR_B	VCHL, 0, 3	
00005DA8	00005E10	00005DA8		4452+	DS	0FD	
00005DAC	0063			4453+	USING	*, R5	base for test data and test routine
00005DAE	00			4454+T99	DC	A(X99)	address of test routine
00005DAF	00			4455+	DC	H' 99'	test number
00005DB0	01			4456+	DC	X' 00'	
00005DB1	03			4457+	DC	HL1' 0'	m4 used
00005DB2	0E			4458+	DC	HL1' 1'	m5 used
00005DB4	00000000 00000000			4459+	DC	HL1' 3'	CC
00005DBC	FF			4460+	DC	HL1' 14'	CC failed mask
00005DBD	E5C3C8D3 40404040			4461+	DS	2F	extracted PSW after test (has CC)
00005DC8	00005E40			4462+	DC	X' FF'	extracted CC, if test failed
00005DCC	00005E50			4463+	DC	CL8' VCHL'	instruction name
00005DD0	00005E60			4464+	DC	A(RE99)	address of v1 result
00005DD4	00000010			4465+	DC	A(RE99+16)	address of v2 source
00005DD8	00005E40			4466+	DC	A(RE99+32)	address of v3 source
00005DE0	00000000 00000000			4467+	DC	A(16)	result length
00005DE8	00000000 00000000			4468+REA99	DC	A(RE99)	result address
00005DF0	00000000 00000000			4469+	DS	2FD	gap
00005DF8	00000000 00000000						
00005E00	00000000 00000000			4470+V1099	DS	XL16	V1 output
				4471+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005E08	00000000 00000000			4472+*			
00005E10				4473+X99	DS	0F	
00005E10	E310 5024 0014		00000024	4474+	LGF	R1, V2ADDR	load v2 source
00005E16	E761 0000 0806		00000000	4475+	VL	v22, 0(R1)	use v21 to test decoder
00005E1C	E310 5028 0014		00000028	4476+	LGF	R1, V3ADDR	load v3 source
00005E22	E771 0000 0806		00000000	4477+	VL	v23, 0(R1)	use v22 to test decoder
00005E28	E756 7010 0EF9			4478+	VCHL	V21, V22, V23, 0, 1	test instruction
00005E2E	B98D 0020			4479+	EPSW	R2, R0	extract psw
00005E32	5020 500C		0000000C	4480+	ST	R2, CCPSW	to save CC
00005E36	E750 5048 080E		00005DF0	4481+	VST	V21, V1099	save v1 output
00005E3C	07FB			4482+	BR	R11	return
00005E40				4483+RE99	DC	0F	V1 for this test
00005E40				4484+	DROP	R5	
00005E40	00000000 00000000			4485	DC	XL16' 0000000000000000 0000000000000000'	result t
00005E48	00000000 00000000						
00005E50	00000000 00000000			4486	DC	XL16' 0000000000000000 0000000000000000'	v2
00005E58	00000000 00000000						
00005E60	00000000 00000000			4487	DC	XL16' 0000000000000000 0000000000000000'	v3
00005E68	00000000 00000000						
				4488			
				4489 *Hal fword			
				4490	VRR_B	VCHL, 1, 0	
00005E70				4491+	DS	0FD	
00005E70		00005E70		4492+	USING	*, R5	base for test data and test routine
00005E70	00005ED8			4493+T100	DC	A(X100)	address of test routine
00005E74	0064			4494+	DC	H' 100'	test number
00005E76	00			4495+	DC	X' 00'	
00005E77	01			4496+	DC	HL1' 1'	m4 used
00005E78	01			4497+	DC	HL1' 1'	m5 used
00005E79	00			4498+	DC	HL1' 0'	CC
00005E7A	07			4499+	DC	HL1' 7'	CC failed mask
00005E7C	00000000 00000000			4500+	DS	2F	extracted PSW after test (has CC)
00005E84	FF			4501+	DC	X' FF'	extracted CC, if test failed
00005E85	E5C3C8D3 40404040			4502+	DC	CL8' VCHL'	instruction name
00005E90	00005F08			4503+	DC	A(RE100)	address of v1 result
00005E94	00005F18			4504+	DC	A(RE100+16)	address of v2 source
00005E98	00005F28			4505+	DC	A(RE100+32)	address of v3 source
00005E9C	00000010			4506+	DC	A(16)	result length
00005EA0	00005F08			4507+REA100	DC	A(RE100)	result address
00005EA8	00000000 00000000			4508+	DS	2FD	gap
00005EB0	00000000 00000000						
00005EB8	00000000 00000000			4509+V10100	DS	XL16	V1 output
00005EC0	00000000 00000000						
00005EC8	00000000 00000000			4510+	DS	2FD	gap
00005ED0	00000000 00000000						
				4511+*			
00005ED8				4512+X100	DS	0F	
00005ED8	E310 5024 0014		00000024	4513+	LGF	R1, V2ADDR	load v2 source
00005EDE	E761 0000 0806		00000000	4514+	VL	v22, 0(R1)	use v21 to test decoder
00005EE4	E310 5028 0014		00000028	4515+	LGF	R1, V3ADDR	load v3 source
00005EEA	E771 0000 0806		00000000	4516+	VL	v23, 0(R1)	use v22 to test decoder
00005EF0	E756 7010 1EF9			4517+	VCHL	V21, V22, V23, 1, 1	test instruction
00005EF6	B98D 0020			4518+	EPSW	R2, R0	extract psw
00005EFA	5020 500C		0000000C	4519+	ST	R2, CCPSW	to save CC
00005EFE	E750 5048 080E		00005EB8	4520+	VST	V21, V10100	save v1 output



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005F04	07FB			4521+	BR	R11	return
00005F08				4522+RE100	DC	0F	V1 for this test
00005F08				4523+	DROP	R5	
00005F08	FFFFFFFF FFFFFFFF			4524	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005F10	FFFFFFFF FFFFFFFF						
00005F18	FFFFFFFF FFFFFFFF			4525	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00005F20	FFFFFFFF FFFFFFFF						
00005F28	00000000 00000000			4526	DC	XL16' 0000000000000000 0000000000000000'	v3
00005F30	00000000 00000000						
				4527			
				4528	VRR_B	VCHL, 1, 1	
00005F38				4529+	DS	0FD	
00005F38		00005F38		4530+	USING	*, R5	base for test data and test routine
00005F38	00005FA0			4531+T101	DC	A(X101)	address of test routine
00005F3C	0065			4532+	DC	H' 101'	test number
00005F3E	00			4533+	DC	X' 00'	
00005F3F	01			4534+	DC	HL1' 1'	m4 used
00005F40	01			4535+	DC	HL1' 1'	m5 used
00005F41	01			4536+	DC	HL1' 1'	CC
00005F42	0B			4537+	DC	HL1' 11'	CC failed mask
00005F44	00000000 00000000			4538+	DS	2F	extracted PSW after test (has CC)
00005F4C	FF			4539+	DC	X' FF'	extracted CC, if test failed
00005F4D	E5C3C8D3 40404040			4540+	DC	CL8' VCHL'	instruction name
00005F58	00005FD0			4541+	DC	A(RE101)	address of v1 result
00005F5C	00005FE0			4542+	DC	A(RE101+16)	address of v2 source
00005F60	00005FF0			4543+	DC	A(RE101+32)	address of v3 source
00005F64	00000010			4544+	DC	A(16)	result length
00005F68	00005FD0			4545+REA101	DC	A(RE101)	result address
00005F70	00000000 00000000			4546+	DS	2FD	gap
00005F78	00000000 00000000						
00005F80	00000000 00000000			4547+V10101	DS	XL16	V1 output
00005F88	00000000 00000000						
00005F90	00000000 00000000			4548+	DS	2FD	gap
00005F98	00000000 00000000						
				4549+*			
00005FA0				4550+X101	DS	0F	
00005FA0	E310 5024 0014		00000024	4551+	LGF	R1, V2ADDR	load v2 source
00005FA6	E761 0000 0806		00000000	4552+	VL	v22, 0(R1)	use v21 to test decoder
00005FAC	E310 5028 0014		00000028	4553+	LGF	R1, V3ADDR	load v3 source
00005FB2	E771 0000 0806		00000000	4554+	VL	v23, 0(R1)	use v22 to test decoder
00005FB8	E756 7010 1EF9			4555+	VCHL	V21, V22, V23, 1, 1	test instruction
00005FBE	B98D 0020			4556+	EPSW	R2, R0	extract psw
00005FC2	5020 500C		0000000C	4557+	ST	R2, CCPSW	to save CC
00005FC6	E750 5048 080E		00005F80	4558+	VST	V21, V10101	save v1 output
00005FCC	07FB			4559+	BR	R11	return
00005FD0				4560+RE101	DC	0F	V1 for this test
00005FD0				4561+	DROP	R5	
00005FD0	00000000 00000000			4562	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result t
00005FD8	FFFFFFFF 00000000						
00005FE0	00000000 00000000			4563	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00005FE8	8FFF8FFF 00000000						
00005FF0	00000000 00000000			4564	DC	XL16' 0000000000000000 0000000000000000'	v2
00005FF8	00000000 00000000						
				4565			
				4566	VRR_B	VCHL, 1, 3	
00006000				4567+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00006000		00006000		4568+	USING *, R5	base for test data and test routine
00006000	00006068			4569+T102	DC A(X102)	address of test routine
00006004	0066			4570+	DC H' 102'	test number
00006006	00			4571+	DC X' 00'	
00006007	01			4572+	DC HL1' 1'	m4 used
00006008	01			4573+	DC HL1' 1'	m5 used
00006009	03			4574+	DC HL1' 3'	CC
0000600A	0E			4575+	DC HL1' 14'	CC failed mask
0000600C	00000000 00000000			4576+	DS 2F	extracted PSW after test (has CC)
00006014	FF			4577+	DC X' FF'	extracted CC, if test failed
00006015	E5C3C8D3 40404040			4578+	DC CL8' VCHL'	instruction name
00006020	00006098			4579+	DC A(RE102)	address of v1 result
00006024	000060A8			4580+	DC A(RE102+16)	address of v2 source
00006028	000060B8			4581+	DC A(RE102+32)	address of v3 source
0000602C	00000010			4582+	DC A(16)	result length
00006030	00006098			4583+REA102	DC A(RE102)	result address
00006038	00000000 00000000			4584+	DS 2FD	gap
00006040	00000000 00000000					
00006048	00000000 00000000			4585+V10102	DS XL16	V1 output
00006050	00000000 00000000					
00006058	00000000 00000000			4586+	DS 2FD	gap
00006060	00000000 00000000					
				4587+*		
00006068				4588+X102	DS 0F	
00006068	E310 5024 0014		00000024	4589+	LGF R1, V2ADDR	load v2 source
0000606E	E761 0000 0806		00000000	4590+	VL v22, 0(R1)	use v21 to test decoder
00006074	E310 5028 0014		00000028	4591+	LGF R1, V3ADDR	load v3 source
0000607A	E771 0000 0806		00000000	4592+	VL v23, 0(R1)	use v22 to test decoder
00006080	E756 7010 1EF9			4593+	VCHL V21, V22, V23, 1, 1	test instruction
00006086	B98D 0020			4594+	EPSW R2, R0	extract psw
0000608A	5020 500C		0000000C	4595+	ST R2, CCPSW	to save CC
0000608E	E750 5048 080E		00006048	4596+	VST V21, V10102	save v1 output
00006094	07FB			4597+	BR R11	return
00006098				4598+RE102	DC 0F	V1 for this test
00006098				4599+	DROP R5	
00006098	00000000 00000000			4600	DC XL16' 0000000000000000 0000000000000000'	result
000060A0	00000000 00000000					
000060A8	00000000 00000000			4601	DC XL16' 0000000000000000 0000000000000000'	v2
000060B0	00000000 00000000					
000060B8	00000000 00000000			4602	DC XL16' 0000000000000000 0000000000000000'	v3
000060C0	00000000 00000000					
				4603		
				4604 *Word		
				4605	VRR_B VCHL, 2, 0	
000060C8				4606+	DS 0FD	
000060C8		000060C8		4607+	USING *, R5	base for test data and test routine
000060C8	00006130			4608+T103	DC A(X103)	address of test routine
000060CC	0067			4609+	DC H' 103'	test number
000060CE	00			4610+	DC X' 00'	
000060CF	02			4611+	DC HL1' 2'	m4 used
000060D0	01			4612+	DC HL1' 1'	m5 used
000060D1	00			4613+	DC HL1' 0'	CC
000060D2	07			4614+	DC HL1' 7'	CC failed mask
000060D4	00000000 00000000			4615+	DS 2F	extracted PSW after test (has CC)
000060DC	FF			4616+	DC X' FF'	extracted CC, if test failed
000060DD	E5C3C8D3 40404040			4617+	DC CL8' VCHL'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000060E8	00006160			4618+	DC	A(RE103)	address of v1 result
000060EC	00006170			4619+	DC	A(RE103+16)	address of v2 source
000060F0	00006180			4620+	DC	A(RE103+32)	address of v3 source
000060F4	00000010			4621+	DC	A(16)	result length
000060F8	00006160			4622+REA103	DC	A(RE103)	result address
00006100	00000000 00000000			4623+	DS	2FD	gap
00006108	00000000 00000000						
00006110	00000000 00000000			4624+V10103	DS	XL16	V1 output
00006118	00000000 00000000						
00006120	00000000 00000000			4625+	DS	2FD	gap
00006128	00000000 00000000						
00006130				4626+*			
00006130	E310 5024 0014		00000024	4627+X103	DS	0F	
00006136	E761 0000 0806		00000000	4628+	LGF	R1, V2ADDR	load v2 source
0000613C	E310 5028 0014		00000028	4629+	VL	v22, 0(R1)	use v21 to test decoder
00006142	E771 0000 0806		00000000	4630+	LGF	R1, V3ADDR	load v3 source
00006148	E756 7010 2EF9			4631+	VL	v23, 0(R1)	use v22 to test decoder
0000614E	B98D 0020			4632+	VCHL	V21, V22, V23, 2, 1	test instruction
00006152	5020 500C		0000000C	4633+	EPSW	R2, R0	extract psw
00006156	E750 5048 080E		00006110	4634+	ST	R2, CCPSW	to save CC
0000615C	07FB			4635+	VST	V21, V10103	save v1 output
00006160				4636+	BR	R11	return
00006160				4637+RE103	DC	0F	V1 for this test
00006160	FFFFFFFF FFFFFFFF			4638+	DROP	R5	
00006168	FFFFFFFF FFFFFFFF			4639	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00006170	FFFFFFFF FFFFFFFF			4640	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00006178	FFFFFFFF FFFFFFFF						
00006180	00000000 00000000			4641	DC	XL16' 0000000000000000 0000000000000000'	v3
00006188	00000000 00000000						
00006190				4642			
00006190		00006190		4643	VRR_B	VCHL, 2, 1	
00006190	000061F8			4644+	DS	0FD	
00006194	0068			4645+	USING	*, R5	base for test data and test routine
00006196	00			4646+T104	DC	A(X104)	address of test routine
00006197	02			4647+	DC	H' 104'	test number
00006198	01			4648+	DC	X' 00'	
00006199	01			4649+	DC	HL1' 2'	m4 used
0000619A	0B			4650+	DC	HL1' 1'	m5 used
0000619C	00000000 00000000			4651+	DC	HL1' 1'	CC
000061A4	FF			4652+	DC	HL1' 11'	CC failed mask
000061A5	E5C3C8D3 40404040			4653+	DS	2F	extracted PSW after test (has CC)
000061B0	00006228			4654+	DC	X' FF'	extracted CC, if test failed
000061B4	00006238			4655+	DC	CL8' VCHL'	instruction name
000061B8	00006248			4656+	DC	A(RE104)	address of v1 result
000061BC	00000010			4657+	DC	A(RE104+16)	address of v2 source
000061C0	00006228			4658+	DC	A(RE104+32)	address of v3 source
000061C8	00000000 00000000			4659+	DC	A(16)	result length
000061D0	00000000 00000000			4660+REA104	DC	A(RE104)	result address
000061D8	00000000 00000000			4661+	DS	2FD	gap
000061E0	00000000 00000000						
000061E8	00000000 00000000			4662+V10104	DS	XL16	V1 output
000061F0	00000000 00000000			4663+	DS	2FD	gap
				4664+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000061F8				4665+X104	DS	0F	
000061F8	E310 5024 0014		00000024	4666+	LGF	R1, V2ADDR	load v2 source
000061FE	E761 0000 0806		00000000	4667+	VL	v22, 0(R1)	use v21 to test decoder
00006204	E310 5028 0014		00000028	4668+	LGF	R1, V3ADDR	load v3 source
0000620A	E771 0000 0806		00000000	4669+	VL	v23, 0(R1)	use v22 to test decoder
00006210	E756 7010 2EF9			4670+	VCHL	V21, V22, V23, 2, 1	test instruction
00006216	B98D 0020			4671+	EPSW	R2, R0	extract psw
0000621A	5020 500C		0000000C	4672+	ST	R2, CCPSW	to save CC
0000621E	E750 5048 080E		000061D8	4673+	VST	V21, V10104	save v1 output
00006224	07FB			4674+	BR	R11	return
00006228				4675+RE104	DC	0F	V1 for this test
00006228				4676+	DROP	R5	
00006228	00000000 00000000			4677	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result
00006230	FFFFFFFF 00000000						
00006238	00000000 00000000			4678	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00006240	8FFF8FFF 00000000						
00006248	00000000 00000000			4679	DC	XL16' 0000000000000000 0000000000000000'	v2
00006250	00000000 00000000						
				4680			
				4681	VRR_B	VCHL, 2, 3	
00006258				4682+	DS	0FD	
00006258		00006258		4683+	USING	*, R5	base for test data and test routine
00006258	000062C0			4684+T105	DC	A(X105)	address of test routine
0000625C	0069			4685+	DC	H' 105'	test number
0000625E	00			4686+	DC	X' 00'	
0000625F	02			4687+	DC	HL1' 2'	m4 used
00006260	01			4688+	DC	HL1' 1'	m5 used
00006261	03			4689+	DC	HL1' 3'	CC
00006262	0E			4690+	DC	HL1' 14'	CC failed mask
00006264	00000000 00000000			4691+	DS	2F	extracted PSW after test (has CC)
0000626C	FF			4692+	DC	X' FF'	extracted CC, if test failed
0000626D	E5C3C8D3 40404040			4693+	DC	CL8' VCHL'	instruction name
00006278	000062F0			4694+	DC	A(RE105)	address of v1 result
0000627C	00006300			4695+	DC	A(RE105+16)	address of v2 source
00006280	00006310			4696+	DC	A(RE105+32)	address of v3 source
00006284	00000010			4697+	DC	A(16)	result length
00006288	000062F0			4698+REA105	DC	A(RE105)	result address
00006290	00000000 00000000			4699+	DS	2FD	gap
00006298	00000000 00000000						
000062A0	00000000 00000000			4700+V10105	DS	XL16	V1 output
000062A8	00000000 00000000						
000062B0	00000000 00000000			4701+	DS	2FD	gap
000062B8	00000000 00000000						
				4702+*			
000062C0				4703+X105	DS	0F	
000062C0	E310 5024 0014		00000024	4704+	LGF	R1, V2ADDR	load v2 source
000062C6	E761 0000 0806		00000000	4705+	VL	v22, 0(R1)	use v21 to test decoder
000062CC	E310 5028 0014		00000028	4706+	LGF	R1, V3ADDR	load v3 source
000062D2	E771 0000 0806		00000000	4707+	VL	v23, 0(R1)	use v22 to test decoder
000062D8	E756 7010 2EF9			4708+	VCHL	V21, V22, V23, 2, 1	test instruction
000062DE	B98D 0020			4709+	EPSW	R2, R0	extract psw
000062E2	5020 500C		0000000C	4710+	ST	R2, CCPSW	to save CC
000062E6	E750 5048 080E		000062A0	4711+	VST	V21, V10105	save v1 output
000062EC	07FB			4712+	BR	R11	return
000062F0				4713+RE105	DC	0F	V1 for this test
000062F0				4714+	DROP	R5	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000062F0	00000000 00000000			4715	DC	XL16' 0000000000000000 0000000000000000'	result
000062F8	00000000 00000000						
00006300	00000000 00000000			4716	DC	XL16' 0000000000000000 0000000000000000'	v2
00006308	00000000 00000000						
00006310	00000000 00000000			4717	DC	XL16' 0000000000000000 0000000000000000'	v3
00006318	00000000 00000000						
				4718			
				4719	*Doubleword		
				4720	VRR_B	VCHL, 3, 0	
00006320				4721+	DS	0FD	
00006320		00006320		4722+	USING	*, R5	base for test data and test routine
00006320	00006388			4723+T106	DC	A(X106)	address of test routine
00006324	006A			4724+	DC	H' 106'	test number
00006326	00			4725+	DC	X' 00'	
00006327	03			4726+	DC	HL1' 3'	m4 used
00006328	01			4727+	DC	HL1' 1'	m5 used
00006329	00			4728+	DC	HL1' 0'	CC
0000632A	07			4729+	DC	HL1' 7'	CC failed mask
0000632C	00000000 00000000			4730+	DS	2F	extracted PSW after test (has CC)
00006334	FF			4731+	DC	X' FF'	extracted CC, if test failed
00006335	E5C3C8D3 40404040			4732+	DC	CL8' VCHL'	instruction name
00006340	000063B8			4733+	DC	A(RE106)	address of v1 result
00006344	000063C8			4734+	DC	A(RE106+16)	address of v2 source
00006348	000063D8			4735+	DC	A(RE106+32)	address of v3 source
0000634C	00000010			4736+	DC	A(16)	result length
00006350	000063B8			4737+REA106	DC	A(RE106)	result address
00006358	00000000 00000000			4738+	DS	2FD	gap
00006360	00000000 00000000						
00006368	00000000 00000000			4739+V10106	DS	XL16	V1 output
00006370	00000000 00000000						
00006378	00000000 00000000			4740+	DS	2FD	gap
00006380	00000000 00000000						
				4741+*			
00006388				4742+X106	DS	0F	
00006388	E310 5024 0014		00000024	4743+	LGF	R1, V2ADDR	load v2 source
0000638E	E761 0000 0806		00000000	4744+	VL	v22, 0(R1)	use v21 to test decoder
00006394	E310 5028 0014		00000028	4745+	LGF	R1, V3ADDR	load v3 source
0000639A	E771 0000 0806		00000000	4746+	VL	v23, 0(R1)	use v22 to test decoder
000063A0	E756 7010 3EF9			4747+	VCHL	V21, V22, V23, 3, 1	test instruction
000063A6	B98D 0020			4748+	EPSW	R2, R0	extract psw
000063AA	5020 500C		0000000C	4749+	ST	R2, CCPSW	to save CC
000063AE	E750 5048 080E		00006368	4750+	VST	V21, V10106	save v1 output
000063B4	07FB			4751+	BR	R11	return
000063B8				4752+RE106	DC	0F	V1 for this test
000063B8				4753+	DROP	R5	
000063B8	FFFFFFFF FFFFFFFF			4754	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000063C0	FFFFFFFF FFFFFFFF						
000063C8	FFFFFFFF FFFFFFFF			4755	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
000063D0	FFFFFFFF FFFFFFFF						
000063D8	00000000 00000000			4756	DC	XL16' 0000000000000000 0000000000000000'	v3
000063E0	00000000 00000000						
				4757			
				4758	VRR_B	VCHL, 3, 1	
000063E8				4759+	DS	0FD	
000063E8		000063E8		4760+	USING	*, R5	base for test data and test routine
000063E8	00006450			4761+T107	DC	A(X107)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000063EC	006B			4762+	DC	H' 107'	test number
000063EE	00			4763+	DC	X' 00'	
000063EF	03			4764+	DC	HL1' 3'	m4 used
000063F0	01			4765+	DC	HL1' 1'	m5 used
000063F1	01			4766+	DC	HL1' 1'	CC
000063F2	0B			4767+	DC	HL1' 11'	CC failed mask
000063F4	00000000 00000000			4768+	DS	2F	extracted PSW after test (has CC)
000063FC	FF			4769+	DC	X' FF'	extracted CC, if test failed
000063FD	E5C3C8D3 40404040			4770+	DC	CL8' VCHL'	instruction name
00006408	00006480			4771+	DC	A(RE107)	address of v1 result
0000640C	00006490			4772+	DC	A(RE107+16)	address of v2 source
00006410	000064A0			4773+	DC	A(RE107+32)	address of v3 source
00006414	00000010			4774+	DC	A(16)	result length
00006418	00006480			4775+REA107	DC	A(RE107)	result address
00006420	00000000 00000000			4776+	DS	2FD	gap
00006428	00000000 00000000						
00006430	00000000 00000000			4777+V10107	DS	XL16	V1 output
00006438	00000000 00000000						
00006440	00000000 00000000			4778+	DS	2FD	gap
00006448	00000000 00000000						
00006450				4779+*			
00006450	E310 5024 0014		00000024	4780+X107	DS	0F	
00006456	E761 0000 0806		00000000	4781+	LGF	R1, V2ADDR	load v2 source
0000645C	E310 5028 0014		00000028	4782+	VL	v22, 0(R1)	use v21 to test decoder
00006462	E771 0000 0806		00000000	4783+	LGF	R1, V3ADDR	load v3 source
00006468	E756 7010 3EF9		00000000	4784+	VL	v23, 0(R1)	use v22 to test decoder
0000646E	B98D 0020			4785+	VCHL	V21, V22, V23, 3, 1	test instruction
00006472	5020 500C		0000000C	4786+	EPSW	R2, R0	extract psw
00006476	E750 5048 080E		00006430	4787+	ST	R2, CCPSW	to save CC
0000647C	07FB			4788+	VST	V21, V10107	save v1 output
00006480				4789+	BR	R11	return
00006480				4790+RE107	DC	0F	V1 for this test
00006480				4791+	DROP	R5	
00006480	00000000 00000000			4792	DC	XL16' 0000000000000000 0000000000000000	result t
00006488	FFFFFFFF FFFFFFFF						
00006490	00000000 00000000			4793	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00006498	8FFF8FFF 00000000						
000064A0	00000000 00000000			4794	DC	XL16' 0000000000000000 0000000000000000'	v2
000064A8	00000000 00000000						
000064B0				4795			
000064B0				4796	VRR_B	VCHL, 3, 3	
000064B0		000064B0		4797+	DS	0FD	
000064B0	00006518			4798+	USING	*, R5	base for test data and test routine
000064B4	006C			4799+T108	DC	A(X108)	address of test routine
000064B6	00			4800+	DC	H' 108'	test number
000064B8	00			4801+	DC	X' 00'	
000064B7	03			4802+	DC	HL1' 3'	m4 used
000064B8	01			4803+	DC	HL1' 1'	m5 used
000064B9	03			4804+	DC	HL1' 3'	CC
000064BA	0E			4805+	DC	HL1' 14'	CC failed mask
000064BC	00000000 00000000			4806+	DS	2F	extracted PSW after test (has CC)
000064C4	FF			4807+	DC	X' FF'	extracted CC, if test failed
000064C5	E5C3C8D3 40404040			4808+	DC	CL8' VCHL'	instruction name
000064D0	00006548			4809+	DC	A(RE108)	address of v1 result
000064D4	00006558			4810+	DC	A(RE108+16)	address of v2 source
000064D8	00006568			4811+	DC	A(RE108+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000064DC	00000010			4812+	DC	A(16)	result length
000064E0	00006548			4813+REA108	DC	A(RE108)	result address
000064E8	00000000 00000000			4814+	DS	2FD	gap
000064F0	00000000 00000000						
000064F8	00000000 00000000			4815+V10108	DS	XL16	V1 output
00006500	00000000 00000000						
00006508	00000000 00000000			4816+	DS	2FD	gap
00006510	00000000 00000000						
				4817+*			
00006518				4818+X108	DS	0F	
00006518	E310 5024 0014		00000024	4819+	LGF	R1, V2ADDR	load v2 source
0000651E	E761 0000 0806		00000000	4820+	VL	v22, 0(R1)	use v21 to test decoder
00006524	E310 5028 0014		00000028	4821+	LGF	R1, V3ADDR	load v3 source
0000652A	E771 0000 0806		00000000	4822+	VL	v23, 0(R1)	use v22 to test decoder
00006530	E756 7010 3EF9			4823+	VCHL	V21, V22, V23, 3, 1	test instruction
00006536	B98D 0020			4824+	EPSW	R2, R0	extract psw
0000653A	5020 500C		0000000C	4825+	ST	R2, CCPSW	to save CC
0000653E	E750 5048 080E		000064F8	4826+	VST	V21, V10108	save v1 output
00006544	07FB			4827+	BR	R11	return
00006548				4828+RE108	DC	0F	V1 for this test
00006548				4829+	DROP	R5	
00006548	00000000 00000000			4830	DC	XL16' 0000000000000000 0000000000000000'	result
00006550	00000000 00000000						
00006558	00000000 00000000			4831	DC	XL16' 0000000000000000 0000000000000000'	v2
00006560	00000000 00000000						
00006568	00000000 00000000			4832	DC	XL16' 0000000000000000 0000000000000000'	v3
00006570	00000000 00000000						
				4833			
				4834 *			
				4835 * case - general			
				4836 *			
				4837 *Byte			
				4838	VRR_B	VCHL, 0, 0	
00006578				4839+	DS	0FD	
00006578		00006578		4840+	USING	*, R5	base for test data and test routine
00006578	000065E0			4841+T109	DC	A(X109)	address of test routine
0000657C	006D			4842+	DC	H' 109'	test number
0000657E	00			4843+	DC	X' 00'	
0000657F	00			4844+	DC	HL1' 0'	m4 used
00006580	01			4845+	DC	HL1' 1'	m5 used
00006581	00			4846+	DC	HL1' 0'	CC
00006582	07			4847+	DC	HL1' 7'	CC failed mask
00006584	00000000 00000000			4848+	DS	2F	extracted PSW after test (has CC)
0000658C	FF			4849+	DC	X' FF'	extracted CC, if test failed
0000658D	E5C3C8D3 40404040			4850+	DC	CL8' VCHL'	instruction name
00006598	00006610			4851+	DC	A(RE109)	address of v1 result
0000659C	00006620			4852+	DC	A(RE109+16)	address of v2 source
000065A0	00006630			4853+	DC	A(RE109+32)	address of v3 source
000065A4	00000010			4854+	DC	A(16)	result length
000065A8	00006610			4855+REA109	DC	A(RE109)	result address
000065B0	00000000 00000000			4856+	DS	2FD	gap
000065B8	00000000 00000000						
000065C0	00000000 00000000			4857+V10109	DS	XL16	V1 output
000065C8	00000000 00000000						
000065D0	00000000 00000000			4858+	DS	2FD	gap
000065D8	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				4859+*			
000065E0				4860+X109	DS	0F	
000065E0	E310 5024 0014		00000024	4861+	LGF	R1, V2ADDR	load v2 source
000065E6	E761 0000 0806		00000000	4862+	VL	v22, 0(R1)	use v21 to test decoder
000065EC	E310 5028 0014		00000028	4863+	LGF	R1, V3ADDR	load v3 source
000065F2	E771 0000 0806		00000000	4864+	VL	v23, 0(R1)	use v22 to test decoder
000065F8	E756 7010 0EF9			4865+	VCHL	V21, V22, V23, 0, 1	test instruction
000065FE	B98D 0020			4866+	EPSW	R2, R0	extract psw
00006602	5020 500C		0000000C	4867+	ST	R2, CCPSW	to save CC
00006606	E750 5048 080E		000065C0	4868+	VST	V21, V10109	save v1 output
0000660C	07FB			4869+	BR	R11	return
00006610				4870+RE109	DC	0F	V1 for this test
00006610				4871+	DROP	R5	
00006610	FFFFFFFF FFFFFFFF			4872	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00006618	FFFFFFFF FFFFFFFF						
00006620	01020304 05060708			4873	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
00006628	090A0B0C 0D0E0F10						
00006630	00010203 04050607			4874	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00006638	08090A0B 0C0D0E0F						
				4875			
00006640				4876	VRR_B	VCHL, 0, 0	
00006640		00006640		4877+	DS	0FD	
00006640	000066A8			4878+	USING	*, R5	base for test data and test routine
00006644	006E			4879+T110	DC	A(X110)	address of test routine
00006646	00			4880+	DC	H' 110'	test number
00006647	00			4881+	DC	X' 00'	
00006647	00			4882+	DC	HL1' 0'	m4 used
00006648	01			4883+	DC	HL1' 1'	m5 used
00006649	00			4884+	DC	HL1' 0'	CC
0000664A	07			4885+	DC	HL1' 7'	CC failed mask
0000664C	00000000 00000000			4886+	DS	2F	extracted PSW after test (has CC)
00006654	FF			4887+	DC	X' FF'	extracted CC, if test failed
00006655	E5C3C8D3 40404040			4888+	DC	CL8' VCHL'	instruction name
00006660	000066D8			4889+	DC	A(RE110)	address of v1 result
00006664	000066E8			4890+	DC	A(RE110+16)	address of v2 source
00006668	000066F8			4891+	DC	A(RE110+32)	address of v3 source
0000666C	00000010			4892+	DC	A(16)	result length
00006670	000066D8			4893+REA110	DC	A(RE110)	result address
00006678	00000000 00000000			4894+	DS	2FD	gap
00006680	00000000 00000000						
00006688	00000000 00000000			4895+V10110	DS	XL16	V1 output
00006690	00000000 00000000						
00006698	00000000 00000000			4896+	DS	2FD	gap
000066A0	00000000 00000000						
				4897+*			
000066A8				4898+X110	DS	0F	
000066A8	E310 5024 0014		00000024	4899+	LGF	R1, V2ADDR	load v2 source
000066AE	E761 0000 0806		00000000	4900+	VL	v22, 0(R1)	use v21 to test decoder
000066B4	E310 5028 0014		00000028	4901+	LGF	R1, V3ADDR	load v3 source
000066BA	E771 0000 0806		00000000	4902+	VL	v23, 0(R1)	use v22 to test decoder
000066C0	E756 7010 0EF9			4903+	VCHL	V21, V22, V23, 0, 1	test instruction
000066C6	B98D 0020			4904+	EPSW	R2, R0	extract psw
000066CA	5020 500C		0000000C	4905+	ST	R2, CCPSW	to save CC
000066CE	E750 5048 080E		00006688	4906+	VST	V21, V10110	save v1 output
000066D4	07FB			4907+	BR	R11	return
000066D8				4908+RE110	DC	0F	V1 for this test



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000066D8				4909+	DROP	R5	
000066D8	FFFFFFFF FFFFFFFF			4910	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000066E0	FFFFFFFF FFFFFFFF						
000066E8	FFFEFFFD FFFCFFFB			4911	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
000066F0	FFFAFFF9 FFF8FFF7						
000066F8	00010203 04050607			4912	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00006700	08090A0B 0C0D0E0F						
				4913			
				4914	VRR_B	VCHL, 0, 1	
00006708				4915+	DS	0FD	
00006708		00006708		4916+	USING	*, R5	base for test data and test routine
00006708	00006770			4917+T111	DC	A(X111)	address of test routine
0000670C	006F			4918+	DC	H' 111'	test number
0000670E	00			4919+	DC	X' 00'	
0000670F	00			4920+	DC	HL1' 0'	m4 used
00006710	01			4921+	DC	HL1' 1'	m5 used
00006711	01			4922+	DC	HL1' 1'	CC
00006712	0B			4923+	DC	HL1' 11'	CC failed mask
00006714	00000000 00000000			4924+	DS	2F	extracted PSW after test (has CC)
0000671C	FF			4925+	DC	X' FF'	extracted CC, if test failed
0000671D	E5C3C8D3 40404040			4926+	DC	CL8' VCHL'	instruction name
00006728	000067A0			4927+	DC	A(RE111)	address of v1 result
0000672C	000067B0			4928+	DC	A(RE111+16)	address of v2 source
00006730	000067C0			4929+	DC	A(RE111+32)	address of v3 source
00006734	00000010			4930+	DC	A(16)	result length
00006738	000067A0			4931+REA111	DC	A(RE111)	result address
00006740	00000000 00000000			4932+	DS	2FD	gap
00006748	00000000 00000000						
00006750	00000000 00000000			4933+V10111	DS	XL16	V1 output
00006758	00000000 00000000						
00006760	00000000 00000000			4934+	DS	2FD	gap
00006768	00000000 00000000						
				4935+*			
00006770				4936+X111	DS	0F	
00006770	E310 5024 0014		00000024	4937+	LGF	R1, V2ADDR	load v2 source
00006776	E761 0000 0806		00000000	4938+	VL	v22, 0(R1)	use v21 to test decoder
0000677C	E310 5028 0014		00000028	4939+	LGF	R1, V3ADDR	load v3 source
00006782	E771 0000 0806		00000000	4940+	VL	v23, 0(R1)	use v22 to test decoder
00006788	E756 7010 0EF9			4941+	VCHL	V21, V22, V23, 0, 1	test instruction
0000678E	B98D 0020			4942+	EPSW	R2, R0	extract psw
00006792	5020 500C		0000000C	4943+	ST	R2, CCPSW	to save CC
00006796	E750 5048 080E		00006750	4944+	VST	V21, V10111	save v1 output
0000679C	07FB			4945+	BR	R11	return
000067A0				4946+RE111	DC	0F	V1 for this test
000067A0				4947+	DROP	R5	
000067A0	00FF00FF 00FF00FF			4948	DC	XL16' 00FF00FF00FF00FF 00000000000000FF'	result
000067A8	00000000 000000FF						
000067B0	00110033 00550077			4949	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'	v2
000067B8	08090A0B 0C0DFE1F						
000067C0	00010203 04050607			4950	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v3
000067C8	08090A0B 0C0DFE0F						
				4951			
				4952	VRR_B	VCHL, 0, 1	
000067D0				4953+	DS	0FD	
000067D0		000067D0		4954+	USING	*, R5	base for test data and test routine
000067D0	00006838			4955+T112	DC	A(X112)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000067D4	0070			4956+	DC	H' 112'	test number
000067D6	00			4957+	DC	X' 00'	
000067D7	00			4958+	DC	HL1' 0'	m4 used
000067D8	01			4959+	DC	HL1' 1'	m5 used
000067D9	01			4960+	DC	HL1' 1'	CC
000067DA	0B			4961+	DC	HL1' 11'	CC failed mask
000067DC	00000000 00000000			4962+	DS	2F	extracted PSW after test (has CC)
000067E4	FF			4963+	DC	X' FF'	extracted CC, if test failed
000067E5	E5C3C8D3 40404040			4964+	DC	CL8' VCHL'	instruction name
000067F0	00006868			4965+	DC	A(RE112)	address of v1 result
000067F4	00006878			4966+	DC	A(RE112+16)	address of v2 source
000067F8	00006888			4967+	DC	A(RE112+32)	address of v3 source
000067FC	00000010			4968+	DC	A(16)	result length
00006800	00006868			4969+REA112	DC	A(RE112)	result address
00006808	00000000 00000000			4970+	DS	2FD	gap
00006810	00000000 00000000						
00006818	00000000 00000000			4971+V10112	DS	XL16	V1 output
00006820	00000000 00000000						
00006828	00000000 00000000			4972+	DS	2FD	gap
00006830	00000000 00000000						
				4973+*			
00006838				4974+X112	DS	0F	
00006838	E310 5024 0014		00000024	4975+	LGF	R1, V2ADDR	load v2 source
0000683E	E761 0000 0806		00000000	4976+	VL	v22, 0(R1)	use v21 to test decoder
00006844	E310 5028 0014		00000028	4977+	LGF	R1, V3ADDR	load v3 source
0000684A	E771 0000 0806		00000000	4978+	VL	v23, 0(R1)	use v22 to test decoder
00006850	E756 7010 0EF9			4979+	VCHL	V21, V22, V23, 0, 1	test instruction
00006856	B98D 0020			4980+	EPSW	R2, R0	extract psw
0000685A	5020 500C		0000000C	4981+	ST	R2, CCPSW	to save CC
0000685E	E750 5048 080E		00006818	4982+	VST	V21, V10112	save v1 output
00006864	07FB			4983+	BR	R11	return
00006868				4984+RE112	DC	0F	V1 for this test
00006868				4985+	DROP	R5	
00006868	00000000 000000FF			4986	DC	XL16' 00000000000000FF 00FF00FF00FF00FF'	result t
00006870	00FF00FF 00FF00FF						
00006878	08090A0B 0C0DFE1F			4987	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
00006880	00110033 00550077						
00006888	08090A0B 0C0DFE0F			4988	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v3
00006890	00010203 04050607						
				4989			
00006898				4990	VRR_B	VCHL, 0, 3	
00006898		00006898		4991+	DS	0FD	
00006898	00006900			4992+	USING	*, R5	base for test data and test routine
0000689C	0071			4993+T113	DC	A(X113)	address of test routine
0000689E	00			4994+	DC	H' 113'	test number
0000689F	00			4995+	DC	X' 00'	
000068A0	01			4996+	DC	HL1' 0'	m4 used
000068A1	03			4997+	DC	HL1' 1'	m5 used
000068A2	0E			4998+	DC	HL1' 3'	CC
000068A4	00000000 00000000			4999+	DC	HL1' 14'	CC failed mask
000068AC	FF			5000+	DS	2F	extracted PSW after test (has CC)
000068AD	E5C3C8D3 40404040			5001+	DC	X' FF'	extracted CC, if test failed
000068B8	00006930			5002+	DC	CL8' VCHL'	instruction name
000068BC	00006940			5003+	DC	A(RE113)	address of v1 result
000068C0	00006950			5004+	DC	A(RE113+16)	address of v2 source
				5005+	DC	A(RE113+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000068C4	00000010			5006+	DC	A(16)	result length
000068C8	00006930			5007+REA113	DC	A(RE113)	result address
000068D0	00000000 00000000			5008+	DS	2FD	gap
000068D8	00000000 00000000						
000068E0	00000000 00000000			5009+V10113	DS	XL16	V1 output
000068E8	00000000 00000000						
000068F0	00000000 00000000			5010+	DS	2FD	gap
000068F8	00000000 00000000						
				5011+*			
00006900				5012+X113	DS	0F	
00006900	E310 5024 0014		00000024	5013+	LGF	R1, V2ADDR	load v2 source
00006906	E761 0000 0806		00000000	5014+	VL	v22, 0(R1)	use v21 to test decoder
0000690C	E310 5028 0014		00000028	5015+	LGF	R1, V3ADDR	load v3 source
00006912	E771 0000 0806		00000000	5016+	VL	v23, 0(R1)	use v22 to test decoder
00006918	E756 7010 0EF9			5017+	VCHL	V21, V22, V23, 0, 1	test instruction
0000691E	B98D 0020			5018+	EPSW	R2, R0	extract psw
00006922	5020 500C		0000000C	5019+	ST	R2, CCPSW	to save CC
00006926	E750 5048 080E		000068E0	5020+	VST	V21, V10113	save v1 output
0000692C	07FB			5021+	BR	R11	return
00006930				5022+RE113	DC	0F	V1 for this test
00006930				5023+	DROP	R5	
00006930	00000000 00000000			5024	DC	XL16' 0000000000000000 0000000000000000'	result
00006938	00000000 00000000						
00006940	00010003 04050607			5025	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00006948	00090A0B 0C0D0E0F						
00006950	01110233 11550677			5026	DC	XL16' 0111023311550677 119911BBF1DD11FF'	v3
00006958	119911BB F1DD11FF						
				5027			
				5028	VRR_B	VCHL, 0, 3	
00006960				5029+	DS	0FD	
00006960		00006960		5030+	USING	*, R5	base for test data and test routine
00006960	000069C8			5031+T114	DC	A(X114)	address of test routine
00006964	0072			5032+	DC	H' 114'	test number
00006966	00			5033+	DC	X' 00'	
00006967	00			5034+	DC	HL1' 0'	m4 used
00006968	01			5035+	DC	HL1' 1'	m5 used
00006969	03			5036+	DC	HL1' 3'	CC
0000696A	0E			5037+	DC	HL1' 14'	CC failed mask
0000696C	00000000 00000000			5038+	DS	2F	extracted PSW after test (has CC)
00006974	FF			5039+	DC	X' FF'	extracted CC, if test failed
00006975	E5C3C8D3 40404040			5040+	DC	CL8' VCHL'	instruction name
00006980	000069F8			5041+	DC	A(RE114)	address of v1 result
00006984	00006A08			5042+	DC	A(RE114+16)	address of v2 source
00006988	00006A18			5043+	DC	A(RE114+32)	address of v3 source
0000698C	00000010			5044+	DC	A(16)	result length
00006990	000069F8			5045+REA114	DC	A(RE114)	result address
00006998	00000000 00000000			5046+	DS	2FD	gap
000069A0	00000000 00000000						
000069A8	00000000 00000000			5047+V10114	DS	XL16	V1 output
000069B0	00000000 00000000						
000069B8	00000000 00000000			5048+	DS	2FD	gap
000069C0	00000000 00000000						
				5049+*			
000069C8				5050+X114	DS	0F	
000069C8	E310 5024 0014		00000024	5051+	LGF	R1, V2ADDR	load v2 source
000069CE	E761 0000 0806		00000000	5052+	VL	v22, 0(R1)	use v21 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000069D4	E310 5028 0014		00000028	5053+	LGF	R1, V3ADDR	load v3 source
000069DA	E771 0000 0806		00000000	5054+	VL	v23, 0(R1)	use v22 to test decoder
000069E0	E756 7010 0EF9			5055+	VCHL	V21, V22, V23, 0, 1	test instruction
000069E6	B98D 0020			5056+	EPSW	R2, R0	extract psw
000069EA	5020 500C		0000000C	5057+	ST	R2, CCPSW	to save CC
000069EE	E750 5048 080E		000069A8	5058+	VST	V21, V10114	save v1 output
000069F4	07FB			5059+	BR	R11	return
000069F8				5060+RE114	DC	0F	V1 for this test
000069F8				5061+	DROP	R5	
000069F8	00000000 00000000			5062	DC	XL16' 0000000000000000 0000000000000000'	result t
00006A00	00000000 00000000						
00006A08	08090A0B 0C0D0E0F			5063	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00006A10	00010203 04050607						
00006A18	119911BB F1DD11FF			5064	DC	XL16' 119911BBF1DD11FF 0111023311550677'	v3
00006A20	01110233 11550677						
				5065			
				5066 *Halfword			
				5067	VRR_B	VCHL, 1, 0	
00006A28				5068+	DS	0FD	
00006A28		00006A28		5069+	USING	*, R5	base for test data and test routine
00006A28	00006A90			5070+T115	DC	A(X115)	address of test routine
00006A2C	0073			5071+	DC	H' 115'	test number
00006A2E	00			5072+	DC	X' 00'	
00006A2F	01			5073+	DC	HL1' 1'	m4 used
00006A30	01			5074+	DC	HL1' 1'	m5 used
00006A31	00			5075+	DC	HL1' 0'	CC
00006A32	07			5076+	DC	HL1' 7'	CC failed mask
00006A34	00000000 00000000			5077+	DS	2F	extracted PSW after test (has CC)
00006A3C	FF			5078+	DC	X' FF'	extracted CC, if test failed
00006A3D	E5C3C8D3 40404040			5079+	DC	CL8' VCHL'	instruction name
00006A48	00006AC0			5080+	DC	A(RE115)	address of v1 result
00006A4C	00006AD0			5081+	DC	A(RE115+16)	address of v2 source
00006A50	00006AE0			5082+	DC	A(RE115+32)	address of v3 source
00006A54	00000010			5083+	DC	A(16)	result length
00006A58	00006AC0			5084+REA115	DC	A(RE115)	result address
00006A60	00000000 00000000			5085+	DS	2FD	gap
00006A68	00000000 00000000						
00006A70	00000000 00000000			5086+V10115	DS	XL16	V1 output
00006A78	00000000 00000000						
00006A80	00000000 00000000			5087+	DS	2FD	gap
00006A88	00000000 00000000						
				5088+*			
00006A90				5089+X115	DS	0F	
00006A90	E310 5024 0014		00000024	5090+	LGF	R1, V2ADDR	load v2 source
00006A96	E761 0000 0806		00000000	5091+	VL	v22, 0(R1)	use v21 to test decoder
00006A9C	E310 5028 0014		00000028	5092+	LGF	R1, V3ADDR	load v3 source
00006AA2	E771 0000 0806		00000000	5093+	VL	v23, 0(R1)	use v22 to test decoder
00006AA8	E756 7010 1EF9			5094+	VCHL	V21, V22, V23, 1, 1	test instruction
00006AAE	B98D 0020			5095+	EPSW	R2, R0	extract psw
00006AB2	5020 500C		0000000C	5096+	ST	R2, CCPSW	to save CC
00006AB6	E750 5048 080E		00006A70	5097+	VST	V21, V10115	save v1 output
00006ABC	07FB			5098+	BR	R11	return
00006AC0				5099+RE115	DC	0F	V1 for this test
00006AC0				5100+	DROP	R5	
00006AC0	FFFFFFFF FFFFFFFF			5101	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00006AC8	FFFFFFFF FFFFFFFF						



LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00006AD0	01020304 05060708			5102	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2	
00006AD8	090A0B0C 0D0E0F10							
00006AE0	00010203 04050607			5103	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3	
00006AE8	08090A0B 0C0D0E0F							
				5104				
00006AF0				5105	VRR_B	VCHL, 1, 0		
00006AF0		00006AF0		5106+	DS	0FD		
00006AF0	00006B58			5107+	USING	*, R5	base for test data and test routine	
00006AF4	0074			5108+T116	DC	A(X116)	address of test routine	
00006AF6	00			5109+	DC	H' 116'	test number	
00006AF7	01			5110+	DC	X' 00'		
00006AF8	01			5111+	DC	HL1' 1'	m4 used	
00006AF8	01			5112+	DC	HL1' 1'	m5 used	
00006AF9	00			5113+	DC	HL1' 0'	CC	
00006AFA	07			5114+	DC	HL1' 7'	CC failed mask	
00006AFC	00000000 00000000			5115+	DS	2F	extracted PSW after test (has CC)	
00006B04	FF			5116+	DC	X' FF'	extracted CC, if test failed	
00006B05	E5C3C8D3 40404040			5117+	DC	CL8' VCHL'	instruction name	
00006B10	00006B88			5118+	DC	A(RE116)	address of v1 result	
00006B14	00006B98			5119+	DC	A(RE116+16)	address of v2 source	
00006B18	00006BA8			5120+	DC	A(RE116+32)	address of v3 source	
00006B1C	00000010			5121+	DC	A(16)	result length	
00006B20	00006B88			5122+REA116	DC	A(RE116)	result address	
00006B28	00000000 00000000			5123+	DS	2FD	gap	
00006B30	00000000 00000000							
00006B38	00000000 00000000			5124+V10116	DS	XL16	V1 output	
00006B40	00000000 00000000							
00006B48	00000000 00000000			5125+	DS	2FD	gap	
00006B50	00000000 00000000							
				5126+*				
00006B58				5127+X116	DS	0F		
00006B58	E310 5024 0014		00000024	5128+	LGF	R1, V2ADDR	load v2 source	
00006B5E	E761 0000 0806		00000000	5129+	VL	v22, 0(R1)	use v21 to test decoder	
00006B64	E310 5028 0014		00000028	5130+	LGF	R1, V3ADDR	load v3 source	
00006B6A	E771 0000 0806		00000000	5131+	VL	v23, 0(R1)	use v22 to test decoder	
00006B70	E756 7010 1EF9			5132+	VCHL	V21, V22, V23, 1, 1	test instruction	
00006B76	B98D 0020			5133+	EPSW	R2, R0	extract psw	
00006B7A	5020 500C		0000000C	5134+	ST	R2, CCPSW	to save CC	
00006B7E	E750 5048 080E		00006B38	5135+	VST	V21, V10116	save v1 output	
00006B84	07FB			5136+	BR	R11	return	
00006B88				5137+RE116	DC	0F	V1 for this test	
00006B88				5138+	DROP	R5		
00006B88	FFFFFFFF FFFFFFFF			5139	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00006B90	FFFFFFFF FFFFFFFF							
00006B98	FFFEFFFD FFFCFFFB			5140	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2	
00006BA0	FFFAFFF9 FFF8FFF7							
00006BA8	00010203 04050607			5141	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3	
00006BB0	08090A0B 0C0D0E0F							
				5142				
00006BB8				5143	VRR_B	VCHL, 1, 1		
00006BB8		00006BB8		5144+	DS	0FD		
00006BB8	00006C20			5145+	USING	*, R5	base for test data and test routine	
00006BBC	0075			5146+T117	DC	A(X117)	address of test routine	
00006BBE	00			5147+	DC	H' 117'	test number	
00006BBE	00			5148+	DC	X' 00'		
00006BBF	01			5149+	DC	HL1' 1'	m4 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006BC0	01			5150+	DC	HL1' 1'	m5 used
00006BC1	01			5151+	DC	HL1' 1'	CC
00006BC2	0B			5152+	DC	HL1' 11'	CC failed mask
00006BC4	00000000	00000000		5153+	DS	2F	extracted PSW after test (has CC)
00006BCC	FF			5154+	DC	X' FF'	extracted CC, if test failed
00006BCD	E5C3C8D3	40404040		5155+	DC	CL8' VCHL'	instruction name
00006BD8	00006C50			5156+	DC	A(RE117)	address of v1 result
00006BDC	00006C60			5157+	DC	A(RE117+16)	address of v2 source
00006BE0	00006C70			5158+	DC	A(RE117+32)	address of v3 source
00006BE4	00000010			5159+	DC	A(16)	result length
00006BE8	00006C50			5160+REA117	DC	A(RE117)	result address
00006BF0	00000000	00000000		5161+	DS	2FD	gap
00006BF8	00000000	00000000					
00006C00	00000000	00000000		5162+V10117	DS	XL16	V1 output
00006C08	00000000	00000000					
00006C10	00000000	00000000		5163+	DS	2FD	gap
00006C18	00000000	00000000					
00006C20				5164+*			
00006C20	E310 5024 0014		00000024	5165+X117	DS	0F	
00006C26	E761 0000 0806		00000000	5166+	LGF	R1, V2ADDR	load v2 source
00006C2C	E310 5028 0014		00000028	5167+	VL	v22, 0(R1)	use v21 to test decoder
00006C32	E771 0000 0806		00000000	5168+	LGF	R1, V3ADDR	load v3 source
00006C38	E756 7010 1EF9			5169+	VL	v23, 0(R1)	use v22 to test decoder
00006C3E	B98D 0020			5170+	VCHL	V21, V22, V23, 1, 1	test instruction
00006C42	5020 500C		0000000C	5171+	EPSW	R2, R0	extract psw
00006C46	E750 5048 080E		00006C00	5172+	ST	R2, CCPSW	to save CC
00006C4C	07FB			5173+	VST	V21, V10117	save v1 output
00006C50				5174+	BR	R11	return
00006C50				5175+RE117	DC	0F	V1 for this test
00006C50				5176+	DROP	R5	
00006C50	FFFFFFFF	FFFFFFFF		5177	DC	XL16' FFFFFFFFFFFFFFFFFF 000000000000FFFF'	result
00006C58	00000000	0000FFFF					
00006C60	00110033	00550077		5178	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'	v2
00006C68	08090A0B	0C0DFE1F					
00006C70	00010023	00450067		5179	DC	XL16' 0001002300450067 08090A0B0C0DFE0F'	v3
00006C78	08090A0B	0C0DFE0F					
00006C80				5180			
00006C80				5181	VRR_B	VCHL, 1, 1	
00006C80		00006C80		5182+	DS	0FD	
00006C80	00006CE8			5183+	USING	*, R5	base for test data and test routine
00006C84	0076			5184+T118	DC	A(X118)	address of test routine
00006C86	00			5185+	DC	H' 118'	test number
00006C87	01			5186+	DC	X' 00'	
00006C88	01			5187+	DC	HL1' 1'	m4 used
00006C88	01			5188+	DC	HL1' 1'	m5 used
00006C89	01			5189+	DC	HL1' 1'	CC
00006C8A	0B			5190+	DC	HL1' 11'	CC failed mask
00006C8C	00000000	00000000		5191+	DS	2F	extracted PSW after test (has CC)
00006C94	FF			5192+	DC	X' FF'	extracted CC, if test failed
00006C95	E5C3C8D3	40404040		5193+	DC	CL8' VCHL'	instruction name
00006CA0	00006D18			5194+	DC	A(RE118)	address of v1 result
00006CA4	00006D28			5195+	DC	A(RE118+16)	address of v2 source
00006CA8	00006D38			5196+	DC	A(RE118+32)	address of v3 source
00006CAC	00000010			5197+	DC	A(16)	result length
00006CB0	00006D18			5198+REA118	DC	A(RE118)	result address
00006CB8	00000000	00000000		5199+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006CC0	00000000 00000000						
00006CC8	00000000 00000000			5200+V10118	DS	XL16	V1 output
00006CD0	00000000 00000000						
00006CD8	00000000 00000000			5201+	DS	2FD	gap
00006CE0	00000000 00000000						
00006CE8				5202+*			
00006CE8	E310 5024 0014		00000024	5203+X118	DS	0F	
00006CEE	E761 0000 0806		00000000	5204+	LGF	R1, V2ADDR	load v2 source
00006CF4	E310 5028 0014		00000028	5205+	VL	v22, 0(R1)	use v21 to test decoder
00006CFA	E771 0000 0806		00000000	5206+	LGF	R1, V3ADDR	load v3 source
00006D00	E756 7010 1EF9			5207+	VL	v23, 0(R1)	use v22 to test decoder
00006D06	B98D 0020			5208+	VCHL	V21, V22, V23, 1, 1	test instruction
00006D0A	5020 500C		0000000C	5209+	EPSW	R2, R0	extract psw
00006D0E	E750 5048 080E		00006CC8	5210+	ST	R2, CCPSW	to save CC
00006D14	07FB			5211+	VST	V21, V10118	save v1 output
00006D18				5212+	BR	R11	return
00006D18				5213+RE118	DC	0F	V1 for this test
00006D18	00000000 0000FFFF			5214+	DROP	R5	
00006D20	FFFFFFFF FFFFFFFF			5215	DC	XL16' 000000000000FFFF FFFFFFFF'	result t
00006D28	08090A0B 0C0DFE1F			5216	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
00006D30	00110033 00550077						
00006D38	08090A0B 0C0DFE0F			5217	DC	XL16' 08090A0B0C0DFE0F 0001002300450067'	v3
00006D40	00010023 00450067						
00006D48				5218			
00006D48		00006D48		5219	VRR_B	VCHL, 1, 3	
00006D48	00006DB0			5220+	DS	0FD	
00006D4C	0077			5221+	USING	*, R5	base for test data and test routine
00006D4E	00			5222+T119	DC	A(X119)	address of test routine
00006D4F	01			5223+	DC	H' 119'	test number
00006D50	01			5224+	DC	X' 00'	
00006D51	03			5225+	DC	HL1' 1'	m4 used
00006D52	0E			5226+	DC	HL1' 1'	m5 used
00006D54	00000000 00000000			5227+	DC	HL1' 3'	CC
00006D5C	FF			5228+	DC	HL1' 14'	CC failed mask
00006D5D	E5C3C8D3 40404040			5229+	DS	2F	extracted PSW after test (has CC)
00006D68	00006DE0			5230+	DC	X' FF'	extracted CC, if test failed
00006D6C	00006DF0			5231+	DC	CL8' VCHL'	instruction name
00006D70	00006E00			5232+	DC	A(RE119)	address of v1 result
00006D74	00000010			5233+	DC	A(RE119+16)	address of v2 source
00006D78	00006DE0			5234+	DC	A(RE119+32)	address of v3 source
00006D80	00000000 00000000			5235+	DC	A(16)	result length
00006D88	00000000 00000000			5236+REA119	DC	A(RE119)	result address
00006D90	00000000 00000000			5237+	DS	2FD	gap
00006D98	00000000 00000000						
00006DA0	00000000 00000000			5238+V10119	DS	XL16	V1 output
00006DA8	00000000 00000000						
00006DB0				5239+	DS	2FD	gap
00006DB0				5240+*			
00006DB0	E310 5024 0014		00000024	5241+X119	DS	0F	
00006DB6	E761 0000 0806		00000000	5242+	LGF	R1, V2ADDR	load v2 source
00006DBC	E310 5028 0014		00000028	5243+	VL	v22, 0(R1)	use v21 to test decoder
00006DC2	E771 0000 0806		00000000	5244+	LGF	R1, V3ADDR	load v3 source
00006DC8	E756 7010 1EF9			5245+	VL	v23, 0(R1)	use v22 to test decoder
				5246+	VCHL	V21, V22, V23, 1, 1	test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006DCE	B98D 0020			5247+	EPSW	R2, R0	extract psw
00006DD2	5020 500C		0000000C	5248+	ST	R2, CCPSW	to save CC
00006DD6	E750 5048 080E		00006D90	5249+	VST	V21, V10119	save v1 output
00006DDC	07FB			5250+	BR	R11	return
00006DE0				5251+RE119	DC	0F	V1 for this test
00006DE0				5252+	DROP	R5	
00006DE0	00000000 00000000			5253	DC	XL16' 0000000000000000 0000000000000000'	result t
00006DE8	00000000 00000000						
00006DF0	00010003 04050607			5254	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00006DF8	00090A0B 0C0D0E0F						
00006E00	01110233 11550677			5255	DC	XL16' 0111023311550677 119911BBF1DD11FF'	v3
00006E08	119911BB F1DD11FF						
				5256			
				5257	VRR_B	VCHL, 1, 3	
00006E10				5258+	DS	0FD	
00006E10		00006E10		5259+	USING	*, R5	base for test data and test routine
00006E10	00006E78			5260+T120	DC	A(X120)	address of test routine
00006E14	0078			5261+	DC	H' 120'	test number
00006E16	00			5262+	DC	X' 00'	
00006E17	01			5263+	DC	HL1' 1'	m4 used
00006E18	01			5264+	DC	HL1' 1'	m5 used
00006E19	03			5265+	DC	HL1' 3'	CC
00006E1A	0E			5266+	DC	HL1' 14'	CC failed mask
00006E1C	00000000 00000000			5267+	DS	2F	extracted PSW after test (has CC)
00006E24	FF			5268+	DC	X' FF'	extracted CC, if test failed
00006E25	E5C3C8D3 40404040			5269+	DC	CL8' VCHL'	instruction name
00006E30	00006EA8			5270+	DC	A(RE120)	address of v1 result
00006E34	00006EB8			5271+	DC	A(RE120+16)	address of v2 source
00006E38	00006EC8			5272+	DC	A(RE120+32)	address of v3 source
00006E3C	00000010			5273+	DC	A(16)	result length
00006E40	00006EA8			5274+REA120	DC	A(RE120)	result address
00006E48	00000000 00000000			5275+	DS	2FD	gap
00006E50	00000000 00000000						
00006E58	00000000 00000000			5276+V10120	DS	XL16	V1 output
00006E60	00000000 00000000						
00006E68	00000000 00000000			5277+	DS	2FD	gap
00006E70	00000000 00000000						
				5278+*			
00006E78				5279+X120	DS	0F	
00006E78	E310 5024 0014		00000024	5280+	LGF	R1, V2ADDR	load v2 source
00006E7E	E761 0000 0806		00000000	5281+	VL	v22, 0(R1)	use v21 to test decoder
00006E84	E310 5028 0014		00000028	5282+	LGF	R1, V3ADDR	load v3 source
00006E8A	E771 0000 0806		00000000	5283+	VL	v23, 0(R1)	use v22 to test decoder
00006E90	E756 7010 1EF9			5284+	VCHL	V21, V22, V23, 1, 1	test instruction
00006E96	B98D 0020			5285+	EPSW	R2, R0	extract psw
00006E9A	5020 500C		0000000C	5286+	ST	R2, CCPSW	to save CC
00006E9E	E750 5048 080E		00006E58	5287+	VST	V21, V10120	save v1 output
00006EA4	07FB			5288+	BR	R11	return
00006EA8				5289+RE120	DC	0F	V1 for this test
00006EA8				5290+	DROP	R5	
00006EA8	00000000 00000000			5291	DC	XL16' 0000000000000000 0000000000000000'	result t
00006EB0	00000000 00000000						
00006EB8	08090A0B 0C0D0E0F			5292	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00006EC0	00010203 04050607						
00006EC8	119911BB F1DD11FF			5293	DC	XL16' 119911BBF1DD11FF 0111023311550677'	v3
00006ED0	01110233 11550677						



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				5294			
				5295	*Word		
				5296	VRR_B VCHL, 2, 0		
00006ED8				5297+	DS 0FD		
00006ED8		00006ED8		5298+	USING *, R5	base for test data and test routine	
00006ED8	00006F40			5299+T121	DC A(X121)	address of test routine	
00006EDC	0079			5300+	DC H' 121'	test number	
00006EDE	00			5301+	DC X' 00'		
00006EDF	02			5302+	DC HL1' 2'	m4 used	
00006EE0	01			5303+	DC HL1' 1'	m5 used	
00006EE1	00			5304+	DC HL1' 0'	CC	
00006EE2	07			5305+	DC HL1' 7'	CC failed mask	
00006EE4	00000000	00000000		5306+	DS 2F	extracted PSW after test (has CC)	
00006EEC	FF			5307+	DC X' FF'	extracted CC, if test failed	
00006EED	E5C3C8D3	40404040		5308+	DC CL8' VCHL'	instruction name	
00006EF8	00006F70			5309+	DC A(RE121)	address of v1 result	
00006EFC	00006F80			5310+	DC A(RE121+16)	address of v2 source	
00006F00	00006F90			5311+	DC A(RE121+32)	address of v3 source	
00006F04	00000010			5312+	DC A(16)	result length	
00006F08	00006F70			5313+REA121	DC A(RE121)	result address	
00006F10	00000000	00000000		5314+	DS 2FD	gap	
00006F18	00000000	00000000					
00006F20	00000000	00000000		5315+V10121	DS XL16	V1 output	
00006F28	00000000	00000000					
00006F30	00000000	00000000		5316+	DS 2FD	gap	
00006F38	00000000	00000000					
				5317+*			
00006F40				5318+X121	DS 0F		
00006F40	E310 5024 0014		00000024	5319+	LGF R1, V2ADDR	load v2 source	
00006F46	E761 0000 0806		00000000	5320+	VL v22, 0(R1)	use v21 to test decoder	
00006F4C	E310 5028 0014		00000028	5321+	LGF R1, V3ADDR	load v3 source	
00006F52	E771 0000 0806		00000000	5322+	VL v23, 0(R1)	use v22 to test decoder	
00006F58	E756 7010 2EF9			5323+	VCHL V21, V22, V23, 2, 1	test instruction	
00006F5E	B98D 0020			5324+	EPSW R2, R0	extract psw	
00006F62	5020 500C		0000000C	5325+	ST R2, CCPSW	to save CC	
00006F66	E750 5048 080E		00006F20	5326+	VST V21, V10121	save v1 output	
00006F6C	07FB			5327+	BR R11	return	
00006F70				5328+RE121	DC 0F	V1 for this test	
00006F70				5329+	DROP R5		
00006F70	FFFFFFFF FFFFFFFF			5330	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00006F78	FFFFFFFF FFFFFFFF						
00006F80	01020304 05060708			5331	DC XL16' 0102030405060708 090A0B0C0D0E0F10'	v2	
00006F88	090A0B0C 0D0E0F10						
00006F90	00010203 04050607			5332	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v3	
00006F98	08090A0B 0C0D0E0F						
				5333			
				5334	VRR_B VCHL, 2, 0		
00006FA0				5335+	DS 0FD		
00006FA0		00006FA0		5336+	USING *, R5	base for test data and test routine	
00006FA0	00007008			5337+T122	DC A(X122)	address of test routine	
00006FA4	007A			5338+	DC H' 122'	test number	
00006FA6	00			5339+	DC X' 00'		
00006FA7	02			5340+	DC HL1' 2'	m4 used	
00006FA8	01			5341+	DC HL1' 1'	m5 used	
00006FA9	00			5342+	DC HL1' 0'	CC	
00006FAA	07			5343+	DC HL1' 7'	CC failed mask	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006FAC	00000000	00000000		5344+	DS	2F	extracted PSW after test (has CC)
00006FB4	FF			5345+	DC	X' FF'	extracted CC, if test failed
00006FB5	E5C3C8D3	40404040		5346+	DC	CL8' VCHL'	instruction name
00006FC0	00007038			5347+	DC	A(RE122)	address of v1 result
00006FC4	00007048			5348+	DC	A(RE122+16)	address of v2 source
00006FC8	00007058			5349+	DC	A(RE122+32)	address of v3 source
00006FCC	00000010			5350+	DC	A(16)	result length
00006FD0	00007038			5351+REA122	DC	A(RE122)	result address
00006FD8	00000000	00000000		5352+	DS	2FD	gap
00006FE0	00000000	00000000					
00006FE8	00000000	00000000		5353+V10122	DS	XL16	V1 output
00006FF0	00000000	00000000					
00006FF8	00000000	00000000		5354+	DS	2FD	gap
00007000	00000000	00000000					
				5355+*			
00007008				5356+X122	DS	0F	
00007008	E310 5024 0014		00000024	5357+	LGF	R1, V2ADDR	load v2 source
0000700E	E761 0000 0806		00000000	5358+	VL	v22, 0(R1)	use v21 to test decoder
00007014	E310 5028 0014		00000028	5359+	LGF	R1, V3ADDR	load v3 source
0000701A	E771 0000 0806		00000000	5360+	VL	v23, 0(R1)	use v22 to test decoder
00007020	E756 7010 2EF9			5361+	VCHL	V21, V22, V23, 2, 1	test instruction
00007026	B98D 0020			5362+	EPSW	R2, R0	extract psw
0000702A	5020 500C		0000000C	5363+	ST	R2, CCPSW	to save CC
0000702E	E750 5048 080E		00006FE8	5364+	VST	V21, V10122	save v1 output
00007034	07FB			5365+	BR	R11	return
00007038				5366+RE122	DC	0F	V1 for this test
00007038				5367+	DROP	R5	
00007038	FFFFFFFF	FFFFFFFF		5368	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00007040	FFFFFFFF	FFFFFFFF					
00007048	FFFEFFFD	FFFCFFFB		5369	DC	XL16' FFFEFFFDFFFCFFFB FFFAFFF9FFF8FFF7'	v2
00007050	FFFAFFF9	FFF8FFF7					
00007058	00010203	04050607		5370	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00007060	08090A0B	0C0D0E0F					
				5371			
				5372	VRR_B	VCHL, 2, 1	
00007068				5373+	DS	0FD	
00007068		00007068		5374+	USING	*, R5	base for test data and test routine
00007068	000070D0			5375+T123	DC	A(X123)	address of test routine
0000706C	007B			5376+	DC	H' 123'	test number
0000706E	00			5377+	DC	X' 00'	
0000706F	02			5378+	DC	HL1' 2'	m4 used
00007070	01			5379+	DC	HL1' 1'	m5 used
00007071	01			5380+	DC	HL1' 1'	CC
00007072	0B			5381+	DC	HL1' 11'	CC failed mask
00007074	00000000	00000000		5382+	DS	2F	extracted PSW after test (has CC)
0000707C	FF			5383+	DC	X' FF'	extracted CC, if test failed
0000707D	E5C3C8D3	40404040		5384+	DC	CL8' VCHL'	instruction name
00007088	00007100			5385+	DC	A(RE123)	address of v1 result
0000708C	00007110			5386+	DC	A(RE123+16)	address of v2 source
00007090	00007120			5387+	DC	A(RE123+32)	address of v3 source
00007094	00000010			5388+	DC	A(16)	result length
00007098	00007100			5389+REA123	DC	A(RE123)	result address
000070A0	00000000	00000000		5390+	DS	2FD	gap
000070A8	00000000	00000000					
000070B0	00000000	00000000		5391+V10123	DS	XL16	V1 output
000070B8	00000000	00000000					

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000070C0	00000000 00000000			5392+	DS	2FD	gap
000070C8	00000000 00000000						
000070D0				5393+*			
000070D0	E310 5024 0014		00000024	5394+X123	DS	0F	
000070D6	E761 0000 0806		00000000	5395+	LGF	R1, V2ADDR	load v2 source
000070DC	E310 5028 0014		00000028	5396+	VL	v22, 0(R1)	use v21 to test decoder
000070E2	E771 0000 0806		00000000	5397+	LGF	R1, V3ADDR	load v3 source
000070E8	E756 7010 2EF9			5398+	VL	v23, 0(R1)	use v22 to test decoder
000070EE	B98D 0020			5399+	VCHL	V21, V22, V23, 2, 1	test instruction
000070F2	5020 500C		0000000C	5400+	EPSW	R2, R0	extract psw
000070F6	E750 5048 080E		000070B0	5401+	ST	R2, CCPSW	to save CC
000070FC	07FB			5402+	VST	V21, V10123	save v1 output
00007100				5403+	BR	R11	return
00007100				5404+RE123	DC	0F	V1 for this test
00007100	FFFFFFFF FFFFFFFF			5405+	DROP	R5	
00007108	00000000 FFFFFFFF			5406	DC	XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result t
00007110	00110033 00550077			5407	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'	v2
00007118	08090A0B 0C0DFE1F						
00007120	00010023 00450067			5408	DC	XL16' 0001002300450067 08090A0B0C0DFE0F'	v3
00007128	08090A0B 0C0DFE0F						
00007130				5409			
00007130		00007130		5410	VRR_B	VCHL, 2, 1	
00007130	00007198			5411+	DS	0FD	
00007134	007C			5412+	USING	*, R5	base for test data and test routine
00007136	00			5413+T124	DC	A(X124)	address of test routine
00007137	02			5414+	DC	H' 124'	test number
00007138	01			5415+	DC	X' 00'	
00007139	01			5416+	DC	HL1' 2'	m4 used
0000713A	0B			5417+	DC	HL1' 1'	m5 used
0000713C	00000000 00000000			5418+	DC	HL1' 1'	CC
00007144	FF			5419+	DC	HL1' 11'	CC failed mask
00007145	E5C3C8D3 40404040			5420+	DS	2F	extracted PSW after test (has CC)
00007150	000071C8			5421+	DC	X' FF'	extracted CC, if test failed
00007154	000071D8			5422+	DC	CL8' VCHL'	instruction name
00007158	000071E8			5423+	DC	A(RE124)	address of v1 result
0000715C	00000010			5424+	DC	A(RE124+16)	address of v2 source
00007160	000071C8			5425+	DC	A(RE124+32)	address of v3 source
00007168	00000000 00000000			5426+	DC	A(16)	result length
00007170	00000000 00000000			5427+REA124	DC	A(RE124)	result address
00007178	00000000 00000000			5428+	DS	2FD	gap
00007180	00000000 00000000						
00007188	00000000 00000000			5429+V10124	DS	XL16	V1 output
00007190	00000000 00000000						
00007198				5430+	DS	2FD	gap
00007198				5431+*			
00007198	E310 5024 0014		00000024	5432+X124	DS	0F	
0000719E	E761 0000 0806		00000000	5433+	LGF	R1, V2ADDR	load v2 source
000071A4	E310 5028 0014		00000028	5434+	VL	v22, 0(R1)	use v21 to test decoder
000071AA	E771 0000 0806		00000000	5435+	LGF	R1, V3ADDR	load v3 source
000071B0	E756 7010 2EF9			5436+	VL	v23, 0(R1)	use v22 to test decoder
000071B6	B98D 0020			5437+	VCHL	V21, V22, V23, 2, 1	test instruction
000071BA	5020 500C		0000000C	5438+	EPSW	R2, R0	extract psw
000071BE	E750 5048 080E		00007178	5439+	ST	R2, CCPSW	to save CC
				5440+	VST	V21, V10124	save v1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000071C4	07FB			5441+	BR	R11	return
000071C8				5442+RE124	DC	0F	V1 for this test
000071C8				5443+	DROP	R5	
000071C8	00000000 FFFFFFFF			5444	DC	XL16' 00000000FFFFFFFF FFFFFFFF	result t
000071D0	FFFFFFFF FFFFFFFF						
000071D8	08090A0B 0C0DFE1F			5445	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
000071E0	00110033 00550077						
000071E8	08090A0B 0C0DFE0F			5446	DC	XL16' 08090A0B0C0DFE0F 0001002300450067'	v3
000071F0	00010023 00450067						
				5447			
				5448	VRR_B	VCHL, 2, 3	
000071F8				5449+	DS	0FD	
000071F8		000071F8		5450+	USING	*, R5	base for test data and test routine
000071F8	00007260			5451+T125	DC	A(X125)	address of test routine
000071FC	007D			5452+	DC	H' 125'	test number
000071FE	00			5453+	DC	X' 00'	
000071FF	02			5454+	DC	HL1' 2'	m4 used
00007200	01			5455+	DC	HL1' 1'	m5 used
00007201	03			5456+	DC	HL1' 3'	CC
00007202	0E			5457+	DC	HL1' 14'	CC failed mask
00007204	00000000 00000000			5458+	DS	2F	extracted PSW after test (has CC)
0000720C	FF			5459+	DC	X' FF'	extracted CC, if test failed
0000720D	E5C3C8D3 40404040			5460+	DC	CL8' VCHL'	instruction name
00007218	00007290			5461+	DC	A(RE125)	address of v1 result
0000721C	000072A0			5462+	DC	A(RE125+16)	address of v2 source
00007220	000072B0			5463+	DC	A(RE125+32)	address of v3 source
00007224	00000010			5464+	DC	A(16)	result length
00007228	00007290			5465+REA125	DC	A(RE125)	result address
00007230	00000000 00000000			5466+	DS	2FD	gap
00007238	00000000 00000000						
00007240	00000000 00000000			5467+V10125	DS	XL16	V1 output
00007248	00000000 00000000						
00007250	00000000 00000000			5468+	DS	2FD	gap
00007258	00000000 00000000						
				5469+*			
00007260				5470+X125	DS	0F	
00007260	E310 5024 0014		00000024	5471+	LGF	R1, V2ADDR	load v2 source
00007266	E761 0000 0806		00000000	5472+	VL	v22, 0(R1)	use v21 to test decoder
0000726C	E310 5028 0014		00000028	5473+	LGF	R1, V3ADDR	load v3 source
00007272	E771 0000 0806		00000000	5474+	VL	v23, 0(R1)	use v22 to test decoder
00007278	E756 7010 2EF9			5475+	VCHL	V21, V22, V23, 2, 1	test instruction
0000727E	B98D 0020			5476+	EPSW	R2, R0	extract psw
00007282	5020 500C		0000000C	5477+	ST	R2, CCPSW	to save CC
00007286	E750 5048 080E		00007240	5478+	VST	V21, V10125	save v1 output
0000728C	07FB			5479+	BR	R11	return
00007290				5480+RE125	DC	0F	V1 for this test
00007290				5481+	DROP	R5	
00007290	00000000 00000000			5482	DC	XL16' 0000000000000000 0000000000000000'	result t
00007298	00000000 00000000						
000072A0	00010003 04050607			5483	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
000072A8	00090A0B 0C0D0E0F						
000072B0	01110233 11550677			5484	DC	XL16' 0111023311550677 119911BBF1DD11FF'	v3
000072B8	119911BB F1DD11FF						
				5485			
				5486	VRR_B	VCHL, 2, 3	
000072C0				5487+	DS	0FD	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000072C0		000072C0		5488+	USING *, R5	base for test data and test routine
000072C0	00007328			5489+T126	DC A(X126)	address of test routine
000072C4	007E			5490+	DC H' 126'	test number
000072C6	00			5491+	DC X' 00'	
000072C7	02			5492+	DC HL1' 2'	m4 used
000072C8	01			5493+	DC HL1' 1'	m5 used
000072C9	03			5494+	DC HL1' 3'	CC
000072CA	0E			5495+	DC HL1' 14'	CC failed mask
000072CC	00000000 00000000			5496+	DS 2F	extracted PSW after test (has CC)
000072D4	FF			5497+	DC X' FF'	extracted CC, if test failed
000072D5	E5C3C8D3 40404040			5498+	DC CL8' VCHL'	instruction name
000072E0	00007358			5499+	DC A(RE126)	address of v1 result
000072E4	00007368			5500+	DC A(RE126+16)	address of v2 source
000072E8	00007378			5501+	DC A(RE126+32)	address of v3 source
000072EC	00000010			5502+	DC A(16)	result length
000072F0	00007358			5503+REA126	DC A(RE126)	result address
000072F8	00000000 00000000			5504+	DS 2FD	gap
00007300	00000000 00000000					
00007308	00000000 00000000			5505+V10126	DS XL16	V1 output
00007310	00000000 00000000					
00007318	00000000 00000000			5506+	DS 2FD	gap
00007320	00000000 00000000					
				5507+*		
00007328				5508+X126	DS 0F	
00007328	E310 5024 0014	00000024		5509+	LGF R1, V2ADDR	load v2 source
0000732E	E761 0000 0806	00000000		5510+	VL v22, 0(R1)	use v21 to test decoder
00007334	E310 5028 0014	00000028		5511+	LGF R1, V3ADDR	load v3 source
0000733A	E771 0000 0806	00000000		5512+	VL v23, 0(R1)	use v22 to test decoder
00007340	E756 7010 2EF9			5513+	VCHL V21, V22, V23, 2, 1	test instruction
00007346	B98D 0020			5514+	EPSW R2, R0	extract psw
0000734A	5020 500C	0000000C		5515+	ST R2, CCPSW	to save CC
0000734E	E750 5048 080E	00007308		5516+	VST V21, V10126	save v1 output
00007354	07FB			5517+	BR R11	return
00007358				5518+RE126	DC 0F	V1 for this test
00007358				5519+	DROP R5	
00007358	00000000 00000000			5520	DC XL16' 0000000000000000 0000000000000000'	result
00007360	00000000 00000000					
00007368	08090A0B 0C0D0E0F			5521	DC XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00007370	00010203 04050607					
00007378	119911BB F1DD11FF			5522	DC XL16' 119911BBF1DD11FF 0111023311550677'	v3
00007380	01110233 11550677					
				5523		
				5524 *Doubleword		
				5525	VRR_B VCHL, 3, 0	
00007388				5526+	DS 0FD	
00007388		00007388		5527+	USING *, R5	base for test data and test routine
00007388	000073F0			5528+T127	DC A(X127)	address of test routine
0000738C	007F			5529+	DC H' 127'	test number
0000738E	00			5530+	DC X' 00'	
0000738F	03			5531+	DC HL1' 3'	m4 used
00007390	01			5532+	DC HL1' 1'	m5 used
00007391	00			5533+	DC HL1' 0'	CC
00007392	07			5534+	DC HL1' 7'	CC failed mask
00007394	00000000 00000000			5535+	DS 2F	extracted PSW after test (has CC)
0000739C	FF			5536+	DC X' FF'	extracted CC, if test failed
0000739D	E5C3C8D3 40404040			5537+	DC CL8' VCHL'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000073A8	00007420			5538+	DC	A(RE127)	address of v1 result
000073AC	00007430			5539+	DC	A(RE127+16)	address of v2 source
000073B0	00007440			5540+	DC	A(RE127+32)	address of v3 source
000073B4	00000010			5541+	DC	A(16)	result length
000073B8	00007420			5542+REA127	DC	A(RE127)	result address
000073C0	00000000 00000000			5543+	DS	2FD	gap
000073C8	00000000 00000000						
000073D0	00000000 00000000			5544+V10127	DS	XL16	V1 output
000073D8	00000000 00000000						
000073E0	00000000 00000000			5545+	DS	2FD	gap
000073E8	00000000 00000000						
000073F0				5546+*			
000073F0	E310 5024 0014		00000024	5547+X127	DS	0F	
000073F6	E761 0000 0806		00000000	5548+	LGF	R1, V2ADDR	load v2 source
000073FC	E310 5028 0014		00000028	5549+	VL	v22, 0(R1)	use v21 to test decoder
00007402	E771 0000 0806		00000000	5550+	LGF	R1, V3ADDR	load v3 source
00007408	E756 7010 3EF9			5551+	VL	v23, 0(R1)	use v22 to test decoder
0000740E	B98D 0020			5552+	VCHL	V21, V22, V23, 3, 1	test instruction
00007412	5020 500C		0000000C	5553+	EPSW	R2, R0	extract psw
00007416	E750 5048 080E		000073D0	5554+	ST	R2, CCPSW	to save CC
0000741C	07FB			5555+	VST	V21, V10127	save v1 output
00007420				5556+	BR	R11	return
00007420				5557+RE127	DC	0F	V1 for this test
00007420				5558+	DROP	R5	
00007420	FFFFFFFF FFFFFFFF			5559	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00007428	FFFFFFFF FFFFFFFF						
00007430	01020304 05060708			5560	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
00007438	090A0B0C 0D0E0F10						
00007440	00010203 04050607			5561	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00007448	08090A0B 0C0D0E0F						
00007450				5562			
00007450		00007450		5563	VRR_B	VCHL, 3, 0	
00007450	000074B8			5564+	DS	0FD	
00007454	0080			5565+	USING	*, R5	base for test data and test routine
00007456	00			5566+T128	DC	A(X128)	address of test routine
00007457	03			5567+	DC	H' 128'	test number
00007458	01			5568+	DC	X' 00'	
00007459	00			5569+	DC	HL1' 3'	m4 used
0000745A	07			5570+	DC	HL1' 1'	m5 used
0000745C	00000000 00000000			5571+	DC	HL1' 0'	CC
00007464	FF			5572+	DC	HL1' 7'	CC failed mask
00007465	E5C3C8D3 40404040			5573+	DS	2F	extracted PSW after test (has CC)
00007470	000074E8			5574+	DC	X' FF'	extracted CC, if test failed
00007474	000074F8			5575+	DC	CL8' VCHL'	instruction name
00007478	00007508			5576+	DC	A(RE128)	address of v1 result
0000747C	00000010			5577+	DC	A(RE128+16)	address of v2 source
00007480	000074E8			5578+	DC	A(RE128+32)	address of v3 source
00007488	00000000 00000000			5579+	DC	A(16)	result length
00007490	00000000 00000000			5580+REA128	DC	A(RE128)	result address
00007498	00000000 00000000			5581+	DS	2FD	gap
000074A0	00000000 00000000			5582+V10128	DS	XL16	V1 output
000074A8	00000000 00000000						
000074B0	00000000 00000000			5583+	DS	2FD	gap
				5584+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000074B8				5585+X128	DS	0F	
000074B8	E310 5024 0014		00000024	5586+	LGF	R1, V2ADDR	load v2 source
000074BE	E761 0000 0806		00000000	5587+	VL	v22, 0(R1)	use v21 to test decoder
000074C4	E310 5028 0014		00000028	5588+	LGF	R1, V3ADDR	load v3 source
000074CA	E771 0000 0806		00000000	5589+	VL	v23, 0(R1)	use v22 to test decoder
000074D0	E756 7010 3EF9			5590+	VCHL	V21, V22, V23, 3, 1	test instruction
000074D6	B98D 0020			5591+	EPSW	R2, R0	extract psw
000074DA	5020 500C		0000000C	5592+	ST	R2, CCPSW	to save CC
000074DE	E750 5048 080E		00007498	5593+	VST	V21, V10128	save v1 output
000074E4	07FB			5594+	BR	R11	return
000074E8				5595+RE128	DC	0F	V1 for this test
000074E8				5596+	DROP	R5	
000074E8	FFFFFFFF FFFFFFFF			5597	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000074F0	FFFFFFFF FFFFFFFF						
000074F8	FFFEFFFD FFFCFFFB			5598	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00007500	FFFAFFF9 FFF8FFF7						
00007508	00010203 04050607			5599	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00007510	08090A0B 0C0D0E0F						
				5600			
				5601	VRR_B	VCHL, 3, 1	
00007518				5602+	DS	0FD	
00007518		00007518		5603+	USING	*, R5	base for test data and test routine
00007518	00007580			5604+T129	DC	A(X129)	address of test routine
0000751C	0081			5605+	DC	H' 129'	test number
0000751E	00			5606+	DC	X' 00'	
0000751F	03			5607+	DC	HL1' 3'	m4 used
00007520	01			5608+	DC	HL1' 1'	m5 used
00007521	01			5609+	DC	HL1' 1'	CC
00007522	0B			5610+	DC	HL1' 11'	CC failed mask
00007524	00000000 00000000			5611+	DS	2F	extracted PSW after test (has CC)
0000752C	FF			5612+	DC	X' FF'	extracted CC, if test failed
0000752D	E5C3C8D3 40404040			5613+	DC	CL8' VCHL'	instruction name
00007538	000075B0			5614+	DC	A(RE129)	address of v1 result
0000753C	000075C0			5615+	DC	A(RE129+16)	address of v2 source
00007540	000075D0			5616+	DC	A(RE129+32)	address of v3 source
00007544	00000010			5617+	DC	A(16)	result length
00007548	000075B0			5618+REA129	DC	A(RE129)	result address
00007550	00000000 00000000			5619+	DS	2FD	gap
00007558	00000000 00000000						
00007560	00000000 00000000			5620+V10129	DS	XL16	V1 output
00007568	00000000 00000000						
00007570	00000000 00000000			5621+	DS	2FD	gap
00007578	00000000 00000000						
				5622+*			
00007580				5623+X129	DS	0F	
00007580	E310 5024 0014		00000024	5624+	LGF	R1, V2ADDR	load v2 source
00007586	E761 0000 0806		00000000	5625+	VL	v22, 0(R1)	use v21 to test decoder
0000758C	E310 5028 0014		00000028	5626+	LGF	R1, V3ADDR	load v3 source
00007592	E771 0000 0806		00000000	5627+	VL	v23, 0(R1)	use v22 to test decoder
00007598	E756 7010 3EF9			5628+	VCHL	V21, V22, V23, 3, 1	test instruction
0000759E	B98D 0020			5629+	EPSW	R2, R0	extract psw
000075A2	5020 500C		0000000C	5630+	ST	R2, CCPSW	to save CC
000075A6	E750 5048 080E		00007560	5631+	VST	V21, V10129	save v1 output
000075AC	07FB			5632+	BR	R11	return
000075B0				5633+RE129	DC	0F	V1 for this test
000075B0				5634+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000075B0	FFFFFFFF FFFFFFFF			5635	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result
000075B8	00000000 00000000						
000075C0	00110033 00550077			5636	DC	XL16' 0011003300550077 08090A0B0C0DFE0F'	v2
000075C8	08090A0B 0C0DFE0F						
000075D0	00010023 00450067			5637	DC	XL16' 0001002300450067 08090A0B0C0DFE1F'	v3
000075D8	08090A0B 0C0DFE1F						
				5638			
				5639	VRR_B	VCHL, 3, 1	
000075E0				5640+	DS	0FD	
000075E0		000075E0		5641+	USING	*, R5	base for test data and test routine
000075E0	00007648			5642+T130	DC	A(X130)	address of test routine
000075E4	0082			5643+	DC	H' 130'	test number
000075E6	00			5644+	DC	X' 00'	
000075E7	03			5645+	DC	HL1' 3'	m4 used
000075E8	01			5646+	DC	HL1' 1'	m5 used
000075E9	01			5647+	DC	HL1' 1'	CC
000075EA	0B			5648+	DC	HL1' 11'	CC failed mask
000075EC	00000000 00000000			5649+	DS	2F	extracted PSW after test (has CC)
000075F4	FF			5650+	DC	X' FF'	extracted CC, if test failed
000075F5	E5C3C8D3 40404040			5651+	DC	CL8' VCHL'	instruction name
00007600	00007678			5652+	DC	A(RE130)	address of v1 result
00007604	00007688			5653+	DC	A(RE130+16)	address of v2 source
00007608	00007698			5654+	DC	A(RE130+32)	address of v3 source
0000760C	00000010			5655+	DC	A(16)	result length
00007610	00007678			5656+REA130	DC	A(RE130)	result address
00007618	00000000 00000000			5657+	DS	2FD	gap
00007620	00000000 00000000						
00007628	00000000 00000000			5658+V10130	DS	XL16	V1 output
00007630	00000000 00000000						
00007638	00000000 00000000			5659+	DS	2FD	gap
00007640	00000000 00000000						
				5660+*			
00007648				5661+X130	DS	0F	
00007648	E310 5024 0014		00000024	5662+	LGF	R1, V2ADDR	load v2 source
0000764E	E761 0000 0806		00000000	5663+	VL	v22, 0(R1)	use v21 to test decoder
00007654	E310 5028 0014		00000028	5664+	LGF	R1, V3ADDR	load v3 source
0000765A	E771 0000 0806		00000000	5665+	VL	v23, 0(R1)	use v22 to test decoder
00007660	E756 7010 3EF9			5666+	VCHL	V21, V22, V23, 3, 1	test instruction
00007666	B98D 0020			5667+	EPSW	R2, R0	extract psw
0000766A	5020 500C		0000000C	5668+	ST	R2, CCPSW	to save CC
0000766E	E750 5048 080E		00007628	5669+	VST	V21, V10130	save v1 output
00007674	07FB			5670+	BR	R11	return
00007678				5671+RE130	DC	0F	V1 for this test
00007678				5672+	DROP	R5	
00007678	00000000 00000000			5673	DC	XL16' 0000000000000000 FFFFFFFFFFFFFFFFFF'	result
00007680	FFFFFFFF FFFFFFFF						
00007688	08090A0B 0C0DFE0F			5674	DC	XL16' 08090A0B0C0DFE0F 0011003300550077'	v2
00007690	00110033 00550077						
00007698	08090A0B 0C0DFE1F			5675	DC	XL16' 08090A0B0C0DFE1F 0001002300450067'	v3
000076A0	00010023 00450067						
				5676			
				5677	VRR_B	VCHL, 3, 3	
000076A8				5678+	DS	0FD	
000076A8		000076A8		5679+	USING	*, R5	base for test data and test routine
000076A8	00007710			5680+T131	DC	A(X131)	address of test routine
000076AC	0083			5681+	DC	H' 131'	test number



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000076AE	00			5682+	DC	X' 00'	
000076AF	03			5683+	DC	HL1' 3'	m4 used
000076B0	01			5684+	DC	HL1' 1'	m5 used
000076B1	03			5685+	DC	HL1' 3'	CC
000076B2	0E			5686+	DC	HL1' 14'	CC failed mask
000076B4	00000000	00000000		5687+	DS	2F	extracted PSW after test (has CC)
000076BC	FF			5688+	DC	X' FF'	extracted CC, if test failed
000076BD	E5C3C8D3	40404040		5689+	DC	CL8' VCHL'	instruction name
000076C8	00007740			5690+	DC	A(RE131)	address of v1 result
000076CC	00007750			5691+	DC	A(RE131+16)	address of v2 source
000076D0	00007760			5692+	DC	A(RE131+32)	address of v3 source
000076D4	00000010			5693+	DC	A(16)	result length
000076D8	00007740			5694+REA131	DC	A(RE131)	result address
000076E0	00000000	00000000		5695+	DS	2FD	gap
000076E8	00000000	00000000					
000076F0	00000000	00000000		5696+V10131	DS	XL16	V1 output
000076F8	00000000	00000000					
00007700	00000000	00000000		5697+	DS	2FD	gap
00007708	00000000	00000000					
				5698+*			
00007710				5699+X131	DS	0F	
00007710	E310 5024 0014		00000024	5700+	LGF	R1, V2ADDR	load v2 source
00007716	E761 0000 0806		00000000	5701+	VL	v22, 0(R1)	use v21 to test decoder
0000771C	E310 5028 0014		00000028	5702+	LGF	R1, V3ADDR	load v3 source
00007722	E771 0000 0806		00000000	5703+	VL	v23, 0(R1)	use v22 to test decoder
00007728	E756 7010 3EF9			5704+	VCHL	V21, V22, V23, 3, 1	test instruction
0000772E	B98D 0020			5705+	EPSW	R2, R0	extract psw
00007732	5020 500C		0000000C	5706+	ST	R2, CCPSW	to save CC
00007736	E750 5048 080E		000076F0	5707+	VST	V21, V10131	save v1 output
0000773C	07FB			5708+	BR	R11	return
00007740				5709+RE131	DC	0F	V1 for this test
00007740				5710+	DROP	R5	
00007740	00000000	00000000		5711	DC	XL16' 0000000000000000 0000000000000000'	result t
00007748	00000000	00000000					
00007750	00010003	04050607		5712	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00007758	00090A0B	0C0D0E0F					
00007760	01110233	11550677		5713	DC	XL16' 0111023311550677 119911BBF1DD11FF'	v3
00007768	119911BB	F1DD11FF					
				5714			
00007770				5715	VRR_B	VCHL, 3, 3	
00007770			00007770	5716+	DS	0FD	
00007770	000077D8			5717+	USING	*, R5	base for test data and test routine
00007774	0084			5718+T132	DC	A(X132)	address of test routine
00007776	00			5719+	DC	H' 132'	test number
00007776	00			5720+	DC	X' 00'	
00007777	03			5721+	DC	HL1' 3'	m4 used
00007778	01			5722+	DC	HL1' 1'	m5 used
00007779	03			5723+	DC	HL1' 3'	CC
0000777A	0E			5724+	DC	HL1' 14'	CC failed mask
0000777C	00000000	00000000		5725+	DS	2F	extracted PSW after test (has CC)
00007784	FF			5726+	DC	X' FF'	extracted CC, if test failed
00007785	E5C3C8D3	40404040		5727+	DC	CL8' VCHL'	instruction name
00007790	00007808			5728+	DC	A(RE132)	address of v1 result
00007794	00007818			5729+	DC	A(RE132+16)	address of v2 source
00007798	00007828			5730+	DC	A(RE132+32)	address of v3 source
0000779C	00000010			5731+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000077A0	00007808			5732+REA132	DC	A(RE132)	result address
000077A8	00000000 00000000			5733+	DS	2FD	gap
000077B0	00000000 00000000						
000077B8	00000000 00000000			5734+V10132	DS	XL16	V1 output
000077C0	00000000 00000000						
000077C8	00000000 00000000			5735+	DS	2FD	gap
000077D0	00000000 00000000						
				5736+*			
000077D8				5737+X132	DS	0F	
000077D8	E310 5024 0014		00000024	5738+	LGF	R1, V2ADDR	load v2 source
000077DE	E761 0000 0806		00000000	5739+	VL	v22, 0(R1)	use v21 to test decoder
000077E4	E310 5028 0014		00000028	5740+	LGF	R1, V3ADDR	load v3 source
000077EA	E771 0000 0806		00000000	5741+	VL	v23, 0(R1)	use v22 to test decoder
000077F0	E756 7010 3EF9			5742+	VCHL	V21, V22, V23, 3, 1	test instruction
000077F6	B98D 0020			5743+	EPSW	R2, R0	extract psw
000077FA	5020 500C		0000000C	5744+	ST	R2, CCPSW	to save CC
000077FE	E750 5048 080E		000077B8	5745+	VST	V21, V10132	save v1 output
00007804	07FB			5746+	BR	R11	return
00007808				5747+RE132	DC	0F	V1 for this test
00007808				5748+	DROP	R5	
00007808	00000000 00000000			5749	DC	XL16' 0000000000000000 0000000000000000'	result
00007810	00000000 00000000						
00007818	08090A0B 0C0D0E0F			5750	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00007820	00010203 04050607						
00007828	119911BB F1DD11FF			5751	DC	XL16' 119911BBF1DD11FF 0111023311550677'	v3
00007830	01110233 11550677						
				5752			
				5753 *			
				5754 * VCH		- Vector Compare High	
				5755 *			
				5756 *		cc=0: All elements high	
				5757 *		cc=1: Some elements high	
				5758 *		cc=3: No element high	
				5759 *			
				5760 *		case - simple cc debug	
				5761 *			
				5762 *		Byte	
				5763		VRR_B VCH, 0, 0	
00007838				5764+	DS	0FD	
00007838		00007838		5765+	USING	*, R5	base for test data and test routine
00007838	000078A0			5766+T133	DC	A(X133)	address of test routine
0000783C	0085			5767+	DC	H' 133'	test number
0000783E	00			5768+	DC	X' 00'	
0000783F	00			5769+	DC	HL1' 0'	m4 used
00007840	01			5770+	DC	HL1' 1'	m5 used
00007841	00			5771+	DC	HL1' 0'	CC
00007842	07			5772+	DC	HL1' 7'	CC failed mask
00007844	00000000 00000000			5773+	DS	2F	extracted PSW after test (has CC)
0000784C	FF			5774+	DC	X' FF'	extracted CC, if test failed
0000784D	E5C3C840 40404040			5775+	DC	CL8' VCH'	instruction name
00007858	000078D0			5776+	DC	A(RE133)	address of v1 result
0000785C	000078E0			5777+	DC	A(RE133+16)	address of v2 source
00007860	000078F0			5778+	DC	A(RE133+32)	address of v3 source
00007864	00000010			5779+	DC	A(16)	result length
00007868	000078D0			5780+REA133	DC	A(RE133)	result address
00007870	00000000 00000000			5781+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007878	00000000	00000000					
00007880	00000000	00000000		5782+V10133	DS	XL16	V1 output
00007888	00000000	00000000					
00007890	00000000	00000000		5783+	DS	2FD	gap
00007898	00000000	00000000					
000078A0				5784+*			
000078A0	E310 5024 0014		00000024	5785+X133	DS	0F	
000078A6	E761 0000 0806		00000000	5786+	LGF	R1, V2ADDR	load v2 source
000078AC	E310 5028 0014		00000028	5787+	VL	v22, 0(R1)	use v21 to test decoder
000078B2	E771 0000 0806		00000000	5788+	LGF	R1, V3ADDR	load v3 source
000078B8	E756 7010 0EFB		00000000	5789+	VL	v23, 0(R1)	use v22 to test decoder
000078BE	B98D 0020			5790+	VCH	V21, V22, V23, 0, 1	test instruction
000078C2	5020 500C		0000000C	5791+	EPSW	R2, R0	extract psw
000078C6	E750 5048 080E		00007880	5792+	ST	R2, CCPSW	to save CC
000078CC	07FB			5793+	VST	V21, V10133	save v1 output
000078D0				5794+	BR	R11	return
000078D0				5795+RE133	DC	0F	V1 for this test
000078D0	FFFFFFFF	FFFFFFFF		5796+	DROP	R5	
000078D8	FFFFFFFF	FFFFFFFF		5797	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000078E0	00000000	00000000		5798	DC	XL16' 0000000000000000 0000000000000000'	v2
000078E8	00000000	00000000					
000078F0	FFFFFFFF	FFFFFFFF		5799	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
000078F8	FFFFFFFF	FFFFFFFF					
00007900				5800			
00007900				5801	VRR_B	VCH, 0, 1	
00007900			00007900	5802+	DS	0FD	
00007900	00007968			5803+	USING	*, R5	base for test data and test routine
00007904	0086			5804+T134	DC	A(X134)	address of test routine
00007906	00			5805+	DC	H' 134'	test number
00007907	00			5806+	DC	X' 00'	
00007908	01			5807+	DC	HL1' 0'	m4 used
00007909	01			5808+	DC	HL1' 1'	m5 used
0000790A	0B			5809+	DC	HL1' 1'	CC
0000790C	00000000	00000000		5810+	DC	HL1' 11'	CC failed mask
00007914	FF			5811+	DS	2F	extracted PSW after test (has CC)
00007915	E5C3C840 40404040			5812+	DC	X' FF'	extracted CC, if test failed
00007920	00007998			5813+	DC	CL8' VCH'	instruction name
00007924	000079A8			5814+	DC	A(RE134)	address of v1 result
00007928	000079B8			5815+	DC	A(RE134+16)	address of v2 source
0000792C	00000010			5816+	DC	A(RE134+32)	address of v3 source
00007930	00007998			5817+	DC	A(16)	result length
00007938	00000000	00000000		5818+REA134	DC	A(RE134)	result address
00007940	00000000	00000000		5819+	DS	2FD	gap
00007948	00000000	00000000		5820+V10134	DS	XL16	V1 output
00007950	00000000	00000000					
00007958	00000000	00000000		5821+	DS	2FD	gap
00007960	00000000	00000000					
00007968				5822+*			
00007968	E310 5024 0014		00000024	5823+X134	DS	0F	
0000796E	E761 0000 0806		00000000	5824+	LGF	R1, V2ADDR	load v2 source
00007974	E310 5028 0014		00000028	5825+	VL	v22, 0(R1)	use v21 to test decoder
0000797A	E771 0000 0806		00000000	5826+	LGF	R1, V3ADDR	load v3 source
00007980	E756 7010 0EFB			5827+	VL	v23, 0(R1)	use v22 to test decoder
				5828+	VCH	V21, V22, V23, 0, 1	test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007986	B98D 0020			5829+	EPSW	R2, R0	extract psw
0000798A	5020 500C		0000000C	5830+	ST	R2, CCPSW	to save CC
0000798E	E750 5048 080E		00007948	5831+	VST	V21, V10134	save v1 output
00007994	07FB			5832+	BR	R11	return
00007998				5833+RE134	DC	0F	V1 for this test
00007998				5834+	DROP	R5	
00007998	00000000 00000000			5835	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result
000079A0	FFFFFFFF 00000000						
000079A8	00000000 00000000			5836	DC	XL16' 0000000000000000 7F017F0200000000'	v2
000079B0	7F017F02 00000000						
000079B8	00000000 00000000			5837	DC	XL16' 0000000000000000 0000000000000000'	v3
000079C0	00000000 00000000						
				5838			
				5839	VRR_B	VCH, 0, 3	
000079C8				5840+	DS	0FD	
000079C8		000079C8		5841+	USING	*, R5	base for test data and test routine
000079C8	00007A30			5842+T135	DC	A(X135)	address of test routine
000079CC	0087			5843+	DC	H' 135'	test number
000079CE	00			5844+	DC	X' 00'	
000079CF	00			5845+	DC	HL1' 0'	m4 used
000079D0	01			5846+	DC	HL1' 1'	m5 used
000079D1	03			5847+	DC	HL1' 3'	CC
000079D2	0E			5848+	DC	HL1' 14'	CC failed mask
000079D4	00000000 00000000			5849+	DS	2F	extracted PSW after test (has CC)
000079DC	FF			5850+	DC	X' FF'	extracted CC, if test failed
000079DD	E5C3C840 40404040			5851+	DC	CL8' VCH'	instruction name
000079E8	00007A60			5852+	DC	A(RE135)	address of v1 result
000079EC	00007A70			5853+	DC	A(RE135+16)	address of v2 source
000079F0	00007A80			5854+	DC	A(RE135+32)	address of v3 source
000079F4	00000010			5855+	DC	A(16)	result length
000079F8	00007A60			5856+REA135	DC	A(RE135)	result address
00007A00	00000000 00000000			5857+	DS	2FD	gap
00007A08	00000000 00000000						
00007A10	00000000 00000000			5858+V10135	DS	XL16	V1 output
00007A18	00000000 00000000						
00007A20	00000000 00000000			5859+	DS	2FD	gap
00007A28	00000000 00000000						
				5860+*			
00007A30				5861+X135	DS	0F	
00007A30	E310 5024 0014		00000024	5862+	LGF	R1, V2ADDR	load v2 source
00007A36	E761 0000 0806		00000000	5863+	VL	v22, 0(R1)	use v21 to test decoder
00007A3C	E310 5028 0014		00000028	5864+	LGF	R1, V3ADDR	load v3 source
00007A42	E771 0000 0806		00000000	5865+	VL	v23, 0(R1)	use v22 to test decoder
00007A48	E756 7010 0EFB			5866+	VCH	V21, V22, V23, 0, 1	test instruction
00007A4E	B98D 0020			5867+	EPSW	R2, R0	extract psw
00007A52	5020 500C		0000000C	5868+	ST	R2, CCPSW	to save CC
00007A56	E750 5048 080E		00007A10	5869+	VST	V21, V10135	save v1 output
00007A5C	07FB			5870+	BR	R11	return
00007A60				5871+RE135	DC	0F	V1 for this test
00007A60				5872+	DROP	R5	
00007A60	00000000 00000000			5873	DC	XL16' 0000000000000000 0000000000000000'	result
00007A68	00000000 00000000						
00007A70	00000000 00000000			5874	DC	XL16' 0000000000000000 0000000000000000'	v2
00007A78	00000000 00000000						
00007A80	00000000 00000000			5875	DC	XL16' 0000000000000000 0000000000000000'	v3
00007A88	00000000 00000000						



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				5876			
				5877	*Halfword		
00007A90				5878	VRR_B VCH, 1, 0		
00007A90		00007A90		5879+	DS 0FD		
00007A90	00007AF8			5880+	USING *, R5	base for test data and test routine	
00007A94	0088			5881+T136	DC A(X136)	address of test routine	
00007A96	00			5882+	DC H' 136'	test number	
00007A97	01			5883+	DC X' 00'		
00007A98	01			5884+	DC HL1' 1'	m4 used	
00007A98	01			5885+	DC HL1' 1'	m5 used	
00007A99	00			5886+	DC HL1' 0'	CC	
00007A9A	07			5887+	DC HL1' 7'	CC failed mask	
00007A9C	00000000 00000000			5888+	DS 2F	extracted PSW after test (has CC)	
00007AA4	FF			5889+	DC X' FF'	extracted CC, if test failed	
00007AA5	E5C3C840 40404040			5890+	DC CL8' VCH'	instruction name	
00007AB0	00007B28			5891+	DC A(RE136)	address of v1 result	
00007AB4	00007B38			5892+	DC A(RE136+16)	address of v2 source	
00007AB8	00007B48			5893+	DC A(RE136+32)	address of v3 source	
00007ABC	00000010			5894+	DC A(16)	result length	
00007AC0	00007B28			5895+REA136	DC A(RE136)	result address	
00007AC8	00000000 00000000			5896+	DS 2FD	gap	
00007AD0	00000000 00000000						
00007AD8	00000000 00000000			5897+V10136	DS XL16	V1 output	
00007AE0	00000000 00000000						
00007AE8	00000000 00000000			5898+	DS 2FD	gap	
00007AF0	00000000 00000000						
				5899+*			
00007AF8				5900+X136	DS 0F		
00007AF8	E310 5024 0014		00000024	5901+	LGF R1, V2ADDR	load v2 source	
00007AFE	E761 0000 0806		00000000	5902+	VL v22, 0(R1)	use v21 to test decoder	
00007B04	E310 5028 0014		00000028	5903+	LGF R1, V3ADDR	load v3 source	
00007B0A	E771 0000 0806		00000000	5904+	VL v23, 0(R1)	use v22 to test decoder	
00007B10	E756 7010 1EFB			5905+	VCH V21, V22, V23, 1, 1	test instruction	
00007B16	B98D 0020			5906+	EPSW R2, R0	extract psw	
00007B1A	5020 500C		0000000C	5907+	ST R2, CCPSW	to save CC	
00007B1E	E750 5048 080E		00007AD8	5908+	VST V21, V10136	save v1 output	
00007B24	07FB			5909+	BR R11	return	
00007B28				5910+RE136	DC 0F	V1 for this test	
00007B28				5911+	DROP R5		
00007B28	FFFFFFFF FFFFFFFF			5912	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00007B30	FFFFFFFF FFFFFFFF						
00007B38	00000000 00000000			5913	DC XL16' 0000000000000000 0000000000000000'	v2	
00007B40	00000000 00000000						
00007B48	FFFFFFFF FFFFFFFF			5914	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3	
00007B50	FFFFFFFF FFFFFFFF						
				5915			
00007B58				5916	VRR_B VCH, 1, 1		
00007B58		00007B58		5917+	DS 0FD		
00007B58	00007BC0			5918+	USING *, R5	base for test data and test routine	
00007B5C	0089			5919+T137	DC A(X137)	address of test routine	
00007B5E	00			5920+	DC H' 137'	test number	
00007B5F	01			5921+	DC X' 00'		
00007B60	01			5922+	DC HL1' 1'	m4 used	
00007B60	01			5923+	DC HL1' 1'	m5 used	
00007B61	01			5924+	DC HL1' 1'	CC	
00007B62	0B			5925+	DC HL1' 11'	CC failed mask	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007B64	00000000 00000000			5926+	DS	2F	extracted PSW after test (has CC)
00007B6C	FF			5927+	DC	X' FF'	extracted CC, if test failed
00007B6D	E5C3C840 40404040			5928+	DC	CL8' VCH'	instruction name
00007B78	00007BF0			5929+	DC	A(RE137)	address of v1 result
00007B7C	00007C00			5930+	DC	A(RE137+16)	address of v2 source
00007B80	00007C10			5931+	DC	A(RE137+32)	address of v3 source
00007B84	00000010			5932+	DC	A(16)	result length
00007B88	00007BF0			5933+REA137	DC	A(RE137)	result address
00007B90	00000000 00000000			5934+	DS	2FD	gap
00007B98	00000000 00000000						
00007BA0	00000000 00000000			5935+V10137	DS	XL16	V1 output
00007BA8	00000000 00000000						
00007BB0	00000000 00000000			5936+	DS	2FD	gap
00007BB8	00000000 00000000						
00007BC0				5937+*			
00007BC0	E310 5024 0014		00000024	5938+X137	DS	0F	
00007BC6	E761 0000 0806		00000000	5939+	LGF	R1, V2ADDR	load v2 source
00007BCC	E310 5028 0014		00000028	5940+	VL	v22, 0(R1)	use v21 to test decoder
00007BD2	E771 0000 0806		00000000	5941+	LGF	R1, V3ADDR	load v3 source
00007BD8	E756 7010 1EFB		00000000	5942+	VL	v23, 0(R1)	use v22 to test decoder
00007BDE	B98D 0020			5943+	VCH	V21, V22, V23, 1, 1	test instruction
00007BDE	B98D 0020			5944+	EPSW	R2, R0	extract psw
00007BE2	5020 500C		0000000C	5945+	ST	R2, CCPSW	to save CC
00007BE6	E750 5048 080E		00007BA0	5946+	VST	V21, V10137	save v1 output
00007BEC	07FB			5947+	BR	R11	return
00007BF0				5948+RE137	DC	0F	V1 for this test
00007BF0				5949+	DROP	R5	
00007BF0	00000000 00000000			5950	DC	XL16' 0000000000000000 00000000'	result
00007BF8	FFFFFFFF 00000000						
00007C00	00000000 00000000			5951	DC	XL16' 0000000000000000 7F017F0200000000'	v2
00007C08	7F017F02 00000000						
00007C10	00000000 00000000			5952	DC	XL16' 0000000000000000 0000000000000000'	v3
00007C18	00000000 00000000						
00007C20				5953			
00007C20				5954	VRR_B	VCH, 1, 3	
00007C20		00007C20		5955+	DS	0FD	
00007C20	00007C88			5956+	USING	*, R5	base for test data and test routine
00007C24	008A			5957+T138	DC	A(X138)	address of test routine
00007C26	00			5958+	DC	H' 138'	test number
00007C27	01			5959+	DC	X' 00'	
00007C28	01			5960+	DC	HL1' 1'	m4 used
00007C28	01			5961+	DC	HL1' 1'	m5 used
00007C29	03			5962+	DC	HL1' 3'	CC
00007C2A	0E			5963+	DC	HL1' 14'	CC failed mask
00007C2C	00000000 00000000			5964+	DS	2F	extracted PSW after test (has CC)
00007C34	FF			5965+	DC	X' FF'	extracted CC, if test failed
00007C35	E5C3C840 40404040			5966+	DC	CL8' VCH'	instruction name
00007C40	00007CB8			5967+	DC	A(RE138)	address of v1 result
00007C44	00007CC8			5968+	DC	A(RE138+16)	address of v2 source
00007C48	00007CD8			5969+	DC	A(RE138+32)	address of v3 source
00007C4C	00000010			5970+	DC	A(16)	result length
00007C50	00007CB8			5971+REA138	DC	A(RE138)	result address
00007C58	00000000 00000000			5972+	DS	2FD	gap
00007C60	00000000 00000000						
00007C68	00000000 00000000			5973+V10138	DS	XL16	V1 output
00007C70	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007C78	00000000 00000000			5974+	DS	2FD	gap
00007C80	00000000 00000000						
00007C88				5975+*			
00007C88	E310 5024 0014		00000024	5976+X138	DS	0F	
00007C8E	E761 0000 0806		00000000	5977+	LGF	R1, V2ADDR	load v2 source
00007C94	E310 5028 0014		00000028	5978+	VL	v22, 0(R1)	use v21 to test decoder
00007C9A	E771 0000 0806		00000000	5979+	LGF	R1, V3ADDR	load v3 source
00007CA0	E756 7010 1EFB			5980+	VL	v23, 0(R1)	use v22 to test decoder
00007CA6	B98D 0020			5981+	VCH	V21, V22, V23, 1, 1	test instruction
00007CAA	5020 500C		0000000C	5982+	EPSW	R2, R0	extract psw
00007CAE	E750 5048 080E		00007C68	5983+	ST	R2, CCPSW	to save CC
00007CB4	07FB			5984+	VST	V21, V10138	save v1 output
00007CB8				5985+	BR	R11	return
00007CB8				5986+RE138	DC	0F	V1 for this test
00007CB8	00000000 00000000			5987+	DROP	R5	
00007CC0	00000000 00000000			5988	DC	XL16' 0000000000000000 0000000000000000'	result t
00007CC8	00000000 00000000			5989	DC	XL16' 0000000000000000 0000000000000000'	v2
00007CD0	00000000 00000000						
00007CD8	00000000 00000000			5990	DC	XL16' 0000000000000000 0000000000000000'	v3
00007CE0	00000000 00000000						
				5991			
				5992 *Word			
00007CE8				5993	VRR_B	VCH, 2, 0	
00007CE8		00007CE8		5994+	DS	0FD	
00007CE8	00007D50			5995+	USING	*, R5	base for test data and test routine
00007CEC	008B			5996+T139	DC	A(X139)	address of test routine
00007CEE	00			5997+	DC	H' 139'	test number
00007CEF	02			5998+	DC	X' 00'	
00007CF0	01			5999+	DC	HL1' 2'	m4 used
00007CF1	00			6000+	DC	HL1' 1'	m5 used
00007CF2	07			6001+	DC	HL1' 0'	CC
00007CF4	00000000 00000000			6002+	DC	HL1' 7'	CC failed mask
00007CFC	FF			6003+	DS	2F	extracted PSW after test (has CC)
00007CFD	E5C3C840 40404040			6004+	DC	X' FF'	extracted CC, if test failed
00007D08	00007D80			6005+	DC	CL8' VCH'	instruction name
00007D0C	00007D90			6006+	DC	A(RE139)	address of v1 result
00007D10	00007DA0			6007+	DC	A(RE139+16)	address of v2 source
00007D14	00000010			6008+	DC	A(RE139+32)	address of v3 source
00007D18	00007D80			6009+	DC	A(16)	result length
00007D20	00000000 00000000			6010+REA139	DC	A(RE139)	result address
00007D28	00000000 00000000			6011+	DS	2FD	gap
00007D30	00000000 00000000			6012+V10139	DS	XL16	V1 output
00007D38	00000000 00000000						
00007D40	00000000 00000000			6013+	DS	2FD	gap
00007D48	00000000 00000000						
				6014+*			
00007D50				6015+X139	DS	0F	
00007D50	E310 5024 0014		00000024	6016+	LGF	R1, V2ADDR	load v2 source
00007D56	E761 0000 0806		00000000	6017+	VL	v22, 0(R1)	use v21 to test decoder
00007D5C	E310 5028 0014		00000028	6018+	LGF	R1, V3ADDR	load v3 source
00007D62	E771 0000 0806		00000000	6019+	VL	v23, 0(R1)	use v22 to test decoder
00007D68	E756 7010 2EFB			6020+	VCH	V21, V22, V23, 2, 1	test instruction
00007D6E	B98D 0020			6021+	EPSW	R2, R0	extract psw
00007D72	5020 500C		0000000C	6022+	ST	R2, CCPSW	to save CC

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00007D76	E750 5048 080E		00007D30	6023+	VST	V21, V10139	save v1 output	
00007D7C	07FB			6024+	BR	R11	return	
00007D80				6025+RE139	DC	0F	V1 for this test	
00007D80				6026+	DROP	R5		
00007D80	FFFFFFFF FFFFFFFF			6027	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00007D88	FFFFFFFF FFFFFFFF							
00007D90	00000000 00000000			6028	DC	XL16' 0000000000000000 0000000000000000'	v2	
00007D98	00000000 00000000							
00007DA0	FFFFFFFF FFFFFFFF			6029	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3	
00007DA8	FFFFFFFF FFFFFFFF							
				6030				
00007DB0				6031	VRR_B	VCH, 2, 1		
00007DB0		00007DB0		6032+	DS	0FD		
00007DB0	00007E18			6033+	USING	*, R5	base for test data and test routine	
00007DB4	008C			6034+T140	DC	A(X140)	address of test routine	
00007DB6	00			6035+	DC	H' 140'	test number	
00007DB7	02			6036+	DC	X' 00'		
00007DB8	01			6037+	DC	HL1' 2'	m4 used	
00007DB8	01			6038+	DC	HL1' 1'	m5 used	
00007DB9	01			6039+	DC	HL1' 1'	CC	
00007DBA	0B			6040+	DC	HL1' 11'	CC failed mask	
00007DBC	00000000 00000000			6041+	DS	2F	extracted PSW after test (has CC)	
00007DC4	FF			6042+	DC	X' FF'	extracted CC, if test failed	
00007DC5	E5C3C840 40404040			6043+	DC	CL8' VCH'	instruction name	
00007DD0	00007E48			6044+	DC	A(RE140)	address of v1 result	
00007DD4	00007E58			6045+	DC	A(RE140+16)	address of v2 source	
00007DD8	00007E68			6046+	DC	A(RE140+32)	address of v3 source	
00007DDC	00000010			6047+	DC	A(16)	result length	
00007DE0	00007E48			6048+REA140	DC	A(RE140)	result address	
00007DE8	00000000 00000000			6049+	DS	2FD	gap	
00007DF0	00000000 00000000							
00007DF8	00000000 00000000			6050+V10140	DS	XL16	V1 output	
00007E00	00000000 00000000							
00007E08	00000000 00000000			6051+	DS	2FD	gap	
00007E10	00000000 00000000							
				6052+*				
00007E18				6053+X140	DS	0F		
00007E18	E310 5024 0014		00000024	6054+	LGF	R1, V2ADDR	load v2 source	
00007E1E	E761 0000 0806		00000000	6055+	VL	v22, 0(R1)	use v21 to test decoder	
00007E24	E310 5028 0014		00000028	6056+	LGF	R1, V3ADDR	load v3 source	
00007E2A	E771 0000 0806		00000000	6057+	VL	v23, 0(R1)	use v22 to test decoder	
00007E30	E756 7010 2EFB			6058+	VCH	V21, V22, V23, 2, 1	test instruction	
00007E36	B98D 0020			6059+	EPSW	R2, R0	extract psw	
00007E3A	5020 500C		0000000C	6060+	ST	R2, CCPSW	to save CC	
00007E3E	E750 5048 080E		00007DF8	6061+	VST	V21, V10140	save v1 output	
00007E44	07FB			6062+	BR	R11	return	
00007E48				6063+RE140	DC	0F	V1 for this test	
00007E48				6064+	DROP	R5		
00007E48	00000000 00000000			6065	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result t	
00007E50	FFFFFFFF 00000000							
00007E58	00000000 00000000			6066	DC	XL16' 0000000000000000 7F017F0200000000'	v2	
00007E60	7F017F02 00000000							
00007E68	00000000 00000000			6067	DC	XL16' 0000000000000000 0000000000000000'	v3	
00007E70	00000000 00000000							
				6068				
				6069	VRR_B	VCH, 2, 3		



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007E78				6070+	DS	0FD	
00007E78		00007E78		6071+	USING	*, R5	base for test data and test routine
00007E78	00007EE0			6072+T141	DC	A(X141)	address of test routine
00007E7C	008D			6073+	DC	H' 141'	test number
00007E7E	00			6074+	DC	X' 00'	
00007E7F	02			6075+	DC	HL1' 2'	m4 used
00007E80	01			6076+	DC	HL1' 1'	m5 used
00007E81	03			6077+	DC	HL1' 3'	CC
00007E82	0E			6078+	DC	HL1' 14'	CC failed mask
00007E84	00000000 00000000			6079+	DS	2F	extracted PSW after test (has CC)
00007E8C	FF			6080+	DC	X' FF'	extracted CC, if test failed
00007E8D	E5C3C840 40404040			6081+	DC	CL8' VCH'	instruction name
00007E98	00007F10			6082+	DC	A(RE141)	address of v1 result
00007E9C	00007F20			6083+	DC	A(RE141+16)	address of v2 source
00007EA0	00007F30			6084+	DC	A(RE141+32)	address of v3 source
00007EA4	00000010			6085+	DC	A(16)	result length
00007EA8	00007F10			6086+REA141	DC	A(RE141)	result address
00007EB0	00000000 00000000			6087+	DS	2FD	gap
00007EB8	00000000 00000000						
00007EC0	00000000 00000000			6088+V10141	DS	XL16	V1 output
00007EC8	00000000 00000000						
00007ED0	00000000 00000000			6089+	DS	2FD	gap
00007ED8	00000000 00000000						
00007EE0				6090+*			
00007EE0	E310 5024 0014		00000024	6091+X141	DS	0F	
00007EE6	E761 0000 0806		00000000	6092+	LGF	R1, V2ADDR	load v2 source
00007EEC	E310 5028 0014		00000028	6093+	VL	v22, 0(R1)	use v21 to test decoder
00007EF2	E771 0000 0806		00000000	6094+	LGF	R1, V3ADDR	load v3 source
00007EF8	E756 7010 2EFB			6095+	VL	v23, 0(R1)	use v22 to test decoder
00007EFE	B98D 0020			6096+	VCH	V21, V22, V23, 2, 1	test instruction
00007F02	5020 500C		0000000C	6097+	EPSW	R2, R0	extract psw
00007F06	E750 5048 080E		00007EC0	6098+	ST	R2, CCPSW	to save CC
00007F0C	07FB			6099+	VST	V21, V10141	save v1 output
00007F10				6100+	BR	R11	return
00007F10				6101+RE141	DC	0F	V1 for this test
00007F10				6102+	DROP	R5	
00007F10	00000000 00000000			6103	DC	XL16' 0000000000000000 0000000000000000'	result
00007F18	00000000 00000000						
00007F20	00000000 00000000			6104	DC	XL16' 0000000000000000 0000000000000000'	v2
00007F28	00000000 00000000						
00007F30	00000000 00000000			6105	DC	XL16' 0000000000000000 0000000000000000'	v3
00007F38	00000000 00000000						
00007F40				6106			
00007F40				6107 *Doubleword			
00007F40	00007FA8	00007F40		6108	VRR_B	VCH, 3, 0	
00007F44	008E			6109+	DS	0FD	
00007F46	00			6110+	USING	*, R5	base for test data and test routine
00007F47	03			6111+T142	DC	A(X142)	address of test routine
00007F48	01			6112+	DC	H' 142'	test number
00007F49	00			6113+	DC	X' 00'	
00007F4A	07			6114+	DC	HL1' 3'	m4 used
00007F4C	00000000 00000000			6115+	DC	HL1' 1'	m5 used
00007F54	FF			6116+	DC	HL1' 0'	CC
				6117+	DC	HL1' 7'	CC failed mask
				6118+	DS	2F	extracted PSW after test (has CC)
				6119+	DC	X' FF'	extracted CC, if test failed

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007F55	E5C3C840 40404040			6120+	DC	CL8' VCH'	instruction name
00007F60	00007FD8			6121+	DC	A(RE142)	address of v1 result
00007F64	00007FE8			6122+	DC	A(RE142+16)	address of v2 source
00007F68	00007FF8			6123+	DC	A(RE142+32)	address of v3 source
00007F6C	00000010			6124+	DC	A(16)	result length
00007F70	00007FD8			6125+REA142	DC	A(RE142)	result address
00007F78	00000000 00000000			6126+	DS	2FD	gap
00007F80	00000000 00000000						
00007F88	00000000 00000000			6127+V10142	DS	XL16	V1 output
00007F90	00000000 00000000						
00007F98	00000000 00000000			6128+	DS	2FD	gap
00007FA0	00000000 00000000						
00007FA8				6129+*			
00007FA8	E310 5024 0014		00000024	6130+X142	DS	0F	
00007FAE	E761 0000 0806		00000000	6131+	LGF	R1, V2ADDR	load v2 source
00007FB4	E310 5028 0014		00000028	6132+	VL	v22, 0(R1)	use v21 to test decoder
00007FBA	E771 0000 0806		00000000	6133+	LGF	R1, V3ADDR	load v3 source
00007FC0	E756 7010 3EFB			6134+	VL	v23, 0(R1)	use v22 to test decoder
00007FC6	B98D 0020			6135+	VCH	V21, V22, V23, 3, 1	test instruction
00007FCA	5020 500C		0000000C	6136+	EPSW	R2, R0	extract psw
00007FCE	E750 5048 080E		00007F88	6137+	ST	R2, CCPSW	to save CC
00007FD4	07FB			6138+	VST	V21, V10142	save v1 output
00007FD8				6139+	BR	R11	return
00007FD8				6140+RE142	DC	0F	V1 for this test
00007FD8				6141+	DROP	R5	
00007FD8	FFFFFFFF FFFFFFFF			6142	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00007FE0	FFFFFFFF FFFFFFFF						
00007FE8	00000000 00000000			6143	DC	XL16' 0000000000000000 0000000000000000'	v2
00007FF0	00000000 00000000						
00007FF8	FFFFFFFF FFFFFFFF			6144	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00008000	FFFFFFFF FFFFFFFF						
00008008				6145			
00008008				6146	VRR_B	VCH, 3, 1	
00008008		00008008		6147+	DS	0FD	
00008008	00008070			6148+	USING	*, R5	base for test data and test routine
0000800C	008F			6149+T143	DC	A(X143)	address of test routine
0000800E	00			6150+	DC	H' 143'	test number
0000800F	03			6151+	DC	X' 00'	
00008010	01			6152+	DC	HL1' 3'	m4 used
00008011	01			6153+	DC	HL1' 1'	m5 used
00008012	0B			6154+	DC	HL1' 1'	CC
00008014	00000000 00000000			6155+	DC	HL1' 11'	CC failed mask
0000801C	FF			6156+	DS	2F	extracted PSW after test (has CC)
0000801D	E5C3C840 40404040			6157+	DC	X' FF'	extracted CC, if test failed
00008028	000080A0			6158+	DC	CL8' VCH'	instruction name
0000802C	000080B0			6159+	DC	A(RE143)	address of v1 result
00008030	000080C0			6160+	DC	A(RE143+16)	address of v2 source
00008034	00000010			6161+	DC	A(RE143+32)	address of v3 source
00008038	000080A0			6162+	DC	A(16)	result length
00008040	00000000 00000000			6163+REA143	DC	A(RE143)	result address
00008048	00000000 00000000			6164+	DS	2FD	gap
00008050	00000000 00000000			6165+V10143	DS	XL16	V1 output
00008058	00000000 00000000						
00008060	00000000 00000000			6166+	DS	2FD	gap
00008068	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008070				6167+*			
00008070	E310 5024 0014		00000024	6168+X143	DS	0F	
00008076	E761 0000 0806		00000000	6169+	LGF	R1, V2ADDR	load v2 source
0000807C	E310 5028 0014		00000028	6170+	VL	v22, 0(R1)	use v21 to test decoder
00008082	E771 0000 0806		00000000	6171+	LGF	R1, V3ADDR	load v3 source
00008088	E756 7010 3EFB		00000000	6172+	VL	v23, 0(R1)	use v22 to test decoder
0000808E	B98D 0020			6173+	VCH	V21, V22, V23, 3, 1	test instruction
00008092	5020 500C		0000000C	6174+	EPSW	R2, R0	extract psw
00008096	E750 5048 080E		00008050	6175+	ST	R2, CCPSW	to save CC
0000809C	07FB			6176+	VST	V21, V10143	save v1 output
000080A0				6177+	BR	R11	return
000080A0				6178+RE143	DC	0F	V1 for this test
000080A0				6179+	DROP	R5	
000080A0	00000000 00000000			6180	DC	XL16' 0000000000000000 FFFFFFFF'	result
000080A8	FFFFFFFF FFFFFFFF						
000080B0	00000000 00000000			6181	DC	XL16' 0000000000000000 7F017F0200000000'	v2
000080B8	7F017F02 00000000						
000080C0	00000000 00000000			6182	DC	XL16' 0000000000000000 0000000000000000'	v3
000080C8	00000000 00000000						
000080D0				6183			
000080D0		000080D0		6184	VRR_B	VCH, 3, 3	
000080D0	00008138			6185+	DS	0FD	
000080D4	0090			6186+	USING	*, R5	base for test data and test routine
000080D6	00			6187+T144	DC	A(X144)	address of test routine
000080D7	03			6188+	DC	H' 144'	test number
000080D8	01			6189+	DC	X' 00'	
000080D9	03			6190+	DC	HL1' 3'	m4 used
000080DA	0E			6191+	DC	HL1' 1'	m5 used
000080DC	00000000 00000000			6192+	DC	HL1' 3'	CC
000080E4	FF			6193+	DC	HL1' 14'	CC failed mask
000080E5	E5C3C840 40404040			6194+	DS	2F	extracted PSW after test (has CC)
000080F0	00008168			6195+	DC	X' FF'	extracted CC, if test failed
000080F4	00008178			6196+	DC	CL8' VCH'	instruction name
000080F8	00008188			6197+	DC	A(RE144)	address of v1 result
000080FC	00000010			6198+	DC	A(RE144+16)	address of v2 source
00008100	00008168			6199+	DC	A(RE144+32)	address of v3 source
00008108	00000000 00000000			6200+	DC	A(16)	result length
00008110	00000000 00000000			6201+REA144	DC	A(RE144)	result address
00008118	00000000 00000000			6202+	DS	2FD	gap
00008120	00000000 00000000			6203+V10144	DS	XL16	V1 output
00008128	00000000 00000000			6204+	DS	2FD	gap
00008130	00000000 00000000						
00008138				6205+*			
00008138	E310 5024 0014		00000024	6206+X144	DS	0F	
0000813E	E761 0000 0806		00000000	6207+	LGF	R1, V2ADDR	load v2 source
00008144	E310 5028 0014		00000028	6208+	VL	v22, 0(R1)	use v21 to test decoder
0000814A	E771 0000 0806		00000000	6209+	LGF	R1, V3ADDR	load v3 source
00008150	E756 7010 3EFB		00000000	6210+	VL	v23, 0(R1)	use v22 to test decoder
00008156	B98D 0020			6211+	VCH	V21, V22, V23, 3, 1	test instruction
0000815A	5020 500C		0000000C	6212+	EPSW	R2, R0	extract psw
0000815E	E750 5048 080E		00008118	6213+	ST	R2, CCPSW	to save CC
00008164	07FB			6214+	VST	V21, V10144	save v1 output
00008168				6215+	BR	R11	return
				6216+RE144	DC	0F	V1 for this test

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008168				6217+	DROP	R5	
00008168	00000000 00000000			6218	DC	XL16' 0000000000000000 0000000000000000'	result t
00008170	00000000 00000000						
00008178	00000000 00000000			6219	DC	XL16' 0000000000000000 0000000000000000'	v2
00008180	00000000 00000000						
00008188	00000000 00000000			6220	DC	XL16' 0000000000000000 0000000000000000'	v3
00008190	00000000 00000000						
				6221			
				6222	*-----		
				6223	* case - general		
				6224	*-----		
				6225	*Byte		
00008198				6226	VRR_B	VCH, 0, 0	
00008198		00008198		6227+	DS	0FD	
00008198	00008200			6228+	USING	*, R5	base for test data and test routine
0000819C	0091			6229+T145	DC	A(X145)	address of test routine
0000819E	00			6230+	DC	H' 145'	test number
0000819F	00			6231+	DC	X' 00'	
000081A0	01			6232+	DC	HL1' 0'	m4 used
000081A1	00			6233+	DC	HL1' 1'	m5 used
000081A2	07			6234+	DC	HL1' 0'	CC
000081A4	00000000 00000000			6235+	DC	HL1' 7'	CC failed mask
000081AC	FF			6236+	DS	2F	extracted PSW after test (has CC)
000081AD	E5C3C840 40404040			6237+	DC	X' FF'	extracted CC, if test failed
000081B8	00008230			6238+	DC	CL8' VCH'	instruction name
000081BC	00008240			6239+	DC	A(RE145)	address of v1 result
000081C0	00008250			6240+	DC	A(RE145+16)	address of v2 source
000081C4	00000010			6241+	DC	A(RE145+32)	address of v3 source
000081C8	00008230			6242+	DC	A(16)	result length
000081D0	00000000 00000000			6243+REA145	DC	A(RE145)	result address
000081D8	00000000 00000000			6244+	DS	2FD	gap
000081E0	00000000 00000000			6245+V10145	DS	XL16	V1 output
000081E8	00000000 00000000						
000081F0	00000000 00000000			6246+	DS	2FD	gap
000081F8	00000000 00000000						
				6247+*			
00008200				6248+X145	DS	0F	
00008200	E310 5024 0014	00000024		6249+	LGF	R1, V2ADDR	load v2 source
00008206	E761 0000 0806	00000000		6250+	VL	v22, 0(R1)	use v21 to test decoder
0000820C	E310 5028 0014	00000028		6251+	LGF	R1, V3ADDR	load v3 source
00008212	E771 0000 0806	00000000		6252+	VL	v23, 0(R1)	use v22 to test decoder
00008218	E756 7010 0EFB			6253+	VCH	V21, V22, V23, 0, 1	test instruction
0000821E	B98D 0020			6254+	EPSW	R2, R0	extract psw
00008222	5020 500C	0000000C		6255+	ST	R2, CCPSW	to save CC
00008226	E750 5048 080E	000081E0		6256+	VST	V21, V10145	save v1 output
0000822C	07FB			6257+	BR	R11	return
00008230				6258+RE145	DC	0F	V1 for this test
00008230				6259+	DROP	R5	
00008230	FFFFFFFF FFFFFFFF			6260	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00008238	FFFFFFFF FFFFFFFF						
00008240	01020304 05060708			6261	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
00008248	090A0B0C 0D0E0F10						
00008250	00010203 04050607			6262	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00008258	08090A0B 0C0D0E0F						
				6263			



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008260				6264	VRR_B	VCH, 0, 0	
00008260				6265+	DS	0FD	
00008260		00008260		6266+	USING	*, R5	base for test data and test routine
00008260	000082C8			6267+T146	DC	A(X146)	address of test routine
00008264	0092			6268+	DC	H' 146'	test number
00008266	00			6269+	DC	X' 00'	
00008267	00			6270+	DC	HL1' 0'	m4 used
00008268	01			6271+	DC	HL1' 1'	m5 used
00008269	00			6272+	DC	HL1' 0'	CC
0000826A	07			6273+	DC	HL1' 7'	CC failed mask
0000826C	00000000 00000000			6274+	DS	2F	extracted PSW after test (has CC)
00008274	FF			6275+	DC	X' FF'	extracted CC, if test failed
00008275	E5C3C840 40404040			6276+	DC	CL8' VCH'	instruction name
00008280	000082F8			6277+	DC	A(RE146)	address of v1 result
00008284	00008308			6278+	DC	A(RE146+16)	address of v2 source
00008288	00008318			6279+	DC	A(RE146+32)	address of v3 source
0000828C	00000010			6280+	DC	A(16)	result length
00008290	000082F8			6281+REA146	DC	A(RE146)	result address
00008298	00000000 00000000			6282+	DS	2FD	gap
000082A0	00000000 00000000						
000082A8	00000000 00000000			6283+V10146	DS	XL16	V1 output
000082B0	00000000 00000000						
000082B8	00000000 00000000			6284+	DS	2FD	gap
000082C0	00000000 00000000						
000082C8				6285+*			
000082C8	E310 5024 0014			6286+X146	DS	0F	
000082CE	E761 0000 0806	00000024		6287+	LGF	R1, V2ADDR	load v2 source
000082D4	E310 5028 0014	00000000		6288+	VL	v22, 0(R1)	use v21 to test decoder
000082DA	E771 0000 0806	00000028		6289+	LGF	R1, V3ADDR	load v3 source
000082E0	E756 7010 0EFB	00000000		6290+	VL	v23, 0(R1)	use v22 to test decoder
000082E6	B98D 0020			6291+	VCH	V21, V22, V23, 0, 1	test instruction
000082EA	5020 500C	0000000C		6292+	EPSW	R2, R0	extract psw
000082EE	E750 5048 080E	000082A8		6293+	ST	R2, CCPSW	to save CC
000082F4	07FB			6294+	VST	V21, V10146	save v1 output
000082F8				6295+	BR	R11	return
000082F8				6296+RE146	DC	0F	V1 for this test
000082F8				6297+	DROP	R5	
000082F8	FFFFFFFF FFFFFFFF			6298	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00008300	FFFFFFFF FFFFFFFF						
00008308	00010203 04050607			6299	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00008310	08090A0B 0C0D0E0F						
00008318	FFFEFFFD FFFCFFFB			6300	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00008320	FFFAFF9 FFF8FFF7						
00008328				6301			
00008328		00008328		6302	VRR_B	VCH, 0, 1	
00008328	00008390			6303+	DS	0FD	
0000832C	0093			6304+	USING	*, R5	base for test data and test routine
0000832E	00			6305+T147	DC	A(X147)	address of test routine
0000832F	00			6306+	DC	H' 147'	test number
00008330	01			6307+	DC	X' 00'	
00008330	01			6308+	DC	HL1' 0'	m4 used
00008331	01			6309+	DC	HL1' 1'	m5 used
00008331	01			6310+	DC	HL1' 1'	CC
00008332	0B			6311+	DC	HL1' 11'	CC failed mask
00008334	00000000 00000000			6312+	DS	2F	extracted PSW after test (has CC)
0000833C	FF			6313+	DC	X' FF'	extracted CC, if test failed

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000833D	E5C3C840 40404040			6314+	DC	CL8' VCH'	instruction name
00008348	000083C0			6315+	DC	A(RE147)	address of v1 result
0000834C	000083D0			6316+	DC	A(RE147+16)	address of v2 source
00008350	000083E0			6317+	DC	A(RE147+32)	address of v3 source
00008354	00000010			6318+	DC	A(16)	result length
00008358	000083C0			6319+REA147	DC	A(RE147)	result address
00008360	00000000 00000000			6320+	DS	2FD	gap
00008368	00000000 00000000						
00008370	00000000 00000000			6321+V10147	DS	XL16	V1 output
00008378	00000000 00000000						
00008380	00000000 00000000			6322+	DS	2FD	gap
00008388	00000000 00000000						
00008390				6323+*			
00008390	E310 5024 0014		00000024	6324+X147	DS	0F	
00008396	E761 0000 0806		00000000	6325+	LGF	R1, V2ADDR	load v2 source
0000839C	E310 5028 0014		00000028	6326+	VL	v22, 0(R1)	use v21 to test decoder
000083A2	E771 0000 0806		00000000	6327+	LGF	R1, V3ADDR	load v3 source
000083A8	E756 7010 0EFB			6328+	VL	v23, 0(R1)	use v22 to test decoder
000083AE	B98D 0020			6329+	VCH	V21, V22, V23, 0, 1	test instruction
000083B2	5020 500C		0000000C	6330+	EPSW	R2, R0	extract psw
000083B6	E750 5048 080E		00008370	6331+	ST	R2, CCPSW	to save CC
000083BC	07FB			6332+	VST	V21, V10147	save v1 output
000083C0				6333+	BR	R11	return
000083C0				6334+RE147	DC	0F	V1 for this test
000083C0				6335+	DROP	R5	
000083C0	00FF00FF 00FF00FF			6336	DC	XL16' 00FF00FF00FF00FF 00000000000000FF'	result
000083C8	00000000 000000FF						
000083D0	00110033 00550077			6337	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'	v2
000083D8	08090A0B 0C0DFE1F						
000083E0	00010203 04050607			6338	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v3
000083E8	08090A0B 0C0DFE0F						
000083F0				6339			
000083F0		000083F0		6340	VRR_B	VCH, 0, 1	
000083F0	00008458			6341+	DS	0FD	
000083F4	0094			6342+	USING	*, R5	base for test data and test routine
000083F6	00			6343+T148	DC	A(X148)	address of test routine
000083F7	00			6344+	DC	H' 148'	test number
000083F8	01			6345+	DC	X' 00'	
000083F9	01			6346+	DC	HL1' 0'	m4 used
000083FA	0B			6347+	DC	HL1' 1'	m5 used
000083FC	00000000 00000000			6348+	DC	HL1' 1'	CC
00008404	FF			6349+	DC	HL1' 11'	CC failed mask
00008405	E5C3C840 40404040			6350+	DS	2F	extracted PSW after test (has CC)
00008410	00008488			6351+	DC	X' FF'	extracted CC, if test failed
00008414	00008498			6352+	DC	CL8' VCH'	instruction name
00008418	000084A8			6353+	DC	A(RE148)	address of v1 result
0000841C	00000010			6354+	DC	A(RE148+16)	address of v2 source
00008420	00008488			6355+	DC	A(RE148+32)	address of v3 source
00008428	00000000 00000000			6356+	DC	A(16)	result length
00008430	00000000 00000000			6357+REA148	DC	A(RE148)	result address
00008438	00000000 00000000			6358+	DS	2FD	gap
00008440	00000000 00000000			6359+V10148	DS	XL16	V1 output
00008448	00000000 00000000						
00008450	00000000 00000000			6360+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008458				6361+*			
00008458	E310 5024 0014		00000024	6362+X148	DS	0F	
0000845E	E761 0000 0806		00000000	6363+	LGF	R1, V2ADDR	load v2 source
00008464	E310 5028 0014		00000028	6364+	VL	v22, 0(R1)	use v21 to test decoder
0000846A	E771 0000 0806		00000000	6365+	LGF	R1, V3ADDR	load v3 source
00008470	E756 7010 0EFB			6366+	VL	v23, 0(R1)	use v22 to test decoder
00008476	B98D 0020			6367+	VCH	V21, V22, V23, 0, 1	test instruction
0000847A	5020 500C		0000000C	6368+	EPSW	R2, R0	extract psw
0000847E	E750 5048 080E		00008438	6369+	ST	R2, CCPSW	to save CC
00008484	07FB			6370+	VST	V21, V10148	save v1 output
00008488				6371+	BR	R11	return
00008488				6372+RE148	DC	0F	V1 for this test
00008488	00000000 000000FF			6373+	DROP	R5	
00008490	00FF00FF 00FF00FF			6374	DC	XL16' 0000000000000000FF 00FF00FF00FF00FF'	result t
00008498	08090A0B 0C0DFE1F			6375	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
000084A0	00110033 00550077						
000084A8	08090A0B 0C0DFE0F			6376	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v3
000084B0	00010203 04050607						
000084B8				6377			
000084B8		000084B8		6378	VRR_B	VCH, 0, 1	
000084B8	00008520			6379+	DS	0FD	
000084BC	0095			6380+	USING	*, R5	base for test data and test routine
000084BE	00			6381+T149	DC	A(X149)	address of test routine
000084BF	00			6382+	DC	H' 149'	test number
000084C0	01			6383+	DC	X' 00'	
000084C1	01			6384+	DC	HL1' 0'	m4 used
000084C2	0B			6385+	DC	HL1' 1'	m5 used
000084C4	00000000 00000000			6386+	DC	HL1' 1'	CC
000084CC	FF			6387+	DC	HL1' 11'	CC failed mask
000084CD	E5C3C840 40404040			6388+	DS	2F	extracted PSW after test (has CC)
000084D8	00008550			6389+	DC	X' FF'	extracted CC, if test failed
000084DC	00008560			6390+	DC	CL8' VCH'	instruction name
000084E0	00008570			6391+	DC	A(RE149)	address of v1 result
000084E4	00000010			6392+	DC	A(RE149+16)	address of v2 source
000084E8	00008550			6393+	DC	A(RE149+32)	address of v3 source
000084F0	00000000 00000000			6394+	DC	A(16)	result length
000084F8	00000000 00000000			6395+REA149	DC	A(RE149)	result address
00008500	00000000 00000000			6396+	DS	2FD	gap
00008508	00000000 00000000			6397+V10149	DS	XL16	V1 output
00008510	00000000 00000000			6398+	DS	2FD	gap
00008518	00000000 00000000						
00008520				6399+*			
00008520	E310 5024 0014		00000024	6400+X149	DS	0F	
00008526	E761 0000 0806		00000000	6401+	LGF	R1, V2ADDR	load v2 source
0000852C	E310 5028 0014		00000028	6402+	VL	v22, 0(R1)	use v21 to test decoder
00008532	E771 0000 0806		00000000	6403+	LGF	R1, V3ADDR	load v3 source
00008538	E756 7010 0EFB			6404+	VL	v23, 0(R1)	use v22 to test decoder
0000853E	B98D 0020			6405+	VCH	V21, V22, V23, 0, 1	test instruction
00008542	5020 500C		0000000C	6406+	EPSW	R2, R0	extract psw
00008546	E750 5048 080E		00008500	6407+	ST	R2, CCPSW	to save CC
0000854C	07FB			6408+	VST	V21, V10149	save v1 output
00008550				6409+	BR	R11	return
				6410+RE149	DC	0F	V1 for this test

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008550				6411+	DROP R5		
00008550	FFFFFFFF FFFFFFFF			6412	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result
00008558	00000000 00000000						
00008560	00010203 04050607			6413	DC	XL16' 0001020304050607 FFFAFF9FFF8FFF7'	v2
00008568	FFFAFFF9 FFF8FFF7						
00008570	FFFEFFFD FFFCFFFB			6414	DC	XL16' FFFEFFFDFFFCFFFB 08090A0B0C0D0E0F'	v3
00008578	08090A0B 0C0D0E0F						
				6415			
00008580				6416	VRR_B VCH, 0, 3		
00008580		00008580		6417+	DS 0FD		
00008580	000085E8			6418+	USING *, R5	base for test data and test routine	
00008584	0096			6419+T150	DC A(X150)	address of test routine	
00008586	00			6420+	DC H' 150'	test number	
00008587	00			6421+	DC X' 00'		
00008587	00			6422+	DC HL1' 0'	m4 used	
00008588	01			6423+	DC HL1' 1'	m5 used	
00008589	03			6424+	DC HL1' 3'	CC	
0000858A	0E			6425+	DC HL1' 14'	CC failed mask	
0000858C	00000000 00000000			6426+	DS 2F	extracted PSW after test (has CC)	
00008594	FF			6427+	DC X' FF'	extracted CC, if test failed	
00008595	E5C3C840 40404040			6428+	DC CL8' VCH'	instruction name	
000085A0	00008618			6429+	DC A(RE150)	address of v1 result	
000085A4	00008628			6430+	DC A(RE150+16)	address of v2 source	
000085A8	00008638			6431+	DC A(RE150+32)	address of v3 source	
000085AC	00000010			6432+	DC A(16)	result length	
000085B0	00008618			6433+REA150	DC A(RE150)	result address	
000085B8	00000000 00000000			6434+	DS 2FD	gap	
000085C0	00000000 00000000						
000085C8	00000000 00000000			6435+V10150	DS XL16	V1 output	
000085D0	00000000 00000000						
000085D8	00000000 00000000			6436+	DS 2FD	gap	
000085E0	00000000 00000000						
				6437+*			
000085E8				6438+X150	DS 0F		
000085E8	E310 5024 0014		00000024	6439+	LGF R1, V2ADDR	load v2 source	
000085EE	E761 0000 0806		00000000	6440+	VL v22, 0(R1)	use v21 to test decoder	
000085F4	E310 5028 0014		00000028	6441+	LGF R1, V3ADDR	load v3 source	
000085FA	E771 0000 0806		00000000	6442+	VL v23, 0(R1)	use v22 to test decoder	
00008600	E756 7010 0EFB			6443+	VCH V21, V22, V23, 0, 1	test instruction	
00008606	B98D 0020			6444+	EPSW R2, R0	extract psw	
0000860A	5020 500C		0000000C	6445+	ST R2, CCPSW	to save CC	
0000860E	E750 5048 080E		000085C8	6446+	VST V21, V10150	save v1 output	
00008614	07FB			6447+	BR R11	return	
00008618				6448+RE150	DC 0F	V1 for this test	
00008618				6449+	DROP R5		
00008618	00000000 00000000			6450	DC	XL16' 0000000000000000 0000000000000000'	result
00008620	00000000 00000000						
00008628	00010003 04050607			6451	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00008630	00090A0B 0C0D0E0F						
00008638	01110233 11550677			6452	DC	XL16' 0111023311550677 1179116B514D312F'	v3
00008640	1179116B 514D312F						
				6453			
00008648				6454	VRR_B VCHL, 0, 3		
00008648		00008648		6455+	DS 0FD		
00008648	000086B0			6456+	USING *, R5	base for test data and test routine	
				6457+T151	DC A(X151)	address of test routine	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
0000864C	0097			6458+	DC	H' 151'
0000864E	00			6459+	DC	X' 00'
0000864F	00			6460+	DC	HL1' 0'
00008650	01			6461+	DC	HL1' 1'
00008651	03			6462+	DC	HL1' 3'
00008652	0E			6463+	DC	HL1' 14'
00008654	00000000 00000000			6464+	DS	2F
0000865C	FF			6465+	DC	X' FF'
0000865D	E5C3C8D3 40404040			6466+	DC	CL8' VCHL'
00008668	000086E0			6467+	DC	A(RE151)
0000866C	000086F0			6468+	DC	A(RE151+16)
00008670	00008700			6469+	DC	A(RE151+32)
00008674	00000010			6470+	DC	A(16)
00008678	000086E0			6471+REA151	DC	A(RE151)
00008680	00000000 00000000			6472+	DS	2FD
00008688	00000000 00000000					
00008690	00000000 00000000			6473+V10151	DS	XL16
00008698	00000000 00000000					
000086A0	00000000 00000000			6474+	DS	2FD
000086A8	00000000 00000000					
000086B0				6475+*		
000086B0	E310 5024 0014			6476+X151	DS	0F
000086B6	E761 0000 0806		00000024	6477+	LGF	R1, V2ADDR
000086BC	E310 5028 0014		00000000	6478+	VL	v22, 0(R1)
000086C2	E771 0000 0806		00000028	6479+	LGF	R1, V3ADDR
000086C8	E756 7010 0EF9		00000000	6480+	VL	v23, 0(R1)
000086CE	B98D 0020			6481+	VCHL	V21, V22, V23, 0, 1
000086D2	5020 500C			6482+	EPSW	R2, R0
000086D6	E750 5048 080E		0000000C	6483+	ST	R2, CCPSW
000086DC	07FB		00008690	6484+	VST	V21, V10151
000086E0				6485+	BR	R11
000086E0				6486+RE151	DC	0F
000086E0	00000000 00000000			6487+	DROP	R5
000086E8	00000000 00000000			6488	DC	XL16' 0000000000000000 0000000000000000'
000086F0	08090A0B 0C0D0E0F			6489	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'
000086F8	00010203 04050607					
00008700	1179116B 514D312F			6490	DC	XL16' 1179116B514D312F 0111023311550677'
00008708	01110233 11550677					
00008710				6491		
00008710				6492	VRR_B	VCH, 0, 3
00008710	00008778	00008710		6493+	DS	0FD
00008714	0098			6494+	USING	*, R5
00008716	00			6495+T152	DC	A(X152)
00008717	00			6496+	DC	H' 152'
00008718	01			6497+	DC	X' 00'
00008719	03			6498+	DC	HL1' 0'
0000871A	0E			6499+	DC	HL1' 1'
0000871C	00000000 00000000			6500+	DC	HL1' 3'
00008724	FF			6501+	DC	HL1' 14'
00008725	E5C3C840 40404040			6502+	DS	2F
00008730	000087A8			6503+	DC	X' FF'
00008734	000087B8			6504+	DC	CL8' VCH'
00008738	000087C8			6505+	DC	A(RE152)
				6506+	DC	A(RE152+16)
				6507+	DC	A(RE152+32)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000873C	00000010			6508+	DC	A(16)	result length
00008740	000087A8			6509+REA152	DC	A(RE152)	result address
00008748	00000000 00000000			6510+	DS	2FD	gap
00008750	00000000 00000000						
00008758	00000000 00000000			6511+V10152	DS	XL16	V1 output
00008760	00000000 00000000						
00008768	00000000 00000000			6512+	DS	2FD	gap
00008770	00000000 00000000						
00008778				6513+*			
00008778	E310 5024 0014		00000024	6514+X152	DS	0F	
0000877E	E761 0000 0806		00000000	6515+	LGF	R1, V2ADDR	load v2 source
00008784	E310 5028 0014		00000028	6516+	VL	v22, 0(R1)	use v21 to test decoder
0000878A	E771 0000 0806		00000000	6517+	LGF	R1, V3ADDR	load v3 source
00008790	E756 7010 0EFB			6518+	VL	v23, 0(R1)	use v22 to test decoder
00008796	B98D 0020			6519+	VCH	V21, V22, V23, 0, 1	test instruction
0000879A	5020 500C		0000000C	6520+	EPSW	R2, R0	extract psw
0000879E	E750 5048 080E		00008758	6521+	ST	R2, CCPSW	to save CC
000087A4	07FB			6522+	VST	V21, V10152	save v1 output
000087A8				6523+	BR	R11	return
000087A8				6524+RE152	DC	0F	V1 for this test
000087A8	00000000 00000000			6525+	DROP	R5	
000087B0	00000000 00000000			6526	DC	XL16' 0000000000000000 0000000000000000'	result
000087B8	FFFEFFFD FFFCFFFB			6527	DC	XL16' FFFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
000087C0	FFFAFFF9 FFF8FFF7						
000087C8	01110233 11550677			6528	DC	XL16' 0111023311550677 08090A0B0C0D0E0F'	v3
000087D0	08090A0B 0C0D0E0F						
				6529			
				6530 *Halfword			
000087D8				6531	VRR_B	VCH, 1, 0	
000087D8		000087D8		6532+	DS	0FD	
000087D8	00008840			6533+	USING	*, R5	base for test data and test routine
000087DC	0099			6534+T153	DC	A(X153)	address of test routine
000087DE	00			6535+	DC	H' 153'	test number
000087DF	01			6536+	DC	X' 00'	
000087E0	01			6537+	DC	HL1' 1'	m4 used
000087E1	00			6538+	DC	HL1' 1'	m5 used
000087E2	07			6539+	DC	HL1' 0'	CC
000087E4	00000000 00000000			6540+	DC	HL1' 7'	CC failed mask
000087EC	FF			6541+	DS	2F	extracted PSW after test (has CC)
000087ED	E5C3C840 40404040			6542+	DC	X' FF'	extracted CC, if test failed
000087F8	00008870			6543+	DC	CL8' VCH'	instruction name
000087FC	00008880			6544+	DC	A(RE153)	address of v1 result
00008800	00008890			6545+	DC	A(RE153+16)	address of v2 source
00008804	00000010			6546+	DC	A(RE153+32)	address of v3 source
00008808	00008870			6547+	DC	A(16)	result length
00008810	00000000 00000000			6548+REA153	DC	A(RE153)	result address
00008818	00000000 00000000			6549+	DS	2FD	gap
00008820	00000000 00000000			6550+V10153	DS	XL16	V1 output
00008828	00000000 00000000						
00008830	00000000 00000000			6551+	DS	2FD	gap
00008838	00000000 00000000						
00008840				6552+*			
00008840	E310 5024 0014		00000024	6553+X153	DS	0F	
				6554+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008846	E761 0000 0806		00000000	6555+	VL	v22, 0(R1)	use v21 to test decoder
0000884C	E310 5028 0014		00000028	6556+	LGF	R1, V3ADDR	load v3 source
00008852	E771 0000 0806		00000000	6557+	VL	v23, 0(R1)	use v22 to test decoder
00008858	E756 7010 1EFB			6558+	VCH	V21, V22, V23, 1, 1	test instruction
0000885E	B98D 0020			6559+	EPSW	R2, R0	extract psw
00008862	5020 500C		0000000C	6560+	ST	R2, CCPSW	to save CC
00008866	E750 5048 080E		00008820	6561+	VST	V21, V10153	save v1 output
0000886C	07FB			6562+	BR	R11	return
00008870				6563+RE153	DC	0F	V1 for this test
00008870				6564+	DROP	R5	
00008870	FFFFFFFF FFFFFFFF			6565	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00008878	FFFFFFFF FFFFFFFF						
00008880	01020304 05060708			6566	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
00008888	090A0B0C 0D0E0F10						
00008890	00010203 04050607			6567	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00008898	08090A0B 0C0D0E0F						
				6568			
000088A0				6569	VRR_B	VCH, 1, 0	
000088A0		000088A0		6570+	DS	0FD	
000088A0	00008908			6571+	USING	*, R5	base for test data and test routine
000088A4	009A			6572+T154	DC	A(X154)	address of test routine
000088A6	00			6573+	DC	H' 154'	test number
000088A7	01			6574+	DC	X' 00'	
000088A8	01			6575+	DC	HL1' 1'	m4 used
000088A8	01			6576+	DC	HL1' 1'	m5 used
000088A9	00			6577+	DC	HL1' 0'	CC
000088AA	07			6578+	DC	HL1' 7'	CC failed mask
000088AC	00000000 00000000			6579+	DS	2F	extracted PSW after test (has CC)
000088B4	FF			6580+	DC	X' FF'	extracted CC, if test failed
000088B5	E5C3C840 40404040			6581+	DC	CL8' VCH'	instruction name
000088C0	00008938			6582+	DC	A(RE154)	address of v1 result
000088C4	00008948			6583+	DC	A(RE154+16)	address of v2 source
000088C8	00008958			6584+	DC	A(RE154+32)	address of v3 source
000088CC	00000010			6585+	DC	A(16)	result length
000088D0	00008938			6586+REA154	DC	A(RE154)	result address
000088D8	00000000 00000000			6587+	DS	2FD	gap
000088E0	00000000 00000000						
000088E8	00000000 00000000			6588+V10154	DS	XL16	V1 output
000088F0	00000000 00000000						
000088F8	00000000 00000000			6589+	DS	2FD	gap
00008900	00000000 00000000						
				6590+*			
00008908				6591+X154	DS	0F	
00008908	E310 5024 0014		00000024	6592+	LGF	R1, V2ADDR	load v2 source
0000890E	E761 0000 0806		00000000	6593+	VL	v22, 0(R1)	use v21 to test decoder
00008914	E310 5028 0014		00000028	6594+	LGF	R1, V3ADDR	load v3 source
0000891A	E771 0000 0806		00000000	6595+	VL	v23, 0(R1)	use v22 to test decoder
00008920	E756 7010 1EFB			6596+	VCH	V21, V22, V23, 1, 1	test instruction
00008926	B98D 0020			6597+	EPSW	R2, R0	extract psw
0000892A	5020 500C		0000000C	6598+	ST	R2, CCPSW	to save CC
0000892E	E750 5048 080E		000088E8	6599+	VST	V21, V10154	save v1 output
00008934	07FB			6600+	BR	R11	return
00008938				6601+RE154	DC	0F	V1 for this test
00008938				6602+	DROP	R5	
00008938	FFFFFFFF FFFFFFFF			6603	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00008940	FFFFFFFF FFFFFFFF						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00008948	00010203 04050607			6604	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00008950	08090A0B 0C0D0E0F							
00008958	FFFEFFFD FFFCFFFB			6605	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3	
00008960	FFFAFF9 FFF8FFF7							
				6606				
00008968				6607	VRR_B	VCH, 1, 1		
00008968		00008968		6608+	DS	0FD		
00008968	000089D0			6609+	USING	*, R5	base for test data and test routine	
0000896C	009B			6610+T155	DC	A(X155)	address of test routine	
0000896E	00			6611+	DC	H' 155'	test number	
0000896F	01			6612+	DC	X' 00'		
00008970	01			6613+	DC	HL1' 1'	m4 used	
00008971	01			6614+	DC	HL1' 1'	m5 used	
00008972	0B			6615+	DC	HL1' 1'	CC	
00008974	00000000 00000000			6616+	DC	HL1' 11'	CC failed mask	
0000897C	FF			6617+	DS	2F	extracted PSW after test (has CC)	
0000897D	E5C3C840 40404040			6618+	DC	X' FF'	extracted CC, if test failed	
00008988	00008A00			6619+	DC	CL8' VCH'	instruction name	
0000898C	00008A10			6620+	DC	A(RE155)	address of v1 result	
00008990	00008A20			6621+	DC	A(RE155+16)	address of v2 source	
00008994	00000010			6622+	DC	A(RE155+32)	address of v3 source	
00008998	00008A00			6623+	DC	A(16)	result length	
000089A0	00000000 00000000			6624+REA155	DC	A(RE155)	result address	
000089A8	00000000 00000000			6625+	DS	2FD	gap	
000089B0	00000000 00000000			6626+V10155	DS	XL16	V1 output	
000089B8	00000000 00000000							
000089C0	00000000 00000000			6627+	DS	2FD	gap	
000089C8	00000000 00000000							
				6628+*				
000089D0				6629+X155	DS	0F		
000089D0	E310 5024 0014		00000024	6630+	LGF	R1, V2ADDR	load v2 source	
000089D6	E761 0000 0806		00000000	6631+	VL	v22, 0(R1)	use v21 to test decoder	
000089DC	E310 5028 0014		00000028	6632+	LGF	R1, V3ADDR	load v3 source	
000089E2	E771 0000 0806		00000000	6633+	VL	v23, 0(R1)	use v22 to test decoder	
000089E8	E756 7010 1EFB			6634+	VCH	V21, V22, V23, 1, 1	test instruction	
000089EE	B98D 0020			6635+	EPSW	R2, R0	extract psw	
000089F2	5020 500C		0000000C	6636+	ST	R2, CCPSW	to save CC	
000089F6	E750 5048 080E		000089B0	6637+	VST	V21, V10155	save v1 output	
000089FC	07FB			6638+	BR	R11	return	
00008A00				6639+RE155	DC	0F	V1 for this test	
00008A00				6640+	DROP	R5		
00008A00	FFFF0000 0000FFFF			6641	DC	XL16' FFFF00000000FFFF 000000000000FFFF'	result t	
00008A08	00000000 0000FFFF							
00008A10	00110033 00550077			6642	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'	v2	
00008A18	08090A0B 0C0DFE1F							
00008A20	00010203 04050067			6643	DC	XL16' 0001020304050067 08090A0B0C0DFE0F'	v3	
00008A28	08090A0B 0C0DFE0F							
				6644				
00008A30				6645	VRR_B	VCH, 1, 1		
00008A30		00008A30		6646+	DS	0FD		
00008A30	00008A98			6647+	USING	*, R5	base for test data and test routine	
00008A34	009C			6648+T156	DC	A(X156)	address of test routine	
00008A36	00			6649+	DC	H' 156'	test number	
00008A37	01			6650+	DC	X' 00'		
				6651+	DC	HL1' 1'	m4 used	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00008A38	01			6652+	DC	HL1' 1' m5 used
00008A39	01			6653+	DC	HL1' 1' CC
00008A3A	0B			6654+	DC	HL1' 11' CC failed mask
00008A3C	00000000	00000000		6655+	DS	2F extracted PSW after test (has CC)
00008A44	FF			6656+	DC	X' FF' extracted CC, if test failed
00008A45	E5C3C840	40404040		6657+	DC	CL8' VCH' instruction name
00008A50	00008AC8			6658+	DC	A(RE156) address of v1 result
00008A54	00008AD8			6659+	DC	A(RE156+16) address of v2 source
00008A58	00008AE8			6660+	DC	A(RE156+32) address of v3 source
00008A5C	00000010			6661+	DC	A(16) result length
00008A60	00008AC8			6662+REA156	DC	A(RE156) result address
00008A68	00000000	00000000		6663+	DS	2FD gap
00008A70	00000000	00000000				
00008A78	00000000	00000000		6664+V10156	DS	XL16 V1 output
00008A80	00000000	00000000				
00008A88	00000000	00000000		6665+	DS	2FD gap
00008A90	00000000	00000000				
00008A98				6666+*		
00008A98	E310 5024 0014		00000024	6667+X156	DS	0F
00008A9E	E761 0000 0806		00000000	6668+	LGF	R1, V2ADDR load v2 source
00008AA4	E310 5028 0014		00000028	6669+	VL	v22, 0(R1) use v21 to test decoder
00008AAA	E771 0000 0806		00000000	6670+	LGF	R1, V3ADDR load v3 source
00008AB0	E756 7010 1EFB			6671+	VL	v23, 0(R1) use v22 to test decoder
00008AB6	B98D 0020			6672+	VCH	V21, V22, V23, 1, 1 test instruction
00008ABA	5020 500C		0000000C	6673+	EPSW	R2, R0 extract psw
00008ABE	E750 5048 080E		00008A78	6674+	ST	R2, CCPSW to save CC
00008AC4	07FB			6675+	VST	V21, V10156 save v1 output
00008AC8				6676+	BR	R11 return
00008AC8				6677+RE156	DC	0F V1 for this test
00008AC8				6678+	DROP	R5
00008AC8	00000000	0000FFFF		6679	DC	XL16' 000000000000FFFF FFFF00000000FFFF' result t
00008AD0	FFFF0000	0000FFFF				
00008AD8	08090A0B	0C0DFE1F		6680	DC	XL16' 08090A0B0C0DFE1F 0011003300550077' v2
00008AE0	00110033	00550077				
00008AE8	08090A0B	0C0DFE0F		6681	DC	XL16' 08090A0B0C0DFE0F 0001020304050067' v3
00008AF0	00010203	04050067				
00008AF8				6682		
00008AF8				6683	VRR_B	VCH, 1, 1
00008AF8	00008B60	00008AF8		6684+	DS	0FD
00008AFC	009D			6685+	USING	*, R5 base for test data and test routine
00008AFE	00			6686+T157	DC	A(X157) address of test routine
00008AFF	01			6687+	DC	H' 157' test number
00008B00	01			6688+	DC	X' 00'
00008B01	01			6689+	DC	HL1' 1' m4 used
00008B02	0B			6690+	DC	HL1' 1' m5 used
00008B04	00000000	00000000		6691+	DC	HL1' 1' CC
00008B0C	FF			6692+	DC	HL1' 11' CC failed mask
00008B0D	E5C3C840	40404040		6693+	DS	2F extracted PSW after test (has CC)
00008B18	00008B90			6694+	DC	X' FF' extracted CC, if test failed
00008B1C	00008BA0			6695+	DC	CL8' VCH' instruction name
00008B20	00008BB0			6696+	DC	A(RE157) address of v1 result
00008B24	00000010			6697+	DC	A(RE157+16) address of v2 source
00008B28	00008B90			6698+	DC	A(RE157+32) address of v3 source
00008B30	00000000	00000000		6699+	DC	A(16) result length
				6700+REA157	DC	A(RE157) result address
				6701+	DS	2FD gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008B38	00000000	00000000					
00008B40	00000000	00000000		6702+V10157	DS	XL16	V1 output
00008B48	00000000	00000000					
00008B50	00000000	00000000		6703+	DS	2FD	gap
00008B58	00000000	00000000					
00008B60				6704+*			
00008B60	E310 5024 0014		00000024	6705+X157	DS	0F	
00008B66	E761 0000 0806		00000000	6706+	LGF	R1, V2ADDR	load v2 source
00008B6C	E310 5028 0014		00000028	6707+	VL	v22, 0(R1)	use v21 to test decoder
00008B72	E771 0000 0806		00000000	6708+	LGF	R1, V3ADDR	load v3 source
00008B78	E756 7010 1EFB			6709+	VL	v23, 0(R1)	use v22 to test decoder
00008B7E	B98D 0020			6710+	VCH	V21, V22, V23, 1, 1	test instruction
00008B82	5020 500C		0000000C	6711+	EPSW	R2, R0	extract psw
00008B86	E750 5048 080E		00008B40	6712+	ST	R2, CCPSW	to save CC
00008B8C	07FB			6713+	VST	V21, V10157	save v1 output
00008B90				6714+	BR	R11	return
00008B90				6715+RE157	DC	0F	V1 for this test
00008B90	FFFFFFFF	FFFFFFFF		6716+	DROP	R5	
00008B98	00000000	00000000		6717	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result
00008BA0	00010203 04050607			6718	DC	XL16' 0001020304050607 FFFAFF9FFF8FFF7'	v2
00008BA8	FFFAFFF9 FFF8FFF7						
00008BB0	FFFEFFFD FFFCFFFB			6719	DC	XL16' FFFEFFFDFFFCFFFB 08090A0B0C0D0E0F'	v3
00008BB8	08090A0B 0C0D0E0F						
00008BC0				6720			
00008BC0				6721	VRR_B	VCH, 1, 3	
00008BC0	00008C28	00008BC0		6722+	DS	0FD	
00008BC4	009E			6723+	USING	*, R5	base for test data and test routine
00008BC6	00			6724+T158	DC	A(X158)	address of test routine
00008BC7	01			6725+	DC	H' 158'	test number
00008BC8	01			6726+	DC	X' 00'	
00008BC9	03			6727+	DC	HL1' 1'	m4 used
00008BCA	0E			6728+	DC	HL1' 1'	m5 used
00008BCC	00000000 00000000			6729+	DC	HL1' 3'	CC
00008BD4	FF			6730+	DC	HL1' 14'	CC failed mask
00008BD5	E5C3C840 40404040			6731+	DS	2F	extracted PSW after test (has CC)
00008BE0	00008C58			6732+	DC	X' FF'	extracted CC, if test failed
00008BE4	00008C68			6733+	DC	CL8' VCH'	instruction name
00008BE8	00008C78			6734+	DC	A(RE158)	address of v1 result
00008BEC	00000010			6735+	DC	A(RE158+16)	address of v2 source
00008BF0	00008C58			6736+	DC	A(RE158+32)	address of v3 source
00008BF8	00000000 00000000			6737+	DC	A(16)	result length
00008C00	00000000 00000000			6738+REA158	DC	A(RE158)	result address
00008C08	00000000 00000000			6739+	DS	2FD	gap
00008C10	00000000 00000000						
00008C18	00000000 00000000			6740+V10158	DS	XL16	V1 output
00008C20	00000000 00000000						
00008C28				6741+	DS	2FD	gap
00008C28	E310 5024 0014		00000024	6742+*			
00008C2E	E761 0000 0806		00000000	6743+X158	DS	0F	
00008C34	E310 5028 0014		00000028	6744+	LGF	R1, V2ADDR	load v2 source
00008C3A	E771 0000 0806		00000000	6745+	VL	v22, 0(R1)	use v21 to test decoder
00008C40	E756 7010 1EFB			6746+	LGF	R1, V3ADDR	load v3 source
				6747+	VL	v23, 0(R1)	use v22 to test decoder
				6748+	VCH	V21, V22, V23, 1, 1	test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008C46	B98D 0020			6749+	EPSW	R2, R0	extract psw
00008C4A	5020 500C		0000000C	6750+	ST	R2, CCPSW	to save CC
00008C4E	E750 5048 080E		00008C08	6751+	VST	V21, V10158	save v1 output
00008C54	07FB			6752+	BR	R11	return
00008C58				6753+RE158	DC	0F	V1 for this test
00008C58				6754+	DROP	R5	
00008C58	00000000 00000000			6755	DC	XL16' 0000000000000000 0000000000000000'	result t
00008C60	00000000 00000000						
00008C68	00010003 04050607			6756	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00008C70	00090A0B 0C0D0E0F						
00008C78	01110233 11550677			6757	DC	XL16' 0111023311550677 1179116B514D312F'	v3
00008C80	1179116B 514D312F						
				6758			
				6759	VRR_B	VCHL, 1, 3	
00008C88				6760+	DS	0FD	
00008C88		00008C88		6761+	USING	*, R5	base for test data and test routine
00008C88	00008CF0			6762+T159	DC	A(X159)	address of test routine
00008C8C	009F			6763+	DC	H' 159'	test number
00008C8E	00			6764+	DC	X' 00'	
00008C8F	01			6765+	DC	HL1' 1'	m4 used
00008C90	01			6766+	DC	HL1' 1'	m5 used
00008C91	03			6767+	DC	HL1' 3'	CC
00008C92	0E			6768+	DC	HL1' 14'	CC failed mask
00008C94	00000000 00000000			6769+	DS	2F	extracted PSW after test (has CC)
00008C9C	FF			6770+	DC	X' FF'	extracted CC, if test failed
00008C9D	E5C3C8D3 40404040			6771+	DC	CL8' VCHL'	instruction name
00008CA8	00008D20			6772+	DC	A(RE159)	address of v1 result
00008CAC	00008D30			6773+	DC	A(RE159+16)	address of v2 source
00008CB0	00008D40			6774+	DC	A(RE159+32)	address of v3 source
00008CB4	00000010			6775+	DC	A(16)	result length
00008CB8	00008D20			6776+REA159	DC	A(RE159)	result address
00008CC0	00000000 00000000			6777+	DS	2FD	gap
00008CC8	00000000 00000000						
00008CD0	00000000 00000000			6778+V10159	DS	XL16	V1 output
00008CD8	00000000 00000000						
00008CE0	00000000 00000000			6779+	DS	2FD	gap
00008CE8	00000000 00000000						
				6780+*			
00008CF0				6781+X159	DS	0F	
00008CF0	E310 5024 0014		00000024	6782+	LGF	R1, V2ADDR	load v2 source
00008CF6	E761 0000 0806		00000000	6783+	VL	v22, 0(R1)	use v21 to test decoder
00008CFC	E310 5028 0014		00000028	6784+	LGF	R1, V3ADDR	load v3 source
00008D02	E771 0000 0806		00000000	6785+	VL	v23, 0(R1)	use v22 to test decoder
00008D08	E756 7010 1EF9			6786+	VCHL	V21, V22, V23, 1, 1	test instruction
00008D0E	B98D 0020			6787+	EPSW	R2, R0	extract psw
00008D12	5020 500C		0000000C	6788+	ST	R2, CCPSW	to save CC
00008D16	E750 5048 080E		00008CD0	6789+	VST	V21, V10159	save v1 output
00008D1C	07FB			6790+	BR	R11	return
00008D20				6791+RE159	DC	0F	V1 for this test
00008D20				6792+	DROP	R5	
00008D20	00000000 00000000			6793	DC	XL16' 0000000000000000 0000000000000000'	result t
00008D28	00000000 00000000						
00008D30	08090A0B 0C0D0E0F			6794	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00008D38	00010203 04050607						
00008D40	1179116B 514D312F			6795	DC	XL16' 1179116B514D312F 0111023311550677'	v3
00008D48	01110233 11550677						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				6796				
				6797	VRR_B	VCH, 1, 3		
00008D50				6798+	DS	0FD		
00008D50		00008D50		6799+	USING	*, R5	base for test data and test routine	
00008D50	00008DB8			6800+T160	DC	A(X160)	address of test routine	
00008D54	00A0			6801+	DC	H' 160'	test number	
00008D56	00			6802+	DC	X' 00'		
00008D57	01			6803+	DC	HL1' 1'	m4 used	
00008D58	01			6804+	DC	HL1' 1'	m5 used	
00008D59	03			6805+	DC	HL1' 3'	CC	
00008D5A	0E			6806+	DC	HL1' 14'	CC failed mask	
00008D5C	00000000	00000000		6807+	DS	2F	extracted PSW after test (has CC)	
00008D64	FF			6808+	DC	X' FF'	extracted CC, if test failed	
00008D65	E5C3C840	40404040		6809+	DC	CL8' VCH'	instruction name	
00008D70	00008DE8			6810+	DC	A(RE160)	address of v1 result	
00008D74	00008DF8			6811+	DC	A(RE160+16)	address of v2 source	
00008D78	00008E08			6812+	DC	A(RE160+32)	address of v3 source	
00008D7C	00000010			6813+	DC	A(16)	result length	
00008D80	00008DE8			6814+REA160	DC	A(RE160)	result address	
00008D88	00000000	00000000		6815+	DS	2FD	gap	
00008D90	00000000	00000000						
00008D98	00000000	00000000		6816+V10160	DS	XL16	V1 output	
00008DA0	00000000	00000000						
00008DA8	00000000	00000000		6817+	DS	2FD	gap	
00008DB0	00000000	00000000						
				6818+*				
00008DB8				6819+X160	DS	0F		
00008DB8	E310 5024 0014		00000024	6820+	LGF	R1, V2ADDR	load v2 source	
00008DBE	E761 0000 0806		00000000	6821+	VL	v22, 0(R1)	use v21 to test decoder	
00008DC4	E310 5028 0014		00000028	6822+	LGF	R1, V3ADDR	load v3 source	
00008DCA	E771 0000 0806		00000000	6823+	VL	v23, 0(R1)	use v22 to test decoder	
00008DD0	E756 7010 1EFB			6824+	VCH	V21, V22, V23, 1, 1	test instruction	
00008DD6	B98D 0020			6825+	EPSW	R2, R0	extract psw	
00008DDA	5020 500C		0000000C	6826+	ST	R2, CCPSW	to save CC	
00008DDE	E750 5048 080E		00008D98	6827+	VST	V21, V10160	save v1 output	
00008DE4	07FB			6828+	BR	R11	return	
00008DE8				6829+RE160	DC	0F	V1 for this test	
00008DE8				6830+	DROP	R5		
00008DE8	00000000	00000000		6831	DC	XL16' 0000000000000000 0000000000000000'	result t	
00008DF0	00000000	00000000						
00008DF8	FFFEFFFD	FFFCFFFB		6832	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2	
00008E00	FFFAFFF9	FFF8FFF7						
00008E08	01110233	11550677		6833	DC	XL16' 0111023311550677 08090A0B0C0D0E0F'	v3	
00008E10	08090A0B	0C0D0E0F						
				6834				
				6835 *Word				
				6836	VRR_B	VCH, 2, 0		
00008E18				6837+	DS	0FD		
00008E18		00008E18		6838+	USING	*, R5	base for test data and test routine	
00008E18	00008E80			6839+T161	DC	A(X161)	address of test routine	
00008E1C	00A1			6840+	DC	H' 161'	test number	
00008E1E	00			6841+	DC	X' 00'		
00008E1F	02			6842+	DC	HL1' 2'	m4 used	
00008E20	01			6843+	DC	HL1' 1'	m5 used	
00008E21	00			6844+	DC	HL1' 0'	CC	
00008E22	07			6845+	DC	HL1' 7'	CC failed mask	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008E24	00000000 00000000			6846+	DS	2F	extracted PSW after test (has CC)
00008E2C	FF			6847+	DC	X' FF'	extracted CC, if test failed
00008E2D	E5C3C840 40404040			6848+	DC	CL8' VCH'	instruction name
00008E38	00008EB0			6849+	DC	A(RE161)	address of v1 result
00008E3C	00008EC0			6850+	DC	A(RE161+16)	address of v2 source
00008E40	00008ED0			6851+	DC	A(RE161+32)	address of v3 source
00008E44	00000010			6852+	DC	A(16)	result length
00008E48	00008EB0			6853+REA161	DC	A(RE161)	result address
00008E50	00000000 00000000			6854+	DS	2FD	gap
00008E58	00000000 00000000						
00008E60	00000000 00000000			6855+V10161	DS	XL16	V1 output
00008E68	00000000 00000000						
00008E70	00000000 00000000			6856+	DS	2FD	gap
00008E78	00000000 00000000						
00008E80				6857+*			
00008E80	E310 5024 0014		00000024	6858+X161	DS	0F	
00008E86	E761 0000 0806		00000000	6859+	LGF	R1, V2ADDR	load v2 source
00008E8C	E310 5028 0014		00000028	6860+	VL	v22, 0(R1)	use v21 to test decoder
00008E92	E771 0000 0806		00000000	6861+	LGF	R1, V3ADDR	load v3 source
00008E98	E756 7010 2EFB			6862+	VL	v23, 0(R1)	use v22 to test decoder
00008E9E	B98D 0020			6863+	VCH	V21, V22, V23, 2, 1	test instruction
00008EA2	5020 500C		0000000C	6864+	EPSW	R2, R0	extract psw
00008EA6	E750 5048 080E		00008E60	6865+	ST	R2, CCPSW	to save CC
00008EAC	07FB			6866+	VST	V21, V10161	save v1 output
00008EB0				6867+	BR	R11	return
00008EB0				6868+RE161	DC	0F	V1 for this test
00008EB0	FFFFFFFF FFFFFFFF			6869+	DROP	R5	
00008EB8	FFFFFFFF FFFFFFFF			6870	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00008EC0	01020304 05060708			6871	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
00008EC8	090A0B0C 0D0E0F10						
00008ED0	00010203 04050607			6872	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00008ED8	08090A0B 0C0D0E0F						
00008EE0				6873			
00008EE0		00008EE0		6874	VRR_B	VCH, 2, 0	
00008EE0	00008F48			6875+	DS	0FD	
00008EE4	00A2			6876+	USING	*, R5	base for test data and test routine
00008EE6	00			6877+T162	DC	A(X162)	address of test routine
00008EE7	02			6878+	DC	H' 162'	test number
00008EE8	01			6879+	DC	X' 00'	
00008EE9	00			6880+	DC	HL1' 2'	m4 used
00008EEA	07			6881+	DC	HL1' 1'	m5 used
00008EEC	00000000 00000000			6882+	DC	HL1' 0'	CC
00008EF4	FF			6883+	DC	HL1' 7'	CC failed mask
00008EF5	E5C3C840 40404040			6884+	DS	2F	extracted PSW after test (has CC)
00008F00	00008F78			6885+	DC	X' FF'	extracted CC, if test failed
00008F04	00008F88			6886+	DC	CL8' VCH'	instruction name
00008F08	00008F98			6887+	DC	A(RE162)	address of v1 result
00008F0C	00000010			6888+	DC	A(RE162+16)	address of v2 source
00008F10	00008F78			6889+	DC	A(RE162+32)	address of v3 source
00008F18	00000000 00000000			6890+	DC	A(16)	result length
00008F20	00000000 00000000			6891+REA162	DC	A(RE162)	result address
00008F28	00000000 00000000			6892+	DS	2FD	gap
00008F30	00000000 00000000			6893+V10162	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008F38	00000000 00000000			6894+	DS	2FD	gap
00008F40	00000000 00000000						
00008F48				6895+*			
00008F48	E310 5024 0014		00000024	6896+X162	DS	0F	
00008F4E	E761 0000 0806		00000000	6897+	LGF	R1, V2ADDR	load v2 source
00008F54	E310 5028 0014		00000028	6898+	VL	v22, 0(R1)	use v21 to test decoder
00008F5A	E771 0000 0806		00000000	6899+	LGF	R1, V3ADDR	load v3 source
00008F60	E756 7010 2EFB			6900+	VL	v23, 0(R1)	use v22 to test decoder
00008F66	B98D 0020			6901+	VCH	V21, V22, V23, 2, 1	test instruction
00008F6A	5020 500C		0000000C	6902+	EPSW	R2, R0	extract psw
00008F6E	E750 5048 080E		00008F28	6903+	ST	R2, CCPSW	to save CC
00008F74	07FB			6904+	VST	V21, V10162	save v1 output
00008F78				6905+	BR	R11	return
00008F78				6906+RE162	DC	0F	V1 for this test
00008F78	FFFFFFFF FFFFFFFF			6907+	DROP	R5	
00008F80	FFFFFFFF FFFFFFFF			6908	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00008F88	00010203 04050607			6909	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00008F90	08090A0B 0C0D0E0F						
00008F98	FFFEFFFD FFFCFFFB			6910	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00008FA0	FFFAFFF9 FFF8FFF7						
00008FA8				6911			
00008FA8				6912	VRR_B	VCH, 2, 1	
00008FA8		00008FA8		6913+	DS	0FD	
00008FAC	00009010			6914+	USING	*, R5	base for test data and test routine
00008FAE	00A3			6915+T163	DC	A(X163)	address of test routine
00008FAF	00			6916+	DC	H' 163'	test number
00008FB0	02			6917+	DC	X' 00'	
00008FB1	01			6918+	DC	HL1' 2'	m4 used
00008FB2	0B			6919+	DC	HL1' 1'	m5 used
00008FB4	00000000 00000000			6920+	DC	HL1' 1'	CC
00008FBC	FF			6921+	DC	HL1' 11'	CC failed mask
00008FBD	E5C3C840 40404040			6922+	DS	2F	extracted PSW after test (has CC)
00008FC8	00009040			6923+	DC	X' FF'	extracted CC, if test failed
00008FCC	00009050			6924+	DC	CL8' VCH'	instruction name
00008FD0	00009060			6925+	DC	A(RE163)	address of v1 result
00008FD4	00000010			6926+	DC	A(RE163+16)	address of v2 source
00008FD8	00009040			6927+	DC	A(RE163+32)	address of v3 source
00008FE0	00000000 00000000			6928+	DC	A(16)	result length
00008FE8	00000000 00000000			6929+REA163	DC	A(RE163)	result address
00008FF0	00000000 00000000			6930+	DS	2FD	gap
00008FF8	00000000 00000000						
00009000	00000000 00000000			6931+V10163	DS	XL16	V1 output
00009008	00000000 00000000						
00009010				6932+	DS	2FD	gap
00009010				6933+*			
00009010	E310 5024 0014		00000024	6934+X163	DS	0F	
00009016	E761 0000 0806		00000000	6935+	LGF	R1, V2ADDR	load v2 source
0000901C	E310 5028 0014		00000028	6936+	VL	v22, 0(R1)	use v21 to test decoder
00009022	E771 0000 0806		00000000	6937+	LGF	R1, V3ADDR	load v3 source
00009028	E756 7010 2EFB			6938+	VL	v23, 0(R1)	use v22 to test decoder
0000902E	B98D 0020			6939+	VCH	V21, V22, V23, 2, 1	test instruction
00009032	5020 500C		0000000C	6940+	EPSW	R2, R0	extract psw
00009036	E750 5048 080E		00008FF0	6941+	ST	R2, CCPSW	to save CC
				6942+	VST	V21, V10163	save v1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000903C	07FB			6943+	BR	R11	return
00009040				6944+RE163	DC	0F	V1 for this test
00009040				6945+	DROP	R5	
00009040	FFFFFFFF	00000000		6946	DC	XL16' FFFFFFFFFF00000000 00000000FFFFFFFF'	result t
00009048	00000000	FFFFFFFF					
00009050	00110033	00550077		6947	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'	v2
00009058	08090A0B	0C0DFE1F					
00009060	00010203	04050067		6948	DC	XL16' 0001020304050067 08090A0B0C0DFE0F'	v3
00009068	08090A0B	0C0DFE0F					
				6949			
				6950	VRR_B	VCH, 2, 1	
00009070				6951+	DS	0FD	
00009070		00009070		6952+	USING	*, R5	base for test data and test routine
00009070	000090D8			6953+T164	DC	A(X164)	address of test routine
00009074	00A4			6954+	DC	H' 164'	test number
00009076	00			6955+	DC	X' 00'	
00009077	02			6956+	DC	HL1' 2'	m4 used
00009078	01			6957+	DC	HL1' 1'	m5 used
00009079	01			6958+	DC	HL1' 1'	CC
0000907A	0B			6959+	DC	HL1' 11'	CC failed mask
0000907C	00000000	00000000		6960+	DS	2F	extracted PSW after test (has CC)
00009084	FF			6961+	DC	X' FF'	extracted CC, if test failed
00009085	E5C3C840	40404040		6962+	DC	CL8' VCH'	instruction name
00009090	00009108			6963+	DC	A(RE164)	address of v1 result
00009094	00009118			6964+	DC	A(RE164+16)	address of v2 source
00009098	00009128			6965+	DC	A(RE164+32)	address of v3 source
0000909C	00000010			6966+	DC	A(16)	result length
000090A0	00009108			6967+REA164	DC	A(RE164)	result address
000090A8	00000000	00000000		6968+	DS	2FD	gap
000090B0	00000000	00000000					
000090B8	00000000	00000000		6969+V10164	DS	XL16	V1 output
000090C0	00000000	00000000					
000090C8	00000000	00000000		6970+	DS	2FD	gap
000090D0	00000000	00000000					
				6971+*			
000090D8				6972+X164	DS	0F	
000090D8	E310 5024 0014		00000024	6973+	LGF	R1, V2ADDR	load v2 source
000090DE	E761 0000 0806		00000000	6974+	VL	v22, 0(R1)	use v21 to test decoder
000090E4	E310 5028 0014		00000028	6975+	LGF	R1, V3ADDR	load v3 source
000090EA	E771 0000 0806		00000000	6976+	VL	v23, 0(R1)	use v22 to test decoder
000090F0	E756 7010 2EFB			6977+	VCH	V21, V22, V23, 2, 1	test instruction
000090F6	B98D 0020			6978+	EPSW	R2, R0	extract psw
000090FA	5020 500C		0000000C	6979+	ST	R2, CCPSW	to save CC
000090FE	E750 5048 080E		000090B8	6980+	VST	V21, V10164	save v1 output
00009104	07FB			6981+	BR	R11	return
00009108				6982+RE164	DC	0F	V1 for this test
00009108				6983+	DROP	R5	
00009108	00000000	FFFFFFFF		6984	DC	XL16' 00000000FFFFFFFF FFFFFFFF00000000'	result t
00009110	FFFFFFFF	00000000					
00009118	08090A0B	0C0DFE1F		6985	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
00009120	00110033	00550077					
00009128	08090A0B	0C0DFE0F		6986	DC	XL16' 08090A0B0C0DFE0F 0001020304050067'	v3
00009130	00010203	04050067					
				6987			
				6988	VRR_B	VCH, 2, 1	
00009138				6989+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00009138		00009138		6990+	USING *, R5	base for test data and test routine
00009138	000091A0			6991+T165	DC A(X165)	address of test routine
0000913C	00A5			6992+	DC H' 165'	test number
0000913E	00			6993+	DC X' 00'	
0000913F	02			6994+	DC HL1' 2'	m4 used
00009140	01			6995+	DC HL1' 1'	m5 used
00009141	01			6996+	DC HL1' 1'	CC
00009142	0B			6997+	DC HL1' 11'	CC failed mask
00009144	00000000 00000000			6998+	DS 2F	extracted PSW after test (has CC)
0000914C	FF			6999+	DC X' FF'	extracted CC, if test failed
0000914D	E5C3C840 40404040			7000+	DC CL8' VCH'	instruction name
00009158	000091D0			7001+	DC A(RE165)	address of v1 result
0000915C	000091E0			7002+	DC A(RE165+16)	address of v2 source
00009160	000091F0			7003+	DC A(RE165+32)	address of v3 source
00009164	00000010			7004+	DC A(16)	result length
00009168	000091D0			7005+REA165	DC A(RE165)	result address
00009170	00000000 00000000			7006+	DS 2FD	gap
00009178	00000000 00000000					
00009180	00000000 00000000			7007+V10165	DS XL16	V1 output
00009188	00000000 00000000					
00009190	00000000 00000000			7008+	DS 2FD	gap
00009198	00000000 00000000					
				7009+*		
000091A0				7010+X165	DS 0F	
000091A0	E310 5024 0014	00000024		7011+	LGF R1, V2ADDR	load v2 source
000091A6	E761 0000 0806	00000000		7012+	VL v22, 0(R1)	use v21 to test decoder
000091AC	E310 5028 0014	00000028		7013+	LGF R1, V3ADDR	load v3 source
000091B2	E771 0000 0806	00000000		7014+	VL v23, 0(R1)	use v22 to test decoder
000091B8	E756 7010 2EFB			7015+	VCH V21, V22, V23, 2, 1	test instruction
000091BE	B98D 0020			7016+	EPSW R2, R0	extract psw
000091C2	5020 500C	0000000C		7017+	ST R2, CCPSW	to save CC
000091C6	E750 5048 080E	00009180		7018+	VST V21, V10165	save v1 output
000091CC	07FB			7019+	BR R11	return
000091D0				7020+RE165	DC 0F	V1 for this test
000091D0				7021+	DROP R5	
000091D0	FFFFFFFF FFFFFFFF			7022	DC XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result
000091D8	00000000 00000000					
000091E0	00010203 04050607			7023	DC XL16' 0001020304050607 FFFAFF9FFF8FFF7'	v2
000091E8	FFFAFFF9 FFF8FFF7					
000091F0	FFFEFFFD FFFCFFFB			7024	DC XL16' FFFEFFFDFFFCFFFB 08090A0B0C0D0E0F'	v3
000091F8	08090A0B 0C0D0E0F					
				7025		
				7026	VRR_B VCH, 2, 3	
00009200				7027+	DS 0FD	
00009200		00009200		7028+	USING *, R5	base for test data and test routine
00009200	00009268			7029+T166	DC A(X166)	address of test routine
00009204	00A6			7030+	DC H' 166'	test number
00009206	00			7031+	DC X' 00'	
00009207	02			7032+	DC HL1' 2'	m4 used
00009208	01			7033+	DC HL1' 1'	m5 used
00009209	03			7034+	DC HL1' 3'	CC
0000920A	0E			7035+	DC HL1' 14'	CC failed mask
0000920C	00000000 00000000			7036+	DS 2F	extracted PSW after test (has CC)
00009214	FF			7037+	DC X' FF'	extracted CC, if test failed
00009215	E5C3C840 40404040			7038+	DC CL8' VCH'	instruction name
00009220	00009298			7039+	DC A(RE166)	address of v1 result



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009224	000092A8			7040+	DC	A(RE166+16)	address of v2 source
00009228	000092B8			7041+	DC	A(RE166+32)	address of v3 source
0000922C	00000010			7042+	DC	A(16)	result length
00009230	00009298			7043+REA166	DC	A(RE166)	result address
00009238	00000000 00000000			7044+	DS	2FD	gap
00009240	00000000 00000000						
00009248	00000000 00000000			7045+V10166	DS	XL16	V1 output
00009250	00000000 00000000						
00009258	00000000 00000000			7046+	DS	2FD	gap
00009260	00000000 00000000						
				7047+*			
00009268				7048+X166	DS	0F	
00009268	E310 5024 0014		00000024	7049+	LGF	R1, V2ADDR	load v2 source
0000926E	E761 0000 0806		00000000	7050+	VL	v22, 0(R1)	use v21 to test decoder
00009274	E310 5028 0014		00000028	7051+	LGF	R1, V3ADDR	load v3 source
0000927A	E771 0000 0806		00000000	7052+	VL	v23, 0(R1)	use v22 to test decoder
00009280	E756 7010 2EFB			7053+	VCH	V21, V22, V23, 2, 1	test instruction
00009286	B98D 0020			7054+	EPSW	R2, R0	extract psw
0000928A	5020 500C		0000000C	7055+	ST	R2, CCPSW	to save CC
0000928E	E750 5048 080E		00009248	7056+	VST	V21, V10166	save v1 output
00009294	07FB			7057+	BR	R11	return
00009298				7058+RE166	DC	0F	V1 for this test
00009298				7059+	DROP	R5	
00009298	00000000 00000000			7060	DC	XL16' 0000000000000000 0000000000000000'	result
000092A0	00000000 00000000						
000092A8	00010003 04050607			7061	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
000092B0	00090A0B 0C0D0E0F						
000092B8	01110233 11550677			7062	DC	XL16' 0111023311550677 1179116B514D312F'	v3
000092C0	1179116B 514D312F						
				7063			
000092C8				7064	VRR_B	VCHL, 2, 3	
000092C8		000092C8		7065+	DS	0FD	
000092C8	00009330			7066+	USING	*, R5	base for test data and test routine
000092CC	00A7			7067+T167	DC	A(X167)	address of test routine
000092CE	00			7068+	DC	H' 167'	test number
000092CF	02			7069+	DC	X' 00'	
000092D0	01			7070+	DC	HL1' 2'	m4 used
000092D1	03			7071+	DC	HL1' 1'	m5 used
000092D2	0E			7072+	DC	HL1' 3'	CC
000092D4	00000000 00000000			7073+	DC	HL1' 14'	CC failed mask
000092DC	FF			7074+	DS	2F	extracted PSW after test (has CC)
000092DD	E5C3C8D3 40404040			7075+	DC	X' FF'	extracted CC, if test failed
000092E8	00009360			7076+	DC	CL8' VCHL'	instruction name
000092EC	00009370			7077+	DC	A(RE167)	address of v1 result
000092F0	00009380			7078+	DC	A(RE167+16)	address of v2 source
000092F4	00000010			7079+	DC	A(RE167+32)	address of v3 source
000092F8	00009360			7080+	DC	A(16)	result length
00009300	00000000 00000000			7081+REA167	DC	A(RE167)	result address
00009308	00000000 00000000			7082+	DS	2FD	gap
00009310	00000000 00000000			7083+V10167	DS	XL16	V1 output
00009318	00000000 00000000						
00009320	00000000 00000000			7084+	DS	2FD	gap
00009328	00000000 00000000						
				7085+*			
00009330				7086+X167	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009330	E310 5024 0014		00000024	7087+	LGF	R1, V2ADDR	load v2 source
00009336	E761 0000 0806		00000000	7088+	VL	v22, 0(R1)	use v21 to test decoder
0000933C	E310 5028 0014		00000028	7089+	LGF	R1, V3ADDR	load v3 source
00009342	E771 0000 0806		00000000	7090+	VL	v23, 0(R1)	use v22 to test decoder
00009348	E756 7010 2EF9			7091+	VCHL	V21, V22, V23, 2, 1	test instruction
0000934E	B98D 0020			7092+	EPSW	R2, R0	extract psw
00009352	5020 500C		0000000C	7093+	ST	R2, CCPSW	to save CC
00009356	E750 5048 080E		00009310	7094+	VST	V21, V10167	save v1 output
0000935C	07FB			7095+	BR	R11	return
00009360				7096+RE167	DC	0F	V1 for this test
00009360				7097+	DROP	R5	
00009360	00000000 00000000			7098	DC	XL16' 0000000000000000 0000000000000000'	result t
00009368	00000000 00000000						
00009370	08090A0B 0C0D0E0F			7099	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00009378	00010203 04050607						
00009380	1179116B 514D312F			7100	DC	XL16' 1179116B514D312F 0111023311550677'	v3
00009388	01110233 11550677						
00009390				7101			
00009390				7102	VRR_B	VCH, 2, 3	
00009390		00009390		7103+	DS	0FD	
00009390	000093F8			7104+	USING	*, R5	base for test data and test routine
00009394	00A8			7105+T168	DC	A(X168)	address of test routine
00009396	00			7106+	DC	H' 168'	test number
00009397	02			7107+	DC	X' 00'	
00009398	01			7108+	DC	HL1' 2'	m4 used
00009398	01			7109+	DC	HL1' 1'	m5 used
00009399	03			7110+	DC	HL1' 3'	CC
0000939A	0E			7111+	DC	HL1' 14'	CC failed mask
0000939C	00000000 00000000			7112+	DS	2F	extracted PSW after test (has CC)
000093A4	FF			7113+	DC	X' FF'	extracted CC, if test failed
000093A5	E5C3C840 40404040			7114+	DC	CL8' VCH'	instruction name
000093B0	00009428			7115+	DC	A(RE168)	address of v1 result
000093B4	00009438			7116+	DC	A(RE168+16)	address of v2 source
000093B8	00009448			7117+	DC	A(RE168+32)	address of v3 source
000093BC	00000010			7118+	DC	A(16)	result length
000093C0	00009428			7119+REA168	DC	A(RE168)	result address
000093C8	00000000 00000000			7120+	DS	2FD	gap
000093D0	00000000 00000000						
000093D8	00000000 00000000			7121+V10168	DS	XL16	V1 output
000093E0	00000000 00000000						
000093E8	00000000 00000000			7122+	DS	2FD	gap
000093F0	00000000 00000000						
000093F8				7123+*			
000093F8	E310 5024 0014		00000024	7124+X168	DS	0F	
000093FE	E761 0000 0806		00000000	7125+	LGF	R1, V2ADDR	load v2 source
00009404	E310 5028 0014		00000028	7126+	VL	v22, 0(R1)	use v21 to test decoder
0000940A	E771 0000 0806		00000000	7127+	LGF	R1, V3ADDR	load v3 source
00009410	E756 7010 2EFB			7128+	VL	v23, 0(R1)	use v22 to test decoder
00009416	B98D 0020			7129+	VCH	V21, V22, V23, 2, 1	test instruction
00009416	B98D 0020			7130+	EPSW	R2, R0	extract psw
0000941A	5020 500C		0000000C	7131+	ST	R2, CCPSW	to save CC
0000941E	E750 5048 080E		000093D8	7132+	VST	V21, V10168	save v1 output
00009424	07FB			7133+	BR	R11	return
00009428				7134+RE168	DC	0F	V1 for this test
00009428				7135+	DROP	R5	
00009428	00000000 00000000			7136	DC	XL16' 0000000000000000 0000000000000000'	result t

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009430	00000000	00000000					
00009438	FFFEFFFD	FFFCFFFB		7137	DC	XL16' FFFEFFFDFFFCFFFB FFFAFFF9FFF8FFF7'	v2
00009440	FFFAFFF9	FFF8FFF7					
00009448	01110233	11550677		7138	DC	XL16' 0111023311550677 08090A0B0C0D0E0F'	v3
00009450	08090A0B	0C0D0E0F					
				7139			
				7140	*Doubleword		
				7141	VRR_B	VCH, 3, 0	
00009458				7142+	DS	0FD	
00009458		00009458		7143+	USING	*, R5	base for test data and test routine
00009458	000094C0			7144+T169	DC	A(X169)	address of test routine
0000945C	00A9			7145+	DC	H' 169'	test number
0000945E	00			7146+	DC	X' 00'	
0000945F	03			7147+	DC	HL1' 3'	m4 used
00009460	01			7148+	DC	HL1' 1'	m5 used
00009461	00			7149+	DC	HL1' 0'	CC
00009462	07			7150+	DC	HL1' 7'	CC failed mask
00009464	00000000	00000000		7151+	DS	2F	extracted PSW after test (has CC)
0000946C	FF			7152+	DC	X' FF'	extracted CC, if test failed
0000946D	E5C3C840	40404040		7153+	DC	CL8' VCH'	instruction name
00009478	000094F0			7154+	DC	A(RE169)	address of v1 result
0000947C	00009500			7155+	DC	A(RE169+16)	address of v2 source
00009480	00009510			7156+	DC	A(RE169+32)	address of v3 source
00009484	00000010			7157+	DC	A(16)	result length
00009488	000094F0			7158+REA169	DC	A(RE169)	result address
00009490	00000000	00000000		7159+	DS	2FD	gap
00009498	00000000	00000000					
000094A0	00000000	00000000		7160+V10169	DS	XL16	V1 output
000094A8	00000000	00000000					
000094B0	00000000	00000000		7161+	DS	2FD	gap
000094B8	00000000	00000000					
				7162+*			
000094C0				7163+X169	DS	0F	
000094C0	E310 5024 0014		00000024	7164+	LGF	R1, V2ADDR	load v2 source
000094C6	E761 0000 0806		00000000	7165+	VL	v22, 0(R1)	use v21 to test decoder
000094CC	E310 5028 0014		00000028	7166+	LGF	R1, V3ADDR	load v3 source
000094D2	E771 0000 0806		00000000	7167+	VL	v23, 0(R1)	use v22 to test decoder
000094D8	E756 7010 3EFB			7168+	VCH	V21, V22, V23, 3, 1	test instruction
000094DE	B98D 0020			7169+	EPSW	R2, R0	extract psw
000094E2	5020 500C		0000000C	7170+	ST	R2, CCPSW	to save CC
000094E6	E750 5048 080E		000094A0	7171+	VST	V21, V10169	save v1 output
000094EC	07FB			7172+	BR	R11	return
000094F0				7173+RE169	DC	0F	V1 for this test
000094F0				7174+	DROP	R5	
000094F0	FFFFFFFF	FFFFFFFF		7175	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000094F8	FFFFFFFF	FFFFFFFF					
00009500	01020304	05060708		7176	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
00009508	090A0B0C	0D0E0F10					
00009510	00010203	04050607		7177	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00009518	08090A0B	0C0D0E0F					
				7178			
				7179	VRR_B	VCH, 3, 0	
00009520				7180+	DS	0FD	
00009520		00009520		7181+	USING	*, R5	base for test data and test routine
00009520	00009588			7182+T170	DC	A(X170)	address of test routine
00009524	00AA			7183+	DC	H' 170'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009526	00			7184+	DC	X' 00'	
00009527	03			7185+	DC	HL1' 3'	m4 used
00009528	01			7186+	DC	HL1' 1'	m5 used
00009529	00			7187+	DC	HL1' 0'	CC
0000952A	07			7188+	DC	HL1' 7'	CC failed mask
0000952C	00000000	00000000		7189+	DS	2F	extracted PSW after test (has CC)
00009534	FF			7190+	DC	X' FF'	extracted CC, if test failed
00009535	E5C3C840	40404040		7191+	DC	CL8' VCH'	instruction name
00009540	000095B8			7192+	DC	A(RE170)	address of v1 result
00009544	000095C8			7193+	DC	A(RE170+16)	address of v2 source
00009548	000095D8			7194+	DC	A(RE170+32)	address of v3 source
0000954C	00000010			7195+	DC	A(16)	result length
00009550	000095B8			7196+REA170	DC	A(RE170)	result address
00009558	00000000	00000000		7197+	DS	2FD	gap
00009560	00000000	00000000					
00009568	00000000	00000000		7198+V10170	DS	XL16	V1 output
00009570	00000000	00000000					
00009578	00000000	00000000		7199+	DS	2FD	gap
00009580	00000000	00000000					
00009588				7200+*			
00009588	E310 5024 0014		00000024	7201+X170	DS	0F	
0000958E	E761 0000 0806		00000000	7202+	LGF	R1, V2ADDR	load v2 source
00009594	E310 5028 0014		00000028	7203+	VL	v22, 0(R1)	use v21 to test decoder
0000959A	E771 0000 0806		00000000	7204+	LGF	R1, V3ADDR	load v3 source
000095A0	E756 7010 3EFB			7205+	VL	v23, 0(R1)	use v22 to test decoder
000095A6	B98D 0020			7206+	VCH	V21, V22, V23, 3, 1	test instruction
000095AA	5020 500C		0000000C	7207+	EPSW	R2, R0	extract psw
000095AE	E750 5048 080E		00009568	7208+	ST	R2, CCPSW	to save CC
000095B4	07FB			7209+	VST	V21, V10170	save v1 output
000095B8				7210+	BR	R11	return
000095B8				7211+RE170	DC	0F	V1 for this test
000095B8				7212+	DROP	R5	
000095B8	FFFFFFFF FFFFFFFF			7213	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000095C0	FFFFFFFF FFFFFFFF						
000095C8	00010203 04050607			7214	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000095D0	08090A0B 0C0D0E0F						
000095D8	FFFEFFFD FFFCFFFB			7215	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
000095E0	FFFAFFF9 FFF8FFF7						
000095E8				7216			
000095E8				7217	VRR_B	VCH, 3, 1	
000095E8	00009650	000095E8		7218+	DS	0FD	
000095E8				7219+	USING	*, R5	base for test data and test routine
000095EC	00AB			7220+T171	DC	A(X171)	address of test routine
000095EE	00			7221+	DC	H' 171'	test number
000095EF	03			7222+	DC	X' 00'	
000095F0	01			7223+	DC	HL1' 3'	m4 used
000095F1	01			7224+	DC	HL1' 1'	m5 used
000095F2	0B			7225+	DC	HL1' 1'	CC
000095F4	00000000	00000000		7226+	DC	HL1' 11'	CC failed mask
000095FC	FF			7227+	DS	2F	extracted PSW after test (has CC)
000095FD	E5C3C840	40404040		7228+	DC	X' FF'	extracted CC, if test failed
00009608	00009680			7229+	DC	CL8' VCH'	instruction name
0000960C	00009690			7230+	DC	A(RE171)	address of v1 result
00009610	000096A0			7231+	DC	A(RE171+16)	address of v2 source
00009614	00000010			7232+	DC	A(RE171+32)	address of v3 source
				7233+	DC	A(16)	result length



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009618	00009680			7234+REA171	DC	A(RE171)	result address
00009620	00000000 00000000			7235+	DS	2FD	gap
00009628	00000000 00000000						
00009630	00000000 00000000			7236+V10171	DS	XL16	V1 output
00009638	00000000 00000000						
00009640	00000000 00000000			7237+	DS	2FD	gap
00009648	00000000 00000000						
				7238+*			
00009650				7239+X171	DS	0F	
00009650	E310 5024 0014		00000024	7240+	LGF	R1, V2ADDR	load v2 source
00009656	E761 0000 0806		00000000	7241+	VL	v22, 0(R1)	use v21 to test decoder
0000965C	E310 5028 0014		00000028	7242+	LGF	R1, V3ADDR	load v3 source
00009662	E771 0000 0806		00000000	7243+	VL	v23, 0(R1)	use v22 to test decoder
00009668	E756 7010 3EFB			7244+	VCH	V21, V22, V23, 3, 1	test instruction
0000966E	B98D 0020			7245+	EPSW	R2, R0	extract psw
00009672	5020 500C		0000000C	7246+	ST	R2, CCPSW	to save CC
00009676	E750 5048 080E		00009630	7247+	VST	V21, V10171	save v1 output
0000967C	07FB			7248+	BR	R11	return
00009680				7249+RE171	DC	0F	V1 for this test
00009680				7250+	DROP	R5	
00009680	FFFFFFFF FFFFFFFF			7251	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result
00009688	00000000 00000000						
00009690	00110033 00550077			7252	DC	XL16' 0011003300550077 08090A0B0C0DFE0F'	v2
00009698	08090A0B 0C0DFE0F						
000096A0	00010203 04050067			7253	DC	XL16' 0001020304050067 08090A0B0C0DFE1F'	v3
000096A8	08090A0B 0C0DFE1F						
				7254			
				7255	VRR_B	VCH, 3, 1	
000096B0				7256+	DS	0FD	
000096B0		000096B0		7257+	USING	*, R5	base for test data and test routine
000096B0	00009718			7258+T172	DC	A(X172)	address of test routine
000096B4	00AC			7259+	DC	H' 172'	test number
000096B6	00			7260+	DC	X' 00'	
000096B7	03			7261+	DC	HL1' 3'	m4 used
000096B8	01			7262+	DC	HL1' 1'	m5 used
000096B9	01			7263+	DC	HL1' 1'	CC
000096BA	0B			7264+	DC	HL1' 11'	CC failed mask
000096BC	00000000 00000000			7265+	DS	2F	extracted PSW after test (has CC)
000096C4	FF			7266+	DC	X' FF'	extracted CC, if test failed
000096C5	E5C3C840 40404040			7267+	DC	CL8' VCH'	instruction name
000096D0	00009748			7268+	DC	A(RE172)	address of v1 result
000096D4	00009758			7269+	DC	A(RE172+16)	address of v2 source
000096D8	00009768			7270+	DC	A(RE172+32)	address of v3 source
000096DC	00000010			7271+	DC	A(16)	result length
000096E0	00009748			7272+REA172	DC	A(RE172)	result address
000096E8	00000000 00000000			7273+	DS	2FD	gap
000096F0	00000000 00000000						
000096F8	00000000 00000000			7274+V10172	DS	XL16	V1 output
00009700	00000000 00000000						
00009708	00000000 00000000			7275+	DS	2FD	gap
00009710	00000000 00000000						
				7276+*			
00009718				7277+X172	DS	0F	
00009718	E310 5024 0014		00000024	7278+	LGF	R1, V2ADDR	load v2 source
0000971E	E761 0000 0806		00000000	7279+	VL	v22, 0(R1)	use v21 to test decoder
00009724	E310 5028 0014		00000028	7280+	LGF	R1, V3ADDR	load v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
0000972A	E771 0000 0806		00000000	7281+	VL	v23, 0(R1)	use v22 to test decoder	
00009730	E756 7010 3EFB			7282+	VCH	V21, V22, V23, 3, 1	test instruction	
00009736	B98D 0020			7283+	EPSW	R2, R0	extract psw	
0000973A	5020 500C		0000000C	7284+	ST	R2, CCPSW	to save CC	
0000973E	E750 5048 080E		000096F8	7285+	VST	V21, V10172	save v1 output	
00009744	07FB			7286+	BR	R11	return	
00009748				7287+RE172	DC	0F	V1 for this test	
00009748				7288+	DROP	R5		
00009748	00000000 00000000			7289	DC	XL16' 0000000000000000 0000000000000000	result t	
00009750	FFFFFFFF FFFFFFFF							
00009758	08090A0B 0C0DFE0F			7290	DC	XL16' 08090A0B0C0DFE0F 0011003300550077'	v2	
00009760	00110033 00550077							
00009768	08090A0B 0C0DFE1F			7291	DC	XL16' 08090A0B0C0DFE1F 0001020304050067'	v3	
00009770	00010203 04050067							
				7292				
				7293	VRR_B	VCH, 3, 1		
00009778				7294+	DS	0FD		
00009778		00009778		7295+	USING	*, R5	base for test data and test routine	
00009778	000097E0			7296+T173	DC	A(X173)	address of test routine	
0000977C	00AD			7297+	DC	H' 173'	test number	
0000977E	00			7298+	DC	X' 00'		
0000977F	03			7299+	DC	HL1' 3'	m4 used	
00009780	01			7300+	DC	HL1' 1'	m5 used	
00009781	01			7301+	DC	HL1' 1'	CC	
00009782	0B			7302+	DC	HL1' 11'	CC failed mask	
00009784	00000000 00000000			7303+	DS	2F	extracted PSW after test (has CC)	
0000978C	FF			7304+	DC	X' FF'	extracted CC, if test failed	
0000978D	E5C3C840 40404040			7305+	DC	CL8' VCH'	instruction name	
00009798	00009810			7306+	DC	A(RE173)	address of v1 result	
0000979C	00009820			7307+	DC	A(RE173+16)	address of v2 source	
000097A0	00009830			7308+	DC	A(RE173+32)	address of v3 source	
000097A4	00000010			7309+	DC	A(16)	result length	
000097A8	00009810			7310+REA173	DC	A(RE173)	result address	
000097B0	00000000 00000000			7311+	DS	2FD	gap	
000097B8	00000000 00000000							
000097C0	00000000 00000000			7312+V10173	DS	XL16	V1 output	
000097C8	00000000 00000000							
000097D0	00000000 00000000			7313+	DS	2FD	gap	
000097D8	00000000 00000000							
				7314+*				
000097E0				7315+X173	DS	0F		
000097E0	E310 5024 0014		00000024	7316+	LGF	R1, V2ADDR	load v2 source	
000097E6	E761 0000 0806		00000000	7317+	VL	v22, 0(R1)	use v21 to test decoder	
000097EC	E310 5028 0014		00000028	7318+	LGF	R1, V3ADDR	load v3 source	
000097F2	E771 0000 0806		00000000	7319+	VL	v23, 0(R1)	use v22 to test decoder	
000097F8	E756 7010 3EFB			7320+	VCH	V21, V22, V23, 3, 1	test instruction	
000097FE	B98D 0020			7321+	EPSW	R2, R0	extract psw	
00009802	5020 500C		0000000C	7322+	ST	R2, CCPSW	to save CC	
00009806	E750 5048 080E		000097C0	7323+	VST	V21, V10173	save v1 output	
0000980C	07FB			7324+	BR	R11	return	
00009810				7325+RE173	DC	0F	V1 for this test	
00009810				7326+	DROP	R5		
00009810	FFFFFFFF FFFFFFFF			7327	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result t	
00009818	00000000 00000000							
00009820	00010203 04050607			7328	DC	XL16' 0001020304050607 FFFAFF9FFF8FFF7'	v2	
00009828	FFFAFFF9 FFF8FFF7							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00009830	FFFEFFFD FFFCFFFB			7329	DC	XL16' FFEFFFDFFFCFFFB	08090A0B0C0D0E0F'	v3
00009838	08090A0B 0C0D0E0F							
				7330				
				7331	VRR_B	VCH, 3, 3		
00009840				7332+	DS	0FD		
00009840		00009840		7333+	USING	*, R5	base for test data and test routine	
00009840	000098A8			7334+T174	DC	A(X174)	address of test routine	
00009844	00AE			7335+	DC	H' 174'	test number	
00009846	00			7336+	DC	X' 00'		
00009847	03			7337+	DC	HL1' 3'	m4 used	
00009848	01			7338+	DC	HL1' 1'	m5 used	
00009849	03			7339+	DC	HL1' 3'	CC	
0000984A	0E			7340+	DC	HL1' 14'	CC failed mask	
0000984C	00000000 00000000			7341+	DS	2F	extracted PSW after test (has CC)	
00009854	FF			7342+	DC	X' FF'	extracted CC, if test failed	
00009855	E5C3C840 40404040			7343+	DC	CL8' VCH'	instruction name	
00009860	000098D8			7344+	DC	A(RE174)	address of v1 result	
00009864	000098E8			7345+	DC	A(RE174+16)	address of v2 source	
00009868	000098F8			7346+	DC	A(RE174+32)	address of v3 source	
0000986C	00000010			7347+	DC	A(16)	result length	
00009870	000098D8			7348+REA174	DC	A(RE174)	result address	
00009878	00000000 00000000			7349+	DS	2FD	gap	
00009880	00000000 00000000							
00009888	00000000 00000000			7350+V10174	DS	XL16	V1 output	
00009890	00000000 00000000							
00009898	00000000 00000000			7351+	DS	2FD	gap	
000098A0	00000000 00000000							
				7352+*				
000098A8				7353+X174	DS	0F		
000098A8	E310 5024 0014		00000024	7354+	LGF	R1, V2ADDR	load v2 source	
000098AE	E761 0000 0806		00000000	7355+	VL	v22, 0(R1)	use v21 to test decoder	
000098B4	E310 5028 0014		00000028	7356+	LGF	R1, V3ADDR	load v3 source	
000098BA	E771 0000 0806		00000000	7357+	VL	v23, 0(R1)	use v22 to test decoder	
000098C0	E756 7010 3EFB			7358+	VCH	V21, V22, V23, 3, 1	test instruction	
000098C6	B98D 0020			7359+	EPSW	R2, R0	extract psw	
000098CA	5020 500C		0000000C	7360+	ST	R2, CCPSW	to save CC	
000098CE	E750 5048 080E		00009888	7361+	VST	V21, V10174	save v1 output	
000098D4	07FB			7362+	BR	R11	return	
000098D8				7363+RE174	DC	0F	V1 for this test	
000098D8				7364+	DROP	R5		
000098D8	00000000 00000000			7365	DC	XL16' 0000000000000000 0000000000000000'	result t	
000098E0	00000000 00000000							
000098E8	00010003 04050607			7366	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2	
000098F0	00090A0B 0C0D0E0F							
000098F8	01110233 11550677			7367	DC	XL16' 0111023311550677 1179116B514D312F'	v3	
00009900	1179116B 514D312F							
				7368				
				7369	VRR_B	VCHL, 3, 3		
00009908				7370+	DS	0FD		
00009908		00009908		7371+	USING	*, R5	base for test data and test routine	
00009908	00009970			7372+T175	DC	A(X175)	address of test routine	
0000990C	00AF			7373+	DC	H' 175'	test number	
0000990E	00			7374+	DC	X' 00'		
0000990F	03			7375+	DC	HL1' 3'	m4 used	
00009910	01			7376+	DC	HL1' 1'	m5 used	
00009911	03			7377+	DC	HL1' 3'	CC	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009912	0E			7378+	DC	HL1' 14'	CC failed mask
00009914	00000000 00000000			7379+	DS	2F	extracted PSW after test (has CC)
0000991C	FF			7380+	DC	X' FF'	extracted CC, if test failed
0000991D	E5C3C8D3 40404040			7381+	DC	CL8' VCHL'	instruction name
00009928	000099A0			7382+	DC	A(RE175)	address of v1 result
0000992C	000099B0			7383+	DC	A(RE175+16)	address of v2 source
00009930	000099C0			7384+	DC	A(RE175+32)	address of v3 source
00009934	00000010			7385+	DC	A(16)	result length
00009938	000099A0			7386+REA175	DC	A(RE175)	result address
00009940	00000000 00000000			7387+	DS	2FD	gap
00009948	00000000 00000000						
00009950	00000000 00000000			7388+V10175	DS	XL16	V1 output
00009958	00000000 00000000						
00009960	00000000 00000000			7389+	DS	2FD	gap
00009968	00000000 00000000						
00009970				7390+*			
00009970	E310 5024 0014		00000024	7391+X175	DS	0F	
00009976	E761 0000 0806		00000000	7392+	LGF	R1, V2ADDR	load v2 source
0000997C	E310 5028 0014		00000028	7393+	VL	v22, 0(R1)	use v21 to test decoder
00009982	E771 0000 0806		00000000	7394+	LGF	R1, V3ADDR	load v3 source
00009988	E756 7010 3EF9		00000000	7395+	VL	v23, 0(R1)	use v22 to test decoder
0000998E	B98D 0020			7396+	VCHL	V21, V22, V23, 3, 1	test instruction
00009992	5020 500C		0000000C	7397+	EPSW	R2, R0	extract psw
00009996	E750 5048 080E		00009950	7398+	ST	R2, CCPSW	to save CC
0000999C	07FB			7399+	VST	V21, V10175	save v1 output
000099A0				7400+	BR	R11	return
000099A0				7401+RE175	DC	0F	V1 for this test
000099A0	00000000 00000000			7402+	DROP	R5	
000099A8	00000000 00000000			7403	DC	XL16' 0000000000000000 0000000000000000'	result t
000099B0	08090A0B 0C0D0E0F			7404	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
000099B8	00010203 04050607						
000099C0	1179116B 514D312F			7405	DC	XL16' 1179116B514D312F 0111023311550677'	v3
000099C8	01110233 11550677						
000099D0				7406			
000099D0		000099D0		7407	VRR_B	VCH, 3, 3	
000099D0	00009A38			7408+	DS	0FD	
000099D4	00B0			7409+	USING	*, R5	base for test data and test routine
000099D6	00			7410+T176	DC	A(X176)	address of test routine
000099D7	03			7411+	DC	H' 176'	test number
000099D8	01			7412+	DC	X' 00'	
000099D9	03			7413+	DC	HL1' 3'	m4 used
000099DA	0E			7414+	DC	HL1' 1'	m5 used
000099DC	00000000 00000000			7415+	DC	HL1' 3'	CC
000099E4	FF			7416+	DC	HL1' 14'	CC failed mask
000099E5	E5C3C840 40404040			7417+	DS	2F	extracted PSW after test (has CC)
000099F0	00009A68			7418+	DC	X' FF'	extracted CC, if test failed
000099F4	00009A78			7419+	DC	CL8' VCH'	instruction name
000099F8	00009A88			7420+	DC	A(RE176)	address of v1 result
000099FC	00000010			7421+	DC	A(RE176+16)	address of v2 source
00009A00	00009A68			7422+	DC	A(RE176+32)	address of v3 source
00009A08	00000000 00000000			7423+	DC	A(16)	result length
00009A10	00000000 00000000			7424+REA176	DC	A(RE176)	result address
00009A18	00000000 00000000			7425+	DS	2FD	gap
				7426+V10176	DS	XL16	V1 output





LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				7449 *	
				7450 * table of pointers to individual tests	
				7451 *	
00009AA0				7452 E7TESTS DS OF	
				7453 PTTABLE	
00009AA0				7454+TTABLE DS OF	
00009AA0	00001118			7455+	DC A(T1) test address
00009AA4	000011E0			7456+	DC A(T2) test address
00009AA8	000012A8			7457+	DC A(T3) test address
00009AAC	00001370			7458+	DC A(T4) test address
00009AB0	00001438			7459+	DC A(T5) test address
00009AB4	00001500			7460+	DC A(T6) test address
00009AB8	000015C8			7461+	DC A(T7) test address
00009ABC	00001690			7462+	DC A(T8) test address
00009AC0	00001758			7463+	DC A(T9) test address
00009AC4	00001820			7464+	DC A(T10) test address
00009AC8	000018E8			7465+	DC A(T11) test address
00009ACC	000019B0			7466+	DC A(T12) test address
00009AD0	00001A78			7467+	DC A(T13) test address
00009AD4	00001B40			7468+	DC A(T14) test address
00009AD8	00001C08			7469+	DC A(T15) test address
00009ADC	00001CD0			7470+	DC A(T16) test address
00009AE0	00001D98			7471+	DC A(T17) test address
00009AE4	00001E60			7472+	DC A(T18) test address
00009AE8	00001F28			7473+	DC A(T19) test address
00009AEC	00001FF0			7474+	DC A(T20) test address
00009AF0	000020B8			7475+	DC A(T21) test address
00009AF4	00002180			7476+	DC A(T22) test address
00009AF8	00002248			7477+	DC A(T23) test address
00009AFC	00002310			7478+	DC A(T24) test address
00009B00	000023D8			7479+	DC A(T25) test address
00009B04	000024A0			7480+	DC A(T26) test address
00009B08	00002568			7481+	DC A(T27) test address
00009B0C	00002630			7482+	DC A(T28) test address
00009B10	000026F8			7483+	DC A(T29) test address
00009B14	000027C0			7484+	DC A(T30) test address
00009B18	00002888			7485+	DC A(T31) test address
00009B1C	00002950			7486+	DC A(T32) test address
00009B20	00002A18			7487+	DC A(T33) test address
00009B24	00002AE0			7488+	DC A(T34) test address
00009B28	00002BA8			7489+	DC A(T35) test address
00009B2C	00002C70			7490+	DC A(T36) test address
00009B30	00002D38			7491+	DC A(T37) test address
00009B34	00002E00			7492+	DC A(T38) test address
00009B38	00002EC8			7493+	DC A(T39) test address
00009B3C	00002F90			7494+	DC A(T40) test address
00009B40	00003058			7495+	DC A(T41) test address
00009B44	00003120			7496+	DC A(T42) test address
00009B48	000031E8			7497+	DC A(T43) test address
00009B4C	000032B0			7498+	DC A(T44) test address
00009B50	00003378			7499+	DC A(T45) test address
00009B54	00003440			7500+	DC A(T46) test address
00009B58	00003508			7501+	DC A(T47) test address
00009B5C	000035D0			7502+	DC A(T48) test address
00009B60	00003698			7503+	DC A(T49) test address
00009B64	00003760			7504+	DC A(T50) test address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009B68	00003828			7505+	DC	A(T51)	test address
00009B6C	000038F0			7506+	DC	A(T52)	test address
00009B70	000039B8			7507+	DC	A(T53)	test address
00009B74	00003A80			7508+	DC	A(T54)	test address
00009B78	00003B48			7509+	DC	A(T55)	test address
00009B7C	00003C10			7510+	DC	A(T56)	test address
00009B80	00003CD8			7511+	DC	A(T57)	test address
00009B84	00003DA0			7512+	DC	A(T58)	test address
00009B88	00003E68			7513+	DC	A(T59)	test address
00009B8C	00003F30			7514+	DC	A(T60)	test address
00009B90	00003FF8			7515+	DC	A(T61)	test address
00009B94	000040C0			7516+	DC	A(T62)	test address
00009B98	00004188			7517+	DC	A(T63)	test address
00009B9C	00004250			7518+	DC	A(T64)	test address
00009BA0	00004318			7519+	DC	A(T65)	test address
00009BA4	000043E0			7520+	DC	A(T66)	test address
00009BA8	000044A8			7521+	DC	A(T67)	test address
00009BAC	00004570			7522+	DC	A(T68)	test address
00009BB0	00004638			7523+	DC	A(T69)	test address
00009BB4	00004700			7524+	DC	A(T70)	test address
00009BB8	000047C8			7525+	DC	A(T71)	test address
00009BBC	00004890			7526+	DC	A(T72)	test address
00009BC0	00004958			7527+	DC	A(T73)	test address
00009BC4	00004A20			7528+	DC	A(T74)	test address
00009BC8	00004AE8			7529+	DC	A(T75)	test address
00009BCC	00004BB0			7530+	DC	A(T76)	test address
00009BD0	00004C78			7531+	DC	A(T77)	test address
00009BD4	00004D40			7532+	DC	A(T78)	test address
00009BD8	00004E08			7533+	DC	A(T79)	test address
00009BDC	00004ED0			7534+	DC	A(T80)	test address
00009BE0	00004F98			7535+	DC	A(T81)	test address
00009BE4	00005060			7536+	DC	A(T82)	test address
00009BE8	00005128			7537+	DC	A(T83)	test address
00009BEC	000051F0			7538+	DC	A(T84)	test address
00009BF0	000052B8			7539+	DC	A(T85)	test address
00009BF4	00005380			7540+	DC	A(T86)	test address
00009BF8	00005448			7541+	DC	A(T87)	test address
00009BFC	00005510			7542+	DC	A(T88)	test address
00009C00	000055D8			7543+	DC	A(T89)	test address
00009C04	000056A0			7544+	DC	A(T90)	test address
00009C08	00005768			7545+	DC	A(T91)	test address
00009C0C	00005830			7546+	DC	A(T92)	test address
00009C10	000058F8			7547+	DC	A(T93)	test address
00009C14	000059C0			7548+	DC	A(T94)	test address
00009C18	00005A88			7549+	DC	A(T95)	test address
00009C1C	00005B50			7550+	DC	A(T96)	test address
00009C20	00005C18			7551+	DC	A(T97)	test address
00009C24	00005CE0			7552+	DC	A(T98)	test address
00009C28	00005DA8			7553+	DC	A(T99)	test address
00009C2C	00005E70			7554+	DC	A(T100)	test address
00009C30	00005F38			7555+	DC	A(T101)	test address
00009C34	00006000			7556+	DC	A(T102)	test address
00009C38	000060C8			7557+	DC	A(T103)	test address
00009C3C	00006190			7558+	DC	A(T104)	test address
00009C40	00006258			7559+	DC	A(T105)	test address
00009C44	00006320			7560+	DC	A(T106)	test address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009C48	000063E8			7561+	DC	A(T107)	test address
00009C4C	000064B0			7562+	DC	A(T108)	test address
00009C50	00006578			7563+	DC	A(T109)	test address
00009C54	00006640			7564+	DC	A(T110)	test address
00009C58	00006708			7565+	DC	A(T111)	test address
00009C5C	000067D0			7566+	DC	A(T112)	test address
00009C60	00006898			7567+	DC	A(T113)	test address
00009C64	00006960			7568+	DC	A(T114)	test address
00009C68	00006A28			7569+	DC	A(T115)	test address
00009C6C	00006AF0			7570+	DC	A(T116)	test address
00009C70	00006BB8			7571+	DC	A(T117)	test address
00009C74	00006C80			7572+	DC	A(T118)	test address
00009C78	00006D48			7573+	DC	A(T119)	test address
00009C7C	00006E10			7574+	DC	A(T120)	test address
00009C80	00006ED8			7575+	DC	A(T121)	test address
00009C84	00006FA0			7576+	DC	A(T122)	test address
00009C88	00007068			7577+	DC	A(T123)	test address
00009C8C	00007130			7578+	DC	A(T124)	test address
00009C90	000071F8			7579+	DC	A(T125)	test address
00009C94	000072C0			7580+	DC	A(T126)	test address
00009C98	00007388			7581+	DC	A(T127)	test address
00009C9C	00007450			7582+	DC	A(T128)	test address
00009CA0	00007518			7583+	DC	A(T129)	test address
00009CA4	000075E0			7584+	DC	A(T130)	test address
00009CA8	000076A8			7585+	DC	A(T131)	test address
00009CAC	00007770			7586+	DC	A(T132)	test address
00009CB0	00007838			7587+	DC	A(T133)	test address
00009CB4	00007900			7588+	DC	A(T134)	test address
00009CB8	000079C8			7589+	DC	A(T135)	test address
00009CBC	00007A90			7590+	DC	A(T136)	test address
00009CC0	00007B58			7591+	DC	A(T137)	test address
00009CC4	00007C20			7592+	DC	A(T138)	test address
00009CC8	00007CE8			7593+	DC	A(T139)	test address
00009CCC	00007DB0			7594+	DC	A(T140)	test address
00009CD0	00007E78			7595+	DC	A(T141)	test address
00009CD4	00007F40			7596+	DC	A(T142)	test address
00009CD8	00008008			7597+	DC	A(T143)	test address
00009CDC	000080D0			7598+	DC	A(T144)	test address
00009CE0	00008198			7599+	DC	A(T145)	test address
00009CE4	00008260			7600+	DC	A(T146)	test address
00009CE8	00008328			7601+	DC	A(T147)	test address
00009CEC	000083F0			7602+	DC	A(T148)	test address
00009CF0	000084B8			7603+	DC	A(T149)	test address
00009CF4	00008580			7604+	DC	A(T150)	test address
00009CF8	00008648			7605+	DC	A(T151)	test address
00009CFC	00008710			7606+	DC	A(T152)	test address
00009D00	000087D8			7607+	DC	A(T153)	test address
00009D04	000088A0			7608+	DC	A(T154)	test address
00009D08	00008968			7609+	DC	A(T155)	test address
00009D0C	00008A30			7610+	DC	A(T156)	test address
00009D10	00008AF8			7611+	DC	A(T157)	test address
00009D14	00008BC0			7612+	DC	A(T158)	test address
00009D18	00008C88			7613+	DC	A(T159)	test address
00009D1C	00008D50			7614+	DC	A(T160)	test address
00009D20	00008E18			7615+	DC	A(T161)	test address
00009D24	00008EE0			7616+	DC	A(T162)	test address



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009D28	00008FA8			7617+	DC	A(T163)	test address
00009D2C	00009070			7618+	DC	A(T164)	test address
00009D30	00009138			7619+	DC	A(T165)	test address
00009D34	00009200			7620+	DC	A(T166)	test address
00009D38	000092C8			7621+	DC	A(T167)	test address
00009D3C	00009390			7622+	DC	A(T168)	test address
00009D40	00009458			7623+	DC	A(T169)	test address
00009D44	00009520			7624+	DC	A(T170)	test address
00009D48	000095E8			7625+	DC	A(T171)	test address
00009D4C	000096B0			7626+	DC	A(T172)	test address
00009D50	00009778			7627+	DC	A(T173)	test address
00009D54	00009840			7628+	DC	A(T174)	test address
00009D58	00009908			7629+	DC	A(T175)	test address
00009D5C	000099D0			7630+	DC	A(T176)	test address
				7631+*			
00009D60	00000000			7632+	DC	A(0)	end of table
00009D64	00000000			7633+	DC	A(0)	end of table
				7634			
00009D68	00000000			7635	DC	F' 0'	END OF TABLE
00009D6C	00000000			7636	DC	F' 0'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				7638	*****
				7639	*            Register equates
				7640	*****
		00000000	00000001	7642 R0	EQU 0
		00000001	00000001	7643 R1	EQU 1
		00000002	00000001	7644 R2	EQU 2
		00000003	00000001	7645 R3	EQU 3
		00000004	00000001	7646 R4	EQU 4
		00000005	00000001	7647 R5	EQU 5
		00000006	00000001	7648 R6	EQU 6
		00000007	00000001	7649 R7	EQU 7
		00000008	00000001	7650 R8	EQU 8
		00000009	00000001	7651 R9	EQU 9
		0000000A	00000001	7652 R10	EQU 10
		0000000B	00000001	7653 R11	EQU 11
		0000000C	00000001	7654 R12	EQU 12
		0000000D	00000001	7655 R13	EQU 13
		0000000E	00000001	7656 R14	EQU 14
		0000000F	00000001	7657 R15	EQU 15
				7659	*****
				7660	*            Register equates
				7661	*****
		00000000	00000001	7663 V0	EQU 0
		00000001	00000001	7664 V1	EQU 1
		00000002	00000001	7665 V2	EQU 2
		00000003	00000001	7666 V3	EQU 3
		00000004	00000001	7667 V4	EQU 4
		00000005	00000001	7668 V5	EQU 5
		00000006	00000001	7669 V6	EQU 6
		00000007	00000001	7670 V7	EQU 7
		00000008	00000001	7671 V8	EQU 8
		00000009	00000001	7672 V9	EQU 9
		0000000A	00000001	7673 V10	EQU 10
		0000000B	00000001	7674 V11	EQU 11
		0000000C	00000001	7675 V12	EQU 12
		0000000D	00000001	7676 V13	EQU 13
		0000000E	00000001	7677 V14	EQU 14
		0000000F	00000001	7678 V15	EQU 15
		00000010	00000001	7679 V16	EQU 16
		00000011	00000001	7680 V17	EQU 17
		00000012	00000001	7681 V18	EQU 18
		00000013	00000001	7682 V19	EQU 19
		00000014	00000001	7683 V20	EQU 20
		00000015	00000001	7684 V21	EQU 21



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES													
BEGIN	I	00000200	2	161	127	157	158	159										
CC	U	00000009	1	522	272													
CCFOUND	X	00000014	1	528	259	279												
CCMASK	U	0000000A	1	523	229													
CCMSG	U	0000031C	1	246	241													
CCPRTEXP	C	00001098	1	487	276													
CCPRTGOT	C	000010A8	1	490	283													
CCPRTLNE	C	00001055	16	482	492	286												
CCPRTLNG	U	00000055	1	492	285													
CCPRTNAME	C	00001082	8	485	269													
CCPRTNUM	C	00001065	3	483	267													
CCPSW	F	0000000C	4	527	256	700	738	776	815	853	891	930	968	1006	1048	1086	1124	
					1162	1200	1238	1277	1315	1353	1391	1429	1467	1506	1544	1582	1620	
					1658	1696	1744	1782	1820	1859	1897	1935	1974	2012	2050	2092	2130	
					2168	2206	2244	2282	2320	2358	2397	2435	2473	2511	2549	2587	2625	
					2663	2702	2740	2778	2816	2854	2892	2930	2968	3016	3054	3092	3131	
					3169	3207	3246	3284	3322	3361	3399	3437	3479	3517	3555	3593	3631	
					3669	3708	3746	3784	3822	3860	3898	3937	3975	4013	4051	4089	4127	
					4166	4204	4242	4280	4318	4356	4404	4442	4480	4519	4557	4595	4634	
					4672	4710	4749	4787	4825	4867	4905	4943	4981	5019	5057	5096	5134	
					5172	5210	5248	5286	5325	5363	5401	5439	5477	5515	5554	5592	5630	
					5668	5706	5744	5792	5830	5868	5907	5945	5983	6022	6060	6098	6137	
					6175	6213	6255	6293	6331	6369	6407	6445	6483	6521	6560	6598	6636	
					6674	6712	6750	6788	6826	6865	6903	6941	6979	7017	7055	7093	7131	
					7170	7208	7246	7284	7322	7360	7398	7436						
CTLRO	F	00000554	4	425	171	172	173	174										
DECNUM	C	000010D6	16	502	264	266	273	275	280	282	302	304	311	313	318	320		
E7TEST	4	00000000	104	516	220													
E7TESTS	F	00009AA0	4	7452	213													
EDIT	X	000010AA	18	497	265	274	281	303	312	319								
ENDTEST	U	00000428	1	340	218													
EOJ	I	00000538	4	415	206	343												
EOJPSW	D	00000528	8	413	415													
FAILCONT	U	00000418	1	330														
FAILED	F	00001000	4	455	290	332	341											
FAILMSG	U	000003B0	1	300	236													
FAILPSW	D	00000540	8	417	419													
FAILTEST	I	00000550	4	419	344													
FB0001	F	00000280	8	190	194	195	197											
IMAGE	1	00000000	40304	0														
K	U	00000400	1	439	440	441	442											
K64	U	00010000	1	441														
M4	U	00000007	1	520	310													
M5	U	00000008	1	521	250	317												
MB	U	00100000	1	442														
MSG	I	00000470	4	375	205	358												
MSGCMD	C	000004BE	9	405	388	389												
MSGMSG	C	000004C7	95	406	382	403	380											
MSGMVC	I	000004B8	6	403	386													
MSGOK	I	00000486	2	384	381													
MSGRET	I	000004A6	4	399	392	395												
MSGSAVE	F	000004AC	4	402	378	399												
NEXTE7	U	000002D4	1	215	239	335												
OPNAME	C	00000015	8	530	269	307												
PAGE	U	00001000	1	440														
PRT3	C	000010C0	18	500	265	266	267	274	275	276	281	282	283	303	304	305	312	



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					313	314	319	320	321								
PRTLNE	C	00001008	16	464	474	324											
PRTLNG	U	0000004D	1	474	323												
PRTM4	C	00001044	3	469	314												
PRTM5	C	00001051	3	472	321												
PRTNAME	C	00001033	8	467	307												
PRTNUM	C	00001018	3	465	305												
R0	U	00000000	1	7642	121	171	174	194	196	197	198	203	222	223	285	289	290
					323	331	332	357	359	375	378	380	382	384	399	699	737
					775	814	852	890	929	967	1005	1047	1085	1123	1161	1199	1237
					1276	1314	1352	1390	1428	1466	1505	1543	1581	1619	1657	1695	1743
					1781	1819	1858	1896	1934	1973	2011	2049	2091	2129	2167	2205	2243
					2281	2319	2357	2396	2434	2472	2510	2548	2586	2624	2662	2701	2739
					2777	2815	2853	2891	2929	2967	3015	3053	3091	3130	3168	3206	3245
					3283	3321	3360	3398	3436	3478	3516	3554	3592	3630	3668	3707	3745
					3783	3821	3859	3897	3936	3974	4012	4050	4088	4126	4165	4203	4241
					4279	4317	4355	4403	4441	4479	4518	4556	4594	4633	4671	4709	4748
					4786	4824	4866	4904	4942	4980	5018	5056	5095	5133	5171	5209	5247
					5285	5324	5362	5400	5438	5476	5514	5553	5591	5629	5667	5705	5743
					5791	5829	5867	5906	5944	5982	6021	6059	6097	6136	6174	6212	6254
					6292	6330	6368	6406	6444	6482	6520	6559	6597	6635	6673	6711	6749
					6787	6825	6864	6902	6940	6978	7016	7054	7092	7130	7169	7207	7245
					7283	7321	7359	7397	7435								
R1	U	00000001	1	7643	204	229	230	231	234	235	250	251	256	257	258	259	286
					324	341	342	389	403	694	695	696	697	732	733	734	735
					770	771	772	773	809	810	811	812	847	848	849	850	885
					886	887	888	924	925	926	927	962	963	964	965	1000	1001
					1002	1003	1042	1043	1044	1045	1080	1081	1082	1083	1118	1119	1120
					1121	1156	1157	1158	1159	1194	1195	1196	1197	1232	1233	1234	1235
					1271	1272	1273	1274	1309	1310	1311	1312	1347	1348	1349	1350	1385
					1386	1387	1388	1423	1424	1425	1426	1461	1462	1463	1464	1500	1501
					1502	1503	1538	1539	1540	1541	1576	1577	1578	1579	1614	1615	1616
					1617	1652	1653	1654	1655	1690	1691	1692	1693	1738	1739	1740	1741
					1776	1777	1778	1779	1814	1815	1816	1817	1853	1854	1855	1856	1891
					1892	1893	1894	1929	1930	1931	1932	1968	1969	1970	1971	2006	2007
					2008	2009	2044	2045	2046	2047	2086	2087	2088	2089	2124	2125	2126
					2127	2162	2163	2164	2165	2200	2201	2202	2203	2238	2239	2240	2241
					2276	2277	2278	2279	2314	2315	2316	2317	2352	2353	2354	2355	2391
					2392	2393	2394	2429	2430	2431	2432	2467	2468	2469	2470	2505	2506
					2507	2508	2543	2544	2545	2546	2581	2582	2583	2584	2619	2620	2621
					2622	2657	2658	2659	2660	2696	2697	2698	2699	2734	2735	2736	2737
					2772	2773	2774	2775	2810	2811	2812	2813	2848	2849	2850	2851	2886
					2887	2888	2889	2924	2925	2926	2927	2962	2963	2964	2965	3010	3011
					3012	3013	3048	3049	3050	3051	3086	3087	3088	3089	3125	3126	3127
					3128	3163	3164	3165	3166	3201	3202	3203	3204	3240	3241	3242	3243
					3278	3279	3280	3281	3316	3317	3318	3319	3355	3356	3357	3358	3393
					3394	3395	3396	3431	3432	3433	3434	3473	3474	3475	3476	3511	3512
					3513	3514	3549	3550	3551	3552	3587	3588	3589	3590	3625	3626	3627
					3628	3663	3664	3665	3666	3702	3703	3704	3705	3740	3741	3742	3743
					3778	3779	3780	3781	3816	3817	3818	3819	3854	3855	3856	3857	3892
					3893	3894	3895	3931	3932	3933	3934	3969	3970	3971	3972	4007	4008
					4009	4010	4045	4046	4047	4048	4083	4084	4085	4086	4121	4122	4123
					4124	4160	4161	4162	4163	4198	4199	4200	4201	4236	4237	4238	4239
					4274	4275	4276	4277	4312	4313	4314	4315	4350	4351	4352	4353	4398
					4399	4400	4401	4436	4437	4438	4439	4474	4475	4476	4477	4513	4514
					4515	4516	4551	4552	4553	4554	4589	4590	4591	4592	4628	4629	4630

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					4631	4666	4667	4668	4669	4704	4705	4706	4707	4743	4744	4745	4746
					4781	4782	4783	4784	4819	4820	4821	4822	4861	4862	4863	4864	4899
					4900	4901	4902	4937	4938	4939	4940	4975	4976	4977	4978	5013	5014
					5015	5016	5051	5052	5053	5054	5090	5091	5092	5093	5128	5129	5130
					5131	5166	5167	5168	5169	5204	5205	5206	5207	5242	5243	5244	5245
					5280	5281	5282	5283	5319	5320	5321	5322	5357	5358	5359	5360	5395
					5396	5397	5398	5433	5434	5435	5436	5471	5472	5473	5474	5509	5510
					5511	5512	5548	5549	5550	5551	5586	5587	5588	5589	5624	5625	5626
					5627	5662	5663	5664	5665	5700	5701	5702	5703	5738	5739	5740	5741
					5786	5787	5788	5789	5824	5825	5826	5827	5862	5863	5864	5865	5901
					5902	5903	5904	5939	5940	5941	5942	5977	5978	5979	5980	6016	6017
					6018	6019	6054	6055	6056	6057	6092	6093	6094	6095	6131	6132	6133
					6134	6169	6170	6171	6172	6207	6208	6209	6210	6249	6250	6251	6252
					6287	6288	6289	6290	6325	6326	6327	6328	6363	6364	6365	6366	6401
					6402	6403	6404	6439	6440	6441	6442	6477	6478	6479	6480	6515	6516
					6517	6518	6554	6555	6556	6557	6592	6593	6594	6595	6630	6631	6632
					6633	6668	6669	6670	6671	6706	6707	6708	6709	6744	6745	6746	6747
					6782	6783	6784	6785	6820	6821	6822	6823	6859	6860	6861	6862	6897
					6898	6899	6900	6935	6936	6937	6938	6973	6974	6975	6976	7011	7012
					7013	7014	7049	7050	7051	7052	7087	7088	7089	7090	7125	7126	7127
R10 R11	U	0000000A 0000000B	1 1	7652 7653	7128	7164	7165	7166	7167	7202	7203	7204	7205	7240	7241	7242	7243
					7278	7279	7280	7281	7316	7317	7318	7319	7354	7355	7356	7357	7392
					7393	7394	7395	7430	7431	7432	7433						
					159	168	169										
					226	227	702	740	778	817	855	893	932	970	1008	1050	1088
					1126	1164	1202	1240	1279	1317	1355	1393	1431	1469	1508	1546	1584
					1622	1660	1698	1746	1784	1822	1861	1899	1937	1976	2014	2052	2094
					2132	2170	2208	2246	2284	2322	2360	2399	2437	2475	2513	2551	2589
					2627	2665	2704	2742	2780	2818	2856	2894	2932	2970	3018	3056	3094
					3133	3171	3209	3248	3286	3324	3363	3401	3439	3481	3519	3557	3595
					3633	3671	3710	3748	3786	3824	3862	3900	3939	3977	4015	4053	4091
					4129	4168	4206	4244	4282	4320	4358	4406	4444	4482	4521	4559	4597
					4636	4674	4712	4751	4789	4827	4869	4907	4945	4983	5021	5059	5098
					5136	5174	5212	5250	5288	5327	5365	5403	5441	5479	5517	5556	5594
					5632	5670	5708	5746	5794	5832	5870	5909	5947	5985	6024	6062	6100
					6139	6177	6215	6257	6295	6333	6371	6409	6447	6485	6523	6562	6600
					6638	6676	6714	6752	6790	6828	6867	6905	6943	6981	7019	7057	7095
					7133	7172	7210	7248	7286	7324	7362	7400	7438				
R12	U	0000000C	1	7654	213	216	238	334									
R13	U	0000000D	1	7655													
R14	U	0000000E	1	7656													
R15	U	0000000F	1	7657	287	325	352	362	363								
R2	U	00000002	1	7644	205	263	264	271	272	273	278	279	280	301	302	309	310
					311	316	317	318	357	358	359	376	378	384	385	386	388
					394	399	400	699	700	737	738	775	776	814	815	852	853
					890	891	929	930	967	968	1005	1006	1047	1048	1085	1086	1123
					1124	1161	1162	1199	1200	1237	1238	1276	1277	1314	1315	1352	1353
					1390	1391	1428	1429	1466	1467	1505	1506	1543	1544	1581	1582	1619
					1620	1657	1658	1695	1696	1743	1744	1781	1782	1819	1820	1858	1859
					1896	1897	1934	1935	1973	1974	2011	2012	2049	2050	2091	2092	2129
					2130	2167	2168	2205	2206	2243	2244	2281	2282	2319	2320	2357	2358
					2396	2397	2434	2435	2472	2473	2510	2511	2548	2549	2586	2587	2624
					2625	2662	2663	2701	2702	2739	2740	2777	2778	2815	2816	2853	2854
					2891	2892	2929	2930	2967	2968	3015	3016	3053	3054	3091	3092	3130
					3131	3168	3169	3206	3207	3245	3246	3283	3284	3321	3322	3360	3361
					3398	3399	3436	3437	3478	3479	3516	3517	3554	3555	3592	3593	3630



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE104	F	00006228	4	4675	4656 4657 4658 4660
RE105	F	000062F0	4	4713	4694 4695 4696 4698
RE106	F	000063B8	4	4752	4733 4734 4735 4737
RE107	F	00006480	4	4790	4771 4772 4773 4775
RE108	F	00006548	4	4828	4809 4810 4811 4813
RE109	F	00006610	4	4870	4851 4852 4853 4855
RE11	F	00001980	4	1089	1070 1071 1072 1074
RE110	F	000066D8	4	4908	4889 4890 4891 4893
RE111	F	000067A0	4	4946	4927 4928 4929 4931
RE112	F	00006868	4	4984	4965 4966 4967 4969
RE113	F	00006930	4	5022	5003 5004 5005 5007
RE114	F	000069F8	4	5060	5041 5042 5043 5045
RE115	F	00006AC0	4	5099	5080 5081 5082 5084
RE116	F	00006B88	4	5137	5118 5119 5120 5122
RE117	F	00006C50	4	5175	5156 5157 5158 5160
RE118	F	00006D18	4	5213	5194 5195 5196 5198
RE119	F	00006DE0	4	5251	5232 5233 5234 5236
RE12	F	00001A48	4	1127	1108 1109 1110 1112
RE120	F	00006EA8	4	5289	5270 5271 5272 5274
RE121	F	00006F70	4	5328	5309 5310 5311 5313
RE122	F	00007038	4	5366	5347 5348 5349 5351
RE123	F	00007100	4	5404	5385 5386 5387 5389
RE124	F	000071C8	4	5442	5423 5424 5425 5427
RE125	F	00007290	4	5480	5461 5462 5463 5465
RE126	F	00007358	4	5518	5499 5500 5501 5503
RE127	F	00007420	4	5557	5538 5539 5540 5542
RE128	F	000074E8	4	5595	5576 5577 5578 5580
RE129	F	000075B0	4	5633	5614 5615 5616 5618
RE13	F	00001B10	4	1165	1146 1147 1148 1150
RE130	F	00007678	4	5671	5652 5653 5654 5656
RE131	F	00007740	4	5709	5690 5691 5692 5694
RE132	F	00007808	4	5747	5728 5729 5730 5732
RE133	F	000078D0	4	5795	5776 5777 5778 5780
RE134	F	00007998	4	5833	5814 5815 5816 5818
RE135	F	00007A60	4	5871	5852 5853 5854 5856
RE136	F	00007B28	4	5910	5891 5892 5893 5895
RE137	F	00007BF0	4	5948	5929 5930 5931 5933
RE138	F	00007CB8	4	5986	5967 5968 5969 5971
RE139	F	00007D80	4	6025	6006 6007 6008 6010
RE14	F	00001BD8	4	1203	1184 1185 1186 1188
RE140	F	00007E48	4	6063	6044 6045 6046 6048
RE141	F	00007F10	4	6101	6082 6083 6084 6086
RE142	F	00007FD8	4	6140	6121 6122 6123 6125
RE143	F	000080A0	4	6178	6159 6160 6161 6163
RE144	F	00008168	4	6216	6197 6198 6199 6201
RE145	F	00008230	4	6258	6239 6240 6241 6243
RE146	F	000082F8	4	6296	6277 6278 6279 6281
RE147	F	000083C0	4	6334	6315 6316 6317 6319
RE148	F	00008488	4	6372	6353 6354 6355 6357
RE149	F	00008550	4	6410	6391 6392 6393 6395
RE15	F	00001CA0	4	1241	1222 1223 1224 1226
RE150	F	00008618	4	6448	6429 6430 6431 6433
RE151	F	000086E0	4	6486	6467 6468 6469 6471
RE152	F	000087A8	4	6524	6505 6506 6507 6509
RE153	F	00008870	4	6563	6544 6545 6546 6548
RE154	F	00008938	4	6601	6582 6583 6584 6586



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE155	F	00008A00	4	6639	6620 6621 6622 6624
RE156	F	00008AC8	4	6677	6658 6659 6660 6662
RE157	F	00008B90	4	6715	6696 6697 6698 6700
RE158	F	00008C58	4	6753	6734 6735 6736 6738
RE159	F	00008D20	4	6791	6772 6773 6774 6776
RE16	F	00001D68	4	1280	1261 1262 1263 1265
RE160	F	00008DE8	4	6829	6810 6811 6812 6814
RE161	F	00008EB0	4	6868	6849 6850 6851 6853
RE162	F	00008F78	4	6906	6887 6888 6889 6891
RE163	F	00009040	4	6944	6925 6926 6927 6929
RE164	F	00009108	4	6982	6963 6964 6965 6967
RE165	F	000091D0	4	7020	7001 7002 7003 7005
RE166	F	00009298	4	7058	7039 7040 7041 7043
RE167	F	00009360	4	7096	7077 7078 7079 7081
RE168	F	00009428	4	7134	7115 7116 7117 7119
RE169	F	000094F0	4	7173	7154 7155 7156 7158
RE17	F	00001E30	4	1318	1299 1300 1301 1303
RE170	F	000095B8	4	7211	7192 7193 7194 7196
RE171	F	00009680	4	7249	7230 7231 7232 7234
RE172	F	00009748	4	7287	7268 7269 7270 7272
RE173	F	00009810	4	7325	7306 7307 7308 7310
RE174	F	000098D8	4	7363	7344 7345 7346 7348
RE175	F	000099A0	4	7401	7382 7383 7384 7386
RE176	F	00009A68	4	7439	7420 7421 7422 7424
RE18	F	00001EF8	4	1356	1337 1338 1339 1341
RE19	F	00001FC0	4	1394	1375 1376 1377 1379
RE2	F	00001278	4	741	722 723 724 726
RE20	F	00002088	4	1432	1413 1414 1415 1417
RE21	F	00002150	4	1470	1451 1452 1453 1455
RE22	F	00002218	4	1509	1490 1491 1492 1494
RE23	F	000022E0	4	1547	1528 1529 1530 1532
RE24	F	000023A8	4	1585	1566 1567 1568 1570
RE25	F	00002470	4	1623	1604 1605 1606 1608
RE26	F	00002538	4	1661	1642 1643 1644 1646
RE27	F	00002600	4	1699	1680 1681 1682 1684
RE28	F	000026C8	4	1747	1728 1729 1730 1732
RE29	F	00002790	4	1785	1766 1767 1768 1770
RE3	F	00001340	4	779	760 761 762 764
RE30	F	00002858	4	1823	1804 1805 1806 1808
RE31	F	00002920	4	1862	1843 1844 1845 1847
RE32	F	000029E8	4	1900	1881 1882 1883 1885
RE33	F	00002AB0	4	1938	1919 1920 1921 1923
RE34	F	00002B78	4	1977	1958 1959 1960 1962
RE35	F	00002C40	4	2015	1996 1997 1998 2000
RE36	F	00002D08	4	2053	2034 2035 2036 2038
RE37	F	00002DD0	4	2095	2076 2077 2078 2080
RE38	F	00002E98	4	2133	2114 2115 2116 2118
RE39	F	00002F60	4	2171	2152 2153 2154 2156
RE4	F	00001408	4	818	799 800 801 803
RE40	F	00003028	4	2209	2190 2191 2192 2194
RE41	F	000030F0	4	2247	2228 2229 2230 2232
RE42	F	000031B8	4	2285	2266 2267 2268 2270
RE43	F	00003280	4	2323	2304 2305 2306 2308
RE44	F	00003348	4	2361	2342 2343 2344 2346
RE45	F	00003410	4	2400	2381 2382 2383 2385
RE46	F	000034D8	4	2438	2419 2420 2421 2423

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE47	F	000035A0	4	2476	2457 2458 2459 2461
RE48	F	00003668	4	2514	2495 2496 2497 2499
RE49	F	00003730	4	2552	2533 2534 2535 2537
RE5	F	000014D0	4	856	837 838 839 841
RE50	F	000037F8	4	2590	2571 2572 2573 2575
RE51	F	000038C0	4	2628	2609 2610 2611 2613
RE52	F	00003988	4	2666	2647 2648 2649 2651
RE53	F	00003A50	4	2705	2686 2687 2688 2690
RE54	F	00003B18	4	2743	2724 2725 2726 2728
RE55	F	00003BE0	4	2781	2762 2763 2764 2766
RE56	F	00003CA8	4	2819	2800 2801 2802 2804
RE57	F	00003D70	4	2857	2838 2839 2840 2842
RE58	F	00003E38	4	2895	2876 2877 2878 2880
RE59	F	00003F00	4	2933	2914 2915 2916 2918
RE6	F	00001598	4	894	875 876 877 879
RE60	F	00003FC8	4	2971	2952 2953 2954 2956
RE61	F	00004090	4	3019	3000 3001 3002 3004
RE62	F	00004158	4	3057	3038 3039 3040 3042
RE63	F	00004220	4	3095	3076 3077 3078 3080
RE64	F	000042E8	4	3134	3115 3116 3117 3119
RE65	F	000043B0	4	3172	3153 3154 3155 3157
RE66	F	00004478	4	3210	3191 3192 3193 3195
RE67	F	00004540	4	3249	3230 3231 3232 3234
RE68	F	00004608	4	3287	3268 3269 3270 3272
RE69	F	000046D0	4	3325	3306 3307 3308 3310
RE7	F	00001660	4	933	914 915 916 918
RE70	F	00004798	4	3364	3345 3346 3347 3349
RE71	F	00004860	4	3402	3383 3384 3385 3387
RE72	F	00004928	4	3440	3421 3422 3423 3425
RE73	F	000049F0	4	3482	3463 3464 3465 3467
RE74	F	00004AB8	4	3520	3501 3502 3503 3505
RE75	F	00004B80	4	3558	3539 3540 3541 3543
RE76	F	00004C48	4	3596	3577 3578 3579 3581
RE77	F	00004D10	4	3634	3615 3616 3617 3619
RE78	F	00004DD8	4	3672	3653 3654 3655 3657
RE79	F	00004EA0	4	3711	3692 3693 3694 3696
RE8	F	00001728	4	971	952 953 954 956
RE80	F	00004F68	4	3749	3730 3731 3732 3734
RE81	F	00005030	4	3787	3768 3769 3770 3772
RE82	F	000050F8	4	3825	3806 3807 3808 3810
RE83	F	000051C0	4	3863	3844 3845 3846 3848
RE84	F	00005288	4	3901	3882 3883 3884 3886
RE85	F	00005350	4	3940	3921 3922 3923 3925
RE86	F	00005418	4	3978	3959 3960 3961 3963
RE87	F	000054E0	4	4016	3997 3998 3999 4001
RE88	F	000055A8	4	4054	4035 4036 4037 4039
RE89	F	00005670	4	4092	4073 4074 4075 4077
RE9	F	000017F0	4	1009	990 991 992 994
RE90	F	00005738	4	4130	4111 4112 4113 4115
RE91	F	00005800	4	4169	4150 4151 4152 4154
RE92	F	000058C8	4	4207	4188 4189 4190 4192
RE93	F	00005990	4	4245	4226 4227 4228 4230
RE94	F	00005A58	4	4283	4264 4265 4266 4268
RE95	F	00005B20	4	4321	4302 4303 4304 4306
RE96	F	00005BE8	4	4359	4340 4341 4342 4344
RE97	F	00005CB0	4	4407	4388 4389 4390 4392

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
RE98	F	00005D78	4	4445	4426	4427	4428	4430	
RE99	F	00005E40	4	4483	4464	4465	4466	4468	
REA1	A	00001148	4	688					
REA10	A	00001850	4	1036					
REA100	A	00005EA0	4	4507					
REA101	A	00005F68	4	4545					
REA102	A	00006030	4	4583					
REA103	A	000060F8	4	4622					
REA104	A	000061C0	4	4660					
REA105	A	00006288	4	4698					
REA106	A	00006350	4	4737					
REA107	A	00006418	4	4775					
REA108	A	000064E0	4	4813					
REA109	A	000065A8	4	4855					
REA11	A	00001918	4	1074					
REA110	A	00006670	4	4893					
REA111	A	00006738	4	4931					
REA112	A	00006800	4	4969					
REA113	A	000068C8	4	5007					
REA114	A	00006990	4	5045					
REA115	A	00006A58	4	5084					
REA116	A	00006B20	4	5122					
REA117	A	00006BE8	4	5160					
REA118	A	00006CB0	4	5198					
REA119	A	00006D78	4	5236					
REA12	A	000019E0	4	1112					
REA120	A	00006E40	4	5274					
REA121	A	00006F08	4	5313					
REA122	A	00006FD0	4	5351					
REA123	A	00007098	4	5389					
REA124	A	00007160	4	5427					
REA125	A	00007228	4	5465					
REA126	A	000072F0	4	5503					
REA127	A	000073B8	4	5542					
REA128	A	00007480	4	5580					
REA129	A	00007548	4	5618					
REA13	A	00001AA8	4	1150					
REA130	A	00007610	4	5656					
REA131	A	000076D8	4	5694					
REA132	A	000077A0	4	5732					
REA133	A	00007868	4	5780					
REA134	A	00007930	4	5818					
REA135	A	000079F8	4	5856					
REA136	A	00007AC0	4	5895					
REA137	A	00007B88	4	5933					
REA138	A	00007C50	4	5971					
REA139	A	00007D18	4	6010					
REA14	A	00001B70	4	1188					
REA140	A	00007DE0	4	6048					
REA141	A	00007EA8	4	6086					
REA142	A	00007F70	4	6125					
REA143	A	00008038	4	6163					
REA144	A	00008100	4	6201					
REA145	A	000081C8	4	6243					
REA146	A	00008290	4	6281					
REA147	A	00008358	4	6319					

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA148	A	00008420	4	6357	
REA149	A	000084E8	4	6395	
REA15	A	00001C38	4	1226	
REA150	A	000085B0	4	6433	
REA151	A	00008678	4	6471	
REA152	A	00008740	4	6509	
REA153	A	00008808	4	6548	
REA154	A	000088D0	4	6586	
REA155	A	00008998	4	6624	
REA156	A	00008A60	4	6662	
REA157	A	00008B28	4	6700	
REA158	A	00008BF0	4	6738	
REA159	A	00008CB8	4	6776	
REA16	A	00001D00	4	1265	
REA160	A	00008D80	4	6814	
REA161	A	00008E48	4	6853	
REA162	A	00008F10	4	6891	
REA163	A	00008FD8	4	6929	
REA164	A	000090A0	4	6967	
REA165	A	00009168	4	7005	
REA166	A	00009230	4	7043	
REA167	A	000092F8	4	7081	
REA168	A	000093C0	4	7119	
REA169	A	00009488	4	7158	
REA17	A	00001DC8	4	1303	
REA170	A	00009550	4	7196	
REA171	A	00009618	4	7234	
REA172	A	000096E0	4	7272	
REA173	A	000097A8	4	7310	
REA174	A	00009870	4	7348	
REA175	A	00009938	4	7386	
REA176	A	00009A00	4	7424	
REA18	A	00001E90	4	1341	
REA19	A	00001F58	4	1379	
REA2	A	00001210	4	726	
REA20	A	00002020	4	1417	
REA21	A	000020E8	4	1455	
REA22	A	000021B0	4	1494	
REA23	A	00002278	4	1532	
REA24	A	00002340	4	1570	
REA25	A	00002408	4	1608	
REA26	A	000024D0	4	1646	
REA27	A	00002598	4	1684	
REA28	A	00002660	4	1732	
REA29	A	00002728	4	1770	
REA3	A	000012D8	4	764	
REA30	A	000027F0	4	1808	
REA31	A	000028B8	4	1847	
REA32	A	00002980	4	1885	
REA33	A	00002A48	4	1923	
REA34	A	00002B10	4	1962	
REA35	A	00002BD8	4	2000	
REA36	A	00002CA0	4	2038	
REA37	A	00002D68	4	2080	
REA38	A	00002E30	4	2118	
REA39	A	00002EF8	4	2156	



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA4	A	000013A0	4	803	
REA40	A	00002FC0	4	2194	
REA41	A	00003088	4	2232	
REA42	A	00003150	4	2270	
REA43	A	00003218	4	2308	
REA44	A	000032E0	4	2346	
REA45	A	000033A8	4	2385	
REA46	A	00003470	4	2423	
REA47	A	00003538	4	2461	
REA48	A	00003600	4	2499	
REA49	A	000036C8	4	2537	
REA5	A	00001468	4	841	
REA50	A	00003790	4	2575	
REA51	A	00003858	4	2613	
REA52	A	00003920	4	2651	
REA53	A	000039E8	4	2690	
REA54	A	00003AB0	4	2728	
REA55	A	00003B78	4	2766	
REA56	A	00003C40	4	2804	
REA57	A	00003D08	4	2842	
REA58	A	00003DD0	4	2880	
REA59	A	00003E98	4	2918	
REA6	A	00001530	4	879	
REA60	A	00003F60	4	2956	
REA61	A	00004028	4	3004	
REA62	A	000040F0	4	3042	
REA63	A	000041B8	4	3080	
REA64	A	00004280	4	3119	
REA65	A	00004348	4	3157	
REA66	A	00004410	4	3195	
REA67	A	000044D8	4	3234	
REA68	A	000045A0	4	3272	
REA69	A	00004668	4	3310	
REA7	A	000015F8	4	918	
REA70	A	00004730	4	3349	
REA71	A	000047F8	4	3387	
REA72	A	000048C0	4	3425	
REA73	A	00004988	4	3467	
REA74	A	00004A50	4	3505	
REA75	A	00004B18	4	3543	
REA76	A	00004BE0	4	3581	
REA77	A	00004CA8	4	3619	
REA78	A	00004D70	4	3657	
REA79	A	00004E38	4	3696	
REA8	A	000016C0	4	956	
REA80	A	00004F00	4	3734	
REA81	A	00004FC8	4	3772	
REA82	A	00005090	4	3810	
REA83	A	00005158	4	3848	
REA84	A	00005220	4	3886	
REA85	A	000052E8	4	3925	
REA86	A	000053B0	4	3963	
REA87	A	00005478	4	4001	
REA88	A	00005540	4	4039	
REA89	A	00005608	4	4077	
REA9	A	00001788	4	994	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA90	A	000056D0	4	4115		
REA91	A	00005798	4	4154		
REA92	A	00005860	4	4192		
REA93	A	00005928	4	4230		
REA94	A	000059F0	4	4268		
REA95	A	00005AB8	4	4306		
REA96	A	00005B80	4	4344		
REA97	A	00005C48	4	4392		
REA98	A	00005D10	4	4430		
REA99	A	00005DD8	4	4468		
READDR	A	00000030	4	535	234	
REG2LOW	U	000000DD	1	445		
REG2PATT	U	AABBCCDD	1	444		
RELEN	A	0000002C	4	534		
RPTDWSAV	D	00000460	8	368	357	359
RPTERROR	I	00000436	4	352	287	325
RPTSAVE	F	00000454	4	365	352	362
RPTSVR5	F	00000458	4	366	353	361
SKL0001	U	0000004E	1	187	203	
SKT0001	C	0000022A	20	184	187	204
SVOLDPSW	U	00000140	0	123		
T1	A	00001118	4	674	7455	
T10	A	00001820	4	1022	7464	
T100	A	00005E70	4	4493	7554	
T101	A	00005F38	4	4531	7555	
T102	A	00006000	4	4569	7556	
T103	A	000060C8	4	4608	7557	
T104	A	00006190	4	4646	7558	
T105	A	00006258	4	4684	7559	
T106	A	00006320	4	4723	7560	
T107	A	000063E8	4	4761	7561	
T108	A	000064B0	4	4799	7562	
T109	A	00006578	4	4841	7563	
T11	A	000018E8	4	1060	7465	
T110	A	00006640	4	4879	7564	
T111	A	00006708	4	4917	7565	
T112	A	000067D0	4	4955	7566	
T113	A	00006898	4	4993	7567	
T114	A	00006960	4	5031	7568	
T115	A	00006A28	4	5070	7569	
T116	A	00006AF0	4	5108	7570	
T117	A	00006BB8	4	5146	7571	
T118	A	00006C80	4	5184	7572	
T119	A	00006D48	4	5222	7573	
T12	A	000019B0	4	1098	7466	
T120	A	00006E10	4	5260	7574	
T121	A	00006ED8	4	5299	7575	
T122	A	00006FA0	4	5337	7576	
T123	A	00007068	4	5375	7577	
T124	A	00007130	4	5413	7578	
T125	A	000071F8	4	5451	7579	
T126	A	000072C0	4	5489	7580	
T127	A	00007388	4	5528	7581	
T128	A	00007450	4	5566	7582	
T129	A	00007518	4	5604	7583	
T13	A	00001A78	4	1136	7467	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T130	A	000075E0	4	5642	7584
T131	A	000076A8	4	5680	7585
T132	A	00007770	4	5718	7586
T133	A	00007838	4	5766	7587
T134	A	00007900	4	5804	7588
T135	A	000079C8	4	5842	7589
T136	A	00007A90	4	5881	7590
T137	A	00007B58	4	5919	7591
T138	A	00007C20	4	5957	7592
T139	A	00007CE8	4	5996	7593
T14	A	00001B40	4	1174	7468
T140	A	00007DB0	4	6034	7594
T141	A	00007E78	4	6072	7595
T142	A	00007F40	4	6111	7596
T143	A	00008008	4	6149	7597
T144	A	000080D0	4	6187	7598
T145	A	00008198	4	6229	7599
T146	A	00008260	4	6267	7600
T147	A	00008328	4	6305	7601
T148	A	000083F0	4	6343	7602
T149	A	000084B8	4	6381	7603
T15	A	00001C08	4	1212	7469
T150	A	00008580	4	6419	7604
T151	A	00008648	4	6457	7605
T152	A	00008710	4	6495	7606
T153	A	000087D8	4	6534	7607
T154	A	000088A0	4	6572	7608
T155	A	00008968	4	6610	7609
T156	A	00008A30	4	6648	7610
T157	A	00008AF8	4	6686	7611
T158	A	00008BC0	4	6724	7612
T159	A	00008C88	4	6762	7613
T16	A	00001CD0	4	1251	7470
T160	A	00008D50	4	6800	7614
T161	A	00008E18	4	6839	7615
T162	A	00008EE0	4	6877	7616
T163	A	00008FA8	4	6915	7617
T164	A	00009070	4	6953	7618
T165	A	00009138	4	6991	7619
T166	A	00009200	4	7029	7620
T167	A	000092C8	4	7067	7621
T168	A	00009390	4	7105	7622
T169	A	00009458	4	7144	7623
T17	A	00001D98	4	1289	7471
T170	A	00009520	4	7182	7624
T171	A	000095E8	4	7220	7625
T172	A	000096B0	4	7258	7626
T173	A	00009778	4	7296	7627
T174	A	00009840	4	7334	7628
T175	A	00009908	4	7372	7629
T176	A	000099D0	4	7410	7630
T18	A	00001E60	4	1327	7472
T19	A	00001F28	4	1365	7473
T2	A	000011E0	4	712	7456
T20	A	00001FF0	4	1403	7474
T21	A	000020B8	4	1441	7475

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T22	A	00002180	4	1480	7476
T23	A	00002248	4	1518	7477
T24	A	00002310	4	1556	7478
T25	A	000023D8	4	1594	7479
T26	A	000024A0	4	1632	7480
T27	A	00002568	4	1670	7481
T28	A	00002630	4	1718	7482
T29	A	000026F8	4	1756	7483
T3	A	000012A8	4	750	7457
T30	A	000027C0	4	1794	7484
T31	A	00002888	4	1833	7485
T32	A	00002950	4	1871	7486
T33	A	00002A18	4	1909	7487
T34	A	00002AE0	4	1948	7488
T35	A	00002BA8	4	1986	7489
T36	A	00002C70	4	2024	7490
T37	A	00002D38	4	2066	7491
T38	A	00002E00	4	2104	7492
T39	A	00002EC8	4	2142	7493
T4	A	00001370	4	789	7458
T40	A	00002F90	4	2180	7494
T41	A	00003058	4	2218	7495
T42	A	00003120	4	2256	7496
T43	A	000031E8	4	2294	7497
T44	A	000032B0	4	2332	7498
T45	A	00003378	4	2371	7499
T46	A	00003440	4	2409	7500
T47	A	00003508	4	2447	7501
T48	A	000035D0	4	2485	7502
T49	A	00003698	4	2523	7503
T5	A	00001438	4	827	7459
T50	A	00003760	4	2561	7504
T51	A	00003828	4	2599	7505
T52	A	000038F0	4	2637	7506
T53	A	000039B8	4	2676	7507
T54	A	00003A80	4	2714	7508
T55	A	00003B48	4	2752	7509
T56	A	00003C10	4	2790	7510
T57	A	00003CD8	4	2828	7511
T58	A	00003DA0	4	2866	7512
T59	A	00003E68	4	2904	7513
T6	A	00001500	4	865	7460
T60	A	00003F30	4	2942	7514
T61	A	00003FF8	4	2990	7515
T62	A	000040C0	4	3028	7516
T63	A	00004188	4	3066	7517
T64	A	00004250	4	3105	7518
T65	A	00004318	4	3143	7519
T66	A	000043E0	4	3181	7520
T67	A	000044A8	4	3220	7521
T68	A	00004570	4	3258	7522
T69	A	00004638	4	3296	7523
T7	A	000015C8	4	904	7461
T70	A	00004700	4	3335	7524
T71	A	000047C8	4	3373	7525
T72	A	00004890	4	3411	7526



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
T73	A	00004958	4	3453	7527		
T74	A	00004A20	4	3491	7528		
T75	A	00004AE8	4	3529	7529		
T76	A	00004BB0	4	3567	7530		
T77	A	00004C78	4	3605	7531		
T78	A	00004D40	4	3643	7532		
T79	A	00004E08	4	3682	7533		
T8	A	00001690	4	942	7462		
T80	A	00004ED0	4	3720	7534		
T81	A	00004F98	4	3758	7535		
T82	A	00005060	4	3796	7536		
T83	A	00005128	4	3834	7537		
T84	A	000051F0	4	3872	7538		
T85	A	000052B8	4	3911	7539		
T86	A	00005380	4	3949	7540		
T87	A	00005448	4	3987	7541		
T88	A	00005510	4	4025	7542		
T89	A	000055D8	4	4063	7543		
T9	A	00001758	4	980	7463		
T90	A	000056A0	4	4101	7544		
T91	A	00005768	4	4140	7545		
T92	A	00005830	4	4178	7546		
T93	A	000058F8	4	4216	7547		
T94	A	000059C0	4	4254	7548		
T95	A	00005A88	4	4292	7549		
T96	A	00005B50	4	4330	7550		
T97	A	00005C18	4	4378	7551		
T98	A	00005CE0	4	4416	7552		
T99	A	00005DA8	4	4454	7553		
TESTCC	I	00000318	4	241	231		
TESTING	F	00001004	4	456	223		
TESTREST	U	00000300	1	233	252	292	
TNUM	H	00000004	2	518	222	263	301
TSUB	A	00000000	4	517	226		
TTABLE	F	00009AA0	4	7454			
V0	U	00000000	1	7663			
V1	U	00000001	1	7664			
V10	U	0000000A	1	7673			
V11	U	0000000B	1	7674			
V12	U	0000000C	1	7675			
V13	U	0000000D	1	7676			
V14	U	0000000E	1	7677			
V15	U	0000000F	1	7678			
V16	U	00000010	1	7679			
V17	U	00000011	1	7680			
V18	U	00000012	1	7681			
V19	U	00000013	1	7682			
V1ADDR	A	00000020	4	531			
V1FUDGE	X	000010F8	16	509	225		
V101	X	00001160	16	690	701		
V1010	X	00001868	16	1038	1049		
V10100	X	00005EB8	16	4509	4520		
V10101	X	00005F80	16	4547	4558		
V10102	X	00006048	16	4585	4596		
V10103	X	00006110	16	4624	4635		
V10104	X	000061D8	16	4662	4673		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V10105	X	000062A0	16	4700	4711
V10106	X	00006368	16	4739	4750
V10107	X	00006430	16	4777	4788
V10108	X	000064F8	16	4815	4826
V10109	X	000065C0	16	4857	4868
V1011	X	00001930	16	1076	1087
V10110	X	00006688	16	4895	4906
V10111	X	00006750	16	4933	4944
V10112	X	00006818	16	4971	4982
V10113	X	000068E0	16	5009	5020
V10114	X	000069A8	16	5047	5058
V10115	X	00006A70	16	5086	5097
V10116	X	00006B38	16	5124	5135
V10117	X	00006C00	16	5162	5173
V10118	X	00006CC8	16	5200	5211
V10119	X	00006D90	16	5238	5249
V1012	X	000019F8	16	1114	1125
V10120	X	00006E58	16	5276	5287
V10121	X	00006F20	16	5315	5326
V10122	X	00006FE8	16	5353	5364
V10123	X	000070B0	16	5391	5402
V10124	X	00007178	16	5429	5440
V10125	X	00007240	16	5467	5478
V10126	X	00007308	16	5505	5516
V10127	X	000073D0	16	5544	5555
V10128	X	00007498	16	5582	5593
V10129	X	00007560	16	5620	5631
V1013	X	00001AC0	16	1152	1163
V10130	X	00007628	16	5658	5669
V10131	X	000076F0	16	5696	5707
V10132	X	000077B8	16	5734	5745
V10133	X	00007880	16	5782	5793
V10134	X	00007948	16	5820	5831
V10135	X	00007A10	16	5858	5869
V10136	X	00007AD8	16	5897	5908
V10137	X	00007BA0	16	5935	5946
V10138	X	00007C68	16	5973	5984
V10139	X	00007D30	16	6012	6023
V1014	X	00001B88	16	1190	1201
V10140	X	00007DF8	16	6050	6061
V10141	X	00007EC0	16	6088	6099
V10142	X	00007F88	16	6127	6138
V10143	X	00008050	16	6165	6176
V10144	X	00008118	16	6203	6214
V10145	X	000081E0	16	6245	6256
V10146	X	000082A8	16	6283	6294
V10147	X	00008370	16	6321	6332
V10148	X	00008438	16	6359	6370
V10149	X	00008500	16	6397	6408
V1015	X	00001C50	16	1228	1239
V10150	X	000085C8	16	6435	6446
V10151	X	00008690	16	6473	6484
V10152	X	00008758	16	6511	6522
V10153	X	00008820	16	6550	6561
V10154	X	000088E8	16	6588	6599
V10155	X	000089B0	16	6626	6637

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V10156	X	00008A78	16	6664	6675
V10157	X	00008B40	16	6702	6713
V10158	X	00008C08	16	6740	6751
V10159	X	00008CD0	16	6778	6789
V1016	X	00001D18	16	1267	1278
V10160	X	00008D98	16	6816	6827
V10161	X	00008E60	16	6855	6866
V10162	X	00008F28	16	6893	6904
V10163	X	00008FF0	16	6931	6942
V10164	X	000090B8	16	6969	6980
V10165	X	00009180	16	7007	7018
V10166	X	00009248	16	7045	7056
V10167	X	00009310	16	7083	7094
V10168	X	000093D8	16	7121	7132
V10169	X	000094A0	16	7160	7171
V1017	X	00001DE0	16	1305	1316
V10170	X	00009568	16	7198	7209
V10171	X	00009630	16	7236	7247
V10172	X	000096F8	16	7274	7285
V10173	X	000097C0	16	7312	7323
V10174	X	00009888	16	7350	7361
V10175	X	00009950	16	7388	7399
V10176	X	00009A18	16	7426	7437
V1018	X	00001EA8	16	1343	1354
V1019	X	00001F70	16	1381	1392
V102	X	00001228	16	728	739
V1020	X	00002038	16	1419	1430
V1021	X	00002100	16	1457	1468
V1022	X	000021C8	16	1496	1507
V1023	X	00002290	16	1534	1545
V1024	X	00002358	16	1572	1583
V1025	X	00002420	16	1610	1621
V1026	X	000024E8	16	1648	1659
V1027	X	000025B0	16	1686	1697
V1028	X	00002678	16	1734	1745
V1029	X	00002740	16	1772	1783
V103	X	000012F0	16	766	777
V1030	X	00002808	16	1810	1821
V1031	X	000028D0	16	1849	1860
V1032	X	00002998	16	1887	1898
V1033	X	00002A60	16	1925	1936
V1034	X	00002B28	16	1964	1975
V1035	X	00002BF0	16	2002	2013
V1036	X	00002CB8	16	2040	2051
V1037	X	00002D80	16	2082	2093
V1038	X	00002E48	16	2120	2131
V1039	X	00002F10	16	2158	2169
V104	X	000013B8	16	805	816
V1040	X	00002FD8	16	2196	2207
V1041	X	000030A0	16	2234	2245
V1042	X	00003168	16	2272	2283
V1043	X	00003230	16	2310	2321
V1044	X	000032F8	16	2348	2359
V1045	X	000033C0	16	2387	2398
V1046	X	00003488	16	2425	2436
V1047	X	00003550	16	2463	2474

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1048	X	00003618	16	2501	2512
V1049	X	000036E0	16	2539	2550
V105	X	00001480	16	843	854
V1050	X	000037A8	16	2577	2588
V1051	X	00003870	16	2615	2626
V1052	X	00003938	16	2653	2664
V1053	X	00003A00	16	2692	2703
V1054	X	00003AC8	16	2730	2741
V1055	X	00003B90	16	2768	2779
V1056	X	00003C58	16	2806	2817
V1057	X	00003D20	16	2844	2855
V1058	X	00003DE8	16	2882	2893
V1059	X	00003EB0	16	2920	2931
V106	X	00001548	16	881	892
V1060	X	00003F78	16	2958	2969
V1061	X	00004040	16	3006	3017
V1062	X	00004108	16	3044	3055
V1063	X	000041D0	16	3082	3093
V1064	X	00004298	16	3121	3132
V1065	X	00004360	16	3159	3170
V1066	X	00004428	16	3197	3208
V1067	X	000044F0	16	3236	3247
V1068	X	000045B8	16	3274	3285
V1069	X	00004680	16	3312	3323
V107	X	00001610	16	920	931
V1070	X	00004748	16	3351	3362
V1071	X	00004810	16	3389	3400
V1072	X	000048D8	16	3427	3438
V1073	X	000049A0	16	3469	3480
V1074	X	00004A68	16	3507	3518
V1075	X	00004B30	16	3545	3556
V1076	X	00004BF8	16	3583	3594
V1077	X	00004CC0	16	3621	3632
V1078	X	00004D88	16	3659	3670
V1079	X	00004E50	16	3698	3709
V108	X	000016D8	16	958	969
V1080	X	00004F18	16	3736	3747
V1081	X	00004FE0	16	3774	3785
V1082	X	000050A8	16	3812	3823
V1083	X	00005170	16	3850	3861
V1084	X	00005238	16	3888	3899
V1085	X	00005300	16	3927	3938
V1086	X	000053C8	16	3965	3976
V1087	X	00005490	16	4003	4014
V1088	X	00005558	16	4041	4052
V1089	X	00005620	16	4079	4090
V109	X	000017A0	16	996	1007
V1090	X	000056E8	16	4117	4128
V1091	X	000057B0	16	4156	4167
V1092	X	00005878	16	4194	4205
V1093	X	00005940	16	4232	4243
V1094	X	00005A08	16	4270	4281
V1095	X	00005AD0	16	4308	4319
V1096	X	00005B98	16	4346	4357
V1097	X	00005C60	16	4394	4405
V1098	X	00005D28	16	4432	4443



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V1099	X	00005DF0	16	4470	4481												
V10OUTPUT	X	00000048	16	537	235												
V2	U	00000002	1	7665													
V20	U	00000014	1	7683													
V21	U	00000015	1	7684	698	701	736	739	774	777	813	816	851	854	889	892	928
					931	966	969	1004	1007	1046	1049	1084	1087	1122	1125	1160	1163
					1198	1201	1236	1239	1275	1278	1313	1316	1351	1354	1389	1392	1427
					1430	1465	1468	1504	1507	1542	1545	1580	1583	1618	1621	1656	1659
					1694	1697	1742	1745	1780	1783	1818	1821	1857	1860	1895	1898	1933
					1936	1972	1975	2010	2013	2048	2051	2090	2093	2128	2131	2166	2169
					2204	2207	2242	2245	2280	2283	2318	2321	2356	2359	2395	2398	2433
					2436	2471	2474	2509	2512	2547	2550	2585	2588	2623	2626	2661	2664
					2700	2703	2738	2741	2776	2779	2814	2817	2852	2855	2890	2893	2928
					2931	2966	2969	3014	3017	3052	3055	3090	3093	3129	3132	3167	3170
					3205	3208	3244	3247	3282	3285	3320	3323	3359	3362	3397	3400	3435
					3438	3477	3480	3515	3518	3553	3556	3591	3594	3629	3632	3667	3670
					3706	3709	3744	3747	3782	3785	3820	3823	3858	3861	3896	3899	3935
					3938	3973	3976	4011	4014	4049	4052	4087	4090	4125	4128	4164	4167
					4202	4205	4240	4243	4278	4281	4316	4319	4354	4357	4402	4405	4440
					4443	4478	4481	4517	4520	4555	4558	4593	4596	4632	4635	4670	4673
					4708	4711	4747	4750	4785	4788	4823	4826	4865	4868	4903	4906	4941
					4944	4979	4982	5017	5020	5055	5058	5094	5097	5132	5135	5170	5173
					5208	5211	5246	5249	5284	5287	5323	5326	5361	5364	5399	5402	5437
					5440	5475	5478	5513	5516	5552	5555	5590	5593	5628	5631	5666	5669
					5704	5707	5742	5745	5790	5793	5828	5831	5866	5869	5905	5908	5943
					5946	5981	5984	6020	6023	6058	6061	6096	6099	6135	6138	6173	6176
					6211	6214	6253	6256	6291	6294	6329	6332	6367	6370	6405	6408	6443
					6446	6481	6484	6519	6522	6558	6561	6596	6599	6634	6637	6672	6675
					6710	6713	6748	6751	6786	6789	6824	6827	6863	6866	6901	6904	6939
					6942	6977	6980	7015	7018	7053	7056	7091	7094	7129	7132	7168	7171
					7206	7209	7244	7247	7282	7285	7320	7323	7358	7361	7396	7399	7434
					7437												
V22	U	00000016	1	7685	225	695	698	733	736	771	774	810	813	848	851	886	889
					925	928	963	966	1001	1004	1043	1046	1081	1084	1119	1122	1157
					1160	1195	1198	1233	1236	1272	1275	1310	1313	1348	1351	1386	1389
					1424	1427	1462	1465	1501	1504	1539	1542	1577	1580	1615	1618	1653
					1656	1691	1694	1739	1742	1777	1780	1815	1818	1854	1857	1892	1895
					1930	1933	1969	1972	2007	2010	2045	2048	2087	2090	2125	2128	2163
					2166	2201	2204	2239	2242	2277	2280	2315	2318	2353	2356	2392	2395
					2430	2433	2468	2471	2506	2509	2544	2547	2582	2585	2620	2623	2658
					2661	2697	2700	2735	2738	2773	2776	2811	2814	2849	2852	2887	2890
					2925	2928	2963	2966	3011	3014	3049	3052	3087	3090	3126	3129	3164
					3167	3202	3205	3241	3244	3279	3282	3317	3320	3356	3359	3394	3397
					3432	3435	3474	3477	3512	3515	3550	3553	3588	3591	3626	3629	3664
					3667	3703	3706	3741	3744	3779	3782	3817	3820	3855	3858	3893	3896
					3932	3935	3970	3973	4008	4011	4046	4049	4084	4087	4122	4125	4161
					4164	4199	4202	4237	4240	4275	4278	4313	4316	4351	4354	4399	4402
					4437	4440	4475	4478	4514	4517	4552	4555	4590	4593	4629	4632	4667
					4670	4705	4708	4744	4747	4782	4785	4820	4823	4862	4865	4900	4903
					4938	4941	4976	4979	5014	5017	5052	5055	5091	5094	5129	5132	5167
					5170	5205	5208	5243	5246	5281	5284	5320	5323	5358	5361	5396	5399
					5434	5437	5472	5475	5510	5513	5549	5552	5587	5590	5625	5628	5663
					5666	5701	5704	5739	5742	5787	5790	5825	5828	5863	5866	5902	5905
					5940	5943	5978	5981	6017	6020	6055	6058	6093	6096	6132	6135	6170
					6173	6208	6211	6250	6253	6288	6291	6326	6329	6364	6367	6402	6405
					6440	6443	6478	6481	6516	6519	6555	6558	6593	6596	6631	6634	6669





SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X131	F	00007710	4	5699	5680
X132	F	000077D8	4	5737	5718
X133	F	000078A0	4	5785	5766
X134	F	00007968	4	5823	5804
X135	F	00007A30	4	5861	5842
X136	F	00007AF8	4	5900	5881
X137	F	00007BC0	4	5938	5919
X138	F	00007C88	4	5976	5957
X139	F	00007D50	4	6015	5996
X14	F	00001BA8	4	1193	1174
X140	F	00007E18	4	6053	6034
X141	F	00007EE0	4	6091	6072
X142	F	00007FA8	4	6130	6111
X143	F	00008070	4	6168	6149
X144	F	00008138	4	6206	6187
X145	F	00008200	4	6248	6229
X146	F	000082C8	4	6286	6267
X147	F	00008390	4	6324	6305
X148	F	00008458	4	6362	6343
X149	F	00008520	4	6400	6381
X15	F	00001C70	4	1231	1212
X150	F	000085E8	4	6438	6419
X151	F	000086B0	4	6476	6457
X152	F	00008778	4	6514	6495
X153	F	00008840	4	6553	6534
X154	F	00008908	4	6591	6572
X155	F	000089D0	4	6629	6610
X156	F	00008A98	4	6667	6648
X157	F	00008B60	4	6705	6686
X158	F	00008C28	4	6743	6724
X159	F	00008CF0	4	6781	6762
X16	F	00001D38	4	1270	1251
X160	F	00008DB8	4	6819	6800
X161	F	00008E80	4	6858	6839
X162	F	00008F48	4	6896	6877
X163	F	00009010	4	6934	6915
X164	F	000090D8	4	6972	6953
X165	F	000091A0	4	7010	6991
X166	F	00009268	4	7048	7029
X167	F	00009330	4	7086	7067
X168	F	000093F8	4	7124	7105
X169	F	000094C0	4	7163	7144
X17	F	00001E00	4	1308	1289
X170	F	00009588	4	7201	7182
X171	F	00009650	4	7239	7220
X172	F	00009718	4	7277	7258
X173	F	000097E0	4	7315	7296
X174	F	000098A8	4	7353	7334
X175	F	00009970	4	7391	7372
X176	F	00009A38	4	7429	7410
X18	F	00001EC8	4	1346	1327
X19	F	00001F90	4	1384	1365
X2	F	00001248	4	731	712
X20	F	00002058	4	1422	1403
X21	F	00002120	4	1460	1441
X22	F	000021E8	4	1499	1480



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X23	F	000022B0	4	1537	1518
X24	F	00002378	4	1575	1556
X25	F	00002440	4	1613	1594
X26	F	00002508	4	1651	1632
X27	F	000025D0	4	1689	1670
X28	F	00002698	4	1737	1718
X29	F	00002760	4	1775	1756
X3	F	00001310	4	769	750
X30	F	00002828	4	1813	1794
X31	F	000028F0	4	1852	1833
X32	F	000029B8	4	1890	1871
X33	F	00002A80	4	1928	1909
X34	F	00002B48	4	1967	1948
X35	F	00002C10	4	2005	1986
X36	F	00002CD8	4	2043	2024
X37	F	00002DA0	4	2085	2066
X38	F	00002E68	4	2123	2104
X39	F	00002F30	4	2161	2142
X4	F	000013D8	4	808	789
X40	F	00002FF8	4	2199	2180
X41	F	000030C0	4	2237	2218
X42	F	00003188	4	2275	2256
X43	F	00003250	4	2313	2294
X44	F	00003318	4	2351	2332
X45	F	000033E0	4	2390	2371
X46	F	000034A8	4	2428	2409
X47	F	00003570	4	2466	2447
X48	F	00003638	4	2504	2485
X49	F	00003700	4	2542	2523
X5	F	000014A0	4	846	827
X50	F	000037C8	4	2580	2561
X51	F	00003890	4	2618	2599
X52	F	00003958	4	2656	2637
X53	F	00003A20	4	2695	2676
X54	F	00003AE8	4	2733	2714
X55	F	00003BB0	4	2771	2752
X56	F	00003C78	4	2809	2790
X57	F	00003D40	4	2847	2828
X58	F	00003E08	4	2885	2866
X59	F	00003ED0	4	2923	2904
X6	F	00001568	4	884	865
X60	F	00003F98	4	2961	2942
X61	F	00004060	4	3009	2990
X62	F	00004128	4	3047	3028
X63	F	000041F0	4	3085	3066
X64	F	000042B8	4	3124	3105
X65	F	00004380	4	3162	3143
X66	F	00004448	4	3200	3181
X67	F	00004510	4	3239	3220
X68	F	000045D8	4	3277	3258
X69	F	000046A0	4	3315	3296
X7	F	00001630	4	923	904
X70	F	00004768	4	3354	3335
X71	F	00004830	4	3392	3373
X72	F	000048F8	4	3430	3411
X73	F	000049C0	4	3472	3453





DESC	SYMBOL	SIZE	POS	ADDR
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**Entry: 0**

Image	IMAGE	40304	0000- 9D6F	0000- 9D6F
Regi on		40304	0000- 9D6F	0000- 9D6F
CSECT	ZVE7TST	40304	0000- 9D6F	0000- 9D6F



STMT	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e7-16-PackCompare.asm
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**\*\* NO ERRORS FOUND \*\***