```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    2 ************************************************************************
                                                    3 *
                                                    4 *   Zvector E7 instruction tests for VRR-d encoded:
                                                    5 *
                                                    6 *   E78B VSTRS  - Vector String Search
                                                    7 *
                                                    8 *        James Wekel March 2025
                                                    9 ************************************************************************


                                                   11 ************************************************************************
                                                   12 *
                                                   13 *        basic instruction tests
                                                   14 *
                                                   15 ************************************************************************
                                                   16 *  This program tests proper functioning of the z/arch E7 VRR-d
                                                   17 *  Vector String Search instruction.
                                                   18 *  Exceptions are not tested.
                                                   19 *
                                                   20 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                   21 *  obvious coding errors.  None of the tests are thorough.  They are
                                                   22 *  NOT designed to test all aspects of any of the instructions.
                                                   23 *
                                                   24 ************************************************************************
                                                   25 *
                                                   26 *   *Testcase zvector-e7-25-VSTRS
                                                   27 *   *
                                                   28 *   *   Zvector E7 instruction tests for VRR-d encoded:
                                                   29 *   *
                                                   30 *   *   E78B VSTRS  - Vector String Search
                                                   31 *   *
                                                   32 *   *   # ---------------------------------------------------------
                                                   33 *   *   #  This tests only the basic function of the instruction.
                                                   34 *   *   #  Exceptions are NOT tested.
                                                   35 *   *   # ---------------------------------------------------------
                                                   36 *   *
                                                   37 *   mainsize    2
                                                   38 *   numcpu      1
                                                   39 *   sysclear
                                                   40 *   archlvl     z/Arch
                                                   41 *
                                                   42 *   loadcore    "$(testpath)/zvector-e7-25-VSTRS.core" 0x0
                                                   43 *
                                                   44 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                   45 *   runtest     5         #
                                                   46 *   diag8cmd    disable   # (reset back to default)
                                                   47 *
                                                   48 *   *Done
                                                   49 *
                                                   50 ************************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    52 ************************************************************************
                                                    53 *        FCHECK Macro - Is a Facility Bit set?
                                                    54 *
                                                    55 *        If the facility bit is NOT set, an message is issued and
                                                    56 *        the test is skipped.
                                                    57 *
                                                    58 *        Fcheck uses R0, R1 and R2
                                                    59 *
                                                    60 * eg.    FCHECK 134,'vector-packed-decimal'
                                                    61 ************************************************************************
                                                    62          MACRO
                                                    63          FCHECK &BITNO,&NOTSETMSG
                                                    64 .*                      &BITNO : facility bit number to check
                                                    65 .*                      &NOTSETMSG : 'facility name'
                                                    66          LCLA  &FBBYTE           Facility bit in Byte
                                                    67          LCLA  &FBBIT            Facility bit within Byte
                                                    68
                                                    69          LCLA  &L(8)
                                                    70 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                    71
                                                    72 &FBBYTE  SETA  &BITNO/8
                                                    73 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                    74 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                    75
                                                    76          B     X&SYSNDX
                                                    77 *                                       Fcheck data area
                                                    78 *                                       skip messgae
                                                    79 SKT&SYSNDX DC  C'    Skipping tests: '
                                                    80          DC    C&NOTSETMSG
                                                    81          DC    C' (bit &BITNO) is not installed.'
                                                    82 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                    83 *                                       facility bits
                                                    84          DS    FD                       gap
                                                    85 FB&SYSNDX DS   4FD
                                                    86          DS    FD                       gap
                                                    87 *
                                                    88 X&SYSNDX EQU *
                                                    89          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                    90          STFLE FB&SYSNDX                get facility bits
                                                    91
                                                    92          XGR   R0,R0
                                                    93          IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                    94          N     R0,=F'&FBBIT'            is bit set?
                                                    95          BNZ   XC&SYSNDX
                                                    96 *
                                                    97 * facility bit not set, issue message and exit
                                                    98 *
                                                    99          LA    R0,SKL&SYSNDX            message length
                                                   100          LA    R1,SKT&SYSNDX            message address
                                                   101          BAL   R2,MSG
                                                   102
                                                   103          B     EOJ
                                                   104 XC&SYSNDX EQU *
                                                   105          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     107 ************************************************************************
                                                     108 *        Low core PSWs
                                                     109 ************************************************************************
                               00000000  00005A3F    110 ZVE7TST  START 0
00000000                       00000000              111          USING ZVE7TST,R0            Low core addressability
                                                     112
                               00000140  00000000    113 SVOLDPSW EQU   ZVE7TST+X'140'        z/Arch Supervisor call old PSW

00000000                       00000000  000001A0    115          ORG   ZVE7TST+X'1A0'       z/Architecure RESTART PSW
000001A0  00000001 80000000                          116          DC    X'0000000180000000'
000001A8  00000000 00000200                          117          DC    AD(BEGIN)

000001B0                       000001B0  000001D0    119          ORG   ZVE7TST+X'1D0'       z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                          120          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                          121          DC    AD(X'DEAD')

000001E0                       000001E0  00000200    123          ORG   ZVE7TST+X'200'       Start of actual test program...

                                                     125 ************************************************************************
                                                     126 *                The actual "ZVE7TST" program itself...
                                                     127 ************************************************************************
                                                     128 *
                                                     129 *  Architecture Mode: z/Arch
                                                     130 *  Register Usage:
                                                     131 *
                                                     132 *    R0       (work)
                                                     133 *    R1-4     (work)
                                                     134 *    R5       Testing control table - current test base
                                                     135 *    R6-R7    (work)
                                                     136 *    R8       First base register
                                                     137 *    R9       Second base register
                                                     138 *    R10      Third base register
                                                     139 *    R11      E7TEST call return
                                                     140 *    R12      E7TESTS register
                                                     141 *    R13      (work)
                                                     142 *    R14      Subroutine call
                                                     143 *    R15      Secondary Subroutine call or work
                                                     144 *
                                                     145 ************************************************************************

00000200                       00000200              147          USING  BEGIN,R8         FIRST Base Register
00000200                       00001200              148          USING  BEGIN+4096,R9    SECOND Base Register
00000200                       00002200              149          USING  BEGIN+8192,R10   THIRD Base Register

00000200  0580                                       151 BEGIN    BALR  R8,0              Initalize FIRST base register
00000202  0680                                       152          BCTR  R8,0              Initalize FIRST base register
00000204  0680                                       153          BCTR  R8,0              Initalize FIRST base register

00000206  4190 8800                    00000800      155          LA    R9,2048(,R8)      Initalize SECOND base register
0000020A  4190 9800                    00000800      156          LA    R9,2048(,R9)      Initalize SECOND base register
                                                     157
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
0000020E  41A0 9800                     00000800   158          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                     00000800   159          LA    R10,2048(,R10)   Initalize THIRD base register
                                                   160
00000216  B600 8344                     00000544   161          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 8345                     00000545   162          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 8345                     00000545   163          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 8344                     00000544   164          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                   165
                                                   166 ********************************************************************
                                                   167 * Is z/Architecture vector facility installed  (bit 129)
                                                   168 ********************************************************************
                                                   169
                                                   170          FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                     000002A8   171+         B     X0001
                                                   172+*                                  Fcheck data area
                                                   173+*                                  skip messgae
0000022A  40404040 E2928997                        174+SKT0001  DC    C'    Skipping tests: '
0000023E  A961C199 838889A3                        175+         DC    C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                        176+         DC    C' (bit 129) is not installed.'
                            0000004E  00000001     177+SKL0001  EQU   *-SKT0001
                                                   178+*                                  facility bits
00000278  00000000 00000000                        179+         DS    FD               gap
00000280  00000000 00000000                        180+FB0001   DS    4FD
000002A0  00000000 00000000                        181+         DS    FD               gap
                                                   182+*
                            000002A8  00000001     183+X0001    EQU   *
000002A8  4100 0004                     00000004   184+         LA    R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                     00000280   185+         STFLE FB0001           get facility bits
000002B0  B982 0000                                186+         XGR   R0,R0
000002B4  4300 8090                     00000290   187+         IC    R0,FB0001+16     get fbit byte
000002B8  5400 834C                     0000054C   188+         N     R0,=F'64'        is bit set?
000002BC  4770 80D0                     000002D0   189+         BNZ   XC0001
                                                   190+*
                                                   191+* facility bit not set, issue message and exit
                                                   192+*
000002C0  4100 004E                     0000004E   193+         LA    R0,SKL0001       message length
000002C4  4110 802A                     0000022A   194+         LA    R1,SKT0001       message address
000002C8  4520 8260                     00000460   195+         BAL   R2,MSG
000002CC  47F0 8328                     00000528   196+         B     EOJ
                            000002D0  00000001     197+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    199 ***************************************************************************
                                                    200 *               Do tests in the E7TESTS table
                                                    201 ***************************************************************************
                                                    202
000002D0  58C0 8350                       00000550  203           L     R12,=A(E7TESTS)       get table of test addresses
                                                    204
                                 000002D4  00000001  205 NEXTE7    EQU   *
000002D4  5850 C000                       00000000  206           L     R5,0(0,R12)       get test address
000002D8  1255                                      207           LTR   R5,R5                have a test?
000002DA  4780 8218                       00000418  208           BZ    ENDTEST                 done?
                                                    209
000002DE                          00000000          210           USING E7TEST,R5
                                                    211
000002DE  4800 5004                       00000004  212           LH    R0,TNUM           save current test number
000002E2  5000 8E04                       00001004  213           ST    R0,TESTING        for easy reference
                                                    214
000002E6  E710 8EF4 0006                  000010F4  215           VL    V1,V1FUDGE
000002EC  58B0 5000                       00000000  216           L     R11,TSUB          get address of test routine
000002F0  05BB                                      217           BALR  R11,R11           do test
                                                    218
000002F2  E310 500A 0076                  0000000A  219           LB    R1,CCMASK               (failure CC mask)
000002F8  8910 0004                       00000004  220           SLL   R1,4                    (shift to BC instr CC position)
000002FC  4410 8118                       00000318  221           EX    R1,TESTCC               fail if...
                                                    222
                                 00000300  00000001  223 TESTREST EQU   *
00000300  E310 5030 0014                  00000030  224           LGF   R1,READDR         get address of expected result
00000306  D50F 5040 1000       00000040  00000000  225           CLC   V1OUTPUT,0(R1)    valid?
0000030C  4770 81A0                       000003A0  226           BNE   FAILMSG              no, issue failed message
                                                    227
00000310  41C0 C004                       00000004  228           LA    R12,4(0,R12)      next test address
00000314  47F0 80D4                       000002D4  229           B     NEXTE7
                                                    230
00000318  4700 811C                       0000031C  231 TESTCC    BC    0,CCMSG                 (unexpected condition code?)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    233 ********************************************************************************
                                                    234 * cc was not as expected
                                                    235 ********************************************************************************
                               0000031C  00000001   236 CCMSG    EQU   *
                                                    237 *
                                                    238 * extract CC from extracted PSW
                                                    239 *
0000031C  5810 500C                      0000000C   240          L     R1,CCPSW
00000320  8810 000C                      0000000C   241          SRL   R1,12
00000324  5410 8354                      00000554   242          N     R1,=XL4'3'
00000328  4210 5014                      00000014   243          STC   R1,CCFOUND              save cc
                                                    244 *
                                                    245 * FILL IN MESSAGE
                                                    246 *
0000032C  4820 5004                      00000004   247          LH    R2,TNUM                 get test number and convert
00000330  4E20 8ED4                      000010D4   248          CVD   R2,DECNUM
00000334  D211 8EBE 8EA8       000010BE  000010A8   249          MVC   PRT3,EDIT
0000033A  DE11 8EBE 8ED4       000010BE  000010D4   250          ED    PRT3,DECNUM
00000340  D202 8E63 8ECB       00001063  000010CB   251          MVC   CCPRTNUM(3),PRT3+13     fill in message with test #
                                                    252
00000346  D207 8E80 5015       00001080  00000015   253          MVC   CCPRTNAME,OPNAME        fill in message with instruction
                                                    254
0000034C  B982 0022                                 255          XGR   R2,R2                   get CC as U8
00000350  4320 5009                      00000009   256          IC    R2,CC
00000354  4E20 8ED4                      000010D4   257          CVD   R2,DECNUM               and convert
00000358  D211 8EBE 8EA8       000010BE  000010A8   258          MVC   PRT3,EDIT
0000035E  DE11 8EBE 8ED4       000010BE  000010D4   259          ED    PRT3,DECNUM
00000364  D200 8E96 8ECD       00001096  000010CD   260          MVC   CCPRTEXP(1),PRT3+15     fill in message with CC field
                                                    261
0000036A  B982 0022                                 262          XGR   R2,R2                   get CCFOUND as U8
0000036E  4320 5014                      00000014   263          IC    R2,CCFOUND
00000372  4E20 8ED4                      000010D4   264          CVD   R2,DECNUM               and convert
00000376  D211 8EBE 8EA8       000010BE  000010A8   265          MVC   PRT3,EDIT
0000037C  DE11 8EBE 8ED4       000010BE  000010D4   266          ED    PRT3,DECNUM
00000382  D200 8EA6 8ECD       000010A6  000010CD   267          MVC   CCPRTGOT(1),PRT3+15     fill in message with ccfound
                                                    268
00000388  4100 0055                      00000055   269          LA    R0,CCPRTLNG             message length
0000038C  4110 8E53                      00001053   270          LA    R1,CCPRTLINE            messagfe address
00000390  45F0 8226                      00000426   271          BAL   R15,RPTERROR
                                                    272
00000394  5800 8358                      00000558   273          L     R0,=F'1'                set failed test indicator
00000398  5000 8E00                      00001000   274          ST    R0,FAILED
                                                    275
0000039C  47F0 8100                      00000300   276          B     TESTREST
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    278 ************************************************************************
                                                    279 * result not as expected:
                                                    280 *        issue message with test number, instruction under test
                                                    281 *              and instruction m5, m6
                                                    282 ************************************************************************
                                 000003A0  00000001  283 FAILMSG  EQU   *
000003A0  4820 5004                        00000004  284          LH    R2,TNUM              get test number and convert
000003A4  4E20 8ED4                        000010D4  285          CVD   R2,DECNUM
000003A8  D211 8EBE 8EA8       000010BE    000010A8  286          MVC   PRT3,EDIT
000003AE  DE11 8EBE 8ED4       000010BE    000010D4  287          ED    PRT3,DECNUM
000003B4  D202 8E18 8ECB       00001018    000010CB  288          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    289
000003BA  D207 8E33 5015       00001033    00000015  290          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    291
000003C0  B982 0022                                 292          XGR   R2,R2                get M5 as U8
000003C4  4320 5007                        00000007  293          IC    R2,M5
000003C8  4E20 8ED4                        000010D4  294          CVD   R2,DECNUM            and convert
000003CC  D211 8EBE 8EA8       000010BE    000010A8  295          MVC   PRT3,EDIT
000003D2  DE11 8EBE 8ED4       000010BE    000010D4  296          ED    PRT3,DECNUM
000003D8  D201 8E44 8ECC       00001044    000010CC  297          MVC   PRTM5(2),PRT3+14     fill in message with M5 field
                                                    298
000003DE  B982 0022                                 299          XGR   R2,R2                get M6 as U8
000003E2  4320 5008                        00000008  300          IC    R2,M6
000003E6  4E20 8ED4                        000010D4  301          CVD   R2,DECNUM            and convert
000003EA  D211 8EBE 8EA8       000010BE    000010A8  302          MVC   PRT3,EDIT
000003F0  DE11 8EBE 8ED4       000010BE    000010D4  303          ED    PRT3,DECNUM
000003F6  D201 8E50 8ECC       00001050    000010CC  304          MVC   PRTM6(2),PRT3+14     fill in message with M6 field
                                                    305
000003FC  4100 004B                        0000004B  306          LA    R0,PRTLNG            message length
00000400  4110 8E08                        00001008  307          LA    R1,PRTLINE           messagfe address
00000404  45F0 8226                        00000426  308          BAL   R15,RPTERROR


                                                    310 ************************************************************************
                                                    311 * continue after a failed test
                                                    312 ************************************************************************
                                 00000408  00000001  313 FAILCONT EQU   *
00000408  5800 8358                        00000558  314          L     R0,=F'1'                set failed test indicator
0000040C  5000 8E00                        00001000  315          ST    R0,FAILED
                                                    316
00000410  41C0 C004                        00000004  317          LA    R12,4(0,R12)            next test address
00000414  47F0 80D4                        000002D4  318          B     NEXTE7


                                                    320 ************************************************************************
                                                    321 * end of testing; set ending psw
                                                    322 ************************************************************************
                                 00000418  00000001  323 ENDTEST  EQU   *
00000418  5810 8E00                        00001000  324          L     R1,FAILED         did a test fail?
0000041C  1211                                      325          LTR   R1,R1
0000041E  4780 8328                        00000528  326          BZ    EOJ                  No, exit
00000422  47F0 8340                        00000540  327          B     FAILTEST             Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    329 ************************************************************************
                                                    330 *        RPTERROR                  Report instruction test in error
                                                    331 ************************************************************************

00000426  50F0 8244                          00000444   333 RPTERROR ST    R15,RPTSAVE          Save return address
0000042A  5050 8248                          00000448   334          ST    R5,RPTSVR5           Save R5
                                                    335 *
                                                    336 *        Use Hercules Diagnose for Message to console
                                                    337 *
0000042E  9002 8250                          00000450   338          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000432  4520 8260                          00000460   339          BAL   R2,MSG               call Hercules console MSG display
00000436  9802 8250                          00000450   340          LM    R0,R2,RPTDWSAV       restore regs

0000043A  5850 8248                          00000448   342          L     R5,RPTSVR5           Restore R5
0000043E  58F0 8244                          00000444   343          L     R15,RPTSAVE          Restore return address
00000442  07FF                                          344          BR    R15                  Return to caller

00000444  00000000                                      346 RPTSAVE  DC    F'0'                 R15 save area
00000448  00000000                                      347 RPTSVR5  DC    F'0'                 R5 save area

00000450  00000000 00000000                             349 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    351 ************************************************************************
                                                    352 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    353 *              R2 = return address
                                                    354 ************************************************************************
00000460  4900 835C                       0000055C  356 MSG      CH    R0,=H'0'                Do we even HAVE a message?
00000464  07D2                                      357           BNHR  R2                      No, ignore

00000466  9002 829C                       0000049C  359           STM   R0,R2,MSGSAVE           Save registers

0000046A  4900 835E                       0000055E  361           CH    R0,=AL2(L'MSGMSG)       Message length within limits?
0000046E  47D0 8276                       00000476  362           BNH   MSGOK                   Yes, continue
00000472  4100 005F                       0000005F  363           LA    R0,L'MSGMSG             No, set to maximum

00000476  1820                                      365 MSGOK     LR    R2,R0                   Copy length to work register
00000478  0620                                      366           BCTR  R2,0                    Minus-1 for execute
0000047A  4420 82A8                       000004A8  367           EX    R2,MSGMVC               Copy message to O/P buffer

0000047E  4120 200A                       0000000A  369           LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
00000482  4110 82AE                       000004AE  370           LA    R1,MSGCMD               Point to true command

00000486  83120008                                  372           DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
0000048A  4780 8296                       00000496  373           BZ    MSGRET                  Return if successful
                                                    374
0000048E  1222                                      375           LTR   R2,R2                   Is Diag8 Ry (R2) 0?
00000490  4780 8296                       00000496  376           BZ    MSGRET                    an error occurred but coninue
                                                    377
00000494  0000                                      378           DC    H'0'                    CRASH for debugging purposes

00000496  9802 829C                       0000049C  380 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
0000049A  07F2                                      381           BR    R2                      Return to caller

0000049C  00000000 00000000                         383 MSGSAVE  DC    3F'0'                   Registers save area
000004A8  D200 82B7 1000        000004B7  00000000  384 MSGMVC   MVC   MSGMSG(0),0(R1)          Executed instruction

000004AE  D4E2C7D5 D6C8405C                         386 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
000004B7  40404040 40404040                         387 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                    388
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     390 ********************************************************************************
                                                     391 *        Normal completion or Abnormal termination PSWs
                                                     392 ********************************************************************************

00000518  00020001 80000000                          394 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
00000528  B2B2 8318                  00000518        396 EOJ      LPSWE EOJPSW               Normal completion

00000530  00020001 80000000                          398 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
00000540  B2B2 8330                  00000530        400 FAILTEST LPSWE FAILPSW              Abnormal termination

                                                     402 ********************************************************************************
                                                     403 *        Working Storage
                                                     404 ********************************************************************************

00000544  00000000                                   406 CTLR0    DS    F                    CR0
00000548  00000000                                   407         DS    F

0000054C                                             409         LTORG ,                    Literals pool
0000054C  00000040                                   410               =F'64'
00000550  000058DC                                   411               =A(E7TESTS)
00000554  00000003                                   412               =XL4'3'
00000558  00000001                                   413               =F'1'
0000055C  0000                                       414               =H'0'
0000055E  005F                                       415               =AL2(L'MSGMSG)
                                                     416
                                                     417 *        some constants
                                                     418
                       00000400  00000001            419 K        EQU   1024               One KB
                       00001000  00000001            420 PAGE     EQU   (4*K)              Size of one page
                       00010000  00000001            421 K64      EQU   (64*K)             64 KB
                       00100000  00000001            422 MB       EQU   (K*K)               1 MB
                                                     423
                       AABBCCDD  00000001            424 REG2PATT EQU   X'AABBCCDD'      Polluted Register pattern
                       000000DD  00000001            425 REG2LOW  EQU         X'DD'      (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    427 *=====================================================================
                                                    428 *
                                                    429 *  NOTE: start data on an address that is easy to display
                                                    430 *        within Hercules
                                                    431 *
                                                    432 *=====================================================================
                                                    433
00000560                      00000560  00001000    434          ORG   ZVE7TST+X'1000'
00001000  00000000                                  435 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                  436 TESTING  DC    F'0'                    current test number

                                                    438 ***************************************************************************
                                                    439 *        TEST failed : result messgae
                                                    440 ***************************************************************************
                                                    441 *
                                                    442 *        failed message and associated editting
                                                    443 *
00001008  40404040 40404040                         444 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                    445 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                         446          DC    C' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                         447 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 884094F5                         448          DC    C' with m5='
00001044  A7A7                                      449 PRTM5    DC    C'xx'
00001046  6B                                        450          DC    C','
00001047  40A689A3 884094F6                         451          DC    C' with m6='
00001050  A7A7                                      452 PRTM6    DC    C'xx'
00001052  4B                                        453          DC    C'.'
                                0000004B  00000001  454 PRTLNG   EQU   *-PRTLINE
                                                    455
                                                    456 ***************************************************************************
                                                    457 *        TEST failed : CC message
                                                    458 ***************************************************************************
                                                    459 *
                                                    460 *        failed message and associated editting
                                                    461 *
00001053  40404040 40404040                         462 CCPRTLINE DC   C'         Test # '
00001063  A7A7A7                                    463 CCPRTNUM DC    C'xxx'
00001066  40A69996 95874083                         464          DC    c' wrong cc for instruction '
00001080  A7A7A7A7 A7A7A7A7                         465 CCPRTNAME DC    CL8'xxxxxxxx'
00001088  4085A797 8583A385                         466          DC    C' expected: cc='
00001096  A7                                        467 CCPRTEXP DC    C'x'
00001097  6B                                        468          DC    C','
00001098  40998583 8589A585                         469          DC    C' received: cc='
000010A6  A7                                        470 CCPRTGOT DC    C'x'
000010A7  4B                                        471          DC    C'.'
                                00000055  00000001  472 CCPRTLNG   EQU   *-CCPRTLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     474 ************************************************************************
                                                     475 *        TEST failed : message working storge
                                                     476 ************************************************************************
000010A8  40212020 20202020                          477 EDIT     DC    XL18'40212020202020202020202020202020'
                                                     478
000010BA  7E7E7E6E                                   479          DC    C'===>'
000010BE  40404040 40404040                          480 PRT3     DC    CL18' '
000010D0  4C7E7E7E                                   481          DC    C'<==='
000010D4  00000000 00000000                          482 DECNUM   DS    CL16


                                                     484 ************************************************************************
                                                     485 *        Vector instruction results, pollution and input
                                                     486 ************************************************************************
000010E4                                             487          DS    0F
000010E4  00000000 00000000                          488          DS    XL16                                        gap
000010F4  FFFFFFFF FFFFFFFF                          489 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
00001104  00000000 00000000                          490          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                      492 ********************************************************************************
                                                      493 *        E7TEST DSECT
                                                      494 ********************************************************************************


                                                      496 E7TEST   DSECT ,
00000000  00000000                                    497 TSUB     DC    A(0)           pointer  to test
00000004  0000                                        498 TNUM     DC    H'00'          Test Number
00000006  00                                          499          DC    X'00'
00000007  00                                          500 M5       DC    HL1'00'                 m5 used
00000008  00                                          501 M6       DC    HL1'00'                 m6 used
00000009  00                                          502 CC       DC    HL1'00'                 cc expected
0000000A  00                                          503 CCMASK   DC    HL1'00'                 not expected CC mask
                                                      504 *
                                                      505 *        CC extrtaction
                                                      506 *
0000000C  00000000 00000000                           507 CCPSW    DS    2F                      extract PSW after test (has CC)
00000014  00                                          508 CCFOUND  DS    X                       extracted cc
                                                      509
00000015  40404040 40404040                           510 OPNAME   DC    CL8' '         E7 name
00000020  00000000                                    511 V2ADDR   DC    A(0)           address of v2 source
00000024  00000000                                    512 V3ADDR   DC    A(0)           address of v3 source
00000028  00000000                                    513 V4ADDR   DC    A(0)           address of v4 source
0000002C  00000000                                    514 RELEN    DC    A(0)           RESULT LENGTH
00000030  00000000                                    515 READDR   DC    A(0)           result (expected) address
00000038  00000000 00000000                           516          DS    FD                gap
00000040  00000000 00000000                           517 V1OUTPUT DS    XL16           V1 Output
00000050  00000000 00000000                           518          DS    FD                gap
                                                      519
                                                      520 *        test routine will be here (from VRR-d macro)
                                                      521 *
                                                      522 *        followed by
                                                      523 *              EXPECTED RESULT


                          00000000  00005A3F          525 ZVE7TST  CSECT ,
00001114                                              526          DS    0F

                                                      528 ********************************************************************************
                                                      529 *     Macros to help build test tables
                                                      530 ********************************************************************************


                                                      532 *
                                                      533 * macro to generate individual test
                                                      534 *
                                                      535          MACRO
                                                      536          VRR_D &INST,&M5,&M6,&CC
                                                      537 .*                                 &INST   - VRR-d instruction under test
                                                      538 .*                                 &M5     - m5 field - element size
                                                      539 .*                                 &M6     - m6 field - ZS
                                                      540 .*                                 &CC     - expected CC
                                                      541
                                                      542          LCLA  &XCC(4)  &XCC has mask values for FAILED condition codes
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   543 &XCC(1)  SETA  7                CC != 0
                                                   544 &XCC(2)  SETA  11               CC != 1
                                                   545 &XCC(3)  SETA  13               CC != 2
                                                   546 &XCC(4)  SETA  14               CC != 3
                                                   547
                                                   548          GBLA  &TNUM
                                                   549 &TNUM    SETA  &TNUM+1
                                                   550
                                                   551          DS    0FD
                                                   552          USING *,R5             base for test data and test routine
                                                   553
                                                   554 T&TNUM   DC    A(X&TNUM)        address of test routine
                                                   555          DC    H'&TNUM'         test number
                                                   556          DC    X'00'
                                                   557          DC    HL1'&M5'               m5 used
                                                   558          DC    HL1'&M6'               m6 used
                                                   559          DC    HL1'&CC'          CC
                                                   560          DC    HL1'&XCC(&CC+1)'  CC failed mask
                                                   561
                                                   562          DS    2F                extracted PSW after test (has CC)
                                                   563          DC    X'FF'             extracted CC, if test failed
                                                   564
                                                   565          DC    CL8'&INST'       instruction name
                                                   566          DC    A(RE&TNUM+16)    address of v2 source
                                                   567          DC    A(RE&TNUM+32)    address of v3 source
                                                   568          DC    A(RE&TNUM+48)    address of v4 source
                                                   569          DC    A(16)            result length
                                                   570 REA&TNUM DC    A(RE&TNUM)       result address
                                                   571          DS    FD               gap
                                                   572 V1O&TNUM DS    XL16             V1 output
                                                   573          DS    FD               gap
                                                   574 .*
                                                   575 *
                                                   576 X&TNUM   DS    0F
                                                   577          LGF   R1,V2ADDR        load v2 source
                                                   578          VL    v22,0(R1)        use v22 to test decoder
                                                   579
                                                   580          LGF   R1,V3ADDR        load v3 source
                                                   581          VL    v23,0(R1)        use v23 to test decoder
                                                   582
                                                   583          LGF   R1,V4ADDR        load v4 source
                                                   584          VL    v24,0(R1)        use v24 to test decoder
                                                   585
                                                   586          &INST V22,V22,V23,V24,&M5,&M6  instruction (dest is a source)
                                                   587
                                                   588          EPSW  R2,R0             extract psw
                                                   589          ST    R2,CCPSW             to save CC
                                                   590
                                                   591          VST   V22,V1O&TNUM      save v1 output
                                                   592
                                                   593          BR    R11              return
                                                   594
                                                   595 RE&TNUM  DC    0F               xl16 expected result
                                                   596
                                                   597          DROP  R5
                                                   598          MEND
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      600 *
                                                      601 * macro to generate table of pointers to individual tests
                                                      602 *
                                                      603          MACRO
                                                      604          PTTABLE
                                                      605          GBLA  &TNUM
                                                      606          LCLA  &CUR
                                                      607 &CUR     SETA  1
                                                      608 .*
                                                      609 TTABLE   DS    0F
                                                      610 .LOOP    ANOP
                                                      611 .*
                                                      612          DC    A(T&CUR)
                                                      613 .*
                                                      614 &CUR     SETA  &CUR+1
                                                      615          AIF   (&CUR LE &TNUM).LOOP
                                                      616 *
                                                      617          DC    A(0)              END OF TABLE
                                                      618          DC    A(0)
                                                      619 .*
                                                      620          MEND
                                                      621
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     623 ********************************************************************************
                                                     624 *        E7 VRR-d tests
                                                     625 ********************************************************************************
                                                     626          PRINT DATA
00001118  00000000 00000000                          627          DS    FD
                                                     628 *
                                                     629 *   E78B VSTRS  - Vector String Search
                                                     630 *
                                                     631 *        VRR-d instruction, m5, M6, CC
                                                     632 *             followed by
                                                     633 *                16 byte expected result (V1)
                                                     634 *                16 byte V2 source
                                                     635 *                16 byte V3 source
                                                     636 *                16 byte V4 source
                                                     637 *-------------------------------------------------------------------
                                                     638 * VSTRS  - Vector String Search
                                                     639 *-------------------------------------------------------------------
                                                     640
                                                     641 *-------------------------------------------------------------------
                                                     642 * case 0 - test: ZS=0
                                                     643 *-------------------------------------------------------------------
                                                     644 * test - ZS=0 CC=0
                                                     645 *NO Match
                                                     646 *Byte
                                                     647          VRR_D VSTRS,0,0,0                              no match
00001120                                             648+         DS    0FD
00001120                          00001120           649+         USING *,R5                 base for test data and test routine
00001120  00001178                                   650+T1       DC    A(X1)                address of test routine
00001124  0001                                       651+         DC    H'1'                 test number
00001126  00                                         652+         DC    X'00'
00001127  00                                         653+         DC    HL1'0'                     m5 used
00001128  00                                         654+         DC    HL1'0'                     m6 used
00001129  00                                         655+         DC    HL1'0'               CC
0000112A  07                                         656+         DC    HL1'7'               CC failed mask
0000112C  00000000 00000000                          657+         DS    2F                   extracted PSW after test (has CC)
00001134  FF                                         658+         DC    X'FF'                extracted CC, if test failed
00001135  E5E2E3D9 E2404040                          659+         DC    CL8'VSTRS'           instruction name
00001140  000011C4                                   660+         DC    A(RE1+16)            address of v2 source
00001144  000011D4                                   661+         DC    A(RE1+32)            address of v3 source
00001148  000011E4                                   662+         DC    A(RE1+48)            address of v4 source
0000114C  00000010                                   663+         DC    A(16)                result length
00001150  000011B4                                   664+REA1     DC    A(RE1)               result address
00001158  00000000 00000000                          665+         DS    FD                   gap
00001160  00000000 00000000                          666+V1O1     DS    XL16                 V1 output
00001168  00000000 00000000
00001170  00000000 00000000                          667+         DS    FD                   gap
                                                     668+*
00001178                                             669+X1       DS    0F
00001178  E310 5020 0014                 00000020    670+         LGF   R1,V2ADDR            load v2 source
0000117E  E761 0000 0806                 00000000    671+         VL    v22,0(R1)            use v22 to test decoder
00001184  E310 5024 0014                 00000024    672+         LGF   R1,V3ADDR            load v3 source
0000118A  E771 0000 0806                 00000000    673+         VL    v23,0(R1)            use v23 to test decoder
00001190  E310 5028 0014                 00000028    674+         LGF   R1,V4ADDR            load v4 source
00001196  E781 0000 0806                 00000000    675+         VL    v24,0(R1)            use v24 to test decoder
0000119C  E766 7000 8F8B                             676+         VSTRS V22,V22,V23,V24,0,0      instruction (dest is a source)
000011A2  B98D 0020                                  677+         EPSW  R2,R0                 extract psw
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000011A6  5020 500C                     0000000C   678+         ST    R2,CCPSW              to save CC
000011AA  E760 5040 080E                00001160   679+         VST   V22,V1O1             save v1 output
000011B0  07FB                                     680+         BR    R11                 return
000011B4                                           681+RE1      DC    0F                  xl16 expected result
000011B4                                           682+         DROP  R5
000011B4  00000000 00000010                        683          DC    XL16'0000000000000010 0000000000000000'   V1
000011BC  00000000 00000000
000011C4  01020304 05060708                        684          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v2
000011CC  090A0B0C 0D0E0F10
000011D4  F0F1F2F3 F4F5F6F7                        685          DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'   v3
000011DC  F8F9FAFB FCFDFEFF
000011E4  00000000 00000008                        686          DC    XL16'0000000000000008 0000000000000000'   v4
000011EC  00000000 00000000
                                                   687
                                                   688 *Halfword
                                                   689          VRR_D VSTRS,1,0,0                               no match
000011F8                                           690+         DS    0FD
000011F8                        000011F8           691+         USING *,R5                base for test data and test routine
000011F8  00001250                                 692+T2       DC    A(X2)               address of test routine
000011FC  0002                                     693+         DC    H'2'                test number
000011FE  00                                       694+         DC    X'00'
000011FF  01                                       695+         DC    HL1'1'                    m5 used
00001200  00                                       696+         DC    HL1'0'                    m6 used
00001201  00                                       697+         DC    HL1'0'               CC
00001202  07                                       698+         DC    HL1'7'               CC failed mask
00001204  00000000 00000000                        699+         DS    2F                   extracted PSW after test (has CC)
0000120C  FF                                       700+         DC    X'FF'                 extracted CC, if test failed
0000120D  E5E2E3D9 E2404040                        701+         DC    CL8'VSTRS'           instruction name
00001218  0000129C                                 702+         DC    A(RE2+16)            address of v2 source
0000121C  000012AC                                 703+         DC    A(RE2+32)            address of v3 source
00001220  000012BC                                 704+         DC    A(RE2+48)            address of v4 source
00001224  00000010                                 705+         DC    A(16)                result length
00001228  0000128C                                 706+REA2     DC    A(RE2)               result address
00001230  00000000 00000000                        707+         DS    FD                   gap
00001238  00000000 00000000                        708+V1O2     DS    XL16                 V1 output
00001240  00000000 00000000
00001248  00000000 00000000                        709+         DS    FD                   gap
                                                   710+*
00001250                                           711+X2       DS    0F
00001250  E310 5020 0014            00000020       712+         LGF   R1,V2ADDR            load v2 source
00001256  E761 0000 0806            00000000       713+         VL    v22,0(R1)            use v22 to test decoder
0000125C  E310 5024 0014            00000024       714+         LGF   R1,V3ADDR            load v3 source
00001262  E771 0000 0806            00000000       715+         VL    v23,0(R1)            use v23 to test decoder
00001268  E310 5028 0014            00000028       716+         LGF   R1,V4ADDR            load v4 source
0000126E  E781 0000 0806            00000000       717+         VL    v24,0(R1)            use v24 to test decoder
00001274  E766 7100 8F8B                           718+         VSTRS V22,V22,V23,V24,1,0       instruction (dest is a source)
0000127A  B98D 0020                                719+         EPSW  R2,R0                extract psw
0000127E  5020 500C                     0000000C   720+         ST    R2,CCPSW                 to save CC
00001282  E760 9038 080E                00001238   721+         VST   V22,V1O2             save v1 output
00001288  07FB                                     722+         BR    R11                  return
0000128C                                           723+RE2      DC    0F                   xl16 expected result
0000128C                                           724+         DROP  R5
0000128C  00000000 00000010                        725          DC    XL16'0000000000000010 0000000000000000'   V1
00001294  00000000 00000000
0000129C  01020304 05060708                        726          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v2
000012A4  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000012AC  F0F1F2F3 F4F5F6F7                          727          DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'   v3
000012B4  F8F9FAFB FCFDFEFF
000012BC  00000000 00000008                          728          DC    XL16'0000000000000008 0000000000000000'   v4
000012C4  00000000 00000000
                                                     729
                                                     730 *Word
                                                     731          VRR_D VSTRS,2,0,0                               no match
000012D0                                             732+         DS    0FD
000012D0                       000012D0              733+         USING *,R5              base for test data and test routine
000012D0  00001328                                   734+T3       DC    A(X3)             address of test routine
000012D4  0003                                       735+         DC    H'3'              test number
000012D6  00                                         736+         DC    X'00'
000012D7  02                                         737+         DC    HL1'2'                  m5 used
000012D8  00                                         738+         DC    HL1'0'                  m6 used
000012D9  00                                         739+         DC    HL1'0'             CC
000012DA  07                                         740+         DC    HL1'7'             CC failed mask
000012DC  00000000 00000000                          741+         DS    2F                 extracted PSW after test (has CC)
000012E4  FF                                         742+         DC    X'FF'              extracted CC, if test failed
000012E5  E5E2E3D9 E2404040                          743+         DC    CL8'VSTRS'        instruction name
000012F0  00001374                                   744+         DC    A(RE3+16)         address of v2 source
000012F4  00001384                                   745+         DC    A(RE3+32)         address of v3 source
000012F8  00001394                                   746+         DC    A(RE3+48)         address of v4 source
000012FC  00000010                                   747+         DC    A(16)             result length
00001300  00001364                                   748+REA3     DC    A(RE3)            result address
00001308  00000000 00000000                          749+         DS    FD                gap
00001310  00000000 00000000                          750+V1O3     DS    XL16              V1 output
00001318  00000000 00000000
00001320  00000000 00000000                          751+         DS    FD                gap
                                                     752+*
00001328                                             753+X3       DS    0F
00001328  E310 5020 0014                 00000020    754+         LGF   R1,V2ADDR         load v2 source
0000132E  E761 0000 0806                 00000000    755+         VL    v22,0(R1)         use v22 to test decoder
00001334  E310 5024 0014                 00000024    756+         LGF   R1,V3ADDR         load v3 source
0000133A  E771 0000 0806                 00000000    757+         VL    v23,0(R1)         use v23 to test decoder
00001340  E310 5028 0014                 00000028    758+         LGF   R1,V4ADDR         load v4 source
00001346  E781 0000 0806                 00000000    759+         VL    v24,0(R1)         use v24 to test decoder
0000134C  E766 7200 8F8B                             760+         VSTRS V22,V22,V23,V24,2,0      instruction (dest is a source)
00001352  B98D 0020                                  761+         EPSW  R2,R0              extract psw
00001356  5020 500C                      0000000C    762+         ST    R2,CCPSW              to save CC
0000135A  E760 5040 080E                 00001310    763+         VST   V22,V1O3           save v1 output
00001360  07FB                                       764+         BR    R11               return
00001364                                             765+RE3      DC    0F                xl16 expected result
00001364                                             766+         DROP  R5
00001364  00000000 00000010                          767          DC    XL16'0000000000000010 0000000000000000'   V1
0000136C  00000000 00000000
00001374  01020304 05060708                          768          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v2
0000137C  090A0B0C 0D0E0F10
00001384  F0F1F2F3 F4F5F6F7                          769          DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'   v3
0000138C  F8F9FAFB FCFDFEFF
00001394  00000000 00000008                          770          DC    XL16'0000000000000008 0000000000000000'   v4
0000139C  00000000 00000000
                                                     771
                                                     772 *Full Match CC=2
                                                     773 *Byte
                                                     774          VRR_D VSTRS,0,0,2                               full match
000013A8                                             775+         DS    0FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000013A8                     000013A8               776+          USING *,R5              base for test data and test routine
000013A8  00001400                                  777+T4        DC    A(X4)             address of test routine
000013AC  0004                                      778+          DC    H'4'              test number
000013AE  00                                        779+          DC    X'00'
000013AF  00                                        780+          DC    HL1'0'                  m5 used
000013B0  00                                        781+          DC    HL1'0'                  m6 used
000013B1  02                                        782+          DC    HL1'2'             CC
000013B2  0D                                        783+          DC    HL1'13'            CC failed mask
000013B4  00000000 00000000                         784+          DS    2F                 extracted PSW after test (has CC)
000013BC  FF                                        785+          DC    X'FF'              extracted CC, if test failed
000013BD  E5E2E3D9 E2404040                         786+          DC    CL8'VSTRS'        instruction name
000013C8  0000144C                                  787+          DC    A(RE4+16)         address of v2 source
000013CC  0000145C                                  788+          DC    A(RE4+32)         address of v3 source
000013D0  0000146C                                  789+          DC    A(RE4+48)         address of v4 source
000013D4  00000010                                  790+          DC    A(16)             result length
000013D8  0000143C                                  791+REA4      DC    A(RE4)            result address
000013E0  00000000 00000000                         792+          DS    FD                gap
000013E8  00000000 00000000                         793+V1O4      DS    XL16              V1 output
000013F0  00000000 00000000
000013F8  00000000 00000000                         794+          DS    FD                gap
                                                    795+*
00001400                                            796+X4        DS    0F
00001400  E310 5020 0014                 00000020   797+          LGF   R1,V2ADDR         load v2 source
00001406  E761 0000 0806                 00000000   798+          VL    v22,0(R1)         use v22 to test decoder
0000140C  E310 5024 0014                 00000024   799+          LGF   R1,V3ADDR         load v3 source
00001412  E771 0000 0806                 00000000   800+          VL    v23,0(R1)         use v23 to test decoder
00001418  E310 5028 0014                 00000028   801+          LGF   R1,V4ADDR         load v4 source
0000141E  E781 0000 0806                 00000000   802+          VL    v24,0(R1)         use v24 to test decoder
00001424  E766 7000 8F8B                            803+          VSTRS V22,V22,V23,V24,0,0     instruction (dest is a source)
0000142A  B98D 0020                                 804+          EPSW  R2,R0              extract psw
0000142E  5020 500C                      0000000C   805+          ST    R2,CCPSW              to save CC
00001432  E760 5040 080E                 000013E8   806+          VST   V22,V1O4             save v1 output
00001438  07FB                                      807+          BR    R11               return
0000143C                                            808+RE4       DC    0F                xl16 expected result
0000143C                                            809+          DROP  R5
0000143C  00000000 00000008                         810           DC    XL16'0000000000000008 0000000000000000'   V1
00001444  00000000 00000000
0000144C  F0F1F2F3 F4F5F6F7                         811           DC    XL16'F0F1F2F3F4F5F6F7 01020304AAFDFEFF'   v2
00001454  01020304 AAFDFEFF
0000145C  01020304 05060708                         812           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00001464  090A0B0C 0D0E0F10
0000146C  00000000 00000004                         813           DC    XL16'0000000000000004 0000000000000000'   v4
00001474  00000000 00000000
                                                    814
                                                    815 *Halfword
                                                    816           VRR_D VSTRS,1,0,2                               full match
00001480                                            817+          DS    0FD
00001480                         00001480           818+          USING *,R5              base for test data and test routine
00001480  000014D8                                  819+T5        DC    A(X5)             address of test routine
00001484  0005                                      820+          DC    H'5'              test number
00001486  00                                        821+          DC    X'00'
00001487  01                                        822+          DC    HL1'1'                  m5 used
00001488  00                                        823+          DC    HL1'0'                  m6 used
00001489  02                                        824+          DC    HL1'2'             CC
0000148A  0D                                        825+          DC    HL1'13'            CC failed mask
0000148C  00000000 00000000                         826+          DS    2F                 extracted PSW after test (has CC)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001494  FF                                       827+         DC    X'FF'                extracted CC, if test failed
00001495  E5E2E3D9 E2404040                         828+         DC    CL8'VSTRS'          instruction name
000014A0  00001524                                 829+         DC    A(RE5+16)           address of v2 source
000014A4  00001534                                 830+         DC    A(RE5+32)           address of v3 source
000014A8  00001544                                 831+         DC    A(RE5+48)           address of v4 source
000014AC  00000010                                 832+         DC    A(16)               result length
000014B0  00001514                                 833+REA5     DC    A(RE5)              result address
000014B8  00000000 00000000                        834+         DS    FD                  gap
000014C0  00000000 00000000                        835+V1O5     DS    XL16                V1 output
000014C8  00000000 00000000
000014D0  00000000 00000000                        836+         DS    FD                  gap
                                                   837+*
000014D8                                           838+X5       DS    0F
000014D8  E310 5020 0014                00000020   839+         LGF   R1,V2ADDR           load v2 source
000014DE  E761 0000 0806                00000000   840+         VL    v22,0(R1)           use v22 to test decoder
000014E4  E310 5024 0014                00000024   841+         LGF   R1,V3ADDR           load v3 source
000014EA  E771 0000 0806                00000000   842+         VL    v23,0(R1)           use v23 to test decoder
000014F0  E310 5028 0014                00000028   843+         LGF   R1,V4ADDR           load v4 source
000014F6  E781 0000 0806                00000000   844+         VL    v24,0(R1)           use v24 to test decoder
000014FC  E766 7100 8F8B                           845+         VSTRS V22,V22,V23,V24,1,0      instruction (dest is a source)
00001502  B98D 0020                                846+         EPSW  R2,R0               extract psw
00001506  5020 500C                     0000000C  847+         ST    R2,CCPSW               to save CC
0000150A  E760 5040 080E                000014C0  848+         VST   V22,V1O5            save v1 output
00001510  07FB                                     849+         BR    R11                 return
00001514                                           850+RE5      DC    0F                  xl16 expected result
00001514                                           851+         DROP  R5
00001514  00000000 00000008                        852          DC    XL16'0000000000000008 0000000000000000'   V1
0000151C  00000000 00000000
00001524  F0F1F2F3 F4F5F6F7                        853          DC    XL16'F0F1F2F3F4F5F6F7 01020304AAFDFEFF'   v2
0000152C  01020304 AAFDFEFF
00001534  01020304 05060708                        854          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
0000153C  090A0B0C 0D0E0F10
00001544  00000000 00000004                        855          DC    XL16'0000000000000004 0000000000000000'   v4
0000154C  00000000 00000000
                                                   856
                                                   857 *Word
                                                   858          VRR_D VSTRS,2,0,2                               full match
00001558                                           859+         DS    0FD
00001558                        00001558           860+         USING *,R5                base for test data and test routine
00001558  000015B0                                 861+T6       DC    A(X6)               address of test routine
0000155C  0006                                     862+         DC    H'6'                test number
0000155E  00                                       863+         DC    X'00'
0000155F  02                                       864+         DC    HL1'2'                  m5 used
00001560  00                                       865+         DC    HL1'0'                  m6 used
00001561  02                                       866+         DC    HL1'2'               CC
00001562  0D                                       867+         DC    HL1'13'              CC failed mask
00001564  00000000 00000000                        868+         DS    2F                   extracted PSW after test (has CC)
0000156C  FF                                       869+         DC    X'FF'                extracted CC, if test failed
0000156D  E5E2E3D9 E2404040                        870+         DC    CL8'VSTRS'          instruction name
00001578  000015FC                                 871+         DC    A(RE6+16)           address of v2 source
0000157C  0000160C                                 872+         DC    A(RE6+32)           address of v3 source
00001580  0000161C                                 873+         DC    A(RE6+48)           address of v4 source
00001584  00000010                                 874+         DC    A(16)               result length
00001588  000015EC                                 875+REA6     DC    A(RE6)              result address
00001590  00000000 00000000                        876+         DS    FD                  gap
00001598  00000000 00000000                        877+V1O6     DS    XL16                V1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000015A0  00000000 00000000
000015A8  00000000 00000000                          878+         DS    FD                gap
                                                     879+*
000015B0                                             880+X6       DS    0F
000015B0  E310 5020 0014                 00000020    881+         LGF   R1,V2ADDR         load v2 source
000015B6  E761 0000 0806                 00000000    882+         VL    v22,0(R1)         use v22 to test decoder
000015BC  E310 5024 0014                 00000024    883+         LGF   R1,V3ADDR         load v3 source
000015C2  E771 0000 0806                 00000000    884+         VL    v23,0(R1)         use v23 to test decoder
000015C8  E310 5028 0014                 00000028    885+         LGF   R1,V4ADDR         load v4 source
000015CE  E781 0000 0806                 00000000    886+         VL    v24,0(R1)         use v24 to test decoder
000015D4  E766 7200 8F8B                             887+         VSTRS V22,V22,V23,V24,2,0      instruction (dest is a source)
000015DA  B98D 0020                                  888+         EPSW  R2,R0              extract psw
000015DE  5020 500C                      0000000C    889+         ST    R2,CCPSW              to save CC
000015E2  E760 5040 080E                 00001598    890+         VST   V22,V1O6             save v1 output
000015E8  07FB                                       891+         BR    R11               return
000015EC                                             892+RE6      DC    0F                xl16 expected result
000015EC                                             893+         DROP  R5
000015EC  00000000 00000008                          894          DC    XL16'0000000000000008 0000000000000000'   V1
000015F4  00000000 00000000
000015FC  F0F1F2F3 F4F5F6F7                          895          DC    XL16'F0F1F2F3F4F5F6F7 0102030405AAAAFF'   v2
00001604  01020304 05AAAAFF
0000160C  01020304 05060708                          896          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00001614  090A0B0C 0D0E0F10
0000161C  00000000 00000004                          897          DC    XL16'0000000000000004 0000000000000000'   v4
00001624  00000000 00000000
                                                     898
                                                     899 *Partial Match CC=3
                                                     900 *Byte
                                                     901          VRR_D VSTRS,0,0,3                                partial match
00001630                                             902+         DS    0FD
00001630                       00001630              903+         USING *,R5              base for test data and test routine
00001630  00001688                                   904+T7       DC    A(X7)             address of test routine
00001634  0007                                       905+         DC    H'7'              test number
00001636  00                                         906+         DC    X'00'
00001637  00                                         907+         DC    HL1'0'                 m5 used
00001638  00                                         908+         DC    HL1'0'                 m6 used
00001639  03                                         909+         DC    HL1'3'             CC
0000163A  0E                                         910+         DC    HL1'14'            CC failed mask
0000163C  00000000 00000000                          911+         DS    2F                 extracted PSW after test (has CC)
00001644  FF                                         912+         DC    X'FF'              extracted CC, if test failed
00001645  E5E2E3D9 E2404040                          913+         DC    CL8'VSTRS'        instruction name
00001650  000016D4                                   914+         DC    A(RE7+16)         address of v2 source
00001654  000016E4                                   915+         DC    A(RE7+32)         address of v3 source
00001658  000016F4                                   916+         DC    A(RE7+48)         address of v4 source
0000165C  00000010                                   917+         DC    A(16)             result length
00001660  000016C4                                   918+REA7     DC    A(RE7)            result address
00001668  00000000 00000000                          919+         DS    FD                gap
00001670  00000000 00000000                          920+V1O7     DS    XL16              V1 output
00001678  00000000 00000000
00001680  00000000 00000000                          921+         DS    FD                gap
                                                     922+*
00001688                                             923+X7       DS    0F
00001688  E310 5020 0014                 00000020    924+         LGF   R1,V2ADDR         load v2 source
0000168E  E761 0000 0806                 00000000    925+         VL    v22,0(R1)         use v22 to test decoder
00001694  E310 5024 0014                 00000024    926+         LGF   R1,V3ADDR         load v3 source
0000169A  E771 0000 0806                 00000000    927+         VL    v23,0(R1)         use v23 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000016A0  E310 5028 0014                 00000028   928+          LGF   R1,V4ADDR          load v4 source
000016A6  E781 0000 0806                 00000000   929+          VL    v24,0(R1)          use v24 to test decoder
000016AC  E766 7000 8F8B                            930+          VSTRS V22,V22,V23,V24,0,0      instruction (dest is a source)
000016B2  B98D 0020                                 931+          EPSW  R2,R0               extract psw
000016B6  5020 500C                      0000000C   932+          ST    R2,CCPSW               to save CC
000016BA  E760 5040 080E                 00001670   933+          VST   V22,V1O7            save v1 output
000016C0  07FB                                      934+          BR    R11                 return
000016C4                                            935+RE7       DC    0F                  xl16 expected result
000016C4                                            936+          DROP  R5
000016C4  00000000 0000000D                         937           DC    XL16'000000000000000D 0000000000000000'   V1
000016CC  00000000 00000000
000016D4  F0F1F2F3 F4F5F6F7                         938           DC    XL16'F0F1F2F3F4F5F6F7 AAAAFDFEFF010203'   v2
000016DC  AAAAFDFE FF010203
000016E4  01020304 05060708                         939           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000016EC  090A0B0C 0D0E0F10
000016F4  00000000 00000004                         940           DC    XL16'0000000000000004 0000000000000000'   v4
000016FC  00000000 00000000
                                                    941
                                                    942 *Halfword
                                                    943           VRR_D VSTRS,1,0,3                               partial match
00001708                                            944+          DS    0FD
00001708                         00001708           945+          USING *,R5                base for test data and test routine
00001708  00001760                                  946+T8        DC    A(X8)               address of test routine
0000170C  0008                                      947+          DC    H'8'                test number
0000170E  00                                        948+          DC    X'00'
0000170F  01                                        949+          DC    HL1'1'                    m5 used
00001710  00                                        950+          DC    HL1'0'                    m6 used
00001711  03                                        951+          DC    HL1'3'               CC
00001712  0E                                        952+          DC    HL1'14'              CC failed mask
00001714  00000000 00000000                         953+          DS    2F                   extracted PSW after test (has CC)
0000171C  FF                                        954+          DC    X'FF'                extracted CC, if test failed
0000171D  E5E2E3D9 E2404040                         955+          DC    CL8'VSTRS'          instruction name
00001728  000017AC                                  956+          DC    A(RE8+16)           address of v2 source
0000172C  000017BC                                  957+          DC    A(RE8+32)           address of v3 source
00001730  000017CC                                  958+          DC    A(RE8+48)           address of v4 source
00001734  00000010                                  959+          DC    A(16)               result length
00001738  0000179C                                  960+REA8      DC    A(RE8)              result address
00001740  00000000 00000000                         961+          DS    FD                  gap
00001748  00000000 00000000                         962+V1O8      DS    XL16                V1 output
00001750  00000000 00000000
00001758  00000000 00000000                         963+          DS    FD                  gap
                                                    964+*
00001760                                            965+X8        DS    0F
00001760  E310 5020 0014                 00000020   966+          LGF   R1,V2ADDR           load v2 source
00001766  E761 0000 0806                 00000000   967+          VL    v22,0(R1)           use v22 to test decoder
0000176C  E310 5024 0014                 00000024   968+          LGF   R1,V3ADDR           load v3 source
00001772  E771 0000 0806                 00000000   969+          VL    v23,0(R1)           use v23 to test decoder
00001778  E310 5028 0014                 00000028   970+          LGF   R1,V4ADDR           load v4 source
0000177E  E781 0000 0806                 00000000   971+          VL    v24,0(R1)           use v24 to test decoder
00001784  E766 7100 8F8B                            972+          VSTRS V22,V22,V23,V24,1,0      instruction (dest is a source)
0000178A  B98D 0020                                 973+          EPSW  R2,R0               extract psw
0000178E  5020 500C                      0000000C   974+          ST    R2,CCPSW               to save CC
00001792  E760 5040 080E                 00001748   975+          VST   V22,V1O8            save v1 output
00001798  07FB                                      976+          BR    R11                 return
0000179C                                            977+RE8       DC    0F                  xl16 expected result
0000179C                                            978+          DROP  R5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000179C  00000000 0000000A                          979          DC    XL16'000000000000000A 0000000000000000'   V1
000017A4  00000000 00000000
000017AC  F0F1F2F3 F4F5F6F7                          980          DC    XL16'F0F1F2F3F4F5F6F7 AAFF010203040506'   v2
000017B4  AAFF0102 03040506
000017BC  01020304 05060708                          981          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000017C4  090A0B0C 0D0E0F10
000017CC  00000000 00000008                          982          DC    XL16'0000000000000008 0000000000000000'   v4
000017D4  00000000 00000000
                                                     983
                                                     984 *Word
                                                     985          VRR_D VSTRS,2,0,3                               partial match
000017E0                                             986+         DS    0FD
000017E0                      000017E0               987+         USING *,R5              base for test data and test routine
000017E0  00001838                                   988+T9       DC    A(X9)             address of test routine
000017E4  0009                                       989+         DC    H'9'              test number
000017E6  00                                         990+         DC    X'00'
000017E7  02                                         991+         DC    HL1'2'                  m5 used
000017E8  00                                         992+         DC    HL1'0'                  m6 used
000017E9  03                                         993+         DC    HL1'3'             CC
000017EA  0E                                         994+         DC    HL1'14'            CC failed mask
000017EC  00000000 00000000                          995+         DS    2F                 extracted PSW after test (has CC)
000017F4  FF                                         996+         DC    X'FF'              extracted CC, if test failed
000017F5  E5E2E3D9 E2404040                          997+         DC    CL8'VSTRS'        instruction name
00001800  00001884                                   998+         DC    A(RE9+16)         address of v2 source
00001804  00001894                                   999+         DC    A(RE9+32)         address of v3 source
00001808  000018A4                                  1000+         DC    A(RE9+48)         address of v4 source
0000180C  00000010                                  1001+         DC    A(16)             result length
00001810  00001874                                  1002+REA9     DC    A(RE9)            result address
00001818  00000000 00000000                         1003+         DS    FD                gap
00001820  00000000 00000000                         1004+V1O9     DS    XL16              V1 output
00001828  00000000 00000000
00001830  00000000 00000000                         1005+         DS    FD                gap
                                                    1006+*
00001838                                            1007+X9       DS    0F
00001838  E310 5020 0014                 00000020   1008+         LGF   R1,V2ADDR         load v2 source
0000183E  E761 0000 0806                 00000000   1009+         VL    v22,0(R1)         use v22 to test decoder
00001844  E310 5024 0014                 00000024   1010+         LGF   R1,V3ADDR         load v3 source
0000184A  E771 0000 0806                 00000000   1011+         VL    v23,0(R1)         use v23 to test decoder
00001850  E310 5028 0014                 00000028   1012+         LGF   R1,V4ADDR         load v4 source
00001856  E781 0000 0806                 00000000   1013+         VL    v24,0(R1)         use v24 to test decoder
0000185C  E766 7200 8F8B                            1014+         VSTRS V22,V22,V23,V24,2,0      instruction (dest is a source)
00001862  B98D 0020                                 1015+         EPSW  R2,R0              extract psw
00001866  5020 500C                      0000000C   1016+         ST    R2,CCPSW              to save CC
0000186A  E760 5040 080E                 00001820   1017+         VST   V22,V1O9           save v1 output
00001870  07FB                                      1018+         BR    R11               return
00001874                                            1019+RE9      DC    0F                xl16 expected result
00001874                                            1020+         DROP  R5
00001874  00000000 00000008                         1021          DC    XL16'0000000000000008 0000000000000000'   V1
0000187C  00000000 00000000
00001884  F0F1F2F3 F4F5F6F7                         1022          DC    XL16'F0F1F2F3F4F5F6F7 0102030405060708'   v2
0000188C  01020304 05060708
00001894  01020304 05060708                         1023          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
0000189C  090A0B0C 0D0E0F10
000018A4  00000000 0000000C                         1024          DC    XL16'000000000000000C 0000000000000000'   v4
000018AC  00000000 00000000
                                                    1025
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1027 *-------------------------------------------------------------------
                                                   1028 * case 1 - test: ZS=1
                                                   1029 *-------------------------------------------------------------------
                                                   1030 *NO Match ZS=1 CC=0
                                                   1031 *Byte
                                                   1032          VRR_D VSTRS,0,2,0                              no match
000018B8                                           1033+         DS    0FD
000018B8                          000018B8         1034+         USING *,R5              base for test data and test routine
000018B8  00001910                                 1035+T10      DC    A(X10)            address of test routine
000018BC  000A                                     1036+         DC    H'10'             test number
000018BE  00                                       1037+         DC    X'00'
000018BF  00                                       1038+         DC    HL1'0'                  m5 used
000018C0  02                                       1039+         DC    HL1'2'                  m6 used
000018C1  00                                       1040+         DC    HL1'0'             CC
000018C2  07                                       1041+         DC    HL1'7'             CC failed mask
000018C4  00000000 00000000                        1042+         DS    2F                 extracted PSW after test (has CC)
000018CC  FF                                       1043+         DC    X'FF'              extracted CC, if test failed
000018CD  E5E2E3D9 E2404040                        1044+         DC    CL8'VSTRS'        instruction name
000018D8  0000195C                                 1045+         DC    A(RE10+16)        address of v2 source
000018DC  0000196C                                 1046+         DC    A(RE10+32)        address of v3 source
000018E0  0000197C                                 1047+         DC    A(RE10+48)        address of v4 source
000018E4  00000010                                 1048+         DC    A(16)             result length
000018E8  0000194C                                 1049+REA10    DC    A(RE10)           result address
000018F0  00000000 00000000                        1050+         DS    FD                gap
000018F8  00000000 00000000                        1051+V1O10    DS    XL16              V1 output
00001900  00000000 00000000
00001908  00000000 00000000                        1052+         DS    FD                gap
                                                   1053+*
00001910                                           1054+X10      DS    0F
00001910  E310 5020 0014                 00000020  1055+         LGF   R1,V2ADDR         load v2 source
00001916  E761 0000 0806                 00000000  1056+         VL    v22,0(R1)         use v22 to test decoder
0000191C  E310 5024 0014                 00000024  1057+         LGF   R1,V3ADDR         load v3 source
00001922  E771 0000 0806                 00000000  1058+         VL    v23,0(R1)         use v23 to test decoder
00001928  E310 5028 0014                 00000028  1059+         LGF   R1,V4ADDR         load v4 source
0000192E  E781 0000 0806                 00000000  1060+         VL    v24,0(R1)         use v24 to test decoder
00001934  E766 7020 8F8B                           1061+         VSTRS V22,V22,V23,V24,0,2     instruction (dest is a source)
0000193A  B98D 0020                                1062+         EPSW  R2,R0              extract psw
0000193E  5020 500C                      0000000C  1063+         ST    R2,CCPSW              to save CC
00001942  E760 5040 080E                 000018F8  1064+         VST   V22,V1O10          save v1 output
00001948  07FB                                     1065+         BR    R11               return
0000194C                                           1066+RE10     DC    0F                xl16 expected result
0000194C                                           1067+         DROP  R5
0000194C  00000000 00000010                        1068          DC    XL16'0000000000000010 0000000000000000'   V1
00001954  00000000 00000000
0000195C  01020304 05060708                        1069          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v2
00001964  090A0B0C 0D0E0F10
0000196C  F0F1F2F3 F4F5F6F7                        1070          DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'   v3
00001974  F8F9FAFB FCFDFEFF
0000197C  00000000 00000008                        1071          DC    XL16'0000000000000008 0000000000000000'   v4
00001984  00000000 00000000
                                                   1072
                                                   1073 *Halfword
                                                   1074          VRR_D VSTRS,1,2,0                              no match
00001990                                           1075+         DS    0FD
00001990                          00001990         1076+         USING *,R5              base for test data and test routine
00001990  000019E8                                 1077+T11      DC    A(X11)            address of test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001994  000B                                    1078+          DC    H'11'              test number
00001996  00                                      1079+          DC    X'00'
00001997  01                                      1080+          DC    HL1'1'                   m5 used
00001998  02                                      1081+          DC    HL1'2'                   m6 used
00001999  00                                      1082+          DC    HL1'0'              CC
0000199A  07                                      1083+          DC    HL1'7'              CC failed mask
0000199C  00000000 00000000                       1084+          DS    2F                  extracted PSW after test (has CC)
000019A4  FF                                      1085+          DC    X'FF'               extracted CC, if test failed
000019A5  E5E2E3D9 E2404040                       1086+          DC    CL8'VSTRS'         instruction name
000019B0  00001A34                                1087+          DC    A(RE11+16)         address of v2 source
000019B4  00001A44                                1088+          DC    A(RE11+32)         address of v3 source
000019B8  00001A54                                1089+          DC    A(RE11+48)         address of v4 source
000019BC  00000010                                1090+          DC    A(16)              result length
000019C0  00001A24                                1091+REA11     DC    A(RE11)            result address
000019C8  00000000 00000000                       1092+          DS    FD                 gap
000019D0  00000000 00000000                       1093+V1O11     DS    XL16               V1 output
000019D8  00000000 00000000
000019E0  00000000 00000000                       1094+          DS    FD                 gap
                                                  1095+*
000019E8                                          1096+X11       DS    0F
000019E8  E310 5020 0014                 00000020 1097+          LGF   R1,V2ADDR          load v2 source
000019EE  E761 0000 0806                 00000000 1098+          VL    v22,0(R1)          use v22 to test decoder
000019F4  E310 5024 0014                 00000024 1099+          LGF   R1,V3ADDR          load v3 source
000019FA  E771 0000 0806                 00000000 1100+          VL    v23,0(R1)          use v23 to test decoder
00001A00  E310 5028 0014                 00000028 1101+          LGF   R1,V4ADDR          load v4 source
00001A06  E781 0000 0806                 00000000 1102+          VL    v24,0(R1)          use v24 to test decoder
00001A0C  E766 7120 8F8B                          1103+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00001A12  B98D 0020                               1104+          EPSW  R2,R0               extract psw
00001A16  5020 500C                      0000000C 1105+          ST    R2,CCPSW               to save CC
00001A1A  E760 5040 080E                 000019D0 1106+          VST   V22,V1O11           save v1 output
00001A20  07FB                                    1107+          BR    R11                 return
00001A24                                          1108+RE11      DC    0F                  xl16 expected result
00001A24                                          1109+          DROP  R5
00001A24  00000000 00000010                       1110           DC    XL16'0000000000000010 0000000000000000'   V1
00001A2C  00000000 00000000
00001A34  01020304 05060008                       1111           DC    XL16'0102030405060008 090A0B0C0D0E0F10'   v2
00001A3C  090A0B0C 0D0E0F10
00001A44  F0F1F2F3 F4F5F6F7                       1112           DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'   v3
00001A4C  F8F9FAFB FCFDFEFF
00001A54  00000000 00000008                       1113           DC    XL16'0000000000000008 0000000000000000'   v4
00001A5C  00000000 00000000
                                                  1114
                                                  1115 *Word
                                                  1116           VRR_D VSTRS,2,2,0                               no match
00001A68                                          1117+          DS    0FD
00001A68                         00001A68         1118+          USING *,R5               base for test data and test routine
00001A68  00001AC0                                1119+T12       DC    A(X12)             address of test routine
00001A6C  000C                                    1120+          DC    H'12'              test number
00001A6E  00                                      1121+          DC    X'00'
00001A6F  02                                      1122+          DC    HL1'2'                   m5 used
00001A70  02                                      1123+          DC    HL1'2'                   m6 used
00001A71  00                                      1124+          DC    HL1'0'              CC
00001A72  07                                      1125+          DC    HL1'7'              CC failed mask
00001A74  00000000 00000000                       1126+          DS    2F                  extracted PSW after test (has CC)
00001A7C  FF                                      1127+          DC    X'FF'               extracted CC, if test failed
00001A7D  E5E2E3D9 E2404040                       1128+          DC    CL8'VSTRS'         instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001A88  00001B0C                                1129+          DC    A(RE12+16)        address of v2 source
00001A8C  00001B1C                                1130+          DC    A(RE12+32)        address of v3 source
00001A90  00001B2C                                1131+          DC    A(RE12+48)        address of v4 source
00001A94  00000010                                1132+          DC    A(16)             result length
00001A98  00001AFC                                1133+REA12     DC    A(RE12)           result address
00001AA0  00000000 00000000                       1134+          DS    FD                gap
00001AA8  00000000 00000000                       1135+V1O12     DS    XL16              V1 output
00001AB0  00000000 00000000
00001AB8  00000000 00000000                       1136+          DS    FD                gap
                                                  1137+*
00001AC0                                          1138+X12       DS    0F
00001AC0  E310 5020 0014                 00000020 1139+          LGF   R1,V2ADDR         load v2 source
00001AC6  E761 0000 0806                 00000000 1140+          VL    v22,0(R1)         use v22 to test decoder
00001ACC  E310 5024 0014                 00000024 1141+          LGF   R1,V3ADDR         load v3 source
00001AD2  E771 0000 0806                 00000000 1142+          VL    v23,0(R1)         use v23 to test decoder
00001AD8  E310 5028 0014                 00000028 1143+          LGF   R1,V4ADDR         load v4 source
00001ADE  E781 0000 0806                 00000000 1144+          VL    v24,0(R1)         use v24 to test decoder
00001AE4  E766 7220 8F8B                          1145+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00001AEA  B98D 0020                               1146+          EPSW  R2,R0              extract psw
00001AEE  5020 500C                      0000000C 1147+          ST    R2,CCPSW              to save CC
00001AF2  E760 5040 080E                 00001AA8 1148+          VST   V22,V1O12          save v1 output
00001AF8  07FB                                    1149+          BR    R11               return
00001AFC                                          1150+RE12      DC    0F                xl16 expected result
00001AFC                                          1151+          DROP  R5
00001AFC  00000000 00000010                       1152           DC    XL16'0000000000000010 0000000000000000'   V1
00001B04  00000000 00000000
00001B0C  01020304 05060008                       1153           DC    XL16'0102030405060008 090A0B0C0D0E0F10'   v2
00001B14  090A0B0C 0D0E0F10
00001B1C  F0F1F2F3 F4F5F6F7                       1154           DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'   v3
00001B24  F8F9FAFB FCFDFEFF
00001B2C  00000000 00000008                       1155           DC    XL16'0000000000000008 0000000000000000'   v4
00001B34  00000000 00000000
                                                  1156
                                                  1157 *NO Match, Zero char  ZS=1 CC=1
                                                  1158 *Byte
                                                  1159           VRR_D VSTRS,0,2,1                               no match
00001B40                                          1160+          DS    0FD
00001B40                          00001B40        1161+          USING *,R5              base for test data and test routine
00001B40  00001B98                                1162+T13       DC    A(X13)            address of test routine
00001B44  000D                                    1163+          DC    H'13'             test number
00001B46  00                                      1164+          DC    X'00'
00001B47  00                                      1165+          DC    HL1'0'                  m5 used
00001B48  02                                      1166+          DC    HL1'2'                  m6 used
00001B49  01                                      1167+          DC    HL1'1'             CC
00001B4A  0B                                      1168+          DC    HL1'11'            CC failed mask
00001B4C  00000000 00000000                       1169+          DS    2F                 extracted PSW after test (has CC)
00001B54  FF                                      1170+          DC    X'FF'              extracted CC, if test failed
00001B55  E5E2E3D9 E2404040                       1171+          DC    CL8'VSTRS'        instruction name
00001B60  00001BE4                                1172+          DC    A(RE13+16)        address of v2 source
00001B64  00001BF4                                1173+          DC    A(RE13+32)        address of v3 source
00001B68  00001C04                                1174+          DC    A(RE13+48)        address of v4 source
00001B6C  00000010                                1175+          DC    A(16)             result length
00001B70  00001BD4                                1176+REA13     DC    A(RE13)           result address
00001B78  00000000 00000000                       1177+          DS    FD                gap
00001B80  00000000 00000000                       1178+V1O13     DS    XL16              V1 output
00001B88  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001B90  00000000 00000000                        1179+          DS    FD                gap
                                                   1180+*
00001B98                                           1181+X13       DS    0F
00001B98  E310 5020 0014                 00000020  1182+          LGF   R1,V2ADDR         load v2 source
00001B9E  E761 0000 0806                 00000000  1183+          VL    v22,0(R1)         use v22 to test decoder
00001BA4  E310 5024 0014                 00000024  1184+          LGF   R1,V3ADDR         load v3 source
00001BAA  E771 0000 0806                 00000000  1185+          VL    v23,0(R1)         use v23 to test decoder
00001BB0  E310 5028 0014                 00000028  1186+          LGF   R1,V4ADDR         load v4 source
00001BB6  E781 0000 0806                 00000000  1187+          VL    v24,0(R1)         use v24 to test decoder
00001BBC  E766 7020 8F8B                           1188+          VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00001BC2  B98D 0020                                1189+          EPSW  R2,R0              extract psw
00001BC6  5020 500C                      0000000C  1190+          ST    R2,CCPSW              to save CC
00001BCA  E760 5040 080E                 00001B80  1191+          VST   V22,V1O13          save v1 output
00001BD0  07FB                                     1192+          BR    R11               return
00001BD4                                           1193+RE13      DC    0F                xl16 expected result
00001BD4                                           1194+          DROP  R5
00001BD4  00000000 00000010                        1195           DC    XL16'0000000000000010 0000000000000000'   V1
00001BDC  00000000 00000000
00001BE4  01020004 05060708                        1196           DC    XL16'0102000405060708 090A0B0C0D0E0F10'   v2
00001BEC  090A0B0C 0D0E0F10
00001BF4  F0F1F2F3 F4F5F6F7                        1197           DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'   v3
00001BFC  F8F9FAFB FCFDFEFF
00001C04  00000000 00000008                        1198           DC    XL16'0000000000000008 0000000000000000'   v4
00001C0C  00000000 00000000
                                                   1199
                                                   1200 *Halfword
                                                   1201           VRR_D VSTRS,1,2,1                                no match
00001C18                                           1202+          DS    0FD
00001C18                         00001C18          1203+          USING *,R5              base for test data and test routine
00001C18  00001C70                                 1204+T14       DC    A(X14)            address of test routine
00001C1C  000E                                     1205+          DC    H'14'             test number
00001C1E  00                                       1206+          DC    X'00'
00001C1F  01                                       1207+          DC    HL1'1'                 m5 used
00001C20  02                                       1208+          DC    HL1'2'                 m6 used
00001C21  01                                       1209+          DC    HL1'1'             CC
00001C22  0B                                       1210+          DC    HL1'11'            CC failed mask
00001C24  00000000 00000000                        1211+          DS    2F                 extracted PSW after test (has CC)
00001C2C  FF                                       1212+          DC    X'FF'              extracted CC, if test failed
00001C2D  E5E2E3D9 E2404040                        1213+          DC    CL8'VSTRS'        instruction name
00001C38  00001CBC                                 1214+          DC    A(RE14+16)        address of v2 source
00001C3C  00001CCC                                 1215+          DC    A(RE14+32)        address of v3 source
00001C40  00001CDC                                 1216+          DC    A(RE14+48)        address of v4 source
00001C44  00000010                                 1217+          DC    A(16)             result length
00001C48  00001CAC                                 1218+REA14     DC    A(RE14)           result address
00001C50  00000000 00000000                        1219+          DS    FD                gap
00001C58  00000000 00000000                        1220+V1O14     DS    XL16              V1 output
00001C60  00000000 00000000
00001C68  00000000 00000000                        1221+          DS    FD                gap
                                                   1222+*
00001C70                                           1223+X14       DS    0F
00001C70  E310 5020 0014                 00000020  1224+          LGF   R1,V2ADDR         load v2 source
00001C76  E761 0000 0806                 00000000  1225+          VL    v22,0(R1)         use v22 to test decoder
00001C7C  E310 5024 0014                 00000024  1226+          LGF   R1,V3ADDR         load v3 source
00001C82  E771 0000 0806                 00000000  1227+          VL    v23,0(R1)         use v23 to test decoder
00001C88  E310 5028 0014                 00000028  1228+          LGF   R1,V4ADDR         load v4 source
00001C8E  E781 0000 0806                 00000000  1229+          VL    v24,0(R1)         use v24 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001C94  E766 7120 8F8B                         1230+         VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00001C9A  B98D 0020                              1231+         EPSW  R2,R0                 extract psw
00001C9E  5020 500C                   0000000C   1232+         ST    R2,CCPSW                 to save CC
00001CA2  E760 5040 080E              00001C58   1233+         VST   V22,V1O14             save v1 output
00001CA8  07FB                                   1234+         BR    R11                  return
00001CAC                                         1235+RE14     DC    0F                   xl16 expected result
00001CAC                                         1236+         DROP  R5
00001CAC  00000000 00000010                      1237          DC    XL16'0000000000000010 0000000000000000'   V1
00001CB4  00000000 00000000
00001CBC  01020000 05060708                      1238          DC    XL16'0102000005060708 090A0B0C0D0E0F10'   v2
00001CC4  090A0B0C 0D0E0F10
00001CCC  F0F1F2F3 F4F5F6F7                      1239          DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'   v3
00001CD4  F8F9FAFB FCFDFEFF
00001CDC  00000000 00000008                      1240          DC    XL16'0000000000000008 0000000000000000'   v4
00001CE4  00000000 00000000
                                                 1241
                                                 1242 *Word
                                                 1243          VRR_D VSTRS,2,2,1                               no match
00001CF0                                         1244+         DS    0FD
00001CF0                      00001CF0           1245+         USING *,R5                 base for test data and test routine
00001CF0  00001D48                               1246+T15      DC    A(X15)               address of test routine
00001CF4  000F                                   1247+         DC    H'15'                test number
00001CF6  00                                     1248+         DC    X'00'
00001CF7  02                                     1249+         DC    HL1'2'                    m5 used
00001CF8  02                                     1250+         DC    HL1'2'                    m6 used
00001CF9  01                                     1251+         DC    HL1'1'                CC
00001CFA  0B                                     1252+         DC    HL1'11'               CC failed mask
00001CFC  00000000 00000000                      1253+         DS    2F                    extracted PSW after test (has CC)
00001D04  FF                                     1254+         DC    X'FF'                 extracted CC, if test failed
00001D05  E5E2E3D9 E2404040                      1255+         DC    CL8'VSTRS'           instruction name
00001D10  00001D94                               1256+         DC    A(RE15+16)           address of v2 source
00001D14  00001DA4                               1257+         DC    A(RE15+32)           address of v3 source
00001D18  00001DB4                               1258+         DC    A(RE15+48)           address of v4 source
00001D1C  00000010                               1259+         DC    A(16)                result length
00001D20  00001D84                               1260+REA15    DC    A(RE15)              result address
00001D28  00000000 00000000                      1261+         DS    FD                   gap
00001D30  00000000 00000000                      1262+V1O15    DS    XL16                 V1 output
00001D38  00000000 00000000
00001D40  00000000 00000000                      1263+         DS    FD                   gap
                                                 1264+*
00001D48                                         1265+X15      DS    0F
00001D48  E310 5020 0014              00000020   1266+         LGF   R1,V2ADDR            load v2 source
00001D4E  E761 0000 0806              00000000   1267+         VL    v22,0(R1)            use v22 to test decoder
00001D54  E310 5024 0014              00000024   1268+         LGF   R1,V3ADDR            load v3 source
00001D5A  E771 0000 0806              00000000   1269+         VL    v23,0(R1)            use v23 to test decoder
00001D60  E310 5028 0014              00000028   1270+         LGF   R1,V4ADDR            load v4 source
00001D66  E781 0000 0806              00000000   1271+         VL    v24,0(R1)            use v24 to test decoder
00001D6C  E766 7220 8F8B                         1272+         VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00001D72  B98D 0020                              1273+         EPSW  R2,R0                 extract psw
00001D76  5020 500C                   0000000C   1274+         ST    R2,CCPSW                 to save CC
00001D7A  E760 5040 080E              00001D30   1275+         VST   V22,V1O15             save v1 output
00001D80  07FB                                   1276+         BR    R11                  return
00001D84                                         1277+RE15     DC    0F                   xl16 expected result
00001D84                                         1278+         DROP  R5
00001D84  00000000 00000010                      1279          DC    XL16'0000000000000010 0000000000000000'   V1
00001D8C  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001D94  01020304 00000000                        1280           DC    XL16'0102030400000000 090A0B0C0D0E0F10'   v2
00001D9C  090A0B0C 0D0E0F10
00001DA4  F0F1F2F3 F4F5F6F7                        1281           DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'   v3
00001DAC  F8F9FAFB FCFDFEFF
00001DB4  00000000 00000008                        1282           DC    XL16'0000000000000008 0000000000000000'   v4
00001DBC  00000000 00000000
                                                   1283
                                                   1284 *Full Match  ZS=1 CC=2
                                                   1285 *Byte
                                                   1286           VRR_D VSTRS,0,2,2                               full match
00001DC8                                           1287+          DS    0FD
00001DC8                     00001DC8              1288+          USING *,R5              base for test data and test routine
00001DC8  00001E20                                 1289+T16       DC    A(X16)            address of test routine
00001DCC  0010                                     1290+          DC    H'16'             test number
00001DCE  00                                       1291+          DC    X'00'
00001DCF  00                                       1292+          DC    HL1'0'                 m5 used
00001DD0  02                                       1293+          DC    HL1'2'                 m6 used
00001DD1  02                                       1294+          DC    HL1'2'             CC
00001DD2  0D                                       1295+          DC    HL1'13'            CC failed mask
00001DD4  00000000 00000000                        1296+          DS    2F                 extracted PSW after test (has CC)
00001DDC  FF                                       1297+          DC    X'FF'              extracted CC, if test failed
00001DDD  E5E2E3D9 E2404040                        1298+          DC    CL8'VSTRS'        instruction name
00001DE8  00001E6C                                 1299+          DC    A(RE16+16)        address of v2 source
00001DEC  00001E7C                                 1300+          DC    A(RE16+32)        address of v3 source
00001DF0  00001E8C                                 1301+          DC    A(RE16+48)        address of v4 source
00001DF4  00000010                                 1302+          DC    A(16)             result length
00001DF8  00001E5C                                 1303+REA16     DC    A(RE16)           result address
00001E00  00000000 00000000                        1304+          DS    FD                gap
00001E08  00000000 00000000                        1305+V1O16     DS    XL16              V1 output
00001E10  00000000 00000000
00001E18  00000000 00000000                        1306+          DS    FD                gap
                                                   1307+*
00001E20                                           1308+X16       DS    0F
00001E20  E310 5020 0014                 00000020  1309+          LGF   R1,V2ADDR         load v2 source
00001E26  E761 0000 0806                 00000000  1310+          VL    v22,0(R1)         use v22 to test decoder
00001E2C  E310 5024 0014                 00000024  1311+          LGF   R1,V3ADDR         load v3 source
00001E32  E771 0000 0806                 00000000  1312+          VL    v23,0(R1)         use v23 to test decoder
00001E38  E310 5028 0014                 00000028  1313+          LGF   R1,V4ADDR         load v4 source
00001E3E  E781 0000 0806                 00000000  1314+          VL    v24,0(R1)         use v24 to test decoder
00001E44  E766 7020 8F8B                           1315+          VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00001E4A  B98D 0020                                1316+          EPSW  R2,R0              extract psw
00001E4E  5020 500C                      0000000C  1317+          ST    R2,CCPSW              to save CC
00001E52  E760 5040 080E                 00001E08  1318+          VST   V22,V1O16          save v1 output
00001E58  07FB                                     1319+          BR    R11               return
00001E5C                                           1320+RE16      DC    0F                xl16 expected result
00001E5C                                           1321+          DROP  R5
00001E5C  00000000 00000008                        1322           DC    XL16'0000000000000008 0000000000000000'   V1
00001E64  00000000 00000000
00001E6C  F0F1F2F3 F4F5F6F7                        1323           DC    XL16'F0F1F2F3F4F5F6F7 01020304AAFDFEFF'   v2
00001E74  01020304 AAFDFEFF
00001E7C  01020304 05060708                        1324           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00001E84  090A0B0C 0D0E0F10
00001E8C  00000000 00000004                        1325           DC    XL16'0000000000000004 0000000000000000'   v4
00001E94  00000000 00000000
                                                   1326
                                                   1327 *Halfword
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                         1328          VRR_D VSTRS,1,2,2                              full match
00001EA0                                 1329+         DS    0FD
00001EA0                      00001EA0   1330+         USING *,R5              base for test data and test routine
00001EA0  00001EF8                       1331+T17      DC    A(X17)            address of test routine
00001EA4  0011                           1332+         DC    H'17'             test number
00001EA6  00                             1333+         DC    X'00'
00001EA7  01                             1334+         DC    HL1'1'                  m5 used
00001EA8  02                             1335+         DC    HL1'2'                  m6 used
00001EA9  02                             1336+         DC    HL1'2'             CC
00001EAA  0D                             1337+         DC    HL1'13'            CC failed mask
00001EAC  00000000 00000000              1338+         DS    2F                 extracted PSW after test (has CC)
00001EB4  FF                             1339+         DC    X'FF'              extracted CC, if test failed
00001EB5  E5E2E3D9 E2404040              1340+         DC    CL8'VSTRS'        instruction name
00001EC0  00001F44                       1341+         DC    A(RE17+16)        address of v2 source
00001EC4  00001F54                       1342+         DC    A(RE17+32)        address of v3 source
00001EC8  00001F64                       1343+         DC    A(RE17+48)        address of v4 source
00001ECC  00000010                       1344+         DC    A(16)             result length
00001ED0  00001F34                       1345+REA17    DC    A(RE17)           result address
00001ED8  00000000 00000000              1346+         DS    FD                gap
00001EE0  00000000 00000000              1347+V1O17    DS    XL16              V1 output
00001EE8  00000000 00000000
00001EF0  00000000 00000000              1348+         DS    FD                gap
                                         1349+*
00001EF8                                 1350+X17      DS    0F
00001EF8  E310 5020 0014       00000020  1351+         LGF   R1,V2ADDR         load v2 source
00001EFE  E761 0000 0806       00000000  1352+         VL    v22,0(R1)         use v22 to test decoder
00001F04  E310 5024 0014       00000024  1353+         LGF   R1,V3ADDR         load v3 source
00001F0A  E771 0000 0806       00000000  1354+         VL    v23,0(R1)         use v23 to test decoder
00001F10  E310 5028 0014       00000028  1355+         LGF   R1,V4ADDR         load v4 source
00001F16  E781 0000 0806       00000000  1356+         VL    v24,0(R1)         use v24 to test decoder
00001F1C  E766 7120 8F8B                 1357+         VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00001F22  B98D 0020                      1358+         EPSW  R2,R0              extract psw
00001F26  5020 500C            0000000C  1359+         ST    R2,CCPSW              to save CC
00001F2A  E760 5040 080E       00001EE0  1360+         VST   V22,V1O17          save v1 output
00001F30  07FB                           1361+         BR    R11               return
00001F34                                 1362+RE17     DC    0F                xl16 expected result
00001F34                                 1363+         DROP  R5
00001F34  00000000 00000008              1364          DC    XL16'0000000000000008 0000000000000000'   V1
00001F3C  00000000 00000000
00001F44  F0F1F2F3 F4F5F6F7              1365          DC    XL16'F0F1F2F3F4F5F6F7 01020304AAFDFEFF'   v2
00001F4C  01020304 AAFDFEFF
00001F54  01020304 05060708              1366          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00001F5C  090A0B0C 0D0E0F10
00001F64  00000000 00000004              1367          DC    XL16'0000000000000004 0000000000000000'   v4
00001F6C  00000000 00000000
                                         1368
                                         1369 *Word
                                         1370          VRR_D VSTRS,2,2,2                              full match
00001F78                                 1371+         DS    0FD
00001F78                      00001F78   1372+         USING *,R5              base for test data and test routine
00001F78  00001FD0                       1373+T18      DC    A(X18)            address of test routine
00001F7C  0012                           1374+         DC    H'18'             test number
00001F7E  00                             1375+         DC    X'00'
00001F7F  02                             1376+         DC    HL1'2'                  m5 used
00001F80  02                             1377+         DC    HL1'2'                  m6 used
00001F81  02                             1378+         DC    HL1'2'             CC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001F82  0D                                     1379+          DC    HL1'13'            CC failed mask
00001F84  00000000 00000000                      1380+          DS    2F                 extracted PSW after test (has CC)
00001F8C  FF                                     1381+          DC    X'FF'              extracted CC, if test failed
00001F8D  E5E2E3D9 E2404040                      1382+          DC    CL8'VSTRS'        instruction name
00001F98  0000201C                               1383+          DC    A(RE18+16)        address of v2 source
00001F9C  0000202C                               1384+          DC    A(RE18+32)        address of v3 source
00001FA0  0000203C                               1385+          DC    A(RE18+48)        address of v4 source
00001FA4  00000010                               1386+          DC    A(16)             result length
00001FA8  0000200C                               1387+REA18     DC    A(RE18)           result address
00001FB0  00000000 00000000                      1388+          DS    FD                gap
00001FB8  00000000 00000000                      1389+V1O18     DS    XL16              V1 output
00001FC0  00000000 00000000
00001FC8  00000000 00000000                      1390+          DS    FD                gap
                                                 1391+*
00001FD0                                         1392+X18       DS    0F
00001FD0  E310 5020 0014                00000020 1393+          LGF   R1,V2ADDR         load v2 source
00001FD6  E761 0000 0806                00000000 1394+          VL    v22,0(R1)         use v22 to test decoder
00001FDC  E310 5024 0014                00000024 1395+          LGF   R1,V3ADDR         load v3 source
00001FE2  E771 0000 0806                00000000 1396+          VL    v23,0(R1)         use v23 to test decoder
00001FE8  E310 5028 0014                00000028 1397+          LGF   R1,V4ADDR         load v4 source
00001FEE  E781 0000 0806                00000000 1398+          VL    v24,0(R1)         use v24 to test decoder
00001FF4  E766 7220 8F8B                         1399+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00001FFA  B98D 0020                              1400+          EPSW  R2,R0              extract psw
00001FFE  5020 500C                0000000C      1401+          ST    R2,CCPSW              to save CC
00002002  E760 5040 080E                00001FB8 1402+          VST   V22,V1O18          save v1 output
00002008  07FB                                   1403+          BR    R11               return
0000200C                                         1404+RE18      DC    0F                xl16 expected result
0000200C                                         1405+          DROP  R5
0000200C  00000000 00000008                      1406           DC    XL16'0000000000000008 0000000000000000'   V1
00002014  00000000 00000000
0000201C  F0F1F2F3 F4F5F6F7                      1407           DC    XL16'F0F1F2F3F4F5F6F7 0102030405AAAAFF'   v2
00002024  01020304 05AAAAFF
0000202C  01020304 05060708                      1408           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002034  090A0B0C 0D0E0F10
0000203C  00000000 00000004                      1409           DC    XL16'0000000000000004 0000000000000000'   v4
00002044  00000000 00000000
                                                 1410
                                                 1411 *Partial Match  ZS=1 CC=3
                                                 1412 *Byte
                                                 1413           VRR_D VSTRS,0,2,3                               partial match
00002050                                         1414+          DS    0FD
00002050                        00002050         1415+          USING *,R5              base for test data and test routine
00002050  000020A8                               1416+T19       DC    A(X19)            address of test routine
00002054  0013                                   1417+          DC    H'19'             test number
00002056  00                                     1418+          DC    X'00'
00002057  00                                     1419+          DC    HL1'0'                 m5 used
00002058  02                                     1420+          DC    HL1'2'                 m6 used
00002059  03                                     1421+          DC    HL1'3'             CC
0000205A  0E                                     1422+          DC    HL1'14'            CC failed mask
0000205C  00000000 00000000                      1423+          DS    2F                 extracted PSW after test (has CC)
00002064  FF                                     1424+          DC    X'FF'              extracted CC, if test failed
00002065  E5E2E3D9 E2404040                      1425+          DC    CL8'VSTRS'        instruction name
00002070  000020F4                               1426+          DC    A(RE19+16)        address of v2 source
00002074  00002104                               1427+          DC    A(RE19+32)        address of v3 source
00002078  00002114                               1428+          DC    A(RE19+48)        address of v4 source
0000207C  00000010                               1429+          DC    A(16)             result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002080  000020E4                          1430+REA19    DC    A(RE19)           result address
00002088  00000000 00000000                 1431+         DS    FD                gap
00002090  00000000 00000000                 1432+V1O19    DS    XL16              V1 output
00002098  00000000 00000000
000020A0  00000000 00000000                 1433+         DS    FD                gap
                                            1434+*
000020A8                                    1435+X19      DS    0F
000020A8  E310 5020 0014                00000020 1436+         LGF   R1,V2ADDR         load v2 source
000020AE  E761 0000 0806                00000000 1437+         VL    v22,0(R1)         use v22 to test decoder
000020B4  E310 5024 0014                00000024 1438+         LGF   R1,V3ADDR         load v3 source
000020BA  E771 0000 0806                00000000 1439+         VL    v23,0(R1)         use v23 to test decoder
000020C0  E310 5028 0014                00000028 1440+         LGF   R1,V4ADDR         load v4 source
000020C6  E781 0000 0806                00000000 1441+         VL    v24,0(R1)         use v24 to test decoder
000020CC  E766 7020 8F8B                         1442+         VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
000020D2  B98D 0020                              1443+         EPSW  R2,R0              extract psw
000020D6  5020 500C                     0000000C 1444+         ST    R2,CCPSW              to save CC
000020DA  E760 5040 080E                00002090 1445+         VST   V22,V1O19          save v1 output
000020E0  07FB                                   1446+         BR    R11               return
000020E4                                         1447+RE19     DC    0F                xl16 expected result
000020E4                                         1448+         DROP  R5
000020E4  00000000 0000000D                      1449          DC    XL16'000000000000000D 0000000000000000'   V1
000020EC  00000000 00000000
000020F4  F0F1F2F3 F4F5F6F7                      1450          DC    XL16'F0F1F2F3F4F5F6F7 AAAAFDFEFF010203'   v2
000020FC  AAAAFDFE FF010203
00002104  01020304 05060708                      1451          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
0000210C  090A0B0C 0D0E0F10
00002114  00000000 00000004                      1452          DC    XL16'0000000000000004 0000000000000000'   v4
0000211C  00000000 00000000
                                                 1453
                                                 1454 *Halfword
                                                 1455          VRR_D VSTRS,1,2,3                               partial match
00002128                                         1456+         DS    0FD
00002128                        00002128         1457+         USING *,R5              base for test data and test routine
00002128  00002180                               1458+T20      DC    A(X20)            address of test routine
0000212C  0014                                   1459+         DC    H'20'             test number
0000212E  00                                     1460+         DC    X'00'
0000212F  01                                     1461+         DC    HL1'1'                  m5 used
00002130  02                                     1462+         DC    HL1'2'                  m6 used
00002131  03                                     1463+         DC    HL1'3'             CC
00002132  0E                                     1464+         DC    HL1'14'            CC failed mask
00002134  00000000 00000000                      1465+         DS    2F                 extracted PSW after test (has CC)
0000213C  FF                                     1466+         DC    X'FF'              extracted CC, if test failed
0000213D  E5E2E3D9 E2404040                      1467+         DC    CL8'VSTRS'        instruction name
00002148  000021CC                               1468+         DC    A(RE20+16)        address of v2 source
0000214C  000021DC                               1469+         DC    A(RE20+32)        address of v3 source
00002150  000021EC                               1470+         DC    A(RE20+48)        address of v4 source
00002154  00000010                               1471+         DC    A(16)             result length
00002158  000021BC                               1472+REA20    DC    A(RE20)           result address
00002160  00000000 00000000                      1473+         DS    FD                gap
00002168  00000000 00000000                      1474+V1O20    DS    XL16              V1 output
00002170  00000000 00000000
00002178  00000000 00000000                      1475+         DS    FD                gap
                                                 1476+*
00002180                                         1477+X20      DS    0F
00002180  E310 5020 0014                00000020 1478+         LGF   R1,V2ADDR         load v2 source
00002186  E761 0000 0806                00000000 1479+         VL    v22,0(R1)         use v22 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000218C  E310 5024 0014                 00000024  1480+          LGF    R1,V3ADDR          load v3 source
00002192  E771 0000 0806                 00000000  1481+          VL     v23,0(R1)          use v23 to test decoder
00002198  E310 5028 0014                 00000028  1482+          LGF    R1,V4ADDR          load v4 source
0000219E  E781 0000 0806                 00000000  1483+          VL     v24,0(R1)          use v24 to test decoder
000021A4  E766 7120 8F8B                           1484+          VSTRS  V22,V22,V23,V24,1,2      instruction (dest is a source)
000021AA  B98D 0020                                1485+          EPSW   R2,R0               extract psw
000021AE  5020 500C                      0000000C  1486+          ST     R2,CCPSW               to save CC
000021B2  E760 5040 080E                 00002168  1487+          VST    V22,V1O20           save v1 output
000021B8  07FB                                     1488+          BR     R11                return
000021BC                                           1489+RE20      DC     0F                 xl16 expected result
000021BC                                           1490+          DROP   R5
000021BC  00000000 0000000A                        1491           DC     XL16'000000000000000A 0000000000000000'   V1
000021C4  00000000 00000000
000021CC  F0F1F2F3 F4F5F6F7                        1492           DC     XL16'F0F1F2F3F4F5F6F7 AAFF010203040506'   v2
000021D4  AAFF0102 03040506
000021DC  01020304 05060708                        1493           DC     XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000021E4  090A0B0C 0D0E0F10
000021EC  00000000 00000008                        1494           DC     XL16'0000000000000008 0000000000000000'   v4
000021F4  00000000 00000000
                                                   1495
                                                   1496 *Word
                                                   1497           VRR_D  VSTRS,2,2,3                               partial match
00002200                                           1498+          DS     0FD
00002200                         00002200          1499+          USING  *,R5               base for test data and test routine
00002200  00002258                                 1500+T21       DC     A(X21)             address of test routine
00002204  0015                                     1501+          DC     H'21'              test number
00002206  00                                       1502+          DC     X'00'
00002207  02                                       1503+          DC     HL1'2'                  m5 used
00002208  02                                       1504+          DC     HL1'2'                  m6 used
00002209  03                                       1505+          DC     HL1'3'             CC
0000220A  0E                                       1506+          DC     HL1'14'            CC failed mask
0000220C  00000000 00000000                        1507+          DS     2F                 extracted PSW after test (has CC)
00002214  FF                                       1508+          DC     X'FF'              extracted CC, if test failed
00002215  E5E2E3D9 E2404040                        1509+          DC     CL8'VSTRS'         instruction name
00002220  000022A4                                 1510+          DC     A(RE21+16)         address of v2 source
00002224  000022B4                                 1511+          DC     A(RE21+32)         address of v3 source
00002228  000022C4                                 1512+          DC     A(RE21+48)         address of v4 source
0000222C  00000010                                 1513+          DC     A(16)              result length
00002230  00002294                                 1514+REA21     DC     A(RE21)            result address
00002238  00000000 00000000                        1515+          DS     FD                 gap
00002240  00000000 00000000                        1516+V1O21     DS     XL16               V1 output
00002248  00000000 00000000
00002250  00000000 00000000                        1517+          DS     FD                 gap
                                                   1518+*
00002258                                           1519+X21       DS     0F
00002258  E310 5020 0014                 00000020  1520+          LGF    R1,V2ADDR          load v2 source
0000225E  E761 0000 0806                 00000000  1521+          VL     v22,0(R1)          use v22 to test decoder
00002264  E310 5024 0014                 00000024  1522+          LGF    R1,V3ADDR          load v3 source
0000226A  E771 0000 0806                 00000000  1523+          VL     v23,0(R1)          use v23 to test decoder
00002270  E310 5028 0014                 00000028  1524+          LGF    R1,V4ADDR          load v4 source
00002276  E781 0000 0806                 00000000  1525+          VL     v24,0(R1)          use v24 to test decoder
0000227C  E766 7220 8F8B                           1526+          VSTRS  V22,V22,V23,V24,2,2      instruction (dest is a source)
00002282  B98D 0020                                1527+          EPSW   R2,R0               extract psw
00002286  5020 500C                      0000000C  1528+          ST     R2,CCPSW               to save CC
0000228A  E760 A040 080E                 00002240  1529+          VST    V22,V1O21           save v1 output
00002290  07FB                                     1530+          BR     R11                return
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00002294                                            1531+RE21     DC    0F                xl16 expected result
00002294                                            1532+         DROP  R5
00002294  00000000 00000008                         1533          DC    XL16'0000000000000008 0000000000000000'   V1
0000229C  00000000 00000000
000022A4  F0F1F2F3 F4F5F6F7                         1534          DC    XL16'F0F1F2F3F4F5F6F7 0102030405060708'   v2
000022AC  01020304 05060708
000022B4  01020304 05060708                         1535          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000022BC  090A0B0C 0D0E0F10
000022C4  00000000 0000000C                         1536          DC    XL16'000000000000000C 0000000000000000'   v4
000022CC  00000000 00000000
                                                    1537
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1539 *-------------------------------------------------------------------
                                                   1540 * case 2 - full match tests: ZS=1 CC=2
                                                   1541 *-------------------------------------------------------------------
                                                   1542 *Full Match: at beginning of vector
                                                   1543 *Byte
                                                   1544           VRR_D VSTRS,0,2,2                              full match
000022D8                                           1545+          DS    0FD
000022D8                          000022D8         1546+          USING *,R5              base for test data and test routine
000022D8  00002330                                 1547+T22       DC    A(X22)            address of test routine
000022DC  0016                                     1548+          DC    H'22'             test number
000022DE  00                                       1549+          DC    X'00'
000022DF  00                                       1550+          DC    HL1'0'                  m5 used
000022E0  02                                       1551+          DC    HL1'2'                  m6 used
000022E1  02                                       1552+          DC    HL1'2'             CC
000022E2  0D                                       1553+          DC    HL1'13'            CC failed mask
000022E4  00000000 00000000                        1554+          DS    2F                 extracted PSW after test (has CC)
000022EC  FF                                       1555+          DC    X'FF'              extracted CC, if test failed
000022ED  E5E2E3D9 E2404040                        1556+          DC    CL8'VSTRS'        instruction name
000022F8  0000237C                                 1557+          DC    A(RE22+16)        address of v2 source
000022FC  0000238C                                 1558+          DC    A(RE22+32)        address of v3 source
00002300  0000239C                                 1559+          DC    A(RE22+48)        address of v4 source
00002304  00000010                                 1560+          DC    A(16)             result length
00002308  0000236C                                 1561+REA22     DC    A(RE22)           result address
00002310  00000000 00000000                        1562+          DS    FD                gap
00002318  00000000 00000000                        1563+V1O22     DS    XL16              V1 output
00002320  00000000 00000000
00002328  00000000 00000000                        1564+          DS    FD                gap
                                                   1565+*
00002330                                           1566+X22       DS    0F
00002330  E310 5020 0014                 00000020  1567+          LGF   R1,V2ADDR         load v2 source
00002336  E761 0000 0806                 00000000  1568+          VL    v22,0(R1)         use v22 to test decoder
0000233C  E310 5024 0014                 00000024  1569+          LGF   R1,V3ADDR         load v3 source
00002342  E771 0000 0806                 00000000  1570+          VL    v23,0(R1)         use v23 to test decoder
00002348  E310 5028 0014                 00000028  1571+          LGF   R1,V4ADDR         load v4 source
0000234E  E781 0000 0806                 00000000  1572+          VL    v24,0(R1)         use v24 to test decoder
00002354  E766 7020 8F8B                           1573+          VSTRS V22,V22,V23,V24,0,2     instruction (dest is a source)
0000235A  B98D 0020                                1574+          EPSW  R2,R0              extract psw
0000235E  5020 500C                      0000000C  1575+          ST    R2,CCPSW              to save CC
00002362  E760 5040 080E                 00002318  1576+          VST   V22,V1O22          save v1 output
00002368  07FB                                     1577+          BR    R11               return
0000236C                                           1578+RE22      DC    0F                xl16 expected result
0000236C                                           1579+          DROP  R5
0000236C  00000000 00000000                        1580           DC    XL16'0000000000000000 0000000000000000'   V1
00002374  00000000 00000000
0000237C  01020304 F4F5F6F7                        1581           DC    XL16'01020304F4F5F6F7 01020304AAFDFEFF'   v2
00002384  01020304 AAFDFEFF
0000238C  01020304 05060708                        1582           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002394  090A0B0C 0D0E0F10
0000239C  00000000 00000004                        1583           DC    XL16'0000000000000004 0000000000000000'   v4
000023A4  00000000 00000000
                                                   1584
                                                   1585 *Halfword
                                                   1586           VRR_D VSTRS,1,2,2                              full match
000023B0                                           1587+          DS    0FD
000023B0                          000023B0         1588+          USING *,R5              base for test data and test routine
000023B0  00002408                                 1589+T23       DC    A(X23)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000023B4  0017                                    1590+          DC    H'23'              test number
000023B6  00                                      1591+          DC    X'00'
000023B7  01                                      1592+          DC    HL1'1'                   m5 used
000023B8  02                                      1593+          DC    HL1'2'                   m6 used
000023B9  02                                      1594+          DC    HL1'2'              CC
000023BA  0D                                      1595+          DC    HL1'13'             CC failed mask
000023BC  00000000 00000000                       1596+          DS    2F                  extracted PSW after test (has CC)
000023C4  FF                                      1597+          DC    X'FF'               extracted CC, if test failed
000023C5  E5E2E3D9 E2404040                       1598+          DC    CL8'VSTRS'         instruction name
000023D0  00002454                                1599+          DC    A(RE23+16)         address of v2 source
000023D4  00002464                                1600+          DC    A(RE23+32)         address of v3 source
000023D8  00002474                                1601+          DC    A(RE23+48)         address of v4 source
000023DC  00000010                                1602+          DC    A(16)              result length
000023E0  00002444                                1603+REA23     DC    A(RE23)            result address
000023E8  00000000 00000000                       1604+          DS    FD                 gap
000023F0  00000000 00000000                       1605+V1O23     DS    XL16               V1 output
000023F8  00000000 00000000
00002400  00000000 00000000                       1606+          DS    FD                 gap
                                                  1607+*
00002408                                          1608+X23       DS    0F
00002408  E310 5020 0014                 00000020 1609+          LGF   R1,V2ADDR          load v2 source
0000240E  E761 0000 0806                 00000000 1610+          VL    v22,0(R1)          use v22 to test decoder
00002414  E310 5024 0014                 00000024 1611+          LGF   R1,V3ADDR          load v3 source
0000241A  E771 0000 0806                 00000000 1612+          VL    v23,0(R1)          use v23 to test decoder
00002420  E310 5028 0014                 00000028 1613+          LGF   R1,V4ADDR          load v4 source
00002426  E781 0000 0806                 00000000 1614+          VL    v24,0(R1)          use v24 to test decoder
0000242C  E766 7120 8F8B                          1615+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00002432  B98D 0020                               1616+          EPSW  R2,R0               extract psw
00002436  5020 500C                      0000000C 1617+          ST    R2,CCPSW               to save CC
0000243A  E760 5040 080E                 000023F0 1618+          VST   V22,V1O23           save v1 output
00002440  07FB                                    1619+          BR    R11                return
00002444                                          1620+RE23      DC    0F                 xl16 expected result
00002444                                          1621+          DROP  R5
00002444  00000000 00000000                       1622           DC    XL16'0000000000000000 0000000000000000'   V1
0000244C  00000000 00000000
00002454  01020304 F4F5F6F7                       1623           DC    XL16'01020304F4F5F6F7 01020304AAFDFEFF'   v2
0000245C  01020304 AAFDFEFF
00002464  01020304 05060708                       1624           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
0000246C  090A0B0C 0D0E0F10
00002474  00000000 00000004                       1625           DC    XL16'0000000000000004 0000000000000000'   v4
0000247C  00000000 00000000
                                                  1626
                                                  1627 *Word
                                                  1628           VRR_D VSTRS,2,2,2                               full match
00002488                                          1629+          DS    0FD
00002488                 00002488                 1630+          USING *,R5               base for test data and test routine
00002488  000024E0                                1631+T24       DC    A(X24)             address of test routine
0000248C  0018                                    1632+          DC    H'24'              test number
0000248E  00                                      1633+          DC    X'00'
0000248F  02                                      1634+          DC    HL1'2'                   m5 used
00002490  02                                      1635+          DC    HL1'2'                   m6 used
00002491  02                                      1636+          DC    HL1'2'              CC
00002492  0D                                      1637+          DC    HL1'13'             CC failed mask
00002494  00000000 00000000                       1638+          DS    2F                  extracted PSW after test (has CC)
0000249C  FF                                      1639+          DC    X'FF'               extracted CC, if test failed
0000249D  E5E2E3D9 E2404040                       1640+          DC    CL8'VSTRS'         instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000024A8  0000252C                             1641+          DC    A(RE24+16)        address of v2 source
000024AC  0000253C                             1642+          DC    A(RE24+32)        address of v3 source
000024B0  0000254C                             1643+          DC    A(RE24+48)        address of v4 source
000024B4  00000010                             1644+          DC    A(16)             result length
000024B8  0000251C                             1645+REA24     DC    A(RE24)           result address
000024C0  00000000 00000000                    1646+          DS    FD                gap
000024C8  00000000 00000000                    1647+V1O24     DS    XL16              V1 output
000024D0  00000000 00000000
000024D8  00000000 00000000                    1648+          DS    FD                gap
                                               1649+*
000024E0                                       1650+X24       DS    0F
000024E0  E310 5020 0014              00000020 1651+          LGF   R1,V2ADDR         load v2 source
000024E6  E761 0000 0806              00000000 1652+          VL    v22,0(R1)         use v22 to test decoder
000024EC  E310 5024 0014              00000024 1653+          LGF   R1,V3ADDR         load v3 source
000024F2  E771 0000 0806              00000000 1654+          VL    v23,0(R1)         use v23 to test decoder
000024F8  E310 5028 0014              00000028 1655+          LGF   R1,V4ADDR         load v4 source
000024FE  E781 0000 0806              00000000 1656+          VL    v24,0(R1)         use v24 to test decoder
00002504  E766 7220 8F8B                       1657+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
0000250A  B98D 0020                            1658+          EPSW  R2,R0              extract psw
0000250E  5020 500C                   0000000C 1659+          ST    R2,CCPSW              to save CC
00002512  E760 5040 080E              000024C8 1660+          VST   V22,V1O24          save v1 output
00002518  07FB                                 1661+          BR    R11               return
0000251C                                       1662+RE24      DC    0F                xl16 expected result
0000251C                                       1663+          DROP  R5
0000251C  00000000 00000000                    1664           DC    XL16'0000000000000000 0000000000000000'   V1
00002524  00000000 00000000
0000252C  01020304 F4F5F6F7                    1665           DC    XL16'01020304F4F5F6F7 0102030405AAAAFF'   v2
00002534  01020304 05AAAAFF
0000253C  01020304 05060708                    1666           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002544  090A0B0C 0D0E0F10
0000254C  00000000 00000004                    1667           DC    XL16'0000000000000004 0000000000000000'   v4
00002554  00000000 00000000
                                               1668
                                               1669 *Full Match: at end of vector
                                               1670 *Byte
                                               1671           VRR_D VSTRS,0,2,2                               full match
00002560                                       1672+          DS    0FD
00002560                        00002560       1673+          USING *,R5              base for test data and test routine
00002560  000025B8                             1674+T25       DC    A(X25)            address of test routine
00002564  0019                                 1675+          DC    H'25'             test number
00002566  00                                   1676+          DC    X'00'
00002567  00                                   1677+          DC    HL1'0'                  m5 used
00002568  02                                   1678+          DC    HL1'2'                  m6 used
00002569  02                                   1679+          DC    HL1'2'             CC
0000256A  0D                                   1680+          DC    HL1'13'            CC failed mask
0000256C  00000000 00000000                    1681+          DS    2F                 extracted PSW after test (has CC)
00002574  FF                                   1682+          DC    X'FF'              extracted CC, if test failed
00002575  E5E2E3D9 E2404040                    1683+          DC    CL8'VSTRS'        instruction name
00002580  00002604                             1684+          DC    A(RE25+16)        address of v2 source
00002584  00002614                             1685+          DC    A(RE25+32)        address of v3 source
00002588  00002624                             1686+          DC    A(RE25+48)        address of v4 source
0000258C  00000010                             1687+          DC    A(16)             result length
00002590  000025F4                             1688+REA25     DC    A(RE25)           result address
00002598  00000000 00000000                    1689+          DS    FD                gap
000025A0  00000000 00000000                    1690+V1O25     DS    XL16              V1 output
000025A8  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000025B0  00000000 00000000                        1691+          DS    FD                gap
                                                   1692+*
000025B8                                           1693+X25       DS    0F
000025B8  E310 5020 0014                 00000020  1694+          LGF   R1,V2ADDR         load v2 source
000025BE  E761 0000 0806                 00000000  1695+          VL    v22,0(R1)         use v22 to test decoder
000025C4  E310 5024 0014                 00000024  1696+          LGF   R1,V3ADDR         load v3 source
000025CA  E771 0000 0806                 00000000  1697+          VL    v23,0(R1)         use v23 to test decoder
000025D0  E310 5028 0014                 00000028  1698+          LGF   R1,V4ADDR         load v4 source
000025D6  E781 0000 0806                 00000000  1699+          VL    v24,0(R1)         use v24 to test decoder
000025DC  E766 7020 8F8B                           1700+          VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
000025E2  B98D 0020                                1701+          EPSW  R2,R0              extract psw
000025E6  5020 500C                      0000000C  1702+          ST    R2,CCPSW              to save CC
000025EA  E760 5040 080E                 000025A0  1703+          VST   V22,V1O25          save v1 output
000025F0  07FB                                     1704+          BR    R11               return
000025F4                                           1705+RE25      DC    0F                xl16 expected result
000025F4                                           1706+          DROP  R5
000025F4  00000000 0000000C                        1707           DC    XL16'000000000000000C 0000000000000000'   V1
000025FC  00000000 00000000
00002604  F0F1F2F3 F4F5F6F7                        1708           DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFB01020304'   v2
0000260C  F8F9FAFB 01020304
00002614  01020304 05060708                        1709           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
0000261C  090A0B0C 0D0E0F10
00002624  00000000 00000004                        1710           DC    XL16'0000000000000004 0000000000000000'   v4
0000262C  00000000 00000000
                                                   1711
                                                   1712 *Halfword
                                                   1713           VRR_D VSTRS,1,2,2                                full match
00002638                                           1714+          DS    0FD
00002638                         00002638          1715+          USING *,R5              base for test data and test routine
00002638  00002690                                 1716+T26       DC    A(X26)            address of test routine
0000263C  001A                                     1717+          DC    H'26'             test number
0000263E  00                                       1718+          DC    X'00'
0000263F  01                                       1719+          DC    HL1'1'                 m5 used
00002640  02                                       1720+          DC    HL1'2'                 m6 used
00002641  02                                       1721+          DC    HL1'2'             CC
00002642  0D                                       1722+          DC    HL1'13'            CC failed mask
00002644  00000000 00000000                        1723+          DS    2F                 extracted PSW after test (has CC)
0000264C  FF                                       1724+          DC    X'FF'              extracted CC, if test failed
0000264D  E5E2E3D9 E2404040                        1725+          DC    CL8'VSTRS'        instruction name
00002658  000026DC                                 1726+          DC    A(RE26+16)        address of v2 source
0000265C  000026EC                                 1727+          DC    A(RE26+32)        address of v3 source
00002660  000026FC                                 1728+          DC    A(RE26+48)        address of v4 source
00002664  00000010                                 1729+          DC    A(16)             result length
00002668  000026CC                                 1730+REA26     DC    A(RE26)           result address
00002670  00000000 00000000                        1731+          DS    FD                gap
00002678  00000000 00000000                        1732+V1O26     DS    XL16              V1 output
00002680  00000000 00000000
00002688  00000000 00000000                        1733+          DS    FD                gap
                                                   1734+*
00002690                                           1735+X26       DS    0F
00002690  E310 5020 0014                 00000020  1736+          LGF   R1,V2ADDR         load v2 source
00002696  E761 0000 0806                 00000000  1737+          VL    v22,0(R1)         use v22 to test decoder
0000269C  E310 5024 0014                 00000024  1738+          LGF   R1,V3ADDR         load v3 source
000026A2  E771 0000 0806                 00000000  1739+          VL    v23,0(R1)         use v23 to test decoder
000026A8  E310 5028 0014                 00000028  1740+          LGF   R1,V4ADDR         load v4 source
000026AE  E781 0000 0806                 00000000  1741+          VL    v24,0(R1)         use v24 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000026B4  E766 7120 8F8B                         1742+         VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
000026BA  B98D 0020                              1743+         EPSW  R2,R0                 extract psw
000026BE  5020 500C                0000000C      1744+         ST    R2,CCPSW                 to save CC
000026C2  E760 5040 080E           00002678      1745+         VST   V22,V1O26             save v1 output
000026C8  07FB                                   1746+         BR    R11                  return
000026CC                                         1747+RE26     DC    0F                   xl16 expected result
000026CC                                         1748+         DROP  R5
000026CC  00000000 0000000C                      1749          DC    XL16'000000000000000C 0000000000000000'   V1
000026D4  00000000 00000000
000026DC  F0F1F2F3 F4F5F6F7                      1750          DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFB01020304'   v2
000026E4  F8F9FAFB 01020304
000026EC  01020304 05060708                      1751          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000026F4  090A0B0C 0D0E0F10
000026FC  00000000 00000004                      1752          DC    XL16'0000000000000004 0000000000000000'   v4
00002704  00000000 00000000
                                                 1753
                                                 1754 *Word
                                                 1755          VRR_D VSTRS,2,2,2                               full match
00002710                                         1756+         DS    0FD
00002710                      00002710           1757+         USING *,R5                base for test data and test routine
00002710  00002768                               1758+T27      DC    A(X27)              address of test routine
00002714  001B                                   1759+         DC    H'27'               test number
00002716  00                                     1760+         DC    X'00'
00002717  02                                     1761+         DC    HL1'2'                   m5 used
00002718  02                                     1762+         DC    HL1'2'                   m6 used
00002719  02                                     1763+         DC    HL1'2'                CC
0000271A  0D                                     1764+         DC    HL1'13'               CC failed mask
0000271C  00000000 00000000                      1765+         DS    2F                    extracted PSW after test (has CC)
00002724  FF                                     1766+         DC    X'FF'                 extracted CC, if test failed
00002725  E5E2E3D9 E2404040                      1767+         DC    CL8'VSTRS'          instruction name
00002730  000027B4                               1768+         DC    A(RE27+16)          address of v2 source
00002734  000027C4                               1769+         DC    A(RE27+32)          address of v3 source
00002738  000027D4                               1770+         DC    A(RE27+48)          address of v4 source
0000273C  00000010                               1771+         DC    A(16)               result length
00002740  000027A4                               1772+REA27    DC    A(RE27)             result address
00002748  00000000 00000000                      1773+         DS    FD                  gap
00002750  00000000 00000000                      1774+V1O27    DS    XL16                V1 output
00002758  00000000 00000000
00002760  00000000 00000000                      1775+         DS    FD                  gap
                                                 1776+*
00002768                                         1777+X27      DS    0F
00002768  E310 5020 0014           00000020      1778+         LGF   R1,V2ADDR           load v2 source
0000276E  E761 0000 0806           00000000      1779+         VL    v22,0(R1)           use v22 to test decoder
00002774  E310 5024 0014           00000024      1780+         LGF   R1,V3ADDR           load v3 source
0000277A  E771 0000 0806           00000000      1781+         VL    v23,0(R1)           use v23 to test decoder
00002780  E310 5028 0014           00000028      1782+         LGF   R1,V4ADDR           load v4 source
00002786  E781 0000 0806           00000000      1783+         VL    v24,0(R1)           use v24 to test decoder
0000278C  E766 7220 8F8B                         1784+         VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00002792  B98D 0020                              1785+         EPSW  R2,R0                 extract psw
00002796  5020 500C                0000000C      1786+         ST    R2,CCPSW                 to save CC
0000279A  E760 5040 080E           00002750      1787+         VST   V22,V1O27             save v1 output
000027A0  07FB                                   1788+         BR    R11                  return
000027A4                                         1789+RE27     DC    0F                   xl16 expected result
000027A4                                         1790+         DROP  R5
000027A4  00000000 0000000C                      1791          DC    XL16'000000000000000C 0000000000000000'   V1
000027AC  00000000 00000000
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000027B4  F0F1F2F3 F4F5F6F7                        1792          DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFB01020304'   v2
000027BC  F8F9FAFB 01020304
000027C4  01020304 05060708                        1793          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000027CC  090A0B0C 0D0E0F10
000027D4  00000000 00000004                        1794          DC    XL16'0000000000000004 0000000000000000'   v4
000027DC  00000000 00000000
                                                   1795
                                                   1796 *Full Match: at middle of vector
                                                   1797 *Byte
                                                   1798          VRR_D VSTRS,0,2,2                               full match
000027E8                                           1799+         DS    0FD
000027E8                     000027E8              1800+         USING *,R5              base for test data and test routine
000027E8  00002840                                 1801+T28      DC    A(X28)            address of test routine
000027EC  001C                                     1802+         DC    H'28'             test number
000027EE  00                                       1803+         DC    X'00'
000027EF  00                                       1804+         DC    HL1'0'                 m5 used
000027F0  02                                       1805+         DC    HL1'2'                 m6 used
000027F1  02                                       1806+         DC    HL1'2'             CC
000027F2  0D                                       1807+         DC    HL1'13'            CC failed mask
000027F4  00000000 00000000                        1808+         DS    2F                 extracted PSW after test (has CC)
000027FC  FF                                       1809+         DC    X'FF'              extracted CC, if test failed
000027FD  E5E2E3D9 E2404040                        1810+         DC    CL8'VSTRS'        instruction name
00002808  0000288C                                 1811+         DC    A(RE28+16)        address of v2 source
0000280C  0000289C                                 1812+         DC    A(RE28+32)        address of v3 source
00002810  000028AC                                 1813+         DC    A(RE28+48)        address of v4 source
00002814  00000010                                 1814+         DC    A(16)             result length
00002818  0000287C                                 1815+REA28    DC    A(RE28)           result address
00002820  00000000 00000000                        1816+         DS    FD                gap
00002828  00000000 00000000                        1817+V1O28    DS    XL16              V1 output
00002830  00000000 00000000
00002838  00000000 00000000                        1818+         DS    FD                gap
                                                   1819+*
00002840                                           1820+X28      DS    0F
00002840  E310 5020 0014              00000020     1821+         LGF   R1,V2ADDR         load v2 source
00002846  E761 0000 0806              00000000     1822+         VL    v22,0(R1)         use v22 to test decoder
0000284C  E310 5024 0014              00000024     1823+         LGF   R1,V3ADDR         load v3 source
00002852  E771 0000 0806              00000000     1824+         VL    v23,0(R1)         use v23 to test decoder
00002858  E310 5028 0014              00000028     1825+         LGF   R1,V4ADDR         load v4 source
0000285E  E781 0000 0806              00000000     1826+         VL    v24,0(R1)         use v24 to test decoder
00002864  E766 7020 8F8B                           1827+         VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
0000286A  B98D 0020                                1828+         EPSW  R2,R0              extract psw
0000286E  5020 500C                   0000000C     1829+         ST    R2,CCPSW              to save CC
00002872  E760 5040 080E              00002828     1830+         VST   V22,V1O28          save v1 output
00002878  07FB                                     1831+         BR    R11               return
0000287C                                           1832+RE28     DC    0F                xl16 expected result
0000287C                                           1833+         DROP  R5
0000287C  00000000 00000006                        1834          DC    XL16'0000000000000006 0000000000000000'   V1
00002884  00000000 00000000
0000288C  F0F1F2F3 F4F50102                        1835          DC    XL16'F0F1F2F3F4F50102 0304FAFBFCFDFEFF'   v2
00002894  0304FAFB FCFDFEFF
0000289C  01020304 05060708                        1836          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000028A4  090A0B0C 0D0E0F10
000028AC  00000000 00000004                        1837          DC    XL16'0000000000000004 0000000000000000'   v4
000028B4  00000000 00000000
                                                   1838
                                                   1839 *Halfword
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1840          VRR_D VSTRS,1,2,2                                full match
000028C0                                           1841+         DS    0FD
000028C0                       000028C0            1842+         USING *,R5              base for test data and test routine
000028C0  00002918                                 1843+T29      DC    A(X29)            address of test routine
000028C4  001D                                     1844+         DC    H'29'             test number
000028C6  00                                       1845+         DC    X'00'
000028C7  01                                       1846+         DC    HL1'1'                  m5 used
000028C8  02                                       1847+         DC    HL1'2'                  m6 used
000028C9  02                                       1848+         DC    HL1'2'             CC
000028CA  0D                                       1849+         DC    HL1'13'            CC failed mask
000028CC  00000000 00000000                        1850+         DS    2F                 extracted PSW after test (has CC)
000028D4  FF                                       1851+         DC    X'FF'              extracted CC, if test failed
000028D5  E5E2E3D9 E2404040                        1852+         DC    CL8'VSTRS'         instruction name
000028E0  00002964                                 1853+         DC    A(RE29+16)         address of v2 source
000028E4  00002974                                 1854+         DC    A(RE29+32)         address of v3 source
000028E8  00002984                                 1855+         DC    A(RE29+48)         address of v4 source
000028EC  00000010                                 1856+         DC    A(16)              result length
000028F0  00002954                                 1857+REA29    DC    A(RE29)            result address
000028F8  00000000 00000000                        1858+         DS    FD                 gap
00002900  00000000 00000000                        1859+V1O29    DS    XL16               V1 output
00002908  00000000 00000000
00002910  00000000 00000000                        1860+         DS    FD                 gap
                                                   1861+*
00002918                                           1862+X29      DS    0F
00002918  E310 5020 0014                 00000020  1863+         LGF   R1,V2ADDR          load v2 source
0000291E  E761 0000 0806                 00000000  1864+         VL    v22,0(R1)          use v22 to test decoder
00002924  E310 5024 0014                 00000024  1865+         LGF   R1,V3ADDR          load v3 source
0000292A  E771 0000 0806                 00000000  1866+         VL    v23,0(R1)          use v23 to test decoder
00002930  E310 5028 0014                 00000028  1867+         LGF   R1,V4ADDR          load v4 source
00002936  E781 0000 0806                 00000000  1868+         VL    v24,0(R1)          use v24 to test decoder
0000293C  E766 7120 8F8B                           1869+         VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00002942  B98D 0020                                1870+         EPSW  R2,R0               extract psw
00002946  5020 500C                      0000000C  1871+         ST    R2,CCPSW               to save CC
0000294A  E760 5040 080E                 00002900  1872+         VST   V22,V1O29           save v1 output
00002950  07FB                                     1873+         BR    R11                 return
00002954                                           1874+RE29     DC    0F                  xl16 expected result
00002954                                           1875+         DROP  R5
00002954  00000000 00000006                        1876          DC    XL16'0000000000000006 0000000000000000'   V1
0000295C  00000000 00000000
00002964  F0F1F2F3 F4F50102                        1877          DC    XL16'F0F1F2F3F4F50102 0304FAFBFCFDFEFF'   v2
0000296C  0304FAFB FCFDFEFF
00002974  01020304 05060708                        1878          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
0000297C  090A0B0C 0D0E0F10
00002984  00000000 00000004                        1879          DC    XL16'0000000000000004 0000000000000000'   v4
0000298C  00000000 00000000
                                                   1880
                                                   1881 *Word
                                                   1882          VRR_D VSTRS,2,2,2                                full match
00002998                                           1883+         DS    0FD
00002998                       00002998            1884+         USING *,R5              base for test data and test routine
00002998  000029F0                                 1885+T30      DC    A(X30)            address of test routine
0000299C  001E                                     1886+         DC    H'30'             test number
0000299E  00                                       1887+         DC    X'00'
0000299F  02                                       1888+         DC    HL1'2'                  m5 used
000029A0  02                                       1889+         DC    HL1'2'                  m6 used
000029A1  02                                       1890+         DC    HL1'2'             CC
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000029A2  0D                                       1891+          DC    HL1'13'            CC failed mask
000029A4  00000000 00000000                        1892+          DS    2F                 extracted PSW after test (has CC)
000029AC  FF                                       1893+          DC    X'FF'              extracted CC, if test failed
000029AD  E5E2E3D9 E2404040                        1894+          DC    CL8'VSTRS'        instruction name
000029B8  00002A3C                                 1895+          DC    A(RE30+16)        address of v2 source
000029BC  00002A4C                                 1896+          DC    A(RE30+32)        address of v3 source
000029C0  00002A5C                                 1897+          DC    A(RE30+48)        address of v4 source
000029C4  00000010                                 1898+          DC    A(16)             result length
000029C8  00002A2C                                 1899+REA30     DC    A(RE30)           result address
000029D0  00000000 00000000                        1900+          DS    FD                gap
000029D8  00000000 00000000                        1901+V1O30     DS    XL16              V1 output
000029E0  00000000 00000000
000029E8  00000000 00000000                        1902+          DS    FD                gap
                                                   1903+*
000029F0                                           1904+X30       DS    0F
000029F0  E310 5020 0014                 00000020  1905+          LGF   R1,V2ADDR         load v2 source
000029F6  E761 0000 0806                 00000000  1906+          VL    v22,0(R1)         use v22 to test decoder
000029FC  E310 5024 0014                 00000024  1907+          LGF   R1,V3ADDR         load v3 source
00002A02  E771 0000 0806                 00000000  1908+          VL    v23,0(R1)         use v23 to test decoder
00002A08  E310 5028 0014                 00000028  1909+          LGF   R1,V4ADDR         load v4 source
00002A0E  E781 0000 0806                 00000000  1910+          VL    v24,0(R1)         use v24 to test decoder
00002A14  E766 7220 8F8B                           1911+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00002A1A  B98D 0020                                1912+          EPSW  R2,R0              extract psw
00002A1E  5020 500C                      0000000C  1913+          ST    R2,CCPSW              to save CC
00002A22  E760 5040 080E                 000029D8  1914+          VST   V22,V1O30          save v1 output
00002A28  07FB                                     1915+          BR    R11               return
00002A2C                                           1916+RE30      DC    0F                xl16 expected result
00002A2C                                           1917+          DROP  R5
00002A2C  00000000 00000004                        1918           DC    XL16'0000000000000004 0000000000000000'   V1
00002A34  00000000 00000000
00002A3C  F0F1F2F3 01020304                        1919           DC    XL16'F0F1F2F301020304 F4F5FAFBFCFDFEFF'   v2
00002A44  F4F5FAFB FCFDFEFF
00002A4C  01020304 05060708                        1920           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002A54  090A0B0C 0D0E0F10
00002A5C  00000000 00000004                        1921           DC    XL16'0000000000000004 0000000000000000'   v4
00002A64  00000000 00000000
                                                   1922
                                                   1923 *Full Match: at beginning of vector (and at end of vector)
                                                   1924 *Byte
                                                   1925           VRR_D VSTRS,0,2,2                               full match
00002A70                                           1926+          DS    0FD
00002A70                          00002A70         1927+          USING *,R5              base for test data and test routine
00002A70  00002AC8                                 1928+T31       DC    A(X31)            address of test routine
00002A74  001F                                     1929+          DC    H'31'             test number
00002A76  00                                       1930+          DC    X'00'
00002A77  00                                       1931+          DC    HL1'0'                 m5 used
00002A78  02                                       1932+          DC    HL1'2'                 m6 used
00002A79  02                                       1933+          DC    HL1'2'             CC
00002A7A  0D                                       1934+          DC    HL1'13'            CC failed mask
00002A7C  00000000 00000000                        1935+          DS    2F                 extracted PSW after test (has CC)
00002A84  FF                                       1936+          DC    X'FF'              extracted CC, if test failed
00002A85  E5E2E3D9 E2404040                        1937+          DC    CL8'VSTRS'        instruction name
00002A90  00002B14                                 1938+          DC    A(RE31+16)        address of v2 source
00002A94  00002B24                                 1939+          DC    A(RE31+32)        address of v3 source
00002A98  00002B34                                 1940+          DC    A(RE31+48)        address of v4 source
00002A9C  00000010                                 1941+          DC    A(16)             result length
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002AA0  00002B04                        1942+REA31    DC    A(RE31)           result address
00002AA8  00000000 00000000               1943+         DS    FD                gap
00002AB0  00000000 00000000               1944+V1O31    DS    XL16              V1 output
00002AB8  00000000 00000000
00002AC0  00000000 00000000               1945+         DS    FD                gap
                                          1946+*
00002AC8                                  1947+X31      DS    0F
00002AC8  E310 5020 0014          00000020 1948+         LGF   R1,V2ADDR         load v2 source
00002ACE  E761 0000 0806          00000000 1949+         VL    v22,0(R1)         use v22 to test decoder
00002AD4  E310 5024 0014          00000024 1950+         LGF   R1,V3ADDR         load v3 source
00002ADA  E771 0000 0806          00000000 1951+         VL    v23,0(R1)         use v23 to test decoder
00002AE0  E310 5028 0014          00000028 1952+         LGF   R1,V4ADDR         load v4 source
00002AE6  E781 0000 0806          00000000 1953+         VL    v24,0(R1)         use v24 to test decoder
00002AEC  E766 7020 8F8B                   1954+         VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00002AF2  B98D 0020                        1955+         EPSW  R2,R0              extract psw
00002AF6  5020 500C               0000000C 1956+         ST    R2,CCPSW              to save CC
00002AFA  E760 5040 080E          00002AB0 1957+         VST   V22,V1O31          save v1 output
00002B00  07FB                             1958+         BR    R11               return
00002B04                                   1959+RE31     DC    0F                xl16 expected result
00002B04                                   1960+         DROP  R5
00002B04  00000000 00000000               1961          DC    XL16'0000000000000000 0000000000000000'   V1
00002B0C  00000000 00000000
00002B14  01020304 F4F5F6F7               1962          DC    XL16'01020304F4F5F6F7 AAFDFEFF01020304'   v2
00002B1C  AAFDFEFF 01020304
00002B24  01020304 05060708               1963          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002B2C  090A0B0C 0D0E0F10
00002B34  00000000 00000004               1964          DC    XL16'0000000000000004 0000000000000000'   v4
00002B3C  00000000 00000000
                                          1965
                                          1966 *Halfword
                                          1967          VRR_D VSTRS,1,2,2                               full match
00002B48                                  1968+         DS    0FD
00002B48                        00002B48  1969+         USING *,R5              base for test data and test routine
00002B48  00002BA0                        1970+T32      DC    A(X32)            address of test routine
00002B4C  0020                            1971+         DC    H'32'             test number
00002B4E  00                              1972+         DC    X'00'
00002B4F  01                              1973+         DC    HL1'1'                 m5 used
00002B50  02                              1974+         DC    HL1'2'                 m6 used
00002B51  02                              1975+         DC    HL1'2'             CC
00002B52  0D                              1976+         DC    HL1'13'            CC failed mask
00002B54  00000000 00000000               1977+         DS    2F                 extracted PSW after test (has CC)
00002B5C  FF                              1978+         DC    X'FF'              extracted CC, if test failed
00002B5D  E5E2E3D9 E2404040               1979+         DC    CL8'VSTRS'        instruction name
00002B68  00002BEC                        1980+         DC    A(RE32+16)        address of v2 source
00002B6C  00002BFC                        1981+         DC    A(RE32+32)        address of v3 source
00002B70  00002C0C                        1982+         DC    A(RE32+48)        address of v4 source
00002B74  00000010                        1983+         DC    A(16)             result length
00002B78  00002BDC                        1984+REA32    DC    A(RE32)           result address
00002B80  00000000 00000000               1985+         DS    FD                gap
00002B88  00000000 00000000               1986+V1O32    DS    XL16              V1 output
00002B90  00000000 00000000
00002B98  00000000 00000000               1987+         DS    FD                gap
                                          1988+*
00002BA0                                  1989+X32      DS    0F
00002BA0  E310 5020 0014          00000020 1990+         LGF   R1,V2ADDR         load v2 source
00002BA6  E761 0000 0806          00000000 1991+         VL    v22,0(R1)         use v22 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002BAC  E310 5024 0014                 00000024  1992+          LGF    R1,V3ADDR          load v3 source
00002BB2  E771 0000 0806                 00000000  1993+          VL     v23,0(R1)          use v23 to test decoder
00002BB8  E310 5028 0014                 00000028  1994+          LGF    R1,V4ADDR          load v4 source
00002BBE  E781 0000 0806                 00000000  1995+          VL     v24,0(R1)          use v24 to test decoder
00002BC4  E766 7120 8F8B                           1996+          VSTRS  V22,V22,V23,V24,1,2      instruction (dest is a source)
00002BCA  B98D 0020                                1997+          EPSW   R2,R0               extract psw
00002BCE  5020 500C                      0000000C  1998+          ST     R2,CCPSW               to save CC
00002BD2  E760 5040 080E                 00002B88  1999+          VST    V22,V1O32           save v1 output
00002BD8  07FB                                     2000+          BR     R11                return
00002BDC                                           2001+RE32      DC     0F                 xl16 expected result
00002BDC                                           2002+          DROP   R5
00002BDC  00000000 00000000                        2003           DC     XL16'0000000000000000 0000000000000000'   V1
00002BE4  00000000 00000000
00002BEC  01020304 F4F5F6F7                        2004           DC     XL16'01020304F4F5F6F7 AAFDFEFF01020304'   v2
00002BF4  AAFDFEFF 01020304
00002BFC  01020304 05060708                        2005           DC     XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002C04  090A0B0C 0D0E0F10
00002C0C  00000000 00000004                        2006           DC     XL16'0000000000000004 0000000000000000'   v4
00002C14  00000000 00000000
                                                   2007
                                                   2008 *Word
                                                   2009           VRR_D  VSTRS,2,2,2                               full match
00002C20                                           2010+          DS     0FD
00002C20                         00002C20          2011+          USING  *,R5               base for test data and test routine
00002C20  00002C78                                 2012+T33       DC     A(X33)             address of test routine
00002C24  0021                                     2013+          DC     H'33'              test number
00002C26  00                                       2014+          DC     X'00'
00002C27  02                                       2015+          DC     HL1'2'                   m5 used
00002C28  02                                       2016+          DC     HL1'2'                   m6 used
00002C29  02                                       2017+          DC     HL1'2'              CC
00002C2A  0D                                       2018+          DC     HL1'13'             CC failed mask
00002C2C  00000000 00000000                        2019+          DS     2F                  extracted PSW after test (has CC)
00002C34  FF                                       2020+          DC     X'FF'               extracted CC, if test failed
00002C35  E5E2E3D9 E2404040                        2021+          DC     CL8'VSTRS'         instruction name
00002C40  00002CC4                                 2022+          DC     A(RE33+16)         address of v2 source
00002C44  00002CD4                                 2023+          DC     A(RE33+32)         address of v3 source
00002C48  00002CE4                                 2024+          DC     A(RE33+48)         address of v4 source
00002C4C  00000010                                 2025+          DC     A(16)              result length
00002C50  00002CB4                                 2026+REA33     DC     A(RE33)            result address
00002C58  00000000 00000000                        2027+          DS     FD                 gap
00002C60  00000000 00000000                        2028+V1O33     DS     XL16               V1 output
00002C68  00000000 00000000
00002C70  00000000 00000000                        2029+          DS     FD                 gap
                                                   2030+*
00002C78                                           2031+X33       DS     0F
00002C78  E310 5020 0014                 00000020  2032+          LGF    R1,V2ADDR          load v2 source
00002C7E  E761 0000 0806                 00000000  2033+          VL     v22,0(R1)          use v22 to test decoder
00002C84  E310 5024 0014                 00000024  2034+          LGF    R1,V3ADDR          load v3 source
00002C8A  E771 0000 0806                 00000000  2035+          VL     v23,0(R1)          use v23 to test decoder
00002C90  E310 5028 0014                 00000028  2036+          LGF    R1,V4ADDR          load v4 source
00002C96  E781 0000 0806                 00000000  2037+          VL     v24,0(R1)          use v24 to test decoder
00002C9C  E766 7220 8F8B                           2038+          VSTRS  V22,V22,V23,V24,2,2      instruction (dest is a source)
00002CA2  B98D 0020                                2039+          EPSW   R2,R0               extract psw
00002CA6  5020 500C                      0000000C  2040+          ST     R2,CCPSW               to save CC
00002CAA  E760 5040 080E                 00002C60  2041+          VST    V22,V1O33           save v1 output
00002CB0  07FB                                     2042+          BR     R11                return
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002CB4                                           2043+RE33     DC    0F                xl16 expected result
00002CB4                                           2044+         DROP  R5
00002CB4  00000000 00000000                        2045          DC    XL16'0000000000000000 0000000000000000'   V1
00002CBC  00000000 00000000
00002CC4  01020304 F4F5F6F7                        2046          DC    XL16'01020304F4F5F6F7 AAFDFEFF01020304'   v2
00002CCC  AAFDFEFF 01020304
00002CD4  01020304 05060708                        2047          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002CDC  090A0B0C 0D0E0F10
00002CE4  00000000 00000004                        2048          DC    XL16'0000000000000004 0000000000000000'   v4
00002CEC  00000000 00000000
                                                   2049
                                                   2050 *Full Match: at beginning of vector (and partial at end of vector)
                                                   2051 *Byte
                                                   2052          VRR_D VSTRS,0,2,2                               full match
00002CF8                                           2053+         DS    0FD
00002CF8                     00002CF8              2054+         USING *,R5              base for test data and test routine
00002CF8  00002D50                                 2055+T34      DC    A(X34)            address of test routine
00002CFC  0022                                     2056+         DC    H'34'             test number
00002CFE  00                                       2057+         DC    X'00'
00002CFF  00                                       2058+         DC    HL1'0'                  m5 used
00002D00  02                                       2059+         DC    HL1'2'                  m6 used
00002D01  02                                       2060+         DC    HL1'2'             CC
00002D02  0D                                       2061+         DC    HL1'13'            CC failed mask
00002D04  00000000 00000000                        2062+         DS    2F                 extracted PSW after test (has CC)
00002D0C  FF                                       2063+         DC    X'FF'              extracted CC, if test failed
00002D0D  E5E2E3D9 E2404040                        2064+         DC    CL8'VSTRS'        instruction name
00002D18  00002D9C                                 2065+         DC    A(RE34+16)        address of v2 source
00002D1C  00002DAC                                 2066+         DC    A(RE34+32)        address of v3 source
00002D20  00002DBC                                 2067+         DC    A(RE34+48)        address of v4 source
00002D24  00000010                                 2068+         DC    A(16)             result length
00002D28  00002D8C                                 2069+REA34    DC    A(RE34)           result address
00002D30  00000000 00000000                        2070+         DS    FD                gap
00002D38  00000000 00000000                        2071+V1O34    DS    XL16              V1 output
00002D40  00000000 00000000
00002D48  00000000 00000000                        2072+         DS    FD                gap
                                                   2073+*
00002D50                                           2074+X34      DS    0F
00002D50  E310 5020 0014              00000020     2075+         LGF   R1,V2ADDR         load v2 source
00002D56  E761 0000 0806              00000000     2076+         VL    v22,0(R1)         use v22 to test decoder
00002D5C  E310 5024 0014              00000024     2077+         LGF   R1,V3ADDR         load v3 source
00002D62  E771 0000 0806              00000000     2078+         VL    v23,0(R1)         use v23 to test decoder
00002D68  E310 5028 0014              00000028     2079+         LGF   R1,V4ADDR         load v4 source
00002D6E  E781 0000 0806              00000000     2080+         VL    v24,0(R1)         use v24 to test decoder
00002D74  E766 7020 8F8B                           2081+         VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00002D7A  B98D 0020                                2082+         EPSW  R2,R0              extract psw
00002D7E  5020 500C                   0000000C     2083+         ST    R2,CCPSW              to save CC
00002D82  E760 5040 080E              00002D38     2084+         VST   V22,V1O34          save v1 output
00002D88  07FB                                     2085+         BR    R11               return
00002D8C                                           2086+RE34     DC    0F                xl16 expected result
00002D8C                                           2087+         DROP  R5
00002D8C  00000000 00000000                        2088          DC    XL16'0000000000000000 0000000000000000'   V1
00002D94  00000000 00000000
00002D9C  01020304 F4F5F6F7                        2089          DC    XL16'01020304F4F5F6F7 AAFDFEFFBB010203'   v2
00002DA4  AAFDFEFF BB010203
00002DAC  01020304 05060708                        2090          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002DB4  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002DBC  00000000 00000004                        2091           DC    XL16'0000000000000004 0000000000000000'   v4
00002DC4  00000000 00000000
                                                   2092
                                                   2093 *Halfword
                                                   2094           VRR_D VSTRS,1,2,2                               full match
00002DD0                                           2095+          DS    0FD
00002DD0                     00002DD0              2096+          USING *,R5              base for test data and test routine
00002DD0  00002E28                                 2097+T35       DC    A(X35)            address of test routine
00002DD4  0023                                     2098+          DC    H'35'             test number
00002DD6  00                                       2099+          DC    X'00'
00002DD7  01                                       2100+          DC    HL1'1'                  m5 used
00002DD8  02                                       2101+          DC    HL1'2'                  m6 used
00002DD9  02                                       2102+          DC    HL1'2'             CC
00002DDA  0D                                       2103+          DC    HL1'13'            CC failed mask
00002DDC  00000000 00000000                        2104+          DS    2F                 extracted PSW after test (has CC)
00002DE4  FF                                       2105+          DC    X'FF'              extracted CC, if test failed
00002DE5  E5E2E3D9 E2404040                        2106+          DC    CL8'VSTRS'        instruction name
00002DF0  00002E74                                 2107+          DC    A(RE35+16)        address of v2 source
00002DF4  00002E84                                 2108+          DC    A(RE35+32)        address of v3 source
00002DF8  00002E94                                 2109+          DC    A(RE35+48)        address of v4 source
00002DFC  00000010                                 2110+          DC    A(16)             result length
00002E00  00002E64                                 2111+REA35     DC    A(RE35)           result address
00002E08  00000000 00000000                        2112+          DS    FD                gap
00002E10  00000000 00000000                        2113+V1O35     DS    XL16              V1 output
00002E18  00000000 00000000
00002E20  00000000 00000000                        2114+          DS    FD                gap
                                                   2115+*
00002E28                                           2116+X35       DS    0F
00002E28  E310 5020 0014                 00000020  2117+          LGF   R1,V2ADDR         load v2 source
00002E2E  E761 0000 0806                 00000000  2118+          VL    v22,0(R1)         use v22 to test decoder
00002E34  E310 5024 0014                 00000024  2119+          LGF   R1,V3ADDR         load v3 source
00002E3A  E771 0000 0806                 00000000  2120+          VL    v23,0(R1)         use v23 to test decoder
00002E40  E310 5028 0014                 00000028  2121+          LGF   R1,V4ADDR         load v4 source
00002E46  E781 0000 0806                 00000000  2122+          VL    v24,0(R1)         use v24 to test decoder
00002E4C  E766 7120 8F8B                           2123+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00002E52  B98D 0020                                2124+          EPSW  R2,R0              extract psw
00002E56  5020 500C                      0000000C  2125+          ST    R2,CCPSW              to save CC
00002E5A  E760 5040 080E                 00002E10  2126+          VST   V22,V1O35          save v1 output
00002E60  07FB                                     2127+          BR    R11               return
00002E64                                           2128+RE35      DC    0F                xl16 expected result
00002E64                                           2129+          DROP  R5
00002E64  00000000 00000000                        2130           DC    XL16'0000000000000000 0000000000000000'   V1
00002E6C  00000000 00000000
00002E74  01020304 F4F5F6F7                        2131           DC    XL16'01020304F4F5F6F7 AAFDFEFFBBBB0102'   v2
00002E7C  AAFDFEFF BBBB0102
00002E84  01020304 05060708                        2132           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002E8C  090A0B0C 0D0E0F10
00002E94  00000000 00000004                        2133           DC    XL16'0000000000000004 0000000000000000'   v4
00002E9C  00000000 00000000
                                                   2134
                                                   2135 *Word
                                                   2136           VRR_D VSTRS,2,2,2                               full match
00002EA8                                           2137+          DS    0FD
00002EA8                     00002EA8              2138+          USING *,R5              base for test data and test routine
00002EA8  00002F00                                 2139+T36       DC    A(X36)            address of test routine
00002EAC  0024                                     2140+          DC    H'36'             test number
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002EAE  00                                      2141+          DC    X'00'
00002EAF  02                                      2142+          DC    HL1'2'                  m5 used
00002EB0  02                                      2143+          DC    HL1'2'                  m6 used
00002EB1  02                                      2144+          DC    HL1'2'               CC
00002EB2  0D                                      2145+          DC    HL1'13'              CC failed mask
00002EB4  00000000 00000000                       2146+          DS    2F                   extracted PSW after test (has CC)
00002EBC  FF                                      2147+          DC    X'FF'                extracted CC, if test failed
00002EBD  E5E2E3D9 E2404040                       2148+          DC    CL8'VSTRS'           instruction name
00002EC8  00002F4C                                2149+          DC    A(RE36+16)           address of v2 source
00002ECC  00002F5C                                2150+          DC    A(RE36+32)           address of v3 source
00002ED0  00002F6C                                2151+          DC    A(RE36+48)           address of v4 source
00002ED4  00000010                                2152+          DC    A(16)                result length
00002ED8  00002F3C                                2153+REA36     DC    A(RE36)              result address
00002EE0  00000000 00000000                       2154+          DS    FD                   gap
00002EE8  00000000 00000000                       2155+V1O36     DS    XL16                 V1 output
00002EF0  00000000 00000000
00002EF8  00000000 00000000                       2156+          DS    FD                   gap
                                                  2157+*
00002F00                                          2158+X36       DS    0F
00002F00  E310 5020 0014                 00000020 2159+          LGF   R1,V2ADDR            load v2 source
00002F06  E761 0000 0806                 00000000 2160+          VL    v22,0(R1)            use v22 to test decoder
00002F0C  E310 5024 0014                 00000024 2161+          LGF   R1,V3ADDR            load v3 source
00002F12  E771 0000 0806                 00000000 2162+          VL    v23,0(R1)            use v23 to test decoder
00002F18  E310 5028 0014                 00000028 2163+          LGF   R1,V4ADDR            load v4 source
00002F1E  E781 0000 0806                 00000000 2164+          VL    v24,0(R1)            use v24 to test decoder
00002F24  E766 7220 8F8B                          2165+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00002F2A  B98D 0020                               2166+          EPSW  R2,R0                 extract psw
00002F2E  5020 500C                      0000000C 2167+          ST    R2,CCPSW                 to save CC
00002F32  E760 5040 080E                 00002EE8 2168+          VST   V22,V1O36             save v1 output
00002F38  07FB                                    2169+          BR    R11                  return
00002F3C                                          2170+RE36      DC    0F                   xl16 expected result
00002F3C                                          2171+          DROP  R5
00002F3C  00000000 00000000                       2172           DC    XL16'0000000000000000 0000000000000000'   V1
00002F44  00000000 00000000
00002F4C  01020304 05060708                       2173           DC    XL16'0102030405060708 AAFDFEFF01020304'   v2
00002F54  AAFDFEFF 01020304
00002F5C  01020304 05060708                       2174           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002F64  090A0B0C 0D0E0F10
00002F6C  00000000 00000008                       2175           DC    XL16'0000000000000008 0000000000000000'   v4
00002F74  00000000 00000000
                                                  2176
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2178 *-------------------------------------------------------------------
                                                   2179 * case 3 - full match; V3 substr length from ZS: ZS=1 CC=2
                                                   2180 *-------------------------------------------------------------------
                                                   2181 *Full Match: at beginning of vector
                                                   2182 *Byte
                                                   2183          VRR_D VSTRS,0,2,2                              full match
00002F80                                           2184+         DS    0FD
00002F80                          00002F80         2185+         USING *,R5              base for test data and test routine
00002F80  00002FD8                                 2186+T37      DC    A(X37)            address of test routine
00002F84  0025                                     2187+         DC    H'37'             test number
00002F86  00                                       2188+         DC    X'00'
00002F87  00                                       2189+         DC    HL1'0'                  m5 used
00002F88  02                                       2190+         DC    HL1'2'                  m6 used
00002F89  02                                       2191+         DC    HL1'2'             CC
00002F8A  0D                                       2192+         DC    HL1'13'            CC failed mask
00002F8C  00000000 00000000                        2193+         DS    2F                 extracted PSW after test (has CC)
00002F94  FF                                       2194+         DC    X'FF'              extracted CC, if test failed
00002F95  E5E2E3D9 E2404040                        2195+         DC    CL8'VSTRS'        instruction name
00002FA0  00003024                                 2196+         DC    A(RE37+16)        address of v2 source
00002FA4  00003034                                 2197+         DC    A(RE37+32)        address of v3 source
00002FA8  00003044                                 2198+         DC    A(RE37+48)        address of v4 source
00002FAC  00000010                                 2199+         DC    A(16)             result length
00002FB0  00003014                                 2200+REA37    DC    A(RE37)           result address
00002FB8  00000000 00000000                        2201+         DS    FD                gap
00002FC0  00000000 00000000                        2202+V1O37    DS    XL16              V1 output
00002FC8  00000000 00000000
00002FD0  00000000 00000000                        2203+         DS    FD                gap
                                                   2204+*
00002FD8                                           2205+X37      DS    0F
00002FD8  E310 5020 0014                 00000020  2206+         LGF   R1,V2ADDR         load v2 source
00002FDE  E761 0000 0806                 00000000  2207+         VL    v22,0(R1)         use v22 to test decoder
00002FE4  E310 5024 0014                 00000024  2208+         LGF   R1,V3ADDR         load v3 source
00002FEA  E771 0000 0806                 00000000  2209+         VL    v23,0(R1)         use v23 to test decoder
00002FF0  E310 5028 0014                 00000028  2210+         LGF   R1,V4ADDR         load v4 source
00002FF6  E781 0000 0806                 00000000  2211+         VL    v24,0(R1)         use v24 to test decoder
00002FFC  E766 7020 8F8B                           2212+         VSTRS V22,V22,V23,V24,0,2     instruction (dest is a source)
00003002  B98D 0020                                2213+         EPSW  R2,R0              extract psw
00003006  5020 500C                      0000000C  2214+         ST    R2,CCPSW              to save CC
0000300A  E760 5040 080E                 00002FC0  2215+         VST   V22,V1O37          save v1 output
00003010  07FB                                     2216+         BR    R11               return
00003014                                           2217+RE37     DC    0F                xl16 expected result
00003014                                           2218+         DROP  R5
00003014  00000000 00000000                        2219          DC    XL16'0000000000000000 0000000000000000'   V1
0000301C  00000000 00000000
00003024  01020304 F4F5F6F7                        2220          DC    XL16'01020304F4F5F6F7 01020304AAFDFEFF'   v2
0000302C  01020304 AAFDFEFF
00003034  01020300 05060700                        2221          DC    XL16'0102030005060700 090A0B0C0D0E0F10'   v3
0000303C  090A0B0C 0D0E0F10
00003044  00000000 00000004                        2222          DC    XL16'0000000000000004 0000000000000000'   v4
0000304C  00000000 00000000
                                                   2223
                                                   2224 *Halfword
                                                   2225          VRR_D VSTRS,1,2,2                              full match
00003058                                           2226+         DS    0FD
00003058                          00003058         2227+         USING *,R5              base for test data and test routine
00003058  000030B0                                 2228+T38      DC    A(X38)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000305C  0026                                    2229+          DC    H'38'              test number
0000305E  00                                      2230+          DC    X'00'
0000305F  01                                      2231+          DC    HL1'1'                   m5 used
00003060  02                                      2232+          DC    HL1'2'                   m6 used
00003061  02                                      2233+          DC    HL1'2'              CC
00003062  0D                                      2234+          DC    HL1'13'             CC failed mask
00003064  00000000 00000000                       2235+          DS    2F                  extracted PSW after test (has CC)
0000306C  FF                                      2236+          DC    X'FF'               extracted CC, if test failed
0000306D  E5E2E3D9 E2404040                       2237+          DC    CL8'VSTRS'         instruction name
00003078  000030FC                                2238+          DC    A(RE38+16)         address of v2 source
0000307C  0000310C                                2239+          DC    A(RE38+32)         address of v3 source
00003080  0000311C                                2240+          DC    A(RE38+48)         address of v4 source
00003084  00000010                                2241+          DC    A(16)              result length
00003088  000030EC                                2242+REA38     DC    A(RE38)            result address
00003090  00000000 00000000                       2243+          DS    FD                 gap
00003098  00000000 00000000                       2244+V1038     DS    XL16               V1 output
000030A0  00000000 00000000
000030A8  00000000 00000000                       2245+          DS    FD                 gap
                                                  2246+*
000030B0                                          2247+X38       DS    0F
000030B0  E310 5020 0014                 00000020 2248+          LGF   R1,V2ADDR          load v2 source
000030B6  E761 0000 0806                 00000000 2249+          VL    v22,0(R1)          use v22 to test decoder
000030BC  E310 5024 0014                 00000024 2250+          LGF   R1,V3ADDR          load v3 source
000030C2  E771 0000 0806                 00000000 2251+          VL    v23,0(R1)          use v23 to test decoder
000030C8  E310 5028 0014                 00000028 2252+          LGF   R1,V4ADDR          load v4 source
000030CE  E781 0000 0806                 00000000 2253+          VL    v24,0(R1)          use v24 to test decoder
000030D4  E766 7120 8F8B                          2254+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
000030DA  B98D 0020                               2255+          EPSW  R2,R0               extract psw
000030DE  5020 500C                      0000000C 2256+          ST    R2,CCPSW               to save CC
000030E2  E760 5040 080E                 00003098 2257+          VST   V22,V1038           save v1 output
000030E8  07FB                                    2258+          BR    R11                return
000030EC                                          2259+RE38      DC    0F                 xl16 expected result
000030EC                                          2260+          DROP  R5
000030EC  00000000 00000000                       2261           DC    XL16'0000000000000000 0000000000000000'   V1
000030F4  00000000 00000000
000030FC  01020304 F4F5F6F7                       2262           DC    XL16'01020304F4F5F6F7 01020304AAFDFEFF'   v2
00003104  01020304 AAFDFEFF
0000310C  01020000 05060000                       2263           DC    XL16'0102000005060000 090A0B0C0D0E0F10'   v3
00003114  090A0B0C 0D0E0F10
0000311C  00000000 00000004                       2264           DC    XL16'0000000000000004 0000000000000000'   v4
00003124  00000000 00000000
                                                  2265
                                                  2266 *Word
                                                  2267           VRR_D VSTRS,2,2,2                               full match
00003130                                          2268+          DS    0FD
00003130                         00003130         2269+          USING *,R5               base for test data and test routine
00003130  00003188                                2270+T39       DC    A(X39)             address of test routine
00003134  0027                                    2271+          DC    H'39'              test number
00003136  00                                      2272+          DC    X'00'
00003137  02                                      2273+          DC    HL1'2'                   m5 used
00003138  02                                      2274+          DC    HL1'2'                   m6 used
00003139  02                                      2275+          DC    HL1'2'              CC
0000313A  0D                                      2276+          DC    HL1'13'             CC failed mask
0000313C  00000000 00000000                       2277+          DS    2F                  extracted PSW after test (has CC)
00003144  FF                                      2278+          DC    X'FF'               extracted CC, if test failed
00003145  E5E2E3D9 E2404040                       2279+          DC    CL8'VSTRS'         instruction name
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003150  000031D4                                2280+          DC    A(RE39+16)         address of v2 source
00003154  000031E4                                2281+          DC    A(RE39+32)         address of v3 source
00003158  000031F4                                2282+          DC    A(RE39+48)         address of v4 source
0000315C  00000010                                2283+          DC    A(16)              result length
00003160  000031C4                                2284+REA39     DC    A(RE39)            result address
00003168  00000000 00000000                       2285+          DS    FD                 gap
00003170  00000000 00000000                       2286+V1O39     DS    XL16               V1 output
00003178  00000000 00000000
00003180  00000000 00000000                       2287+          DS    FD                 gap
                                                  2288+*
00003188                                          2289+X39       DS    0F
00003188  E310 5020 0014                 00000020 2290+          LGF   R1,V2ADDR          load v2 source
0000318E  E761 0000 0806                 00000000 2291+          VL    v22,0(R1)          use v22 to test decoder
00003194  E310 5024 0014                 00000024 2292+          LGF   R1,V3ADDR          load v3 source
0000319A  E771 0000 0806                 00000000 2293+          VL    v23,0(R1)          use v23 to test decoder
000031A0  E310 5028 0014                 00000028 2294+          LGF   R1,V4ADDR          load v4 source
000031A6  E781 0000 0806                 00000000 2295+          VL    v24,0(R1)          use v24 to test decoder
000031AC  E766 7220 8F8B                          2296+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
000031B2  B98D 0020                               2297+          EPSW  R2,R0               extract psw
000031B6  5020 500C                      0000000C 2298+          ST    R2,CCPSW               to save CC
000031BA  E760 5040 080E                 00003170 2299+          VST   V22,V1O39           save v1 output
000031C0  07FB                                    2300+          BR    R11                return
000031C4                                          2301+RE39      DC    0F                 xl16 expected result
000031C4                                          2302+          DROP  R5
000031C4  00000000 00000000                       2303           DC    XL16'0000000000000000 0000000000000000'   V1
000031CC  00000000 00000000
000031D4  01020304 F4F5F6F7                       2304           DC    XL16'01020304F4F5F6F7 0102030405AAAAFF'   v2
000031DC  01020304 05AAAAFF
000031E4  01020304 00000000                       2305           DC    XL16'0102030400000000 000000000D0E0F10'   v3
000031EC  00000000 0D0E0F10
000031F4  00000000 00000004                       2306           DC    XL16'0000000000000004 0000000000000000'   v4
000031FC  00000000 00000000
                                                  2307
                                                  2308 *Full Match: at end of vector
                                                  2309 *Byte
                                                  2310           VRR_D VSTRS,0,2,2                               full match
00003208                                          2311+          DS    0FD
00003208                          00003208        2312+          USING *,R5               base for test data and test routine
00003208  00003260                                2313+T40       DC    A(X40)             address of test routine
0000320C  0028                                    2314+          DC    H'40'              test number
0000320E  00                                      2315+          DC    X'00'
0000320F  00                                      2316+          DC    HL1'0'                   m5 used
00003210  02                                      2317+          DC    HL1'2'                   m6 used
00003211  02                                      2318+          DC    HL1'2'              CC
00003212  0D                                      2319+          DC    HL1'13'             CC failed mask
00003214  00000000 00000000                       2320+          DS    2F                  extracted PSW after test (has CC)
0000321C  FF                                      2321+          DC    X'FF'               extracted CC, if test failed
0000321D  E5E2E3D9 E2404040                       2322+          DC    CL8'VSTRS'         instruction name
00003228  000032AC                                2323+          DC    A(RE40+16)         address of v2 source
0000322C  000032BC                                2324+          DC    A(RE40+32)         address of v3 source
00003230  000032CC                                2325+          DC    A(RE40+48)         address of v4 source
00003234  00000010                                2326+          DC    A(16)              result length
00003238  0000329C                                2327+REA40     DC    A(RE40)            result address
00003240  00000000 00000000                       2328+          DS    FD                 gap
00003248  00000000 00000000                       2329+V1O40     DS    XL16               V1 output
00003250  00000000 00000000
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003258  00000000 00000000                        2330+          DS    FD                gap
                                                   2331+*
00003260                                           2332+X40       DS    0F
00003260  E310 5020 0014                 00000020  2333+          LGF   R1,V2ADDR          load v2 source
00003266  E761 0000 0806                 00000000  2334+          VL    v22,0(R1)         use v22 to test decoder
0000326C  E310 5024 0014                 00000024  2335+          LGF   R1,V3ADDR          load v3 source
00003272  E771 0000 0806                 00000000  2336+          VL    v23,0(R1)         use v23 to test decoder
00003278  E310 5028 0014                 00000028  2337+          LGF   R1,V4ADDR          load v4 source
0000327E  E781 0000 0806                 00000000  2338+          VL    v24,0(R1)         use v24 to test decoder
00003284  E766 7020 8F8B                           2339+          VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
0000328A  B98D 0020                                2340+          EPSW  R2,R0              extract psw
0000328E  5020 500C                      0000000C  2341+          ST    R2,CCPSW              to save CC
00003292  E760 5040 080E                 00003248  2342+          VST   V22,V1O40           save v1 output
00003298  07FB                                     2343+          BR    R11               return
0000329C                                           2344+RE40      DC    0F                xl16 expected result
0000329C                                           2345+          DROP  R5
0000329C  00000000 0000000C                        2346           DC    XL16'000000000000000C 0000000000000000'   V1
000032A4  00000000 00000000
000032AC  F0F1F2F3 F4F5F6F7                        2347           DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFB01020304'   v2
000032B4  F8F9FAFB 01020304
000032BC  01020300 05060700                        2348           DC    XL16'0102030005060700 090A0B0C0D0E0F10'   v3
000032C4  090A0B0C 0D0E0F10
000032CC  00000000 00000004                        2349           DC    XL16'0000000000000004 0000000000000000'   v4
000032D4  00000000 00000000
                                                   2350
                                                   2351 *Halfword
                                                   2352           VRR_D VSTRS,1,2,2                              full match
000032E0                                           2353+          DS    0FD
000032E0                         000032E0          2354+          USING *,R5              base for test data and test routine
000032E0  00003338                                 2355+T41       DC    A(X41)            address of test routine
000032E4  0029                                     2356+          DC    H'41'             test number
000032E6  00                                       2357+          DC    X'00'
000032E7  01                                       2358+          DC    HL1'1'                 m5 used
000032E8  02                                       2359+          DC    HL1'2'                 m6 used
000032E9  02                                       2360+          DC    HL1'2'             CC
000032EA  0D                                       2361+          DC    HL1'13'            CC failed mask
000032EC  00000000 00000000                        2362+          DS    2F                 extracted PSW after test (has CC)
000032F4  FF                                       2363+          DC    X'FF'              extracted CC, if test failed
000032F5  E5E2E3D9 E2404040                        2364+          DC    CL8'VSTRS'        instruction name
00003300  00003384                                 2365+          DC    A(RE41+16)        address of v2 source
00003304  00003394                                 2366+          DC    A(RE41+32)        address of v3 source
00003308  000033A4                                 2367+          DC    A(RE41+48)        address of v4 source
0000330C  00000010                                 2368+          DC    A(16)             result length
00003310  00003374                                 2369+REA41     DC    A(RE41)           result address
00003318  00000000 00000000                        2370+          DS    FD                gap
00003320  00000000 00000000                        2371+V1O41     DS    XL16              V1 output
00003328  00000000 00000000
00003330  00000000 00000000                        2372+          DS    FD                gap
                                                   2373+*
00003338                                           2374+X41       DS    0F
00003338  E310 5020 0014                 00000020  2375+          LGF   R1,V2ADDR          load v2 source
0000333E  E761 0000 0806                 00000000  2376+          VL    v22,0(R1)         use v22 to test decoder
00003344  E310 5024 0014                 00000024  2377+          LGF   R1,V3ADDR          load v3 source
0000334A  E771 0000 0806                 00000000  2378+          VL    v23,0(R1)         use v23 to test decoder
00003350  E310 5028 0014                 00000028  2379+          LGF   R1,V4ADDR          load v4 source
00003356  E781 0000 0806                 00000000  2380+          VL    v24,0(R1)         use v24 to test decoder
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000335C  E766 7120 8F8B                          2381+         VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00003362  B98D 0020                               2382+         EPSW  R2,R0                 extract psw
00003366  5020 500C                     0000000C  2383+         ST    R2,CCPSW                 to save CC
0000336A  E760 5040 080E                00003320  2384+         VST   V22,V1O41               save v1 output
00003370  07FB                                    2385+         BR    R11                   return
00003374                                          2386+RE41     DC    0F                    xl16 expected result
00003374                                          2387+         DROP  R5
00003374  00000000 0000000C                       2388          DC    XL16'000000000000000C 0000000000000000'   V1
0000337C  00000000 00000000
00003384  F0F1F2F3 F4F5F6F7                       2389          DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFB01020304'   v2
0000338C  F8F9FAFB 01020304
00003394  01020000 05060000                       2390          DC    XL16'0102000005060000 090A0B0C0D0E0F10'   v3
0000339C  090A0B0C 0D0E0F10
000033A4  00000000 00000004                       2391          DC    XL16'0000000000000004 0000000000000000'   v4
000033AC  00000000 00000000
                                                  2392
                                                  2393 *Word
                                                  2394          VRR_D VSTRS,2,2,2                               full match
000033B8                                          2395+         DS    0FD
000033B8                        000033B8          2396+         USING *,R5                  base for test data and test routine
000033B8  00003410                                2397+T42      DC    A(X42)                address of test routine
000033BC  002A                                    2398+         DC    H'42'                 test number
000033BE  00                                      2399+         DC    X'00'
000033BF  02                                      2400+         DC    HL1'2'                      m5 used
000033C0  02                                      2401+         DC    HL1'2'                      m6 used
000033C1  02                                      2402+         DC    HL1'2'                 CC
000033C2  0D                                      2403+         DC    HL1'13'                CC failed mask
000033C4  00000000 00000000                       2404+         DS    2F                     extracted PSW after test (has CC)
000033CC  FF                                      2405+         DC    X'FF'                  extracted CC, if test failed
000033CD  E5E2E3D9 E2404040                       2406+         DC    CL8'VSTRS'            instruction name
000033D8  0000345C                                2407+         DC    A(RE42+16)            address of v2 source
000033DC  0000346C                                2408+         DC    A(RE42+32)            address of v3 source
000033E0  0000347C                                2409+         DC    A(RE42+48)            address of v4 source
000033E4  00000010                                2410+         DC    A(16)                 result length
000033E8  0000344C                                2411+REA42    DC    A(RE42)               result address
000033F0  00000000 00000000                       2412+         DS    FD                    gap
000033F8  00000000 00000000                       2413+V1O42    DS    XL16                  V1 output
00003400  00000000 00000000
00003408  00000000 00000000                       2414+         DS    FD                    gap
                                                  2415+*
00003410                                          2416+X42      DS    0F
00003410  E310 5020 0014                00000020  2417+         LGF   R1,V2ADDR             load v2 source
00003416  E761 0000 0806                00000000  2418+         VL    v22,0(R1)             use v22 to test decoder
0000341C  E310 5024 0014                00000024  2419+         LGF   R1,V3ADDR             load v3 source
00003422  E771 0000 0806                00000000  2420+         VL    v23,0(R1)             use v23 to test decoder
00003428  E310 5028 0014                00000028  2421+         LGF   R1,V4ADDR             load v4 source
0000342E  E781 0000 0806                00000000  2422+         VL    v24,0(R1)             use v24 to test decoder
00003434  E766 7220 8F8B                          2423+         VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
0000343A  B98D 0020                               2424+         EPSW  R2,R0                 extract psw
0000343E  5020 500C                     0000000C  2425+         ST    R2,CCPSW                 to save CC
00003442  E760 5040 080E                000033F8  2426+         VST   V22,V1O42               save v1 output
00003448  07FB                                    2427+         BR    R11                   return
0000344C                                          2428+RE42     DC    0F                    xl16 expected result
0000344C                                          2429+         DROP  R5
0000344C  00000000 0000000C                       2430          DC    XL16'000000000000000C 0000000000000000'   V1
00003454  00000000 00000000
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000345C  F0F1F2F3 F4F5F6F7                        2431           DC    XL16'F0F1F2F3F4F5F6F7 F8F9FAFB01020304'   v2
00003464  F8F9FAFB 01020304
0000346C  01020304 00000000                        2432           DC    XL16'0102030400000000 000000000D0E0F10'   v3
00003474  00000000 0D0E0F10
0000347C  00000000 00000004                        2433           DC    XL16'0000000000000004 0000000000000000'   v4
00003484  00000000 00000000
                                                   2434
                                                   2435 *Full Match: at middle of vector
                                                   2436 *Byte
                                                   2437           VRR_D VSTRS,0,2,2                               full match
00003490                                           2438+          DS    0FD
00003490                      00003490             2439+          USING *,R5              base for test data and test routine
00003490  000034E8                                 2440+T43       DC    A(X43)            address of test routine
00003494  002B                                     2441+          DC    H'43'             test number
00003496  00                                       2442+          DC    X'00'
00003497  00                                       2443+          DC    HL1'0'                  m5 used
00003498  02                                       2444+          DC    HL1'2'                  m6 used
00003499  02                                       2445+          DC    HL1'2'             CC
0000349A  0D                                       2446+          DC    HL1'13'            CC failed mask
0000349C  00000000 00000000                        2447+          DS    2F                 extracted PSW after test (has CC)
000034A4  FF                                       2448+          DC    X'FF'              extracted CC, if test failed
000034A5  E5E2E3D9 E2404040                        2449+          DC    CL8'VSTRS'        instruction name
000034B0  00003534                                 2450+          DC    A(RE43+16)        address of v2 source
000034B4  00003544                                 2451+          DC    A(RE43+32)        address of v3 source
000034B8  00003554                                 2452+          DC    A(RE43+48)        address of v4 source
000034BC  00000010                                 2453+          DC    A(16)             result length
000034C0  00003524                                 2454+REA43     DC    A(RE43)           result address
000034C8  00000000 00000000                        2455+          DS    FD                gap
000034D0  00000000 00000000                        2456+V1O43     DS    XL16              V1 output
000034D8  00000000 00000000
000034E0  00000000 00000000                        2457+          DS    FD                gap
                                                   2458+*
000034E8                                           2459+X43       DS    0F
000034E8  E310 5020 0014                 00000020  2460+          LGF   R1,V2ADDR         load v2 source
000034EE  E761 0000 0806                 00000000  2461+          VL    v22,0(R1)         use v22 to test decoder
000034F4  E310 5024 0014                 00000024  2462+          LGF   R1,V3ADDR         load v3 source
000034FA  E771 0000 0806                 00000000  2463+          VL    v23,0(R1)         use v23 to test decoder
00003500  E310 5028 0014                 00000028  2464+          LGF   R1,V4ADDR         load v4 source
00003506  E781 0000 0806                 00000000  2465+          VL    v24,0(R1)         use v24 to test decoder
0000350C  E766 7020 8F8B                           2466+          VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00003512  B98D 0020                                2467+          EPSW  R2,R0              extract psw
00003516  5020 500C                      0000000C  2468+          ST    R2,CCPSW              to save CC
0000351A  E760 5040 080E                 000034D0  2469+          VST   V22,V1O43          save v1 output
00003520  07FB                                     2470+          BR    R11               return
00003524                                           2471+RE43      DC    0F                xl16 expected result
00003524                                           2472+          DROP  R5
00003524  00000000 00000006                        2473           DC    XL16'0000000000000006 0000000000000000'   V1
0000352C  00000000 00000000
00003534  F0F1F2F3 F4F50102                        2474           DC    XL16'F0F1F2F3F4F50102 0304FAFBFCFDFEFF'   v2
0000353C  0304FAFB FCFDFEFF
00003544  01020300 05060700                        2475           DC    XL16'0102030005060700 090A0B0C0D0E0F10'   v3
0000354C  090A0B0C 0D0E0F10
00003554  00000000 00000004                        2476           DC    XL16'0000000000000004 0000000000000000'   v4
0000355C  00000000 00000000
                                                   2477
                                                   2478 *Halfword
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2479           VRR_D VSTRS,1,2,2                                 full match
00003568                                           2480+          DS    0FD
00003568                      00003568             2481+          USING *,R5              base for test data and test routine
00003568  000035C0                                 2482+T44       DC    A(X44)            address of test routine
0000356C  002C                                     2483+          DC    H'44'             test number
0000356E  00                                       2484+          DC    X'00'
0000356F  01                                       2485+          DC    HL1'1'                  m5 used
00003570  02                                       2486+          DC    HL1'2'                  m6 used
00003571  02                                       2487+          DC    HL1'2'             CC
00003572  0D                                       2488+          DC    HL1'13'            CC failed mask
00003574  00000000 00000000                        2489+          DS    2F                 extracted PSW after test (has CC)
0000357C  FF                                       2490+          DC    X'FF'              extracted CC, if test failed
0000357D  E5E2E3D9 E2404040                        2491+          DC    CL8'VSTRS'        instruction name
00003588  0000360C                                 2492+          DC    A(RE44+16)        address of v2 source
0000358C  0000361C                                 2493+          DC    A(RE44+32)        address of v3 source
00003590  0000362C                                 2494+          DC    A(RE44+48)        address of v4 source
00003594  00000010                                 2495+          DC    A(16)             result length
00003598  000035FC                                 2496+REA44     DC    A(RE44)           result address
000035A0  00000000 00000000                        2497+          DS    FD                gap
000035A8  00000000 00000000                        2498+V1O44     DS    XL16              V1 output
000035B0  00000000 00000000
000035B8  00000000 00000000                        2499+          DS    FD                gap
                                                   2500+*
000035C0                                           2501+X44       DS    0F
000035C0  E310 5020 0014                 00000020  2502+          LGF   R1,V2ADDR         load v2 source
000035C6  E761 0000 0806                 00000000  2503+          VL    v22,0(R1)         use v22 to test decoder
000035CC  E310 5024 0014                 00000024  2504+          LGF   R1,V3ADDR         load v3 source
000035D2  E771 0000 0806                 00000000  2505+          VL    v23,0(R1)         use v23 to test decoder
000035D8  E310 5028 0014                 00000028  2506+          LGF   R1,V4ADDR         load v4 source
000035DE  E781 0000 0806                 00000000  2507+          VL    v24,0(R1)         use v24 to test decoder
000035E4  E766 7120 8F8B                           2508+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
000035EA  B98D 0020                                2509+          EPSW  R2,R0              extract psw
000035EE  5020 500C                      0000000C  2510+          ST    R2,CCPSW              to save CC
000035F2  E760 5040 080E                 000035A8  2511+          VST   V22,V1O44          save v1 output
000035F8  07FB                                     2512+          BR    R11               return
000035FC                                           2513+RE44      DC    0F                xl16 expected result
000035FC                                           2514+          DROP  R5
000035FC  00000000 00000006                        2515           DC    XL16'0000000000000006 0000000000000000'   V1
00003604  00000000 00000000
0000360C  F0F1F2F3 F4F50102                        2516           DC    XL16'F0F1F2F3F4F50102 0304FAFBFCFDFEFF'   v2
00003614  0304FAFB FCFDFEFF
0000361C  01020000 05060000                        2517           DC    XL16'0102000005060000 090A0B0C0D0E0F10'   v3
00003624  090A0B0C 0D0E0F10
0000362C  00000000 00000004                        2518           DC    XL16'0000000000000004 0000000000000000'   v4
00003634  00000000 00000000
                                                   2519
                                                   2520 *Word
                                                   2521           VRR_D VSTRS,2,2,2                               full match
00003640                                           2522+          DS    0FD
00003640                      00003640             2523+          USING *,R5              base for test data and test routine
00003640  00003698                                 2524+T45       DC    A(X45)            address of test routine
00003644  002D                                     2525+          DC    H'45'             test number
00003646  00                                       2526+          DC    X'00'
00003647  02                                       2527+          DC    HL1'2'                  m5 used
00003648  02                                       2528+          DC    HL1'2'                  m6 used
00003649  02                                       2529+          DC    HL1'2'             CC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000364A  0D                                      2530+          DC    HL1'13'            CC failed mask
0000364C  00000000 00000000                       2531+          DS    2F                 extracted PSW after test (has CC)
00003654  FF                                      2532+          DC    X'FF'              extracted CC, if test failed
00003655  E5E2E3D9 E2404040                       2533+          DC    CL8'VSTRS'        instruction name
00003660  000036E4                                2534+          DC    A(RE45+16)        address of v2 source
00003664  000036F4                                2535+          DC    A(RE45+32)        address of v3 source
00003668  00003704                                2536+          DC    A(RE45+48)        address of v4 source
0000366C  00000010                                2537+          DC    A(16)             result length
00003670  000036D4                                2538+REA45     DC    A(RE45)           result address
00003678  00000000 00000000                       2539+          DS    FD                gap
00003680  00000000 00000000                       2540+V1045     DS    XL16              V1 output
00003688  00000000 00000000
00003690  00000000 00000000                       2541+          DS    FD                gap
                                                  2542+*
00003698                                          2543+X45       DS    0F
00003698  E310 5020 0014                 00000020 2544+          LGF   R1,V2ADDR         load v2 source
0000369E  E761 0000 0806                 00000000 2545+          VL    v22,0(R1)         use v22 to test decoder
000036A4  E310 5024 0014                 00000024 2546+          LGF   R1,V3ADDR         load v3 source
000036AA  E771 0000 0806                 00000000 2547+          VL    v23,0(R1)         use v23 to test decoder
000036B0  E310 5028 0014                 00000028 2548+          LGF   R1,V4ADDR         load v4 source
000036B6  E781 0000 0806                 00000000 2549+          VL    v24,0(R1)         use v24 to test decoder
000036BC  E766 7220 8F8B                          2550+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
000036C2  B98D 0020                               2551+          EPSW  R2,R0              extract psw
000036C6  5020 500C                      0000000C 2552+          ST    R2,CCPSW              to save CC
000036CA  E760 5040 080E                 00003680 2553+          VST   V22,V1045          save v1 output
000036D0  07FB                                    2554+          BR    R11               return
000036D4                                          2555+RE45      DC    0F                xl16 expected result
000036D4                                          2556+          DROP  R5
000036D4  00000000 00000004                       2557           DC    XL16'0000000000000004 0000000000000000'   V1
000036DC  00000000 00000000
000036E4  F0F1F2F3 01020304                       2558           DC    XL16'F0F1F2F301020304 F4F5FAFBFCFDFEFF'   v2
000036EC  F4F5FAFB FCFDFEFF
000036F4  01020304 00000000                       2559           DC    XL16'0102030400000000 000000000D0E0F10'   v3
000036FC  00000000 0D0E0F10
00003704  00000000 00000004                       2560           DC    XL16'0000000000000004 0000000000000000'   v4
0000370C  00000000 00000000
                                                  2561
                                                  2562 *Full Match: at beginning of vector (and at end of vector)
                                                  2563 *Byte
                                                  2564           VRR_D VSTRS,0,2,2                               full match
00003718                                          2565+          DS    0FD
00003718                 00003718                 2566+          USING *,R5              base for test data and test routine
00003718  00003770                                2567+T46       DC    A(X46)            address of test routine
0000371C  002E                                    2568+          DC    H'46'             test number
0000371E  00                                      2569+          DC    X'00'
0000371F  00                                      2570+          DC    HL1'0'                 m5 used
00003720  02                                      2571+          DC    HL1'2'                 m6 used
00003721  02                                      2572+          DC    HL1'2'             CC
00003722  0D                                      2573+          DC    HL1'13'            CC failed mask
00003724  00000000 00000000                       2574+          DS    2F                 extracted PSW after test (has CC)
0000372C  FF                                      2575+          DC    X'FF'              extracted CC, if test failed
0000372D  E5E2E3D9 E2404040                       2576+          DC    CL8'VSTRS'        instruction name
00003738  000037BC                                2577+          DC    A(RE46+16)        address of v2 source
0000373C  000037CC                                2578+          DC    A(RE46+32)        address of v3 source
00003740  000037DC                                2579+          DC    A(RE46+48)        address of v4 source
00003744  00000010                                2580+          DC    A(16)             result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003748  000037AC                        2581+REA46    DC    A(RE46)           result address
00003750  00000000 00000000               2582+         DS    FD                gap
00003758  00000000 00000000               2583+V1O46    DS    XL16              V1 output
00003760  00000000 00000000
00003768  00000000 00000000               2584+         DS    FD                gap
                                          2585+*
00003770                                  2586+X46      DS    0F
00003770  E310 5020 0014          00000020 2587+         LGF   R1,V2ADDR         load v2 source
00003776  E761 0000 0806          00000000 2588+         VL    v22,0(R1)         use v22 to test decoder
0000377C  E310 5024 0014          00000024 2589+         LGF   R1,V3ADDR         load v3 source
00003782  E771 0000 0806          00000000 2590+         VL    v23,0(R1)         use v23 to test decoder
00003788  E310 5028 0014          00000028 2591+         LGF   R1,V4ADDR         load v4 source
0000378E  E781 0000 0806          00000000 2592+         VL    v24,0(R1)         use v24 to test decoder
00003794  E766 7020 8F8B                   2593+         VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
0000379A  B98D 0020                        2594+         EPSW  R2,R0              extract psw
0000379E  5020 500C               0000000C 2595+         ST    R2,CCPSW              to save CC
000037A2  E760 5040 080E          00003758 2596+         VST   V22,V1O46          save v1 output
000037A8  07FB                             2597+         BR    R11               return
000037AC                                   2598+RE46     DC    0F                xl16 expected result
000037AC                                   2599+         DROP  R5
000037AC  00000000 00000000               2600          DC    XL16'0000000000000000 0000000000000000'   V1
000037B4  00000000 00000000
000037BC  01020304 F4F5F6F7               2601          DC    XL16'01020304F4F5F6F7 AAFDFEFF01020304'   v2
000037C4  AAFDFEFF 01020304
000037CC  01020300 05060700               2602          DC    XL16'0102030005060700 090A0B0C0D0E0F10'   v3
000037D4  090A0B0C 0D0E0F10
000037DC  00000000 00000004               2603          DC    XL16'0000000000000004 0000000000000000'   v4
000037E4  00000000 00000000
                                          2604
                                          2605 *Halfword
                                          2606          VRR_D VSTRS,1,2,2                               full match
000037F0                                  2607+         DS    0FD
000037F0                        000037F0  2608+         USING *,R5              base for test data and test routine
000037F0  00003848                        2609+T47      DC    A(X47)            address of test routine
000037F4  002F                            2610+         DC    H'47'             test number
000037F6  00                              2611+         DC    X'00'
000037F7  01                              2612+         DC    HL1'1'                  m5 used
000037F8  02                              2613+         DC    HL1'2'                  m6 used
000037F9  02                              2614+         DC    HL1'2'             CC
000037FA  0D                              2615+         DC    HL1'13'            CC failed mask
000037FC  00000000 00000000               2616+         DS    2F                 extracted PSW after test (has CC)
00003804  FF                              2617+         DC    X'FF'              extracted CC, if test failed
00003805  E5E2E3D9 E2404040               2618+         DC    CL8'VSTRS'        instruction name
00003810  00003894                        2619+         DC    A(RE47+16)        address of v2 source
00003814  000038A4                        2620+         DC    A(RE47+32)        address of v3 source
00003818  000038B4                        2621+         DC    A(RE47+48)        address of v4 source
0000381C  00000010                        2622+         DC    A(16)             result length
00003820  00003884                        2623+REA47    DC    A(RE47)           result address
00003828  00000000 00000000               2624+         DS    FD                gap
00003830  00000000 00000000               2625+V1O47    DS    XL16              V1 output
00003838  00000000 00000000
00003840  00000000 00000000               2626+         DS    FD                gap
                                          2627+*
00003848                                  2628+X47      DS    0F
00003848  E310 5020 0014          00000020 2629+         LGF   R1,V2ADDR         load v2 source
0000384E  E761 0000 0806          00000000 2630+         VL    v22,0(R1)         use v22 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003854  E310 5024 0014                 00000024  2631+          LGF    R1,V3ADDR          load v3 source
0000385A  E771 0000 0806                 00000000  2632+          VL     v23,0(R1)          use v23 to test decoder
00003860  E310 5028 0014                 00000028  2633+          LGF    R1,V4ADDR          load v4 source
00003866  E781 0000 0806                 00000000  2634+          VL     v24,0(R1)          use v24 to test decoder
0000386C  E766 7120 8F8B                           2635+          VSTRS  V22,V22,V23,V24,1,2      instruction (dest is a source)
00003872  B98D 0020                                2636+          EPSW   R2,R0               extract psw
00003876  5020 500C                      0000000C  2637+          ST     R2,CCPSW               to save CC
0000387A  E760 5040 080E                 00003830  2638+          VST    V22,V1O47           save v1 output
00003880  07FB                                     2639+          BR     R11                return
00003884                                           2640+RE47      DC     0F                 xl16 expected result
00003884                                           2641+          DROP   R5
00003884  00000000 00000000                        2642           DC     XL16'0000000000000000 0000000000000000'   V1
0000388C  00000000 00000000
00003894  01020304 F4F5F6F7                        2643           DC     XL16'01020304F4F5F6F7 AAFDFEFF01020304'   v2
0000389C  AAFDFEFF 01020304
000038A4  01020000 05060000                        2644           DC     XL16'0102000005060000 090A0B0C0D0E0F10'   v3
000038AC  090A0B0C 0D0E0F10
000038B4  00000000 00000004                        2645           DC     XL16'0000000000000004 0000000000000000'   v4
000038BC  00000000 00000000
                                                   2646
                                                   2647 *Word
                                                   2648           VRR_D  VSTRS,2,2,2                               full match
000038C8                                           2649+          DS     0FD
000038C8                         000038C8          2650+          USING  *,R5               base for test data and test routine
000038C8  00003920                                 2651+T48       DC     A(X48)             address of test routine
000038CC  0030                                     2652+          DC     H'48'              test number
000038CE  00                                       2653+          DC     X'00'
000038CF  02                                       2654+          DC     HL1'2'                   m5 used
000038D0  02                                       2655+          DC     HL1'2'                   m6 used
000038D1  02                                       2656+          DC     HL1'2'              CC
000038D2  0D                                       2657+          DC     HL1'13'             CC failed mask
000038D4  00000000 00000000                        2658+          DS     2F                  extracted PSW after test (has CC)
000038DC  FF                                       2659+          DC     X'FF'               extracted CC, if test failed
000038DD  E5E2E3D9 E2404040                        2660+          DC     CL8'VSTRS'         instruction name
000038E8  0000396C                                 2661+          DC     A(RE48+16)         address of v2 source
000038EC  0000397C                                 2662+          DC     A(RE48+32)         address of v3 source
000038F0  0000398C                                 2663+          DC     A(RE48+48)         address of v4 source
000038F4  00000010                                 2664+          DC     A(16)              result length
000038F8  0000395C                                 2665+REA48     DC     A(RE48)            result address
00003900  00000000 00000000                        2666+          DS     FD                 gap
00003908  00000000 00000000                        2667+V1O48     DS     XL16               V1 output
00003910  00000000 00000000
00003918  00000000 00000000                        2668+          DS     FD                 gap
                                                   2669+*
00003920                                           2670+X48       DS     0F
00003920  E310 5020 0014                 00000020  2671+          LGF    R1,V2ADDR          load v2 source
00003926  E761 0000 0806                 00000000  2672+          VL     v22,0(R1)          use v22 to test decoder
0000392C  E310 5024 0014                 00000024  2673+          LGF    R1,V3ADDR          load v3 source
00003932  E771 0000 0806                 00000000  2674+          VL     v23,0(R1)          use v23 to test decoder
00003938  E310 5028 0014                 00000028  2675+          LGF    R1,V4ADDR          load v4 source
0000393E  E781 0000 0806                 00000000  2676+          VL     v24,0(R1)          use v24 to test decoder
00003944  E766 7220 8F8B                           2677+          VSTRS  V22,V22,V23,V24,2,2      instruction (dest is a source)
0000394A  B98D 0020                                2678+          EPSW   R2,R0               extract psw
0000394E  5020 500C                      0000000C  2679+          ST     R2,CCPSW               to save CC
00003952  E760 5040 080E                 00003908  2680+          VST    V22,V1O48           save v1 output
00003958  07FB                                     2681+          BR     R11                return
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000395C                                          2682+RE48     DC    0F                xl16 expected result
0000395C                                          2683+         DROP  R5
0000395C  00000000 00000000                       2684          DC    XL16'0000000000000000 0000000000000000'   V1
00003964  00000000 00000000
0000396C  01020304 F4F5F6F7                       2685          DC    XL16'01020304F4F5F6F7 AAFDFEFF01020304'   v2
00003974  AAFDFEFF 01020304
0000397C  01020304 00000000                       2686          DC    XL16'0102030400000000 000000000D0E0F10'   v3
00003984  00000000 0D0E0F10
0000398C  00000000 00000004                       2687          DC    XL16'0000000000000004 0000000000000000'   v4
00003994  00000000 00000000
                                                  2688
                                                  2689 *Full Match: at beginning of vector (and partial at end of vector)
                                                  2690 *Byte
                                                  2691          VRR_D VSTRS,0,2,2                               full match
000039A0                                          2692+         DS    0FD
000039A0                          000039A0        2693+         USING *,R5              base for test data and test routine
000039A0  000039F8                                2694+T49      DC    A(X49)            address of test routine
000039A4  0031                                    2695+         DC    H'49'             test number
000039A6  00                                      2696+         DC    X'00'
000039A7  00                                      2697+         DC    HL1'0'                  m5 used
000039A8  02                                      2698+         DC    HL1'2'                  m6 used
000039A9  02                                      2699+         DC    HL1'2'             CC
000039AA  0D                                      2700+         DC    HL1'13'            CC failed mask
000039AC  00000000 00000000                       2701+         DS    2F                 extracted PSW after test (has CC)
000039B4  FF                                      2702+         DC    X'FF'              extracted CC, if test failed
000039B5  E5E2E3D9 E2404040                       2703+         DC    CL8'VSTRS'        instruction name
000039C0  00003A44                                2704+         DC    A(RE49+16)        address of v2 source
000039C4  00003A54                                2705+         DC    A(RE49+32)        address of v3 source
000039C8  00003A64                                2706+         DC    A(RE49+48)        address of v4 source
000039CC  00000010                                2707+         DC    A(16)             result length
000039D0  00003A34                                2708+REA49    DC    A(RE49)           result address
000039D8  00000000 00000000                       2709+         DS    FD                gap
000039E0  00000000 00000000                       2710+V1049    DS    XL16              V1 output
000039E8  00000000 00000000
000039F0  00000000 00000000                       2711+         DS    FD                gap
                                                  2712+*
000039F8                                          2713+X49      DS    0F
000039F8  E310 5020 0014              00000020    2714+         LGF   R1,V2ADDR         load v2 source
000039FE  E761 0000 0806              00000000    2715+         VL    v22,0(R1)         use v22 to test decoder
00003A04  E310 5024 0014              00000024    2716+         LGF   R1,V3ADDR         load v3 source
00003A0A  E771 0000 0806              00000000    2717+         VL    v23,0(R1)         use v23 to test decoder
00003A10  E310 5028 0014              00000028    2718+         LGF   R1,V4ADDR         load v4 source
00003A16  E781 0000 0806              00000000    2719+         VL    v24,0(R1)         use v24 to test decoder
00003A1C  E766 7020 8F8B                          2720+         VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00003A22  B98D 0020                               2721+         EPSW  R2,R0              extract psw
00003A26  5020 500C                   0000000C    2722+         ST    R2,CCPSW              to save CC
00003A2A  E760 5040 080E              000039E0    2723+         VST   V22,V1049          save v1 output
00003A30  07FB                                    2724+         BR    R11               return
00003A34                                          2725+RE49     DC    0F                xl16 expected result
00003A34                                          2726+         DROP  R5
00003A34  00000000 00000000                       2727          DC    XL16'0000000000000000 0000000000000000'   V1
00003A3C  00000000 00000000
00003A44  01020304 F4F5F6F7                       2728          DC    XL16'01020304F4F5F6F7 AAFDFEFFBB010203'   v2
00003A4C  AAFDFEFF BB010203
00003A54  01020300 05060700                       2729          DC    XL16'0102030005060700 090A0B0C0D0E0F10'   v3
00003A5C  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003A64  00000000 00000004                        2730           DC    XL16'0000000000000004 0000000000000000'   v4
00003A6C  00000000 00000000
                                                   2731
                                                   2732 *Halfword
                                                   2733           VRR_D VSTRS,1,2,2                               full match
00003A78                                           2734+          DS    0FD
00003A78                     00003A78              2735+          USING *,R5              base for test data and test routine
00003A78  00003AD0                                 2736+T50       DC    A(X50)            address of test routine
00003A7C  0032                                     2737+          DC    H'50'             test number
00003A7E  00                                       2738+          DC    X'00'
00003A7F  01                                       2739+          DC    HL1'1'                  m5 used
00003A80  02                                       2740+          DC    HL1'2'                  m6 used
00003A81  02                                       2741+          DC    HL1'2'             CC
00003A82  0D                                       2742+          DC    HL1'13'            CC failed mask
00003A84  00000000 00000000                        2743+          DS    2F                 extracted PSW after test (has CC)
00003A8C  FF                                       2744+          DC    X'FF'              extracted CC, if test failed
00003A8D  E5E2E3D9 E2404040                        2745+          DC    CL8'VSTRS'        instruction name
00003A98  00003B1C                                 2746+          DC    A(RE50+16)        address of v2 source
00003A9C  00003B2C                                 2747+          DC    A(RE50+32)        address of v3 source
00003AA0  00003B3C                                 2748+          DC    A(RE50+48)        address of v4 source
00003AA4  00000010                                 2749+          DC    A(16)             result length
00003AA8  00003B0C                                 2750+REA50     DC    A(RE50)           result address
00003AB0  00000000 00000000                        2751+          DS    FD                gap
00003AB8  00000000 00000000                        2752+V1O50     DS    XL16              V1 output
00003AC0  00000000 00000000
00003AC8  00000000 00000000                        2753+          DS    FD                gap
                                                   2754+*
00003AD0                                           2755+X50       DS    0F
00003AD0  E310 5020 0014                 00000020  2756+          LGF   R1,V2ADDR         load v2 source
00003AD6  E761 0000 0806                 00000000  2757+          VL    v22,0(R1)         use v22 to test decoder
00003ADC  E310 5024 0014                 00000024  2758+          LGF   R1,V3ADDR         load v3 source
00003AE2  E771 0000 0806                 00000000  2759+          VL    v23,0(R1)         use v23 to test decoder
00003AE8  E310 5028 0014                 00000028  2760+          LGF   R1,V4ADDR         load v4 source
00003AEE  E781 0000 0806                 00000000  2761+          VL    v24,0(R1)         use v24 to test decoder
00003AF4  E766 7120 8F8B                           2762+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00003AFA  B98D 0020                                2763+          EPSW  R2,R0              extract psw
00003AFE  5020 500C                      0000000C  2764+          ST    R2,CCPSW              to save CC
00003B02  E760 5040 080E                 00003AB8  2765+          VST   V22,V1O50          save v1 output
00003B08  07FB                                     2766+          BR    R11               return
00003B0C                                           2767+RE50      DC    0F                xl16 expected result
00003B0C                                           2768+          DROP  R5
00003B0C  00000000 00000000                        2769           DC    XL16'0000000000000000 0000000000000000'   V1
00003B14  00000000 00000000
00003B1C  01020304 F4F5F6F7                        2770           DC    XL16'01020304F4F5F6F7 AAFDFEFFBBBB0102'   v2
00003B24  AAFDFEFF BBBB0102
00003B2C  01020000 05060000                        2771           DC    XL16'0102000005060000 090A0B0C0D0E0F10'   v3
00003B34  090A0B0C 0D0E0F10
00003B3C  00000000 00000004                        2772           DC    XL16'0000000000000004 0000000000000000'   v4
00003B44  00000000 00000000
                                                   2773
                                                   2774 *Word
                                                   2775           VRR_D VSTRS,2,2,2                               full match
00003B50                                           2776+          DS    0FD
00003B50                     00003B50              2777+          USING *,R5              base for test data and test routine
00003B50  00003BA8                                 2778+T51       DC    A(X51)            address of test routine
00003B54  0033                                     2779+          DC    H'51'             test number
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003B56  00                               2780+          DC    X'00'
00003B57  02                               2781+          DC    HL1'2'                  m5 used
00003B58  02                               2782+          DC    HL1'2'                  m6 used
00003B59  02                               2783+          DC    HL1'2'              CC
00003B5A  0D                               2784+          DC    HL1'13'             CC failed mask
00003B5C  00000000 00000000                2785+          DS    2F                  extracted PSW after test (has CC)
00003B64  FF                               2786+          DC    X'FF'               extracted CC, if test failed
00003B65  E5E2E3D9 E2404040                2787+          DC    CL8'VSTRS'          instruction name
00003B70  00003BF4                         2788+          DC    A(RE51+16)          address of v2 source
00003B74  00003C04                         2789+          DC    A(RE51+32)          address of v3 source
00003B78  00003C14                         2790+          DC    A(RE51+48)          address of v4 source
00003B7C  00000010                         2791+          DC    A(16)               result length
00003B80  00003BE4                         2792+REA51     DC    A(RE51)             result address
00003B88  00000000 00000000                2793+          DS    FD                  gap
00003B90  00000000 00000000                2794+V1O51     DS    XL16                V1 output
00003B98  00000000 00000000
00003BA0  00000000 00000000                2795+          DS    FD                  gap
                                           2796+*
00003BA8                                   2797+X51       DS    0F
00003BA8  E310 5020 0014          00000020 2798+          LGF   R1,V2ADDR           load v2 source
00003BAE  E761 0000 0806          00000000 2799+          VL    v22,0(R1)           use v22 to test decoder
00003BB4  E310 5024 0014          00000024 2800+          LGF   R1,V3ADDR           load v3 source
00003BBA  E771 0000 0806          00000000 2801+          VL    v23,0(R1)           use v23 to test decoder
00003BC0  E310 5028 0014          00000028 2802+          LGF   R1,V4ADDR           load v4 source
00003BC6  E781 0000 0806          00000000 2803+          VL    v24,0(R1)           use v24 to test decoder
00003BCC  E766 7220 8F8B                   2804+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00003BD2  B98D 0020                        2805+          EPSW  R2,R0                extract psw
00003BD6  5020 500C               0000000C 2806+          ST    R2,CCPSW                to save CC
00003BDA  E760 5040 080E          00003B90 2807+          VST   V22,V1O51           save v1 output
00003BE0  07FB                             2808+          BR    R11                 return
00003BE4                                   2809+RE51      DC    0F                  xl16 expected result
00003BE4                                   2810+          DROP  R5
00003BE4  00000000 00000000                2811           DC    XL16'0000000000000000 0000000000000000'   V1
00003BEC  00000000 00000000
00003BF4  01020304 05060708                2812           DC    XL16'0102030405060708 AAFDFEFF01020304'   v2
00003BFC  AAFDFEFF 01020304
00003C04  01020304 00000000                2813           DC    XL16'0102030400000000 000000000D0E0F10'   v3
00003C0C  00000000 0D0E0F10
00003C14  00000000 00000008                2814           DC    XL16'0000000000000008 0000000000000000'   v4
00003C1C  00000000 00000000
                                           2815
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2817 *-------------------------------------------------------------------
                                                   2818 * case 4 - full match; V2 str length from ZS: ZS=1 CC=2
                                                   2819 *-------------------------------------------------------------------
                                                   2820 *Full Match: at beginning of vector
                                                   2821 *Byte
                                                   2822          VRR_D VSTRS,0,2,2                              full match
00003C28                                           2823+         DS    0FD
00003C28                          00003C28         2824+         USING *,R5              base for test data and test routine
00003C28  00003C80                                 2825+T52      DC    A(X52)            address of test routine
00003C2C  0034                                     2826+         DC    H'52'             test number
00003C2E  00                                       2827+         DC    X'00'
00003C2F  00                                       2828+         DC    HL1'0'                  m5 used
00003C30  02                                       2829+         DC    HL1'2'                  m6 used
00003C31  02                                       2830+         DC    HL1'2'             CC
00003C32  0D                                       2831+         DC    HL1'13'            CC failed mask
00003C34  00000000 00000000                        2832+         DS    2F                 extracted PSW after test (has CC)
00003C3C  FF                                       2833+         DC    X'FF'              extracted CC, if test failed
00003C3D  E5E2E3D9 E2404040                        2834+         DC    CL8'VSTRS'        instruction name
00003C48  00003CCC                                 2835+         DC    A(RE52+16)        address of v2 source
00003C4C  00003CDC                                 2836+         DC    A(RE52+32)        address of v3 source
00003C50  00003CEC                                 2837+         DC    A(RE52+48)        address of v4 source
00003C54  00000010                                 2838+         DC    A(16)             result length
00003C58  00003CBC                                 2839+REA52    DC    A(RE52)           result address
00003C60  00000000 00000000                        2840+         DS    FD                gap
00003C68  00000000 00000000                        2841+V1O52    DS    XL16              V1 output
00003C70  00000000 00000000
00003C78  00000000 00000000                        2842+         DS    FD                gap
                                                   2843+*
00003C80                                           2844+X52      DS    0F
00003C80  E310 5020 0014                 00000020  2845+         LGF   R1,V2ADDR         load v2 source
00003C86  E761 0000 0806                 00000000  2846+         VL    v22,0(R1)         use v22 to test decoder
00003C8C  E310 5024 0014                 00000024  2847+         LGF   R1,V3ADDR         load v3 source
00003C92  E771 0000 0806                 00000000  2848+         VL    v23,0(R1)         use v23 to test decoder
00003C98  E310 5028 0014                 00000028  2849+         LGF   R1,V4ADDR         load v4 source
00003C9E  E781 0000 0806                 00000000  2850+         VL    v24,0(R1)         use v24 to test decoder
00003CA4  E766 7020 8F8B                           2851+         VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00003CAA  B98D 0020                                2852+         EPSW  R2,R0              extract psw
00003CAE  5020 500C                      0000000C  2853+         ST    R2,CCPSW              to save CC
00003CB2  E760 5040 080E                 00003C68  2854+         VST   V22,V1O52          save v1 output
00003CB8  07FB                                     2855+         BR    R11               return
00003CBC                                           2856+RE52     DC    0F                xl16 expected result
00003CBC                                           2857+         DROP  R5
00003CBC  00000000 00000000                        2858          DC    XL16'0000000000000000 0000000000000000'   V1
00003CC4  00000000 00000000
00003CCC  01020304 F4F5F6F7                        2859          DC    XL16'01020304F4F5F6F7 00020304AAFDFEFF'   v2
00003CD4  00020304 AAFDFEFF
00003CDC  01020300 05060700                        2860          DC    XL16'0102030005060700 090A0B0C0D0E0F10'   v3
00003CE4  090A0B0C 0D0E0F10
00003CEC  00000000 00000004                        2861          DC    XL16'0000000000000004 0000000000000000'   v4
00003CF4  00000000 00000000
                                                   2862
                                                   2863 *Halfword
                                                   2864          VRR_D VSTRS,1,2,2                              full match
00003D00                                           2865+         DS    0FD
00003D00                          00003D00         2866+         USING *,R5              base for test data and test routine
00003D00  00003D58                                 2867+T53      DC    A(X53)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003D04  0035                                     2868+          DC    H'53'              test number
00003D06  00                                       2869+          DC    X'00'
00003D07  01                                       2870+          DC    HL1'1'                   m5 used
00003D08  02                                       2871+          DC    HL1'2'                   m6 used
00003D09  02                                       2872+          DC    HL1'2'              CC
00003D0A  0D                                       2873+          DC    HL1'13'             CC failed mask
00003D0C  00000000 00000000                        2874+          DS    2F                  extracted PSW after test (has CC)
00003D14  FF                                       2875+          DC    X'FF'               extracted CC, if test failed
00003D15  E5E2E3D9 E2404040                        2876+          DC    CL8'VSTRS'          instruction name
00003D20  00003DA4                                 2877+          DC    A(RE53+16)          address of v2 source
00003D24  00003DB4                                 2878+          DC    A(RE53+32)          address of v3 source
00003D28  00003DC4                                 2879+          DC    A(RE53+48)          address of v4 source
00003D2C  00000010                                 2880+          DC    A(16)               result length
00003D30  00003D94                                 2881+REA53     DC    A(RE53)             result address
00003D38  00000000 00000000                        2882+          DS    FD                  gap
00003D40  00000000 00000000                        2883+V1O53     DS    XL16                V1 output
00003D48  00000000 00000000
00003D50  00000000 00000000                        2884+          DS    FD                  gap
                                                   2885+*
00003D58                                           2886+X53       DS    0F
00003D58  E310 5020 0014                 00000020  2887+          LGF   R1,V2ADDR           load v2 source
00003D5E  E761 0000 0806                 00000000  2888+          VL    v22,0(R1)           use v22 to test decoder
00003D64  E310 5024 0014                 00000024  2889+          LGF   R1,V3ADDR           load v3 source
00003D6A  E771 0000 0806                 00000000  2890+          VL    v23,0(R1)           use v23 to test decoder
00003D70  E310 5028 0014                 00000028  2891+          LGF   R1,V4ADDR           load v4 source
00003D76  E781 0000 0806                 00000000  2892+          VL    v24,0(R1)           use v24 to test decoder
00003D7C  E766 7120 8F8B                           2893+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00003D82  B98D 0020                                2894+          EPSW  R2,R0               extract psw
00003D86  5020 500C                      0000000C  2895+          ST    R2,CCPSW               to save CC
00003D8A  E760 5040 080E                 00003D40  2896+          VST   V22,V1O53           save v1 output
00003D90  07FB                                     2897+          BR    R11                 return
00003D94                                           2898+RE53      DC    0F                  xl16 expected result
00003D94                                           2899+          DROP  R5
00003D94  00000000 00000000                        2900           DC    XL16'0000000000000000 0000000000000000'   V1
00003D9C  00000000 00000000
00003DA4  01020304 F4F5F6F7                        2901           DC    XL16'01020304F4F5F6F7 00000304AAFDFEFF'   v2
00003DAC  00000304 AAFDFEFF
00003DB4  01020000 05060000                        2902           DC    XL16'0102000005060000 090A0B0C0D0E0F10'   v3
00003DBC  090A0B0C 0D0E0F10
00003DC4  00000000 00000004                        2903           DC    XL16'0000000000000004 0000000000000000'   v4
00003DCC  00000000 00000000
                                                   2904
                                                   2905 *Word
                                                   2906           VRR_D VSTRS,2,2,2                               full match
00003DD8                                           2907+          DS    0FD
00003DD8                       00003DD8            2908+          USING *,R5                base for test data and test routine
00003DD8  00003E30                                 2909+T54       DC    A(X54)              address of test routine
00003DDC  0036                                     2910+          DC    H'54'               test number
00003DDE  00                                       2911+          DC    X'00'
00003DDF  02                                       2912+          DC    HL1'2'                   m5 used
00003DE0  02                                       2913+          DC    HL1'2'                   m6 used
00003DE1  02                                       2914+          DC    HL1'2'              CC
00003DE2  0D                                       2915+          DC    HL1'13'             CC failed mask
00003DE4  00000000 00000000                        2916+          DS    2F                  extracted PSW after test (has CC)
00003DEC  FF                                       2917+          DC    X'FF'               extracted CC, if test failed
00003DED  E5E2E3D9 E2404040                        2918+          DC    CL8'VSTRS'          instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003DF8  00003E7C                          2919+          DC    A(RE54+16)        address of v2 source
00003DFC  00003E8C                          2920+          DC    A(RE54+32)        address of v3 source
00003E00  00003E9C                          2921+          DC    A(RE54+48)        address of v4 source
00003E04  00000010                          2922+          DC    A(16)             result length
00003E08  00003E6C                          2923+REA54     DC    A(RE54)           result address
00003E10  00000000 00000000                 2924+          DS    FD                gap
00003E18  00000000 00000000                 2925+V1O54     DS    XL16              V1 output
00003E20  00000000 00000000
00003E28  00000000 00000000                 2926+          DS    FD                gap
                                            2927+*
00003E30                                    2928+X54       DS    0F
00003E30  E310 5020 0014                00000020  2929+          LGF   R1,V2ADDR         load v2 source
00003E36  E761 0000 0806                00000000  2930+          VL    v22,0(R1)         use v22 to test decoder
00003E3C  E310 5024 0014                00000024  2931+          LGF   R1,V3ADDR         load v3 source
00003E42  E771 0000 0806                00000000  2932+          VL    v23,0(R1)         use v23 to test decoder
00003E48  E310 5028 0014                00000028  2933+          LGF   R1,V4ADDR         load v4 source
00003E4E  E781 0000 0806                00000000  2934+          VL    v24,0(R1)         use v24 to test decoder
00003E54  E766 7220 8F8B                          2935+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00003E5A  B98D 0020                               2936+          EPSW  R2,R0              extract psw
00003E5E  5020 500C                     0000000C  2937+          ST    R2,CCPSW              to save CC
00003E62  E760 5040 080E                00003E18  2938+          VST   V22,V1O54          save v1 output
00003E68  07FB                                    2939+          BR    R11               return
00003E6C                                          2940+RE54      DC    0F                xl16 expected result
00003E6C                                          2941+          DROP  R5
00003E6C  00000000 00000000                       2942           DC    XL16'0000000000000000 0000000000000000'   V1
00003E74  00000000 00000000
00003E7C  01020304 F4F5F6F7                       2943           DC    XL16'01020304F4F5F6F7 0000000005AAAAFF'   v2
00003E84  00000000 05AAAAFF
00003E8C  01020304 00000000                       2944           DC    XL16'0102030400000000 000000000D0E0F10'   v3
00003E94  00000000 0D0E0F10
00003E9C  00000000 00000004                       2945           DC    XL16'0000000000000004 0000000000000000'   v4
00003EA4  00000000 00000000
                                                  2946
                                                  2947 *Full Match: at middle of vector
                                                  2948 *Byte
                                                  2949           VRR_D VSTRS,0,2,2                               full match
00003EB0                                          2950+          DS    0FD
00003EB0                        00003EB0          2951+          USING *,R5              base for test data and test routine
00003EB0  00003F08                                2952+T55       DC    A(X55)            address of test routine
00003EB4  0037                                    2953+          DC    H'55'             test number
00003EB6  00                                      2954+          DC    X'00'
00003EB7  00                                      2955+          DC    HL1'0'                  m5 used
00003EB8  02                                      2956+          DC    HL1'2'                  m6 used
00003EB9  02                                      2957+          DC    HL1'2'             CC
00003EBA  0D                                      2958+          DC    HL1'13'            CC failed mask
00003EBC  00000000 00000000                       2959+          DS    2F                 extracted PSW after test (has CC)
00003EC4  FF                                      2960+          DC    X'FF'              extracted CC, if test failed
00003EC5  E5E2E3D9 E2404040                       2961+          DC    CL8'VSTRS'        instruction name
00003ED0  00003F54                                2962+          DC    A(RE55+16)        address of v2 source
00003ED4  00003F64                                2963+          DC    A(RE55+32)        address of v3 source
00003ED8  00003F74                                2964+          DC    A(RE55+48)        address of v4 source
00003EDC  00000010                                2965+          DC    A(16)             result length
00003EE0  00003F44                                2966+REA55     DC    A(RE55)           result address
00003EE8  00000000 00000000                       2967+          DS    FD                gap
00003EF0  00000000 00000000                       2968+V1O55     DS    XL16              V1 output
00003EF8  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003F00  00000000 00000000                        2969+          DS    FD                gap
                                                   2970+*
00003F08                                           2971+X55       DS    0F
00003F08  E310 5020 0014                 00000020  2972+          LGF   R1,V2ADDR          load v2 source
00003F0E  E761 0000 0806                 00000000  2973+          VL    v22,0(R1)         use v22 to test decoder
00003F14  E310 5024 0014                 00000024  2974+          LGF   R1,V3ADDR          load v3 source
00003F1A  E771 0000 0806                 00000000  2975+          VL    v23,0(R1)         use v23 to test decoder
00003F20  E310 5028 0014                 00000028  2976+          LGF   R1,V4ADDR          load v4 source
00003F26  E781 0000 0806                 00000000  2977+          VL    v24,0(R1)         use v24 to test decoder
00003F2C  E766 7020 8F8B                           2978+          VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00003F32  B98D 0020                                2979+          EPSW  R2,R0              extract psw
00003F36  5020 500C                      0000000C  2980+          ST    R2,CCPSW              to save CC
00003F3A  E760 5040 080E                 00003EF0  2981+          VST   V22,V1O55           save v1 output
00003F40  07FB                                     2982+          BR    R11               return
00003F44                                           2983+RE55      DC    0F                xl16 expected result
00003F44                                           2984+          DROP  R5
00003F44  00000000 00000006                        2985           DC    XL16'0000000000000006 0000000000000000'   V1
00003F4C  00000000 00000000
00003F54  F0F1F2F3 F4F50102                        2986           DC    XL16'F0F1F2F3F4F50102 0300FAFBFCFDFEFF'   v2
00003F5C  0300FAFB FCFDFEFF
00003F64  01020300 05060700                        2987           DC    XL16'0102030005060700 090A0B0C0D0E0F10'   v3
00003F6C  090A0B0C 0D0E0F10
00003F74  00000000 00000004                        2988           DC    XL16'0000000000000004 0000000000000000'   v4
00003F7C  00000000 00000000
                                                   2989
                                                   2990 *Halfword
                                                   2991           VRR_D VSTRS,1,2,2                        full match
00003F88                                           2992+          DS    0FD
00003F88                         00003F88          2993+          USING *,R5              base for test data and test routine
00003F88  00003FE0                                 2994+T56       DC    A(X56)            address of test routine
00003F8C  0038                                     2995+          DC    H'56'             test number
00003F8E  00                                       2996+          DC    X'00'
00003F8F  01                                       2997+          DC    HL1'1'                 m5 used
00003F90  02                                       2998+          DC    HL1'2'                 m6 used
00003F91  02                                       2999+          DC    HL1'2'             CC
00003F92  0D                                       3000+          DC    HL1'13'            CC failed mask
00003F94  00000000 00000000                        3001+          DS    2F                 extracted PSW after test (has CC)
00003F9C  FF                                       3002+          DC    X'FF'              extracted CC, if test failed
00003F9D  E5E2E3D9 E2404040                        3003+          DC    CL8'VSTRS'        instruction name
00003FA8  0000402C                                 3004+          DC    A(RE56+16)        address of v2 source
00003FAC  0000403C                                 3005+          DC    A(RE56+32)        address of v3 source
00003FB0  0000404C                                 3006+          DC    A(RE56+48)        address of v4 source
00003FB4  00000010                                 3007+          DC    A(16)             result length
00003FB8  0000401C                                 3008+REA56     DC    A(RE56)           result address
00003FC0  00000000 00000000                        3009+          DS    FD                gap
00003FC8  00000000 00000000                        3010+V1O56     DS    XL16              V1 output
00003FD0  00000000 00000000
00003FD8  00000000 00000000                        3011+          DS    FD                gap
                                                   3012+*
00003FE0                                           3013+X56       DS    0F
00003FE0  E310 5020 0014                 00000020  3014+          LGF   R1,V2ADDR          load v2 source
00003FE6  E761 0000 0806                 00000000  3015+          VL    v22,0(R1)         use v22 to test decoder
00003FEC  E310 5024 0014                 00000024  3016+          LGF   R1,V3ADDR          load v3 source
00003FF2  E771 0000 0806                 00000000  3017+          VL    v23,0(R1)         use v23 to test decoder
00003FF8  E310 5028 0014                 00000028  3018+          LGF   R1,V4ADDR          load v4 source
00003FFE  E781 0000 0806                 00000000  3019+          VL    v24,0(R1)         use v24 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004004  E766 7120 8F8B                          3020+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
0000400A  B98D 0020                               3021+          EPSW  R2,R0                 extract psw
0000400E  5020 500C                     0000000C  3022+          ST    R2,CCPSW                 to save CC
00004012  E760 5040 080E                00003FC8  3023+          VST   V22,V1056             save v1 output
00004018  07FB                                    3024+          BR    R11                  return
0000401C                                          3025+RE56      DC    0F                   xl16 expected result
0000401C                                          3026+          DROP  R5
0000401C  00000000 00000006                       3027           DC    XL16'0000000000000006 0000000000000000'   V1
00004024  00000000 00000000
0000402C  F0F1F2F3 F4F50102                       3028           DC    XL16'F0F1F2F3F4F50102 0000FAFBFCFDFEFF'   v2
00004034  0000FAFB FCFDFEFF
0000403C  01020000 05060000                       3029           DC    XL16'0102000005060000 090A0B0C0D0E0F10'   v3
00004044  090A0B0C 0D0E0F10
0000404C  00000000 00000004                       3030           DC    XL16'0000000000000004 0000000000000000'   v4
00004054  00000000 00000000
                                                  3031
                                                  3032 *Word
                                                  3033           VRR_D VSTRS,2,2,2                               full match
00004060                                          3034+          DS    0FD
00004060                        00004060          3035+          USING *,R5                base for test data and test routine
00004060  000040B8                                3036+T57       DC    A(X57)              address of test routine
00004064  0039                                    3037+          DC    H'57'               test number
00004066  00                                      3038+          DC    X'00'
00004067  02                                      3039+          DC    HL1'2'                   m5 used
00004068  02                                      3040+          DC    HL1'2'                   m6 used
00004069  02                                      3041+          DC    HL1'2'              CC
0000406A  0D                                      3042+          DC    HL1'13'              CC failed mask
0000406C  00000000 00000000                       3043+          DS    2F                   extracted PSW after test (has CC)
00004074  FF                                      3044+          DC    X'FF'                extracted CC, if test failed
00004075  E5E2E3D9 E2404040                       3045+          DC    CL8'VSTRS'          instruction name
00004080  00004104                                3046+          DC    A(RE57+16)          address of v2 source
00004084  00004114                                3047+          DC    A(RE57+32)          address of v3 source
00004088  00004124                                3048+          DC    A(RE57+48)          address of v4 source
0000408C  00000010                                3049+          DC    A(16)               result length
00004090  000040F4                                3050+REA57     DC    A(RE57)             result address
00004098  00000000 00000000                       3051+          DS    FD                  gap
000040A0  00000000 00000000                       3052+V1O57     DS    XL16                V1 output
000040A8  00000000 00000000
000040B0  00000000 00000000                       3053+          DS    FD                  gap
                                                  3054+*
000040B8                                          3055+X57       DS    0F
000040B8  E310 5020 0014                00000020  3056+          LGF   R1,V2ADDR           load v2 source
000040BE  E761 0000 0806                00000000  3057+          VL    v22,0(R1)           use v22 to test decoder
000040C4  E310 5024 0014                00000024  3058+          LGF   R1,V3ADDR           load v3 source
000040CA  E771 0000 0806                00000000  3059+          VL    v23,0(R1)           use v23 to test decoder
000040D0  E310 5028 0014                00000028  3060+          LGF   R1,V4ADDR           load v4 source
000040D6  E781 0000 0806                00000000  3061+          VL    v24,0(R1)           use v24 to test decoder
000040DC  E766 7220 8F8B                          3062+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
000040E2  B98D 0020                               3063+          EPSW  R2,R0                 extract psw
000040E6  5020 500C                     0000000C  3064+          ST    R2,CCPSW                 to save CC
000040EA  E760 5040 080E                000040A0  3065+          VST   V22,V1O57             save v1 output
000040F0  07FB                                    3066+          BR    R11                  return
000040F4                                          3067+RE57      DC    0F                   xl16 expected result
000040F4                                          3068+          DROP  R5
000040F4  00000000 00000004                       3069           DC    XL16'0000000000000004 0000000000000000'   V1
000040FC  00000000 00000000
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004104  F0F1F2F3 01020304                        3070          DC    XL16'F0F1F2F301020304 00000000FCFDFEFF'   v2
0000410C  00000000 FCFDFEFF
00004114  01020304 00000000                        3071          DC    XL16'0102030400000000 000000000D0E0F10'   v3
0000411C  00000000 0D0E0F10
00004124  00000000 00000004                        3072          DC    XL16'0000000000000004 0000000000000000'   v4
0000412C  00000000 00000000
                                                   3073
                                                   3074 *Full Match: at beginning of vector (and at end of vector)
                                                   3075 *Byte
                                                   3076          VRR_D VSTRS,0,2,2                               full match
00004138                                           3077+         DS    0FD
00004138                     00004138              3078+         USING *,R5              base for test data and test routine
00004138  00004190                                 3079+T58      DC    A(X58)            address of test routine
0000413C  003A                                     3080+         DC    H'58'             test number
0000413E  00                                       3081+         DC    X'00'
0000413F  00                                       3082+         DC    HL1'0'                 m5 used
00004140  02                                       3083+         DC    HL1'2'                 m6 used
00004141  02                                       3084+         DC    HL1'2'             CC
00004142  0D                                       3085+         DC    HL1'13'            CC failed mask
00004144  00000000 00000000                        3086+         DS    2F                 extracted PSW after test (has CC)
0000414C  FF                                       3087+         DC    X'FF'              extracted CC, if test failed
0000414D  E5E2E3D9 E2404040                        3088+         DC    CL8'VSTRS'        instruction name
00004158  000041DC                                 3089+         DC    A(RE58+16)        address of v2 source
0000415C  000041EC                                 3090+         DC    A(RE58+32)        address of v3 source
00004160  000041FC                                 3091+         DC    A(RE58+48)        address of v4 source
00004164  00000010                                 3092+         DC    A(16)             result length
00004168  000041CC                                 3093+REA58    DC    A(RE58)           result address
00004170  00000000 00000000                        3094+         DS    FD                gap
00004178  00000000 00000000                        3095+V1O58    DS    XL16              V1 output
00004180  00000000 00000000
00004188  00000000 00000000                        3096+         DS    FD                gap
                                                   3097+*
00004190                                           3098+X58      DS    0F
00004190  E310 5020 0014              00000020     3099+         LGF   R1,V2ADDR         load v2 source
00004196  E761 0000 0806              00000000     3100+         VL    v22,0(R1)         use v22 to test decoder
0000419C  E310 5024 0014              00000024     3101+         LGF   R1,V3ADDR         load v3 source
000041A2  E771 0000 0806              00000000     3102+         VL    v23,0(R1)         use v23 to test decoder
000041A8  E310 5028 0014              00000028     3103+         LGF   R1,V4ADDR         load v4 source
000041AE  E781 0000 0806              00000000     3104+         VL    v24,0(R1)         use v24 to test decoder
000041B4  E766 7020 8F8B                           3105+         VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
000041BA  B98D 0020                                3106+         EPSW  R2,R0              extract psw
000041BE  5020 500C                   0000000C     3107+         ST    R2,CCPSW              to save CC
000041C2  E760 5040 080E              00004178     3108+         VST   V22,V1O58          save v1 output
000041C8  07FB                                     3109+         BR    R11               return
000041CC                                           3110+RE58     DC    0F                xl16 expected result
000041CC                                           3111+         DROP  R5
000041CC  00000000 00000000                        3112          DC    XL16'0000000000000000 0000000000000000'   V1
000041D4  00000000 00000000
000041DC  01020304 F4F5F6F7                        3113          DC    XL16'01020304F4F5F6F7 00FDFEFF01020304'   v2
000041E4  00FDFEFF 01020304
000041EC  01020300 05060700                        3114          DC    XL16'0102030005060700 090A0B0C0D0E0F10'   v3
000041F4  090A0B0C 0D0E0F10
000041FC  00000000 00000004                        3115          DC    XL16'0000000000000004 0000000000000000'   v4
00004204  00000000 00000000
                                                   3116
                                                   3117 *Halfword
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   3118          VRR_D VSTRS,1,2,2                              full match
00004210                                           3119+         DS    0FD
00004210                      00004210             3120+         USING *,R5              base for test data and test routine
00004210  00004268                                 3121+T59      DC    A(X59)            address of test routine
00004214  003B                                     3122+         DC    H'59'             test number
00004216  00                                       3123+         DC    X'00'
00004217  01                                       3124+         DC    HL1'1'                  m5 used
00004218  02                                       3125+         DC    HL1'2'                  m6 used
00004219  02                                       3126+         DC    HL1'2'             CC
0000421A  0D                                       3127+         DC    HL1'13'            CC failed mask
0000421C  00000000 00000000                        3128+         DS    2F                 extracted PSW after test (has CC)
00004224  FF                                       3129+         DC    X'FF'              extracted CC, if test failed
00004225  E5E2E3D9 E2404040                        3130+         DC    CL8'VSTRS'        instruction name
00004230  000042B4                                 3131+         DC    A(RE59+16)        address of v2 source
00004234  000042C4                                 3132+         DC    A(RE59+32)        address of v3 source
00004238  000042D4                                 3133+         DC    A(RE59+48)        address of v4 source
0000423C  00000010                                 3134+         DC    A(16)             result length
00004240  000042A4                                 3135+REA59    DC    A(RE59)           result address
00004248  00000000 00000000                        3136+         DS    FD                gap
00004250  00000000 00000000                        3137+V1O59    DS    XL16              V1 output
00004258  00000000 00000000
00004260  00000000 00000000                        3138+         DS    FD                gap
                                                   3139+*
00004268                                           3140+X59      DS    0F
00004268  E310 5020 0014                 00000020  3141+          LGF   R1,V2ADDR         load v2 source
0000426E  E761 0000 0806                 00000000  3142+          VL    v22,0(R1)         use v22 to test decoder
00004274  E310 5024 0014                 00000024  3143+          LGF   R1,V3ADDR         load v3 source
0000427A  E771 0000 0806                 00000000  3144+          VL    v23,0(R1)         use v23 to test decoder
00004280  E310 5028 0014                 00000028  3145+          LGF   R1,V4ADDR         load v4 source
00004286  E781 0000 0806                 00000000  3146+          VL    v24,0(R1)         use v24 to test decoder
0000428C  E766 7120 8F8B                           3147+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00004292  B98D 0020                                3148+          EPSW  R2,R0              extract psw
00004296  5020 500C                      0000000C  3149+          ST    R2,CCPSW              to save CC
0000429A  E760 5040 080E                 00004250  3150+          VST   V22,V1O59          save v1 output
000042A0  07FB                                     3151+          BR    R11               return
000042A4                                           3152+RE59     DC    0F                xl16 expected result
000042A4                                           3153+         DROP  R5
000042A4  00000000 00000000                       3154          DC    XL16'0000000000000000 0000000000000000'   V1
000042AC  00000000 00000000
000042B4  01020304 F4F5F6F7                        3155          DC    XL16'01020304F4F5F6F7 0000FEFF01020304'   v2
000042BC  0000FEFF 01020304
000042C4  01020000 05060000                        3156          DC    XL16'0102000005060000 090A0B0C0D0E0F10'   v3
000042CC  090A0B0C 0D0E0F10
000042D4  00000000 00000004                        3157          DC    XL16'0000000000000004 0000000000000000'   v4
000042DC  00000000 00000000
                                                   3158
                                                   3159 *Word
                                                   3160          VRR_D VSTRS,2,2,2                              full match
000042E8                                           3161+         DS    0FD
000042E8                      000042E8             3162+         USING *,R5              base for test data and test routine
000042E8  00004340                                 3163+T60      DC    A(X60)            address of test routine
000042EC  003C                                     3164+         DC    H'60'             test number
000042EE  00                                       3165+         DC    X'00'
000042EF  02                                       3166+         DC    HL1'2'                  m5 used
000042F0  02                                       3167+         DC    HL1'2'                  m6 used
000042F1  02                                       3168+         DC    HL1'2'             CC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000042F2  0D                                      3169+          DC    HL1'13'            CC failed mask
000042F4  00000000 00000000                       3170+          DS    2F                 extracted PSW after test (has CC)
000042FC  FF                                      3171+          DC    X'FF'              extracted CC, if test failed
000042FD  E5E2E3D9 E2404040                       3172+          DC    CL8'VSTRS'        instruction name
00004308  0000438C                                3173+          DC    A(RE60+16)        address of v2 source
0000430C  0000439C                                3174+          DC    A(RE60+32)        address of v3 source
00004310  000043AC                                3175+          DC    A(RE60+48)        address of v4 source
00004314  00000010                                3176+          DC    A(16)             result length
00004318  0000437C                                3177+REA60     DC    A(RE60)           result address
00004320  00000000 00000000                       3178+          DS    FD                gap
00004328  00000000 00000000                       3179+V1O60     DS    XL16              V1 output
00004330  00000000 00000000
00004338  00000000 00000000                       3180+          DS    FD                gap
                                                  3181+*
00004340                                          3182+X60       DS    0F
00004340  E310 5020 0014                 00000020 3183+          LGF   R1,V2ADDR         load v2 source
00004346  E761 0000 0806                 00000000 3184+          VL    v22,0(R1)         use v22 to test decoder
0000434C  E310 5024 0014                 00000024 3185+          LGF   R1,V3ADDR         load v3 source
00004352  E771 0000 0806                 00000000 3186+          VL    v23,0(R1)         use v23 to test decoder
00004358  E310 5028 0014                 00000028 3187+          LGF   R1,V4ADDR         load v4 source
0000435E  E781 0000 0806                 00000000 3188+          VL    v24,0(R1)         use v24 to test decoder
00004364  E766 7220 8F8B                          3189+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
0000436A  B98D 0020                               3190+          EPSW  R2,R0              extract psw
0000436E  5020 500C                      0000000C 3191+          ST    R2,CCPSW              to save CC
00004372  E760 5040 080E                 00004328 3192+          VST   V22,V1O60          save v1 output
00004378  07FB                                    3193+          BR    R11               return
0000437C                                          3194+RE60      DC    0F                xl16 expected result
0000437C                                          3195+          DROP  R5
0000437C  00000000 00000000                       3196           DC    XL16'0000000000000000 0000000000000000'   V1
00004384  00000000 00000000
0000438C  01020304 F4F5F6F7                       3197           DC    XL16'01020304F4F5F6F7 0000000001020304'   v2
00004394  00000000 01020304
0000439C  01020304 00000000                       3198           DC    XL16'0102030400000000 000000000D0E0F10'   v3
000043A4  00000000 0D0E0F10
000043AC  00000000 00000004                       3199           DC    XL16'0000000000000004 0000000000000000'   v4
000043B4  00000000 00000000
                                                  3200
                                                  3201 *Full Match: at beginning of vector (and partial at end of vector)
                                                  3202 *Byte
                                                  3203           VRR_D VSTRS,0,2,2                               full match
000043C0                                          3204+          DS    0FD
000043C0                         000043C0         3205+          USING *,R5              base for test data and test routine
000043C0  00004418                                3206+T61       DC    A(X61)            address of test routine
000043C4  003D                                    3207+          DC    H'61'             test number
000043C6  00                                      3208+          DC    X'00'
000043C7  00                                      3209+          DC    HL1'0'                 m5 used
000043C8  02                                      3210+          DC    HL1'2'                 m6 used
000043C9  02                                      3211+          DC    HL1'2'             CC
000043CA  0D                                      3212+          DC    HL1'13'            CC failed mask
000043CC  00000000 00000000                       3213+          DS    2F                 extracted PSW after test (has CC)
000043D4  FF                                      3214+          DC    X'FF'              extracted CC, if test failed
000043D5  E5E2E3D9 E2404040                       3215+          DC    CL8'VSTRS'        instruction name
000043E0  00004464                                3216+          DC    A(RE61+16)        address of v2 source
000043E4  00004474                                3217+          DC    A(RE61+32)        address of v3 source
000043E8  00004484                                3218+          DC    A(RE61+48)        address of v4 source
000043EC  00000010                                3219+          DC    A(16)             result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000043F0  00004454                          3220+REA61    DC    A(RE61)           result address
000043F8  00000000 00000000                 3221+         DS    FD                gap
00004400  00000000 00000000                 3222+V1O61    DS    XL16              V1 output
00004408  00000000 00000000
00004410  00000000 00000000                 3223+         DS    FD                gap
                                            3224+*
00004418                                    3225+X61      DS    0F
00004418  E310 5020 0014              00000020  3226+         LGF   R1,V2ADDR         load v2 source
0000441E  E761 0000 0806              00000000  3227+         VL    v22,0(R1)         use v22 to test decoder
00004424  E310 5024 0014              00000024  3228+         LGF   R1,V3ADDR         load v3 source
0000442A  E771 0000 0806              00000000  3229+         VL    v23,0(R1)         use v23 to test decoder
00004430  E310 5028 0014              00000028  3230+         LGF   R1,V4ADDR         load v4 source
00004436  E781 0000 0806              00000000  3231+         VL    v24,0(R1)         use v24 to test decoder
0000443C  E766 7020 8F8B                        3232+         VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00004442  B98D 0020                             3233+         EPSW  R2,R0              extract psw
00004446  5020 500C                   0000000C  3234+         ST    R2,CCPSW              to save CC
0000444A  E760 5040 080E              00004400  3235+         VST   V22,V1O61          save v1 output
00004450  07FB                                  3236+         BR    R11               return
00004454                                        3237+RE61     DC    0F                xl16 expected result
00004454                                        3238+         DROP  R5
00004454  00000000 00000000                     3239          DC    XL16'0000000000000000 0000000000000000'   V1
0000445C  00000000 00000000
00004464  01020304 F4F5F6F7                     3240          DC    XL16'01020304F4F5F6F7 00FDFEFFBB010203'   v2
0000446C  00FDFEFF BB010203
00004474  01020300 05060700                     3241          DC    XL16'0102030005060700 090A0B0C0D0E0F10'   v3
0000447C  090A0B0C 0D0E0F10
00004484  00000000 00000004                     3242          DC    XL16'0000000000000004 0000000000000000'   v4
0000448C  00000000 00000000
                                                3243
                                                3244 *Halfword
                                                3245          VRR_D VSTRS,1,2,2                               full match
00004498                                        3246+         DS    0FD
00004498                      00004498          3247+         USING *,R5              base for test data and test routine
00004498  000044F0                              3248+T62      DC    A(X62)            address of test routine
0000449C  003E                                  3249+         DC    H'62'             test number
0000449E  00                                    3250+         DC    X'00'
0000449F  01                                    3251+         DC    HL1'1'                 m5 used
000044A0  02                                    3252+         DC    HL1'2'                 m6 used
000044A1  02                                    3253+         DC    HL1'2'             CC
000044A2  0D                                    3254+         DC    HL1'13'            CC failed mask
000044A4  00000000 00000000                     3255+         DS    2F                 extracted PSW after test (has CC)
000044AC  FF                                    3256+         DC    X'FF'              extracted CC, if test failed
000044AD  E5E2E3D9 E2404040                     3257+         DC    CL8'VSTRS'        instruction name
000044B8  0000453C                              3258+         DC    A(RE62+16)        address of v2 source
000044BC  0000454C                              3259+         DC    A(RE62+32)        address of v3 source
000044C0  0000455C                              3260+         DC    A(RE62+48)        address of v4 source
000044C4  00000010                              3261+         DC    A(16)             result length
000044C8  0000452C                              3262+REA62    DC    A(RE62)           result address
000044D0  00000000 00000000                     3263+         DS    FD                gap
000044D8  00000000 00000000                     3264+V1O62    DS    XL16              V1 output
000044E0  00000000 00000000
000044E8  00000000 00000000                     3265+         DS    FD                gap
                                                3266+*
000044F0                                        3267+X62      DS    0F
000044F0  E310 5020 0014              00000020  3268+         LGF   R1,V2ADDR         load v2 source
000044F6  E761 0000 0806              00000000  3269+         VL    v22,0(R1)         use v22 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000044FC  E310 5024 0014                 00000024  3270+          LGF    R1,V3ADDR          load v3 source
00004502  E771 0000 0806                 00000000  3271+          VL     v23,0(R1)          use v23 to test decoder
00004508  E310 5028 0014                 00000028  3272+          LGF    R1,V4ADDR          load v4 source
0000450E  E781 0000 0806                 00000000  3273+          VL     v24,0(R1)          use v24 to test decoder
00004514  E766 7120 8F8B                           3274+          VSTRS  V22,V22,V23,V24,1,2      instruction (dest is a source)
0000451A  B98D 0020                                3275+          EPSW   R2,R0               extract psw
0000451E  5020 500C                      0000000C  3276+          ST     R2,CCPSW               to save CC
00004522  E760 5040 080E                 000044D8  3277+          VST    V22,V1O62           save v1 output
00004528  07FB                                     3278+          BR     R11                return
0000452C                                           3279+RE62      DC     0F                 xl16 expected result
0000452C                                           3280+          DROP   R5
0000452C  00000000 00000000                        3281           DC     XL16'0000000000000000 0000000000000000'   V1
00004534  00000000 00000000
0000453C  01020304 F4F5F6F7                        3282           DC     XL16'01020304F4F5F6F7 0000FEFFBBBB0102'   v2
00004544  0000FEFF BBBB0102
0000454C  01020000 05060000                        3283           DC     XL16'0102000005060000 090A0B0C0D0E0F10'   v3
00004554  090A0B0C 0D0E0F10
0000455C  00000000 00000004                        3284           DC     XL16'0000000000000004 0000000000000000'   v4
00004564  00000000 00000000
                                                   3285
                                                   3286 *Word
                                                   3287           VRR_D  VSTRS,2,2,2                               full match
00004570                                           3288+          DS     0FD
00004570                           00004570        3289+          USING  *,R5               base for test data and test routine
00004570  000045C8                                 3290+T63       DC     A(X63)             address of test routine
00004574  003F                                     3291+          DC     H'63'              test number
00004576  00                                       3292+          DC     X'00'
00004577  02                                       3293+          DC     HL1'2'                   m5 used
00004578  02                                       3294+          DC     HL1'2'                   m6 used
00004579  02                                       3295+          DC     HL1'2'              CC
0000457A  0D                                       3296+          DC     HL1'13'             CC failed mask
0000457C  00000000 00000000                        3297+          DS     2F                  extracted PSW after test (has CC)
00004584  FF                                       3298+          DC     X'FF'               extracted CC, if test failed
00004585  E5E2E3D9 E2404040                       3299+          DC     CL8'VSTRS'         instruction name
00004590  00004614                                 3300+          DC     A(RE63+16)         address of v2 source
00004594  00004624                                 3301+          DC     A(RE63+32)         address of v3 source
00004598  00004634                                 3302+          DC     A(RE63+48)         address of v4 source
0000459C  00000010                                 3303+          DC     A(16)              result length
000045A0  00004604                                 3304+REA63     DC     A(RE63)            result address
000045A8  00000000 00000000                        3305+          DS     FD                 gap
000045B0  00000000 00000000                        3306+V1O63     DS     XL16               V1 output
000045B8  00000000 00000000
000045C0  00000000 00000000                        3307+          DS     FD                 gap
                                                   3308+*
000045C8                                           3309+X63       DS     0F
000045C8  E310 5020 0014                 00000020  3310+          LGF    R1,V2ADDR          load v2 source
000045CE  E761 0000 0806                 00000000  3311+          VL     v22,0(R1)          use v22 to test decoder
000045D4  E310 5024 0014                 00000024  3312+          LGF    R1,V3ADDR          load v3 source
000045DA  E771 0000 0806                 00000000  3313+          VL     v23,0(R1)          use v23 to test decoder
000045E0  E310 5028 0014                 00000028  3314+          LGF    R1,V4ADDR          load v4 source
000045E6  E781 0000 0806                 00000000  3315+          VL     v24,0(R1)          use v24 to test decoder
000045EC  E766 7220 8F8B                           3316+          VSTRS  V22,V22,V23,V24,2,2      instruction (dest is a source)
000045F2  B98D 0020                                3317+          EPSW   R2,R0               extract psw
000045F6  5020 500C                      0000000C  3318+          ST     R2,CCPSW               to save CC
000045FA  E760 5040 080E                 000045B0  3319+          VST    V22,V1O63           save v1 output
00004600  07FB                                     3320+          BR     R11                return
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00004604                                            3321+RE63     DC    0F                xl16 expected result
00004604                                            3322+         DROP  R5
00004604  00000000 00000000                         3323          DC    XL16'0000000000000000 0000000000000000'   V1
0000460C  00000000 00000000
00004614  01020304 05060708                         3324          DC    XL16'0102030405060708 0000000001020304'   v2
0000461C  00000000 01020304
00004624  01020304 00000000                         3325          DC    XL16'0102030400000000 000000000D0E0F10'   v3
0000462C  00000000 0D0E0F10
00004634  00000000 00000008                         3326          DC    XL16'0000000000000008 0000000000000000'   v4
0000463C  00000000 00000000
                                                    3327
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3329 *-------------------------------------------------------------------
                                                   3330 * case 5 - zero length  - full match tests: ZS=1 CC=2
                                                   3331 *-------------------------------------------------------------------
                                                   3332 *Full Match: zero length in V4
                                                   3333 *Byte
                                                   3334          VRR_D VSTRS,0,2,2                              full match
00004648                                           3335+         DS    0FD
00004648                          00004648         3336+         USING *,R5              base for test data and test routine
00004648  000046A0                                 3337+T64      DC    A(X64)            address of test routine
0000464C  0040                                     3338+         DC    H'64'             test number
0000464E  00                                       3339+         DC    X'00'
0000464F  00                                       3340+         DC    HL1'0'                  m5 used
00004650  02                                       3341+         DC    HL1'2'                  m6 used
00004651  02                                       3342+         DC    HL1'2'             CC
00004652  0D                                       3343+         DC    HL1'13'            CC failed mask
00004654  00000000 00000000                        3344+         DS    2F                 extracted PSW after test (has CC)
0000465C  FF                                       3345+         DC    X'FF'              extracted CC, if test failed
0000465D  E5E2E3D9 E2404040                        3346+         DC    CL8'VSTRS'        instruction name
00004668  000046EC                                 3347+         DC    A(RE64+16)        address of v2 source
0000466C  000046FC                                 3348+         DC    A(RE64+32)        address of v3 source
00004670  0000470C                                 3349+         DC    A(RE64+48)        address of v4 source
00004674  00000010                                 3350+         DC    A(16)             result length
00004678  000046DC                                 3351+REA64    DC    A(RE64)           result address
00004680  00000000 00000000                        3352+         DS    FD                gap
00004688  00000000 00000000                        3353+V1O64    DS    XL16              V1 output
00004690  00000000 00000000
00004698  00000000 00000000                        3354+         DS    FD                gap
                                                   3355+*
000046A0                                           3356+X64      DS    0F
000046A0  E310 5020 0014                 00000020  3357+         LGF   R1,V2ADDR         load v2 source
000046A6  E761 0000 0806                 00000000  3358+         VL    v22,0(R1)         use v22 to test decoder
000046AC  E310 5024 0014                 00000024  3359+         LGF   R1,V3ADDR         load v3 source
000046B2  E771 0000 0806                 00000000  3360+         VL    v23,0(R1)         use v23 to test decoder
000046B8  E310 5028 0014                 00000028  3361+         LGF   R1,V4ADDR         load v4 source
000046BE  E781 0000 0806                 00000000  3362+         VL    v24,0(R1)         use v24 to test decoder
000046C4  E766 7020 8F8B                           3363+         VSTRS V22,V22,V23,V24,0,2     instruction (dest is a source)
000046CA  B98D 0020                                3364+         EPSW  R2,R0              extract psw
000046CE  5020 500C                      0000000C  3365+         ST    R2,CCPSW              to save CC
000046D2  E760 5040 080E                 00004688  3366+         VST   V22,V1O64          save v1 output
000046D8  07FB                                     3367+         BR    R11               return
000046DC                                           3368+RE64     DC    0F                xl16 expected result
000046DC                                           3369+         DROP  R5
000046DC  00000000 00000000                        3370          DC    XL16'0000000000000000 0000000000000000'   V1
000046E4  00000000 00000000
000046EC  01020304 F4F5F6F7                        3371          DC    XL16'01020304F4F5F6F7 01020304AAFDFEFF'   v2
000046F4  01020304 AAFDFEFF
000046FC  01020304 05060708                        3372          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00004704  090A0B0C 0D0E0F10
0000470C  00000000 00000000                        3373          DC    XL16'0000000000000000 0000000000000000'   v4
00004714  00000000 00000000
                                                   3374
                                                   3375 *Halfword
                                                   3376          VRR_D VSTRS,1,2,2                              full match
00004720                                           3377+         DS    0FD
00004720                          00004720         3378+         USING *,R5              base for test data and test routine
00004720  00004778                                 3379+T65      DC    A(X65)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004724  0041                                    3380+          DC    H'65'              test number
00004726  00                                      3381+          DC    X'00'
00004727  01                                      3382+          DC    HL1'1'                   m5 used
00004728  02                                      3383+          DC    HL1'2'                   m6 used
00004729  02                                      3384+          DC    HL1'2'              CC
0000472A  0D                                      3385+          DC    HL1'13'             CC failed mask
0000472C  00000000 00000000                       3386+          DS    2F                  extracted PSW after test (has CC)
00004734  FF                                      3387+          DC    X'FF'               extracted CC, if test failed
00004735  E5E2E3D9 E2404040                       3388+          DC    CL8'VSTRS'         instruction name
00004740  000047C4                                3389+          DC    A(RE65+16)         address of v2 source
00004744  000047D4                                3390+          DC    A(RE65+32)         address of v3 source
00004748  000047E4                                3391+          DC    A(RE65+48)         address of v4 source
0000474C  00000010                                3392+          DC    A(16)              result length
00004750  000047B4                                3393+REA65     DC    A(RE65)            result address
00004758  00000000 00000000                       3394+          DS    FD                 gap
00004760  00000000 00000000                       3395+V1O65     DS    XL16               V1 output
00004768  00000000 00000000
00004770  00000000 00000000                       3396+          DS    FD                 gap
                                                  3397+*
00004778                                          3398+X65       DS    0F
00004778  E310 5020 0014                 00000020 3399+          LGF   R1,V2ADDR          load v2 source
0000477E  E761 0000 0806                 00000000 3400+          VL    v22,0(R1)          use v22 to test decoder
00004784  E310 5024 0014                 00000024 3401+          LGF   R1,V3ADDR          load v3 source
0000478A  E771 0000 0806                 00000000 3402+          VL    v23,0(R1)          use v23 to test decoder
00004790  E310 5028 0014                 00000028 3403+          LGF   R1,V4ADDR          load v4 source
00004796  E781 0000 0806                 00000000 3404+          VL    v24,0(R1)          use v24 to test decoder
0000479C  E766 7120 8F8B                          3405+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
000047A2  B98D 0020                               3406+          EPSW  R2,R0               extract psw
000047A6  5020 500C                      0000000C 3407+          ST    R2,CCPSW               to save CC
000047AA  E760 5040 080E                 00004760 3408+          VST   V22,V1O65           save v1 output
000047B0  07FB                                    3409+          BR    R11                 return
000047B4                                          3410+RE65      DC    0F                  xl16 expected result
000047B4                                          3411+          DROP  R5
000047B4  00000000 00000000                       3412           DC    XL16'0000000000000000 0000000000000000'   V1
000047BC  00000000 00000000
000047C4  01020304 F4F5F6F7                       3413           DC    XL16'01020304F4F5F6F7 01020304AAFDFEFF'   v2
000047CC  01020304 AAFDFEFF
000047D4  01020304 05060708                       3414           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000047DC  090A0B0C 0D0E0F10
000047E4  00000000 00000000                       3415           DC    XL16'0000000000000000 0000000000000000'   v4
000047EC  00000000 00000000
                                                  3416
                                                  3417 *Word
                                                  3418           VRR_D VSTRS,2,2,2                               full match
000047F8                                          3419+          DS    0FD
000047F8                 000047F8                 3420+          USING *,R5               base for test data and test routine
000047F8  00004850                                3421+T66       DC    A(X66)             address of test routine
000047FC  0042                                    3422+          DC    H'66'              test number
000047FE  00                                      3423+          DC    X'00'
000047FF  02                                      3424+          DC    HL1'2'                   m5 used
00004800  02                                      3425+          DC    HL1'2'                   m6 used
00004801  02                                      3426+          DC    HL1'2'              CC
00004802  0D                                      3427+          DC    HL1'13'             CC failed mask
00004804  00000000 00000000                       3428+          DS    2F                  extracted PSW after test (has CC)
0000480C  FF                                      3429+          DC    X'FF'               extracted CC, if test failed
0000480D  E5E2E3D9 E2404040                       3430+          DC    CL8'VSTRS'         instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004818  0000489C                                3431+          DC    A(RE66+16)          address of v2 source
0000481C  000048AC                                3432+          DC    A(RE66+32)          address of v3 source
00004820  000048BC                                3433+          DC    A(RE66+48)          address of v4 source
00004824  00000010                                3434+          DC    A(16)               result length
00004828  0000488C                                3435+REA66     DC    A(RE66)             result address
00004830  00000000 00000000                       3436+          DS    FD                  gap
00004838  00000000 00000000                       3437+V1O66     DS    XL16                V1 output
00004840  00000000 00000000
00004848  00000000 00000000                       3438+          DS    FD                  gap
                                                  3439+*
00004850                                          3440+X66       DS    0F
00004850  E310 5020 0014                 00000020 3441+          LGF   R1,V2ADDR           load v2 source
00004856  E761 0000 0806                 00000000 3442+          VL    v22,0(R1)           use v22 to test decoder
0000485C  E310 5024 0014                 00000024 3443+          LGF   R1,V3ADDR           load v3 source
00004862  E771 0000 0806                 00000000 3444+          VL    v23,0(R1)           use v23 to test decoder
00004868  E310 5028 0014                 00000028 3445+          LGF   R1,V4ADDR           load v4 source
0000486E  E781 0000 0806                 00000000 3446+          VL    v24,0(R1)           use v24 to test decoder
00004874  E766 7220 8F8B                          3447+          VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
0000487A  B98D 0020                               3448+          EPSW  R2,R0               extract psw
0000487E  5020 500C                      0000000C 3449+          ST    R2,CCPSW               to save CC
00004882  E760 5040 080E                 00004838 3450+          VST   V22,V1O66           save v1 output
00004888  07FB                                    3451+          BR    R11                 return
0000488C                                          3452+RE66      DC    0F                  xl16 expected result
0000488C                                          3453+          DROP  R5
0000488C  00000000 00000000                       3454           DC    XL16'0000000000000000 0000000000000000'   V1
00004894  00000000 00000000
0000489C  01020304 F4F5F6F7                       3455           DC    XL16'01020304F4F5F6F7 0102030405AAAAFF'   v2
000048A4  01020304 05AAAAFF
000048AC  01020304 05060708                       3456           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000048B4  090A0B0C 0D0E0F10
000048BC  00000000 00000000                       3457           DC    XL16'0000000000000000 0000000000000000'   v4
000048C4  00000000 00000000
                                                  3458
                                                  3459 *Full Match: zero length from ZS
                                                  3460 *Byte
                                                  3461           VRR_D VSTRS,0,2,2                               full match
000048D0                                          3462+          DS    0FD
000048D0                          000048D0        3463+          USING *,R5                base for test data and test routine
000048D0  00004928                                3464+T67       DC    A(X67)              address of test routine
000048D4  0043                                    3465+          DC    H'67'               test number
000048D6  00                                      3466+          DC    X'00'
000048D7  00                                      3467+          DC    HL1'0'                    m5 used
000048D8  02                                      3468+          DC    HL1'2'                    m6 used
000048D9  02                                      3469+          DC    HL1'2'               CC
000048DA  0D                                      3470+          DC    HL1'13'              CC failed mask
000048DC  00000000 00000000                       3471+          DS    2F                   extracted PSW after test (has CC)
000048E4  FF                                      3472+          DC    X'FF'                extracted CC, if test failed
000048E5  E5E2E3D9 E2404040                       3473+          DC    CL8'VSTRS'          instruction name
000048F0  00004974                                3474+          DC    A(RE67+16)          address of v2 source
000048F4  00004984                                3475+          DC    A(RE67+32)          address of v3 source
000048F8  00004994                                3476+          DC    A(RE67+48)          address of v4 source
000048FC  00000010                                3477+          DC    A(16)               result length
00004900  00004964                                3478+REA67     DC    A(RE67)             result address
00004908  00000000 00000000                       3479+          DS    FD                  gap
00004910  00000000 00000000                       3480+V1O67     DS    XL16                V1 output
00004918  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004920  00000000 00000000                        3481+          DS    FD                gap
                                                   3482+*
00004928                                           3483+X67       DS    0F
00004928  E310 5020 0014                 00000020  3484+          LGF   R1,V2ADDR          load v2 source
0000492E  E761 0000 0806                 00000000  3485+          VL    v22,0(R1)         use v22 to test decoder
00004934  E310 5024 0014                 00000024  3486+          LGF   R1,V3ADDR          load v3 source
0000493A  E771 0000 0806                 00000000  3487+          VL    v23,0(R1)         use v23 to test decoder
00004940  E310 5028 0014                 00000028  3488+          LGF   R1,V4ADDR          load v4 source
00004946  E781 0000 0806                 00000000  3489+          VL    v24,0(R1)         use v24 to test decoder
0000494C  E766 7020 8F8B                           3490+          VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00004952  B98D 0020                                3491+          EPSW  R2,R0              extract psw
00004956  5020 500C                      0000000C  3492+          ST    R2,CCPSW              to save CC
0000495A  E760 5040 080E                 00004910  3493+          VST   V22,V1O67           save v1 output
00004960  07FB                                     3494+          BR    R11               return
00004964                                           3495+RE67      DC    0F                xl16 expected result
00004964                                           3496+          DROP  R5
00004964  00000000 00000000                        3497           DC    XL16'0000000000000000 0000000000000000'   V1
0000496C  00000000 00000000
00004974  01020304 F4F5F6F7                        3498           DC    XL16'01020304F4F5F6F7 01020304AAFDFEFF'   v2
0000497C  01020304 AAFDFEFF
00004984  00020304 05060708                        3499           DC    XL16'0002030405060708 090A0B0C0D0E0F10'   v3
0000498C  090A0B0C 0D0E0F10
00004994  00000000 00000004                        3500           DC    XL16'0000000000000004 0000000000000000'   v4
0000499C  00000000 00000000
                                                   3501
                                                   3502 *Halfword
                                                   3503           VRR_D VSTRS,1,2,2                                full match
000049A8                                           3504+          DS    0FD
000049A8                         000049A8          3505+          USING *,R5              base for test data and test routine
000049A8  00004A00                                 3506+T68       DC    A(X68)            address of test routine
000049AC  0044                                     3507+          DC    H'68'             test number
000049AE  00                                       3508+          DC    X'00'
000049AF  01                                       3509+          DC    HL1'1'                 m5 used
000049B0  02                                       3510+          DC    HL1'2'                 m6 used
000049B1  02                                       3511+          DC    HL1'2'             CC
000049B2  0D                                       3512+          DC    HL1'13'            CC failed mask
000049B4  00000000 00000000                        3513+          DS    2F                 extracted PSW after test (has CC)
000049BC  FF                                       3514+          DC    X'FF'              extracted CC, if test failed
000049BD  E5E2E3D9 E2404040                        3515+          DC    CL8'VSTRS'        instruction name
000049C8  00004A4C                                 3516+          DC    A(RE68+16)        address of v2 source
000049CC  00004A5C                                 3517+          DC    A(RE68+32)        address of v3 source
000049D0  00004A6C                                 3518+          DC    A(RE68+48)        address of v4 source
000049D4  00000010                                 3519+          DC    A(16)             result length
000049D8  00004A3C                                 3520+REA68     DC    A(RE68)           result address
000049E0  00000000 00000000                        3521+          DS    FD                gap
000049E8  00000000 00000000                        3522+V1O68     DS    XL16              V1 output
000049F0  00000000 00000000
000049F8  00000000 00000000                        3523+          DS    FD                gap
                                                   3524+*
00004A00                                           3525+X68       DS    0F
00004A00  E310 5020 0014                 00000020  3526+          LGF   R1,V2ADDR          load v2 source
00004A06  E761 0000 0806                 00000000  3527+          VL    v22,0(R1)         use v22 to test decoder
00004A0C  E310 5024 0014                 00000024  3528+          LGF   R1,V3ADDR          load v3 source
00004A12  E771 0000 0806                 00000000  3529+          VL    v23,0(R1)         use v23 to test decoder
00004A18  E310 5028 0014                 00000028  3530+          LGF   R1,V4ADDR          load v4 source
00004A1E  E781 0000 0806                 00000000  3531+          VL    v24,0(R1)         use v24 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004A24  E766 7120 8F8B                         3532+         VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00004A2A  B98D 0020                              3533+         EPSW  R2,R0                 extract psw
00004A2E  5020 500C                 0000000C     3534+         ST    R2,CCPSW                 to save CC
00004A32  E760 5040 080E            000049E8     3535+         VST   V22,V1O68             save v1 output
00004A38  07FB                                   3536+         BR    R11                  return
00004A3C                                         3537+RE68     DC    0F                   xl16 expected result
00004A3C                                         3538+         DROP  R5
00004A3C  00000000 00000000                      3539          DC    XL16'0000000000000000 0000000000000000'   V1
00004A44  00000000 00000000
00004A4C  01020304 F4F5F6F7                      3540          DC    XL16'01020304F4F5F6F7 01020304AAFDFEFF'   v2
00004A54  01020304 AAFDFEFF
00004A5C  00000304 05060708                      3541          DC    XL16'0000030405060708 090A0B0C0D0E0F10'   v3
00004A64  090A0B0C 0D0E0F10
00004A6C  00000000 00000004                      3542          DC    XL16'0000000000000004 0000000000000000'   v4
00004A74  00000000 00000000
                                                 3543
                                                 3544 *Word
                                                 3545          VRR_D VSTRS,2,2,2                               full match
00004A80                                         3546+         DS    0FD
00004A80                            00004A80     3547+         USING *,R5                base for test data and test routine
00004A80  00004AD8                               3548+T69      DC    A(X69)              address of test routine
00004A84  0045                                   3549+         DC    H'69'               test number
00004A86  00                                     3550+         DC    X'00'
00004A87  02                                     3551+         DC    HL1'2'                   m5 used
00004A88  02                                     3552+         DC    HL1'2'                   m6 used
00004A89  02                                     3553+         DC    HL1'2'                CC
00004A8A  0D                                     3554+         DC    HL1'13'               CC failed mask
00004A8C  00000000 00000000                      3555+         DS    2F                    extracted PSW after test (has CC)
00004A94  FF                                     3556+         DC    X'FF'                 extracted CC, if test failed
00004A95  E5E2E3D9 E2404040                      3557+         DC    CL8'VSTRS'          instruction name
00004AA0  00004B24                               3558+         DC    A(RE69+16)          address of v2 source
00004AA4  00004B34                               3559+         DC    A(RE69+32)          address of v3 source
00004AA8  00004B44                               3560+         DC    A(RE69+48)          address of v4 source
00004AAC  00000010                               3561+         DC    A(16)               result length
00004AB0  00004B14                               3562+REA69    DC    A(RE69)             result address
00004AB8  00000000 00000000                      3563+         DS    FD                  gap
00004AC0  00000000 00000000                      3564+V1O69    DS    XL16                V1 output
00004AC8  00000000 00000000
00004AD0  00000000 00000000                      3565+         DS    FD                  gap
                                                 3566+*
00004AD8                                         3567+X69      DS    0F
00004AD8  E310 5020 0014            00000020     3568+         LGF   R1,V2ADDR           load v2 source
00004ADE  E761 0000 0806            00000000     3569+         VL    v22,0(R1)           use v22 to test decoder
00004AE4  E310 5024 0014            00000024     3570+         LGF   R1,V3ADDR           load v3 source
00004AEA  E771 0000 0806            00000000     3571+         VL    v23,0(R1)           use v23 to test decoder
00004AF0  E310 5028 0014            00000028     3572+         LGF   R1,V4ADDR           load v4 source
00004AF6  E781 0000 0806            00000000     3573+         VL    v24,0(R1)           use v24 to test decoder
00004AFC  E766 7220 8F8B                         3574+         VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00004B02  B98D 0020                              3575+         EPSW  R2,R0                 extract psw
00004B06  5020 500C                 0000000C     3576+         ST    R2,CCPSW                 to save CC
00004B0A  E760 5040 080E            00004AC0     3577+         VST   V22,V1O69             save v1 output
00004B10  07FB                                   3578+         BR    R11                  return
00004B14                                         3579+RE69     DC    0F                   xl16 expected result
00004B14                                         3580+         DROP  R5
00004B14  00000000 00000000                      3581          DC    XL16'0000000000000000 0000000000000000'   V1
00004B1C  00000000 00000000
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
00004B24  01020304 F4F5F6F7                         3582           DC    XL16'01020304F4F5F6F7 0102030405AAAAFF'   v2
00004B2C  01020304 05AAAAFF
00004B34  00000000 05060708                         3583           DC    XL16'0000000005060708 090A0B0C0D0E0F10'   v3
00004B3C  090A0B0C 0D0E0F10
00004B44  00000000 00000008                         3584           DC    XL16'0000000000000008 0000000000000000'   v4
00004B4C  00000000 00000000
                                                    3585
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3587 *-------------------------------------------------------------------
                                                   3588 * case 6 - MODEL DEPENDENT - Hercules / z15
                                                   3589 *-------------------------------------------------------------------
                                                   3590 *No Match = bad substring length
                                                   3591 *Halfword
                                                   3592          VRR_D VSTRS,1,0,0                              no match
00004B58                                           3593+         DS    0FD
00004B58                          00004B58         3594+         USING *,R5              base for test data and test routine
00004B58  00004BB0                                 3595+T70      DC    A(X70)            address of test routine
00004B5C  0046                                     3596+         DC    H'70'             test number
00004B5E  00                                       3597+         DC    X'00'
00004B5F  01                                       3598+         DC    HL1'1'                  m5 used
00004B60  00                                       3599+         DC    HL1'0'                  m6 used
00004B61  00                                       3600+         DC    HL1'0'             CC
00004B62  07                                       3601+         DC    HL1'7'             CC failed mask
00004B64  00000000 00000000                        3602+         DS    2F                 extracted PSW after test (has CC)
00004B6C  FF                                       3603+         DC    X'FF'              extracted CC, if test failed
00004B6D  E5E2E3D9 E2404040                        3604+         DC    CL8'VSTRS'        instruction name
00004B78  00004BFC                                 3605+         DC    A(RE70+16)        address of v2 source
00004B7C  00004C0C                                 3606+         DC    A(RE70+32)        address of v3 source
00004B80  00004C1C                                 3607+         DC    A(RE70+48)        address of v4 source
00004B84  00000010                                 3608+         DC    A(16)             result length
00004B88  00004BEC                                 3609+REA70    DC    A(RE70)           result address
00004B90  00000000 00000000                        3610+         DS    FD                gap
00004B98  00000000 00000000                        3611+V1O70    DS    XL16              V1 output
00004BA0  00000000 00000000
00004BA8  00000000 00000000                        3612+         DS    FD                gap
                                                   3613+*
00004BB0                                           3614+X70      DS    0F
00004BB0  E310 5020 0014                 00000020  3615+         LGF   R1,V2ADDR         load v2 source
00004BB6  E761 0000 0806                 00000000  3616+         VL    v22,0(R1)         use v22 to test decoder
00004BBC  E310 5024 0014                 00000024  3617+         LGF   R1,V3ADDR         load v3 source
00004BC2  E771 0000 0806                 00000000  3618+         VL    v23,0(R1)         use v23 to test decoder
00004BC8  E310 5028 0014                 00000028  3619+         LGF   R1,V4ADDR         load v4 source
00004BCE  E781 0000 0806                 00000000  3620+         VL    v24,0(R1)         use v24 to test decoder
00004BD4  E766 7100 8F8B                           3621+         VSTRS V22,V22,V23,V24,1,0      instruction (dest is a source)
00004BDA  B98D 0020                                3622+         EPSW  R2,R0              extract psw
00004BDE  5020 500C                      0000000C  3623+         ST    R2,CCPSW              to save CC
00004BE2  E760 5040 080E                 00004B98  3624+         VST   V22,V1O70          save v1 output
00004BE8  07FB                                     3625+         BR    R11               return
00004BEC                                           3626+RE70     DC    0F                xl16 expected result
00004BEC                                           3627+         DROP  R5
00004BEC  00000000 00000010                        3628          DC    XL16'0000000000000010 0000000000000000'   V1
00004BF4  00000000 00000000
00004BFC  01020304 F4F5F6F7                        3629          DC    XL16'01020304F4F5F6F7 01020304AAFDFEFF'   v2
00004C04  01020304 AAFDFEFF
00004C0C  01020304 05060708                        3630          DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00004C14  090A0B0C 0D0E0F10
00004C1C  00000000 00000003                        3631          DC    XL16'0000000000000003 0000000000000000'   v4
00004C24  00000000 00000000
                                                   3632
                                                   3633 *Word
                                                   3634          VRR_D VSTRS,2,0,0                              no match
00004C30                                           3635+         DS    0FD
00004C30                          00004C30         3636+         USING *,R5              base for test data and test routine
00004C30  00004C88                                 3637+T71      DC    A(X71)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004C34  0047                                    3638+          DC    H'71'              test number
00004C36  00                                      3639+          DC    X'00'
00004C37  02                                      3640+          DC    HL1'2'                   m5 used
00004C38  00                                      3641+          DC    HL1'0'                   m6 used
00004C39  00                                      3642+          DC    HL1'0'              CC
00004C3A  07                                      3643+          DC    HL1'7'              CC failed mask
00004C3C  00000000 00000000                       3644+          DS    2F                  extracted PSW after test (has CC)
00004C44  FF                                      3645+          DC    X'FF'               extracted CC, if test failed
00004C45  E5E2E3D9 E2404040                       3646+          DC    CL8'VSTRS'         instruction name
00004C50  00004CD4                                3647+          DC    A(RE71+16)         address of v2 source
00004C54  00004CE4                                3648+          DC    A(RE71+32)         address of v3 source
00004C58  00004CF4                                3649+          DC    A(RE71+48)         address of v4 source
00004C5C  00000010                                3650+          DC    A(16)              result length
00004C60  00004CC4                                3651+REA71     DC    A(RE71)            result address
00004C68  00000000 00000000                       3652+          DS    FD                 gap
00004C70  00000000 00000000                       3653+V1O71     DS    XL16               V1 output
00004C78  00000000 00000000
00004C80  00000000 00000000                       3654+          DS    FD                 gap
                                                  3655+*
00004C88                                          3656+X71       DS    0F
00004C88  E310 5020 0014                 00000020 3657+          LGF   R1,V2ADDR          load v2 source
00004C8E  E761 0000 0806                 00000000 3658+          VL    v22,0(R1)          use v22 to test decoder
00004C94  E310 5024 0014                 00000024 3659+          LGF   R1,V3ADDR          load v3 source
00004C9A  E771 0000 0806                 00000000 3660+          VL    v23,0(R1)          use v23 to test decoder
00004CA0  E310 5028 0014                 00000028 3661+          LGF   R1,V4ADDR          load v4 source
00004CA6  E781 0000 0806                 00000000 3662+          VL    v24,0(R1)          use v24 to test decoder
00004CAC  E766 7200 8F8B                          3663+          VSTRS V22,V22,V23,V24,2,0      instruction (dest is a source)
00004CB2  B98D 0020                               3664+          EPSW  R2,R0               extract psw
00004CB6  5020 500C                      0000000C 3665+          ST    R2,CCPSW               to save CC
00004CBA  E760 5040 080E                 00004C70 3666+          VST   V22,V1O71           save v1 output
00004CC0  07FB                                    3667+          BR    R11                 return
00004CC4                                          3668+RE71      DC    0F                  xl16 expected result
00004CC4                                          3669+          DROP  R5
00004CC4  00000000 00000010                       3670           DC    XL16'0000000000000010 0000000000000000'   V1
00004CCC  00000000 00000000
00004CD4  01020304 F4F5F6F7                       3671           DC    XL16'01020304F4F5F6F7 0102030405AAAAFF'   v2
00004CDC  01020304 05AAAAFF
00004CE4  01020304 05060708                       3672           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00004CEC  090A0B0C 0D0E0F10
00004CF4  00000000 00000005                       3673           DC    XL16'0000000000000005 0000000000000000'   v4
00004CFC  00000000 00000000
                                                  3674
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   3676 *-------------------------------------------------------------------
                                                   3677 * case 7 - misc
                                                   3678 *-------------------------------------------------------------------
                                                   3679 *Full Match: many common substrings
                                                   3680 *Byte
                                                   3681          VRR_D VSTRS,0,2,2                              full match
00004D08                                           3682+         DS    0FD
00004D08                          00004D08         3683+         USING *,R5              base for test data and test routine
00004D08  00004D60                                 3684+T72      DC    A(X72)            address of test routine
00004D0C  0048                                     3685+         DC    H'72'             test number
00004D0E  00                                       3686+         DC    X'00'
00004D0F  00                                       3687+         DC    HL1'0'                  m5 used
00004D10  02                                       3688+         DC    HL1'2'                  m6 used
00004D11  02                                       3689+         DC    HL1'2'             CC
00004D12  0D                                       3690+         DC    HL1'13'            CC failed mask
00004D14  00000000 00000000                        3691+         DS    2F                 extracted PSW after test (has CC)
00004D1C  FF                                       3692+         DC    X'FF'              extracted CC, if test failed
00004D1D  E5E2E3D9 E2404040                        3693+         DC    CL8'VSTRS'        instruction name
00004D28  00004DAC                                 3694+         DC    A(RE72+16)        address of v2 source
00004D2C  00004DBC                                 3695+         DC    A(RE72+32)        address of v3 source
00004D30  00004DCC                                 3696+         DC    A(RE72+48)        address of v4 source
00004D34  00000010                                 3697+         DC    A(16)             result length
00004D38  00004D9C                                 3698+REA72    DC    A(RE72)           result address
00004D40  00000000 00000000                        3699+         DS    FD                gap
00004D48  00000000 00000000                        3700+V1O72    DS    XL16              V1 output
00004D50  00000000 00000000
00004D58  00000000 00000000                        3701+         DS    FD                gap
                                                   3702+*
00004D60                                           3703+X72      DS    0F
00004D60  E310 5020 0014                 00000020  3704+         LGF   R1,V2ADDR         load v2 source
00004D66  E761 0000 0806                 00000000  3705+         VL    v22,0(R1)         use v22 to test decoder
00004D6C  E310 5024 0014                 00000024  3706+         LGF   R1,V3ADDR         load v3 source
00004D72  E771 0000 0806                 00000000  3707+         VL    v23,0(R1)         use v23 to test decoder
00004D78  E310 5028 0014                 00000028  3708+         LGF   R1,V4ADDR         load v4 source
00004D7E  E781 0000 0806                 00000000  3709+         VL    v24,0(R1)         use v24 to test decoder
00004D84  E766 7020 8F8B                           3710+         VSTRS V22,V22,V23,V24,0,2     instruction (dest is a source)
00004D8A  B98D 0020                                3711+         EPSW  R2,R0              extract psw
00004D8E  5020 500C                      0000000C  3712+         ST    R2,CCPSW              to save CC
00004D92  E760 5040 080E                 00004D48  3713+         VST   V22,V1O72          save v1 output
00004D98  07FB                                     3714+         BR    R11               return
00004D9C                                           3715+RE72     DC    0F                xl16 expected result
00004D9C                                           3716+         DROP  R5
00004D9C  00000000 00000008                        3717          DC    XL16'0000000000000008 0000000000000000'   V1
00004DA4  00000000 00000000
00004DAC  01020301 02010201                        3718          DC    XL16'0102030102010201 0102030401020304'   v2
00004DB4  01020304 01020304
00004DBC  01020304 00506070                        3719          DC    XL16'0102030400506070 090A0B0C0D0E0F10'   v3
00004DC4  090A0B0C 0D0E0F10
00004DCC  00000000 00000004                        3720          DC    XL16'0000000000000004 0000000000000000'   v4
00004DD4  00000000 00000000
                                                   3721
                                                   3722 *Halfword
                                                   3723          VRR_D VSTRS,1,2,2                              full match
00004DE0                                           3724+         DS    0FD
00004DE0                          00004DE0         3725+         USING *,R5              base for test data and test routine
00004DE0  00004E38                                 3726+T73      DC    A(X73)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004DE4  0049                                    3727+          DC    H'73'              test number
00004DE6  00                                      3728+          DC    X'00'
00004DE7  01                                      3729+          DC    HL1'1'                   m5 used
00004DE8  02                                      3730+          DC    HL1'2'                   m6 used
00004DE9  02                                      3731+          DC    HL1'2'              CC
00004DEA  0D                                      3732+          DC    HL1'13'             CC failed mask
00004DEC  00000000 00000000                       3733+          DS    2F                  extracted PSW after test (has CC)
00004DF4  FF                                      3734+          DC    X'FF'               extracted CC, if test failed
00004DF5  E5E2E3D9 E2404040                       3735+          DC    CL8'VSTRS'          instruction name
00004E00  00004E84                                3736+          DC    A(RE73+16)          address of v2 source
00004E04  00004E94                                3737+          DC    A(RE73+32)          address of v3 source
00004E08  00004EA4                                3738+          DC    A(RE73+48)          address of v4 source
00004E0C  00000010                                3739+          DC    A(16)               result length
00004E10  00004E74                                3740+REA73     DC    A(RE73)             result address
00004E18  00000000 00000000                       3741+          DS    FD                  gap
00004E20  00000000 00000000                       3742+V1O73     DS    XL16                V1 output
00004E28  00000000 00000000
00004E30  00000000 00000000                       3743+          DS    FD                  gap
                                                  3744+*
00004E38                                          3745+X73       DS    0F
00004E38  E310 5020 0014                 00000020 3746+          LGF   R1,V2ADDR           load v2 source
00004E3E  E761 0000 0806                 00000000 3747+          VL    v22,0(R1)           use v22 to test decoder
00004E44  E310 5024 0014                 00000024 3748+          LGF   R1,V3ADDR           load v3 source
00004E4A  E771 0000 0806                 00000000 3749+          VL    v23,0(R1)           use v23 to test decoder
00004E50  E310 5028 0014                 00000028 3750+          LGF   R1,V4ADDR           load v4 source
00004E56  E781 0000 0806                 00000000 3751+          VL    v24,0(R1)           use v24 to test decoder
00004E5C  E766 7120 8F8B                          3752+          VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
00004E62  B98D 0020                               3753+          EPSW  R2,R0               extract psw
00004E66  5020 500C                      0000000C 3754+          ST    R2,CCPSW               to save CC
00004E6A  E760 5040 080E                 00004E20 3755+          VST   V22,V1O73           save v1 output
00004E70  07FB                                    3756+          BR    R11                 return
00004E74                                          3757+RE73      DC    0F                  xl16 expected result
00004E74                                          3758+          DROP  R5
00004E74  00000000 0000000C                       3759           DC    XL16'000000000000000C 0000000000000000'   V1
00004E7C  00000000 00000000
00004E84  01020301 02010201                       3760           DC    XL16'0102030102010201 0102030501020304'   v2
00004E8C  01020305 01020304
00004E94  01020304 05060000                       3761           DC    XL16'0102030405060000 090A0B0C0D0E0F10'   v3
00004E9C  090A0B0C 0D0E0F10
00004EA4  00000000 00000004                       3762           DC    XL16'0000000000000004 0000000000000000'   v4
00004EAC  00000000 00000000
                                                  3763
                                                  3764 *Word
                                                  3765           VRR_D VSTRS,2,2,2                               full match
00004EB8                                          3766+          DS    0FD
00004EB8                         00004EB8         3767+          USING *,R5                base for test data and test routine
00004EB8  00004F10                                3768+T74       DC    A(X74)              address of test routine
00004EBC  004A                                    3769+          DC    H'74'               test number
00004EBE  00                                      3770+          DC    X'00'
00004EBF  02                                      3771+          DC    HL1'2'                   m5 used
00004EC0  02                                      3772+          DC    HL1'2'                   m6 used
00004EC1  02                                      3773+          DC    HL1'2'              CC
00004EC2  0D                                      3774+          DC    HL1'13'             CC failed mask
00004EC4  00000000 00000000                       3775+          DS    2F                  extracted PSW after test (has CC)
00004ECC  FF                                      3776+          DC    X'FF'               extracted CC, if test failed
00004ECD  E5E2E3D9 E2404040                       3777+          DC    CL8'VSTRS'          instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004ED8  00004F5C                       3778+          DC    A(RE74+16)        address of v2 source
00004EDC  00004F6C                       3779+          DC    A(RE74+32)        address of v3 source
00004EE0  00004F7C                       3780+          DC    A(RE74+48)        address of v4 source
00004EE4  00000010                       3781+          DC    A(16)             result length
00004EE8  00004F4C                       3782+REA74     DC    A(RE74)           result address
00004EF0  00000000 00000000              3783+          DS    FD                gap
00004EF8  00000000 00000000              3784+V1O74     DS    XL16              V1 output
00004F00  00000000 00000000
00004F08  00000000 00000000              3785+          DS    FD                gap
                                         3786+*
00004F10                                 3787+X74       DS    0F
00004F10  E310 5020 0014          00000020  3788+       LGF   R1,V2ADDR         load v2 source
00004F16  E761 0000 0806          00000000  3789+       VL    v22,0(R1)         use v22 to test decoder
00004F1C  E310 5024 0014          00000024  3790+       LGF   R1,V3ADDR         load v3 source
00004F22  E771 0000 0806          00000000  3791+       VL    v23,0(R1)         use v23 to test decoder
00004F28  E310 5028 0014          00000028  3792+       LGF   R1,V4ADDR         load v4 source
00004F2E  E781 0000 0806          00000000  3793+       VL    v24,0(R1)         use v24 to test decoder
00004F34  E766 7220 8F8B                    3794+       VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
00004F3A  B98D 0020                         3795+       EPSW  R2,R0              extract psw
00004F3E  5020 500C               0000000C  3796+       ST    R2,CCPSW              to save CC
00004F42  E760 5040 080E          00004EF8  3797+       VST   V22,V1O74          save v1 output
00004F48  07FB                              3798+       BR    R11               return
00004F4C                                    3799+RE74     DC    0F                xl16 expected result
00004F4C                                    3800+       DROP  R5
00004F4C  00000000 0000000C                 3801        DC    XL16'000000000000000C 0000000000000000'   V1
00004F54  00000000 00000000
00004F5C  01020301 01030400                 3802        DC    XL16'0102030101030400 0102010401020304'   v2
00004F64  01020104 01020304
00004F6C  01020304 05060708                 3803        DC    XL16'0102030405060708 0000000001020304'   v3
00004F74  00000000 01020304
00004F7C  00000000 00000004                 3804        DC    XL16'0000000000000004 0000000000000000'   v4
00004F84  00000000 00000000
                                            3805
                                            3806 *Full Match: ZS=1; v4 substring length > 16; many common substrings
                                            3807 *Byte
                                            3808        VRR_D VSTRS,0,2,2                               full match
00004F90                                    3809+       DS    0FD
00004F90                          00004F90  3810+       USING *,R5              base for test data and test routine
00004F90  00004FE8                          3811+T75      DC    A(X75)            address of test routine
00004F94  004B                              3812+         DC    H'75'             test number
00004F96  00                                3813+         DC    X'00'
00004F97  00                                3814+         DC    HL1'0'                 m5 used
00004F98  02                                3815+         DC    HL1'2'                 m6 used
00004F99  02                                3816+         DC    HL1'2'             CC
00004F9A  0D                                3817+         DC    HL1'13'            CC failed mask
00004F9C  00000000 00000000                 3818+         DS    2F                 extracted PSW after test (has CC)
00004FA4  FF                                3819+         DC    X'FF'              extracted CC, if test failed
00004FA5  E5E2E3D9 E2404040                 3820+         DC    CL8'VSTRS'        instruction name
00004FB0  00005034                          3821+         DC    A(RE75+16)        address of v2 source
00004FB4  00005044                          3822+         DC    A(RE75+32)        address of v3 source
00004FB8  00005054                          3823+         DC    A(RE75+48)        address of v4 source
00004FBC  00000010                          3824+         DC    A(16)             result length
00004FC0  00005024                          3825+REA75    DC    A(RE75)           result address
00004FC8  00000000 00000000                 3826+         DS    FD                gap
00004FD0  00000000 00000000                 3827+V1O75    DS    XL16              V1 output
00004FD8  00000000 00000000
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004FE0  00000000 00000000                      3828+          DS    FD                gap
                                                 3829+*
00004FE8                                         3830+X75       DS    0F
00004FE8  E310 5020 0014                00000020 3831+          LGF   R1,V2ADDR         load v2 source
00004FEE  E761 0000 0806                00000000 3832+          VL    v22,0(R1)         use v22 to test decoder
00004FF4  E310 5024 0014                00000024 3833+          LGF   R1,V3ADDR         load v3 source
00004FFA  E771 0000 0806                00000000 3834+          VL    v23,0(R1)         use v23 to test decoder
00005000  E310 5028 0014                00000028 3835+          LGF   R1,V4ADDR         load v4 source
00005006  E781 0000 0806                00000000 3836+          VL    v24,0(R1)         use v24 to test decoder
0000500C  E766 7020 8F8B                         3837+          VSTRS V22,V22,V23,V24,0,2      instruction (dest is a source)
00005012  B98D 0020                              3838+          EPSW  R2,R0              extract psw
00005016  5020 500C                     0000000C 3839+          ST    R2,CCPSW              to save CC
0000501A  E760 5040 080E                00004FD0 3840+          VST   V22,V1O75          save v1 output
00005020  07FB                                   3841+          BR    R11               return
00005024                                         3842+RE75      DC    0F                xl16 expected result
00005024                                         3843+          DROP  R5
00005024  00000000 00000008                      3844           DC    XL16'0000000000000008 0000000000000000'   V1
0000502C  00000000 00000000
00005034  01020301 02010201                      3845           DC    XL16'0102030102010201 0102030401020304'   v2
0000503C  01020304 01020304
00005044  01020304 00506070                      3846           DC    XL16'0102030400506070 090A0B0C0D0E0F10'   v3
0000504C  090A0B0C 0D0E0F10
00005054  00000000 000000FF                      3847           DC    XL16'00000000000000FF 0000000000000000'   v4
0000505C  00000000 00000000
                                                 3848
                                                 3849 *Halfword
                                                 3850           VRR_D VSTRS,1,2,2                        full match
00005068                                         3851+          DS    0FD
00005068                        00005068         3852+          USING *,R5              base for test data and test routine
00005068  000050C0                               3853+T76       DC    A(X76)            address of test routine
0000506C  004C                                   3854+          DC    H'76'             test number
0000506E  00                                     3855+          DC    X'00'
0000506F  01                                     3856+          DC    HL1'1'                 m5 used
00005070  02                                     3857+          DC    HL1'2'                 m6 used
00005071  02                                     3858+          DC    HL1'2'             CC
00005072  0D                                     3859+          DC    HL1'13'            CC failed mask
00005074  00000000 00000000                      3860+          DS    2F                 extracted PSW after test (has CC)
0000507C  FF                                     3861+          DC    X'FF'              extracted CC, if test failed
0000507D  E5E2E3D9 E2404040                      3862+          DC    CL8'VSTRS'        instruction name
00005088  0000510C                               3863+          DC    A(RE76+16)        address of v2 source
0000508C  0000511C                               3864+          DC    A(RE76+32)        address of v3 source
00005090  0000512C                               3865+          DC    A(RE76+48)        address of v4 source
00005094  00000010                               3866+          DC    A(16)             result length
00005098  000050FC                               3867+REA76     DC    A(RE76)           result address
000050A0  00000000 00000000                      3868+          DS    FD                gap
000050A8  00000000 00000000                      3869+V1O76     DS    XL16              V1 output
000050B0  00000000 00000000
000050B8  00000000 00000000                      3870+          DS    FD                gap
                                                 3871+*
000050C0                                         3872+X76       DS    0F
000050C0  E310 5020 0014                00000020 3873+          LGF   R1,V2ADDR         load v2 source
000050C6  E761 0000 0806                00000000 3874+          VL    v22,0(R1)         use v22 to test decoder
000050CC  E310 5024 0014                00000024 3875+          LGF   R1,V3ADDR         load v3 source
000050D2  E771 0000 0806                00000000 3876+          VL    v23,0(R1)         use v23 to test decoder
000050D8  E310 5028 0014                00000028 3877+          LGF   R1,V4ADDR         load v4 source
000050DE  E781 0000 0806                00000000 3878+          VL    v24,0(R1)         use v24 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000050E4  E766 7120 8F8B                          3879+         VSTRS V22,V22,V23,V24,1,2      instruction (dest is a source)
000050EA  B98D 0020                               3880+         EPSW  R2,R0                 extract psw
000050EE  5020 500C                     0000000C  3881+         ST    R2,CCPSW                 to save CC
000050F2  E760 5040 080E                000050A8  3882+         VST   V22,V1O76             save v1 output
000050F8  07FB                                    3883+         BR    R11                  return
000050FC                                          3884+RE76     DC    0F                   xl16 expected result
000050FC                                          3885+         DROP  R5
000050FC  00000000 0000000C                       3886          DC    XL16'000000000000000C 0000000000000000'   V1
00005104  00000000 00000000
0000510C  01020301 02010201                       3887          DC    XL16'0102030102010201 0102030501020304'   v2
00005114  01020305 01020304
0000511C  01020304 00000700                       3888          DC    XL16'0102030400000700 090A0B0C0D0E0F10'   v3
00005124  090A0B0C 0D0E0F10
0000512C  00000000 000000FF                       3889          DC    XL16'00000000000000FF 0000000000000000'   v4
00005134  00000000 00000000
                                                  3890
                                                  3891 *Word
                                                  3892          VRR_D VSTRS,2,2,2                               full match
00005140                                          3893+         DS    0FD
00005140                        00005140          3894+         USING *,R5                base for test data and test routine
00005140  00005198                                3895+T77      DC    A(X77)              address of test routine
00005144  004D                                    3896+         DC    H'77'               test number
00005146  00                                      3897+         DC    X'00'
00005147  02                                      3898+         DC    HL1'2'                   m5 used
00005148  02                                      3899+         DC    HL1'2'                   m6 used
00005149  02                                      3900+         DC    HL1'2'               CC
0000514A  0D                                      3901+         DC    HL1'13'              CC failed mask
0000514C  00000000 00000000                       3902+         DS    2F                   extracted PSW after test (has CC)
00005154  FF                                      3903+         DC    X'FF'                extracted CC, if test failed
00005155  E5E2E3D9 E2404040                       3904+         DC    CL8'VSTRS'          instruction name
00005160  000051E4                                3905+         DC    A(RE77+16)          address of v2 source
00005164  000051F4                                3906+         DC    A(RE77+32)          address of v3 source
00005168  00005204                                3907+         DC    A(RE77+48)          address of v4 source
0000516C  00000010                                3908+         DC    A(16)               result length
00005170  000051D4                                3909+REA77    DC    A(RE77)             result address
00005178  00000000 00000000                       3910+         DS    FD                  gap
00005180  00000000 00000000                       3911+V1O77    DS    XL16                V1 output
00005188  00000000 00000000
00005190  00000000 00000000                       3912+         DS    FD                  gap
                                                  3913+*
00005198                                          3914+X77      DS    0F
00005198  E310 5020 0014                00000020  3915+         LGF   R1,V2ADDR           load v2 source
0000519E  E761 0000 0806                00000000  3916+         VL    v22,0(R1)           use v22 to test decoder
000051A4  E310 5024 0014                00000024  3917+         LGF   R1,V3ADDR           load v3 source
000051AA  E771 0000 0806                00000000  3918+         VL    v23,0(R1)           use v23 to test decoder
000051B0  E310 5028 0014                00000028  3919+         LGF   R1,V4ADDR           load v4 source
000051B6  E781 0000 0806                00000000  3920+         VL    v24,0(R1)           use v24 to test decoder
000051BC  E766 7220 8F8B                          3921+         VSTRS V22,V22,V23,V24,2,2      instruction (dest is a source)
000051C2  B98D 0020                               3922+         EPSW  R2,R0                 extract psw
000051C6  5020 500C                     0000000C  3923+         ST    R2,CCPSW                 to save CC
000051CA  E760 5040 080E                00005180  3924+         VST   V22,V1O77             save v1 output
000051D0  07FB                                    3925+         BR    R11                  return
000051D4                                          3926+RE77     DC    0F                   xl16 expected result
000051D4                                          3927+         DROP  R5
000051D4  00000000 0000000C                       3928          DC    XL16'000000000000000C 0000000000000000'   V1
000051DC  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000051E4  01020301 01030400                      3929           DC    XL16'0102030101030400 0102010401020304'   v2
000051EC  01020104 01020304
000051F4  01020304 00000000                      3930           DC    XL16'0102030400000000 0000000001020304'   v3
000051FC  00000000 01020304
00005204  00000000 000000FF                      3931           DC    XL16'00000000000000FF 0000000000000000'   v4
0000520C  00000000 00000000
                                                 3932
                                                 3933 *No Match: ZS=0; v4 substring length > 16; many common substrings
                                                 3934 *Byte
                                                 3935           VRR_D VSTRS,0,0,0                                 no match
00005218                                         3936+          DS    0FD
00005218                        00005218         3937+          USING *,R5              base for test data and test routine
00005218  00005270                               3938+T78       DC    A(X78)            address of test routine
0000521C  004E                                   3939+          DC    H'78'             test number
0000521E  00                                     3940+          DC    X'00'
0000521F  00                                     3941+          DC    HL1'0'                  m5 used
00005220  00                                     3942+          DC    HL1'0'                  m6 used
00005221  00                                     3943+          DC    HL1'0'             CC
00005222  07                                     3944+          DC    HL1'7'             CC failed mask
00005224  00000000 00000000                      3945+          DS    2F                 extracted PSW after test (has CC)
0000522C  FF                                     3946+          DC    X'FF'              extracted CC, if test failed
0000522D  E5E2E3D9 E2404040                      3947+          DC    CL8'VSTRS'        instruction name
00005238  000052BC                               3948+          DC    A(RE78+16)        address of v2 source
0000523C  000052CC                               3949+          DC    A(RE78+32)        address of v3 source
00005240  000052DC                               3950+          DC    A(RE78+48)        address of v4 source
00005244  00000010                               3951+          DC    A(16)             result length
00005248  000052AC                               3952+REA78     DC    A(RE78)           result address
00005250  00000000 00000000                      3953+          DS    FD                gap
00005258  00000000 00000000                      3954+V1078     DS    XL16              V1 output
00005260  00000000 00000000
00005268  00000000 00000000                      3955+          DS    FD                gap
                                                 3956+*
00005270                                         3957+X78       DS    0F
00005270  E310 5020 0014                00000020 3958+          LGF   R1,V2ADDR         load v2 source
00005276  E761 0000 0806                00000000 3959+          VL    v22,0(R1)         use v22 to test decoder
0000527C  E310 5024 0014                00000024 3960+          LGF   R1,V3ADDR         load v3 source
00005282  E771 0000 0806                00000000 3961+          VL    v23,0(R1)         use v23 to test decoder
00005288  E310 5028 0014                00000028 3962+          LGF   R1,V4ADDR         load v4 source
0000528E  E781 0000 0806                00000000 3963+          VL    v24,0(R1)         use v24 to test decoder
00005294  E766 7000 8F8B                         3964+          VSTRS V22,V22,V23,V24,0,0      instruction (dest is a source)
0000529A  B98D 0020                              3965+          EPSW  R2,R0              extract psw
0000529E  5020 500C                     0000000C 3966+          ST    R2,CCPSW              to save CC
000052A2  E760 5040 080E                00005258 3967+          VST   V22,V1078          save v1 output
000052A8  07FB                                   3968+          BR    R11               return
000052AC                                         3969+RE78      DC    0F                xl16 expected result
000052AC                                         3970+          DROP  R5
000052AC  00000000 00000010                      3971           DC    XL16'0000000000000010 0000000000000000'   V1
000052B4  00000000 00000000
000052BC  01020301 02010201                      3972           DC    XL16'0102030102010201 0102030401020300'   v2
000052C4  01020304 01020300
000052CC  01020304 00506070                      3973           DC    XL16'0102030400506070 090A0B0C0D0E0F10'   v3
000052D4  090A0B0C 0D0E0F10
000052DC  00000000 000000FF                      3974           DC    XL16'00000000000000FF 0000000000000000'   v4
000052E4  00000000 00000000
                                                 3975
                                                 3976 *Halfword
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                         3977          VRR_D VSTRS,1,0,0                              no match
000052F0                                 3978+         DS    0FD
000052F0                    000052F0     3979+         USING *,R5             base for test data and test routine
000052F0  00005348                       3980+T79      DC    A(X79)           address of test routine
000052F4  004F                           3981+         DC    H'79'            test number
000052F6  00                             3982+         DC    X'00'
000052F7  01                             3983+         DC    HL1'1'                 m5 used
000052F8  00                             3984+         DC    HL1'0'                 m6 used
000052F9  00                             3985+         DC    HL1'0'            CC
000052FA  07                             3986+         DC    HL1'7'            CC failed mask
000052FC  00000000 00000000              3987+         DS    2F                extracted PSW after test (has CC)
00005304  FF                             3988+         DC    X'FF'             extracted CC, if test failed
00005305  E5E2E3D9 E2404040              3989+         DC    CL8'VSTRS'       instruction name
00005310  00005394                       3990+         DC    A(RE79+16)       address of v2 source
00005314  000053A4                       3991+         DC    A(RE79+32)       address of v3 source
00005318  000053B4                       3992+         DC    A(RE79+48)       address of v4 source
0000531C  00000010                       3993+         DC    A(16)            result length
00005320  00005384                       3994+REA79    DC    A(RE79)          result address
00005328  00000000 00000000              3995+         DS    FD               gap
00005330  00000000 00000000              3996+V1O79    DS    XL16             V1 output
00005338  00000000 00000000
00005340  00000000 00000000              3997+         DS    FD               gap
                                         3998+*
00005348                                 3999+X79      DS    0F
00005348  E310 5020 0014                 4000+         LGF   R1,V2ADDR        load v2 source
0000534E  E761 0000 0806                 4001+         VL    v22,0(R1)        use v22 to test decoder
00005354  E310 5024 0014                 4002+         LGF   R1,V3ADDR        load v3 source
0000535A  E771 0000 0806                 4003+         VL    v23,0(R1)        use v23 to test decoder
00005360  E310 5028 0014                 4004+         LGF   R1,V4ADDR        load v4 source
00005366  E781 0000 0806                 4005+         VL    v24,0(R1)        use v24 to test decoder
0000536C  E766 7100 8F8B                 4006+         VSTRS V22,V22,V23,V24,1,0     instruction (dest is a source)
00005372  B98D 0020                      4007+         EPSW  R2,R0             extract psw
00005376  5020 500C                      4008+         ST    R2,CCPSW             to save CC
0000537A  E760 5040 080E                 4009+         VST   V22,V1O79         save v1 output
00005380  07FB                           4010+         BR    R11               return
00005384                                 4011+RE79     DC    0F                xl16 expected result
00005384                                 4012+         DROP  R5
00005384  00000000 00000010              4013          DC    XL16'0000000000000010 0000000000000000'   V1
0000538C  00000000 00000000
00005394  01020301 02010201              4014          DC    XL16'0102030102010201 0102030501020300'   v2
0000539C  01020305 01020300
000053A4  01020304 00000700              4015          DC    XL16'0102030400000700 090A0B0C0D0E0F10'   v3
000053AC  090A0B0C 0D0E0F10
000053B4  00000000 000000FF              4016          DC    XL16'00000000000000FF 0000000000000000'   v4
000053BC  00000000 00000000
                                         4017
                                         4018 *Word
                                         4019          VRR_D VSTRS,2,0,0                              no match
000053C8                                 4020+         DS    0FD
000053C8                    000053C8     4021+         USING *,R5             base for test data and test routine
000053C8  00005420                       4022+T80      DC    A(X80)           address of test routine
000053CC  0050                           4023+         DC    H'80'            test number
000053CE  00                             4024+         DC    X'00'
000053CF  02                             4025+         DC    HL1'2'                 m5 used
000053D0  00                             4026+         DC    HL1'0'                 m6 used
000053D1  00                             4027+         DC    HL1'0'            CC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000053D2  07                                       4028+          DC    HL1'7'             CC failed mask
000053D4  00000000 00000000                        4029+          DS    2F                 extracted PSW after test (has CC)
000053DC  FF                                       4030+          DC    X'FF'              extracted CC, if test failed
000053DD  E5E2E3D9 E2404040                        4031+          DC    CL8'VSTRS'        instruction name
000053E8  0000546C                                 4032+          DC    A(RE80+16)        address of v2 source
000053EC  0000547C                                 4033+          DC    A(RE80+32)        address of v3 source
000053F0  0000548C                                 4034+          DC    A(RE80+48)        address of v4 source
000053F4  00000010                                 4035+          DC    A(16)             result length
000053F8  0000545C                                 4036+REA80     DC    A(RE80)           result address
00005400  00000000 00000000                        4037+          DS    FD                gap
00005408  00000000 00000000                        4038+V1O80     DS    XL16              V1 output
00005410  00000000 00000000
00005418  00000000 00000000                        4039+          DS    FD                gap
                                                   4040+*
00005420                                           4041+X80       DS    0F
00005420  E310 5020 0014                00000020   4042+          LGF   R1,V2ADDR         load v2 source
00005426  E761 0000 0806                00000000   4043+          VL    v22,0(R1)         use v22 to test decoder
0000542C  E310 5024 0014                00000024   4044+          LGF   R1,V3ADDR         load v3 source
00005432  E771 0000 0806                00000000   4045+          VL    v23,0(R1)         use v23 to test decoder
00005438  E310 5028 0014                00000028   4046+          LGF   R1,V4ADDR         load v4 source
0000543E  E781 0000 0806                00000000   4047+          VL    v24,0(R1)         use v24 to test decoder
00005444  E766 7200 8F8B                           4048+          VSTRS V22,V22,V23,V24,2,0      instruction (dest is a source)
0000544A  B98D 0020                                4049+          EPSW  R2,R0              extract psw
0000544E  5020 500C                     0000000C   4050+          ST    R2,CCPSW              to save CC
00005452  E760 5040 080E                00005408   4051+          VST   V22,V1O80          save v1 output
00005458  07FB                                     4052+          BR    R11               return
0000545C                                           4053+RE80      DC    0F                xl16 expected result
0000545C                                           4054+          DROP  R5
0000545C  00000000 00000010                        4055           DC    XL16'000000000000010 0000000000000000'   V1
00005464  00000000 00000000
0000546C  01020301 01030400                        4056           DC    XL16'0102030101030400 0102010401020300'   v2
00005474  01020104 01020300
0000547C  01020304 00000000                        4057           DC    XL16'0102030400000000 0000000001020304'   v3
00005484  00000000 01020304
0000548C  00000000 000000FF                        4058           DC    XL16'00000000000000FF 0000000000000000'   v4
00005494  00000000 00000000
                                                   4059
                                                   4060 *Partial Match: ZS=0; v4 substring length > 16; many common substrings
                                                   4061 *Note: substr length is a multiple of element size!
                                                   4062 *Byte
                                                   4063           VRR_D VSTRS,0,0,3                              partial match
000054A0                                           4064+          DS    0FD
000054A0                        000054A0           4065+          USING *,R5              base for test data and test routine
000054A0  000054F8                                 4066+T81       DC    A(X81)            address of test routine
000054A4  0051                                     4067+          DC    H'81'             test number
000054A6  00                                       4068+          DC    X'00'
000054A7  00                                       4069+          DC    HL1'0'                 m5 used
000054A8  00                                       4070+          DC    HL1'0'                 m6 used
000054A9  03                                       4071+          DC    HL1'3'             CC
000054AA  0E                                       4072+          DC    HL1'14'            CC failed mask
000054AC  00000000 00000000                        4073+          DS    2F                 extracted PSW after test (has CC)
000054B4  FF                                       4074+          DC    X'FF'              extracted CC, if test failed
000054B5  E5E2E3D9 E2404040                        4075+          DC    CL8'VSTRS'        instruction name
000054C0  00005544                                 4076+          DC    A(RE81+16)        address of v2 source
000054C4  00005554                                 4077+          DC    A(RE81+32)        address of v3 source
000054C8  00005564                                 4078+          DC    A(RE81+48)        address of v4 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000054CC  00000010                                 4079+          DC    A(16)              result length
000054D0  00005534                                 4080+REA81     DC    A(RE81)            result address
000054D8  00000000 00000000                        4081+          DS    FD                 gap
000054E0  00000000 00000000                        4082+V1O81     DS    XL16               V1 output
000054E8  00000000 00000000
000054F0  00000000 00000000                        4083+          DS    FD                 gap
                                                   4084+*
000054F8                                           4085+X81       DS    0F
000054F8  E310 5020 0014                00000020   4086+          LGF   R1,V2ADDR          load v2 source
000054FE  E761 0000 0806                00000000   4087+          VL    v22,0(R1)          use v22 to test decoder
00005504  E310 5024 0014                00000024   4088+          LGF   R1,V3ADDR          load v3 source
0000550A  E771 0000 0806                00000000   4089+          VL    v23,0(R1)          use v23 to test decoder
00005510  E310 5028 0014                00000028   4090+          LGF   R1,V4ADDR          load v4 source
00005516  E781 0000 0806                00000000   4091+          VL    v24,0(R1)          use v24 to test decoder
0000551C  E766 7000 8F8B                           4092+          VSTRS V22,V22,V23,V24,0,0      instruction (dest is a source)
00005522  B98D 0020                                4093+          EPSW  R2,R0               extract psw
00005526  5020 500C                     0000000C   4094+          ST    R2,CCPSW               to save CC
0000552A  E760 5040 080E                000054E0   4095+          VST   V22,V1O81           save v1 output
00005530  07FB                                     4096+          BR    R11                return
00005534                                           4097+RE81      DC    0F                 xl16 expected result
00005534                                           4098+          DROP  R5
00005534  00000000 0000000C                        4099           DC    XL16'000000000000000C 0000000000000000'   V1
0000553C  00000000 00000000
00005544  01020301 02010201                        4100           DC    XL16'0102030102010201 0102030401020304'   v2
0000554C  01020304 01020304
00005554  01020304 00506070                        4101           DC    XL16'0102030400506070 090A0B0C0D0E0F10'   v3
0000555C  090A0B0C 0D0E0F10
00005564  00000000 000000FF                        4102           DC    XL16'00000000000000FF 0000000000000000'   v4
0000556C  00000000 00000000
                                                   4103
                                                   4104 *Halfword
                                                   4105           VRR_D VSTRS,1,0,3                               partial match
00005578                                           4106+          DS    0FD
00005578                        00005578           4107+          USING *,R5               base for test data and test routine
00005578  000055D0                                 4108+T82       DC    A(X82)             address of test routine
0000557C  0052                                     4109+          DC    H'82'              test number
0000557E  00                                       4110+          DC    X'00'
0000557F  01                                       4111+          DC    HL1'1'                   m5 used
00005580  00                                       4112+          DC    HL1'0'                   m6 used
00005581  03                                       4113+          DC    HL1'3'              CC
00005582  0E                                       4114+          DC    HL1'14'             CC failed mask
00005584  00000000 00000000                        4115+          DS    2F                  extracted PSW after test (has CC)
0000558C  FF                                       4116+          DC    X'FF'               extracted CC, if test failed
0000558D  E5E2E3D9 E2404040                        4117+          DC    CL8'VSTRS'         instruction name
00005598  0000561C                                 4118+          DC    A(RE82+16)         address of v2 source
0000559C  0000562C                                 4119+          DC    A(RE82+32)         address of v3 source
000055A0  0000563C                                 4120+          DC    A(RE82+48)         address of v4 source
000055A4  00000010                                 4121+          DC    A(16)              result length
000055A8  0000560C                                 4122+REA82     DC    A(RE82)            result address
000055B0  00000000 00000000                        4123+          DS    FD                 gap
000055B8  00000000 00000000                        4124+V1O82     DS    XL16               V1 output
000055C0  00000000 00000000
000055C8  00000000 00000000                        4125+          DS    FD                 gap
                                                   4126+*
000055D0                                           4127+X82       DS    0F
000055D0  E310 5020 0014                00000020   4128+          LGF   R1,V2ADDR          load v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000055D6  E761 0000 0806                 00000000  4129+         VL    v22,0(R1)          use v22 to test decoder
000055DC  E310 5024 0014                 00000024  4130+         LGF   R1,V3ADDR          load v3 source
000055E2  E771 0000 0806                 00000000  4131+         VL    v23,0(R1)          use v23 to test decoder
000055E8  E310 5028 0014                 00000028  4132+         LGF   R1,V4ADDR          load v4 source
000055EE  E781 0000 0806                 00000000  4133+         VL    v24,0(R1)          use v24 to test decoder
000055F4  E766 7100 8F8B                           4134+         VSTRS V22,V22,V23,V24,1,0      instruction (dest is a source)
000055FA  B98D 0020                                4135+         EPSW  R2,R0               extract psw
000055FE  5020 500C                      0000000C  4136+         ST    R2,CCPSW               to save CC
00005602  E760 5040 080E                 000055B8  4137+         VST   V22,V1O82           save v1 output
00005608  07FB                                     4138+         BR    R11                return
0000560C                                           4139+RE82     DC    0F                 xl16 expected result
0000560C                                           4140+         DROP  R5
0000560C  00000000 0000000C                        4141          DC    XL16'000000000000000C 0000000000000000'   V1
00005614  00000000 00000000
0000561C  01020301 02010201                        4142          DC    XL16'0102030102010201 0102030501020304'   v2
00005624  01020305 01020304
0000562C  01020304 00000700                        4143          DC    XL16'0102030400000700 090A0B0C0D0E0F10'   v3
00005634  090A0B0C 0D0E0F10
0000563C  00000000 000000FE                        4144          DC    XL16'00000000000000FE 0000000000000000'   v4
00005644  00000000 00000000
                                                   4145
                                                   4146 *Word
                                                   4147          VRR_D VSTRS,2,0,3                               partial match
00005650                                           4148+         DS    0FD
00005650                 00005650                  4149+         USING *,R5               base for test data and test routine
00005650  000056A8                                 4150+T83      DC    A(X83)             address of test routine
00005654  0053                                     4151+         DC    H'83'              test number
00005656  00                                       4152+         DC    X'00'
00005657  02                                       4153+         DC    HL1'2'                   m5 used
00005658  00                                       4154+         DC    HL1'0'                   m6 used
00005659  03                                       4155+         DC    HL1'3'              CC
0000565A  0E                                       4156+         DC    HL1'14'             CC failed mask
0000565C  00000000 00000000                        4157+         DS    2F                  extracted PSW after test (has CC)
00005664  FF                                       4158+         DC    X'FF'               extracted CC, if test failed
00005665  E5E2E3D9 E2404040                       4159+         DC    CL8'VSTRS'         instruction name
00005670  000056F4                                 4160+         DC    A(RE83+16)         address of v2 source
00005674  00005704                                 4161+         DC    A(RE83+32)         address of v3 source
00005678  00005714                                 4162+         DC    A(RE83+48)         address of v4 source
0000567C  00000010                                 4163+         DC    A(16)              result length
00005680  000056E4                                 4164+REA83    DC    A(RE83)            result address
00005688  00000000 00000000                        4165+         DS    FD                 gap
00005690  00000000 00000000                        4166+V1O83    DS    XL16               V1 output
00005698  00000000 00000000
000056A0  00000000 00000000                        4167+         DS    FD                 gap
                                                   4168+*
000056A8                                           4169+X83      DS    0F
000056A8  E310 5020 0014                 00000020  4170+         LGF   R1,V2ADDR          load v2 source
000056AE  E761 0000 0806                 00000000  4171+         VL    v22,0(R1)          use v22 to test decoder
000056B4  E310 5024 0014                 00000024  4172+         LGF   R1,V3ADDR          load v3 source
000056BA  E771 0000 0806                 00000000  4173+         VL    v23,0(R1)          use v23 to test decoder
000056C0  E310 5028 0014                 00000028  4174+         LGF   R1,V4ADDR          load v4 source
000056C6  E781 0000 0806                 00000000  4175+         VL    v24,0(R1)          use v24 to test decoder
000056CC  E766 7200 8F8B                           4176+         VSTRS V22,V22,V23,V24,2,0      instruction (dest is a source)
000056D2  B98D 0020                                4177+         EPSW  R2,R0               extract psw
000056D6  5020 500C                      0000000C  4178+         ST    R2,CCPSW               to save CC
000056DA  E760 5040 080E                 00005690  4179+         VST   V22,V1O83           save v1 output
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000056E0  07FB                           4180+          BR    R11               return
000056E4                                 4181+RE83      DC    0F                xl16 expected result
000056E4                                 4182+          DROP  R5
000056E4  00000000 0000000C             4183           DC    XL16'000000000000000C 0000000000000000'   V1
000056EC  00000000 00000000
000056F4  01020301 01030400             4184           DC    XL16'0102030101030400 0102010401020304'   v2
000056FC  01020104 01020304
00005704  01020304 00000000             4185           DC    XL16'0102030400000000 0000000001020304'   v3
0000570C  00000000 01020304
00005714  00000000 000000FC             4186           DC    XL16'00000000000000FC 0000000000000000'   v4
0000571C  00000000 00000000
                                        4187
                                        4188 *No Match: ZS=0; v4 substring length > 16; many common substrings
                                        4189 *Note: substr length is a NOT a multiple of element size!
                                        4190 *      --> Model dependent result: no match
                                        4191 *Halfword
                                        4192           VRR_D VSTRS,1,0,0                              no match
00005728                                4193+          DS    0FD
00005728                 00005728       4194+          USING *,R5              base for test data and test routine
00005728  00005780                      4195+T84       DC    A(X84)            address of test routine
0000572C  0054                          4196+          DC    H'84'             test number
0000572E  00                            4197+          DC    X'00'
0000572F  01                            4198+          DC    HL1'1'                  m5 used
00005730  00                            4199+          DC    HL1'0'                  m6 used
00005731  00                            4200+          DC    HL1'0'             CC
00005732  07                            4201+          DC    HL1'7'             CC failed mask
00005734  00000000 00000000             4202+          DS    2F                 extracted PSW after test (has CC)
0000573C  FF                            4203+          DC    X'FF'              extracted CC, if test failed
0000573D  E5E2E3D9 E2404040             4204+          DC    CL8'VSTRS'        instruction name
00005748  000057CC                      4205+          DC    A(RE84+16)        address of v2 source
0000574C  000057DC                      4206+          DC    A(RE84+32)        address of v3 source
00005750  000057EC                      4207+          DC    A(RE84+48)        address of v4 source
00005754  00000010                      4208+          DC    A(16)             result length
00005758  000057BC                      4209+REA84     DC    A(RE84)           result address
00005760  00000000 00000000             4210+          DS    FD                gap
00005768  00000000 00000000             4211+V1O84     DS    XL16              V1 output
00005770  00000000 00000000
00005778  00000000 00000000             4212+          DS    FD                gap
                                        4213+*
00005780                                4214+X84       DS    0F
00005780  E310 5020 0014       00000020 4215+          LGF   R1,V2ADDR         load v2 source
00005786  E761 0000 0806       00000000 4216+          VL    v22,0(R1)         use v22 to test decoder
0000578C  E310 5024 0014       00000024 4217+          LGF   R1,V3ADDR         load v3 source
00005792  E771 0000 0806       00000000 4218+          VL    v23,0(R1)         use v23 to test decoder
00005798  E310 5028 0014       00000028 4219+          LGF   R1,V4ADDR         load v4 source
0000579E  E781 0000 0806       00000000 4220+          VL    v24,0(R1)         use v24 to test decoder
000057A4  E766 7100 8F8B                4221+          VSTRS V22,V22,V23,V24,1,0      instruction (dest is a source)
000057AA  B98D 0020                     4222+          EPSW  R2,R0              extract psw
000057AE  5020 500C            0000000C 4223+          ST    R2,CCPSW              to save CC
000057B2  E760 5040 080E       00005768 4224+          VST   V22,V1O84          save v1 output
000057B8  07FB                          4225+          BR    R11               return
000057BC                                4226+RE84      DC    0F                xl16 expected result
000057BC                                4227+          DROP  R5
000057BC  00000000 00000010             4228           DC    XL16'0000000000000010 0000000000000000'   V1
000057C4  00000000 00000000
000057CC  01020301 02010201             4229           DC    XL16'0102030102010201 0102030501020304'   v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000057D4  01020305 01020304
000057DC  01020304 00000700                        4230          DC    XL16'0102030400000700 090A0B0C0D0E0F10'   v3
000057E4  090A0B0C 0D0E0F10
000057EC  00000000 000000FF                        4231          DC    XL16'00000000000000FF 0000000000000000'   v4
000057F4  00000000 00000000
                                                   4232
                                                   4233 *Word
                                                   4234          VRR_D VSTRS,2,0,0                               no match
00005800                                           4235+         DS    0FD
00005800                     00005800              4236+         USING *,R5              base for test data and test routine
00005800  00005858                                 4237+T85      DC    A(X85)            address of test routine
00005804  0055                                     4238+         DC    H'85'             test number
00005806  00                                       4239+         DC    X'00'
00005807  02                                       4240+         DC    HL1'2'                  m5 used
00005808  00                                       4241+         DC    HL1'0'                  m6 used
00005809  00                                       4242+         DC    HL1'0'             CC
0000580A  07                                       4243+         DC    HL1'7'             CC failed mask
0000580C  00000000 00000000                        4244+         DS    2F                 extracted PSW after test (has CC)
00005814  FF                                       4245+         DC    X'FF'              extracted CC, if test failed
00005815  E5E2E3D9 E2404040                        4246+         DC    CL8'VSTRS'        instruction name
00005820  000058A4                                 4247+         DC    A(RE85+16)        address of v2 source
00005824  000058B4                                 4248+         DC    A(RE85+32)        address of v3 source
00005828  000058C4                                 4249+         DC    A(RE85+48)        address of v4 source
0000582C  00000010                                 4250+         DC    A(16)             result length
00005830  00005894                                 4251+REA85    DC    A(RE85)           result address
00005838  00000000 00000000                        4252+         DS    FD                gap
00005840  00000000 00000000                        4253+V1O85    DS    XL16              V1 output
00005848  00000000 00000000
00005850  00000000 00000000                        4254+         DS    FD                gap
                                                   4255+*
00005858                                           4256+X85      DS    0F
00005858  E310 5020 0014                 00000020  4257+         LGF   R1,V2ADDR         load v2 source
0000585E  E761 0000 0806                 00000000  4258+         VL    v22,0(R1)         use v22 to test decoder
00005864  E310 5024 0014                 00000024  4259+         LGF   R1,V3ADDR         load v3 source
0000586A  E771 0000 0806                 00000000  4260+         VL    v23,0(R1)         use v23 to test decoder
00005870  E310 5028 0014                 00000028  4261+         LGF   R1,V4ADDR         load v4 source
00005876  E781 0000 0806                 00000000  4262+         VL    v24,0(R1)         use v24 to test decoder
0000587C  E766 7200 8F8B                           4263+         VSTRS V22,V22,V23,V24,2,0      instruction (dest is a source)
00005882  B98D 0020                                4264+         EPSW  R2,R0              extract psw
00005886  5020 500C                      0000000C  4265+         ST    R2,CCPSW              to save CC
0000588A  E760 5040 080E                 00005840  4266+         VST   V22,V1O85          save v1 output
00005890  07FB                                     4267+         BR    R11               return
00005894                                           4268+RE85     DC    0F                xl16 expected result
00005894                                           4269+         DROP  R5
00005894  00000000 00000010                        4270          DC    XL16'0000000000000010 0000000000000000'   V1
0000589C  00000000 00000000
000058A4  01020301 01030400                        4271          DC    XL16'0102030101030400 0102010401020304'   v2
000058AC  01020104 01020304
000058B4  01020304 00000000                        4272          DC    XL16'0102030400000000 0000000001020304'   v3
000058BC  00000000 01020304
000058C4  00000000 000000FF                        4273          DC    XL16'00000000000000FF 0000000000000000'   v4
000058CC  00000000 00000000
                                                   4274
                                                   4275
000058D4  00000000                                 4276          DC    F'0'     END OF TABLE
000058D8  00000000                                 4277          DC    F'0'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   4279 *
                                                   4280 * table of pointers to individual load test
                                                   4281 *
000058DC                                           4282 E7TESTS  DS    0F
                                                   4283          PTTABLE
000058DC                                           4284+TTABLE   DS    0F
000058DC  00001120                                 4285+         DC    A(T1)
000058E0  000011F8                                 4286+         DC    A(T2)
000058E4  000012D0                                 4287+         DC    A(T3)
000058E8  000013A8                                 4288+         DC    A(T4)
000058EC  00001480                                 4289+         DC    A(T5)
000058F0  00001558                                 4290+         DC    A(T6)
000058F4  00001630                                 4291+         DC    A(T7)
000058F8  00001708                                 4292+         DC    A(T8)
000058FC  000017E0                                 4293+         DC    A(T9)
00005900  000018B8                                 4294+         DC    A(T10)
00005904  00001990                                 4295+         DC    A(T11)
00005908  00001A68                                 4296+         DC    A(T12)
0000590C  00001B40                                 4297+         DC    A(T13)
00005910  00001C18                                 4298+         DC    A(T14)
00005914  00001CF0                                 4299+         DC    A(T15)
00005918  00001DC8                                 4300+         DC    A(T16)
0000591C  00001EA0                                 4301+         DC    A(T17)
00005920  00001F78                                 4302+         DC    A(T18)
00005924  00002050                                 4303+         DC    A(T19)
00005928  00002128                                 4304+         DC    A(T20)
0000592C  00002200                                 4305+         DC    A(T21)
00005930  000022D8                                 4306+         DC    A(T22)
00005934  000023B0                                 4307+         DC    A(T23)
00005938  00002488                                 4308+         DC    A(T24)
0000593C  00002560                                 4309+         DC    A(T25)
00005940  00002638                                 4310+         DC    A(T26)
00005944  00002710                                 4311+         DC    A(T27)
00005948  000027E8                                 4312+         DC    A(T28)
0000594C  000028C0                                 4313+         DC    A(T29)
00005950  00002998                                 4314+         DC    A(T30)
00005954  00002A70                                 4315+         DC    A(T31)
00005958  00002B48                                 4316+         DC    A(T32)
0000595C  00002C20                                 4317+         DC    A(T33)
00005960  00002CF8                                 4318+         DC    A(T34)
00005964  00002DD0                                 4319+         DC    A(T35)
00005968  00002EA8                                 4320+         DC    A(T36)
0000596C  00002F80                                 4321+         DC    A(T37)
00005970  00003058                                 4322+         DC    A(T38)
00005974  00003130                                 4323+         DC    A(T39)
00005978  00003208                                 4324+         DC    A(T40)
0000597C  000032E0                                 4325+         DC    A(T41)
00005980  000033B8                                 4326+         DC    A(T42)
00005984  00003490                                 4327+         DC    A(T43)
00005988  00003568                                 4328+         DC    A(T44)
0000598C  00003640                                 4329+         DC    A(T45)
00005990  00003718                                 4330+         DC    A(T46)
00005994  000037F0                                 4331+         DC    A(T47)
00005998  000038C8                                 4332+         DC    A(T48)
0000599C  000039A0                                 4333+         DC    A(T49)
000059A0  00003A78                                 4334+         DC    A(T50)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000059A4  00003B50                                4335+          DC    A(T51)
000059A8  00003C28                                4336+          DC    A(T52)
000059AC  00003D00                                4337+          DC    A(T53)
000059B0  00003DD8                                4338+          DC    A(T54)
000059B4  00003EB0                                4339+          DC    A(T55)
000059B8  00003F88                                4340+          DC    A(T56)
000059BC  00004060                                4341+          DC    A(T57)
000059C0  00004138                                4342+          DC    A(T58)
000059C4  00004210                                4343+          DC    A(T59)
000059C8  000042E8                                4344+          DC    A(T60)
000059CC  000043C0                                4345+          DC    A(T61)
000059D0  00004498                                4346+          DC    A(T62)
000059D4  00004570                                4347+          DC    A(T63)
000059D8  00004648                                4348+          DC    A(T64)
000059DC  00004720                                4349+          DC    A(T65)
000059E0  000047F8                                4350+          DC    A(T66)
000059E4  000048D0                                4351+          DC    A(T67)
000059E8  000049A8                                4352+          DC    A(T68)
000059EC  00004A80                                4353+          DC    A(T69)
000059F0  00004B58                                4354+          DC    A(T70)
000059F4  00004C30                                4355+          DC    A(T71)
000059F8  00004D08                                4356+          DC    A(T72)
000059FC  00004DE0                                4357+          DC    A(T73)
00005A00  00004EB8                                4358+          DC    A(T74)
00005A04  00004F90                                4359+          DC    A(T75)
00005A08  00005068                                4360+          DC    A(T76)
00005A0C  00005140                                4361+          DC    A(T77)
00005A10  00005218                                4362+          DC    A(T78)
00005A14  000052F0                                4363+          DC    A(T79)
00005A18  000053C8                                4364+          DC    A(T80)
00005A1C  000054A0                                4365+          DC    A(T81)
00005A20  00005578                                4366+          DC    A(T82)
00005A24  00005650                                4367+          DC    A(T83)
00005A28  00005728                                4368+          DC    A(T84)
00005A2C  00005800                                4369+          DC    A(T85)
                                                  4370+*
00005A30  00000000                                4371+          DC    A(0)              END OF TABLE
00005A34  00000000                                4372+          DC    A(0)
                                                  4373
00005A38  00000000                                4374           DC    F'0'     END OF TABLE
00005A3C  00000000                                4375           DC    F'0'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                  4377 ********************************************************************************
                                                  4378 *        Register equates
                                                  4379 ********************************************************************************

                                00000000  00000001  4381 R0       EQU   0
                                00000001  00000001  4382 R1       EQU   1
                                00000002  00000001  4383 R2       EQU   2
                                00000003  00000001  4384 R3       EQU   3
                                00000004  00000001  4385 R4       EQU   4
                                00000005  00000001  4386 R5       EQU   5
                                00000006  00000001  4387 R6       EQU   6
                                00000007  00000001  4388 R7       EQU   7
                                00000008  00000001  4389 R8       EQU   8
                                00000009  00000001  4390 R9       EQU   9
                                0000000A  00000001  4391 R10      EQU   10
                                0000000B  00000001  4392 R11      EQU   11
                                0000000C  00000001  4393 R12      EQU   12
                                0000000D  00000001  4394 R13      EQU   13
                                0000000E  00000001  4395 R14      EQU   14
                                0000000F  00000001  4396 R15      EQU   15

                                                  4398 ********************************************************************************
                                                  4399 *        Register equates
                                                  4400 ********************************************************************************

                              00000000  00000001  4402 V0       EQU   0
                              00000001  00000001  4403 V1       EQU   1
                              00000002  00000001  4404 V2       EQU   2
                              00000003  00000001  4405 V3       EQU   3
                              00000004  00000001  4406 V4       EQU   4
                              00000005  00000001  4407 V5       EQU   5
                              00000006  00000001  4408 V6       EQU   6
                              00000007  00000001  4409 V7       EQU   7
                              00000008  00000001  4410 V8       EQU   8
                              00000009  00000001  4411 V9       EQU   9
                              0000000A  00000001  4412 V10      EQU   10
                              0000000B  00000001  4413 V11      EQU   11
                              0000000C  00000001  4414 V12      EQU   12
                              0000000D  00000001  4415 V13      EQU   13
                              0000000E  00000001  4416 V14      EQU   14
                              0000000F  00000001  4417 V15      EQU   15
                              00000010  00000001  4418 V16      EQU   16
                              00000011  00000001  4419 V17      EQU   17
                              00000012  00000001  4420 V18      EQU   18
                              00000013  00000001  4421 V19      EQU   19
                              00000014  00000001  4422 V20      EQU   20
                              00000015  00000001  4423 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001  4424 V22       EQU   22
                                00000017  00000001  4425 V23       EQU   23
                                00000018  00000001  4426 V24       EQU   24
                                00000019  00000001  4427 V25       EQU   25
                                0000001A  00000001  4428 V26       EQU   26
                                0000001B  00000001  4429 V27       EQU   27
                                0000001C  00000001  4430 V28       EQU   28
                                0000001D  00000001  4431 V29       EQU   29
                                0000001E  00000001  4432 V30       EQU   30
                                0000001F  00000001  4433 V31       EQU   31
                                                    4434
                                                    4435           END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	151	117 147 148 149
CC	U	00000009	1	502	256
CCFOUND	X	00000014	1	508	243 263
CCMASK	U	0000000A	1	503	219
CCMSG	U	0000031C	1	236	231
CCPRTEXP	C	00001096	1	467	260
CCPRTGOT	C	000010A6	1	470	267
CCPRTLINE	C	00001053	16	462	472 270
CCPRTLNG	U	00000055	1	472	269
CCPRTNAME	C	00001080	8	465	253
CCPRTNUM	C	00001063	3	463	251
CCPSW	F	0000000C	4	507	240 678 720 762 805 847 889 932 974 1016 1063 1105 1147 1190 1232 1274 1317 1359 1401 1444 1486 1528 1575 1617 1659 1702 1744 1786 1829 1871 1913 1956 1998 2040 2083 2125 2167 2214 2256 2298 2341 2383 2425 2468 2510 2552 2595 2637 2679 2722 2764 2806 2853 2895 2937 2980 3022 3064 3107 3149 3191 3234 3276 3318 3365 3407 3449 3492 3534 3576 3623 3665 3712 3754 3796 3839 3881 3923 3966 4008 4050 4094 4136 4178 4223 4265
CTLR0	F	00000544	4	406	161 162 163 164
DECNUM	C	000010D4	16	482	248 250 257 259 264 266 285 287 294 296 301 303
E7TEST	4	00000000	88	496	210
E7TESTS	F	000058DC	4	4282	203
EDIT	X	000010A8	18	477	249 258 265 286 295 302
ENDTEST	U	00000418	1	323	208
EOJ	I	00000528	4	396	196 326
EOJPSW	D	00000518	8	394	396
FAILCONT	U	00000408	1	313	
FAILED	F	00001000	4	435	274 315 324
FAILMSG	U	000003A0	1	283	226
FAILPSW	D	00000530	8	398	400
FAILTEST	I	00000540	4	400	327
FB0001	F	00000280	8	180	184 185 187
IMAGE	1	00000000	23104	0	
K	U	00000400	1	419	420 421 422
K64	U	00010000	1	421	
M5	U	00000007	1	500	293
M6	U	00000008	1	501	300
MB	U	00100000	1	422	
MSG	I	00000460	4	356	195 339
MSGCMD	C	000004AE	9	386	369 370
MSGMSG	C	000004B7	95	387	363 384 361
MSGMVC	I	000004A8	6	384	367
MSGOK	I	00000476	2	365	362
MSGRET	I	00000496	4	380	373 376
MSGSAVE	F	0000049C	4	383	359 380
NEXTE7	U	000002D4	1	205	229 318
OPNAME	C	00000015	8	510	253 290
PAGE	U	00001000	1	420	
PRT3	C	000010BE	18	480	249 250 251 258 259 260 265 266 267 286 287 288 295 296 297 302 303 304
PRTLINE	C	00001008	16	444	454 307
PRTLNG	U	0000004B	1	454	306
PRTM5	C	00001044	2	449	297
PRTM6	C	00001050	2	452	304
PRTNAME	C	00001033	8	447	290
PRTNUM	C	00001018	3	445	288

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
R0	U	00000000	1	4381	111 161 164 184 186 187 188 193 212 213 269 273 274 306 314 315 338 340 356 359 361 363 365 380 677 719 761 804 846 888 931 973 1015 1062 1104 1146 1189 1231 1273 1316 1358 1400 1443 1485 1527 1574 1616 1658 1701 1743 1785 1828 1870 1912 1955 1997 2039 2082 2124 2166 2213 2255 2297 2340 2382 2424 2467 2509 2551 2594 2636 2678 2721 2763 2805 2852 2894 2936 2979 3021 3063 3106 3148 3190 3233 3275 3317 3364 3406 3448 3491 3533 3575 3622 3664 3711 3753 3795 3838 3880 3922 3965 4007 4049 4093 4135 4177 4222 4264
R1	U	00000001	1	4382	194 219 220 221 224 225 240 241 242 243 270 307 324 325 370 384 670 671 672 673 674 675 712 713 714 715 716 717 754 755 756 757 758 759 797 798 799 800 801 802 839 840 841 842 843 844 881 882 883 884 885 886 924 925 926 927 928 929 966 967 968 969 970 971 1008 1009 1010 1011 1012 1013 1055 1056 1057 1058 1059 1060 1097 1098 1099 1100 1101 1102 1139 1140 1141 1142 1143 1144 1182 1183 1184 1185 1186 1187 1224 1225 1226 1227 1228 1229 1266 1267 1268 1269 1270 1271 1309 1310 1311 1312 1313 1314 1351 1352 1353 1354 1355 1356 1393 1394 1395 1396 1397 1398 1436 1437 1438 1439 1440 1441 1478 1479 1480 1481 1482 1483 1520 1521 1522 1523 1524 1525 1567 1568 1569 1570 1571 1572 1609 1610 1611 1612 1613 1614 1651 1652 1653 1654 1655 1656 1694 1695 1696 1697 1698 1699 1736 1737 1738 1739 1740 1741 1778 1779 1780 1781 1782 1783 1821 1822 1823 1824 1825 1826 1863 1864 1865 1866 1867 1868 1905 1906 1907 1908 1909 1910 1948 1949 1950 1951 1952 1953 1990 1991 1992 1993 1994 1995 2032 2033 2034 2035 2036 2037 2075 2076 2077 2078 2079 2080 2117 2118 2119 2120 2121 2122 2159 2160 2161 2162 2163 2164 2206 2207 2208 2209 2210 2211 2248 2249 2250 2251 2252 2253 2290 2291 2292 2293 2294 2295 2333 2334 2335 2336 2337 2338 2375 2376 2377 2378 2379 2380 2417 2418 2419 2420 2421 2422 2460 2461 2462 2463 2464 2465 2502 2503 2504 2505 2506 2507 2544 2545 2546 2547 2548 2549 2587 2588 2589 2590 2591 2592 2629 2630 2631 2632 2633 2634 2671 2672 2673 2674 2675 2676 2714 2715 2716 2717 2718 2719 2756 2757 2758 2759 2760 2761 2798 2799 2800 2801 2802 2803 2845 2846 2847 2848 2849 2850 2887 2888 2889 2890 2891 2892 2929 2930 2931 2932 2933 2934 2972 2973 2974 2975 2976 2977 3014 3015 3016 3017 3018 3019 3056 3057 3058 3059 3060 3061 3099 3100 3101 3102 3103 3104 3141 3142 3143 3144 3145 3146 3183 3184 3185 3186 3187 3188 3226 3227 3228 3229 3230 3231 3268 3269 3270 3271 3272 3273 3310 3311 3312 3313 3314 3315 3357 3358 3359 3360 3361 3362 3399 3400 3401 3402 3403 3404 3441 3442 3443 3444 3445 3446 3484 3485 3486 3487 3488 3489 3526 3527 3528 3529 3530 3531 3568 3569 3570 3571 3572 3573 3615 3616 3617 3618 3619 3620 3657 3658 3659 3660 3661 3662 3704 3705 3706 3707 3708 3709 3746 3747 3748 3749 3750 3751 3788 3789 3790 3791 3792 3793 3831 3832 3833 3834 3835 3836 3873 3874 3875 3876 3877 3878 3915 3916 3917 3918 3919 3920 3958 3959 3960 3961 3962 3963 4000 4001 4002 4003 4004 4005 4042 4043 4044 4045 4046 4047 4086 4087 4088 4089 4090 4091 4128 4129 4130 4131 4132 4133 4170 4171 4172 4173 4174 4175 4215 4216 4217 4218 4219 4220 4257 4258 4259 4260 4261 4262
R10	U	0000000A	1	4391	149 158 159
R11	U	0000000B	1	4392	216 217 680 722 764 807 849 891 934 976 1018 1065 1107 1149 1192 1234 1276 1319 1361 1403 1446 1488 1530 1577 1619 1661 1704 1746 1788 1831 1873 1915 1958 2000 2042 2085 2127 2169 2216 2258 2300 2343 2385 2427 2470 2512 2554 2597 2639 2681 2724 2766 2808 2855 2897 2939 2982 3024 3066 3109 3151 3193 3236 3278 3320

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					3367 3409 3451 3494 3536 3578 3625 3667 3714 3756 3798 3841 3883 3925 3968 4010 4052 4096 4138 4180 4225 4267
R12	U	0000000C	1	4393	203 206 228 317
R13	U	0000000D	1	4394	
R14	U	0000000E	1	4395	
R15	U	0000000F	1	4396	271 308 333 343 344
R2	U	00000002	1	4383	195 247 248 255 256 257 262 263 264 284 285 292 293 294 299 300 301 338 339 340 357 359 365 366 367 369 375 380 381 677 678 719 720 761 762 804 805 846 847 888 889 931 932 973 974 1015 1016 1062 1063 1104 1105 1146 1147 1189 1190 1231 1232 1273 1274 1316 1317 1358 1359 1400 1401 1443 1444 1485 1486 1527 1528 1574 1575 1616 1617 1658 1659 1701 1702 1743 1744 1785 1786 1828 1829 1870 1871 1912 1913 1955 1956 1997 1998 2039 2040 2082 2083 2124 2125 2166 2167 2213 2214 2255 2256 2297 2298 2340 2341 2382 2383 2424 2425 2467 2468 2509 2510 2551 2552 2594 2595 2636 2637 2678 2679 2721 2722 2763 2764 2805 2806 2852 2853 2894 2895 2936 2937 2979 2980 3021 3022 3063 3064 3106 3107 3148 3149 3190 3191 3233 3234 3275 3276 3317 3318 3364 3365 3406 3407 3448 3449 3491 3492 3533 3534 3575 3576 3622 3623 3664 3665 3711 3712 3753 3754 3795 3796 3838 3839 3880 3881 3922 3923 3965 3966 4007 4008 4049 4050 4093 4094 4135 4136 4177 4178 4222 4223 4264 4265
R3	U	00000003	1	4384	
R4	U	00000004	1	4385	
R5	U	00000005	1	4386	206 207 210 334 342 649 682 691 724 733 766 776 809 818 851 860 893 903 936 945 978 987 1020 1034 1067 1076 1109 1118 1151 1161 1194 1203 1236 1245 1278 1288 1321 1330 1363 1372 1405 1415 1448 1457 1490 1499 1532 1546 1579 1588 1621 1630 1663 1673 1706 1715 1748 1757 1790 1800 1833 1842 1875 1884 1917 1927 1960 1969 2002 2011 2044 2054 2087 2096 2129 2138 2171 2185 2218 2227 2260 2269 2302 2312 2345 2354 2387 2396 2429 2439 2472 2481 2514 2523 2556 2566 2599 2608 2641 2650 2683 2693 2726 2735 2768 2777 2810 2824 2857 2866 2899 2908 2941 2951 2984 2993 3026 3035 3068 3078 3111 3120 3153 3162 3195 3205 3238 3247 3280 3289 3322 3336 3369 3378 3411 3420 3453 3463 3496 3505 3538 3547 3580 3594 3627 3636 3669 3683 3716 3725 3758 3767 3800 3810 3843 3852 3885 3894 3927 3937 3970 3979 4012 4021 4054 4065 4098 4107 4140 4149 4182 4194 4227 4236 4269
R6	U	00000006	1	4387	
R7	U	00000007	1	4388	
R8	U	00000008	1	4389	147 151 152 153 155
R9	U	00000009	1	4390	148 155 156 158
RE1	F	000011B4	4	681	660 661 662 664
RE10	F	0000194C	4	1066	1045 1046 1047 1049
RE11	F	00001A24	4	1108	1087 1088 1089 1091
RE12	F	00001AFC	4	1150	1129 1130 1131 1133
RE13	F	00001BD4	4	1193	1172 1173 1174 1176
RE14	F	00001CAC	4	1235	1214 1215 1216 1218
RE15	F	00001D84	4	1277	1256 1257 1258 1260
RE16	F	00001E5C	4	1320	1299 1300 1301 1303
RE17	F	00001F34	4	1362	1341 1342 1343 1345
RE18	F	0000200C	4	1404	1383 1384 1385 1387
RE19	F	000020E4	4	1447	1426 1427 1428 1430
RE2	F	0000128C	4	723	702 703 704 706
RE20	F	000021BC	4	1489	1468 1469 1470 1472
RE21	F	00002294	4	1531	1510 1511 1512 1514

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE22	F	0000236C	4	1578	1557	1558	1559	1561
RE23	F	00002444	4	1620	1599	1600	1601	1603
RE24	F	0000251C	4	1662	1641	1642	1643	1645
RE25	F	000025F4	4	1705	1684	1685	1686	1688
RE26	F	000026CC	4	1747	1726	1727	1728	1730
RE27	F	000027A4	4	1789	1768	1769	1770	1772
RE28	F	0000287C	4	1832	1811	1812	1813	1815
RE29	F	00002954	4	1874	1853	1854	1855	1857
RE3	F	00001364	4	765	744	745	746	748
RE30	F	00002A2C	4	1916	1895	1896	1897	1899
RE31	F	00002B04	4	1959	1938	1939	1940	1942
RE32	F	00002BDC	4	2001	1980	1981	1982	1984
RE33	F	00002CB4	4	2043	2022	2023	2024	2026
RE34	F	00002D8C	4	2086	2065	2066	2067	2069
RE35	F	00002E64	4	2128	2107	2108	2109	2111
RE36	F	00002F3C	4	2170	2149	2150	2151	2153
RE37	F	00003014	4	2217	2196	2197	2198	2200
RE38	F	000030EC	4	2259	2238	2239	2240	2242
RE39	F	000031C4	4	2301	2280	2281	2282	2284
RE4	F	0000143C	4	808	787	788	789	791
RE40	F	0000329C	4	2344	2323	2324	2325	2327
RE41	F	00003374	4	2386	2365	2366	2367	2369
RE42	F	0000344C	4	2428	2407	2408	2409	2411
RE43	F	00003524	4	2471	2450	2451	2452	2454
RE44	F	000035FC	4	2513	2492	2493	2494	2496
RE45	F	000036D4	4	2555	2534	2535	2536	2538
RE46	F	000037AC	4	2598	2577	2578	2579	2581
RE47	F	00003884	4	2640	2619	2620	2621	2623
RE48	F	0000395C	4	2682	2661	2662	2663	2665
RE49	F	00003A34	4	2725	2704	2705	2706	2708
RE5	F	00001514	4	850	829	830	831	833
RE50	F	00003B0C	4	2767	2746	2747	2748	2750
RE51	F	00003BE4	4	2809	2788	2789	2790	2792
RE52	F	00003CBC	4	2856	2835	2836	2837	2839
RE53	F	00003D94	4	2898	2877	2878	2879	2881
RE54	F	00003E6C	4	2940	2919	2920	2921	2923
RE55	F	00003F44	4	2983	2962	2963	2964	2966
RE56	F	0000401C	4	3025	3004	3005	3006	3008
RE57	F	000040F4	4	3067	3046	3047	3048	3050
RE58	F	000041CC	4	3110	3089	3090	3091	3093
RE59	F	000042A4	4	3152	3131	3132	3133	3135
RE6	F	000015EC	4	892	871	872	873	875
RE60	F	0000437C	4	3194	3173	3174	3175	3177
RE61	F	00004454	4	3237	3216	3217	3218	3220
RE62	F	0000452C	4	3279	3258	3259	3260	3262
RE63	F	00004604	4	3321	3300	3301	3302	3304
RE64	F	000046DC	4	3368	3347	3348	3349	3351
RE65	F	000047B4	4	3410	3389	3390	3391	3393
RE66	F	0000488C	4	3452	3431	3432	3433	3435
RE67	F	00004964	4	3495	3474	3475	3476	3478
RE68	F	00004A3C	4	3537	3516	3517	3518	3520
RE69	F	00004B14	4	3579	3558	3559	3560	3562
RE7	F	000016C4	4	935	914	915	916	918
RE70	F	00004BEC	4	3626	3605	3606	3607	3609
RE71	F	00004CC4	4	3668	3647	3648	3649	3651
RE72	F	00004D9C	4	3715	3694	3695	3696	3698

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE73	F	00004E74	4	3757	3736	3737	3738	3740
RE74	F	00004F4C	4	3799	3778	3779	3780	3782
RE75	F	00005024	4	3842	3821	3822	3823	3825
RE76	F	000050FC	4	3884	3863	3864	3865	3867
RE77	F	000051D4	4	3926	3905	3906	3907	3909
RE78	F	000052AC	4	3969	3948	3949	3950	3952
RE79	F	00005384	4	4011	3990	3991	3992	3994
RE8	F	0000179C	4	977	956	957	958	960
RE80	F	0000545C	4	4053	4032	4033	4034	4036
RE81	F	00005534	4	4097	4076	4077	4078	4080
RE82	F	0000560C	4	4139	4118	4119	4120	4122
RE83	F	000056E4	4	4181	4160	4161	4162	4164
RE84	F	000057BC	4	4226	4205	4206	4207	4209
RE85	F	00005894	4	4268	4247	4248	4249	4251
RE9	F	00001874	4	1019	998	999	1000	1002
REA1	A	00001150	4	664				
REA10	A	000018E8	4	1049				
REA11	A	000019C0	4	1091				
REA12	A	00001A98	4	1133				
REA13	A	00001B70	4	1176				
REA14	A	00001C48	4	1218				
REA15	A	00001D20	4	1260				
REA16	A	00001DF8	4	1303				
REA17	A	00001ED0	4	1345				
REA18	A	00001FA8	4	1387				
REA19	A	00002080	4	1430				
REA2	A	00001228	4	706				
REA20	A	00002158	4	1472				
REA21	A	00002230	4	1514				
REA22	A	00002308	4	1561				
REA23	A	000023E0	4	1603				
REA24	A	000024B8	4	1645				
REA25	A	00002590	4	1688				
REA26	A	00002668	4	1730				
REA27	A	00002740	4	1772				
REA28	A	00002818	4	1815				
REA29	A	000028F0	4	1857				
REA3	A	00001300	4	748				
REA30	A	000029C8	4	1899				
REA31	A	00002AA0	4	1942				
REA32	A	00002B78	4	1984				
REA33	A	00002C50	4	2026				
REA34	A	00002D28	4	2069				
REA35	A	00002E00	4	2111				
REA36	A	00002ED8	4	2153				
REA37	A	00002FB0	4	2200				
REA38	A	00003088	4	2242				
REA39	A	00003160	4	2284				
REA4	A	000013D8	4	791				
REA40	A	00003238	4	2327				
REA41	A	00003310	4	2369				
REA42	A	000033E8	4	2411				
REA43	A	000034C0	4	2454				
REA44	A	00003598	4	2496				
REA45	A	00003670	4	2538				
REA46	A	00003748	4	2581				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA47	A	00003820	4	2623	
REA48	A	000038F8	4	2665	
REA49	A	000039D0	4	2708	
REA5	A	000014B0	4	833	
REA50	A	00003AA8	4	2750	
REA51	A	00003B80	4	2792	
REA52	A	00003C58	4	2839	
REA53	A	00003D30	4	2881	
REA54	A	00003E08	4	2923	
REA55	A	00003EE0	4	2966	
REA56	A	00003FB8	4	3008	
REA57	A	00004090	4	3050	
REA58	A	00004168	4	3093	
REA59	A	00004240	4	3135	
REA6	A	00001588	4	875	
REA60	A	00004318	4	3177	
REA61	A	000043F0	4	3220	
REA62	A	000044C8	4	3262	
REA63	A	000045A0	4	3304	
REA64	A	00004678	4	3351	
REA65	A	00004750	4	3393	
REA66	A	00004828	4	3435	
REA67	A	00004900	4	3478	
REA68	A	000049D8	4	3520	
REA69	A	00004AB0	4	3562	
REA7	A	00001660	4	918	
REA70	A	00004B88	4	3609	
REA71	A	00004C60	4	3651	
REA72	A	00004D38	4	3698	
REA73	A	00004E10	4	3740	
REA74	A	00004EE8	4	3782	
REA75	A	00004FC0	4	3825	
REA76	A	00005098	4	3867	
REA77	A	00005170	4	3909	
REA78	A	00005248	4	3952	
REA79	A	00005320	4	3994	
REA8	A	00001738	4	960	
REA80	A	000053F8	4	4036	
REA81	A	000054D0	4	4080	
REA82	A	000055A8	4	4122	
REA83	A	00005680	4	4164	
REA84	A	00005758	4	4209	
REA85	A	00005830	4	4251	
REA9	A	00001810	4	1002	
READDR	A	00000030	4	515	224
REG2LOW	U	000000DD	1	425	
REG2PATT	U	AABBCCDD	1	424	
RELEN	A	0000002C	4	514	
RPTDWSAV	D	00000450	8	349	338 340
RPTERROR	I	00000426	4	333	271 308
RPTSAVE	F	00000444	4	346	333 343
RPTSVR5	F	00000448	4	347	334 342
SKL0001	U	0000004E	1	177	193
SKT0001	C	0000022A	20	174	177 194
SVOLDPSW	U	00000140	0	113	
T1	A	00001120	4	650	4285

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T10	A	000018B8	4	1035	4294
T11	A	00001990	4	1077	4295
T12	A	00001A68	4	1119	4296
T13	A	00001B40	4	1162	4297
T14	A	00001C18	4	1204	4298
T15	A	00001CF0	4	1246	4299
T16	A	00001DC8	4	1289	4300
T17	A	00001EA0	4	1331	4301
T18	A	00001F78	4	1373	4302
T19	A	00002050	4	1416	4303
T2	A	000011F8	4	692	4286
T20	A	00002128	4	1458	4304
T21	A	00002200	4	1500	4305
T22	A	000022D8	4	1547	4306
T23	A	000023B0	4	1589	4307
T24	A	00002488	4	1631	4308
T25	A	00002560	4	1674	4309
T26	A	00002638	4	1716	4310
T27	A	00002710	4	1758	4311
T28	A	000027E8	4	1801	4312
T29	A	000028C0	4	1843	4313
T3	A	000012D0	4	734	4287
T30	A	00002998	4	1885	4314
T31	A	00002A70	4	1928	4315
T32	A	00002B48	4	1970	4316
T33	A	00002C20	4	2012	4317
T34	A	00002CF8	4	2055	4318
T35	A	00002DD0	4	2097	4319
T36	A	00002EA8	4	2139	4320
T37	A	00002F80	4	2186	4321
T38	A	00003058	4	2228	4322
T39	A	00003130	4	2270	4323
T4	A	000013A8	4	777	4288
T40	A	00003208	4	2313	4324
T41	A	000032E0	4	2355	4325
T42	A	000033B8	4	2397	4326
T43	A	00003490	4	2440	4327
T44	A	00003568	4	2482	4328
T45	A	00003640	4	2524	4329
T46	A	00003718	4	2567	4330
T47	A	000037F0	4	2609	4331
T48	A	000038C8	4	2651	4332
T49	A	000039A0	4	2694	4333
T5	A	00001480	4	819	4289
T50	A	00003A78	4	2736	4334
T51	A	00003B50	4	2778	4335
T52	A	00003C28	4	2825	4336
T53	A	00003D00	4	2867	4337
T54	A	00003DD8	4	2909	4338
T55	A	00003EB0	4	2952	4339
T56	A	00003F88	4	2994	4340
T57	A	00004060	4	3036	4341
T58	A	00004138	4	3079	4342
T59	A	00004210	4	3121	4343
T6	A	00001558	4	861	4290
T60	A	000042E8	4	3163	4344

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T61	A	000043C0	4	3206	4345
T62	A	00004498	4	3248	4346
T63	A	00004570	4	3290	4347
T64	A	00004648	4	3337	4348
T65	A	00004720	4	3379	4349
T66	A	000047F8	4	3421	4350
T67	A	000048D0	4	3464	4351
T68	A	000049A8	4	3506	4352
T69	A	00004A80	4	3548	4353
T7	A	00001630	4	904	4291
T70	A	00004B58	4	3595	4354
T71	A	00004C30	4	3637	4355
T72	A	00004D08	4	3684	4356
T73	A	00004DE0	4	3726	4357
T74	A	00004EB8	4	3768	4358
T75	A	00004F90	4	3811	4359
T76	A	00005068	4	3853	4360
T77	A	00005140	4	3895	4361
T78	A	00005218	4	3938	4362
T79	A	000052F0	4	3980	4363
T8	A	00001708	4	946	4292
T80	A	000053C8	4	4022	4364
T81	A	000054A0	4	4066	4365
T82	A	00005578	4	4108	4366
T83	A	00005650	4	4150	4367
T84	A	00005728	4	4195	4368
T85	A	00005800	4	4237	4369
T9	A	000017E0	4	988	4293
TESTCC	I	00000318	4	231	221
TESTING	F	00001004	4	436	213
TESTREST	U	00000300	1	223	276
TNUM	H	00000004	2	498	212 247 284
TSUB	A	00000000	4	497	216
TTABLE	F	000058DC	4	4284	
V0	U	00000000	1	4402	
V1	U	00000001	1	4403	215
V10	U	0000000A	1	4412	
V11	U	0000000B	1	4413	
V12	U	0000000C	1	4414	
V13	U	0000000D	1	4415	
V14	U	0000000E	1	4416	
V15	U	0000000F	1	4417	
V16	U	00000010	1	4418	
V17	U	00000011	1	4419	
V18	U	00000012	1	4420	
V19	U	00000013	1	4421	
V1FUDGE	X	000010F4	16	489	215
V1O1	X	00001160	16	666	679
V1O10	X	000018F8	16	1051	1064
V1O11	X	000019D0	16	1093	1106
V1O12	X	00001AA8	16	1135	1148
V1O13	X	00001B80	16	1178	1191
V1O14	X	00001C58	16	1220	1233
V1O15	X	00001D30	16	1262	1275
V1O16	X	00001E08	16	1305	1318
V1O17	X	00001EE0	16	1347	1360

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1018	X	00001FB8	16	1389	1402
V1019	X	00002090	16	1432	1445
V102	X	00001238	16	708	721
V1020	X	00002168	16	1474	1487
V1021	X	00002240	16	1516	1529
V1022	X	00002318	16	1563	1576
V1023	X	000023F0	16	1605	1618
V1024	X	000024C8	16	1647	1660
V1025	X	000025A0	16	1690	1703
V1026	X	00002678	16	1732	1745
V1027	X	00002750	16	1774	1787
V1028	X	00002828	16	1817	1830
V1029	X	00002900	16	1859	1872
V103	X	00001310	16	750	763
V1030	X	000029D8	16	1901	1914
V1031	X	00002AB0	16	1944	1957
V1032	X	00002B88	16	1986	1999
V1033	X	00002C60	16	2028	2041
V1034	X	00002D38	16	2071	2084
V1035	X	00002E10	16	2113	2126
V1036	X	00002EE8	16	2155	2168
V1037	X	00002FC0	16	2202	2215
V1038	X	00003098	16	2244	2257
V1039	X	00003170	16	2286	2299
V104	X	000013E8	16	793	806
V1040	X	00003248	16	2329	2342
V1041	X	00003320	16	2371	2384
V1042	X	000033F8	16	2413	2426
V1043	X	000034D0	16	2456	2469
V1044	X	000035A8	16	2498	2511
V1045	X	00003680	16	2540	2553
V1046	X	00003758	16	2583	2596
V1047	X	00003830	16	2625	2638
V1048	X	00003908	16	2667	2680
V1049	X	000039E0	16	2710	2723
V105	X	000014C0	16	835	848
V1050	X	00003AB8	16	2752	2765
V1051	X	00003B90	16	2794	2807
V1052	X	00003C68	16	2841	2854
V1053	X	00003D40	16	2883	2896
V1054	X	00003E18	16	2925	2938
V1055	X	00003EF0	16	2968	2981
V1056	X	00003FC8	16	3010	3023
V1057	X	000040A0	16	3052	3065
V1058	X	00004178	16	3095	3108
V1059	X	00004250	16	3137	3150
V106	X	00001598	16	877	890
V1060	X	00004328	16	3179	3192
V1061	X	00004400	16	3222	3235
V1062	X	000044D8	16	3264	3277
V1063	X	000045B0	16	3306	3319
V1064	X	00004688	16	3353	3366
V1065	X	00004760	16	3395	3408
V1066	X	00004838	16	3437	3450
V1067	X	00004910	16	3480	3493
V1068	X	000049E8	16	3522	3535

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1069	X	00004AC0	16	3564	3577
V107	X	00001670	16	920	933
V1070	X	00004B98	16	3611	3624
V1071	X	00004C70	16	3653	3666
V1072	X	00004D48	16	3700	3713
V1073	X	00004E20	16	3742	3755
V1074	X	00004EF8	16	3784	3797
V1075	X	00004FD0	16	3827	3840
V1076	X	000050A8	16	3869	3882
V1077	X	00005180	16	3911	3924
V1078	X	00005258	16	3954	3967
V1079	X	00005330	16	3996	4009
V108	X	00001748	16	962	975
V1080	X	00005408	16	4038	4051
V1081	X	000054E0	16	4082	4095
V1082	X	000055B8	16	4124	4137
V1083	X	00005690	16	4166	4179
V1084	X	00005768	16	4211	4224
V1085	X	00005840	16	4253	4266
V109	X	00001820	16	1004	1017
V1OUTPUT	X	00000040	16	517	225
V2	U	00000002	1	4404	
V20	U	00000014	1	4422	
V21	U	00000015	1	4423	
V22	U	00000016	1	4424	671 676 679 713 718 721 755 760 763 798 803 806 840 845 848 882 887 890 925 930 933 967 972 975 1009 1014 1017 1056 1061 1064 1098 1103 1106 1140 1145 1148 1183 1188 1191 1225 1230 1233 1267 1272 1275 1310 1315 1318 1352 1357 1360 1394 1399 1402 1437 1442 1445 1479 1484 1487 1521 1526 1529 1568 1573 1576 1610 1615 1618 1652 1657 1660 1695 1700 1703 1737 1742 1745 1779 1784 1787 1822 1827 1830 1864 1869 1872 1906 1911 1914 1949 1954 1957 1991 1996 1999 2033 2038 2041 2076 2081 2084 2118 2123 2126 2160 2165 2168 2207 2212 2215 2249 2254 2257 2291 2296 2299 2334 2339 2342 2376 2381 2384 2418 2423 2426 2461 2466 2469 2503 2508 2511 2545 2550 2553 2588 2593 2596 2630 2635 2638 2672 2677 2680 2715 2720 2723 2757 2762 2765 2799 2804 2807 2846 2851 2854 2888 2893 2896 2930 2935 2938 2973 2978 2981 3015 3020 3023 3057 3062 3065 3100 3105 3108 3142 3147 3150 3184 3189 3192 3227 3232 3235 3269 3274 3277 3311 3316 3319 3358 3363 3366 3400 3405 3408 3442 3447 3450 3485 3490 3493 3527 3532 3535 3569 3574 3577 3616 3621 3624 3658 3663 3666 3705 3710 3713 3747 3752 3755 3789 3794 3797 3832 3837 3840 3874 3879 3882 3916 3921 3924 3959 3964 3967 4001 4006 4009 4043 4048 4051 4087 4092 4095 4129 4134 4137 4171 4176 4179 4216 4221 4224 4258 4263 4266
V23	U	00000017	1	4425	673 676 715 718 757 760 800 803 842 845 884 887 927 930 969 972 1011 1014 1058 1061 1100 1103 1142 1145 1185 1188 1227 1230 1269 1272 1312 1315 1354 1357 1396 1399 1439 1442 1481 1484 1523 1526 1570 1573 1612 1615 1654 1657 1697 1700 1739 1742 1781 1784 1824 1827 1866 1869 1908 1911 1951 1954 1993 1996 2035 2038 2078 2081 2120 2123 2162 2165 2209 2212 2251 2254 2293 2296 2336 2339 2378 2381 2420 2423 2463 2466 2505 2508 2547 2550 2590 2593 2632 2635 2674 2677 2717 2720 2759 2762 2801 2804 2848 2851 2890 2893 2932 2935 2975 2978 3017 3020 3059 3062 3102 3105 3144 3147 3186 3189 3229 3232 3271 3274 3313 3316 3360 3363 3402 3405 3444 3447 3487 3490 3529 3532 3571 3574 3618 3621 3660 3663 3707 3710 3749 3752 3791 3794 3834 3837 3876 3879 3918 3921 3961 3964

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					4003 4006 4045 4048 4089 4092 4131 4134 4173 4176 4218 4221 4260 4263
V24	U	00000018	1	4426	675 676 717 718 759 760 802 803 844 845 886 887 929 930 971 972 1013 1014 1060 1061 1102 1103 1144 1145 1187 1188 1229 1230 1271 1272 1314 1315 1356 1357 1398 1399 1441 1442 1483 1484 1525 1526 1572 1573 1614 1615 1656 1657 1699 1700 1741 1742 1783 1784 1826 1827 1868 1869 1910 1911 1953 1954 1995 1996 2037 2038 2080 2081 2122 2123 2164 2165 2211 2212 2253 2254 2295 2296 2338 2339 2380 2381 2422 2423 2465 2466 2507 2508 2549 2550 2592 2593 2634 2635 2676 2677 2719 2720 2761 2762 2803 2804 2850 2851 2892 2893 2934 2935 2977 2978 3019 3020 3061 3062 3104 3105 3146 3147 3188 3189 3231 3232 3273 3274 3315 3316 3362 3363 3404 3405 3446 3447 3489 3490 3531 3532 3573 3574 3620 3621 3662 3663 3709 3710 3751 3752 3793 3794 3836 3837 3878 3879 3920 3921 3963 3964 4005 4006 4047 4048 4091 4092 4133 4134 4175 4176 4220 4221 4262 4263
V25	U	00000019	1	4427	
V26	U	0000001A	1	4428	
V27	U	0000001B	1	4429	
V28	U	0000001C	1	4430	
V29	U	0000001D	1	4431	
V2ADDR	A	00000020	4	511	670 712 754 797 839 881 924 966 1008 1055 1097 1139 1182 1224 1266 1309 1351 1393 1436 1478 1520 1567 1609 1651 1694 1736 1778 1821 1863 1905 1948 1990 2032 2075 2117 2159 2206 2248 2290 2333 2375 2417 2460 2502 2544 2587 2629 2671 2714 2756 2798 2845 2887 2929 2972 3014 3056 3099 3141 3183 3226 3268 3310 3357 3399 3441 3484 3526 3568 3615 3657 3704 3746 3788 3831 3873 3915 3958 4000 4042 4086 4128 4170 4215 4257
V3	U	00000003	1	4405	
V30	U	0000001E	1	4432	
V31	U	0000001F	1	4433	
V3ADDR	A	00000024	4	512	672 714 756 799 841 883 926 968 1010 1057 1099 1141 1184 1226 1268 1311 1353 1395 1438 1480 1522 1569 1611 1653 1696 1738 1780 1823 1865 1907 1950 1992 2034 2077 2119 2161 2208 2250 2292 2335 2377 2419 2462 2504 2546 2589 2631 2673 2716 2758 2800 2847 2889 2931 2974 3016 3058 3101 3143 3185 3228 3270 3312 3359 3401 3443 3486 3528 3570 3617 3659 3706 3748 3790 3833 3875 3917 3960 4002 4044 4088 4130 4172 4217 4259
V4	U	00000004	1	4406	
V4ADDR	A	00000028	4	513	674 716 758 801 843 885 928 970 1012 1059 1101 1143 1186 1228 1270 1313 1355 1397 1440 1482 1524 1571 1613 1655 1698 1740 1782 1825 1867 1909 1952 1994 2036 2079 2121 2163 2210 2252 2294 2337 2379 2421 2464 2506 2548 2591 2633 2675 2718 2760 2802 2849 2891 2933 2976 3018 3060 3103 3145 3187 3230 3272 3314 3361 3403 3445 3488 3530 3572 3619 3661 3708 3750 3792 3835 3877 3919 3962 4004 4046 4090 4132 4174 4219 4261
V5	U	00000005	1	4407	
V6	U	00000006	1	4408	
V7	U	00000007	1	4409	
V8	U	00000008	1	4410	
V9	U	00000009	1	4411	
X0001	U	000002A8	1	183	171 184
X1	F	00001178	4	669	650
X10	F	00001910	4	1054	1035
X11	F	000019E8	4	1096	1077
X12	F	00001AC0	4	1138	1119

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X13	F	00001B98	4	1181	1162
X14	F	00001C70	4	1223	1204
X15	F	00001D48	4	1265	1246
X16	F	00001E20	4	1308	1289
X17	F	00001EF8	4	1350	1331
X18	F	00001FD0	4	1392	1373
X19	F	000020A8	4	1435	1416
X2	F	00001250	4	711	692
X20	F	00002180	4	1477	1458
X21	F	00002258	4	1519	1500
X22	F	00002330	4	1566	1547
X23	F	00002408	4	1608	1589
X24	F	000024E0	4	1650	1631
X25	F	000025B8	4	1693	1674
X26	F	00002690	4	1735	1716
X27	F	00002768	4	1777	1758
X28	F	00002840	4	1820	1801
X29	F	00002918	4	1862	1843
X3	F	00001328	4	753	734
X30	F	000029F0	4	1904	1885
X31	F	00002AC8	4	1947	1928
X32	F	00002BA0	4	1989	1970
X33	F	00002C78	4	2031	2012
X34	F	00002D50	4	2074	2055
X35	F	00002E28	4	2116	2097
X36	F	00002F00	4	2158	2139
X37	F	00002FD8	4	2205	2186
X38	F	000030B0	4	2247	2228
X39	F	00003188	4	2289	2270
X4	F	00001400	4	796	777
X40	F	00003260	4	2332	2313
X41	F	00003338	4	2374	2355
X42	F	00003410	4	2416	2397
X43	F	000034E8	4	2459	2440
X44	F	000035C0	4	2501	2482
X45	F	00003698	4	2543	2524
X46	F	00003770	4	2586	2567
X47	F	00003848	4	2628	2609
X48	F	00003920	4	2670	2651
X49	F	000039F8	4	2713	2694
X5	F	000014D8	4	838	819
X50	F	00003AD0	4	2755	2736
X51	F	00003BA8	4	2797	2778
X52	F	00003C80	4	2844	2825
X53	F	00003D58	4	2886	2867
X54	F	00003E30	4	2928	2909
X55	F	00003F08	4	2971	2952
X56	F	00003FE0	4	3013	2994
X57	F	000040B8	4	3055	3036
X58	F	00004190	4	3098	3079
X59	F	00004268	4	3140	3121
X6	F	000015B0	4	880	861
X60	F	00004340	4	3182	3163
X61	F	00004418	4	3225	3206
X62	F	000044F0	4	3267	3248
X63	F	000045C8	4	3309	3290

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X64	F	000046A0	4	3356	3337
X65	F	00004778	4	3398	3379
X66	F	00004850	4	3440	3421
X67	F	00004928	4	3483	3464
X68	F	00004A00	4	3525	3506
X69	F	00004AD8	4	3567	3548
X7	F	00001688	4	923	904
X70	F	00004BB0	4	3614	3595
X71	F	00004C88	4	3656	3637
X72	F	00004D60	4	3703	3684
X73	F	00004E38	4	3745	3726
X74	F	00004F10	4	3787	3768
X75	F	00004FE8	4	3830	3811
X76	F	000050C0	4	3872	3853
X77	F	00005198	4	3914	3895
X78	F	00005270	4	3957	3938
X79	F	00005348	4	3999	3980
X8	F	00001760	4	965	946
X80	F	00005420	4	4041	4022
X81	F	000054F8	4	4085	4066
X82	F	000055D0	4	4127	4108
X83	F	000056A8	4	4169	4150
X84	F	00005780	4	4214	4195
X85	F	00005858	4	4256	4237
X9	F	00001838	4	1007	988
XC0001	U	000002D0	1	197	189
ZVE7TST	J	00000000	23104	110	113 115 119 123 434 111
=A(E7TESTS)	A	00000550	4	411	203
=AL2(L'MSGMSG)	R	0000055E	2	415	361
=F'1'	F	00000558	4	413	273 314
=F'64'	F	0000054C	4	410	188
=H'0'	H	0000055C	2	414	356
=XL4'3'	X	00000554	4	412	242

```
 MACRO   DEFN  REFERENCES

FCHECK     63    170
PTTABLE   604   4283
VRR_D     536    647    689    731    774    816    858    901    943    985   1032   1074   1116   1159   1201   1243   1286   1328
                1370   1413   1455   1497   1544   1586   1628   1671   1713   1755   1798   1840   1882   1925   1967   2009   2052
                2094   2136   2183   2225   2267   2310   2352   2394   2437   2479   2521   2564   2606   2648   2691   2733   2775
                2822   2864   2906   2949   2991   3033   3076   3118   3160   3203   3245   3287   3334   3376   3418   3461   3503
                3545   3592   3634   3681   3723   3765   3808   3850   3892   3935   3977   4019   4063   4105   4147   4192   4234
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   DESC      SYMBOL    SIZE      POS         ADDR

Entry: 0

Image       IMAGE     23104   0000-5A3F   0000-5A3F
  Region              23104   0000-5A3F   0000-5A3F
    CSECT   ZVE7TST   23104   0000-5A3F   0000-5A3F
```

```
   STMT                          FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e7-25-VSTRS.asm

** NO ERRORS FOUND **
```