```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    2 ************************************************************************
                                                    3 *
                                                    4 *   Zvector E7 instruction tests for VRR-c encoded:
                                                    5 *
                                                    6 *   E7A1 VMLH   - Vector Multiply Logical High
                                                    7 *   E7A2 VML    - Vector Multiply Low
                                                    8 *   E7A3 VMH    - Vector Multiply High
                                                    9 *   E7A4 VMLE   - Vector Multiply Logical Even
                                                   10 *   E7A5 VMLO   - Vector Multiply Logical Odd
                                                   11 *   E7A6 VME    - Vector Multiply Even
                                                   12 *   E7A7 VMO    - Vector Multiply Odd
                                                   13 *
                                                   14 *        James Wekel March 2025
                                                   15 ************************************************************************


                                                   17 ************************************************************************
                                                   18 *
                                                   19 *        basic instruction tests
                                                   20 *
                                                   21 ************************************************************************
                                                   22 *  This program tests proper functioning of the z/arch E7 VRR-c vector
                                                   23 *  multiply (logical high, low, high, logical even, logical odd,
                                                   24 *  even, and odd) instructions.
                                                   25 *  Exceptions are not tested.
                                                   26 *
                                                   27 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                   28 *  obvious coding errors.  None of the tests are thorough.  They are
                                                   29 *  NOT designed to test all aspects of any of the instructions.
                                                   30 *
                                                   31 ************************************************************************
                                                   32 *
                                                   33 *   *Testcase zvector-e7-09-multiply
                                                   34 *   *
                                                   35 *   *   Zvector E7 instruction tests for VRR-c encoded:
                                                   36 *   *
                                                   37 *   *   E7A1 VMLH   - Vector Multiply Logical High
                                                   38 *   *   E7A2 VML    - Vector Multiply Low
                                                   39 *   *   E7A3 VMH    - Vector Multiply High
                                                   40 *   *   E7A4 VMLE   - Vector Multiply Logical Even
                                                   41 *   *   E7A5 VMLO   - Vector Multiply Logical Odd
                                                   42 *   *   E7A6 VME    - Vector Multiply Even
                                                   43 *   *   E7A7 VMO    - Vector Multiply Odd
                                                   44 *   *
                                                   45 *   *   # ------------------------------------------------------------
                                                   46 *   *   #  This tests only the basic function of the instructions.
                                                   47 *   *   #  Exceptions are NOT tested.
                                                   48 *   *   # ------------------------------------------------------------
                                                   49 *   *
                                                   50 *   mainsize    2
                                                   51 *   numcpu      1
                                                   52 *   sysclear
                                                   53 *   archlvl     z/Arch
                                                   54 *
                                                   55 *   loadcore    "$(testpath)/zvector-e7-09-multiply.core" 0x0
                                                   56 *
```

```
 LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      57 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                      58 *   runtest     2
                                                      59 *   diag8cmd    disable   # (reset back to default)
                                                      60 *
                                                      61 *   *Done
                                                      62 *
                                                      63 ********************************************************************************
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                      65 ************************************************************************
                                                      66 *        FCHECK Macro - Is a Facility Bit set?
                                                      67 *
                                                      68 *        If the facility bit is NOT set, an message is issued and
                                                      69 *        the test is skipped.
                                                      70 *
                                                      71 *        Fcheck uses R0, R1 and R2
                                                      72 *
                                                      73 * eg.    FCHECK 134,'vector-packed-decimal'
                                                      74 ************************************************************************
                                                      75          MACRO
                                                      76          FCHECK &BITNO,&NOTSETMSG
                                                      77 .*                      &BITNO : facility bit number to check
                                                      78 .*                      &NOTSETMSG : 'facility name'
                                                      79          LCLA  &FBBYTE           Facility bit in Byte
                                                      80          LCLA  &FBBIT            Facility bit within Byte
                                                      81
                                                      82          LCLA  &L(8)
                                                      83 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                      84
                                                      85 &FBBYTE  SETA  &BITNO/8
                                                      86 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                      87 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                      88
                                                      89          B     X&SYSNDX
                                                      90 *                                       Fcheck data area
                                                      91 *                                       skip messgae
                                                      92 SKT&SYSNDX DC  C'    Skipping tests: '
                                                      93          DC    C&NOTSETMSG
                                                      94          DC    C' (bit &BITNO) is not installed.'
                                                      95 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                      96 *                                       facility bits
                                                      97          DS    FD                       gap
                                                      98 FB&SYSNDX DS   4FD
                                                      99          DS    FD                       gap
                                                     100 *
                                                     101 X&SYSNDX EQU *
                                                     102          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                     103          STFLE FB&SYSNDX                get facility bits
                                                     104
                                                     105          XGR   R0,R0
                                                     106          IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                     107          N     R0,=F'&FBBIT'            is bit set?
                                                     108          BNZ   XC&SYSNDX
                                                     109 *
                                                     110 * facility bit not set, issue message and exit
                                                     111 *
                                                     112          LA    R0,SKL&SYSNDX            message length
                                                     113          LA    R1,SKT&SYSNDX            message address
                                                     114          BAL   R2,MSG
                                                     115
                                                     116          B     EOJ
                                                     117 XC&SYSNDX EQU *
                                                     118          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     120 ********************************************************************************
                                                     121 *        Low core PSWs
                                                     122 ********************************************************************************
                               00000000  000043FF   123 ZVE7TST  START 0
00000000                       00000000             124          USING ZVE7TST,R0            Low core addressability
                                                     125
                               00000140  00000000   126 SVOLDPSW EQU   ZVE7TST+X'140'        z/Arch Supervisor call old PSW

00000000                       00000000  000001A0   128          ORG   ZVE7TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                         129          DC    X'0000000180000000'
000001A8  00000000 00000200                         130          DC    AD(BEGIN)

000001B0                       000001B0  000001D0   132          ORG   ZVE7TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                         133          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                         134          DC    AD(X'DEAD')

000001E0                       000001E0  00000200   136          ORG   ZVE7TST+X'200'        Start of actual test program...

                                                     138 ********************************************************************************
                                                     139 *                The actual "ZVE7TST" program itself...
                                                     140 ********************************************************************************
                                                     141 *
                                                     142 *  Architecture Mode: z/Arch
                                                     143 *  Register Usage:
                                                     144 *
                                                     145 *    R0       (work)
                                                     146 *    R1-4     (work)
                                                     147 *    R5       Testing control table - current test base
                                                     148 *    R6-R7    (work)
                                                     149 *    R8       First base register
                                                     150 *    R9       Second base register
                                                     151 *    R10      Third base register
                                                     152 *    R11      E7TEST call return
                                                     153 *    R12      E7TESTS register
                                                     154 *    R13      (work)
                                                     155 *    R14      Subroutine call
                                                     156 *    R15      Secondary Subroutine call or work
                                                     157 *
                                                     158 ********************************************************************************

00000200                       00000200             160          USING  BEGIN,R8         FIRST Base Register
00000200                       00001200             161          USING  BEGIN+4096,R9    SECOND Base Register
00000200                       00002200             162          USING  BEGIN+8192,R10   THIRD Base Register

00000200  0580                                       164 BEGIN    BALR  R8,0              Initalize FIRST base register
00000202  0680                                       165          BCTR  R8,0              Initalize FIRST base register
00000204  0680                                       166          BCTR  R8,0              Initalize FIRST base register

00000206  4190 8800                    00000800     168          LA    R9,2048(,R8)      Initalize SECOND base register
0000020A  4190 9800                    00000800     169          LA    R9,2048(,R9)      Initalize SECOND base register
                                                     170
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
0000020E  41A0 9800                    00000800   171          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                    00000800   172          LA    R10,2048(,R10)   Initalize THIRD base register
                                                  173
00000216  B600 828C                    0000048C   174          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 828D                    0000048D   175          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 828D                    0000048D   176          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 828C                    0000048C   177          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                  178
                                                  179 ********************************************************************
                                                  180 * Is z/Architecture vector facility installed  (bit 129)
                                                  181 ********************************************************************
                                                  182
                                                  183          FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                    000002A8  184+         B     X0001
                                                  185+*                                 Fcheck data area
                                                  186+*                                 skip messgae
0000022A  40404040 E2928997                       187+SKT0001  DC    C'    Skipping tests: '
0000023E  A961C199 838889A3                       188+         DC    C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                       189+         DC    C' (bit 129) is not installed.'
                           0000004E  00000001     190+SKL0001  EQU   *-SKT0001
                                                  191+*                                 facility bits
00000278  00000000 00000000                       192+         DS    FD               gap
00000280  00000000 00000000                       193+FB0001   DS    4FD
000002A0  00000000 00000000                       194+         DS    FD               gap
                                                  195+*
                           000002A8  00000001     196+X0001    EQU   *
000002A8  4100 0004                    00000004   197+         LA    R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                    00000280   198+         STFLE FB0001           get facility bits
000002B0  B982 0000                               199+         XGR   R0,R0
000002B4  4300 8090                    00000290   200+         IC    R0,FB0001+16     get fbit byte
000002B8  5400 8294                    00000494   201+         N     R0,=F'64'        is bit set?
000002BC  4770 80D0                    000002D0   202+         BNZ   XC0001
                                                  203+*
                                                  204+* facility bit not set, issue message and exit
                                                  205+*
000002C0  4100 004E                    0000004E   206+         LA    R0,SKL0001       message length
000002C4  4110 802A                    0000022A   207+         LA    R1,SKT0001       message address
000002C8  4520 81A8                    000003A8   208+         BAL   R2,MSG
000002CC  47F0 8270                    00000470   209+         B     EOJ
                           000002D0  00000001     210+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    212 ************************************************************************
                                                    213 *               Do tests in the E7TESTS table
                                                    214 ************************************************************************
                                                    215
000002D0  58C0 8298                       00000498 216          L     R12,=A(E7TESTS)       get table of test addresses
                                                    217
                                 000002D4  00000001 218 NEXTE7   EQU   *
000002D4  5850 C000                       00000000 219          L     R5,0(0,R12)       get test address
000002D8  1255                                     220          LTR   R5,R5                  have a test?
000002DA  4780 811E                       0000031E 221          BZ    ENDTEST                   done?
                                                    222
000002DE                          00000000         223          USING E7TEST,R5
                                                    224
000002DE  4800 5004                       00000004 225          LH    R0,TNUM           save current test number
000002E2  5000 8E04                       00001004 226          ST    R0,TESTING        for easy reference
                                                    227
000002E6  E710 8E94 0006                  00001094 228          VL    V1,V1FUDGE
000002EC  58B0 5000                       00000000 229          L     R11,TSUB          get address of test routine
000002F0  05BB                                     230          BALR  R11,R11           do test
                                                    231
000002F2  E310 501C 0014                  0000001C 232          LGF   R1,READDR         get address of expected result
000002F8  D50F 5028 1000        00000028  00000000 233          CLC   V1OUTPUT,0(R1)    valid?
000002FE  4770 810A                       0000030A 234          BNE   FAILMSG                no, issue failed message
                                                    235
00000302  41C0 C004                       00000004 236          LA    R12,4(0,R12)      next test address
00000306  47F0 80D4                       000002D4 237          B     NEXTE7
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    239 ************************************************************************
                                                    240 * result not as expected:
                                                    241 *        issue message with test number, instruction under test
                                                    242 *              and instruction m4
                                                    243 ************************************************************************
                               0000030A  00000001   244 FAILMSG  EQU   *
0000030A  45F0 812C                      0000032C   245          BAL   R15,RPTERROR

                                                    247 ************************************************************************
                                                    248 * continue after a failed test
                                                    249 ************************************************************************
                               0000030E  00000001   250 FAILCONT EQU   *
0000030E  5800 829C                      0000049C   251          L     R0,=F'1'          set failed test indicator
00000312  5000 8E00                      00001000   252          ST    R0,FAILED
                                                    253
00000316  41C0 C004                      00000004   254          LA    R12,4(0,R12)      next test address
0000031A  47F0 80D4                      000002D4   255          B     NEXTE7

                                                    257 ************************************************************************
                                                    258 * end of testing; set ending psw
                                                    259 ************************************************************************
                               0000031E  00000001   260 ENDTEST  EQU   *
0000031E  5810 8E00                      00001000   261          L     R1,FAILED         did a test fail?
00000322  1211                                      262          LTR   R1,R1
00000324  4780 8270                      00000470   263          BZ    EOJ               No, exit
00000328  47F0 8288                      00000488   264          B     FAILTEST          Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    266 ********************************************************************************
                                                    267 *        RPTERROR                  Report instruction test in error
                                                    268 ********************************************************************************

0000032C  50F0 8190                        00000390   270 RPTERROR ST    R15,RPTSAVE          Save return address
00000330  5050 8194                        00000394   271          ST    R5,RPTSVR5           Save R5
                                                      272 *
00000334  4820 5004                        00000004   273          LH    R2,TNUM              get test number and convert
00000338  4E20 8E73                        00001073   274          CVD   R2,DECNUM
0000033C  D211 8E5D 8E47       0000105D    00001047   275          MVC   PRT3,EDIT
00000342  DE11 8E5D 8E73       0000105D    00001073   276          ED    PRT3,DECNUM
00000348  D202 8E18 8E6A       00001018    0000106A   277          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                      278
0000034E  D207 8E33 5008       00001033    00000008   279          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                      280 *
00000354  E320 5007 0076                   00000007   281          LB    R2,m4                get m4 and convert
0000035A  4E20 8E73                        00001073   282          CVD   R2,DECNUM
0000035E  D211 8E5D 8E47       0000105D    00001047   283          MVC   PRT3,EDIT
00000364  DE11 8E5D 8E73       0000105D    00001073   284          ED    PRT3,DECNUM
0000036A  D201 8E44 8E6B       00001044    0000106B   285          MVC   PRTM4(2),PRT3+14     fill in message with m4 field

                                                      287 *
                                                      288 *        Use Hercules Diagnose for Message to console
                                                      289 *
00000370  9002 8198                        00000398   290          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000374  4100 003F                        0000003F   291          LA    R0,PRTLNG            message length
00000378  4110 8E08                        00001008   292          LA    R1,PRTLINE             messagfe address
0000037C  4520 81A8                        000003A8   293          BAL   R2,MSG               call Hercules console MSG display
00000380  9802 8198                        00000398   294          LM    R0,R2,RPTDWSAV       restore regs


00000384  5850 8194                        00000394   296          L     R5,RPTSVR5           Restore R5
00000388  58F0 8190                        00000390   297          L     R15,RPTSAVE          Restore return address
0000038C  07FF                                        298          BR    R15                  Return to caller

00000390  00000000                                    300 RPTSAVE  DC    F'0'                 R15 save area
00000394  00000000                                    301 RPTSVR5  DC    F'0'                 R5 save area

00000398  00000000 00000000                           303 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    305 ************************************************************************
                                                    306 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    307 *              R2 = return address
                                                    308 ************************************************************************
000003A8  4900 82A0                      000004A0   310 MSG      CH    R0,=H'0'              Do we even HAVE a message?
000003AC  07D2                                      311          BNHR  R2                    No, ignore

000003AE  9002 81E4                      000003E4   313          STM   R0,R2,MSGSAVE         Save registers

000003B2  4900 82A2                      000004A2   315          CH    R0,=AL2(L'MSGMSG)     Message length within limits?
000003B6  47D0 81BE                      000003BE   316          BNH   MSGOK                 Yes, continue
000003BA  4100 005F                      0000005F   317          LA    R0,L'MSGMSG           No, set to maximum

000003BE  1820                                      319 MSGOK    LR    R2,R0                 Copy length to work register
000003C0  0620                                      320          BCTR  R2,0                  Minus-1 for execute
000003C2  4420 81F0                      000003F0   321          EX    R2,MSGMVC             Copy message to O/P buffer

000003C6  4120 200A                      0000000A   323          LA    R2,1+L'MSGCMD(,R2)    Calculate true command length
000003CA  4110 81F6                      000003F6   324          LA    R1,MSGCMD             Point to true command

000003CE  83120008                                  326          DC    X'83',X'12',X'0008'   Issue Hercules Diagnose X'008'
000003D2  4780 81DE                      000003DE   327          BZ    MSGRET                Return if successful
                                                    328
000003D6  1222                                      329          LTR   R2,R2                 Is Diag8 Ry (R2) 0?
000003D8  4780 81DE                      000003DE   330          BZ    MSGRET                  an error occurred but coninue
                                                    331
000003DC  0000                                      332          DC    H'0'                  CRASH for debugging purposes

000003DE  9802 81E4                      000003E4   334 MSGRET   LM    R0,R2,MSGSAVE         Restore registers
000003E2  07F2                                      335          BR    R2                    Return to caller

000003E4  00000000 00000000                         337 MSGSAVE  DC    3F'0'                 Registers save area
000003F0  D200 81FF 1000      000003FF  00000000    338 MSGMVC   MVC   MSGMSG(0),0(R1)       Executed instruction

000003F6  D4E2C7D5 D6C8405C                         340 MSGCMD   DC    C'MSGNOH * '          *** HERCULES MESSAGE COMMAND ***
000003FF  40404040 40404040                         341 MSGMSG   DC    CL95' '               The message text to be displayed
                                                    342
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    344 ************************************************************************
                                                    345 *        Normal completion or Abnormal termination PSWs
                                                    346 ************************************************************************


00000460  00020001 80000000                         348 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
00000470  B2B2 8260                   00000460      350 EOJ      LPSWE EOJPSW                Normal completion


00000478  00020001 80000000                         352 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
00000488  B2B2 8278                   00000478      354 FAILTEST LPSWE FAILPSW               Abnormal termination


                                                    356 ************************************************************************
                                                    357 *        Working Storage
                                                    358 ************************************************************************


0000048C  00000000                                  360 CTLR0    DS    F                    CR0
00000490  00000000                                  361          DS    F

00000494                                            363          LTORG ,                    Literals pool
00000494  00000040                                  364                =F'64'
00000498  000042A0                                  365                =A(E7TESTS)
0000049C  00000001                                  366                =F'1'
000004A0  0000                                      367                =H'0'
000004A2  005F                                      368                =AL2(L'MSGMSG)
                                                    369
                                                    370 *        some constants
                                                    371
                          00000400  00000001        372 K        EQU   1024                 One KB
                          00001000  00000001        373 PAGE     EQU   (4*K)                Size of one page
                          00010000  00000001        374 K64      EQU   (64*K)               64 KB
                          00100000  00000001        375 MB       EQU   (K*K)                 1 MB
                                                    376
                          AABBCCDD  00000001        377 REG2PATT EQU   X'AABBCCDD'     Polluted Register pattern
                          000000DD  00000001        378 REG2LOW  EQU         X'DD'     (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     380 *=====================================================================
                                                     381 *
                                                     382 *  NOTE: start data on an address that is easy to display
                                                     383 *        within Hercules
                                                     384 *
                                                     385 *=====================================================================
                                                     386
000004A4                      000004A4  00001000     387          ORG   ZVE7TST+X'1000'
00001000  00000000                                   388 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                   389 TESTING  DC    F'0'                    current test number


                                                     391 *
                                                     392 *        failed message and associated editting
                                                     393 *
00001008  40404040 40404040                          394 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                     395 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                          396          DC    c' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                          397 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 884094F4                          398          DC    C' with m4='
00001044  A7A7                                       399 PRTm4    DC    C'xx'
00001046  4B                                         400          DC    C'.'
                                0000003F  00000001   401 PRTLNG   EQU   *-PRTLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     403 ************************************************************************
                                                     404 *        TEST failed : message working storge
                                                     405 ************************************************************************
00001047  40212020 20202020                         406 EDIT     DC    XL18'402120202020202020202020202020202020'
                                                     407
00001059  7E7E7E6E                                   408          DC    C'===>'
0000105D  40404040 40404040                         409 PRT3     DC    CL18' '
0000106F  4C7E7E7E                                   410          DC    C'<==='
00001073  00000000 00000000                         411 DECNUM   DS    CL16


                                                     413 ************************************************************************
                                                     414 *        Vector instruction results, pollution and input
                                                     415 ************************************************************************
00001084                                             416          DS    0F
00001084  00000000 00000000                         417          DS    XL16                                        gap
00001094  FFFFFFFF FFFFFFFF                         418 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010A4  00000000 00000000                         419          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     421 ********************************************************************************
                                                     422 *        E7TEST DSECT
                                                     423 ********************************************************************************


                                                     425 E7TEST   DSECT ,
00000000  00000000                                   426 TSUB     DC    A(0)           pointer  to test
00000004  0000                                       427 TNUM     DC    H'00'          Test Number
00000006  00                                         428          DC    X'00'
00000007  00                                         429 M4       DC    HL1'00'        m4 used
                                                     430
00000008  40404040 40404040                          431 OPNAME   DC    CL8' '         E7 name
00000010  00000000                                   432 V2ADDR   DC    A(0)           address of v2 source
00000014  00000000                                   433 V3ADDR   DC    A(0)           address of v3 source
00000018  00000000                                   434 RELEN    DC    A(0)           RESULT LENGTH
0000001C  00000000                                   435 READDR   DC    A(0)           result (expected) address
00000020  00000000 00000000                          436          DS    FD                gap
00000028  00000000 00000000                          437 V1OUTPUT DS    XL16           V1 Output
00000038  00000000 00000000                          438          DS    FD                gap
                                                     439
                                                     440 *        test routine will be here (from VRR-c macro)
                                                     441 *
                                                     442 *        followed by
                                                     443 *              EXPECTED RESULT


                          00000000  000043FF         445 ZVE7TST  CSECT ,
000010B4                                             446          DS    0F


                                                     448 ********************************************************************************
                                                     449 *     Macros to help build test tables
                                                     450 ********************************************************************************


                                                     452 *
                                                     453 * macro to generate individual test
                                                     454 *
                                                     455          MACRO
                                                     456          VRR_C &INST,&M4
                                                     457 .*                              &INST   - VRR-c instruction under test
                                                     458 .*                              &m4     - m4 field
                                                     459
                                                     460          GBLA  &TNUM
                                                     461 &TNUM    SETA  &TNUM+1
                                                     462
                                                     463          DS    0FD
                                                     464          USING *,R5             base for test data and test routine
                                                     465
                                                     466 T&TNUM   DC    A(X&TNUM)        address of test routine
                                                     467          DC    H'&TNUM'         test number
                                                     468          DC    X'00'
                                                     469          DC    HL1'&M4'         m4
                                                     470          DC    CL8'&INST'       instruction name
                                                     471          DC    A(RE&TNUM+16)    address of v2 source
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      472           DC    A(RE&TNUM+32)     address of v3 source
                                                      473           DC    A(16)             result length
                                                      474 REA&TNUM  DC    A(RE&TNUM)        result address
                                                      475           DS    FD                gap
                                                      476 V1O&TNUM  DS    XL16              V1 output
                                                      477           DS    FD                gap
                                                      478 .*
                                                      479 *
                                                      480 X&TNUM    DS    0F
                                                      481           LGF   R1,V2ADDR         load v2 source
                                                      482           VL    v22,0(R1)         use v22 to test decoder
                                                      483
                                                      484           LGF   R1,V3ADDR         load v3 source
                                                      485           VL    v23,0(R1)         use v23 to test decoder
                                                      486
                                                      487           &INST V22,V22,V23,&M4    test instruction (dest is a source)
                                                      488           VST   V22,V1O&TNUM       save v1 output
                                                      489
                                                      490           BR    R11               return
                                                      491
                                                      492 RE&TNUM   DC    0F                xl16 expected result
                                                      493
                                                      494           DROP  R5
                                                      495           MEND


                                                      497 *
                                                      498 * macro to generate table of pointers to individual tests
                                                      499 *
                                                      500           MACRO
                                                      501           PTTABLE
                                                      502           GBLA  &TNUM
                                                      503           LCLA  &CUR
                                                      504 &CUR      SETA  1
                                                      505 .*
                                                      506 TTABLE    DS    0F
                                                      507 .LOOP     ANOP
                                                      508 .*
                                                      509           DC    A(T&CUR)
                                                      510 .*
                                                      511 &CUR      SETA  &CUR+1
                                                      512           AIF   (&CUR LE &TNUM).LOOP
                                                      513 *
                                                      514           DC    A(0)              END OF TABLE
                                                      515           DC    A(0)
                                                      516 .*
                                                      517           MEND
                                                      518
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    520 ********************************************************************************
                                                    521 *        E7 VRR-c tests
                                                    522 ********************************************************************************
                                                    523          PRINT DATA
                                                    524
                                                    525 *   E7A1 VMLH   - Vector Multiply Logical High
                                                    526 *   E7A2 VML    - Vector Multiply Low
                                                    527 *   E7A3 VMH    - Vector Multiply High
                                                    528 *   E7A4 VMLE   - Vector Multiply Logical Even
                                                    529 *   E7A5 VMLO   - Vector Multiply Logical Odd
                                                    530 *   E7A6 VME    - Vector Multiply Even
                                                    531 *   E7A7 VMO    - Vector Multiply Odd
                                                    532
                                                    533 *        VRR-c instruction, m4
                                                    534 *             followed by
                                                    535 *                16 byte expected result (V1)
                                                    536 *                16 byte V2 source
                                                    537 *                16 byte V3 source
                                                    538 *-------------------------------------------------------------------
                                                    539 *  VMLH   - Vector Multiply Logical High
                                                    540 *-------------------------------------------------------------------
                                                    541 * Byte
                                                    542          VRR_C VMLH,0
000010B8                                            543+         DS    0FD
000010B8                    000010B8                544+         USING *,R5              base for test data and test routine
000010B8  000010F8                                  545+T1       DC    A(X1)             address of test routine
000010BC  0001                                      546+         DC    H'1'              test number
000010BE  00                                        547+         DC    X'00'
000010BF  00                                        548+         DC    HL1'0'            m4
000010C0  E5D4D3C8 40404040                         549+         DC    CL8'VMLH'         instruction name
000010C8  00001130                                  550+         DC    A(RE1+16)         address of v2 source
000010CC  00001140                                  551+         DC    A(RE1+32)         address of v3 source
000010D0  00000010                                  552+         DC    A(16)             result length
000010D4  00001120                                  553+REA1     DC    A(RE1)            result address
000010D8  00000000 00000000                         554+         DS    FD                gap
000010E0  00000000 00000000                         555+V1O1     DS    XL16              V1 output
000010E8  00000000 00000000
000010F0  00000000 00000000                         556+         DS    FD                gap
                                                    557+*
000010F8                                            558+X1       DS    0F
000010F8  E310 5010 0014                 00000010   559+         LGF   R1,V2ADDR         load v2 source
000010FE  E761 0000 0806                 00000000   560+         VL    v22,0(R1)         use v22 to test decoder
00001104  E310 5014 0014                 00000014   561+         LGF   R1,V3ADDR         load v3 source
0000110A  E771 0000 0806                 00000000   562+         VL    v23,0(R1)         use v23 to test decoder
00001110  E766 7000 0EA1                            563+         VMLH  V22,V22,V23,0      test instruction (dest is a source)
00001116  E760 5028 080E                 000010E0   564+         VST   V22,V1O1          save v1 output
0000111C  07FB                                      565+         BR    R11               return
00001120                                            566+RE1      DC    0F                xl16 expected result
00001120                                            567+         DROP  R5
00001120  FE000000 00000002                         568          DC    XL16'FE00000000000002 0000000C000000F4'   result
00001128  0000000C 000000F4
00001130  FF000000 00000019                         569          DC    XL16'FF00000000000019 00000038000000FA'   v2
00001138  00000038 000000FA
00001140  FF000000 00000019                         570          DC    XL16'FF00000000000019 00000038000000FA'   v3
00001148  00000038 000000FA
                                                    571
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    572          VRR_C VMLH,0
00001150                                            573+         DS    0FD
00001150                      00001150              574+         USING *,R5              base for test data and test routine
00001150  00001190                                  575+T2       DC    A(X2)             address of test routine
00001154  0002                                      576+         DC    H'2'              test number
00001156  00                                        577+         DC    X'00'
00001157  00                                        578+         DC    HL1'0'            m4
00001158  E5D4D3C8 40404040                         579+         DC    CL8'VMLH'         instruction name
00001160  000011C8                                  580+         DC    A(RE2+16)         address of v2 source
00001164  000011D8                                  581+         DC    A(RE2+32)         address of v3 source
00001168  00000010                                  582+         DC    A(16)             result length
0000116C  000011B8                                  583+REA2     DC    A(RE2)            result address
00001170  00000000 00000000                         584+         DS    FD                gap
00001178  00000000 00000000                         585+V1O2     DS    XL16              V1 output
00001180  00000000 00000000
00001188  00000000 00000000                         586+         DS    FD                gap
                                                    587+*
00001190                                            588+X2       DS    0F
00001190  E310 5010 0014                00000010    589+         LGF   R1,V2ADDR         load v2 source
00001196  E761 0000 0806                00000000    590+         VL    v22,0(R1)         use v22 to test decoder
0000119C  E310 5014 0014                00000014    591+         LGF   R1,V3ADDR         load v3 source
000011A2  E771 0000 0806                00000000    592+         VL    v23,0(R1)         use v23 to test decoder
000011A8  E766 7000 0EA1                            593+         VMLH  V22,V22,V23,0      test instruction (dest is a source)
000011AE  E760 5028 080E                00001178    594+         VST   V22,V1O2          save v1 output
000011B4  07FB                                      595+         BR    R11               return
000011B8                                            596+RE2      DC    0F                xl16 expected result
000011B8                                            597+         DROP  R5
000011B8  FE000000 00000019                         598          DC    XL16'FE00000000000019 0000038000000FA'   result
000011C0  00000038 000000FA
000011C8  FF020304 05060750                         599          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000011D0  090A0B78 0C0D0EFD
000011D8  FF020304 05060750                         600          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
000011E0  090A0B78 0D0E0FFD
                                                    601
                                                    602          VRR_C VMLH,0
000011E8                                            603+         DS    0FD
000011E8                      000011E8              604+         USING *,R5              base for test data and test routine
000011E8  00001228                                  605+T3       DC    A(X3)             address of test routine
000011EC  0003                                      606+         DC    H'3'              test number
000011EE  00                                        607+         DC    X'00'
000011EF  00                                        608+         DC    HL1'0'            m4
000011F0  E5D4D3C8 40404040                         609+         DC    CL8'VMLH'         instruction name
000011F8  00001260                                  610+         DC    A(RE3+16)         address of v2 source
000011FC  00001270                                  611+         DC    A(RE3+32)         address of v3 source
00001200  00000010                                  612+         DC    A(16)             result length
00001204  00001250                                  613+REA3     DC    A(RE3)            result address
00001208  00000000 00000000                         614+         DS    FD                gap
00001210  00000000 00000000                         615+V1O3     DS    XL16              V1 output
00001218  00000000 00000000
00001220  00000000 00000000                         616+         DS    FD                gap
                                                    617+*
00001228                                            618+X3       DS    0F
00001228  E310 5010 0014                00000010    619+         LGF   R1,V2ADDR         load v2 source
0000122E  E761 0000 0806                00000000    620+         VL    v22,0(R1)         use v22 to test decoder
00001234  E310 5014 0014                00000014    621+         LGF   R1,V3ADDR         load v3 source
0000123A  E771 0000 0806                00000000    622+         VL    v23,0(R1)         use v23 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001240  E766 7000 0EA1                             623+         VMLH  V22,V22,V23,0      test instruction (dest is a source)
00001246  E760 9010 080E                 00001210    624+         VST   V22,V1O3           save v1 output
0000124C  07FB                                       625+         BR    R11               return
00001250                                             626+RE3      DC    0F                xl16 expected result
00001250                                             627+         DROP  R5
00001250  FE000000 0000000C                          628          DC    XL16'FE0000000000000C 0000001C000000FB'   result
00001258  0000001C 000000FB
00001260  FF020304 05060750                          629          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00001268  090A0B78 0C0D0EFD
00001270  FF010102 02030328                          630          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00001278  0405053C 060707FE
                                                     631
                                                     632          VRR_C VMLH,0
00001280                                             633+         DS    0FD
00001280                       00001280              634+         USING *,R5              base for test data and test routine
00001280  000012C0                                   635+T4       DC    A(X4)             address of test routine
00001284  0004                                       636+         DC    H'4'              test number
00001286  00                                         637+         DC    X'00'
00001287  00                                         638+         DC    HL1'0'            m4
00001288  E5D4D3C8 40404040                         639+         DC    CL8'VMLH'         instruction name
00001290  000012F8                                   640+         DC    A(RE4+16)         address of v2 source
00001294  00001308                                   641+         DC    A(RE4+32)         address of v3 source
00001298  00000010                                   642+         DC    A(16)             result length
0000129C  000012E8                                   643+REA4     DC    A(RE4)            result address
000012A0  00000000 00000000                          644+         DS    FD                gap
000012A8  00000000 00000000                          645+V1O4     DS    XL16              V1 output
000012B0  00000000 00000000
000012B8  00000000 00000000                          646+         DS    FD                gap
                                                     647+*
000012C0                                             648+X4       DS    0F
000012C0  E310 5010 0014                 00000010    649+         LGF   R1,V2ADDR         load v2 source
000012C6  E761 0000 0806                 00000000    650+         VL    v22,0(R1)         use v22 to test decoder
000012CC  E310 5014 0014                 00000014    651+         LGF   R1,V3ADDR         load v3 source
000012D2  E771 0000 0806                 00000000    652+         VL    v23,0(R1)         use v23 to test decoder
000012D8  E766 7000 0EA1                             653+         VMLH  V22,V22,V23,0      test instruction (dest is a source)
000012DE  E760 5028 080E                 000012A8    654+         VST   V22,V1O4           save v1 output
000012E4  07FB                                       655+         BR    R11               return
000012E8                                             656+RE4      DC    0F                xl16 expected result
000012E8                                             657+         DROP  R5
000012E8  FE000000 00000003                          658          DC    XL16'FE00000000000003 00000007000000FC'   result
000012F0  00000007 000000FC
000012F8  FF020304 05060750                          659          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00001300  090A0B78 0C0D0EFD
00001308  FF000000 0000000A                          660          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00001310  0101010F 010101FF
                                                     661
                                                     662
                                                     663 * Halfword
                                                     664          VRR_C VMLH,1
00001318                                             665+         DS    0FD
00001318                       00001318              666+         USING *,R5              base for test data and test routine
00001318  00001358                                   667+T5       DC    A(X5)             address of test routine
0000131C  0005                                       668+         DC    H'5'              test number
0000131E  00                                         669+         DC    X'00'
0000131F  01                                         670+         DC    HL1'1'            m4
00001320  E5D4D3C8 40404040                         671+         DC    CL8'VMLH'         instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001328  00001390                                672+         DC    A(RE5+16)          address of v2 source
0000132C  000013A0                                673+         DC    A(RE5+32)          address of v3 source
00001330  00000010                                674+         DC    A(16)              result length
00001334  00001380                                675+REA5     DC    A(RE5)             result address
00001338  00000000 00000000                       676+         DS    FD                 gap
00001340  00000000 00000000                       677+V1O5     DS    XL16               V1 output
00001348  00000000 00000000
00001350  00000000 00000000                       678+         DS    FD                 gap
                                                  679+*
00001358                                          680+X5       DS    0F
00001358  E310 5010 0014                 00000010 681+         LGF   R1,V2ADDR          load v2 source
0000135E  E761 0000 0806                 00000000 682+         VL    v22,0(R1)          use v22 to test decoder
00001364  E310 5014 0014                 00000014 683+         LGF   R1,V3ADDR          load v3 source
0000136A  E771 0000 0806                 00000000 684+         VL    v23,0(R1)          use v23 to test decoder
00001370  E766 7000 1EA1                          685+         VMLH  V22,V22,V23,1       test instruction (dest is a source)
00001376  E760 5028 080E                 00001340 686+         VST   V22,V1O5           save v1 output
0000137C  07FB                                    687+         BR    R11                return
00001380                                          688+RE5      DC    0F                 xl16 expected result
00001380                                          689+         DROP  R5
00001380  FFFE0000 00000000                       690          DC    XL16'FFFE000000000000 000000000000DF15'   result
00001388  00000000 0000DF15
00001390  FFFF0000 00000019                       691          DC    XL16'FFFF000000000019 000000380000EEFA'   v2
00001398  00000038 0000EEFA
000013A0  FFFF0000 00000019                       692          DC    XL16'FFFF000000000019 000000380000EEFA'   v3
000013A8  00000038 0000EEFA
                                                  693
                                                  694          VRR_C VMLH,1
000013B0                                          695+         DS    0FD
000013B0                      000013B0            696+         USING *,R5               base for test data and test routine
000013B0  000013F0                                697+T6       DC    A(X6)              address of test routine
000013B4  0006                                    698+         DC    H'6'               test number
000013B6  00                                      699+         DC    X'00'
000013B7  01                                      700+         DC    HL1'1'             m4
000013B8  E5D4D3C8 40404040                       701+         DC    CL8'VMLH'          instruction name
000013C0  00001428                                702+         DC    A(RE6+16)          address of v2 source
000013C4  00001438                                703+         DC    A(RE6+32)          address of v3 source
000013C8  00000010                                704+         DC    A(16)              result length
000013CC  00001418                                705+REA6     DC    A(RE6)             result address
000013D0  00000000 00000000                       706+         DS    FD                 gap
000013D8  00000000 00000000                       707+V1O6     DS    XL16               V1 output
000013E0  00000000 00000000
000013E8  00000000 00000000                       708+         DS    FD                 gap
                                                  709+*
000013F0                                          710+X6       DS    0F
000013F0  E310 5010 0014                 00000010 711+         LGF   R1,V2ADDR          load v2 source
000013F6  E761 0000 0806                 00000000 712+         VL    v22,0(R1)          use v22 to test decoder
000013FC  E310 5014 0014                 00000014 713+         LGF   R1,V3ADDR          load v3 source
00001402  E771 0000 0806                 00000000 714+         VL    v23,0(R1)          use v23 to test decoder
00001408  E766 7000 1EA1                          715+         VMLH  V22,V22,V23,1       test instruction (dest is a source)
0000140E  E760 5028 080E                 000013D8 716+         VST   V22,V1O6           save v1 output
00001414  07FB                                    717+         BR    R11                return
00001418                                          718+RE6      DC    0F                 xl16 expected result
00001418                                          719+         DROP  R5
00001418  FE040009 00190035                       720          DC    XL16'FE04000900190035 00510083009D00EF'   result
00001420  00510083 009D00EF
00001428  FF020304 05060750                       721          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001430  090A0B78 0C0D0EFD
00001438  FF020304 05060750                          722          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00001440  090A0B78 0D0E0FFD
                                                     723
                                                     724          VRR_C VMLH,1
00001448                                             725+         DS    0FD
00001448                      00001448               726+         USING *,R5              base for test data and test routine
00001448  00001488                                   727+T7       DC    A(X7)             address of test routine
0000144C  0007                                       728+         DC    H'7'              test number
0000144E  00                                         729+         DC    X'00'
0000144F  01                                         730+         DC    HL1'1'            m4
00001450  E5D4D3C8 40404040                          731+         DC    CL8'VMLH'         instruction name
00001458  000014C0                                   732+         DC    A(RE7+16)         address of v2 source
0000145C  000014D0                                   733+         DC    A(RE7+32)         address of v3 source
00001460  00000010                                   734+         DC    A(16)             result length
00001464  000014B0                                   735+REA7     DC    A(RE7)            result address
00001468  00000000 00000000                          736+         DS    FD                gap
00001470  00000000 00000000                          737+V1O7     DS    XL16              V1 output
00001478  00000000 00000000
00001480  00000000 00000000                          738+         DS    FD                gap
                                                     739+*
00001488                                             740+X7       DS    0F
00001488  E310 5010 0014                 00000010    741+         LGF   R1,V2ADDR         load v2 source
0000148E  E761 0000 0806                 00000000    742+         VL    v22,0(R1)         use v22 to test decoder
00001494  E310 5014 0014                 00000014    743+         LGF   R1,V3ADDR         load v3 source
0000149A  E771 0000 0806                 00000000    744+         VL    v23,0(R1)         use v23 to test decoder
000014A0  E766 7000 1EA1                             745+         VMLH  V22,V22,V23,1      test instruction (dest is a source)
000014A6  E760 5028 080E                 00001470    746+         VST   V22,V1O7           save v1 output
000014AC  07FB                                       747+         BR    R11               return
000014B0                                             748+RE7      DC    0F                xl16 expected result
000014B0                                             749+         DROP  R5
000014B0  FE030003 000A0017                          750          DC    XL16'FE030003000A0017 0024003C00480077'   result
000014B8  0024003C 00480077
000014C0  FF020304 05060750                          751          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000014C8  090A0B78 0C0D0EFD
000014D0  FF010102 02030328                          752          DC    XL16'FF01010202030328 0405053C060707FE'   v3
000014D8  0405053C 060707FE
                                                     753
                                                     754          VRR_C VMLH,1
000014E0                                             755+         DS    0FD
000014E0                      000014E0               756+         USING *,R5              base for test data and test routine
000014E0  00001520                                   757+T8       DC    A(X8)             address of test routine
000014E4  0008                                       758+         DC    H'8'              test number
000014E6  00                                         759+         DC    X'00'
000014E7  01                                         760+         DC    HL1'1'            m4
000014E8  E5D4D3C8 40404040                          761+         DC    CL8'VMLH'         instruction name
000014F0  00001558                                   762+         DC    A(RE8+16)         address of v2 source
000014F4  00001568                                   763+         DC    A(RE8+32)         address of v3 source
000014F8  00000010                                   764+         DC    A(16)             result length
000014FC  00001548                                   765+REA8     DC    A(RE8)            result address
00001500  00000000 00000000                          766+         DS    FD                gap
00001508  00000000 00000000                          767+V1O8     DS    XL16              V1 output
00001510  00000000 00000000
00001518  00000000 00000000                          768+         DS    FD                gap
                                                     769+*
00001520                                             770+X8       DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
00001520  E310 5010 0014                 00000010   771+         LGF   R1,V2ADDR          load v2 source
00001526  E761 0000 0806                 00000000   772+         VL    v22,0(R1)          use v22 to test decoder
0000152C  E310 5014 0014                 00000014   773+         LGF   R1,V3ADDR          load v3 source
00001532  E771 0000 0806                 00000000   774+         VL    v23,0(R1)          use v23 to test decoder
00001538  E766 7000 1EA1                            775+         VMLH  V22,V22,V23,1       test instruction (dest is a source)
0000153E  E760 5028 080E                 00001508   776+         VST   V22,V1O8           save v1 output
00001544  07FB                                      777+         BR    R11                return
00001548                                            778+RE8      DC    0F                 xl16 expected result
00001548                                            779+         DROP  R5
00001548  FE020000 00000000                         780          DC    XL16'FE02000000000000 0009000C000C001D'   result
00001550  0009000C 000C001D
00001558  FF020304 05060750                         781          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00001560  090A0B78 0C0D0EFD
00001568  FF000000 0000000A                         782          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00001570  0101010F 010101FF
                                                    783
                                                    784 * Word
                                                    785          VRR_C VMLH,2
00001578                                            786+         DS    0FD
00001578                    00001578                787+         USING *,R5               base for test data and test routine
00001578  000015B8                                  788+T9       DC    A(X9)              address of test routine
0000157C  0009                                      789+         DC    H'9'               test number
0000157E  00                                        790+         DC    X'00'
0000157F  02                                        791+         DC    HL1'2'             m4
00001580  E5D4D3C8 40404040                         792+         DC    CL8'VMLH'          instruction name
00001588  000015F0                                  793+         DC    A(RE9+16)          address of v2 source
0000158C  00001600                                  794+         DC    A(RE9+32)          address of v3 source
00001590  00000010                                  795+         DC    A(16)              result length
00001594  000015E0                                  796+REA9     DC    A(RE9)             result address
00001598  00000000 00000000                         797+         DS    FD                 gap
000015A0  00000000 00000000                         798+V1O9     DS    XL16               V1 output
000015A8  00000000 00000000
000015B0  00000000 00000000                         799+         DS    FD                 gap
                                                    800+*
000015B8                                            801+X9       DS    0F
000015B8  E310 5010 0014                 00000010   802+         LGF   R1,V2ADDR          load v2 source
000015BE  E761 0000 0806                 00000000   803+         VL    v22,0(R1)          use v22 to test decoder
000015C4  E310 5014 0014                 00000014   804+         LGF   R1,V3ADDR          load v3 source
000015CA  E771 0000 0806                 00000000   805+         VL    v23,0(R1)          use v23 to test decoder
000015D0  E766 7000 2EA1                            806+         VMLH  V22,V22,V23,2       test instruction (dest is a source)
000015D6  E760 5028 080E                 000015A0   807+         VST   V22,V1O9           save v1 output
000015DC  07FB                                      808+         BR    R11                return
000015E0                                            809+RE9      DC    0F                 xl16 expected result
000015E0                                            810+         DROP  R5
000015E0  FFFFFFFE 00000002                         811          DC    XL16'FFFFFFFE00000002 00000000DF01235A'   result
000015E8  00000000 DF01235A
000015F0  FFFFFFFF 00019000                         812          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
000015F8  00000038 EEEEEEFA
00001600  FFFFFFFF 00019000                         813          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v3
00001608  00000038 EEEEEEFA
                                                    814
                                                    815          VRR_C VMLH,2
00001610                                            816+         DS    0FD
00001610                    00001610                817+         USING *,R5               base for test data and test routine
00001610  00001650                                  818+T10      DC    A(X10)             address of test routine
00001614  000A                                      819+         DC    H'10'              test number
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001616  00                                       820+          DC    X'00'
00001617  02                                       821+          DC    HL1'2'              m4
00001618  E5D4D3C8 40404040                        822+          DC    CL8'VMLH'           instruction name
00001620  00001688                                 823+          DC    A(RE10+16)          address of v2 source
00001624  00001698                                 824+          DC    A(RE10+32)          address of v3 source
00001628  00000010                                 825+          DC    A(16)               result length
0000162C  00001678                                 826+REA10     DC    A(RE10)             result address
00001630  00000000 00000000                        827+          DS    FD                  gap
00001638  00000000 00000000                        828+V1O10     DS    XL16                V1 output
00001640  00000000 00000000
00001648  00000000 00000000                        829+          DS    FD                  gap
                                                   830+*
00001650                                           831+X10       DS    0F
00001650  E310 5010 0014                 00000010  832+          LGF   R1,V2ADDR           load v2 source
00001656  E761 0000 0806                 00000000  833+          VL    v22,0(R1)           use v22 to test decoder
0000165C  E310 5014 0014                 00000014  834+          LGF   R1,V3ADDR           load v3 source
00001662  E771 0000 0806                 00000000  835+          VL    v23,0(R1)           use v23 to test decoder
00001668  E766 7000 2EA1                           836+          VMLH  V22,V22,V23,2        test instruction (dest is a source)
0000166E  E760 5028 080E                 00001638  837+          VST   V22,V1O10           save v1 output
00001674  07FB                                     838+          BR    R11                 return
00001678                                           839+RE10      DC    0F                  xl16 expected result
00001678                                           840+          DROP  R5
00001678  FE050206 00193C6D                        841           DC    XL16'FE05020600193C6D 0051B52B00AA6E58'   result
00001680  0051B52B 00AA6E58
00001688  FF020304 05060750                        842           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00001690  090A0B0C 0D0E0F7F
00001698  FF020304 05060750                        843           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v3
000016A0  090A0B0C 0D0E0F7F
                                                   844
                                                   845           VRR_C VMLH,2
000016A8                                           846+          DS    0FD
000016A8                         000016A8          847+          USING *,R5                base for test data and test routine
000016A8  000016E8                                 848+T11       DC    A(X11)              address of test routine
000016AC  000B                                     849+          DC    H'11'               test number
000016AE  00                                       850+          DC    X'00'
000016AF  02                                       851+          DC    HL1'2'              m4
000016B0  E5D4D3C8 40404040                        852+          DC    CL8'VMLH'           instruction name
000016B8  00001720                                 853+          DC    A(RE11+16)          address of v2 source
000016BC  00001730                                 854+          DC    A(RE11+32)          address of v3 source
000016C0  00000010                                 855+          DC    A(16)               result length
000016C4  00001710                                 856+REA11     DC    A(RE11)             result address
000016C8  00000000 00000000                        857+          DS    FD                  gap
000016D0  00000000 00000000                        858+V1O11     DS    XL16                V1 output
000016D8  00000000 00000000
000016E0  00000000 00000000                        859+          DS    FD                  gap
                                                   860+*
000016E8                                           861+X11       DS    0F
000016E8  E310 5010 0014                 00000010  862+          LGF   R1,V2ADDR           load v2 source
000016EE  E761 0000 0806                 00000000  863+          VL    v22,0(R1)           use v22 to test decoder
000016F4  E310 5014 0014                 00000014  864+          LGF   R1,V3ADDR           load v3 source
000016FA  E771 0000 0806                 00000000  865+          VL    v23,0(R1)           use v23 to test decoder
00001700  E766 7000 2EA1                           866+          VMLH  V22,V22,V23,2        test instruction (dest is a source)
00001706  E760 5028 080E                 000016D0  867+          VST   V22,V1O11           save v1 output
0000170C  07FB                                     868+          BR    R11                 return
00001710                                           869+RE11      DC    0F                  xl16 expected result
00001710                                           870+          DROP  R5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001710  FE040103 000A1B30                          871          DC    XL16'FE040103000A1B30 0024558D004EB01D'   result
00001718  0024558D 004EB01D
00001720  FF020304 05060750                          872          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00001728  090A0B0C 0D0E0F7F
00001730  FF010102 02030328                          873          DC    XL16'FF01010202030328 0405053C0607073F'   v3
00001738  0405053C 0607073F
                                                     874
                                                     875          VRR_C VMLH,2
00001740                                             876+         DS    0FD
00001740                      00001740               877+         USING *,R5              base for test data and test routine
00001740  00001780                                   878+T12      DC    A(X12)            address of test routine
00001744  000C                                       879+         DC    H'12'             test number
00001746  00                                         880+         DC    X'00'
00001747  02                                         881+         DC    HL1'2'            m4
00001748  E5D4D3C8 40404040                          882+         DC    CL8'VMLH'         instruction name
00001750  000017B8                                   883+         DC    A(RE12+16)        address of v2 source
00001754  000017C8                                   884+         DC    A(RE12+32)        address of v3 source
00001758  00000010                                   885+         DC    A(16)             result length
0000175C  000017A8                                   886+REA12    DC    A(RE12)           result address
00001760  00000000 00000000                         887+         DS    FD                gap
00001768  00000000 00000000                         888+V1O12    DS    XL16              V1 output
00001770  00000000 00000000
00001778  00000000 00000000                         889+         DS    FD                gap
                                                     890+*
00001780                                             891+X12      DS    0F
00001780  E310 5010 0014                 00000010    892+         LGF   R1,V2ADDR         load v2 source
00001786  E761 0000 0806                 00000000    893+         VL    v22,0(R1)         use v22 to test decoder
0000178C  E310 5014 0014                 00000014    894+         LGF   R1,V3ADDR         load v3 source
00001792  E771 0000 0806                 00000000    895+         VL    v23,0(R1)         use v23 to test decoder
00001798  E766 7000 2EA1                             896+         VMLH  V22,V22,V23,2      test instruction (dest is a source)
0000179E  E760 5028 080E                 00001768    897+         VST   V22,V1O12          save v1 output
000017A4  07FB                                       898+         BR    R11               return
000017A8                                             899+RE12     DC    0F                xl16 expected result
000017A8                                             900+         DROP  R5
000017A8  FE030100 00000000                         901          DC    XL16'FE03010000000000 0009131E000D1B2B'   result
000017B0  0009131E 000D1B2B
000017B8  FF020304 05060750                          902          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000017C0  090A0B0C 0D0E0F7F
000017C8  FF000000 0000000A                          903          DC    XL16'FF0000000000000A 0101010F0101010F'   v3
000017D0  0101010F 0101010F
                                                     904
                                                     905 *-------------------------------------------------------------------
                                                     906 *  VML    - Vector Multiply Low
                                                     907 *-------------------------------------------------------------------
                                                     908 * Byte
                                                     909          VRR_C VML,0
000017D8                                             910+         DS    0FD
000017D8                      000017D8               911+         USING *,R5              base for test data and test routine
000017D8  00001818                                   912+T13      DC    A(X13)            address of test routine
000017DC  000D                                       913+         DC    H'13'             test number
000017DE  00                                         914+         DC    X'00'
000017DF  00                                         915+         DC    HL1'0'            m4
000017E0  E5D4D340 40404040                          916+         DC    CL8'VML'          instruction name
000017E8  00001850                                   917+         DC    A(RE13+16)        address of v2 source
000017EC  00001860                                   918+         DC    A(RE13+32)        address of v3 source
000017F0  00000010                                   919+         DC    A(16)             result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000017F4  00001840                                 920+REA13    DC    A(RE13)            result address
000017F8  00000000 00000000                        921+         DS    FD                 gap
00001800  00000000 00000000                        922+V1O13    DS    XL16               V1 output
00001808  00000000 00000000
00001810  00000000 00000000                        923+         DS    FD                 gap
                                                   924+*
00001818                                           925+X13      DS    0F
00001818  E310 5010 0014                 00000010  926+         LGF   R1,V2ADDR          load v2 source
0000181E  E761 0000 0806                 00000000  927+         VL    v22,0(R1)          use v22 to test decoder
00001824  E310 5014 0014                 00000014  928+         LGF   R1,V3ADDR          load v3 source
0000182A  E771 0000 0806                 00000000  929+         VL    v23,0(R1)          use v23 to test decoder
00001830  E766 7000 0EA2                           930+         VML   V22,V22,V23,0       test instruction (dest is a source)
00001836  E760 5028 080E                 00001800  931+         VST   V22,V1O13          save v1 output
0000183C  07FB                                     932+         BR    R11                return
00001840                                           933+RE13     DC    0F                 xl16 expected result
00001840                                           934+         DROP  R5
00001840  01000000 00000071                        935          DC    XL16'0100000000000071 0000004000000024'   result
00001848  00000040 00000024
00001850  FF000000 00000019                        936          DC    XL16'FF00000000000019 00000038000000FA'   v2
00001858  00000038 000000FA
00001860  FF000000 00000019                        937          DC    XL16'FF00000000000019 00000038000000FA'   v3
00001868  00000038 000000FA
                                                   938
                                                   939          VRR_C VML,0
00001870                                           940+         DS    0FD
00001870                      00001870             941+         USING *,R5               base for test data and test routine
00001870  000018B0                                 942+T14      DC    A(X14)             address of test routine
00001874  000E                                     943+         DC    H'14'              test number
00001876  00                                       944+         DC    X'00'
00001877  00                                       945+         DC    HL1'0'             m4
00001878  E5D4D340 40404040                       946+         DC    CL8'VML'           instruction name
00001880  000018E8                                 947+         DC    A(RE14+16)         address of v2 source
00001884  000018F8                                 948+         DC    A(RE14+32)         address of v3 source
00001888  00000010                                 949+         DC    A(16)              result length
0000188C  000018D8                                 950+REA14    DC    A(RE14)            result address
00001890  00000000 00000000                        951+         DS    FD                 gap
00001898  00000000 00000000                        952+V1O14    DS    XL16               V1 output
000018A0  00000000 00000000
000018A8  00000000 00000000                        953+         DS    FD                 gap
                                                   954+*
000018B0                                           955+X14      DS    0F
000018B0  E310 5010 0014                 00000010  956+         LGF   R1,V2ADDR          load v2 source
000018B6  E761 0000 0806                 00000000  957+         VL    v22,0(R1)          use v22 to test decoder
000018BC  E310 5014 0014                 00000014  958+         LGF   R1,V3ADDR          load v3 source
000018C2  E771 0000 0806                 00000000  959+         VL    v23,0(R1)          use v23 to test decoder
000018C8  E766 7000 0EA2                           960+         VML   V22,V22,V23,0       test instruction (dest is a source)
000018CE  E760 5028 080E                 00001898  961+         VST   V22,V1O14          save v1 output
000018D4  07FB                                     962+         BR    R11                return
000018D8                                           963+RE14     DC    0F                 xl16 expected result
000018D8                                           964+         DROP  R5
000018D8  01040910 19243140                        965          DC    XL16'0104091019243140 51647990A9C4E100'   result
000018E0  51647990 A9C4E100
000018E8  FF020304 05060708                        966          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
000018F0  090A0B0C 0D0E0F10
000018F8  FF020304 05060708                        967          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00001900  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    968
                                                    969          VRR_C VML,0
00001908                                            970+         DS    0FD
00001908                      00001908              971+         USING *,R5              base for test data and test routine
00001908  00001948                                  972+T15      DC    A(X15)            address of test routine
0000190C  000F                                      973+         DC    H'15'             test number
0000190E  00                                        974+         DC    X'00'
0000190F  00                                        975+         DC    HL1'0'            m4
00001910  E5D4D340 40404040                         976+         DC    CL8'VML'          instruction name
00001918  00001980                                  977+         DC    A(RE15+16)        address of v2 source
0000191C  00001990                                  978+         DC    A(RE15+32)        address of v3 source
00001920  00000010                                  979+         DC    A(16)             result length
00001924  00001970                                  980+REA15    DC    A(RE15)           result address
00001928  00000000 00000000                         981+         DS    FD                gap
00001930  00000000 00000000                         982+V1O15    DS    XL16              V1 output
00001938  00000000 00000000
00001940  00000000 00000000                         983+         DS    FD                gap
                                                    984+*
00001948                                            985+X15      DS    0F
00001948  E310 5010 0014                 00000010   986+         LGF   R1,V2ADDR         load v2 source
0000194E  E761 0000 0806                 00000000   987+         VL    v22,0(R1)         use v22 to test decoder
00001954  E310 5014 0014                 00000014   988+         LGF   R1,V3ADDR         load v3 source
0000195A  E771 0000 0806                 00000000   989+         VL    v23,0(R1)         use v23 to test decoder
00001960  E766 7000 0EA2                            990+         VML   V22,V22,V23,0      test instruction (dest is a source)
00001966  E760 5028 080E                 00001930   991+         VST   V22,V1O15         save v1 output
0000196C  07FB                                      992+         BR    R11               return
00001970                                            993+RE15     DC    0F                xl16 expected result
00001970                                            994+         DROP  R5
00001970  01020308 0A121520                         995          DC    XL16'010203080A121520 243237484E626980'   result
00001978  24323748 4E626980
00001980  FF020304 05060708                         996          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001988  090A0B0C 0D0E0F10
00001990  FF010102 02030304                         997          DC    XL16'FF01010202030304 0405050606070708'   v3
00001998  04050506 06070708
                                                    998
                                                    999          VRR_C VML,0
000019A0                                           1000+         DS    0FD
000019A0                      000019A0             1001+         USING *,R5              base for test data and test routine
000019A0  000019E0                                 1002+T16      DC    A(X16)            address of test routine
000019A4  0010                                     1003+         DC    H'16'             test number
000019A6  00                                       1004+         DC    X'00'
000019A7  00                                       1005+         DC    HL1'0'            m4
000019A8  E5D4D340 40404040                        1006+         DC    CL8'VML'          instruction name
000019B0  00001A18                                 1007+         DC    A(RE16+16)        address of v2 source
000019B4  00001A28                                 1008+         DC    A(RE16+32)        address of v3 source
000019B8  00000010                                 1009+         DC    A(16)             result length
000019BC  00001A08                                 1010+REA16    DC    A(RE16)           result address
000019C0  00000000 00000000                        1011+         DS    FD                gap
000019C8  00000000 00000000                        1012+V1O16    DS    XL16              V1 output
000019D0  00000000 00000000
000019D8  00000000 00000000                        1013+         DS    FD                gap
                                                   1014+*
000019E0                                           1015+X16      DS    0F
000019E0  E310 5010 0014                 00000010  1016+         LGF   R1,V2ADDR         load v2 source
000019E6  E761 0000 0806                 00000000  1017+         VL    v22,0(R1)         use v22 to test decoder
000019EC  E310 5014 0014                 00000014  1018+         LGF   R1,V3ADDR         load v3 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000019F2  E771 0000 0806                 00000000  1019+         VL    v23,0(R1)          use v23 to test decoder
000019F8  E766 7000 0EA2                           1020+         VML   V22,V22,V23,0       test instruction (dest is a source)
000019FE  E760 5028 080E                 000019C8  1021+         VST   V22,V1O16          save v1 output
00001A04  07FB                                     1022+         BR    R11                return
00001A08                                           1023+RE16     DC    0F                 xl16 expected result
00001A08                                           1024+         DROP  R5
00001A08  01000000 00000008                        1025          DC    XL16'0100000000000008 090A0B0C0D0E0F20'   result
00001A10  090A0B0C 0D0E0F20
00001A18  FF020304 05060708                        1026          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001A20  090A0B0C 0D0E0F10
00001A28  FF000000 00000001                        1027          DC    XL16'FF00000000000001 0101010101010102'   v3
00001A30  01010101 01010102
                                                   1028
                                                   1029 * Halfword
                                                   1030          VRR_C VML,1
00001A38                                           1031+         DS    0FD
00001A38                           00001A38        1032+         USING *,R5               base for test data and test routine
00001A38  00001A78                                 1033+T17      DC    A(X17)             address of test routine
00001A3C  0011                                     1034+         DC    H'17'              test number
00001A3E  00                                       1035+         DC    X'00'
00001A3F  01                                       1036+         DC    HL1'1'             m4
00001A40  E5D4D340 40404040                        1037+         DC    CL8'VML'           instruction name
00001A48  00001AB0                                 1038+         DC    A(RE17+16)         address of v2 source
00001A4C  00001AC0                                 1039+         DC    A(RE17+32)         address of v3 source
00001A50  00000010                                 1040+         DC    A(16)              result length
00001A54  00001AA0                                 1041+REA17    DC    A(RE17)            result address
00001A58  00000000 00000000                        1042+         DS    FD                 gap
00001A60  00000000 00000000                        1043+V1O17    DS    XL16               V1 output
00001A68  00000000 00000000
00001A70  00000000 00000000                        1044+         DS    FD                 gap
                                                   1045+*
00001A78                                           1046+X17      DS    0F
00001A78  E310 5010 0014                 00000010  1047+         LGF   R1,V2ADDR          load v2 source
00001A7E  E761 0000 0806                 00000000  1048+         VL    v22,0(R1)          use v22 to test decoder
00001A84  E310 5014 0014                 00000014  1049+         LGF   R1,V3ADDR          load v3 source
00001A8A  E771 0000 0806                 00000000  1050+         VL    v23,0(R1)          use v23 to test decoder
00001A90  E766 7000 1EA2                           1051+         VML   V22,V22,V23,1       test instruction (dest is a source)
00001A96  E760 5028 080E                 00001A60  1052+         VST   V22,V1O17          save v1 output
00001A9C  07FB                                     1053+         BR    R11                return
00001AA0                                           1054+RE17     DC    0F                 xl16 expected result
00001AA0                                           1055+         DROP  R5
00001AA0  00010000 00000271                        1056          DC    XL16'0001000000000271 00000C400000CC24'   result
00001AA8  00000C40 0000CC24
00001AB0  FFFF0000 00000019                        1057          DC    XL16'FFFF000000000019 000000380000EEFA'   v2
00001AB8  00000038 0000EEFA
00001AC0  FFFF0000 00000019                        1058          DC    XL16'FFFF000000000019 000000380000EEFA'   v3
00001AC8  00000038 0000EEFA
                                                   1059
                                                   1060          VRR_C VML,1
00001AD0                                           1061+         DS    0FD
00001AD0                           00001AD0        1062+         USING *,R5               base for test data and test routine
00001AD0  00001B10                                 1063+T18      DC    A(X18)             address of test routine
00001AD4  0012                                     1064+         DC    H'18'              test number
00001AD6  00                                       1065+         DC    X'00'
00001AD7  01                                       1066+         DC    HL1'1'             m4
00001AD8  E5D4D340 40404040                        1067+         DC    CL8'VML'           instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001AE0  00001B48                                1068+          DC    A(RE18+16)          address of v2 source
00001AE4  00001B58                                1069+          DC    A(RE18+32)          address of v3 source
00001AE8  00000010                                1070+          DC    A(16)               result length
00001AEC  00001B38                                1071+REA18     DC    A(RE18)             result address
00001AF0  00000000 00000000                       1072+          DS    FD                  gap
00001AF8  00000000 00000000                       1073+V1O18     DS    XL16                V1 output
00001B00  00000000 00000000
00001B08  00000000 00000000                       1074+          DS    FD                  gap
                                                  1075+*
00001B10                                          1076+X18       DS    0F
00001B10  E310 5010 0014                 00000010 1077+          LGF   R1,V2ADDR           load v2 source
00001B16  E761 0000 0806                 00000000 1078+          VL    v22,0(R1)           use v22 to test decoder
00001B1C  E310 5014 0014                 00000014 1079+          LGF   R1,V3ADDR           load v3 source
00001B22  E771 0000 0806                 00000000 1080+          VL    v23,0(R1)           use v23 to test decoder
00001B28  E766 7000 1EA2                          1081+          VML   V22,V22,V23,1        test instruction (dest is a source)
00001B2E  E760 5028 080E                 00001AF8 1082+          VST   V22,V1O18           save v1 output
00001B34  07FB                                    1083+          BR    R11                 return
00001B38                                          1084+RE18      DC    0F                  xl16 expected result
00001B38                                          1085+          DROP  R5
00001B38  FC041810 3C247040                       1086           DC    XL16'FC0418103C247040 B46408906CC4E100'   result
00001B40  B4640890 6CC4E100
00001B48  FF020304 05060708                       1087           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001B50  090A0B0C 0D0E0F10
00001B58  FF020304 05060708                       1088           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00001B60  090A0B0C 0D0E0F10
                                                  1089
                                                  1090           VRR_C VML,1
00001B68                                          1091+          DS    0FD
00001B68                         00001B68         1092+          USING *,R5                base for test data and test routine
00001B68  00001BA8                                1093+T19       DC    A(X19)              address of test routine
00001B6C  0013                                    1094+          DC    H'19'               test number
00001B6E  00                                      1095+          DC    X'00'
00001B6F  01                                      1096+          DC    HL1'1'              m4
00001B70  E5D4D340 40404040                       1097+          DC    CL8'VML'            instruction name
00001B78  00001BE0                                1098+          DC    A(RE19+16)          address of v2 source
00001B7C  00001BF0                                1099+          DC    A(RE19+32)          address of v3 source
00001B80  00000010                                1100+          DC    A(16)               result length
00001B84  00001BD0                                1101+REA19     DC    A(RE19)             result address
00001B88  00000000 00000000                       1102+          DS    FD                  gap
00001B90  00000000 00000000                       1103+V1O19     DS    XL16                V1 output
00001B98  00000000 00000000
00001BA0  00000000 00000000                       1104+          DS    FD                  gap
                                                  1105+*
00001BA8                                          1106+X19       DS    0F
00001BA8  E310 5010 0014                 00000010 1107+          LGF   R1,V2ADDR           load v2 source
00001BAE  E761 0000 0806                 00000000 1108+          VL    v22,0(R1)           use v22 to test decoder
00001BB4  E310 5014 0014                 00000014 1109+          LGF   R1,V3ADDR           load v3 source
00001BBA  E771 0000 0806                 00000000 1110+          VL    v23,0(R1)           use v23 to test decoder
00001BC0  E766 7000 1EA2                          1111+          VML   V22,V22,V23,1        test instruction (dest is a source)
00001BC6  E760 5028 080E                 00001B90 1112+          VST   V22,V1O19           save v1 output
00001BCC  07FB                                    1113+          BR    R11                 return
00001BD0                                          1114+RE19      DC    0F                  xl16 expected result
00001BD0                                          1115+          DROP  R5
00001BD0  FD020A08 1B123420                       1116           DC    XL16'FD020A081B123420 55327E48AF62E880'   result
00001BD8  55327E48 AF62E880
00001BE0  FF020304 05060708                       1117           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001BE8  090A0B0C 0D0E0F10
00001BF0  FF010102 02030304                        1118          DC    XL16'FF01010202030304 0405050606070708'   v3
00001BF8  04050506 06070708
                                                   1119
                                                   1120          VRR_C VML,1
00001C00                                           1121+         DS    0FD
00001C00                     00001C00              1122+         USING *,R5              base for test data and test routine
00001C00  00001C40                                 1123+T20      DC    A(X20)            address of test routine
00001C04  0014                                     1124+         DC    H'20'             test number
00001C06  00                                       1125+         DC    X'00'
00001C07  01                                       1126+         DC    HL1'1'            m4
00001C08  E5D4D340 40404040                        1127+         DC    CL8'VML'          instruction name
00001C10  00001C78                                 1128+         DC    A(RE20+16)        address of v2 source
00001C14  00001C88                                 1129+         DC    A(RE20+32)        address of v3 source
00001C18  00000010                                 1130+         DC    A(16)             result length
00001C1C  00001C68                                 1131+REA20    DC    A(RE20)           result address
00001C20  00000000 00000000                        1132+         DS    FD                gap
00001C28  00000000 00000000                        1133+V1O20    DS    XL16              V1 output
00001C30  00000000 00000000
00001C38  00000000 00000000                        1134+         DS    FD                gap
                                                   1135+*
00001C40                                           1136+X20      DS    0F
00001C40  E310 5010 0014                 00000010  1137+         LGF   R1,V2ADDR         load v2 source
00001C46  E761 0000 0806                 00000000  1138+         VL    v22,0(R1)         use v22 to test decoder
00001C4C  E310 5014 0014                 00000014  1139+         LGF   R1,V3ADDR         load v3 source
00001C52  E771 0000 0806                 00000000  1140+         VL    v23,0(R1)         use v23 to test decoder
00001C58  E766 7000 1EA2                           1141+         VML   V22,V22,V23,1      test instruction (dest is a source)
00001C5E  E760 5028 080E                 00001C28  1142+         VST   V22,V1O20         save v1 output
00001C64  07FB                                     1143+         BR    R11               return
00001C68                                           1144+RE20     DC    0F                xl16 expected result
00001C68                                           1145+         DROP  R5
00001C68  FE000000 00000708                        1146          DC    XL16'FE00000000000708 130A170C1B0E2E20'   result
00001C70  130A170C 1B0E2E20
00001C78  FF020304 05060708                        1147          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001C80  090A0B0C 0D0E0F10
00001C88  FF000000 00000001                        1148          DC    XL16'FF00000000000001 0101010101010102'   v3
00001C90  01010101 01010102
                                                   1149
                                                   1150 * Word
                                                   1151          VRR_C VML,2
00001C98                                           1152+         DS    0FD
00001C98                     00001C98              1153+         USING *,R5              base for test data and test routine
00001C98  00001CD8                                 1154+T21      DC    A(X21)            address of test routine
00001C9C  0015                                     1155+         DC    H'21'             test number
00001C9E  00                                       1156+         DC    X'00'
00001C9F  02                                       1157+         DC    HL1'2'            m4
00001CA0  E5D4D340 40404040                        1158+         DC    CL8'VML'          instruction name
00001CA8  00001D10                                 1159+         DC    A(RE21+16)        address of v2 source
00001CAC  00001D20                                 1160+         DC    A(RE21+32)        address of v3 source
00001CB0  00000010                                 1161+         DC    A(16)             result length
00001CB4  00001D00                                 1162+REA21    DC    A(RE21)           result address
00001CB8  00000000 00000000                        1163+         DS    FD                gap
00001CC0  00000000 00000000                        1164+V1O21    DS    XL16              V1 output
00001CC8  00000000 00000000
00001CD0  00000000 00000000                        1165+         DS    FD                gap
                                                   1166+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001CD8                                           1167+X21      DS    0F
00001CD8  E310 5010 0014                 00000010  1168+         LGF   R1,V2ADDR         load v2 source
00001CDE  E761 0000 0806                 00000000  1169+         VL    v22,0(R1)         use v22 to test decoder
00001CE4  E310 5014 0014                 00000014  1170+         LGF   R1,V3ADDR         load v3 source
00001CEA  E771 0000 0806                 00000000  1171+         VL    v23,0(R1)         use v23 to test decoder
00001CF0  E766 7000 2EA2                           1172+         VML   V22,V22,V23,2      test instruction (dest is a source)
00001CF6  E760 5028 080E                 00001CC0  1173+         VST   V22,V1O21          save v1 output
00001CFC  07FB                                     1174+         BR    R11               return
00001D00                                           1175+RE21     DC    0F                xl16 expected result
00001D00                                           1176+         DROP  R5
00001D00  00000001 71000000                        1177          DC    XL16'000000171000000 00000C400FEDCC24'   result
00001D08  00000C40 0FEDCC24
00001D10  FFFFFFFF 00019000                        1178          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00001D18  00000038 EEEEEEFA
00001D20  FFFFFFFF 00019000                        1179          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v3
00001D28  00000038 EEEEEEFA
                                                   1180
                                                   1181          VRR_C VML,2
00001D30                                           1182+         DS    0FD
00001D30                         00001D30          1183+         USING *,R5              base for test data and test routine
00001D30  00001D70                                 1184+T22      DC    A(X22)            address of test routine
00001D34  0016                                     1185+         DC    H'22'             test number
00001D36  00                                       1186+         DC    X'00'
00001D37  02                                       1187+         DC    HL1'2'            m4
00001D38  E5D4D340 40404040                        1188+         DC    CL8'VML'          instruction name
00001D40  00001DA8                                 1189+         DC    A(RE22+16)        address of v2 source
00001D44  00001DB8                                 1190+         DC    A(RE22+32)        address of v3 source
00001D48  00000010                                 1191+         DC    A(16)             result length
00001D4C  00001D98                                 1192+REA22    DC    A(RE22)           result address
00001D50  00000000 00000000                        1193+         DS    FD                gap
00001D58  00000000 00000000                        1194+V1O22    DS    XL16              V1 output
00001D60  00000000 00000000
00001D68  00000000 00000000                        1195+         DS    FD                gap
                                                   1196+*
00001D70                                           1197+X22      DS    0F
00001D70  E310 5010 0014                 00000010  1198+         LGF   R1,V2ADDR         load v2 source
00001D76  E761 0000 0806                 00000000  1199+         VL    v22,0(R1)         use v22 to test decoder
00001D7C  E310 5014 0014                 00000014  1200+         LGF   R1,V3ADDR         load v3 source
00001D82  E771 0000 0806                 00000000  1201+         VL    v23,0(R1)         use v23 to test decoder
00001D88  E766 7000 2EA2                           1202+         VML   V22,V22,V23,2      test instruction (dest is a source)
00001D8E  E760 5028 080E                 00001D58  1203+         VST   V22,V1O22          save v1 output
00001D94  07FB                                     1204+         BR    R11               return
00001D98                                           1205+RE22     DC    0F                xl16 expected result
00001D98                                           1206+         DROP  R5
00001D98  04191810 A4917040                        1207          DC    XL16'04191810A4917040 B56A089046A2E100'   result
00001DA0  B56A0890 46A2E100
00001DA8  FF020304 05060708                        1208          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001DB0  090A0B0C 0D0E0F10
00001DB8  FF020304 05060708                        1209          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00001DC0  090A0B0C 0D0E0F10
                                                   1210
                                                   1211          VRR_C VML,2
00001DC8                                           1212+         DS    0FD
00001DC8                         00001DC8          1213+         USING *,R5              base for test data and test routine
00001DC8  00001E08                                 1214+T23      DC    A(X23)            address of test routine
00001DCC  0017                                     1215+         DC    H'23'             test number
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001DCE  00                                       1216+          DC    X'00'
00001DCF  02                                       1217+          DC    HL1'2'             m4
00001DD0  E5D4D340 40404040                        1218+          DC    CL8'VML'           instruction name
00001DD8  00001E40                                 1219+          DC    A(RE23+16)         address of v2 source
00001DDC  00001E50                                 1220+          DC    A(RE23+32)         address of v3 source
00001DE0  00000010                                 1221+          DC    A(16)              result length
00001DE4  00001E30                                 1222+REA23     DC    A(RE23)            result address
00001DE8  00000000 00000000                        1223+          DS    FD                 gap
00001DF0  00000000 00000000                        1224+V1O23     DS    XL16               V1 output
00001DF8  00000000 00000000
00001E00  00000000 00000000                        1225+          DS    FD                 gap
                                                   1226+*
00001E08                                           1227+X23       DS    0F
00001E08  E310 5010 0014                 00000010  1228+          LGF   R1,V2ADDR          load v2 source
00001E0E  E761 0000 0806                 00000000  1229+          VL    v22,0(R1)          use v22 to test decoder
00001E14  E310 5014 0014                 00000014  1230+          LGF   R1,V3ADDR          load v3 source
00001E1A  E771 0000 0806                 00000000  1231+          VL    v23,0(R1)          use v23 to test decoder
00001E20  E766 7000 2EA2                           1232+          VML   V22,V22,V23,2       test instruction (dest is a source)
00001E26  E760 5028 080E                 00001DF0  1233+          VST   V22,V1O23          save v1 output
00001E2C  07FB                                     1234+          BR    R11                return
00001E30                                           1235+RE23      DC    0F                 xl16 expected result
00001E30                                           1236+          DROP  R5
00001E30  FF0B0A08 4B453420                        1237           DC    XL16'FF0B0A084B453420 CFAF7E489449E880'   result
00001E38  CFAF7E48 9449E880
00001E40  FF020304 05060708                        1238           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001E48  090A0B0C 0D0E0F10
00001E50  FF010102 02030304                        1239           DC    XL16'FF01010202030304 0405050606070708'   v3
00001E58  04050506 06070708
                                                   1240
                                                   1241           VRR_C VML,2
00001E60                                           1242+          DS    0FD
00001E60                         00001E60          1243+          USING *,R5               base for test data and test routine
00001E60  00001EA0                                 1244+T24       DC    A(X24)             address of test routine
00001E64  0018                                     1245+          DC    H'24'              test number
00001E66  00                                       1246+          DC    X'00'
00001E67  02                                       1247+          DC    HL1'2'             m4
00001E68  E5D4D340 40404040                        1248+          DC    CL8'VML'           instruction name
00001E70  00001ED8                                 1249+          DC    A(RE24+16)         address of v2 source
00001E74  00001EE8                                 1250+          DC    A(RE24+32)         address of v3 source
00001E78  00000010                                 1251+          DC    A(16)              result length
00001E7C  00001EC8                                 1252+REA24     DC    A(RE24)            result address
00001E80  00000000 00000000                        1253+          DS    FD                 gap
00001E88  00000000 00000000                        1254+V1O24     DS    XL16               V1 output
00001E90  00000000 00000000
00001E98  00000000 00000000                        1255+          DS    FD                 gap
                                                   1256+*
00001EA0                                           1257+X24       DS    0F
00001EA0  E310 5010 0014                 00000010  1258+          LGF   R1,V2ADDR          load v2 source
00001EA6  E761 0000 0806                 00000000  1259+          VL    v22,0(R1)          use v22 to test decoder
00001EAC  E310 5014 0014                 00000014  1260+          LGF   R1,V3ADDR          load v3 source
00001EB2  E771 0000 0806                 00000000  1261+          VL    v23,0(R1)          use v23 to test decoder
00001EB8  E766 7000 2EA2                           1262+          VML   V22,V22,V23,2       test instruction (dest is a source)
00001EBE  E760 5028 080E                 00001E88  1263+          VST   V22,V1O24          save v1 output
00001EC4  07FB                                     1264+          BR    R11                return
00001EC8                                           1265+RE24      DC    0F                 xl16 expected result
00001EC8                                           1266+          DROP  R5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001EC8  FC000000 05060708                        1267          DC    XL16'FC00000005060708 2A21170C473B2E20'   result
00001ED0  2A21170C 473B2E20
00001ED8  FF020304 05060708                        1268          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001EE0  090A0B0C 0D0E0F10
00001EE8  FF000000 00000001                        1269          DC    XL16'FF00000000000001 0101010101010102'   v3
00001EF0  01010101 01010102
                                                   1270
                                                   1271 *-------------------------------------------------------------------
                                                   1272 *  VMH    - Vector Multiply High
                                                   1273 *-------------------------------------------------------------------
                                                   1274 * Byte
                                                   1275          VRR_C VMH,0
00001EF8                                           1276+         DS    0FD
00001EF8                          00001EF8         1277+         USING *,R5              base for test data and test routine
00001EF8  00001F38                                 1278+T25      DC    A(X25)            address of test routine
00001EFC  0019                                     1279+         DC    H'25'             test number
00001EFE  00                                       1280+         DC    X'00'
00001EFF  00                                       1281+         DC    HL1'0'            m4
00001F00  E5D4C840 40404040                        1282+         DC    CL8'VMH'          instruction name
00001F08  00001F70                                 1283+         DC    A(RE25+16)        address of v2 source
00001F0C  00001F80                                 1284+         DC    A(RE25+32)        address of v3 source
00001F10  00000010                                 1285+         DC    A(16)             result length
00001F14  00001F60                                 1286+REA25    DC    A(RE25)           result address
00001F18  00000000 00000000                        1287+         DS    FD                gap
00001F20  00000000 00000000                        1288+V1O25    DS    XL16              V1 output
00001F28  00000000 00000000
00001F30  00000000 00000000                        1289+         DS    FD                gap
                                                   1290+*
00001F38                                           1291+X25      DS    0F
00001F38  E310 5010 0014                  00000010 1292+         LGF   R1,V2ADDR         load v2 source
00001F3E  E761 0000 0806                  00000000 1293+         VL    v22,0(R1)         use v22 to test decoder
00001F44  E310 5014 0014                  00000014 1294+         LGF   R1,V3ADDR         load v3 source
00001F4A  E771 0000 0806                  00000000 1295+         VL    v23,0(R1)         use v23 to test decoder
00001F50  E766 7000 0EA3                           1296+         VMH   V22,V22,V23,0      test instruction (dest is a source)
00001F56  E760 5028 080E                  00001F20 1297+         VST   V22,V1O25          save v1 output
00001F5C  07FB                                     1298+         BR    R11               return
00001F60                                           1299+RE25     DC    0F                xl16 expected result
00001F60                                           1300+         DROP  R5
00001F60  00000000 00000002                        1301          DC    XL16'0000000000000002 0000000C00000000'   result
00001F68  0000000C 00000000
00001F70  FF000000 00000019                        1302          DC    XL16'FF00000000000019 00000038000000FA'   v2
00001F78  00000038 000000FA
00001F80  FF000000 00000019                        1303          DC    XL16'FF00000000000019 00000038000000FA'   v3
00001F88  00000038 000000FA
                                                   1304
                                                   1305          VRR_C VMH,0
00001F90                                           1306+         DS    0FD
00001F90                          00001F90         1307+         USING *,R5              base for test data and test routine
00001F90  00001FD0                                 1308+T26      DC    A(X26)            address of test routine
00001F94  001A                                     1309+         DC    H'26'             test number
00001F96  00                                       1310+         DC    X'00'
00001F97  00                                       1311+         DC    HL1'0'            m4
00001F98  E5D4C840 40404040                        1312+         DC    CL8'VMH'          instruction name
00001FA0  00002008                                 1313+         DC    A(RE26+16)        address of v2 source
00001FA4  00002018                                 1314+         DC    A(RE26+32)        address of v3 source
00001FA8  00000010                                 1315+         DC    A(16)             result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001FAC  00001FF8                        1316+REA26    DC    A(RE26)            result address
00001FB0  00000000 00000000               1317+         DS    FD                 gap
00001FB8  00000000 00000000               1318+V1O26    DS    XL16               V1 output
00001FC0  00000000 00000000
00001FC8  00000000 00000000               1319+         DS    FD                 gap
                                          1320+*
00001FD0                                  1321+X26      DS    0F
00001FD0  E310 5010 0014          00000010 1322+         LGF   R1,V2ADDR          load v2 source
00001FD6  E761 0000 0806          00000000 1323+         VL    v22,0(R1)          use v22 to test decoder
00001FDC  E310 5014 0014          00000014 1324+         LGF   R1,V3ADDR          load v3 source
00001FE2  E771 0000 0806          00000000 1325+         VL    v23,0(R1)          use v23 to test decoder
00001FE8  E766 7000 0EA3                   1326+         VMH   V22,V22,V23,0       test instruction (dest is a source)
00001FEE  E760 5028 080E          00001FB8 1327+         VST   V22,V1O26          save v1 output
00001FF4  07FB                             1328+         BR    R11                return
00001FF8                                  1329+RE26     DC    0F                 xl16 expected result
00001FF8                                  1330+         DROP  R5
00001FF8  FF000000 00000019               1331          DC    XL16'FF00000000000019 000000050000003F'   result
00002000  00000005 0000003F
00002008  FF020304 05060750               1332          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002010  090A0B0C 0D0E0F7F
00002018  01020304 05060750               1333          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00002020  090A0B78 0D0E0F7F
                                          1334
                                          1335          VRR_C VMH,0
00002028                                  1336+         DS    0FD
00002028                  00002028        1337+         USING *,R5               base for test data and test routine
00002028  00002068                        1338+T27      DC    A(X27)             address of test routine
0000202C  001B                            1339+         DC    H'27'              test number
0000202E  00                              1340+         DC    X'00'
0000202F  00                              1341+         DC    HL1'0'             m4
00002030  E5D4C840 40404040               1342+         DC    CL8'VMH'           instruction name
00002038  000020A0                        1343+         DC    A(RE27+16)         address of v2 source
0000203C  000020B0                        1344+         DC    A(RE27+32)         address of v3 source
00002040  00000010                        1345+         DC    A(16)              result length
00002044  00002090                        1346+REA27    DC    A(RE27)            result address
00002048  00000000 00000000               1347+         DS    FD                 gap
00002050  00000000 00000000               1348+V1O27    DS    XL16               V1 output
00002058  00000000 00000000
00002060  00000000 00000000               1349+         DS    FD                 gap
                                          1350+*
00002068                                  1351+X27      DS    0F
00002068  E310 5010 0014          00000010 1352+         LGF   R1,V2ADDR          load v2 source
0000206E  E761 0000 0806          00000000 1353+         VL    v22,0(R1)          use v22 to test decoder
00002074  E310 5014 0014          00000014 1354+         LGF   R1,V3ADDR          load v3 source
0000207A  E771 0000 0806          00000000 1355+         VL    v23,0(R1)          use v23 to test decoder
00002080  E766 7000 0EA3                   1356+         VMH   V22,V22,V23,0       test instruction (dest is a source)
00002086  E760 5028 080E          00002050 1357+         VST   V22,V1O27          save v1 output
0000208C  07FB                             1358+         BR    R11                return
00002090                                  1359+RE27     DC    0F                 xl16 expected result
00002090                                  1360+         DROP  R5
00002090  00000000 0000000C               1361          DC    XL16'000000000000000C 000000020000001F'   result
00002098  00000002 0000001F
000020A0  FF020304 05060750               1362          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000020A8  090A0B0C 0D0E0F7F
000020B0  00010102 02030328               1363          DC    XL16'0001010202030328 0405053C0607073F'   v3
000020B8  0405053C 0607073F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   1364
                                                   1365          VRR_C VMH,0
000020C0                                           1366+         DS    0FD
000020C0                     000020C0              1367+         USING *,R5              base for test data and test routine
000020C0  00002100                                 1368+T28      DC    A(X28)            address of test routine
000020C4  001C                                     1369+         DC    H'28'             test number
000020C6  00                                       1370+         DC    X'00'
000020C7  00                                       1371+         DC    HL1'0'            m4
000020C8  E5D4C840 40404040                        1372+         DC    CL8'VMH'          instruction name
000020D0  00002138                                 1373+         DC    A(RE28+16)        address of v2 source
000020D4  00002148                                 1374+         DC    A(RE28+32)        address of v3 source
000020D8  00000010                                 1375+         DC    A(16)             result length
000020DC  00002128                                 1376+REA28    DC    A(RE28)           result address
000020E0  00000000 00000000                        1377+         DS    FD                gap
000020E8  00000000 00000000                        1378+V1O28    DS    XL16              V1 output
000020F0  00000000 00000000
000020F8  00000000 00000000                        1379+         DS    FD                gap
                                                   1380+*
00002100                                           1381+X28      DS    0F
00002100  E310 5010 0014                 00000010  1382+         LGF   R1,V2ADDR         load v2 source
00002106  E761 0000 0806                 00000000  1383+         VL    v22,0(R1)         use v22 to test decoder
0000210C  E310 5014 0014                 00000014  1384+         LGF   R1,V3ADDR         load v3 source
00002112  E771 0000 0806                 00000000  1385+         VL    v23,0(R1)         use v23 to test decoder
00002118  E766 7000 0EA3                           1386+         VMH   V22,V22,V23,0      test instruction (dest is a source)
0000211E  E760 5028 080E                 000020E8  1387+         VST   V22,V1O28         save v1 output
00002124  07FB                                     1388+         BR    R11               return
00002128                                           1389+RE28     DC    0F                xl16 expected result
00002128                                           1390+         DROP  R5
00002128  00000000 00000003                        1391          DC    XL16'0000000000000003 0000000000000007'   result
00002130  00000000 00000007
00002138  FF020304 05060750                        1392          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002140  090A0B0C 0D0E0F7F
00002148  00000000 0000000A                        1393          DC    XL16'000000000000000A 0101010F0101010F'   v3
00002150  0101010F 0101010F
                                                   1394
                                                   1395 * Halfword
                                                   1396          VRR_C VMH,1
00002158                                           1397+         DS    0FD
00002158                     00002158              1398+         USING *,R5              base for test data and test routine
00002158  00002198                                 1399+T29      DC    A(X29)            address of test routine
0000215C  001D                                     1400+         DC    H'29'             test number
0000215E  00                                       1401+         DC    X'00'
0000215F  01                                       1402+         DC    HL1'1'            m4
00002160  E5D4C840 40404040                        1403+         DC    CL8'VMH'          instruction name
00002168  000021D0                                 1404+         DC    A(RE29+16)        address of v2 source
0000216C  000021E0                                 1405+         DC    A(RE29+32)        address of v3 source
00002170  00000010                                 1406+         DC    A(16)             result length
00002174  000021C0                                 1407+REA29    DC    A(RE29)           result address
00002178  00000000 00000000                        1408+         DS    FD                gap
00002180  00000000 00000000                        1409+V1O29    DS    XL16              V1 output
00002188  00000000 00000000
00002190  00000000 00000000                        1410+         DS    FD                gap
                                                   1411+*
00002198                                           1412+X29      DS    0F
00002198  E310 5010 0014                 00000010  1413+         LGF   R1,V2ADDR         load v2 source
0000219E  E761 0000 0806                 00000000  1414+         VL    v22,0(R1)         use v22 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000021A4  E310 5014 0014                 00000014  1415+         LGF    R1,V3ADDR          load v3 source
000021AA  E771 0000 0806                 00000000  1416+         VL     v23,0(R1)          use v23 to test decoder
000021B0  E766 7000 1EA3                           1417+         VMH    V22,V22,V23,1       test instruction (dest is a source)
000021B6  E760 5028 080E                 00002180  1418+         VST    V22,V1O29           save v1 output
000021BC  07FB                                     1419+         BR     R11                return
000021C0                                           1420+RE29     DC     0F                 xl16 expected result
000021C0                                           1421+         DROP   R5
000021C0  00000000 00000000                       1422          DC     XL16'0000000000000000 0000000000000121'   result
000021C8  00000000 00000121
000021D0  FFFF0000 00000019                       1423          DC     XL16'FFFF000000000019 000000380000EEFA'   v2
000021D8  00000038 0000EEFA
000021E0  FFFF0000 00000019                       1424          DC     XL16'FFFF000000000019 000000380000EEFA'   v3
000021E8  00000038 0000EEFA
                                                  1425
                                                  1426          VRR_C  VMH,1
000021F0                                          1427+         DS     0FD
000021F0                         000021F0         1428+         USING  *,R5               base for test data and test routine
000021F0  00002230                                1429+T30      DC     A(X30)             address of test routine
000021F4  001E                                    1430+         DC     H'30'              test number
000021F6  00                                      1431+         DC     X'00'
000021F7  01                                      1432+         DC     HL1'1'             m4
000021F8  E5D4C840 40404040                       1433+         DC     CL8'VMH'           instruction name
00002200  00002268                                1434+         DC     A(RE30+16)         address of v2 source
00002204  00002278                                1435+         DC     A(RE30+32)         address of v3 source
00002208  00000010                                1436+         DC     A(16)              result length
0000220C  00002258                                1437+REA30    DC     A(RE30)            result address
00002210  00000000 00000000                       1438+         DS     FD                 gap
00002218  00000000 00000000                       1439+V1O30    DS     XL16               V1 output
00002220  00000000 00000000
00002228  00000000 00000000                       1440+         DS     FD                 gap
                                                  1441+*
00002230                                          1442+X30      DS     0F
00002230  E310 5010 0014                 00000010 1443+         LGF    R1,V2ADDR          load v2 source
00002236  E761 0000 0806                 00000000 1444+         VL     v22,0(R1)          use v22 to test decoder
0000223C  E310 5014 0014                 00000014 1445+         LGF    R1,V3ADDR          load v3 source
00002242  E771 0000 0806                 00000000 1446+         VL     v23,0(R1)          use v23 to test decoder
00002248  E766 7000 1EA3                           1447+         VMH    V22,V22,V23,1       test instruction (dest is a source)
0000224E  E760 A018 080E                 00002218  1448+         VST    V22,V1O30           save v1 output
00002254  07FB                                     1449+         BR     R11                return
00002258                                           1450+RE30     DC     0F                 xl16 expected result
00002258                                           1451+         DROP   R5
00002258  FFFF0009 00190035                       1452          DC     XL16'FFFF000900190035 0051007E00AA00F0'   result
00002260  0051007E 00AA00F0
00002268  FF020304 05060750                       1453          DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002270  090A0B0C 0D0E0F7F
00002278  01020304 05060750                       1454          DC     XL16'0102030405060750 090A0B780D0E0F7F'   v3
00002280  090A0B78 0D0E0F7F
                                                  1455
                                                  1456          VRR_C  VMH,1
00002288                                          1457+         DS     0FD
00002288                         00002288         1458+         USING  *,R5               base for test data and test routine
00002288  000022C8                                1459+T31      DC     A(X31)             address of test routine
0000228C  001F                                    1460+         DC     H'31'              test number
0000228E  00                                      1461+         DC     X'00'
0000228F  01                                      1462+         DC     HL1'1'             m4
00002290  E5D4C840 40404040                       1463+         DC     CL8'VMH'           instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002298  00002300                          1464+          DC    A(RE31+16)          address of v2 source
0000229C  00002310                          1465+          DC    A(RE31+32)          address of v3 source
000022A0  00000010                          1466+          DC    A(16)               result length
000022A4  000022F0                          1467+REA31     DC    A(RE31)             result address
000022A8  00000000 00000000                 1468+          DS    FD                  gap
000022B0  00000000 00000000                 1469+V1O31     DS    XL16                V1 output
000022B8  00000000 00000000
000022C0  00000000 00000000                 1470+          DS    FD                  gap
                                            1471+*
000022C8                                    1472+X31       DS    0F
000022C8  E310 5010 0014          00000010  1473+          LGF   R1,V2ADDR           load v2 source
000022CE  E761 0000 0806          00000000  1474+          VL    v22,0(R1)           use v22 to test decoder
000022D4  E310 5014 0014          00000014  1475+          LGF   R1,V3ADDR           load v3 source
000022DA  E771 0000 0806          00000000  1476+          VL    v23,0(R1)           use v23 to test decoder
000022E0  E766 7000 1EA3                    1477+          VMH   V22,V22,V23,1        test instruction (dest is a source)
000022E6  E760 5028 080E          000022B0  1478+          VST   V22,V1O31           save v1 output
000022EC  07FB                              1479+          BR    R11                 return
000022F0                                    1480+RE31      DC    0F                  xl16 expected result
000022F0                                    1481+          DROP  R5
000022F0  FFFF0003 000A0017                 1482           DC    XL16'FFFF0003000A0017 00240039004E0070'   result
000022F8  00240039 004E0070
00002300  FF020304 05060750                 1483           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002308  090A0B0C 0D0E0F7F
00002310  00010102 02030328                 1484           DC    XL16'0001010202030328 0405053C0607073F'   v3
00002318  0405053C 0607073F
                                            1485
                                            1486           VRR_C VMH,1
00002320                                    1487+          DS    0FD
00002320                        00002320    1488+          USING *,R5                base for test data and test routine
00002320  00002360                          1489+T32       DC    A(X32)              address of test routine
00002324  0020                              1490+          DC    H'32'               test number
00002326  00                                1491+          DC    X'00'
00002327  01                                1492+          DC    HL1'1'              m4
00002328  E5D4C840 40404040                 1493+          DC    CL8'VMH'            instruction name
00002330  00002398                          1494+          DC    A(RE32+16)          address of v2 source
00002334  000023A8                          1495+          DC    A(RE32+32)          address of v3 source
00002338  00000010                          1496+          DC    A(16)               result length
0000233C  00002388                          1497+REA32     DC    A(RE32)             result address
00002340  00000000 00000000                 1498+          DS    FD                  gap
00002348  00000000 00000000                 1499+V1O32     DS    XL16                V1 output
00002350  00000000 00000000
00002358  00000000 00000000                 1500+          DS    FD                  gap
                                            1501+*
00002360                                    1502+X32       DS    0F
00002360  E310 5010 0014          00000010  1503+          LGF   R1,V2ADDR           load v2 source
00002366  E761 0000 0806          00000000  1504+          VL    v22,0(R1)           use v22 to test decoder
0000236C  E310 5014 0014          00000014  1505+          LGF   R1,V3ADDR           load v3 source
00002372  E771 0000 0806          00000000  1506+          VL    v23,0(R1)           use v23 to test decoder
00002378  E766 7000 1EA3                    1507+          VMH   V22,V22,V23,1        test instruction (dest is a source)
0000237E  E760 5028 080E          00002348  1508+          VST   V22,V1O32           save v1 output
00002384  07FB                              1509+          BR    R11                 return
00002388                                    1510+RE32      DC    0F                  xl16 expected result
00002388                                    1511+          DROP  R5
00002388  00000000 00000000                 1512           DC    XL16'0000000000000000 0009000B000D0010'   result
00002390  0009000B 000D0010
00002398  FF020304 05060750                 1513           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000023A0  090A0B0C 0D0E0F7F
000023A8  00000000 0000000A                        1514           DC    XL16'000000000000000A 0101010F0101010F'   v3
000023B0  0101010F 0101010F
                                                   1515
                                                   1516 * Word
                                                   1517           VRR_C VMH,2
000023B8                                           1518+          DS    0FD
000023B8                     000023B8              1519+          USING *,R5              base for test data and test routine
000023B8  000023F8                                 1520+T33       DC    A(X33)            address of test routine
000023BC  0021                                     1521+          DC    H'33'             test number
000023BE  00                                       1522+          DC    X'00'
000023BF  02                                       1523+          DC    HL1'2'            m4
000023C0  E5D4C840 40404040                        1524+          DC    CL8'VMH'          instruction name
000023C8  00002430                                 1525+          DC    A(RE33+16)        address of v2 source
000023CC  00002440                                 1526+          DC    A(RE33+32)        address of v3 source
000023D0  00000010                                 1527+          DC    A(16)             result length
000023D4  00002420                                 1528+REA33     DC    A(RE33)           result address
000023D8  00000000 00000000                        1529+          DS    FD                gap
000023E0  00000000 00000000                        1530+V1O33     DS    XL16              V1 output
000023E8  00000000 00000000
000023F0  00000000 00000000                        1531+          DS    FD                gap
                                                   1532+*
000023F8                                           1533+X33       DS    0F
000023F8  E310 5010 0014                 00000010  1534+          LGF   R1,V2ADDR         load v2 source
000023FE  E761 0000 0806                 00000000  1535+          VL    v22,0(R1)         use v22 to test decoder
00002404  E310 5014 0014                 00000014  1536+          LGF   R1,V3ADDR         load v3 source
0000240A  E771 0000 0806                 00000000  1537+          VL    v23,0(R1)         use v23 to test decoder
00002410  E766 7000 2EA3                           1538+          VMH   V22,V22,V23,2      test instruction (dest is a source)
00002416  E760 5028 080E                 000023E0  1539+          VST   V22,V1O33         save v1 output
0000241C  07FB                                     1540+          BR    R11               return
00002420                                           1541+RE33      DC    0F                xl16 expected result
00002420                                           1542+          DROP  R5
00002420  00000000 00000002                        1543           DC    XL16'0000000000000002 00000000FF012345'   result
00002428  00000000 FF012345
00002430  FFFFFFFF 00019000                        1544           DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00002438  00000038 EEEEEEFA
00002440  FFFFFFFF 00019000                        1545           DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00002448  00000038 0EEEEEFA
                                                   1546
                                                   1547           VRR_C VMH,2
00002450                                           1548+          DS    0FD
00002450                     00002450              1549+          USING *,R5              base for test data and test routine
00002450  00002490                                 1550+T34       DC    A(X34)            address of test routine
00002454  0022                                     1551+          DC    H'34'             test number
00002456  00                                       1552+          DC    X'00'
00002457  02                                       1553+          DC    HL1'2'            m4
00002458  E5D4C840 40404040                        1554+          DC    CL8'VMH'          instruction name
00002460  000024C8                                 1555+          DC    A(RE34+16)        address of v2 source
00002464  000024D8                                 1556+          DC    A(RE34+32)        address of v3 source
00002468  00000010                                 1557+          DC    A(16)             result length
0000246C  000024B8                                 1558+REA34     DC    A(RE34)           result address
00002470  00000000 00000000                        1559+          DS    FD                gap
00002478  00000000 00000000                        1560+V1O34     DS    XL16              V1 output
00002480  00000000 00000000
00002488  00000000 00000000                        1561+          DS    FD                gap
                                                   1562+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002490                                           1563+X34      DS    0F
00002490  E310 5010 0014                 00000010  1564+         LGF   R1,V2ADDR         load v2 source
00002496  E761 0000 0806                 00000000  1565+         VL    v22,0(R1)         use v22 to test decoder
0000249C  E310 5014 0014                 00000014  1566+         LGF   R1,V3ADDR         load v3 source
000024A2  E771 0000 0806                 00000000  1567+         VL    v23,0(R1)         use v23 to test decoder
000024A8  E766 7000 2EA3                           1568+         VMH   V22,V22,V23,2      test instruction (dest is a source)
000024AE  E760 5028 080E                 00002478  1569+         VST   V22,V1O34          save v1 output
000024B4  07FB                                     1570+         BR    R11               return
000024B8                                           1571+RE34     DC    0F                xl16 expected result
000024B8                                           1572+         DROP  R5
000024B8  FFFF0004 00193C6D                        1573          DC    XL16'FFFF000400193C6D 0051B52F00AA6E58'   result
000024C0  0051B52F 00AA6E58
000024C8  FF020304 05060750                        1574          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000024D0  090A0B0C 0D0E0F7F
000024D8  01020304 05060750                        1575          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
000024E0  090A0B78 0D0E0F7F
                                                   1576
                                                   1577          VRR_C VMH,2
000024E8                                           1578+         DS    0FD
000024E8                         000024E8          1579+         USING *,R5              base for test data and test routine
000024E8  00002528                                 1580+T35      DC    A(X35)            address of test routine
000024EC  0023                                     1581+         DC    H'35'             test number
000024EE  00                                       1582+         DC    X'00'
000024EF  02                                       1583+         DC    HL1'2'            m4
000024F0  E5D4C840 40404040                        1584+         DC    CL8'VMH'          instruction name
000024F8  00002560                                 1585+         DC    A(RE35+16)        address of v2 source
000024FC  00002570                                 1586+         DC    A(RE35+32)        address of v3 source
00002500  00000010                                 1587+         DC    A(16)             result length
00002504  00002550                                 1588+REA35    DC    A(RE35)           result address
00002508  00000000 00000000                        1589+         DS    FD                gap
00002510  00000000 00000000                        1590+V1O35    DS    XL16              V1 output
00002518  00000000 00000000
00002520  00000000 00000000                        1591+         DS    FD                gap
                                                   1592+*
00002528                                           1593+X35      DS    0F
00002528  E310 5010 0014                 00000010  1594+         LGF   R1,V2ADDR         load v2 source
0000252E  E761 0000 0806                 00000000  1595+         VL    v22,0(R1)         use v22 to test decoder
00002534  E310 5014 0014                 00000014  1596+         LGF   R1,V3ADDR         load v3 source
0000253A  E771 0000 0806                 00000000  1597+         VL    v23,0(R1)         use v23 to test decoder
00002540  E766 7000 2EA3                           1598+         VMH   V22,V22,V23,2      test instruction (dest is a source)
00002546  E760 5028 080E                 00002510  1599+         VST   V22,V1O35          save v1 output
0000254C  07FB                                     1600+         BR    R11               return
00002550                                           1601+RE35     DC    0F                xl16 expected result
00002550                                           1602+         DROP  R5
00002550  FFFFFF01 000A1B30                        1603          DC    XL16'FFFFFF01000A1B30 0024558D004EB01D'   result
00002558  0024558D 004EB01D
00002560  FF020304 05060750                        1604          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002568  090A0B0C 0D0E0F7F
00002570  00010102 02030328                        1605          DC    XL16'0001010202030328 0405053C0607073F'   v3
00002578  0405053C 0607073F
                                                   1606
                                                   1607          VRR_C VMH,2
00002580                                           1608+         DS    0FD
00002580                         00002580          1609+         USING *,R5              base for test data and test routine
00002580  000025C0                                 1610+T36      DC    A(X36)            address of test routine
00002584  0024                                     1611+         DC    H'36'             test number
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002586  00                                       1612+          DC    X'00'
00002587  02                                       1613+          DC    HL1'2'             m4
00002588  E5D4C840 40404040                        1614+          DC    CL8'VMH'           instruction name
00002590  000025F8                                 1615+          DC    A(RE36+16)         address of v2 source
00002594  00002608                                 1616+          DC    A(RE36+32)         address of v3 source
00002598  00000010                                 1617+          DC    A(16)              result length
0000259C  000025E8                                 1618+REA36     DC    A(RE36)            result address
000025A0  00000000 00000000                        1619+          DS    FD                 gap
000025A8  00000000 00000000                        1620+V1O36     DS    XL16               V1 output
000025B0  00000000 00000000
000025B8  00000000 00000000                        1621+          DS    FD                 gap
                                                   1622+*
000025C0                                           1623+X36       DS    0F
000025C0  E310 5010 0014                 00000010  1624+          LGF   R1,V2ADDR          load v2 source
000025C6  E761 0000 0806                 00000000  1625+          VL    v22,0(R1)          use v22 to test decoder
000025CC  E310 5014 0014                 00000014  1626+          LGF   R1,V3ADDR          load v3 source
000025D2  E771 0000 0806                 00000000  1627+          VL    v23,0(R1)          use v23 to test decoder
000025D8  E766 7000 2EA3                           1628+          VMH   V22,V22,V23,2       test instruction (dest is a source)
000025DE  E760 5028 080E                 000025A8  1629+          VST   V22,V1O36          save v1 output
000025E4  07FB                                     1630+          BR    R11                return
000025E8                                           1631+RE36      DC    0F                 xl16 expected result
000025E8                                           1632+          DROP  R5
000025E8  00000000 00000000                        1633           DC    XL16'0000000000000000 0009131E000D1B2B'   result
000025F0  0009131E 000D1B2B
000025F8  FF020304 05060750                        1634           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002600  090A0B0C 0D0E0F7F
00002608  00000000 0000000A                        1635           DC    XL16'000000000000000A 0101010F0101010F'   v3
00002610  0101010F 0101010F
                                                   1636
                                                   1637
                                                   1638 *-------------------------------------------------------------------
                                                   1639 *  VMLE   - Vector Multiply Logical Even
                                                   1640 *-------------------------------------------------------------------
                                                   1641 * Byte
                                                   1642           VRR_C VMLE,0
00002618                                           1643+          DS    0FD
00002618                           00002618        1644+          USING *,R5               base for test data and test routine
00002618  00002658                                 1645+T37       DC    A(X37)             address of test routine
0000261C  0025                                     1646+          DC    H'37'              test number
0000261E  00                                       1647+          DC    X'00'
0000261F  00                                       1648+          DC    HL1'0'             m4
00002620  E5D4D3C5 40404040                        1649+          DC    CL8'VMLE'          instruction name
00002628  00002690                                 1650+          DC    A(RE37+16)         address of v2 source
0000262C  000026A0                                 1651+          DC    A(RE37+32)         address of v3 source
00002630  00000010                                 1652+          DC    A(16)              result length
00002634  00002680                                 1653+REA37     DC    A(RE37)            result address
00002638  00000000 00000000                        1654+          DS    FD                 gap
00002640  00000000 00000000                        1655+V1O37     DS    XL16               V1 output
00002648  00000000 00000000
00002650  00000000 00000000                        1656+          DS    FD                 gap
                                                   1657+*
00002658                                           1658+X37       DS    0F
00002658  E310 5010 0014                 00000010  1659+          LGF   R1,V2ADDR          load v2 source
0000265E  E761 0000 0806                 00000000  1660+          VL    v22,0(R1)          use v22 to test decoder
00002664  E310 5014 0014                 00000014  1661+          LGF   R1,V3ADDR          load v3 source
0000266A  E771 0000 0806                 00000000  1662+          VL    v23,0(R1)          use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002670  E766 7000 0EA4                          1663+          VMLE  V22,V22,V23,0      test instruction (dest is a source)
00002676  E760 5028 080E                00002640  1664+          VST   V22,V1O37          save v1 output
0000267C  07FB                                    1665+          BR    R11               return
00002680                                          1666+RE37      DC    0F                xl16 expected result
00002680                                          1667+          DROP  R5
00002680  FE010000 00000000                       1668           DC    XL16'FE01000000000000 0C40000000000000'   result
00002688  0C400000 00000000
00002690  FF000000 00000019                       1669           DC    XL16'FF00000000000019 38000000000000FA'   v2
00002698  38000000 000000FA
000026A0  FF000000 00000019                       1670           DC    XL16'FF00000000000019 38000000000000FA'   v3
000026A8  38000000 000000FA
                                                  1671
                                                  1672           VRR_C VMLE,0
000026B0                                          1673+          DS    0FD
000026B0                    000026B0              1674+          USING *,R5              base for test data and test routine
000026B0  000026F0                                1675+T38       DC    A(X38)            address of test routine
000026B4  0026                                    1676+          DC    H'38'             test number
000026B6  00                                      1677+          DC    X'00'
000026B7  00                                      1678+          DC    HL1'0'            m4
000026B8  E5D4D3C5 40404040                       1679+          DC    CL8'VMLE'         instruction name
000026C0  00002728                                1680+          DC    A(RE38+16)        address of v2 source
000026C4  00002738                                1681+          DC    A(RE38+32)        address of v3 source
000026C8  00000010                                1682+          DC    A(16)             result length
000026CC  00002718                                1683+REA38     DC    A(RE38)           result address
000026D0  00000000 00000000                       1684+          DS    FD                gap
000026D8  00000000 00000000                       1685+V1O38     DS    XL16              V1 output
000026E0  00000000 00000000
000026E8  00000000 00000000                       1686+          DS    FD                gap
                                                  1687+*
000026F0                                          1688+X38       DS    0F
000026F0  E310 5010 0014                00000010  1689+          LGF   R1,V2ADDR         load v2 source
000026F6  E761 0000 0806                00000000  1690+          VL    v22,0(R1)         use v22 to test decoder
000026FC  E310 5014 0014                00000014  1691+          LGF   R1,V3ADDR         load v3 source
00002702  E771 0000 0806                00000000  1692+          VL    v23,0(R1)         use v23 to test decoder
00002708  E766 7000 0EA4                          1693+          VMLE  V22,V22,V23,0      test instruction (dest is a source)
0000270E  E760 5028 080E                000026D8  1694+          VST   V22,V1O38          save v1 output
00002714  07FB                                    1695+          BR    R11               return
00002718                                          1696+RE38      DC    0F                xl16 expected result
00002718                                          1697+          DROP  R5
00002718  FE010009 00190031                       1698           DC    XL16'FE01000900190031 00510079009C00D2'   result
00002720  00510079 009C00D2
00002728  FF020304 05060750                       1699           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00002730  090A0B78 0C0D0EFD
00002738  FF020304 05060750                       1700           DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00002740  090A0B78 0D0E0FFD
                                                  1701
                                                  1702           VRR_C VMLE,0
00002748                                          1703+          DS    0FD
00002748                    00002748              1704+          USING *,R5              base for test data and test routine
00002748  00002788                                1705+T39       DC    A(X39)            address of test routine
0000274C  0027                                    1706+          DC    H'39'             test number
0000274E  00                                      1707+          DC    X'00'
0000274F  00                                      1708+          DC    HL1'0'            m4
00002750  E5D4D3C5 40404040                       1709+          DC    CL8'VMLE'         instruction name
00002758  000027C0                                1710+          DC    A(RE39+16)        address of v2 source
0000275C  000027D0                                1711+          DC    A(RE39+32)        address of v3 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002760  00000010                          1712+          DC    A(16)              result length
00002764  000027B0                          1713+REA39     DC    A(RE39)            result address
00002768  00000000 00000000                 1714+          DS    FD                 gap
00002770  00000000 00000000                 1715+V1O39     DS    XL16               V1 output
00002778  00000000 00000000
00002780  00000000 00000000                 1716+          DS    FD                 gap
                                            1717+*
00002788                                    1718+X39       DS    0F
00002788  E310 5010 0014                00000010 1719+          LGF   R1,V2ADDR          load v2 source
0000278E  E761 0000 0806                00000000 1720+          VL    v22,0(R1)          use v22 to test decoder
00002794  E310 5014 0014                00000014 1721+          LGF   R1,V3ADDR          load v3 source
0000279A  E771 0000 0806                00000000 1722+          VL    v23,0(R1)          use v23 to test decoder
000027A0  E766 7000 0EA4                         1723+          VMLE  V22,V22,V23,0       test instruction (dest is a source)
000027A6  E760 5028 080E                00002770 1724+          VST   V22,V1O39          save v1 output
000027AC  07FB                                   1725+          BR    R11                return
000027B0                                         1726+RE39      DC    0F                 xl16 expected result
000027B0                                         1727+          DROP  R5
000027B0  FE010003 000A0015                      1728           DC    XL16'FE010003000A0015 0024003700480062'   result
000027B8  00240037 00480062
000027C0  FF020304 05060750                      1729           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000027C8  090A0B78 0C0D0EFD
000027D0  FF010102 02030328                      1730           DC    XL16'FF01010202030328 0405053C060707FE'   v3
000027D8  0405053C 060707FE
                                                 1731
                                                 1732           VRR_C VMLE,0
000027E0                                         1733+          DS    0FD
000027E0                    000027E0             1734+          USING *,R5               base for test data and test routine
000027E0  00002820                               1735+T40       DC    A(X40)             address of test routine
000027E4  0028                                   1736+          DC    H'40'              test number
000027E6  00                                     1737+          DC    X'00'
000027E7  00                                     1738+          DC    HL1'0'             m4
000027E8  E5D4D3C5 40404040                      1739+          DC    CL8'VMLE'          instruction name
000027F0  00002858                               1740+          DC    A(RE40+16)         address of v2 source
000027F4  00002868                               1741+          DC    A(RE40+32)         address of v3 source
000027F8  00000010                               1742+          DC    A(16)              result length
000027FC  00002848                               1743+REA40     DC    A(RE40)            result address
00002800  00000000 00000000                      1744+          DS    FD                 gap
00002808  00000000 00000000                      1745+V1O40     DS    XL16               V1 output
00002810  00000000 00000000
00002818  00000000 00000000                      1746+          DS    FD                 gap
                                                 1747+*
00002820                                         1748+X40       DS    0F
00002820  E310 5010 0014                00000010 1749+          LGF   R1,V2ADDR          load v2 source
00002826  E761 0000 0806                00000000 1750+          VL    v22,0(R1)          use v22 to test decoder
0000282C  E310 5014 0014                00000014 1751+          LGF   R1,V3ADDR          load v3 source
00002832  E771 0000 0806                00000000 1752+          VL    v23,0(R1)          use v23 to test decoder
00002838  E766 7000 0EA4                         1753+          VMLE  V22,V22,V23,0       test instruction (dest is a source)
0000283E  E760 5028 080E                00002808 1754+          VST   V22,V1O40          save v1 output
00002844  07FB                                   1755+          BR    R11                return
00002848                                         1756+RE40      DC    0F                 xl16 expected result
00002848                                         1757+          DROP  R5
00002848  FE010000 00000000                      1758           DC    XL16'FE01000000000000 0009000B000C000E'   result
00002850  0009000B 000C000E
00002858  FF020304 05060750                      1759           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00002860  090A0B78 0C0D0EFD
00002868  FF000000 0000000A                      1760           DC    XL16'FF0000000000000A 0101010F010101FF'   v3
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002870  0101010F 010101FF                        1761
                                                   1762 * Halfword
                                                   1763          VRR_C VMLE,1
00002878                                           1764+         DS    0FD
00002878                    00002878               1765+         USING *,R5              base for test data and test routine
00002878  000028B8                                 1766+T41      DC    A(X41)            address of test routine
0000287C  0029                                     1767+         DC    H'41'             test number
0000287E  00                                       1768+         DC    X'00'
0000287F  01                                       1769+         DC    HL1'1'            m4
00002880  E5D4D3C5 40404040                        1770+         DC    CL8'VMLE'         instruction name
00002888  000028F0                                 1771+         DC    A(RE41+16)        address of v2 source
0000288C  00002900                                 1772+         DC    A(RE41+32)        address of v3 source
00002890  00000010                                 1773+         DC    A(16)             result length
00002894  000028E0                                 1774+REA41    DC    A(RE41)           result address
00002898  00000000 00000000                        1775+         DS    FD                gap
000028A0  00000000 00000000                        1776+V1O41    DS    XL16              V1 output
000028A8  00000000 00000000
000028B0  00000000 00000000                        1777+         DS    FD                gap
                                                   1778+*
000028B8                                           1779+X41      DS    0F
000028B8  E310 5010 0014                00000010   1780+         LGF   R1,V2ADDR         load v2 source
000028BE  E761 0000 0806                00000000   1781+         VL    v22,0(R1)         use v22 to test decoder
000028C4  E310 5014 0014                00000014   1782+         LGF   R1,V3ADDR         load v3 source
000028CA  E771 0000 0806                00000000   1783+         VL    v23,0(R1)         use v23 to test decoder
000028D0  E766 7000 1EA4                           1784+         VMLE  V22,V22,V23,1      test instruction (dest is a source)
000028D6  E760 5028 080E                000028A0   1785+         VST   V22,V1O41          save v1 output
000028DC  07FB                                     1786+         BR    R11               return
000028E0                                           1787+RE41     DC    0F                xl16 expected result
000028E0                                           1788+         DROP  R5
000028E0  FFFE0001 00000000                        1789          DC    XL16'FFFE000100000000 00000C4008000000'   result
000028E8  00000C40 08000000
000028F0  FFFF0000 00000019                        1790          DC    XL16'FFFF000000000019 003800001000EEFA'   v2
000028F8  00380000 1000EEFA
00002900  FFFF0000 00000019                        1791          DC    XL16'FFFF000000000019 003800038000EEFA'   v3
00002908  00380003 8000EEFA
                                                   1792
                                                   1793          VRR_C VMLE,1
00002910                                           1794+         DS    0FD
00002910                    00002910               1795+         USING *,R5              base for test data and test routine
00002910  00002950                                 1796+T42      DC    A(X42)            address of test routine
00002914  002A                                     1797+         DC    H'42'             test number
00002916  00                                       1798+         DC    X'00'
00002917  01                                       1799+         DC    HL1'1'            m4
00002918  E5D4D3C5 40404040                        1800+         DC    CL8'VMLE'         instruction name
00002920  00002988                                 1801+         DC    A(RE42+16)        address of v2 source
00002924  00002998                                 1802+         DC    A(RE42+32)        address of v3 source
00002928  00000010                                 1803+         DC    A(16)             result length
0000292C  00002978                                 1804+REA42    DC    A(RE42)           result address
00002930  00000000 00000000                        1805+         DS    FD                gap
00002938  00000000 00000000                        1806+V1O42    DS    XL16              V1 output
00002940  00000000 00000000
00002948  00000000 00000000                        1807+         DS    FD                gap
                                                   1808+*
00002950                                           1809+X42      DS    0F
00002950  E310 5010 0014                00000010   1810+         LGF   R1,V2ADDR         load v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002956  E761 0000 0806                 00000000  1811+          VL    v22,0(R1)          use v22 to test decoder
0000295C  E310 5014 0014                 00000014  1812+          LGF   R1,V3ADDR          load v3 source
00002962  E771 0000 0806                 00000000  1813+          VL    v23,0(R1)          use v23 to test decoder
00002968  E766 7000 1EA4                           1814+          VMLE  V22,V22,V23,1       test instruction (dest is a source)
0000296E  E760 5028 080E                 00002938  1815+          VST   V22,V1O42           save v1 output
00002974  07FB                                     1816+          BR    R11                return
00002978                                           1817+RE42      DC    0F                 xl16 expected result
00002978                                           1818+          DROP  R5
00002978  FE04FC04 00193C24                        1819           DC    XL16'FE04FC0400193C24 0051B464009D51B6'   result
00002980  0051B464 009D51B6
00002988  FF020304 05060750                        1820           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00002990  090A0B78 0C0D0EFD
00002998  FF020304 05060750                        1821           DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
000029A0  090A0B78 0D0E0FFD
                                                   1822
                                                   1823           VRR_C VMLE,1
000029A8                                           1824+          DS    0FD
000029A8                           000029A8        1825+          USING *,R5               base for test data and test routine
000029A8  000029E8                                 1826+T43       DC    A(X43)             address of test routine
000029AC  002B                                     1827+          DC    H'43'              test number
000029AE  00                                       1828+          DC    X'00'
000029AF  01                                       1829+          DC    HL1'1'             m4
000029B0  E5D4D3C5 40404040                        1830+          DC    CL8'VMLE'          instruction name
000029B8  00002A20                                 1831+          DC    A(RE43+16)         address of v2 source
000029BC  00002A30                                 1832+          DC    A(RE43+32)         address of v3 source
000029C0  00000010                                 1833+          DC    A(16)              result length
000029C4  00002A10                                 1834+REA43     DC    A(RE43)            result address
000029C8  00000000 00000000                        1835+          DS    FD                 gap
000029D0  00000000 00000000                        1836+V1O43     DS    XL16               V1 output
000029D8  00000000 00000000
000029E0  00000000 00000000                        1837+          DS    FD                 gap
                                                   1838+*
000029E8                                           1839+X43       DS    0F
000029E8  E310 5010 0014                 00000010  1840+          LGF   R1,V2ADDR          load v2 source
000029EE  E761 0000 0806                 00000000  1841+          VL    v22,0(R1)          use v22 to test decoder
000029F4  E310 5014 0014                 00000014  1842+          LGF   R1,V3ADDR          load v3 source
000029FA  E771 0000 0806                 00000000  1843+          VL    v23,0(R1)          use v23 to test decoder
00002A00  E766 7000 1EA4                           1844+          VMLE  V22,V22,V23,1       test instruction (dest is a source)
00002A06  E760 5028 080E                 000029D0  1845+          VST   V22,V1O43           save v1 output
00002A0C  07FB                                     1846+          BR    R11                return
00002A10                                           1847+RE43      DC    0F                 xl16 expected result
00002A10                                           1848+          DROP  R5
00002A10  FE03FD02 000A1B12                        1849           DC    XL16'FE03FD02000A1B12 002455320048A25B'   result
00002A18  00245532 0048A25B
00002A20  FF020304 05060750                        1850           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00002A28  090A0B78 0C0D0EFD
00002A30  FF010102 02030328                        1851           DC    XL16'FF01010202030328 0405053C060707FE'   v3
00002A38  0405053C 060707FE
                                                   1852
                                                   1853           VRR_C VMLE,1
00002A40                                           1854+          DS    0FD
00002A40                           00002A40        1855+          USING *,R5               base for test data and test routine
00002A40  00002A80                                 1856+T44       DC    A(X44)             address of test routine
00002A44  002C                                     1857+          DC    H'44'              test number
00002A46  00                                       1858+          DC    X'00'
00002A47  01                                       1859+          DC    HL1'1'             m4
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002A48  E5D4D3C5 40404040                        1860+          DC    CL8'VMLE'          instruction name
00002A50  00002AB8                                 1861+          DC    A(RE44+16)         address of v2 source
00002A54  00002AC8                                 1862+          DC    A(RE44+32)         address of v3 source
00002A58  00000010                                 1863+          DC    A(16)              result length
00002A5C  00002AA8                                 1864+REA44     DC    A(RE44)            result address
00002A60  00000000 00000000                        1865+          DS    FD                 gap
00002A68  00000000 00000000                        1866+V1O44     DS    XL16               V1 output
00002A70  00000000 00000000
00002A78  00000000 00000000                        1867+          DS    FD                 gap
                                                   1868+*
00002A80                                           1869+X44       DS    0F
00002A80  E310 5010 0014                 00000010  1870+          LGF   R1,V2ADDR          load v2 source
00002A86  E761 0000 0806                 00000000  1871+          VL    v22,0(R1)          use v22 to test decoder
00002A8C  E310 5014 0014                 00000014  1872+          LGF   R1,V3ADDR          load v3 source
00002A92  E771 0000 0806                 00000000  1873+          VL    v23,0(R1)          use v23 to test decoder
00002A98  E766 7000 1EA4                           1874+          VMLE  V22,V22,V23,1       test instruction (dest is a source)
00002A9E  E760 5028 080E                 00002A68  1875+          VST   V22,V1O44          save v1 output
00002AA4  07FB                                     1876+          BR    R11                return
00002AA8                                           1877+RE44      DC    0F                 xl16 expected result
00002AA8                                           1878+          DROP  R5
00002AA8  FE02FE00 00000000                        1879           DC    XL16'FE02FE0000000000 0009130A000C190D'   result
00002AB0  0009130A 000C190D
00002AB8  FF020304 05060750                        1880           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00002AC0  090A0B78 0C0D0EFD
00002AC8  FF000000 0000000A                        1881           DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00002AD0  0101010F 010101FF
                                                   1882
                                                   1883 * Word
                                                   1884           VRR_C VMLE,2
00002AD8                                           1885+          DS    0FD
00002AD8                 00002AD8                  1886+          USING *,R5               base for test data and test routine
00002AD8  00002B18                                 1887+T45       DC    A(X45)             address of test routine
00002ADC  002D                                     1888+          DC    H'45'              test number
00002ADE  00                                       1889+          DC    X'00'
00002ADF  02                                       1890+          DC    HL1'2'             m4
00002AE0  E5D4D3C5 40404040                        1891+          DC    CL8'VMLE'          instruction name
00002AE8  00002B50                                 1892+          DC    A(RE45+16)         address of v2 source
00002AEC  00002B60                                 1893+          DC    A(RE45+32)         address of v3 source
00002AF0  00000010                                 1894+          DC    A(16)              result length
00002AF4  00002B40                                 1895+REA45     DC    A(RE45)            result address
00002AF8  00000000 00000000                        1896+          DS    FD                 gap
00002B00  00000000 00000000                        1897+V1O45     DS    XL16               V1 output
00002B08  00000000 00000000
00002B10  00000000 00000000                        1898+          DS    FD                 gap
                                                   1899+*
00002B18                                           1900+X45       DS    0F
00002B18  E310 5010 0014                 00000010  1901+          LGF   R1,V2ADDR          load v2 source
00002B1E  E761 0000 0806                 00000000  1902+          VL    v22,0(R1)          use v22 to test decoder
00002B24  E310 5014 0014                 00000014  1903+          LGF   R1,V3ADDR          load v3 source
00002B2A  E771 0000 0806                 00000000  1904+          VL    v23,0(R1)          use v23 to test decoder
00002B30  E766 7000 2EA4                           1905+          VMLE  V22,V22,V23,2       test instruction (dest is a source)
00002B36  E760 5028 080E                 00002B00  1906+          VST   V22,V1O45          save v1 output
00002B3C  07FB                                     1907+          BR    R11                return
00002B40                                           1908+RE45      DC    0F                 xl16 expected result
00002B40                                           1909+          DROP  R5
00002B40  FFFFFFFE 00000001                        1910           DC    XL16'FFFFFFFE00000001 0000000000000C40'   result
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002B48  00000000 00000C40
00002B50  FFFFFFFF 00019000                        1911          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00002B58  00000038 EEEEEEFA
00002B60  FFFFFFFF 00019000                        1912          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00002B68  00000038 0EEEEEFA
                                                   1913
                                                   1914          VRR_C VMLE,2
00002B70                                           1915+         DS    0FD
00002B70                     00002B70              1916+         USING *,R5                base for test data and test routine
00002B70  00002BB0                                 1917+T46      DC    A(X46)              address of test routine
00002B74  002E                                     1918+         DC    H'46'               test number
00002B76  00                                       1919+         DC    X'00'
00002B77  02                                       1920+         DC    HL1'2'              m4
00002B78  E5D4D3C5 40404040                        1921+         DC    CL8'VMLE'           instruction name
00002B80  00002BE8                                 1922+         DC    A(RE46+16)          address of v2 source
00002B84  00002BF8                                 1923+         DC    A(RE46+32)          address of v3 source
00002B88  00000010                                 1924+         DC    A(16)               result length
00002B8C  00002BD8                                 1925+REA46    DC    A(RE46)             result address
00002B90  00000000 00000000                        1926+         DS    FD                  gap
00002B98  00000000 00000000                        1927+V1O46    DS    XL16                V1 output
00002BA0  00000000 00000000
00002BA8  00000000 00000000                        1928+         DS    FD                  gap
                                                   1929+*
00002BB0                                           1930+X46      DS    0F
00002BB0  E310 5010 0014                 00000010  1931+         LGF   R1,V2ADDR           load v2 source
00002BB6  E761 0000 0806                 00000000  1932+         VL    v22,0(R1)           use v22 to test decoder
00002BBC  E310 5014 0014                 00000014  1933+         LGF   R1,V3ADDR           load v3 source
00002BC2  E771 0000 0806                 00000000  1934+         VL    v23,0(R1)           use v23 to test decoder
00002BC8  E766 7000 2EA4                           1935+         VMLE  V22,V22,V23,2        test instruction (dest is a source)
00002BCE  E760 5028 080E                 00002B98  1936+         VST   V22,V1O46           save v1 output
00002BD4  07FB                                     1937+         BR    R11                 return
00002BD8                                           1938+RE46     DC    0F                  xl16 expected result
00002BD8                                           1939+         DROP  R5
00002BD8  FE050206 04191810                        1940          DC    XL16'FE05020604191810 0051B52F85A6B1A0'   result
00002BE0  0051B52F 85A6B1A0
00002BE8  FF020304 05060750                        1941          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002BF0  090A0B0C 0D0E0F7F
00002BF8  FF020304 05060750                        1942          DC    XL16'FF02030405060750 090A0B780D0E0F7F'   v3
00002C00  090A0B78 0D0E0F7F
                                                   1943
                                                   1944          VRR_C VMLE,2
00002C08                                           1945+         DS    0FD
00002C08                     00002C08              1946+         USING *,R5                base for test data and test routine
00002C08  00002C48                                 1947+T47      DC    A(X47)              address of test routine
00002C0C  002F                                     1948+         DC    H'47'               test number
00002C0E  00                                       1949+         DC    X'00'
00002C0F  02                                       1950+         DC    HL1'2'              m4
00002C10  E5D4D3C5 40404040                        1951+         DC    CL8'VMLE'           instruction name
00002C18  00002C80                                 1952+         DC    A(RE47+16)          address of v2 source
00002C1C  00002C90                                 1953+         DC    A(RE47+32)          address of v3 source
00002C20  00000010                                 1954+         DC    A(16)               result length
00002C24  00002C70                                 1955+REA47    DC    A(RE47)             result address
00002C28  00000000 00000000                        1956+         DS    FD                  gap
00002C30  00000000 00000000                        1957+V1O47    DS    XL16                V1 output
00002C38  00000000 00000000
00002C40  00000000 00000000                        1958+         DS    FD                  gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   1959+*
00002C48                                           1960+X47      DS    0F
00002C48  E310 5010 0014                 00000010  1961+         LGF   R1,V2ADDR          load v2 source
00002C4E  E761 0000 0806                 00000000  1962+         VL    v22,0(R1)          use v22 to test decoder
00002C54  E310 5014 0014                 00000014  1963+         LGF   R1,V3ADDR          load v3 source
00002C5A  E771 0000 0806                 00000000  1964+         VL    v23,0(R1)          use v23 to test decoder
00002C60  E766 7000 2EA4                           1965+         VMLE  V22,V22,V23,2       test instruction (dest is a source)
00002C66  E760 5028 080E                 00002C30  1966+         VST   V22,V1O47           save v1 output
00002C6C  07FB                                     1967+         BR    R11                return
00002C70                                           1968+RE47     DC    0F                 xl16 expected result
00002C70                                           1969+         DROP  R5
00002C70  FE040103 FF0B0A08                        1970          DC    XL16'FE040103FF0B0A08 0024558DB7CDD2D0'   result
00002C78  0024558D B7CDD2D0
00002C80  FF020304 05060750                        1971          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002C88  090A0B0C 0D0E0F7F
00002C90  FF010102 02030328                        1972          DC    XL16'FF01010202030328 0405053C0607073F'   v3
00002C98  0405053C 0607073F
                                                   1973
                                                   1974          VRR_C VMLE,2
00002CA0                                           1975+         DS    0FD
00002CA0                         00002CA0          1976+         USING *,R5               base for test data and test routine
00002CA0  00002CE0                                 1977+T48      DC    A(X48)             address of test routine
00002CA4  0030                                     1978+         DC    H'48'              test number
00002CA6  00                                       1979+         DC    X'00'
00002CA7  02                                       1980+         DC    HL1'2'             m4
00002CA8  E5D4D3C5 40404040                        1981+         DC    CL8'VMLE'          instruction name
00002CB0  00002D18                                 1982+         DC    A(RE48+16)         address of v2 source
00002CB4  00002D28                                 1983+         DC    A(RE48+32)         address of v3 source
00002CB8  00000010                                 1984+         DC    A(16)              result length
00002CBC  00002D08                                 1985+REA48    DC    A(RE48)            result address
00002CC0  00000000 00000000                        1986+         DS    FD                 gap
00002CC8  00000000 00000000                        1987+V1O48    DS    XL16               V1 output
00002CD0  00000000 00000000
00002CD8  00000000 00000000                        1988+         DS    FD                 gap
                                                   1989+*
00002CE0                                           1990+X48      DS    0F
00002CE0  E310 5010 0014                 00000010  1991+         LGF   R1,V2ADDR          load v2 source
00002CE6  E761 0000 0806                 00000000  1992+         VL    v22,0(R1)          use v22 to test decoder
00002CEC  E310 5014 0014                 00000014  1993+         LGF   R1,V3ADDR          load v3 source
00002CF2  E771 0000 0806                 00000000  1994+         VL    v23,0(R1)          use v23 to test decoder
00002CF8  E766 7000 2EA4                           1995+         VMLE  V22,V22,V23,2       test instruction (dest is a source)
00002CFE  E760 5028 080E                 00002CC8  1996+         VST   V22,V1O48           save v1 output
00002D04  07FB                                     1997+         BR    R11                return
00002D08                                           1998+RE48     DC    0F                 xl16 expected result
00002D08                                           1999+         DROP  R5
00002D08  FE030100 FC000000                        2000          DC    XL16'FE030100FC000000 0009131EA8ADB1B4'   result
00002D10  0009131E A8ADB1B4
00002D18  FF020304 05060750                        2001          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002D20  090A0B0C 0D0E0F7F
00002D28  FF000000 0000000A                        2002          DC    XL16'FF0000000000000A 0101010F0101010F'   v3
00002D30  0101010F 0101010F
                                                   2003
                                                   2004 *-------------------------------------------------------------------
                                                   2005 *  VMLO   - Vector Multiply Logical Odd
                                                   2006 *-------------------------------------------------------------------
                                                   2007 * Byte
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   2008          VRR_C VMLO,0
00002D38                                           2009+         DS    0FD
00002D38                     00002D38              2010+         USING *,R5              base for test data and test routine
00002D38  00002D78                                 2011+T49      DC    A(X49)            address of test routine
00002D3C  0031                                     2012+         DC    H'49'             test number
00002D3E  00                                       2013+         DC    X'00'
00002D3F  00                                       2014+         DC    HL1'0'            m4
00002D40  E5D4D3D6 40404040                        2015+         DC    CL8'VMLO'         instruction name
00002D48  00002DB0                                 2016+         DC    A(RE49+16)        address of v2 source
00002D4C  00002DC0                                 2017+         DC    A(RE49+32)        address of v3 source
00002D50  00000010                                 2018+         DC    A(16)             result length
00002D54  00002DA0                                 2019+REA49    DC    A(RE49)           result address
00002D58  00000000 00000000                        2020+         DS    FD                gap
00002D60  00000000 00000000                        2021+V1O49    DS    XL16              V1 output
00002D68  00000000 00000000
00002D70  00000000 00000000                        2022+         DS    FD                gap
                                                   2023+*
00002D78                                           2024+X49      DS    0F
00002D78  E310 5010 0014                 00000010  2025+         LGF   R1,V2ADDR         load v2 source
00002D7E  E761 0000 0806                 00000000  2026+         VL    v22,0(R1)         use v22 to test decoder
00002D84  E310 5014 0014                 00000014  2027+         LGF   R1,V3ADDR         load v3 source
00002D8A  E771 0000 0806                 00000000  2028+         VL    v23,0(R1)         use v23 to test decoder
00002D90  E766 7000 0EA5                           2029+         VMLO  V22,V22,V23,0      test instruction (dest is a source)
00002D96  E760 5028 080E                 00002D60  2030+         VST   V22,V1O49         save v1 output
00002D9C  07FB                                     2031+         BR    R11               return
00002DA0                                           2032+RE49     DC    0F                xl16 expected result
00002DA0                                           2033+         DROP  R5
00002DA0  00000000 00000271                        2034          DC    XL16'0000000000000271 000000000000F424'   result
00002DA8  00000000 0000F424
00002DB0  FF000000 00000019                        2035          DC    XL16'FF00000000000019 38000000000000FA'   v2
00002DB8  38000000 000000FA
00002DC0  FF000000 00000019                        2036          DC    XL16'FF00000000000019 38000000000000FA'   v3
00002DC8  38000000 000000FA
                                                   2037
                                                   2038          VRR_C VMLO,0
00002DD0                                           2039+         DS    0FD
00002DD0                     00002DD0              2040+         USING *,R5              base for test data and test routine
00002DD0  00002E10                                 2041+T50      DC    A(X50)            address of test routine
00002DD4  0032                                     2042+         DC    H'50'             test number
00002DD6  00                                       2043+         DC    X'00'
00002DD7  00                                       2044+         DC    HL1'0'            m4
00002DD8  E5D4D3D6 40404040                        2045+         DC    CL8'VMLO'         instruction name
00002DE0  00002E48                                 2046+         DC    A(RE50+16)        address of v2 source
00002DE4  00002E58                                 2047+         DC    A(RE50+32)        address of v3 source
00002DE8  00000010                                 2048+         DC    A(16)             result length
00002DEC  00002E38                                 2049+REA50    DC    A(RE50)           result address
00002DF0  00000000 00000000                        2050+         DS    FD                gap
00002DF8  00000000 00000000                        2051+V1O50    DS    XL16              V1 output
00002E00  00000000 00000000
00002E08  00000000 00000000                        2052+         DS    FD                gap
                                                   2053+*
00002E10                                           2054+X50      DS    0F
00002E10  E310 5010 0014                 00000010  2055+         LGF   R1,V2ADDR         load v2 source
00002E16  E761 0000 0806                 00000000  2056+         VL    v22,0(R1)         use v22 to test decoder
00002E1C  E310 5014 0014                 00000014  2057+         LGF   R1,V3ADDR         load v3 source
00002E22  E771 0000 0806                 00000000  2058+         VL    v23,0(R1)         use v23 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002E28  E766 7000 0EA5                          2059+         VMLO  V22,V22,V23,0      test instruction (dest is a source)
00002E2E  E760 5028 080E               00002DF8   2060+         VST   V22,V1O50         save v1 output
00002E34  07FB                                    2061+         BR    R11               return
00002E38                                          2062+RE50     DC    0F                xl16 expected result
00002E38                                          2063+         DROP  R5
00002E38  00040010 00241900                       2064          DC    XL16'0004001000241900 0064384000B6FA09'   result
00002E40  00643840 00B6FA09
00002E48  FF020304 05060750                       2065          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00002E50  090A0B78 0C0D0EFD
00002E58  FF020304 05060750                       2066          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00002E60  090A0B78 0D0E0FFD
                                                  2067
                                                  2068          VRR_C VMLO,0
00002E68                                          2069+         DS    0FD
00002E68                  00002E68                2070+         USING *,R5              base for test data and test routine
00002E68  00002EA8                                2071+T51      DC    A(X51)            address of test routine
00002E6C  0033                                    2072+         DC    H'51'             test number
00002E6E  00                                      2073+         DC    X'00'
00002E6F  00                                      2074+         DC    HL1'0'            m4
00002E70  E5D4D3D6 40404040                       2075+         DC    CL8'VMLO'         instruction name
00002E78  00002EE0                                2076+         DC    A(RE51+16)        address of v2 source
00002E7C  00002EF0                                2077+         DC    A(RE51+32)        address of v3 source
00002E80  00000010                                2078+         DC    A(16)             result length
00002E84  00002ED0                                2079+REA51    DC    A(RE51)           result address
00002E88  00000000 00000000                       2080+         DS    FD                gap
00002E90  00000000 00000000                       2081+V1O51    DS    XL16              V1 output
00002E98  00000000 00000000
00002EA0  00000000 00000000                       2082+         DS    FD                gap
                                                  2083+*
00002EA8                                          2084+X51      DS    0F
00002EA8  E310 5010 0014               00000010   2085+         LGF   R1,V2ADDR         load v2 source
00002EAE  E761 0000 0806               00000000   2086+         VL    v22,0(R1)         use v22 to test decoder
00002EB4  E310 5014 0014               00000014   2087+         LGF   R1,V3ADDR         load v3 source
00002EBA  E771 0000 0806               00000000   2088+         VL    v23,0(R1)         use v23 to test decoder
00002EC0  E766 7000 0EA5                          2089+         VMLO  V22,V22,V23,0      test instruction (dest is a source)
00002EC6  E760 5028 080E               00002E90   2090+         VST   V22,V1O51         save v1 output
00002ECC  07FB                                    2091+         BR    R11               return
00002ED0                                          2092+RE51     DC    0F                xl16 expected result
00002ED0                                          2093+         DROP  R5
00002ED0  00020008 00120C80                       2094          DC    XL16'0002000800120C80 00321C20005BFB06'   result
00002ED8  00321C20 005BFB06
00002EE0  FF020304 05060750                       2095          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00002EE8  090A0B78 0C0D0EFD
00002EF0  FF010102 02030328                       2096          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00002EF8  0405053C 060707FE
                                                  2097
                                                  2098          VRR_C VMLO,0
00002F00                                          2099+         DS    0FD
00002F00                  00002F00                2100+         USING *,R5              base for test data and test routine
00002F00  00002F40                                2101+T52      DC    A(X52)            address of test routine
00002F04  0034                                    2102+         DC    H'52'             test number
00002F06  00                                      2103+         DC    X'00'
00002F07  00                                      2104+         DC    HL1'0'            m4
00002F08  E5D4D3D6 40404040                       2105+         DC    CL8'VMLO'         instruction name
00002F10  00002F78                                2106+         DC    A(RE52+16)        address of v2 source
00002F14  00002F88                                2107+         DC    A(RE52+32)        address of v3 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002F18  00000010                                2108+          DC    A(16)              result length
00002F1C  00002F68                                2109+REA52     DC    A(RE52)            result address
00002F20  00000000 00000000                       2110+          DS    FD                 gap
00002F28  00000000 00000000                       2111+V1O52     DS    XL16               V1 output
00002F30  00000000 00000000
00002F38  00000000 00000000                       2112+          DS    FD                 gap
                                                  2113+*
00002F40                                          2114+X52       DS    0F
00002F40  E310 5010 0014                00000010  2115+          LGF   R1,V2ADDR          load v2 source
00002F46  E761 0000 0806                00000000  2116+          VL    v22,0(R1)          use v22 to test decoder
00002F4C  E310 5014 0014                00000014  2117+          LGF   R1,V3ADDR          load v3 source
00002F52  E771 0000 0806                00000000  2118+          VL    v23,0(R1)          use v23 to test decoder
00002F58  E766 7000 0EA5                          2119+          VMLO  V22,V22,V23,0       test instruction (dest is a source)
00002F5E  E760 5028 080E                00002F28  2120+          VST   V22,V1O52          save v1 output
00002F64  07FB                                    2121+          BR    R11                return
00002F68                                          2122+RE52      DC    0F                 xl16 expected result
00002F68                                          2123+          DROP  R5
00002F68  00000000 00000320                       2124           DC    XL16'0000000000000320 000A0708000DFC03'   result
00002F70  000A0708 000DFC03
00002F78  FF020304 05060750                       2125           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00002F80  090A0B78 0C0D0EFD
00002F88  FF000000 0000000A                       2126           DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00002F90  0101010F 010101FF
                                                  2127
                                                  2128 * Halfword
                                                  2129           VRR_C VMLO,1
00002F98                                          2130+          DS    0FD
00002F98                        00002F98          2131+          USING *,R5               base for test data and test routine
00002F98  00002FD8                                2132+T53       DC    A(X53)             address of test routine
00002F9C  0035                                    2133+          DC    H'53'              test number
00002F9E  00                                      2134+          DC    X'00'
00002F9F  01                                      2135+          DC    HL1'1'             m4
00002FA0  E5D4D3D6 40404040                       2136+          DC    CL8'VMLO'          instruction name
00002FA8  00003010                                2137+          DC    A(RE53+16)         address of v2 source
00002FAC  00003020                                2138+          DC    A(RE53+32)         address of v3 source
00002FB0  00000010                                2139+          DC    A(16)              result length
00002FB4  00003000                                2140+REA53     DC    A(RE53)            result address
00002FB8  00000000 00000000                       2141+          DS    FD                 gap
00002FC0  00000000 00000000                       2142+V1O53     DS    XL16               V1 output
00002FC8  00000000 00000000
00002FD0  00000000 00000000                       2143+          DS    FD                 gap
                                                  2144+*
00002FD8                                          2145+X53       DS    0F
00002FD8  E310 5010 0014                00000010  2146+          LGF   R1,V2ADDR          load v2 source
00002FDE  E761 0000 0806                00000000  2147+          VL    v22,0(R1)          use v22 to test decoder
00002FE4  E310 5014 0014                00000014  2148+          LGF   R1,V3ADDR          load v3 source
00002FEA  E771 0000 0806                00000000  2149+          VL    v23,0(R1)          use v23 to test decoder
00002FF0  E766 7000 1EA5                          2150+          VMLO  V22,V22,V23,1       test instruction (dest is a source)
00002FF6  E760 5028 080E                00002FC0  2151+          VST   V22,V1O53          save v1 output
00002FFC  07FB                                    2152+          BR    R11                return
00003000                                          2153+RE53      DC    0F                 xl16 expected result
00003000                                          2154+          DROP  R5
00003000  00000000 00000271                       2155           DC    XL16'0000000000000271 00000000DF15CC24'   result
00003008  00000000 DF15CC24
00003010  FFFF0000 00000019                       2156           DC    XL16'FFFF000000000019 003800001000EEFA'   v2
00003018  00380000 1000EEFA
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003020  FFFF0000 00000019                        2157          DC    XL16'FFFF000000000019 003800038000EEFA'   v3
00003028  00380003 8000EEFA
                                                   2158
                                                   2159          VRR_C VMLO,1
00003030                                           2160+         DS    0FD
00003030                      00003030             2161+         USING *,R5              base for test data and test routine
00003030  00003070                                 2162+T54      DC    A(X54)            address of test routine
00003034  0036                                     2163+         DC    H'54'             test number
00003036  00                                       2164+         DC    X'00'
00003037  01                                       2165+         DC    HL1'1'            m4
00003038  E5D4D3D6 40404040                       2166+         DC    CL8'VMLO'         instruction name
00003040  000030A8                                 2167+         DC    A(RE54+16)        address of v2 source
00003044  000030B8                                 2168+         DC    A(RE54+32)        address of v3 source
00003048  00000010                                 2169+         DC    A(16)             result length
0000304C  00003098                                 2170+REA54    DC    A(RE54)           result address
00003050  00000000 00000000                        2171+         DS    FD                gap
00003058  00000000 00000000                        2172+V1O54    DS    XL16              V1 output
00003060  00000000 00000000
00003068  00000000 00000000                        2173+         DS    FD                gap
                                                   2174+*
00003070                                           2175+X54      DS    0F
00003070  E310 5010 0014                00000010   2176+         LGF   R1,V2ADDR         load v2 source
00003076  E761 0000 0806                00000000   2177+         VL    v22,0(R1)         use v22 to test decoder
0000307C  E310 5014 0014                00000014   2178+         LGF   R1,V3ADDR         load v3 source
00003082  E771 0000 0806                00000000   2179+         VL    v23,0(R1)         use v23 to test decoder
00003088  E766 7000 1EA5                           2180+         VMLO  V22,V22,V23,1      test instruction (dest is a source)
0000308E  E760 5028 080E                00003058   2181+         VST   V22,V1O54          save v1 output
00003094  07FB                                     2182+         BR    R11               return
00003098                                           2183+RE54     DC    0F                xl16 expected result
00003098                                           2184+         DROP  R5
00003098  00091810 00357900                        2185          DC    XL16'0009181000357900 0083884000EFA309'   result
000030A0  00838840 00EFA309
000030A8  FF020304 05060750                        2186          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000030B0  090A0B78 0C0D0EFD
000030B8  FF020304 05060750                        2187          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
000030C0  090A0B78 0D0E0FFD
                                                   2188
                                                   2189          VRR_C VMLO,1
000030C8                                           2190+         DS    0FD
000030C8                      000030C8             2191+         USING *,R5              base for test data and test routine
000030C8  00003108                                 2192+T55      DC    A(X55)            address of test routine
000030CC  0037                                     2193+         DC    H'55'             test number
000030CE  00                                       2194+         DC    X'00'
000030CF  01                                       2195+         DC    HL1'1'            m4
000030D0  E5D4D3D6 40404040                        2196+         DC    CL8'VMLO'         instruction name
000030D8  00003140                                 2197+         DC    A(RE55+16)        address of v2 source
000030DC  00003150                                 2198+         DC    A(RE55+32)        address of v3 source
000030E0  00000010                                 2199+         DC    A(16)             result length
000030E4  00003130                                 2200+REA55    DC    A(RE55)           result address
000030E8  00000000 00000000                        2201+         DS    FD                gap
000030F0  00000000 00000000                        2202+V1O55    DS    XL16              V1 output
000030F8  00000000 00000000
00003100  00000000 00000000                        2203+         DS    FD                gap
                                                   2204+*
00003108                                           2205+X55      DS    0F
00003108  E310 5010 0014                00000010   2206+         LGF   R1,V2ADDR         load v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000310E  E761 0000 0806                 00000000  2207+          VL    v22,0(R1)          use v22 to test decoder
00003114  E310 5014 0014                 00000014  2208+          LGF   R1,V3ADDR          load v3 source
0000311A  E771 0000 0806                 00000000  2209+          VL    v23,0(R1)          use v23 to test decoder
00003120  E766 7000 1EA5                           2210+          VMLO  V22,V22,V23,1       test instruction (dest is a source)
00003126  E760 5028 080E                 000030F0  2211+          VST   V22,V1O55           save v1 output
0000312C  07FB                                     2212+          BR    R11                return
00003130                                           2213+RE55      DC    0F                 xl16 expected result
00003130                                           2214+          DROP  R5
00003130  00030A08 00171480                        2215           DC    XL16'00030A0800171480 003C08200077CA06'   result
00003138  003C0820 0077CA06
00003140  FF020304 05060750                        2216           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003148  090A0B78 0C0D0EFD
00003150  FF010102 02030328                        2217           DC    XL16'FF01010202030328 0405053C060707FE'   v3
00003158  0405053C 060707FE
                                                   2218
                                                   2219           VRR_C VMLO,1
00003160                                           2220+          DS    0FD
00003160                         00003160          2221+          USING *,R5               base for test data and test routine
00003160  000031A0                                 2222+T56       DC    A(X56)             address of test routine
00003164  0038                                     2223+          DC    H'56'              test number
00003166  00                                       2224+          DC    X'00'
00003167  01                                       2225+          DC    HL1'1'             m4
00003168  E5D4D3D6 40404040                       2226+          DC    CL8'VMLO'          instruction name
00003170  000031D8                                 2227+          DC    A(RE56+16)         address of v2 source
00003174  000031E8                                 2228+          DC    A(RE56+32)         address of v3 source
00003178  00000010                                 2229+          DC    A(16)              result length
0000317C  000031C8                                 2230+REA56     DC    A(RE56)            result address
00003180  00000000 00000000                        2231+          DS    FD                 gap
00003188  00000000 00000000                        2232+V1O56     DS    XL16               V1 output
00003190  00000000 00000000
00003198  00000000 00000000                        2233+          DS    FD                 gap
                                                   2234+*
000031A0                                           2235+X56       DS    0F
000031A0  E310 5010 0014                 00000010  2236+          LGF   R1,V2ADDR          load v2 source
000031A6  E761 0000 0806                 00000000  2237+          VL    v22,0(R1)          use v22 to test decoder
000031AC  E310 5014 0014                 00000014  2238+          LGF   R1,V3ADDR          load v3 source
000031B2  E771 0000 0806                 00000000  2239+          VL    v23,0(R1)          use v23 to test decoder
000031B8  E766 7000 1EA5                           2240+          VMLO  V22,V22,V23,1       test instruction (dest is a source)
000031BE  E760 5028 080E                 00003188  2241+          VST   V22,V1O56           save v1 output
000031C4  07FB                                     2242+          BR    R11                return
000031C8                                           2243+RE56      DC    0F                 xl16 expected result
000031C8                                           2244+          DROP  R5
000031C8  00000000 00004920                        2245           DC    XL16'0000000000004920 000C2408001DEB03'   result
000031D0  000C2408 001DEB03
000031D8  FF020304 05060750                        2246           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000031E0  090A0B78 0C0D0EFD
000031E8  FF000000 0000000A                        2247           DC    XL16'FF0000000000000A 0101010F010101FF'   v3
000031F0  0101010F 010101FF
                                                   2248
                                                   2249 * Word
                                                   2250           VRR_C VMLO,2
000031F8                                           2251+          DS    0FD
000031F8                         000031F8          2252+          USING *,R5               base for test data and test routine
000031F8  00003238                                 2253+T57       DC    A(X57)             address of test routine
000031FC  0039                                     2254+          DC    H'57'              test number
000031FE  00                                       2255+          DC    X'00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000031FF  02                                      2256+          DC    HL1'2'              m4
00003200  E5D4D3D6 40404040                       2257+          DC    CL8'VMLO'           instruction name
00003208  00003270                                2258+          DC    A(RE57+16)          address of v2 source
0000320C  00003280                                2259+          DC    A(RE57+32)          address of v3 source
00003210  00000010                                2260+          DC    A(16)               result length
00003214  00003260                                2261+REA57     DC    A(RE57)             result address
00003218  00000000 00000000                       2262+          DS    FD                  gap
00003220  00000000 00000000                       2263+V1O57     DS    XL16                V1 output
00003228  00000000 00000000
00003230  00000000 00000000                       2264+          DS    FD                  gap
                                                  2265+*
00003238                                          2266+X57       DS    0F
00003238  E310 5010 0014                 00000010 2267+          LGF   R1,V2ADDR           load v2 source
0000323E  E761 0000 0806                 00000000 2268+          VL    v22,0(R1)           use v22 to test decoder
00003244  E310 5014 0014                 00000014 2269+          LGF   R1,V3ADDR           load v3 source
0000324A  E771 0000 0806                 00000000 2270+          VL    v23,0(R1)           use v23 to test decoder
00003250  E766 7000 2EA5                          2271+          VMLO  V22,V22,V23,2        test instruction (dest is a source)
00003256  E760 5028 080E                 00003220 2272+          VST   V22,V1O57           save v1 output
0000325C  07FB                                    2273+          BR    R11               return
00003260                                          2274+RE57      DC    0F                xl16 expected result
00003260                                          2275+          DROP  R5
00003260  00000002 71000000                       2276           DC    XL16'0000000271000000 0DF0123F4FEDCC24'   result
00003268  0DF0123F 4FEDCC24
00003270  FFFFFFFF 00019000                       2277           DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00003278  00000038 EEEEEEFA
00003280  FFFFFFFF 00019000                       2278           DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00003288  00000038 0EEEEEFA
                                                  2279
                                                  2280           VRR_C VMLO,2
00003290                                          2281+          DS    0FD
00003290                  00003290                2282+          USING *,R5              base for test data and test routine
00003290  000032D0                                2283+T58       DC    A(X58)              address of test routine
00003294  003A                                    2284+          DC    H'58'               test number
00003296  00                                      2285+          DC    X'00'
00003297  02                                      2286+          DC    HL1'2'              m4
00003298  E5D4D3D6 40404040                       2287+          DC    CL8'VMLO'           instruction name
000032A0  00003308                                2288+          DC    A(RE58+16)          address of v2 source
000032A4  00003318                                2289+          DC    A(RE58+32)          address of v3 source
000032A8  00000010                                2290+          DC    A(16)               result length
000032AC  000032F8                                2291+REA58     DC    A(RE58)             result address
000032B0  00000000 00000000                       2292+          DS    FD                  gap
000032B8  00000000 00000000                       2293+V1O58     DS    XL16                V1 output
000032C0  00000000 00000000
000032C8  00000000 00000000                       2294+          DS    FD                  gap
                                                  2295+*
000032D0                                          2296+X58       DS    0F
000032D0  E310 5010 0014                 00000010 2297+          LGF   R1,V2ADDR           load v2 source
000032D6  E761 0000 0806                 00000000 2298+          VL    v22,0(R1)           use v22 to test decoder
000032DC  E310 5014 0014                 00000014 2299+          LGF   R1,V3ADDR           load v3 source
000032E2  E771 0000 0806                 00000000 2300+          VL    v23,0(R1)           use v23 to test decoder
000032E8  E766 7000 2EA5                          2301+          VMLO  V22,V22,V23,2        test instruction (dest is a source)
000032EE  E760 5028 080E                 000032B8 2302+          VST   V22,V1O58           save v1 output
000032F4  07FB                                    2303+          BR    R11               return
000032F8                                          2304+RE58      DC    0F                xl16 expected result
000032F8                                          2305+          DROP  R5
000032F8  00193C6D 77F57900                       2306           DC    XL16'00193C6D77F57900 00AA6E5898D42101'   result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003300  00AA6E58 98D42101
00003308  FF020304 05060750                        2307           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003310  090A0B0C 0D0E0F7F
00003318  FF020304 05060750                        2308           DC    XL16'FF02030405060750 090A0B780D0E0F7F'   v3
00003320  090A0B78 0D0E0F7F
                                                   2309
                                                   2310           VRR_C VMLO,2
00003328                                           2311+          DS    0FD
00003328                    00003328               2312+          USING *,R5              base for test data and test routine
00003328  00003368                                 2313+T59       DC    A(X59)            address of test routine
0000332C  003B                                     2314+          DC    H'59'             test number
0000332E  00                                       2315+          DC    X'00'
0000332F  02                                       2316+          DC    HL1'2'            m4
00003330  E5D4D3D6 40404040                        2317+          DC    CL8'VMLO'         instruction name
00003338  000033A0                                 2318+          DC    A(RE59+16)        address of v2 source
0000333C  000033B0                                 2319+          DC    A(RE59+32)        address of v3 source
00003340  00000010                                 2320+          DC    A(16)             result length
00003344  00003390                                 2321+REA59     DC    A(RE59)           result address
00003348  00000000 00000000                        2322+          DS    FD                gap
00003350  00000000 00000000                        2323+V1O59     DS    XL16              V1 output
00003358  00000000 00000000
00003360  00000000 00000000                        2324+          DS    FD                gap
                                                   2325+*
00003368                                           2326+X59       DS    0F
00003368  E310 5010 0014                00000010   2327+          LGF   R1,V2ADDR         load v2 source
0000336E  E761 0000 0806                00000000   2328+          VL    v22,0(R1)         use v22 to test decoder
00003374  E310 5014 0014                00000014   2329+          LGF   R1,V3ADDR         load v3 source
0000337A  E771 0000 0806                00000000   2330+          VL    v23,0(R1)         use v23 to test decoder
00003380  E766 7000 2EA5                           2331+          VMLO  V22,V22,V23,2      test instruction (dest is a source)
00003386  E760 5028 080E                00003350   2332+          VST   V22,V1O59         save v1 output
0000338C  07FB                                     2333+          BR    R11               return
00003390                                           2334+RE59      DC    0F                xl16 expected result
00003390                                           2335+          DROP  R5
00003390  000A1B30 90F71480                        2336           DC    XL16'000A1B3090F71480 004EB01DFF5B4941'   result
00003398  004EB01D FF5B4941
000033A0  FF020304 05060750                        2337           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000033A8  090A0B0C 0D0E0F7F
000033B0  FF010102 02030328                        2338           DC    XL16'FF01010202030328 0405053C0607073F'   v3
000033B8  0405053C 0607073F
                                                   2339
                                                   2340           VRR_C VMLO,2
000033C0                                           2341+          DS    0FD
000033C0                    000033C0               2342+          USING *,R5              base for test data and test routine
000033C0  00003400                                 2343+T60       DC    A(X60)            address of test routine
000033C4  003C                                     2344+          DC    H'60'             test number
000033C6  00                                       2345+          DC    X'00'
000033C7  02                                       2346+          DC    HL1'2'            m4
000033C8  E5D4D3D6 40404040                        2347+          DC    CL8'VMLO'         instruction name
000033D0  00003438                                 2348+          DC    A(RE60+16)        address of v2 source
000033D4  00003448                                 2349+          DC    A(RE60+32)        address of v3 source
000033D8  00000010                                 2350+          DC    A(16)             result length
000033DC  00003428                                 2351+REA60     DC    A(RE60)           result address
000033E0  00000000 00000000                        2352+          DS    FD                gap
000033E8  00000000 00000000                        2353+V1O60     DS    XL16              V1 output
000033F0  00000000 00000000
000033F8  00000000 00000000                        2354+          DS    FD                gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   2355+*
00003400                                           2356+X60      DS    0F
00003400  E310 5010 0014                 00000010  2357+         LGF   R1,V2ADDR          load v2 source
00003406  E761 0000 0806                 00000000  2358+         VL    v22,0(R1)          use v22 to test decoder
0000340C  E310 5014 0014                 00000014  2359+         LGF   R1,V3ADDR          load v3 source
00003412  E771 0000 0806                 00000000  2360+         VL    v23,0(R1)          use v23 to test decoder
00003418  E766 7000 2EA5                           2361+         VMLO  V22,V22,V23,2       test instruction (dest is a source)
0000341E  E760 5028 080E                 000033E8  2362+         VST   V22,V1O60           save v1 output
00003424  07FB                                     2363+         BR    R11                return
00003428                                           2364+RE60     DC    0F                 xl16 expected result
00003428                                           2365+         DROP  R5
00003428  00000000 323C4920                        2366          DC    XL16'00000000323C4920 000D1B2B60616771'   result
00003430  000D1B2B 60616771
00003438  FF020304 05060750                        2367          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003440  090A0B0C 0D0E0F7F
00003448  FF000000 0000000A                        2368          DC    XL16'FF0000000000000A 0101010F0101010F'   v3
00003450  0101010F 0101010F
                                                   2369
                                                   2370 *-------------------------------------------------------------------
                                                   2371 *  VME    - Vector Multiply Even
                                                   2372 *-------------------------------------------------------------------
                                                   2373 * Byte
                                                   2374          VRR_C VME,0
00003458                                           2375+         DS    0FD
00003458                 00003458                  2376+         USING *,R5               base for test data and test routine
00003458  00003498                                 2377+T61      DC    A(X61)             address of test routine
0000345C  003D                                     2378+         DC    H'61'              test number
0000345E  00                                       2379+         DC    X'00'
0000345F  00                                       2380+         DC    HL1'0'             m4
00003460  E5D4C540 40404040                        2381+         DC    CL8'VME'           instruction name
00003468  000034D0                                 2382+         DC    A(RE61+16)         address of v2 source
0000346C  000034E0                                 2383+         DC    A(RE61+32)         address of v3 source
00003470  00000010                                 2384+         DC    A(16)              result length
00003474  000034C0                                 2385+REA61    DC    A(RE61)            result address
00003478  00000000 00000000                        2386+         DS    FD                 gap
00003480  00000000 00000000                        2387+V1O61    DS    XL16               V1 output
00003488  00000000 00000000
00003490  00000000 00000000                        2388+         DS    FD                 gap
                                                   2389+*
00003498                                           2390+X61      DS    0F
00003498  E310 5010 0014                 00000010  2391+         LGF   R1,V2ADDR          load v2 source
0000349E  E761 0000 0806                 00000000  2392+         VL    v22,0(R1)          use v22 to test decoder
000034A4  E310 5014 0014                 00000014  2393+         LGF   R1,V3ADDR          load v3 source
000034AA  E771 0000 0806                 00000000  2394+         VL    v23,0(R1)          use v23 to test decoder
000034B0  E766 7000 0EA6                           2395+         VME   V22,V22,V23,0       test instruction (dest is a source)
000034B6  E760 5028 080E                 00003480  2396+         VST   V22,V1O61           save v1 output
000034BC  07FB                                     2397+         BR    R11                return
000034C0                                           2398+RE61     DC    0F                 xl16 expected result
000034C0                                           2399+         DROP  R5
000034C0  00010000 00000000                        2400          DC    XL16'0001000000000000 0C40000000000000'   result
000034C8  0C400000 00000000
000034D0  FF000000 00000019                        2401          DC    XL16'FF00000000000019 38000000000000FA'   v2
000034D8  38000000 000000FA
000034E0  FF000000 00000019                        2402          DC    XL16'FF00000000000019 38000000000000FA'   v3
000034E8  38000000 000000FA
                                                   2403
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   2404          VRR_C VME,0
000034F0                                           2405+         DS    0FD
000034F0                     000034F0              2406+         USING *,R5              base for test data and test routine
000034F0  00003530                                 2407+T62      DC    A(X62)            address of test routine
000034F4  003E                                     2408+         DC    H'62'             test number
000034F6  00                                       2409+         DC    X'00'
000034F7  00                                       2410+         DC    HL1'0'            m4
000034F8  E5D4C540 40404040                        2411+         DC    CL8'VME'          instruction name
00003500  00003568                                 2412+         DC    A(RE62+16)        address of v2 source
00003504  00003578                                 2413+         DC    A(RE62+32)        address of v3 source
00003508  00000010                                 2414+         DC    A(16)             result length
0000350C  00003558                                 2415+REA62    DC    A(RE62)           result address
00003510  00000000 00000000                        2416+         DS    FD                gap
00003518  00000000 00000000                        2417+V1O62    DS    XL16              V1 output
00003520  00000000 00000000
00003528  00000000 00000000                        2418+         DS    FD                gap
                                                   2419+*
00003530                                           2420+X62      DS    0F
00003530  E310 5010 0014                 00000010  2421+         LGF   R1,V2ADDR         load v2 source
00003536  E761 0000 0806                 00000000  2422+         VL    v22,0(R1)         use v22 to test decoder
0000353C  E310 5014 0014                 00000014  2423+         LGF   R1,V3ADDR         load v3 source
00003542  E771 0000 0806                 00000000  2424+         VL    v23,0(R1)         use v23 to test decoder
00003548  E766 7000 0EA6                           2425+         VME   V22,V22,V23,0      test instruction (dest is a source)
0000354E  E760 5028 080E                 00003518  2426+         VST   V22,V1O62          save v1 output
00003554  07FB                                     2427+         BR    R11               return
00003558                                           2428+RE62     DC    0F                xl16 expected result
00003558                                           2429+         DROP  R5
00003558  00010009 00190031                        2430          DC    XL16'0001000900190031 00510079009C00D2'   result
00003560  00510079 009C00D2
00003568  FF020304 05060750                        2431          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003570  090A0B78 0C0D0EFD
00003578  FF020304 05060750                        2432          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00003580  090A0B78 0D0E0FFD
                                                   2433
                                                   2434          VRR_C VME,0
00003588                                           2435+         DS    0FD
00003588                     00003588              2436+         USING *,R5              base for test data and test routine
00003588  000035C8                                 2437+T63      DC    A(X63)            address of test routine
0000358C  003F                                     2438+         DC    H'63'             test number
0000358E  00                                       2439+         DC    X'00'
0000358F  00                                       2440+         DC    HL1'0'            m4
00003590  E5D4C540 40404040                        2441+         DC    CL8'VME'          instruction name
00003598  00003600                                 2442+         DC    A(RE63+16)        address of v2 source
0000359C  00003610                                 2443+         DC    A(RE63+32)        address of v3 source
000035A0  00000010                                 2444+         DC    A(16)             result length
000035A4  000035F0                                 2445+REA63    DC    A(RE63)           result address
000035A8  00000000 00000000                        2446+         DS    FD                gap
000035B0  00000000 00000000                        2447+V1O63    DS    XL16              V1 output
000035B8  00000000 00000000
000035C0  00000000 00000000                        2448+         DS    FD                gap
                                                   2449+*
000035C8                                           2450+X63      DS    0F
000035C8  E310 5010 0014                 00000010  2451+         LGF   R1,V2ADDR         load v2 source
000035CE  E761 0000 0806                 00000000  2452+         VL    v22,0(R1)         use v22 to test decoder
000035D4  E310 5014 0014                 00000014  2453+         LGF   R1,V3ADDR         load v3 source
000035DA  E771 0000 0806                 00000000  2454+         VL    v23,0(R1)         use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000035E0  E766 7000 0EA6                          2455+          VME   V22,V22,V23,0      test instruction (dest is a source)
000035E6  E760 5028 080E                 000035B0 2456+          VST   V22,V1O63          save v1 output
000035EC  07FB                                    2457+          BR    R11               return
000035F0                                          2458+RE63      DC    0F                xl16 expected result
000035F0                                          2459+          DROP  R5
000035F0  00010003 000A0015                       2460           DC    XL16'00010003000A0015 0024003700480062'   result
000035F8  00240037 00480062
00003600  FF020304 05060750                       2461           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003608  090A0B78 0C0D0EFD
00003610  FF010102 02030328                       2462           DC    XL16'FF01010202030328 0405053C060707FE'   v3
00003618  0405053C 060707FE
                                                  2463
                                                  2464           VRR_C VME,0
00003620                                          2465+          DS    0FD
00003620                  00003620                2466+          USING *,R5              base for test data and test routine
00003620  00003660                                2467+T64       DC    A(X64)            address of test routine
00003624  0040                                    2468+          DC    H'64'             test number
00003626  00                                      2469+          DC    X'00'
00003627  00                                      2470+          DC    HL1'0'            m4
00003628  E5D4C540 40404040                       2471+          DC    CL8'VME'          instruction name
00003630  00003698                                2472+          DC    A(RE64+16)        address of v2 source
00003634  000036A8                                2473+          DC    A(RE64+32)        address of v3 source
00003638  00000010                                2474+          DC    A(16)             result length
0000363C  00003688                                2475+REA64     DC    A(RE64)           result address
00003640  00000000 00000000                       2476+          DS    FD                gap
00003648  00000000 00000000                       2477+V1O64     DS    XL16              V1 output
00003650  00000000 00000000
00003658  00000000 00000000                       2478+          DS    FD                gap
                                                  2479+*
00003660                                          2480+X64       DS    0F
00003660  E310 5010 0014                 00000010 2481+          LGF   R1,V2ADDR         load v2 source
00003666  E761 0000 0806                 00000000 2482+          VL    v22,0(R1)         use v22 to test decoder
0000366C  E310 5014 0014                 00000014 2483+          LGF   R1,V3ADDR         load v3 source
00003672  E771 0000 0806                 00000000 2484+          VL    v23,0(R1)         use v23 to test decoder
00003678  E766 7000 0EA6                          2485+          VME   V22,V22,V23,0      test instruction (dest is a source)
0000367E  E760 5028 080E                 00003648 2486+          VST   V22,V1O64         save v1 output
00003684  07FB                                    2487+          BR    R11               return
00003688                                          2488+RE64      DC    0F                xl16 expected result
00003688                                          2489+          DROP  R5
00003688  00010000 00000000                       2490           DC    XL16'0001000000000000 0009000B000C000E'   result
00003690  0009000B 000C000E
00003698  FF020304 05060750                       2491           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000036A0  090A0B78 0C0D0EFD
000036A8  FF000000 0000000A                       2492           DC    XL16'FF0000000000000A 0101010F010101FF'   v3
000036B0  0101010F 010101FF
                                                  2493
                                                  2494 * Halfword
                                                  2495           VRR_C VME,1
000036B8                                          2496+          DS    0FD
000036B8                  000036B8                2497+          USING *,R5              base for test data and test routine
000036B8  000036F8                                2498+T65       DC    A(X65)            address of test routine
000036BC  0041                                    2499+          DC    H'65'             test number
000036BE  00                                      2500+          DC    X'00'
000036BF  01                                      2501+          DC    HL1'1'            m4
000036C0  E5D4C540 40404040                       2502+          DC    CL8'VME'          instruction name
000036C8  00003730                                2503+          DC    A(RE65+16)        address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000036CC  00003740                                2504+          DC    A(RE65+32)         address of v3 source
000036D0  00000010                                2505+          DC    A(16)              result length
000036D4  00003720                                2506+REA65     DC    A(RE65)            result address
000036D8  00000000 00000000                       2507+          DS    FD                 gap
000036E0  00000000 00000000                       2508+V1O65     DS    XL16               V1 output
000036E8  00000000 00000000
000036F0  00000000 00000000                       2509+          DS    FD                 gap
                                                  2510+*
000036F8                                          2511+X65       DS    0F
000036F8  E310 5010 0014                 00000010 2512+          LGF   R1,V2ADDR          load v2 source
000036FE  E761 0000 0806                 00000000 2513+          VL    v22,0(R1)          use v22 to test decoder
00003704  E310 5014 0014                 00000014 2514+          LGF   R1,V3ADDR          load v3 source
0000370A  E771 0000 0806                 00000000 2515+          VL    v23,0(R1)          use v23 to test decoder
00003710  E766 7000 1EA6                          2516+          VME   V22,V22,V23,1       test instruction (dest is a source)
00003716  E760 5028 080E                 000036E0 2517+          VST   V22,V1O65          save v1 output
0000371C  07FB                                    2518+          BR    R11                return
00003720                                          2519+RE65      DC    0F                 xl16 expected result
00003720                                          2520+          DROP  R5
00003720  00000001 00000000                       2521           DC    XL16'0000000100000000 00000C40F8000000'   result
00003728  00000C40 F8000000
00003730  FFFF0000 00000019                       2522           DC    XL16'FFFF000000000019 003800001000EEFA'   v2
00003738  00380000 1000EEFA
00003740  FFFF0000 00000019                       2523           DC    XL16'FFFF000000000019 003800038000EEFA'   v3
00003748  00380003 8000EEFA
                                                  2524
                                                  2525           VRR_C VME,1
00003750                                          2526+          DS    0FD
00003750                  00003750                2527+          USING *,R5               base for test data and test routine
00003750  00003790                                2528+T66       DC    A(X66)             address of test routine
00003754  0042                                    2529+          DC    H'66'              test number
00003756  00                                      2530+          DC    X'00'
00003757  01                                      2531+          DC    HL1'1'             m4
00003758  E5D4C540 40404040                       2532+          DC    CL8'VME'           instruction name
00003760  000037C8                                2533+          DC    A(RE66+16)         address of v2 source
00003764  000037D8                                2534+          DC    A(RE66+32)         address of v3 source
00003768  00000010                                2535+          DC    A(16)              result length
0000376C  000037B8                                2536+REA66     DC    A(RE66)            result address
00003770  00000000 00000000                       2537+          DS    FD                 gap
00003778  00000000 00000000                       2538+V1O66     DS    XL16               V1 output
00003780  00000000 00000000
00003788  00000000 00000000                       2539+          DS    FD                 gap
                                                  2540+*
00003790                                          2541+X66       DS    0F
00003790  E310 5010 0014                 00000010 2542+          LGF   R1,V2ADDR          load v2 source
00003796  E761 0000 0806                 00000000 2543+          VL    v22,0(R1)          use v22 to test decoder
0000379C  E310 5014 0014                 00000014 2544+          LGF   R1,V3ADDR          load v3 source
000037A2  E771 0000 0806                 00000000 2545+          VL    v23,0(R1)          use v23 to test decoder
000037A8  E766 7000 1EA6                          2546+          VME   V22,V22,V23,1       test instruction (dest is a source)
000037AE  E760 5028 080E                 00003778 2547+          VST   V22,V1O66          save v1 output
000037B4  07FB                                    2548+          BR    R11                return
000037B8                                          2549+RE66      DC    0F                 xl16 expected result
000037B8                                          2550+          DROP  R5
000037B8  0000FC04 00193C24                       2551           DC    XL16'0000FC0400193C24 0051B464009D51B6'   result
000037C0  0051B464 009D51B6
000037C8  FF020304 05060750                       2552           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000037D0  090A0B78 0C0D0EFD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000037D8  FF020304 05060750                        2553          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
000037E0  090A0B78 0D0E0FFD
                                                   2554
                                                   2555          VRR_C VME,1
000037E8                                           2556+         DS    0FD
000037E8                      000037E8             2557+         USING *,R5              base for test data and test routine
000037E8  00003828                                 2558+T67      DC    A(X67)            address of test routine
000037EC  0043                                     2559+         DC    H'67'             test number
000037EE  00                                       2560+         DC    X'00'
000037EF  01                                       2561+         DC    HL1'1'            m4
000037F0  E5D4C540 40404040                        2562+         DC    CL8'VME'          instruction name
000037F8  00003860                                 2563+         DC    A(RE67+16)        address of v2 source
000037FC  00003870                                 2564+         DC    A(RE67+32)        address of v3 source
00003800  00000010                                 2565+         DC    A(16)             result length
00003804  00003850                                 2566+REA67    DC    A(RE67)           result address
00003808  00000000 00000000                        2567+         DS    FD                gap
00003810  00000000 00000000                        2568+V1O67    DS    XL16              V1 output
00003818  00000000 00000000
00003820  00000000 00000000                        2569+         DS    FD                gap
                                                   2570+*
00003828                                           2571+X67      DS    0F
00003828  E310 5010 0014                00000010   2572+         LGF   R1,V2ADDR         load v2 source
0000382E  E761 0000 0806                00000000   2573+         VL    v22,0(R1)         use v22 to test decoder
00003834  E310 5014 0014                00000014   2574+         LGF   R1,V3ADDR         load v3 source
0000383A  E771 0000 0806                00000000   2575+         VL    v23,0(R1)         use v23 to test decoder
00003840  E766 7000 1EA6                           2576+         VME   V22,V22,V23,1      test instruction (dest is a source)
00003846  E760 5028 080E                00003810   2577+         VST   V22,V1O67          save v1 output
0000384C  07FB                                     2578+         BR    R11               return
00003850                                           2579+RE67     DC    0F                xl16 expected result
00003850                                           2580+         DROP  R5
00003850  0000FD02 000A1B12                        2581          DC    XL16'0000FD02000A1B12 002455320048A25B'   result
00003858  00245532 0048A25B
00003860  FF020304 05060750                        2582          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003868  090A0B78 0C0D0EFD
00003870  FF010102 02030328                        2583          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00003878  0405053C 060707FE
                                                   2584
                                                   2585          VRR_C VME,1
00003880                                           2586+         DS    0FD
00003880                      00003880             2587+         USING *,R5              base for test data and test routine
00003880  000038C0                                 2588+T68      DC    A(X68)            address of test routine
00003884  0044                                     2589+         DC    H'68'             test number
00003886  00                                       2590+         DC    X'00'
00003887  01                                       2591+         DC    HL1'1'            m4
00003888  E5D4C540 40404040                        2592+         DC    CL8'VME'          instruction name
00003890  000038F8                                 2593+         DC    A(RE68+16)        address of v2 source
00003894  00003908                                 2594+         DC    A(RE68+32)        address of v3 source
00003898  00000010                                 2595+         DC    A(16)             result length
0000389C  000038E8                                 2596+REA68    DC    A(RE68)           result address
000038A0  00000000 00000000                        2597+         DS    FD                gap
000038A8  00000000 00000000                        2598+V1O68    DS    XL16              V1 output
000038B0  00000000 00000000
000038B8  00000000 00000000                        2599+         DS    FD                gap
                                                   2600+*
000038C0                                           2601+X68      DS    0F
000038C0  E310 5010 0014                00000010   2602+         LGF   R1,V2ADDR         load v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000038C6  E761 0000 0806                 00000000  2603+         VL    v22,0(R1)          use v22 to test decoder
000038CC  E310 5014 0014                 00000014  2604+         LGF   R1,V3ADDR          load v3 source
000038D2  E771 0000 0806                 00000000  2605+         VL    v23,0(R1)          use v23 to test decoder
000038D8  E766 7000 1EA6                           2606+         VME   V22,V22,V23,1       test instruction (dest is a source)
000038DE  E760 5028 080E                 000038A8  2607+         VST   V22,V1O68           save v1 output
000038E4  07FB                                     2608+         BR    R11                return
000038E8                                           2609+RE68     DC    0F                 xl16 expected result
000038E8                                           2610+         DROP  R5
000038E8  0000FE00 00000000                        2611          DC    XL16'0000FE0000000000 0009130A000C190D'   result
000038F0  0009130A 000C190D
000038F8  FF020304 05060750                        2612          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003900  090A0B78 0C0D0EFD
00003908  FF000000 0000000A                        2613          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00003910  0101010F 010101FF
                                                   2614
                                                   2615 * Word
                                                   2616          VRR_C VME,2
00003918                                           2617+         DS    0FD
00003918                           00003918        2618+         USING *,R5               base for test data and test routine
00003918  00003958                                 2619+T69      DC    A(X69)             address of test routine
0000391C  0045                                     2620+         DC    H'69'              test number
0000391E  00                                       2621+         DC    X'00'
0000391F  02                                       2622+         DC    HL1'2'             m4
00003920  E5D4C540 40404040                        2623+         DC    CL8'VME'           instruction name
00003928  00003990                                 2624+         DC    A(RE69+16)         address of v2 source
0000392C  000039A0                                 2625+         DC    A(RE69+32)         address of v3 source
00003930  00000010                                 2626+         DC    A(16)              result length
00003934  00003980                                 2627+REA69    DC    A(RE69)            result address
00003938  00000000 00000000                        2628+         DS    FD                 gap
00003940  00000000 00000000                        2629+V1O69    DS    XL16               V1 output
00003948  00000000 00000000
00003950  00000000 00000000                        2630+         DS    FD                 gap
                                                   2631+*
00003958                                           2632+X69      DS    0F
00003958  E310 5010 0014                 00000010  2633+         LGF   R1,V2ADDR          load v2 source
0000395E  E761 0000 0806                 00000000  2634+         VL    v22,0(R1)          use v22 to test decoder
00003964  E310 5014 0014                 00000014  2635+         LGF   R1,V3ADDR          load v3 source
0000396A  E771 0000 0806                 00000000  2636+         VL    v23,0(R1)          use v23 to test decoder
00003970  E766 7000 2EA6                           2637+         VME   V22,V22,V23,2       test instruction (dest is a source)
00003976  E760 5028 080E                 00003940  2638+         VST   V22,V1O69           save v1 output
0000397C  07FB                                     2639+         BR    R11                return
00003980                                           2640+RE69     DC    0F                 xl16 expected result
00003980                                           2641+         DROP  R5
00003980  00000000 00000001                        2642          DC    XL16'0000000000000001 0000000000000C40'   result
00003988  00000000 00000C40
00003990  FFFFFFFF 00019000                        2643          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00003998  00000038 EEEEEEFA
000039A0  FFFFFFFF 00019000                        2644          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
000039A8  00000038 0EEEEEFA
                                                   2645
                                                   2646          VRR_C VME,2
000039B0                                           2647+         DS    0FD
000039B0                           000039B0        2648+         USING *,R5               base for test data and test routine
000039B0  000039F0                                 2649+T70      DC    A(X70)             address of test routine
000039B4  0046                                     2650+         DC    H'70'              test number
000039B6  00                                       2651+         DC    X'00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000039B7  02                                      2652+          DC    HL1'2'              m4
000039B8  E5D4C540 40404040                       2653+          DC    CL8'VME'            instruction name
000039C0  00003A28                                2654+          DC    A(RE70+16)          address of v2 source
000039C4  00003A38                                2655+          DC    A(RE70+32)          address of v3 source
000039C8  00000010                                2656+          DC    A(16)               result length
000039CC  00003A18                                2657+REA70     DC    A(RE70)             result address
000039D0  00000000 00000000                       2658+          DS    FD                  gap
000039D8  00000000 00000000                       2659+V1O70     DS    XL16                V1 output
000039E0  00000000 00000000
000039E8  00000000 00000000                       2660+          DS    FD                  gap
                                                  2661+*
000039F0                                          2662+X70       DS    0F
000039F0  E310 5010 0014                 00000010 2663+          LGF   R1,V2ADDR           load v2 source
000039F6  E761 0000 0806                 00000000 2664+          VL    v22,0(R1)           use v22 to test decoder
000039FC  E310 5014 0014                 00000014 2665+          LGF   R1,V3ADDR           load v3 source
00003A02  E771 0000 0806                 00000000 2666+          VL    v23,0(R1)           use v23 to test decoder
00003A08  E766 7000 2EA6                          2667+          VME   V22,V22,V23,2        test instruction (dest is a source)
00003A0E  E760 5028 080E                 000039D8 2668+          VST   V22,V1O70           save v1 output
00003A14  07FB                                    2669+          BR    R11                 return
00003A18                                          2670+RE70      DC    0F                  xl16 expected result
00003A18                                          2671+          DROP  R5
00003A18  FFFF0004 0C191810                       2672           DC    XL16'FFFF00040C191810 0051B52F85A6B1A0'   result
00003A20  0051B52F 85A6B1A0
00003A28  FF020304 05060750                       2673           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003A30  090A0B0C 0D0E0F7F
00003A38  01020304 05060750                       2674           DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00003A40  090A0B78 0D0E0F7F
                                                  2675
                                                  2676           VRR_C VME,2
00003A48                                          2677+          DS    0FD
00003A48                  00003A48                2678+          USING *,R5                base for test data and test routine
00003A48  00003A88                                2679+T71       DC    A(X71)              address of test routine
00003A4C  0047                                    2680+          DC    H'71'               test number
00003A4E  00                                      2681+          DC    X'00'
00003A4F  02                                      2682+          DC    HL1'2'              m4
00003A50  E5D4C540 40404040                       2683+          DC    CL8'VME'            instruction name
00003A58  00003AC0                                2684+          DC    A(RE71+16)          address of v2 source
00003A5C  00003AD0                                2685+          DC    A(RE71+32)          address of v3 source
00003A60  00000010                                2686+          DC    A(16)               result length
00003A64  00003AB0                                2687+REA71     DC    A(RE71)             result address
00003A68  00000000 00000000                       2688+          DS    FD                  gap
00003A70  00000000 00000000                       2689+V1O71     DS    XL16                V1 output
00003A78  00000000 00000000
00003A80  00000000 00000000                       2690+          DS    FD                  gap
                                                  2691+*
00003A88                                          2692+X71       DS    0F
00003A88  E310 5010 0014                 00000010 2693+          LGF   R1,V2ADDR           load v2 source
00003A8E  E761 0000 0806                 00000000 2694+          VL    v22,0(R1)           use v22 to test decoder
00003A94  E310 5014 0014                 00000014 2695+          LGF   R1,V3ADDR           load v3 source
00003A9A  E771 0000 0806                 00000000 2696+          VL    v23,0(R1)           use v23 to test decoder
00003AA0  E766 7000 2EA6                          2697+          VME   V22,V22,V23,2        test instruction (dest is a source)
00003AA6  E760 5028 080E                 00003A70 2698+          VST   V22,V1O71           save v1 output
00003AAC  07FB                                    2699+          BR    R11                 return
00003AB0                                          2700+RE71      DC    0F                  xl16 expected result
00003AB0                                          2701+          DROP  R5
00003AB0  FFFFFF01 030B0A08                       2702           DC    XL16'FFFFFF01030B0A08 0024558DB7CDD2D0'   result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003AB8  0024558D B7CDD2D0
00003AC0  FF020304 05060750                        2703           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003AC8  090A0B0C 0D0E0F7F
00003AD0  00010102 02030328                        2704           DC    XL16'0001010202030328 0405053C0607073F'   v3
00003AD8  0405053C 0607073F
                                                   2705
                                                   2706           VRR_C VME,2
00003AE0                                           2707+          DS    0FD
00003AE0                     00003AE0              2708+          USING *,R5              base for test data and test routine
00003AE0  00003B20                                 2709+T72       DC    A(X72)            address of test routine
00003AE4  0048                                     2710+          DC    H'72'             test number
00003AE6  00                                       2711+          DC    X'00'
00003AE7  02                                       2712+          DC    HL1'2'            m4
00003AE8  E5D4C540 40404040                        2713+          DC    CL8'VME'          instruction name
00003AF0  00003B58                                 2714+          DC    A(RE72+16)        address of v2 source
00003AF4  00003B68                                 2715+          DC    A(RE72+32)        address of v3 source
00003AF8  00000010                                 2716+          DC    A(16)             result length
00003AFC  00003B48                                 2717+REA72     DC    A(RE72)           result address
00003B00  00000000 00000000                        2718+          DS    FD                gap
00003B08  00000000 00000000                        2719+V1O72     DS    XL16              V1 output
00003B10  00000000 00000000
00003B18  00000000 00000000                        2720+          DS    FD                gap
                                                   2721+*
00003B20                                           2722+X72       DS    0F
00003B20  E310 5010 0014                 00000010  2723+          LGF   R1,V2ADDR         load v2 source
00003B26  E761 0000 0806                 00000000  2724+          VL    v22,0(R1)         use v22 to test decoder
00003B2C  E310 5014 0014                 00000014  2725+          LGF   R1,V3ADDR         load v3 source
00003B32  E771 0000 0806                 00000000  2726+          VL    v23,0(R1)         use v23 to test decoder
00003B38  E766 7000 2EA6                           2727+          VME   V22,V22,V23,2      test instruction (dest is a source)
00003B3E  E760 5028 080E                 00003B08  2728+          VST   V22,V1O72          save v1 output
00003B44  07FB                                     2729+          BR    R11               return
00003B48                                           2730+RE72      DC    0F                xl16 expected result
00003B48                                           2731+          DROP  R5
00003B48  00000000 00000000                        2732           DC    XL16'0000000000000000 0009131EA8ADB1B4'   result
00003B50  0009131E A8ADB1B4
00003B58  FF020304 05060750                        2733           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003B60  090A0B0C 0D0E0F7F
00003B68  00000000 0000000A                        2734           DC    XL16'000000000000000A 0101010F0101010F'   v3
00003B70  0101010F 0101010F
                                                   2735
                                                   2736 *-------------------------------------------------------------------
                                                   2737 *  VMO    - Vector Multiply Odd
                                                   2738 *-------------------------------------------------------------------
                                                   2739 * Byte
                                                   2740           VRR_C VMO,0
00003B78                                           2741+          DS    0FD
00003B78                     00003B78              2742+          USING *,R5              base for test data and test routine
00003B78  00003BB8                                 2743+T73       DC    A(X73)            address of test routine
00003B7C  0049                                     2744+          DC    H'73'             test number
00003B7E  00                                       2745+          DC    X'00'
00003B7F  00                                       2746+          DC    HL1'0'            m4
00003B80  E5D4D640 40404040                        2747+          DC    CL8'VMO'          instruction name
00003B88  00003BF0                                 2748+          DC    A(RE73+16)        address of v2 source
00003B8C  00003C00                                 2749+          DC    A(RE73+32)        address of v3 source
00003B90  00000010                                 2750+          DC    A(16)             result length
00003B94  00003BE0                                 2751+REA73     DC    A(RE73)           result address
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003B98  00000000 00000000                        2752+          DS    FD                gap
00003BA0  00000000 00000000                        2753+V1O73     DS    XL16              V1 output
00003BA8  00000000 00000000
00003BB0  00000000 00000000                        2754+          DS    FD                gap
                                                   2755+*
00003BB8                                           2756+X73       DS    0F
00003BB8  E310 5010 0014                 00000010  2757+          LGF   R1,V2ADDR         load v2 source
00003BBE  E761 0000 0806                 00000000  2758+          VL    v22,0(R1)         use v22 to test decoder
00003BC4  E310 5014 0014                 00000014  2759+          LGF   R1,V3ADDR         load v3 source
00003BCA  E771 0000 0806                 00000000  2760+          VL    v23,0(R1)         use v23 to test decoder
00003BD0  E766 7000 0EA7                           2761+          VMO   V22,V22,V23,0      test instruction (dest is a source)
00003BD6  E760 5028 080E                 00003BA0  2762+          VST   V22,V1O73         save v1 output
00003BDC  07FB                                     2763+          BR    R11               return
00003BE0                                           2764+RE73      DC    0F                xl16 expected result
00003BE0                                           2765+          DROP  R5
00003BE0  00000000 00000271                        2766           DC    XL16'0000000000000271 0000000000000024'   result
00003BE8  00000000 00000024
00003BF0  FF000000 00000019                        2767           DC    XL16'FF00000000000019 38000000000000FA'   v2
00003BF8  38000000 000000FA
00003C00  FF000000 00000019                        2768           DC    XL16'FF00000000000019 38000000000000FA'   v3
00003C08  38000000 000000FA
                                                   2769
                                                   2770           VRR_C VMO,0
00003C10                                           2771+          DS    0FD
00003C10                       00003C10            2772+          USING *,R5              base for test data and test routine
00003C10  00003C50                                 2773+T74       DC    A(X74)            address of test routine
00003C14  004A                                     2774+          DC    H'74'             test number
00003C16  00                                       2775+          DC    X'00'
00003C17  00                                       2776+          DC    HL1'0'            m4
00003C18  E5D4D640 40404040                        2777+          DC    CL8'VMO'          instruction name
00003C20  00003C88                                 2778+          DC    A(RE74+16)        address of v2 source
00003C24  00003C98                                 2779+          DC    A(RE74+32)        address of v3 source
00003C28  00000010                                 2780+          DC    A(16)             result length
00003C2C  00003C78                                 2781+REA74     DC    A(RE74)           result address
00003C30  00000000 00000000                        2782+          DS    FD                gap
00003C38  00000000 00000000                        2783+V1O74     DS    XL16              V1 output
00003C40  00000000 00000000
00003C48  00000000 00000000                        2784+          DS    FD                gap
                                                   2785+*
00003C50                                           2786+X74       DS    0F
00003C50  E310 5010 0014                 00000010  2787+          LGF   R1,V2ADDR         load v2 source
00003C56  E761 0000 0806                 00000000  2788+          VL    v22,0(R1)         use v22 to test decoder
00003C5C  E310 5014 0014                 00000014  2789+          LGF   R1,V3ADDR         load v3 source
00003C62  E771 0000 0806                 00000000  2790+          VL    v23,0(R1)         use v23 to test decoder
00003C68  E766 7000 0EA7                           2791+          VMO   V22,V22,V23,0      test instruction (dest is a source)
00003C6E  E760 5028 080E                 00003C38  2792+          VST   V22,V1O74         save v1 output
00003C74  07FB                                     2793+          BR    R11               return
00003C78                                           2794+RE74      DC    0F                xl16 expected result
00003C78                                           2795+          DROP  R5
00003C78  00040010 00241900                        2796           DC    XL16'0004001000241900 0064384000B60009'   result
00003C80  00643840 00B60009
00003C88  FF020304 05060750                        2797           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003C90  090A0B78 0C0D0EFD
00003C98  FF020304 05060750                        2798           DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00003CA0  090A0B78 0D0E0FFD
                                                   2799
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```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   2800          VRR_C VMO,0
00003CA8                                           2801+         DS    0FD
00003CA8                     00003CA8              2802+         USING *,R5              base for test data and test routine
00003CA8  00003CE8                                 2803+T75      DC    A(X75)            address of test routine
00003CAC  004B                                     2804+         DC    H'75'             test number
00003CAE  00                                       2805+         DC    X'00'
00003CAF  00                                       2806+         DC    HL1'0'            m4
00003CB0  E5D4D640 40404040                        2807+         DC    CL8'VMO'          instruction name
00003CB8  00003D20                                 2808+         DC    A(RE75+16)        address of v2 source
00003CBC  00003D30                                 2809+         DC    A(RE75+32)        address of v3 source
00003CC0  00000010                                 2810+         DC    A(16)             result length
00003CC4  00003D10                                 2811+REA75    DC    A(RE75)           result address
00003CC8  00000000 00000000                        2812+         DS    FD                gap
00003CD0  00000000 00000000                        2813+V1O75    DS    XL16              V1 output
00003CD8  00000000 00000000
00003CE0  00000000 00000000                        2814+         DS    FD                gap
                                                   2815+*
00003CE8                                           2816+X75      DS    0F
00003CE8  E310 5010 0014                 00000010  2817+         LGF   R1,V2ADDR         load v2 source
00003CEE  E761 0000 0806                 00000000  2818+         VL    v22,0(R1)         use v22 to test decoder
00003CF4  E310 5014 0014                 00000014  2819+         LGF   R1,V3ADDR         load v3 source
00003CFA  E771 0000 0806                 00000000  2820+         VL    v23,0(R1)         use v23 to test decoder
00003D00  E766 7000 0EA7                           2821+         VMO   V22,V22,V23,0      test instruction (dest is a source)
00003D06  E760 5028 080E                 00003CD0  2822+         VST   V22,V1O75         save v1 output
00003D0C  07FB                                     2823+         BR    R11               return
00003D10                                           2824+RE75     DC    0F                xl16 expected result
00003D10                                           2825+         DROP  R5
00003D10  00020008 00120C80                        2826          DC    XL16'0002000800120C80 00321C20005B0006'   result
00003D18  00321C20 005B0006
00003D20  FF020304 05060750                        2827          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003D28  090A0B78 0C0D0EFD
00003D30  FF010102 02030328                        2828          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00003D38  0405053C 060707FE
                                                   2829
                                                   2830          VRR_C VMO,0
00003D40                                           2831+         DS    0FD
00003D40                     00003D40              2832+         USING *,R5              base for test data and test routine
00003D40  00003D80                                 2833+T76      DC    A(X76)            address of test routine
00003D44  004C                                     2834+         DC    H'76'             test number
00003D46  00                                       2835+         DC    X'00'
00003D47  00                                       2836+         DC    HL1'0'            m4
00003D48  E5D4D640 40404040                        2837+         DC    CL8'VMO'          instruction name
00003D50  00003DB8                                 2838+         DC    A(RE76+16)        address of v2 source
00003D54  00003DC8                                 2839+         DC    A(RE76+32)        address of v3 source
00003D58  00000010                                 2840+         DC    A(16)             result length
00003D5C  00003DA8                                 2841+REA76    DC    A(RE76)           result address
00003D60  00000000 00000000                        2842+         DS    FD                gap
00003D68  00000000 00000000                        2843+V1O76    DS    XL16              V1 output
00003D70  00000000 00000000
00003D78  00000000 00000000                        2844+         DS    FD                gap
                                                   2845+*
00003D80                                           2846+X76      DS    0F
00003D80  E310 5010 0014                 00000010  2847+         LGF   R1,V2ADDR         load v2 source
00003D86  E761 0000 0806                 00000000  2848+         VL    v22,0(R1)         use v22 to test decoder
00003D8C  E310 5014 0014                 00000014  2849+         LGF   R1,V3ADDR         load v3 source
00003D92  E771 0000 0806                 00000000  2850+         VL    v23,0(R1)         use v23 to test decoder
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003D98  E766 7000 0EA7                          2851+          VMO   V22,V22,V23,0      test instruction (dest is a source)
00003D9E  E760 5028 080E                00003D68  2852+          VST   V22,V1O76          save v1 output
00003DA4  07FB                                    2853+          BR    R11                return
00003DA8                                          2854+RE76      DC    0F                 xl16 expected result
00003DA8                                          2855+          DROP  R5
00003DA8  00000000 00000320                       2856           DC    XL16'0000000000000320 000A0708000D0003'   result
00003DB0  000A0708 000D0003
00003DB8  FF020304 05060750                       2857           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003DC0  090A0B78 0C0D0EFD
00003DC8  FF000000 0000000A                       2858           DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00003DD0  0101010F 010101FF
                                                  2859
                                                  2860 * Halfword
                                                  2861           VRR_C VMO,1
00003DD8                                          2862+          DS    0FD
00003DD8                        00003DD8          2863+          USING *,R5               base for test data and test routine
00003DD8  00003E18                                2864+T77       DC    A(X77)             address of test routine
00003DDC  004D                                    2865+          DC    H'77'              test number
00003DDE  00                                      2866+          DC    X'00'
00003DDF  01                                      2867+          DC    HL1'1'             m4
00003DE0  E5D4D640 40404040                       2868+          DC    CL8'VMO'           instruction name
00003DE8  00003E50                                2869+          DC    A(RE77+16)         address of v2 source
00003DEC  00003E60                                2870+          DC    A(RE77+32)         address of v3 source
00003DF0  00000010                                2871+          DC    A(16)              result length
00003DF4  00003E40                                2872+REA77     DC    A(RE77)            result address
00003DF8  00000000 00000000                       2873+          DS    FD                 gap
00003E00  00000000 00000000                       2874+V1O77     DS    XL16               V1 output
00003E08  00000000 00000000
00003E10  00000000 00000000                       2875+          DS    FD                 gap
                                                  2876+*
00003E18                                          2877+X77       DS    0F
00003E18  E310 5010 0014                00000010  2878+          LGF   R1,V2ADDR          load v2 source
00003E1E  E761 0000 0806                00000000  2879+          VL    v22,0(R1)          use v22 to test decoder
00003E24  E310 5014 0014                00000014  2880+          LGF   R1,V3ADDR          load v3 source
00003E2A  E771 0000 0806                00000000  2881+          VL    v23,0(R1)          use v23 to test decoder
00003E30  E766 7000 1EA7                          2882+          VMO   V22,V22,V23,1       test instruction (dest is a source)
00003E36  E760 5028 080E                00003E00  2883+          VST   V22,V1O77          save v1 output
00003E3C  07FB                                    2884+          BR    R11                return
00003E40                                          2885+RE77      DC    0F                 xl16 expected result
00003E40                                          2886+          DROP  R5
00003E40  00000000 00000271                       2887           DC    XL16'0000000000000271 000000000121CC24'   result
00003E48  00000000 0121CC24
00003E50  FFFF0000 00000019                       2888           DC    XL16'FFFF000000000019 003800001000EEFA'   v2
00003E58  00380000 1000EEFA
00003E60  FFFF0000 00000019                       2889           DC    XL16'FFFF000000000019 003800038000EEFA'   v3
00003E68  00380003 8000EEFA
                                                  2890
                                                  2891           VRR_C VMO,1
00003E70                                          2892+          DS    0FD
00003E70                        00003E70          2893+          USING *,R5               base for test data and test routine
00003E70  00003EB0                                2894+T78       DC    A(X78)             address of test routine
00003E74  004E                                    2895+          DC    H'78'              test number
00003E76  00                                      2896+          DC    X'00'
00003E77  01                                      2897+          DC    HL1'1'             m4
00003E78  E5D4D640 40404040                       2898+          DC    CL8'VMO'           instruction name
00003E80  00003EE8                                2899+          DC    A(RE78+16)         address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003E84  00003EF8                          2900+          DC    A(RE78+32)          address of v3 source
00003E88  00000010                          2901+          DC    A(16)               result length
00003E8C  00003ED8                          2902+REA78     DC    A(RE78)             result address
00003E90  00000000 00000000                 2903+          DS    FD                  gap
00003E98  00000000 00000000                 2904+V1O78     DS    XL16                V1 output
00003EA0  00000000 00000000
00003EA8  00000000 00000000                 2905+          DS    FD                  gap
                                            2906+*
00003EB0                                    2907+X78       DS    0F
00003EB0  E310 5010 0014              00000010  2908+      LGF   R1,V2ADDR           load v2 source
00003EB6  E761 0000 0806              00000000  2909+      VL    v22,0(R1)           use v22 to test decoder
00003EBC  E310 5014 0014              00000014  2910+      LGF   R1,V3ADDR           load v3 source
00003EC2  E771 0000 0806              00000000  2911+      VL    v23,0(R1)           use v23 to test decoder
00003EC8  E766 7000 1EA7                        2912+      VMO   V22,V22,V23,1        test instruction (dest is a source)
00003ECE  E760 5028 080E              00003E98  2913+      VST   V22,V1O78           save v1 output
00003ED4  07FB                                  2914+      BR    R11                 return
00003ED8                                    2915+RE78      DC    0F                  xl16 expected result
00003ED8                                    2916+          DROP  R5
00003ED8  00091810 00357900                 2917           DC    XL16'0009181000357900 0083884000EFA309'   result
00003EE0  00838840 00EFA309
00003EE8  FF020304 05060750                 2918           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003EF0  090A0B78 0C0D0EFD
00003EF8  FF020304 05060750                 2919           DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00003F00  090A0B78 0D0E0FFD
                                            2920
                                            2921           VRR_C VMO,1
00003F08                                    2922+          DS    0FD
00003F08                    00003F08        2923+          USING *,R5                base for test data and test routine
00003F08  00003F48                          2924+T79       DC    A(X79)              address of test routine
00003F0C  004F                              2925+          DC    H'79'               test number
00003F0E  00                                2926+          DC    X'00'
00003F0F  01                                2927+          DC    HL1'1'              m4
00003F10  E5D4D640 40404040                 2928+          DC    CL8'VMO'            instruction name
00003F18  00003F80                          2929+          DC    A(RE79+16)          address of v2 source
00003F1C  00003F90                          2930+          DC    A(RE79+32)          address of v3 source
00003F20  00000010                          2931+          DC    A(16)               result length
00003F24  00003F70                          2932+REA79     DC    A(RE79)             result address
00003F28  00000000 00000000                 2933+          DS    FD                  gap
00003F30  00000000 00000000                 2934+V1O79     DS    XL16                V1 output
00003F38  00000000 00000000
00003F40  00000000 00000000                 2935+          DS    FD                  gap
                                            2936+*
00003F48                                    2937+X79       DS    0F
00003F48  E310 5010 0014              00000010  2938+      LGF   R1,V2ADDR           load v2 source
00003F4E  E761 0000 0806              00000000  2939+      VL    v22,0(R1)           use v22 to test decoder
00003F54  E310 5014 0014              00000014  2940+      LGF   R1,V3ADDR           load v3 source
00003F5A  E771 0000 0806              00000000  2941+      VL    v23,0(R1)           use v23 to test decoder
00003F60  E766 7000 1EA7                        2942+      VMO   V22,V22,V23,1        test instruction (dest is a source)
00003F66  E760 5028 080E              00003F30  2943+      VST   V22,V1O79           save v1 output
00003F6C  07FB                                  2944+      BR    R11                 return
00003F70                                    2945+RE79      DC    0F                  xl16 expected result
00003F70                                    2946+          DROP  R5
00003F70  00030A08 00171480                 2947           DC    XL16'00030A0800171480 003C08200077CA06'   result
00003F78  003C0820 0077CA06
00003F80  FF020304 05060750                 2948           DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003F88  090A0B78 0C0D0EFD
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003F90  FF010102 02030328                        2949          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00003F98  0405053C 060707FE
                                                   2950
                                                   2951          VRR_C VMO,1
00003FA0                                           2952+         DS    0FD
00003FA0                      00003FA0             2953+         USING *,R5              base for test data and test routine
00003FA0  00003FE0                                 2954+T80      DC    A(X80)            address of test routine
00003FA4  0050                                     2955+         DC    H'80'             test number
00003FA6  00                                       2956+         DC    X'00'
00003FA7  01                                       2957+         DC    HL1'1'            m4
00003FA8  E5D4D640 40404040                        2958+         DC    CL8'VMO'          instruction name
00003FB0  00004018                                 2959+         DC    A(RE80+16)        address of v2 source
00003FB4  00004028                                 2960+         DC    A(RE80+32)        address of v3 source
00003FB8  00000010                                 2961+         DC    A(16)             result length
00003FBC  00004008                                 2962+REA80    DC    A(RE80)           result address
00003FC0  00000000 00000000                        2963+         DS    FD                gap
00003FC8  00000000 00000000                        2964+V1O80    DS    XL16              V1 output
00003FD0  00000000 00000000
00003FD8  00000000 00000000                        2965+         DS    FD                gap
                                                   2966+*
00003FE0                                           2967+X80      DS    0F
00003FE0  E310 5010 0014                00000010   2968+         LGF   R1,V2ADDR         load v2 source
00003FE6  E761 0000 0806                00000000   2969+         VL    v22,0(R1)         use v22 to test decoder
00003FEC  E310 5014 0014                00000014   2970+         LGF   R1,V3ADDR         load v3 source
00003FF2  E771 0000 0806                00000000   2971+         VL    v23,0(R1)         use v23 to test decoder
00003FF8  E766 7000 1EA7                           2972+         VMO   V22,V22,V23,1      test instruction (dest is a source)
00003FFE  E760 5028 080E                00003FC8   2973+         VST   V22,V1O80          save v1 output
00004004  07FB                                     2974+         BR    R11               return
00004008                                           2975+RE80     DC    0F                xl16 expected result
00004008                                           2976+         DROP  R5
00004008  00000000 00004920                        2977          DC    XL16'0000000000004920 000C2408001DEB03'   result
00004010  000C2408 001DEB03
00004018  FF020304 05060750                        2978          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00004020  090A0B78 0C0D0EFD
00004028  FF000000 0000000A                        2979          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00004030  0101010F 010101FF
                                                   2980
                                                   2981 * Word
                                                   2982          VRR_C VMO,2
00004038                                           2983+         DS    0FD
00004038                      00004038             2984+         USING *,R5              base for test data and test routine
00004038  00004078                                 2985+T81      DC    A(X81)            address of test routine
0000403C  0051                                     2986+         DC    H'81'             test number
0000403E  00                                       2987+         DC    X'00'
0000403F  02                                       2988+         DC    HL1'2'            m4
00004040  E5D4D640 40404040                        2989+         DC    CL8'VMO'          instruction name
00004048  000040B0                                 2990+         DC    A(RE81+16)        address of v2 source
0000404C  000040C0                                 2991+         DC    A(RE81+32)        address of v3 source
00004050  00000010                                 2992+         DC    A(16)             result length
00004054  000040A0                                 2993+REA81    DC    A(RE81)           result address
00004058  00000000 00000000                        2994+         DS    FD                gap
00004060  00000000 00000000                        2995+V1O81    DS    XL16              V1 output
00004068  00000000 00000000
00004070  00000000 00000000                        2996+         DS    FD                gap
                                                   2997+*
00004078                                           2998+X81      DS    0F
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004078  E310 5010 0014                 00000010  2999+          LGF   R1,V2ADDR          load v2 source
0000407E  E761 0000 0806                 00000000  3000+          VL    v22,0(R1)          use v22 to test decoder
00004084  E310 5014 0014                 00000014  3001+          LGF   R1,V3ADDR          load v3 source
0000408A  E771 0000 0806                 00000000  3002+          VL    v23,0(R1)          use v23 to test decoder
00004090  E766 7000 2EA7                           3003+          VMO   V22,V22,V23,2       test instruction (dest is a source)
00004096  E760 5028 080E                 00004060  3004+          VST   V22,V1O81           save v1 output
0000409C  07FB                                     3005+          BR    R11                return
000040A0                                           3006+RE81      DC    0F                 xl16 expected result
000040A0                                           3007+          DROP  R5
000040A0  00000002 71000000                        3008           DC    XL16'0000000271000000 FF0123454FEDCC24'   result
000040A8  FF012345 4FEDCC24
000040B0  FFFFFFFF 00019000                        3009           DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
000040B8  00000038 EEEEEEFA
000040C0  FFFFFFFF 00019000                        3010           DC    XL16'FFFFFFFF00019000 000000380EEEEFA'   v3
000040C8  00000038 0EEEEEFA
                                                   3011
                                                   3012           VRR_C VMO,2
000040D0                                           3013+          DS    0FD
000040D0                         000040D0          3014+          USING *,R5               base for test data and test routine
000040D0  00004110                                 3015+T82       DC    A(X82)             address of test routine
000040D4  0052                                     3016+          DC    H'82'              test number
000040D6  00                                       3017+          DC    X'00'
000040D7  02                                       3018+          DC    HL1'2'             m4
000040D8  E5D4D640 40404040                        3019+          DC    CL8'VMO'           instruction name
000040E0  00004148                                 3020+          DC    A(RE82+16)         address of v2 source
000040E4  00004158                                 3021+          DC    A(RE82+32)         address of v3 source
000040E8  00000010                                 3022+          DC    A(16)              result length
000040EC  00004138                                 3023+REA82     DC    A(RE82)            result address
000040F0  00000000 00000000                        3024+          DS    FD                 gap
000040F8  00000000 00000000                        3025+V1O82     DS    XL16               V1 output
00004100  00000000 00000000
00004108  00000000 00000000                        3026+          DS    FD                 gap
                                                   3027+*
00004110                                           3028+X82       DS    0F
00004110  E310 5010 0014                 00000010  3029+          LGF   R1,V2ADDR          load v2 source
00004116  E761 0000 0806                 00000000  3030+          VL    v22,0(R1)          use v22 to test decoder
0000411C  E310 5014 0014                 00000014  3031+          LGF   R1,V3ADDR          load v3 source
00004122  E771 0000 0806                 00000000  3032+          VL    v23,0(R1)          use v23 to test decoder
00004128  E766 7000 2EA7                           3033+          VMO   V22,V22,V23,2       test instruction (dest is a source)
0000412E  E760 5028 080E                 000040F8  3034+          VST   V22,V1O82           save v1 output
00004134  07FB                                     3035+          BR    R11                return
00004138                                           3036+RE82      DC    0F                 xl16 expected result
00004138                                           3037+          DROP  R5
00004138  00193C6D 77F57900                        3038           DC    XL16'00193C6D77F57900 00AA6E5898D42101'   result
00004140  00AA6E58 98D42101
00004148  FF020304 05060750                        3039           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004150  090A0B0C 0D0E0F7F
00004158  FF020304 05060750                        3040           DC    XL16'FF02030405060750 090A0B780D0E0F7F'   v3
00004160  090A0B78 0D0E0F7F
                                                   3041
                                                   3042           VRR_C VMO,2
00004168                                           3043+          DS    0FD
00004168                         00004168          3044+          USING *,R5               base for test data and test routine
00004168  000041A8                                 3045+T83       DC    A(X83)             address of test routine
0000416C  0053                                     3046+          DC    H'83'              test number
0000416E  00                                       3047+          DC    X'00'
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000416F  02                                       3048+         DC    HL1'2'              m4
00004170  E5D4D640 40404040                        3049+         DC    CL8'VMO'            instruction name
00004178  000041E0                                 3050+         DC    A(RE83+16)          address of v2 source
0000417C  000041F0                                 3051+         DC    A(RE83+32)          address of v3 source
00004180  00000010                                 3052+         DC    A(16)               result length
00004184  000041D0                                 3053+REA83    DC    A(RE83)             result address
00004188  00000000 00000000                        3054+         DS    FD                  gap
00004190  00000000 00000000                        3055+V1O83    DS    XL16                V1 output
00004198  00000000 00000000
000041A0  00000000 00000000                        3056+         DS    FD                  gap
                                                   3057+*
000041A8                                           3058+X83      DS    0F
000041A8  E310 5010 0014                 00000010  3059+         LGF   R1,V2ADDR           load v2 source
000041AE  E761 0000 0806                 00000000  3060+         VL    v22,0(R1)           use v22 to test decoder
000041B4  E310 5014 0014                 00000014  3061+         LGF   R1,V3ADDR           load v3 source
000041BA  E771 0000 0806                 00000000  3062+         VL    v23,0(R1)           use v23 to test decoder
000041C0  E766 7000 2EA7                           3063+         VMO   V22,V22,V23,2        test instruction (dest is a source)
000041C6  E760 5028 080E                 00004190  3064+         VST   V22,V1O83           save v1 output
000041CC  07FB                                     3065+         BR    R11                 return
000041D0                                           3066+RE83     DC    0F                  xl16 expected result
000041D0                                           3067+         DROP  R5
000041D0  000A1B30 90F71480                        3068          DC    XL16'000A1B3090F71480 004EB01DFF5B4941'   result
000041D8  004EB01D FF5B4941
000041E0  FF020304 05060750                        3069          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000041E8  090A0B0C 0D0E0F7F
000041F0  FF010102 02030328                        3070          DC    XL16'FF01010202030328 0405053C0607073F'   v3
000041F8  0405053C 0607073F
                                                   3071
                                                   3072          VRR_C VMO,2
00004200                                           3073+         DS    0FD
00004200                      00004200             3074+         USING *,R5                base for test data and test routine
00004200  00004240                                 3075+T84      DC    A(X84)              address of test routine
00004204  0054                                     3076+         DC    H'84'               test number
00004206  00                                       3077+         DC    X'00'
00004207  02                                       3078+         DC    HL1'2'              m4
00004208  E5D4D640 40404040                        3079+         DC    CL8'VMO'            instruction name
00004210  00004278                                 3080+         DC    A(RE84+16)          address of v2 source
00004214  00004288                                 3081+         DC    A(RE84+32)          address of v3 source
00004218  00000010                                 3082+         DC    A(16)               result length
0000421C  00004268                                 3083+REA84    DC    A(RE84)             result address
00004220  00000000 00000000                        3084+         DS    FD                  gap
00004228  00000000 00000000                        3085+V1O84    DS    XL16                V1 output
00004230  00000000 00000000
00004238  00000000 00000000                        3086+         DS    FD                  gap
                                                   3087+*
00004240                                           3088+X84      DS    0F
00004240  E310 5010 0014                 00000010  3089+         LGF   R1,V2ADDR           load v2 source
00004246  E761 0000 0806                 00000000  3090+         VL    v22,0(R1)           use v22 to test decoder
0000424C  E310 5014 0014                 00000014  3091+         LGF   R1,V3ADDR           load v3 source
00004252  E771 0000 0806                 00000000  3092+         VL    v23,0(R1)           use v23 to test decoder
00004258  E766 7000 2EA7                           3093+         VMO   V22,V22,V23,2        test instruction (dest is a source)
0000425E  E760 5028 080E                 00004228  3094+         VST   V22,V1O84           save v1 output
00004264  07FB                                     3095+         BR    R11                 return
00004268                                           3096+RE84     DC    0F                  xl16 expected result
00004268                                           3097+         DROP  R5
00004268  00000000 323C4920                        3098          DC    XL16'00000000323C4920 000D1B2B60616771'   result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004270  000D1B2B 60616771
00004278  FF020304 05060750                        3099           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004280  090A0B0C 0D0E0F7F
00004288  FF000000 0000000A                        3100           DC    XL16'FF0000000000000A 0101010F0101010F'   v3
00004290  0101010F 0101010F
                                                   3101
                                                   3102
00004298  00000000                                 3103           DC    F'0'     END OF TABLE
0000429C  00000000                                 3104           DC    F'0'
                                                   3105 *
                                                   3106 * table of pointers to individual load test
                                                   3107 *
000042A0                                           3108 E7TESTS   DS    0F
                                                   3109           PTTABLE
000042A0                                           3110+TTABLE    DS    0F
000042A0  000010B8                                 3111+          DC    A(T1)
000042A4  00001150                                 3112+          DC    A(T2)
000042A8  000011E8                                 3113+          DC    A(T3)
000042AC  00001280                                 3114+          DC    A(T4)
000042B0  00001318                                 3115+          DC    A(T5)
000042B4  000013B0                                 3116+          DC    A(T6)
000042B8  00001448                                 3117+          DC    A(T7)
000042BC  000014E0                                 3118+          DC    A(T8)
000042C0  00001578                                 3119+          DC    A(T9)
000042C4  00001610                                 3120+          DC    A(T10)
000042C8  000016A8                                 3121+          DC    A(T11)
000042CC  00001740                                 3122+          DC    A(T12)
000042D0  000017D8                                 3123+          DC    A(T13)
000042D4  00001870                                 3124+          DC    A(T14)
000042D8  00001908                                 3125+          DC    A(T15)
000042DC  000019A0                                 3126+          DC    A(T16)
000042E0  00001A38                                 3127+          DC    A(T17)
000042E4  00001AD0                                 3128+          DC    A(T18)
000042E8  00001B68                                 3129+          DC    A(T19)
000042EC  00001C00                                 3130+          DC    A(T20)
000042F0  00001C98                                 3131+          DC    A(T21)
000042F4  00001D30                                 3132+          DC    A(T22)
000042F8  00001DC8                                 3133+          DC    A(T23)
000042FC  00001E60                                 3134+          DC    A(T24)
00004300  00001EF8                                 3135+          DC    A(T25)
00004304  00001F90                                 3136+          DC    A(T26)
00004308  00002028                                 3137+          DC    A(T27)
0000430C  000020C0                                 3138+          DC    A(T28)
00004310  00002158                                 3139+          DC    A(T29)
00004314  000021F0                                 3140+          DC    A(T30)
00004318  00002288                                 3141+          DC    A(T31)
0000431C  00002320                                 3142+          DC    A(T32)
00004320  000023B8                                 3143+          DC    A(T33)
00004324  00002450                                 3144+          DC    A(T34)
00004328  000024E8                                 3145+          DC    A(T35)
0000432C  00002580                                 3146+          DC    A(T36)
00004330  00002618                                 3147+          DC    A(T37)
00004334  000026B0                                 3148+          DC    A(T38)
00004338  00002748                                 3149+          DC    A(T39)
0000433C  000027E0                                 3150+          DC    A(T40)
00004340  00002878                                 3151+          DC    A(T41)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004344  00002910                          3152+          DC    A(T42)
00004348  000029A8                          3153+          DC    A(T43)
0000434C  00002A40                          3154+          DC    A(T44)
00004350  00002AD8                          3155+          DC    A(T45)
00004354  00002B70                          3156+          DC    A(T46)
00004358  00002C08                          3157+          DC    A(T47)
0000435C  00002CA0                          3158+          DC    A(T48)
00004360  00002D38                          3159+          DC    A(T49)
00004364  00002DD0                          3160+          DC    A(T50)
00004368  00002E68                          3161+          DC    A(T51)
0000436C  00002F00                          3162+          DC    A(T52)
00004370  00002F98                          3163+          DC    A(T53)
00004374  00003030                          3164+          DC    A(T54)
00004378  000030C8                          3165+          DC    A(T55)
0000437C  00003160                          3166+          DC    A(T56)
00004380  000031F8                          3167+          DC    A(T57)
00004384  00003290                          3168+          DC    A(T58)
00004388  00003328                          3169+          DC    A(T59)
0000438C  000033C0                          3170+          DC    A(T60)
00004390  00003458                          3171+          DC    A(T61)
00004394  000034F0                          3172+          DC    A(T62)
00004398  00003588                          3173+          DC    A(T63)
0000439C  00003620                          3174+          DC    A(T64)
000043A0  000036B8                          3175+          DC    A(T65)
000043A4  00003750                          3176+          DC    A(T66)
000043A8  000037E8                          3177+          DC    A(T67)
000043AC  00003880                          3178+          DC    A(T68)
000043B0  00003918                          3179+          DC    A(T69)
000043B4  000039B0                          3180+          DC    A(T70)
000043B8  00003A48                          3181+          DC    A(T71)
000043BC  00003AE0                          3182+          DC    A(T72)
000043C0  00003B78                          3183+          DC    A(T73)
000043C4  00003C10                          3184+          DC    A(T74)
000043C8  00003CA8                          3185+          DC    A(T75)
000043CC  00003D40                          3186+          DC    A(T76)
000043D0  00003DD8                          3187+          DC    A(T77)
000043D4  00003E70                          3188+          DC    A(T78)
000043D8  00003F08                          3189+          DC    A(T79)
000043DC  00003FA0                          3190+          DC    A(T80)
000043E0  00004038                          3191+          DC    A(T81)
000043E4  000040D0                          3192+          DC    A(T82)
000043E8  00004168                          3193+          DC    A(T83)
000043EC  00004200                          3194+          DC    A(T84)
                                            3195+*
000043F0  00000000                          3196+          DC    A(0)              END OF TABLE
000043F4  00000000                          3197+          DC    A(0)
                                            3198
000043F8  00000000                          3199           DC    F'0'      END OF TABLE
000043FC  00000000                          3200           DC    F'0'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                          3202 ********************************************************************************
                                          3203 *        Register equates
                                          3204 ********************************************************************************


                             00000000  00000001  3206 R0       EQU   0
                             00000001  00000001  3207 R1       EQU   1
                             00000002  00000001  3208 R2       EQU   2
                             00000003  00000001  3209 R3       EQU   3
                             00000004  00000001  3210 R4       EQU   4
                             00000005  00000001  3211 R5       EQU   5
                             00000006  00000001  3212 R6       EQU   6
                             00000007  00000001  3213 R7       EQU   7
                             00000008  00000001  3214 R8       EQU   8
                             00000009  00000001  3215 R9       EQU   9
                             0000000A  00000001  3216 R10      EQU   10
                             0000000B  00000001  3217 R11      EQU   11
                             0000000C  00000001  3218 R12      EQU   12
                             0000000D  00000001  3219 R13      EQU   13
                             0000000E  00000001  3220 R14      EQU   14
                             0000000F  00000001  3221 R15      EQU   15


                                          3223 ********************************************************************************
                                          3224 *        Register equates
                                          3225 ********************************************************************************


                             00000000  00000001  3227 V0       EQU   0
                             00000001  00000001  3228 V1       EQU   1
                             00000002  00000001  3229 V2       EQU   2
                             00000003  00000001  3230 V3       EQU   3
                             00000004  00000001  3231 V4       EQU   4
                             00000005  00000001  3232 V5       EQU   5
                             00000006  00000001  3233 V6       EQU   6
                             00000007  00000001  3234 V7       EQU   7
                             00000008  00000001  3235 V8       EQU   8
                             00000009  00000001  3236 V9       EQU   9
                             0000000A  00000001  3237 V10      EQU   10
                             0000000B  00000001  3238 V11      EQU   11
                             0000000C  00000001  3239 V12      EQU   12
                             0000000D  00000001  3240 V13      EQU   13
                             0000000E  00000001  3241 V14      EQU   14
                             0000000F  00000001  3242 V15      EQU   15
                             00000010  00000001  3243 V16      EQU   16
                             00000011  00000001  3244 V17      EQU   17
                             00000012  00000001  3245 V18      EQU   18
                             00000013  00000001  3246 V19      EQU   19
                             00000014  00000001  3247 V20      EQU   20
                             00000015  00000001  3248 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001  3249 V22       EQU   22
                                00000017  00000001  3250 V23       EQU   23
                                00000018  00000001  3251 V24       EQU   24
                                00000019  00000001  3252 V25       EQU   25
                                0000001A  00000001  3253 V26       EQU   26
                                0000001B  00000001  3254 V27       EQU   27
                                0000001C  00000001  3255 V28       EQU   28
                                0000001D  00000001  3256 V29       EQU   29
                                0000001E  00000001  3257 V30       EQU   30
                                0000001F  00000001  3258 V31       EQU   31
                                                    3259
                                                    3260           END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	164	130 160 161 162
CTLR0	F	0000048C	4	360	174 175 176 177
DECNUM	C	00001073	16	411	274 276 282 284
E7TEST	4	00000000	64	425	223
E7TESTS	F	000042A0	4	3108	216
EDIT	X	00001047	18	406	275 283
ENDTEST	U	0000031E	1	260	221
EOJ	I	00000470	4	350	209 263
EOJPSW	D	00000460	8	348	350
FAILCONT	U	0000030E	1	250	
FAILED	F	00001000	4	388	252 261
FAILMSG	U	0000030A	1	244	234
FAILPSW	D	00000478	8	352	354
FAILTEST	I	00000488	4	354	264
FB0001	F	00000280	8	193	197 198 200
IMAGE	1	00000000	17408	0	
K	U	00000400	1	372	373 374 375
K64	U	00010000	1	374	
M4	U	00000007	1	429	281
MB	U	00100000	1	375	
MSG	I	000003A8	4	310	208 293
MSGCMD	C	000003F6	9	340	323 324
MSGMSG	C	000003FF	95	341	317 338 315
MSGMVC	I	000003F0	6	338	321
MSGOK	I	000003BE	2	319	316
MSGRET	I	000003DE	4	334	327 330
MSGSAVE	F	000003E4	4	337	313 334
NEXTE7	U	000002D4	1	218	237 255
OPNAME	C	00000008	8	431	279
PAGE	U	00001000	1	373	
PRT3	C	0000105D	18	409	275 276 277 283 284 285
PRTLINE	C	00001008	16	394	401 292
PRTLNG	U	0000003F	1	401	291
PRTM4	C	00001044	2	399	285
PRTNAME	C	00001033	8	397	279
PRTNUM	C	00001018	3	395	277
R0	U	00000000	1	3206	124 174 177 197 199 200 201 206 225 226 251 252 290
					291 294 310 313 315 317 319 334
R1	U	00000001	1	3207	207 232 233 261 262 292 324 338 559 560 561 562 589
					590 591 592 619 620 621 622 649 650 651 652 681 682
					683 684 711 712 713 714 741 742 743 744 771 772 773
					774 802 803 804 805 832 833 834 835 862 863 864 865
					892 893 894 895 926 927 928 929 956 957 958 959 986
					987 988 989 1016 1017 1018 1019 1047 1048 1049 1050 1077 1078
					1079 1080 1107 1108 1109 1110 1137 1138 1139 1140 1168 1169 1170
					1171 1198 1199 1200 1201 1228 1229 1230 1231 1258 1259 1260 1261
					1292 1293 1294 1295 1322 1323 1324 1325 1352 1353 1354 1355 1382
					1383 1384 1385 1413 1414 1415 1416 1443 1444 1445 1446 1473 1474
					1475 1476 1503 1504 1505 1506 1534 1535 1536 1537 1564 1565 1566
					1567 1594 1595 1596 1597 1624 1625 1626 1627 1659 1660 1661 1662
					1689 1690 1691 1692 1719 1720 1721 1722 1749 1750 1751 1752 1780
					1781 1782 1783 1810 1811 1812 1813 1840 1841 1842 1843 1870 1871
					1872 1873 1901 1902 1903 1904 1931 1932 1933 1934 1961 1962 1963
					1964 1991 1992 1993 1994 2025 2026 2027 2028 2055 2056 2057 2058
					2085 2086 2087 2088 2115 2116 2117 2118 2146 2147 2148 2149 2176
					2177 2178 2179 2206 2207 2208 2209 2236 2237 2238 2239 2267 2268

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					2269 2270 2297 2298 2299 2300 2327 2328 2329 2330 2357 2358 2359
					2360 2391 2392 2393 2394 2421 2422 2423 2424 2451 2452 2453 2454
					2481 2482 2483 2484 2512 2513 2514 2515 2542 2543 2544 2545 2572
					2573 2574 2575 2602 2603 2604 2605 2633 2634 2635 2636 2663 2664
					2665 2666 2693 2694 2695 2696 2723 2724 2725 2726 2757 2758 2759
					2760 2787 2788 2789 2790 2817 2818 2819 2820 2847 2848 2849 2850
					2878 2879 2880 2881 2908 2909 2910 2911 2938 2939 2940 2941 2968
					2969 2970 2971 2999 3000 3001 3002 3029 3030 3031 3032 3059 3060
					3061 3062 3089 3090 3091 3092
R10	U	0000000A	1	3216	162 171 172
R11	U	0000000B	1	3217	229 230 565 595 625 655 687 717 747 777 808 838 868
					898 932 962 992 1022 1053 1083 1113 1143 1174 1204 1234 1264
					1298 1328 1358 1388 1419 1449 1479 1509 1540 1570 1600 1630 1665
					1695 1725 1755 1786 1816 1846 1876 1907 1937 1967 1997 2031 2061
					2091 2121 2152 2182 2212 2242 2273 2303 2333 2363 2397 2427 2457
					2487 2518 2548 2578 2608 2639 2669 2699 2729 2763 2793 2823 2853
					2884 2914 2944 2974 3005 3035 3065 3095
R12	U	0000000C	1	3218	216 219 236 254
R13	U	0000000D	1	3219	
R14	U	0000000E	1	3220	
R15	U	0000000F	1	3221	245 270 297 298
R2	U	00000002	1	3208	208 273 274 281 282 290 293 294 311 313 319 320 321
					323 329 334 335
R3	U	00000003	1	3209	
R4	U	00000004	1	3210	
R5	U	00000005	1	3211	219 220 223 271 296 544 567 574 597 604 627 634 657
					666 689 696 719 726 749 756 779 787 810 817 840 847
					870 877 900 911 934 941 964 971 994 1001 1024 1032 1055
					1062 1085 1092 1115 1122 1145 1153 1176 1183 1206 1213 1236 1243
					1266 1277 1300 1307 1330 1337 1360 1367 1390 1398 1421 1428 1451
					1458 1481 1488 1511 1519 1542 1549 1572 1579 1602 1609 1632 1644
					1667 1674 1697 1704 1727 1734 1757 1765 1788 1795 1818 1825 1848
					1855 1878 1886 1909 1916 1939 1946 1969 1976 1999 2010 2033 2040
					2063 2070 2093 2100 2123 2131 2154 2161 2184 2191 2214 2221 2244
					2252 2275 2282 2305 2312 2335 2342 2365 2376 2399 2406 2429 2436
					2459 2466 2489 2497 2520 2527 2550 2557 2580 2587 2610 2618 2641
					2648 2671 2678 2701 2708 2731 2742 2765 2772 2795 2802 2825 2832
					2855 2863 2886 2893 2916 2923 2946 2953 2976 2984 3007 3014 3037
					3044 3067 3074 3097
R6	U	00000006	1	3212	
R7	U	00000007	1	3213	
R8	U	00000008	1	3214	160 164 165 166 168
R9	U	00000009	1	3215	161 168 169 171
RE1	F	00001120	4	566	550 551 553
RE10	F	00001678	4	839	823 824 826
RE11	F	00001710	4	869	853 854 856
RE12	F	000017A8	4	899	883 884 886
RE13	F	00001840	4	933	917 918 920
RE14	F	000018D8	4	963	947 948 950
RE15	F	00001970	4	993	977 978 980
RE16	F	00001A08	4	1023	1007 1008 1010
RE17	F	00001AA0	4	1054	1038 1039 1041
RE18	F	00001B38	4	1084	1068 1069 1071
RE19	F	00001BD0	4	1114	1098 1099 1101
RE2	F	000011B8	4	596	580 581 583
RE20	F	00001C68	4	1144	1128 1129 1131

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
RE21	F	00001D00	4	1175	1159	1160	1162
RE22	F	00001D98	4	1205	1189	1190	1192
RE23	F	00001E30	4	1235	1219	1220	1222
RE24	F	00001EC8	4	1265	1249	1250	1252
RE25	F	00001F60	4	1299	1283	1284	1286
RE26	F	00001FF8	4	1329	1313	1314	1316
RE27	F	00002090	4	1359	1343	1344	1346
RE28	F	00002128	4	1389	1373	1374	1376
RE29	F	000021C0	4	1420	1404	1405	1407
RE3	F	00001250	4	626	610	611	613
RE30	F	00002258	4	1450	1434	1435	1437
RE31	F	000022F0	4	1480	1464	1465	1467
RE32	F	00002388	4	1510	1494	1495	1497
RE33	F	00002420	4	1541	1525	1526	1528
RE34	F	000024B8	4	1571	1555	1556	1558
RE35	F	00002550	4	1601	1585	1586	1588
RE36	F	000025E8	4	1631	1615	1616	1618
RE37	F	00002680	4	1666	1650	1651	1653
RE38	F	00002718	4	1696	1680	1681	1683
RE39	F	000027B0	4	1726	1710	1711	1713
RE4	F	000012E8	4	656	640	641	643
RE40	F	00002848	4	1756	1740	1741	1743
RE41	F	000028E0	4	1787	1771	1772	1774
RE42	F	00002978	4	1817	1801	1802	1804
RE43	F	00002A10	4	1847	1831	1832	1834
RE44	F	00002AA8	4	1877	1861	1862	1864
RE45	F	00002B40	4	1908	1892	1893	1895
RE46	F	00002BD8	4	1938	1922	1923	1925
RE47	F	00002C70	4	1968	1952	1953	1955
RE48	F	00002D08	4	1998	1982	1983	1985
RE49	F	00002DA0	4	2032	2016	2017	2019
RE5	F	00001380	4	688	672	673	675
RE50	F	00002E38	4	2062	2046	2047	2049
RE51	F	00002ED0	4	2092	2076	2077	2079
RE52	F	00002F68	4	2122	2106	2107	2109
RE53	F	00003000	4	2153	2137	2138	2140
RE54	F	00003098	4	2183	2167	2168	2170
RE55	F	00003130	4	2213	2197	2198	2200
RE56	F	000031C8	4	2243	2227	2228	2230
RE57	F	00003260	4	2274	2258	2259	2261
RE58	F	000032F8	4	2304	2288	2289	2291
RE59	F	00003390	4	2334	2318	2319	2321
RE6	F	00001418	4	718	702	703	705
RE60	F	00003428	4	2364	2348	2349	2351
RE61	F	000034C0	4	2398	2382	2383	2385
RE62	F	00003558	4	2428	2412	2413	2415
RE63	F	000035F0	4	2458	2442	2443	2445
RE64	F	00003688	4	2488	2472	2473	2475
RE65	F	00003720	4	2519	2503	2504	2506
RE66	F	000037B8	4	2549	2533	2534	2536
RE67	F	00003850	4	2579	2563	2564	2566
RE68	F	000038E8	4	2609	2593	2594	2596
RE69	F	00003980	4	2640	2624	2625	2627
RE7	F	000014B0	4	748	732	733	735
RE70	F	00003A18	4	2670	2654	2655	2657
RE71	F	00003AB0	4	2700	2684	2685	2687

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE72	F	00003B48	4	2730	2714 2715 2717
RE73	F	00003BE0	4	2764	2748 2749 2751
RE74	F	00003C78	4	2794	2778 2779 2781
RE75	F	00003D10	4	2824	2808 2809 2811
RE76	F	00003DA8	4	2854	2838 2839 2841
RE77	F	00003E40	4	2885	2869 2870 2872
RE78	F	00003ED8	4	2915	2899 2900 2902
RE79	F	00003F70	4	2945	2929 2930 2932
RE8	F	00001548	4	778	762 763 765
RE80	F	00004008	4	2975	2959 2960 2962
RE81	F	000040A0	4	3006	2990 2991 2993
RE82	F	00004138	4	3036	3020 3021 3023
RE83	F	000041D0	4	3066	3050 3051 3053
RE84	F	00004268	4	3096	3080 3081 3083
RE9	F	000015E0	4	809	793 794 796
REA1	A	000010D4	4	553	
REA10	A	0000162C	4	826	
REA11	A	000016C4	4	856	
REA12	A	0000175C	4	886	
REA13	A	000017F4	4	920	
REA14	A	0000188C	4	950	
REA15	A	00001924	4	980	
REA16	A	000019BC	4	1010	
REA17	A	00001A54	4	1041	
REA18	A	00001AEC	4	1071	
REA19	A	00001B84	4	1101	
REA2	A	0000116C	4	583	
REA20	A	00001C1C	4	1131	
REA21	A	00001CB4	4	1162	
REA22	A	00001D4C	4	1192	
REA23	A	00001DE4	4	1222	
REA24	A	00001E7C	4	1252	
REA25	A	00001F14	4	1286	
REA26	A	00001FAC	4	1316	
REA27	A	00002044	4	1346	
REA28	A	000020DC	4	1376	
REA29	A	00002174	4	1407	
REA3	A	00001204	4	613	
REA30	A	0000220C	4	1437	
REA31	A	000022A4	4	1467	
REA32	A	0000233C	4	1497	
REA33	A	000023D4	4	1528	
REA34	A	0000246C	4	1558	
REA35	A	00002504	4	1588	
REA36	A	0000259C	4	1618	
REA37	A	00002634	4	1653	
REA38	A	000026CC	4	1683	
REA39	A	00002764	4	1713	
REA4	A	0000129C	4	643	
REA40	A	000027FC	4	1743	
REA41	A	00002894	4	1774	
REA42	A	0000292C	4	1804	
REA43	A	000029C4	4	1834	
REA44	A	00002A5C	4	1864	
REA45	A	00002AF4	4	1895	
REA46	A	00002B8C	4	1925	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA47	A	00002C24	4	1955	
REA48	A	00002CBC	4	1985	
REA49	A	00002D54	4	2019	
REA5	A	00001334	4	675	
REA50	A	00002DEC	4	2049	
REA51	A	00002E84	4	2079	
REA52	A	00002F1C	4	2109	
REA53	A	00002FB4	4	2140	
REA54	A	0000304C	4	2170	
REA55	A	000030E4	4	2200	
REA56	A	0000317C	4	2230	
REA57	A	00003214	4	2261	
REA58	A	000032AC	4	2291	
REA59	A	00003344	4	2321	
REA6	A	000013CC	4	705	
REA60	A	000033DC	4	2351	
REA61	A	00003474	4	2385	
REA62	A	0000350C	4	2415	
REA63	A	000035A4	4	2445	
REA64	A	0000363C	4	2475	
REA65	A	000036D4	4	2506	
REA66	A	0000376C	4	2536	
REA67	A	00003804	4	2566	
REA68	A	0000389C	4	2596	
REA69	A	00003934	4	2627	
REA7	A	00001464	4	735	
REA70	A	000039CC	4	2657	
REA71	A	00003A64	4	2687	
REA72	A	00003AFC	4	2717	
REA73	A	00003B94	4	2751	
REA74	A	00003C2C	4	2781	
REA75	A	00003CC4	4	2811	
REA76	A	00003D5C	4	2841	
REA77	A	00003DF4	4	2872	
REA78	A	00003E8C	4	2902	
REA79	A	00003F24	4	2932	
REA8	A	000014FC	4	765	
REA80	A	00003FBC	4	2962	
REA81	A	00004054	4	2993	
REA82	A	000040EC	4	3023	
REA83	A	00004184	4	3053	
REA84	A	0000421C	4	3083	
REA9	A	00001594	4	796	
READDR	A	0000001C	4	435	232
REG2LOW	U	000000DD	1	378	
REG2PATT	U	AABBCCDD	1	377	
RELEN	A	00000018	4	434	
RPTDWSAV	D	00000398	8	303	290 294
RPTERROR	I	0000032C	4	270	245
RPTSAVE	F	00000390	4	300	270 297
RPTSVR5	F	00000394	4	301	271 296
SKL0001	U	0000004E	1	190	206
SKT0001	C	0000022A	20	187	190 207
SVOLDPSW	U	00000140	0	126	
T1	A	000010B8	4	545	3111
T10	A	00001610	4	818	3120

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T11	A	000016A8	4	848	3121
T12	A	00001740	4	878	3122
T13	A	000017D8	4	912	3123
T14	A	00001870	4	942	3124
T15	A	00001908	4	972	3125
T16	A	000019A0	4	1002	3126
T17	A	00001A38	4	1033	3127
T18	A	00001AD0	4	1063	3128
T19	A	00001B68	4	1093	3129
T2	A	00001150	4	575	3112
T20	A	00001C00	4	1123	3130
T21	A	00001C98	4	1154	3131
T22	A	00001D30	4	1184	3132
T23	A	00001DC8	4	1214	3133
T24	A	00001E60	4	1244	3134
T25	A	00001EF8	4	1278	3135
T26	A	00001F90	4	1308	3136
T27	A	00002028	4	1338	3137
T28	A	000020C0	4	1368	3138
T29	A	00002158	4	1399	3139
T3	A	000011E8	4	605	3113
T30	A	000021F0	4	1429	3140
T31	A	00002288	4	1459	3141
T32	A	00002320	4	1489	3142
T33	A	000023B8	4	1520	3143
T34	A	00002450	4	1550	3144
T35	A	000024E8	4	1580	3145
T36	A	00002580	4	1610	3146
T37	A	00002618	4	1645	3147
T38	A	000026B0	4	1675	3148
T39	A	00002748	4	1705	3149
T4	A	00001280	4	635	3114
T40	A	000027E0	4	1735	3150
T41	A	00002878	4	1766	3151
T42	A	00002910	4	1796	3152
T43	A	000029A8	4	1826	3153
T44	A	00002A40	4	1856	3154
T45	A	00002AD8	4	1887	3155
T46	A	00002B70	4	1917	3156
T47	A	00002C08	4	1947	3157
T48	A	00002CA0	4	1977	3158
T49	A	00002D38	4	2011	3159
T5	A	00001318	4	667	3115
T50	A	00002DD0	4	2041	3160
T51	A	00002E68	4	2071	3161
T52	A	00002F00	4	2101	3162
T53	A	00002F98	4	2132	3163
T54	A	00003030	4	2162	3164
T55	A	000030C8	4	2192	3165
T56	A	00003160	4	2222	3166
T57	A	000031F8	4	2253	3167
T58	A	00003290	4	2283	3168
T59	A	00003328	4	2313	3169
T6	A	000013B0	4	697	3116
T60	A	000033C0	4	2343	3170
T61	A	00003458	4	2377	3171

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T62	A	000034F0	4	2407	3172
T63	A	00003588	4	2437	3173
T64	A	00003620	4	2467	3174
T65	A	000036B8	4	2498	3175
T66	A	00003750	4	2528	3176
T67	A	000037E8	4	2558	3177
T68	A	00003880	4	2588	3178
T69	A	00003918	4	2619	3179
T7	A	00001448	4	727	3117
T70	A	000039B0	4	2649	3180
T71	A	00003A48	4	2679	3181
T72	A	00003AE0	4	2709	3182
T73	A	00003B78	4	2743	3183
T74	A	00003C10	4	2773	3184
T75	A	00003CA8	4	2803	3185
T76	A	00003D40	4	2833	3186
T77	A	00003DD8	4	2864	3187
T78	A	00003E70	4	2894	3188
T79	A	00003F08	4	2924	3189
T8	A	000014E0	4	757	3118
T80	A	00003FA0	4	2954	3190
T81	A	00004038	4	2985	3191
T82	A	000040D0	4	3015	3192
T83	A	00004168	4	3045	3193
T84	A	00004200	4	3075	3194
T9	A	00001578	4	788	3119
TESTING	F	00001004	4	389	226
TNUM	H	00000004	2	427	225 273
TSUB	A	00000000	4	426	229
TTABLE	F	000042A0	4	3110	
V0	U	00000000	1	3227	
V1	U	00000001	1	3228	228
V10	U	0000000A	1	3237	
V11	U	0000000B	1	3238	
V12	U	0000000C	1	3239	
V13	U	0000000D	1	3240	
V14	U	0000000E	1	3241	
V15	U	0000000F	1	3242	
V16	U	00000010	1	3243	
V17	U	00000011	1	3244	
V18	U	00000012	1	3245	
V19	U	00000013	1	3246	
V1FUDGE	X	00001094	16	418	228
V1O1	X	000010E0	16	555	564
V1O10	X	00001638	16	828	837
V1O11	X	000016D0	16	858	867
V1O12	X	00001768	16	888	897
V1O13	X	00001800	16	922	931
V1O14	X	00001898	16	952	961
V1O15	X	00001930	16	982	991
V1O16	X	000019C8	16	1012	1021
V1O17	X	00001A60	16	1043	1052
V1O18	X	00001AF8	16	1073	1082
V1O19	X	00001B90	16	1103	1112
V1O2	X	00001178	16	585	594
V1O20	X	00001C28	16	1133	1142

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1021	X	00001CC0	16	1164	1173
V1022	X	00001D58	16	1194	1203
V1023	X	00001DF0	16	1224	1233
V1024	X	00001E88	16	1254	1263
V1025	X	00001F20	16	1288	1297
V1026	X	00001FB8	16	1318	1327
V1027	X	00002050	16	1348	1357
V1028	X	000020E8	16	1378	1387
V1029	X	00002180	16	1409	1418
V103	X	00001210	16	615	624
V1030	X	00002218	16	1439	1448
V1031	X	000022B0	16	1469	1478
V1032	X	00002348	16	1499	1508
V1033	X	000023E0	16	1530	1539
V1034	X	00002478	16	1560	1569
V1035	X	00002510	16	1590	1599
V1036	X	000025A8	16	1620	1629
V1037	X	00002640	16	1655	1664
V1038	X	000026D8	16	1685	1694
V1039	X	00002770	16	1715	1724
V104	X	000012A8	16	645	654
V1040	X	00002808	16	1745	1754
V1041	X	000028A0	16	1776	1785
V1042	X	00002938	16	1806	1815
V1043	X	000029D0	16	1836	1845
V1044	X	00002A68	16	1866	1875
V1045	X	00002B00	16	1897	1906
V1046	X	00002B98	16	1927	1936
V1047	X	00002C30	16	1957	1966
V1048	X	00002CC8	16	1987	1996
V1049	X	00002D60	16	2021	2030
V105	X	00001340	16	677	686
V1050	X	00002DF8	16	2051	2060
V1051	X	00002E90	16	2081	2090
V1052	X	00002F28	16	2111	2120
V1053	X	00002FC0	16	2142	2151
V1054	X	00003058	16	2172	2181
V1055	X	000030F0	16	2202	2211
V1056	X	00003188	16	2232	2241
V1057	X	00003220	16	2263	2272
V1058	X	000032B8	16	2293	2302
V1059	X	00003350	16	2323	2332
V106	X	000013D8	16	707	716
V1060	X	000033E8	16	2353	2362
V1061	X	00003480	16	2387	2396
V1062	X	00003518	16	2417	2426
V1063	X	000035B0	16	2447	2456
V1064	X	00003648	16	2477	2486
V1065	X	000036E0	16	2508	2517
V1066	X	00003778	16	2538	2547
V1067	X	00003810	16	2568	2577
V1068	X	000038A8	16	2598	2607
V1069	X	00003940	16	2629	2638
V107	X	00001470	16	737	746
V1070	X	000039D8	16	2659	2668
V1071	X	00003A70	16	2689	2698

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1O72	X	00003B08	16	2719	2728
V1O73	X	00003BA0	16	2753	2762
V1O74	X	00003C38	16	2783	2792
V1O75	X	00003CD0	16	2813	2822
V1O76	X	00003D68	16	2843	2852
V1O77	X	00003E00	16	2874	2883
V1O78	X	00003E98	16	2904	2913
V1O79	X	00003F30	16	2934	2943
V1O8	X	00001508	16	767	776
V1O80	X	00003FC8	16	2964	2973
V1O81	X	00004060	16	2995	3004
V1O82	X	000040F8	16	3025	3034
V1O83	X	00004190	16	3055	3064
V1O84	X	00004228	16	3085	3094
V1O9	X	000015A0	16	798	807
V1OUTPUT	X	00000028	16	437	233
V2	U	00000002	1	3229	
V20	U	00000014	1	3247	
V21	U	00000015	1	3248	
V22	U	00000016	1	3249	560 563 564 590 593 594 620 623 624 650 653 654 682 685 686 712 715 716 742 745 746 772 775 776 803 806 807 833 836 837 863 866 867 893 896 897 927 930 931 957 960 961 987 990 991 1017 1020 1021 1048 1051 1052 1078 1081 1082 1108 1111 1112 1138 1141 1142 1169 1172 1173 1199 1202 1203 1229 1232 1233 1259 1262 1263 1293 1296 1297 1323 1326 1327 1353 1356 1357 1383 1386 1387 1414 1417 1418 1444 1447 1448 1474 1477 1478 1504 1507 1508 1535 1538 1539 1565 1568 1569 1595 1598 1599 1625 1628 1629 1660 1663 1664 1690 1693 1694 1720 1723 1724 1750 1753 1754 1781 1784 1785 1811 1814 1815 1841 1844 1845 1871 1874 1875 1902 1905 1906 1932 1935 1936 1962 1965 1966 1992 1995 1996 2026 2029 2030 2056 2059 2060 2086 2089 2090 2116 2119 2120 2147 2150 2151 2177 2180 2181 2207 2210 2211 2237 2240 2241 2268 2271 2272 2298 2301 2302 2328 2331 2332 2358 2361 2362 2392 2395 2396 2422 2425 2426 2452 2455 2456 2482 2485 2486 2513 2516 2517 2543 2546 2547 2573 2576 2577 2603 2606 2607 2634 2637 2638 2664 2667 2668 2694 2697 2698 2724 2727 2728 2758 2761 2762 2788 2791 2792 2818 2821 2822 2848 2851 2852 2879 2882 2883 2909 2912 2913 2939 2942 2943 2969 2972 2973 3000 3003 3004 3030 3033 3034 3060 3063 3064 3090 3093 3094
V23	U	00000017	1	3250	562 563 592 593 622 623 652 653 684 685 714 715 744 745 774 775 805 806 835 836 865 866 895 896 929 930 959 960 989 990 1019 1020 1050 1051 1080 1081 1110 1111 1140 1141 1171 1172 1201 1202 1231 1232 1261 1262 1295 1296 1325 1326 1355 1356 1385 1386 1416 1417 1446 1447 1476 1477 1506 1507 1537 1538 1567 1568 1597 1598 1627 1628 1662 1663 1692 1693 1722 1723 1752 1753 1783 1784 1813 1814 1843 1844 1873 1874 1904 1905 1934 1935 1964 1965 1994 1995 2028 2029 2058 2059 2088 2089 2118 2119 2149 2150 2179 2180 2209 2210 2239 2240 2270 2271 2300 2301 2330 2331 2360 2361 2394 2395 2424 2425 2454 2455 2484 2485 2515 2516 2545 2546 2575 2576 2605 2606 2636 2637 2666 2667 2696 2697 2726 2727 2760 2761 2790 2791 2820 2821 2850 2851 2881 2882 2911 2912 2941 2942 2971 2972 3002 3003 3032 3033 3062 3063 3092 3093
V24	U	00000018	1	3251	
V25	U	00000019	1	3252	
V26	U	0000001A	1	3253	
V27	U	0000001B	1	3254	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V28	U	0000001C	1	3255	
V29	U	0000001D	1	3256	
V2ADDR	A	00000010	4	432	559 589 619 649 681 711 741 771 802 832 862 892 926 956 986 1016 1047 1077 1107 1137 1168 1198 1228 1258 1292 1322 1352 1382 1413 1443 1473 1503 1534 1564 1594 1624 1659 1689 1719 1749 1780 1810 1840 1870 1901 1931 1961 1991 2025 2055 2085 2115 2146 2176 2206 2236 2267 2297 2327 2357 2391 2421 2451 2481 2512 2542 2572 2602 2633 2663 2693 2723 2757 2787 2817 2847 2878 2908 2938 2968 2999 3029 3059 3089
V3	U	00000003	1	3230	
V30	U	0000001E	1	3257	
V31	U	0000001F	1	3258	
V3ADDR	A	00000014	4	433	561 591 621 651 683 713 743 773 804 834 864 894 928 958 988 1018 1049 1079 1109 1139 1170 1200 1230 1260 1294 1324 1354 1384 1415 1445 1475 1505 1536 1566 1596 1626 1661 1691 1721 1751 1782 1812 1842 1872 1903 1933 1963 1993 2027 2057 2087 2117 2148 2178 2208 2238 2269 2299 2329 2359 2393 2423 2453 2483 2514 2544 2574 2604 2635 2665 2695 2725 2759 2789 2819 2849 2880 2910 2940 2970 3001 3031 3061 3091
V4	U	00000004	1	3231	
V5	U	00000005	1	3232	
V6	U	00000006	1	3233	
V7	U	00000007	1	3234	
V8	U	00000008	1	3235	
V9	U	00000009	1	3236	
X0001	U	000002A8	1	196	184 197
X1	F	000010F8	4	558	545
X10	F	00001650	4	831	818
X11	F	000016E8	4	861	848
X12	F	00001780	4	891	878
X13	F	00001818	4	925	912
X14	F	000018B0	4	955	942
X15	F	00001948	4	985	972
X16	F	000019E0	4	1015	1002
X17	F	00001A78	4	1046	1033
X18	F	00001B10	4	1076	1063
X19	F	00001BA8	4	1106	1093
X2	F	00001190	4	588	575
X20	F	00001C40	4	1136	1123
X21	F	00001CD8	4	1167	1154
X22	F	00001D70	4	1197	1184
X23	F	00001E08	4	1227	1214
X24	F	00001EA0	4	1257	1244
X25	F	00001F38	4	1291	1278
X26	F	00001FD0	4	1321	1308
X27	F	00002068	4	1351	1338
X28	F	00002100	4	1381	1368
X29	F	00002198	4	1412	1399
X3	F	00001228	4	618	605
X30	F	00002230	4	1442	1429
X31	F	000022C8	4	1472	1459
X32	F	00002360	4	1502	1489
X33	F	000023F8	4	1533	1520
X34	F	00002490	4	1563	1550
X35	F	00002528	4	1593	1580
X36	F	000025C0	4	1623	1610

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X37	F	00002658	4	1658	1645
X38	F	000026F0	4	1688	1675
X39	F	00002788	4	1718	1705
X4	F	000012C0	4	648	635
X40	F	00002820	4	1748	1735
X41	F	000028B8	4	1779	1766
X42	F	00002950	4	1809	1796
X43	F	000029E8	4	1839	1826
X44	F	00002A80	4	1869	1856
X45	F	00002B18	4	1900	1887
X46	F	00002BB0	4	1930	1917
X47	F	00002C48	4	1960	1947
X48	F	00002CE0	4	1990	1977
X49	F	00002D78	4	2024	2011
X5	F	00001358	4	680	667
X50	F	00002E10	4	2054	2041
X51	F	00002EA8	4	2084	2071
X52	F	00002F40	4	2114	2101
X53	F	00002FD8	4	2145	2132
X54	F	00003070	4	2175	2162
X55	F	00003108	4	2205	2192
X56	F	000031A0	4	2235	2222
X57	F	00003238	4	2266	2253
X58	F	000032D0	4	2296	2283
X59	F	00003368	4	2326	2313
X6	F	000013F0	4	710	697
X60	F	00003400	4	2356	2343
X61	F	00003498	4	2390	2377
X62	F	00003530	4	2420	2407
X63	F	000035C8	4	2450	2437
X64	F	00003660	4	2480	2467
X65	F	000036F8	4	2511	2498
X66	F	00003790	4	2541	2528
X67	F	00003828	4	2571	2558
X68	F	000038C0	4	2601	2588
X69	F	00003958	4	2632	2619
X7	F	00001488	4	740	727
X70	F	000039F0	4	2662	2649
X71	F	00003A88	4	2692	2679
X72	F	00003B20	4	2722	2709
X73	F	00003BB8	4	2756	2743
X74	F	00003C50	4	2786	2773
X75	F	00003CE8	4	2816	2803
X76	F	00003D80	4	2846	2833
X77	F	00003E18	4	2877	2864
X78	F	00003EB0	4	2907	2894
X79	F	00003F48	4	2937	2924
X8	F	00001520	4	770	757
X80	F	00003FE0	4	2967	2954
X81	F	00004078	4	2998	2985
X82	F	00004110	4	3028	3015
X83	F	000041A8	4	3058	3045
X84	F	00004240	4	3088	3075
X9	F	000015B8	4	801	788
XC0001	U	000002D0	1	210	202
ZVE7TST	J	00000000	17408	123	126 128 132 136 387 124

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
=A(E7TESTS)	A	00000498	4	365	216
=AL2(L'MSGMSG)	R	000004A2	2	368	315
=F'1'	F	0000049C	4	366	251
=F'64'	F	00000494	4	364	201
=H'0'	H	000004A0	2	367	310

```
 MACRO    DEFN   REFERENCES

FCHECK     76    183
PTTABLE   501   3109
VRR_C     456    542    572    602    632    664    694    724    754    785    815    845    875    909    939    969    999   1030
                1060   1090   1120   1151   1181   1211   1241   1275   1305   1335   1365   1396   1426   1456   1486   1517   1547
                1577   1607   1642   1672   1702   1732   1763   1793   1823   1853   1884   1914   1944   1974   2008   2038   2068
                2098   2129   2159   2189   2219   2250   2280   2310   2340   2374   2404   2434   2464   2495   2525   2555   2585
                2616   2646   2676   2706   2740   2770   2800   2830   2861   2891   2921   2951   2982   3012   3042   3072
```

```
   DESC      SYMBOL    SIZE      POS         ADDR

Entry: 0

Image       IMAGE     17408   0000-43FF   0000-43FF
  Region                17408   0000-43FF   0000-43FF
    CSECT   ZVE7TST   17408   0000-43FF   0000-43FF
```

```
   STMT                         FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e7-09-multiply.asm

** NO ERRORS FOUND **
```