```
     LOC        OBJECT CODE        ADDR1     ADDR2     STMT

                                                         2 ***************************************************************************
                                                         3 *
                                                         4 *    Zvector E7 instruction tests for VRR-d encoded:
                                                         5 *
                                                         6 *      E7A9 VMALH  - Vector Multiply and Add Logical High
                                                         7 *      E7AA VMAL   - Vector Multiply and Add Low
                                                         8 *      E7AB VMAH   - Vector Multiply and Add High
                                                         9 *      E7AC VMALE  - Vector Multiply and Add Logical Even
                                                        10 *      E7AD VMALO  - Vector Multiply and Add Logical Odd
                                                        11 *      E7AE VMAE   - Vector Multiply and Add Even
                                                        12 *      E7AF VMAO   - Vector Multiply and Add Odd
                                                        13 *
                                                        14 *         James Wekel March 2025
                                                        15 *              July 2025 - Vector-enhancements facility 3 update
                                                        16 ***************************************************************************

                                                        18 ***************************************************************************
                                                        19 *
                                                        20 *        basic instruction tests
                                                        21 *
                                                        22 ***************************************************************************
                                                        23 *  This program tests proper functioning of the z/arch E7 VRR-d vector
                                                        24 *  multiply and add (logical high, low, high, logical even,
                                                        25 *  logical odd, even, and odd) instructions.
                                                        26 *  Exceptions are not tested.
                                                        27 *
                                                        28 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                        29 *  obvious coding errors.  None of the tests are thorough.  They are
                                                        30 *  NOT designed to test all aspects of any of the instructions.
                                                        31 *
                                                        32 ***************************************************************************
                                                        33 *
                                                        34 *    *Testcase zvector-e7-10-multiplyAdd
                                                        35 *    *
                                                        36 *    *   Zvector E7 instruction tests for VRR-d encoded:
                                                        37 *    *
                                                        38 *    *   E7A9 VMALH  - Vector Multiply and Add Logical High
                                                        39 *    *   E7AA VMAL   - Vector Multiply and Add Low
                                                        40 *    *   E7AB VMAH   - Vector Multiply and Add High
                                                        41 *    *   E7AC VMALE  - Vector Multiply and Add Logical Even
                                                        42 *    *   E7AD VMALO  - Vector Multiply and Add Logical Odd
                                                        43 *    *   E7AE VMAE   - Vector Multiply and Add Even
                                                        44 *    *   E7AF VMAO   - Vector Multiply and Add Odd
                                                        45 *    *
                                                        46 *    *   # -----------------------------------------------------------------
                                                        47 *    *   #  This tests only the basic function of the instruction.
                                                        48 *    *   #  Exceptions are NOT tested.
                                                        49 *    *   # -----------------------------------------------------------------
                                                        50 *    *
                                                        51 *    mainsize    2
                                                        52 *    numcpu      1
                                                        53 *    sysclear
                                                        54 *    archlvl     z/Arch
                                                        55 *
                                                        56 *    loadcore    "$(testpath)/zvector-e7-10-multiplyAdd.core" 0x0
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                            57 *
                                            58 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                            59 *    runtest     10        # (2 secs if intrinsic used, 10 otherwise!)
                                            60 *    diag8cmd    disable   # (reset back to default)
                                            61 *
                                            62 *    *Done
                                            63 *
                                            64 **********************************************************************
```

```
 LOC          OBJECT CODE      ADDR1    ADDR2    STMT

             66 ****************************************************************************
             67 *          FCHECK Macro - Is a Facility Bit set?
             68 *
             69 *          If the facility bit is NOT set, an message is issued and
             70 *          the test is skipped.
             71 *
             72 *          Fcheck uses R0, R1 and R2
             73 *
             74 * eg.      FCHECK 134,'vector-packed-decimal'
             75 ****************************************************************************
             76          MACRO
             77          FCHECK &BITNO,&NOTSETMSG
             78 .*                      &BITNO : facility bit number to check
             79 .*                      &NOTSETMSG : 'facility name'
             80          LCLA   &FBBYTE        Facility bit in Byte
             81          LCLA   &FBBIT         Facility bit within Byte
             82
             83          LCLA   &L(8)
             84 &L(1)    SetA   128,64,32,16,8,4,2,1  bit positions within byte
             85
             86 &FBBYTE  SETA   &BITNO/8
             87 &FBBIT   SETA   &L((&BITNO-(&FBBYTE*8))+1)
             88 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
             89
             90          B      X&SYSNDX
             91 *                                      Fcheck data area
             92 *                                      skip messgae
             93 SKT&SYSNDX DC  C'     Skipping tests: '
             94          DC     C&NOTSETMSG
             95          DC     C' (bit &BITNO) is not installed.'
             96 SKL&SYSNDX EQU *-SKT&SYSNDX
             97 *                                      facility bits
             98          DS     FD                     gap
             99 FB&SYSNDX DS   4FD
            100          DS     FD                     gap
            101 *
            102 X&SYSNDX EQU *
            103          LA     R0,((X&SYSNDX-FB&SYSNDX)/8)-1
            104          STFLE FB&SYSNDX               get facility bits
            105
            106          XGR    R0,R0
            107          IC     R0,FB&SYSNDX+&FBBYTE    get fbit byte
            108          N      R0,=F'&FBBIT'          is bit set?
            109          BNZ    XC&SYSNDX
            110 *
            111 * facility bit not set, issue message and exit
            112 *
            113          LA     R0,SKL&SYSNDX          message length
            114          LA     R1,SKT&SYSNDX          message address
            115          BAL    R2,MSG
            116
            117          B      EOJ
            118 XC&SYSNDX EQU *
            119          MEND
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2    STMT

                                                 121 ****************************************************************************
                                                 122 *        Low core PSWs
                                                 123 ****************************************************************************
                            00000000  000082E7   124 ZVE7TST  START 0
            00000000                              125          USING ZVE7TST,R0              Low core addressability
                                                 126
                            00000140  00000000   127 SVOLDPSW EQU   ZVE7TST+X'140'           z/Arch Supervisor call old PSW

            00000000        00000000  000001A0   129          ORG   ZVE7TST+X'1A0'          z/Architecure RESTART PSW
            000001A0  00000001 80000000           130          DC    X'0000000180000000'
            000001A8  00000000 00000200           131          DC    AD(BEGIN)

            000001B0        000001B0  000001D0   133          ORG   ZVE7TST+X'1D0'          z/Architecure PROGRAM CHECK PSW
            000001D0  00020001 80000000           134          DC    X'0002000180000000'
            000001D8  00000000 0000DEAD           135          DC    AD(X'DEAD')


            000001E0        000001E0  00000200   137          ORG   ZVE7TST+X'200'          Start of actual test program..


                                                 139 ****************************************************************************
                                                 140 *               The actual "ZVE7TST" program itself...
                                                 141 ****************************************************************************
                                                 142 *
                                                 143 *   Architecture Mode: z/Arch
                                                 144 *   Register Usage:
                                                 145 *
                                                 146 *    R0         (work)
                                                 147 *    R1-4       (work)
                                                 148 *    R5         Testing control table - current test base
                                                 149 *    R6-R7      (work)
                                                 150 *    R8         First base register
                                                 151 *    R9         Second base register
                                                 152 *    R10        Third base register
                                                 153 *    R11        E7TEST call return
                                                 154 *    R12        E7TESTS register
                                                 155 *    R13        (work)
                                                 156 *    R14        Subroutine call
                                                 157 *    R15        Secondary Subroutine call or work
                                                 158 *
                                                 159 ****************************************************************************
            00000200        00000200             161          USING  BEGIN,R8            FIRST Base Register
            00000200        00001200             162          USING  BEGIN+4096,R9       SECOND Base Register
            00000200        00002200             163          USING  BEGIN+8192,R10      THIRD Base Register

            00000200  0580                        165 BEGIN    BALR  R8,0                Initialize FIRST base register
            00000202  0680                        166          BCTR  R8,0                Initialize FIRST base register
            00000204  0680                        167          BCTR  R8,0                Initialize FIRST base register

            00000206  4190 8800            00000800 169        LA    R9,2048(,R8)        Initialize SECOND base register
            0000020A  4190 9800            00000800 170        LA    R9,2048(,R9)        Initialize SECOND base register
                                                 171
```

```
  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

0000020E  41A0 9800                   00000800   172              LA     R10,2048(,R9)    Initialize THIRD base register
00000212  41A0 A800                   00000800   173              LA     R10,2048(,R10)   Initialize THIRD base register
                                                 174
00000216  B600 833C                   0000053C   175              STCTL  R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 833D                   0000053D   176              OI     CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 833D                   0000053D   177              OI     CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 833C                   0000053C   178              LCTL   R0,R0,CTLR0      Reload updated CR0
                                                 179
                                                 180 *******************************************************************
                                                 181 * Is z/Architecture vector facility installed  (bit 129)
                                                 182 *******************************************************************
                                                 183
                                                 184              FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                   000002A8   185+             B      X0001
                                                 186+*                                              Fcheck data area
                                                 187+*                                              skip messgae
0000022A  40404040 E2928997                      188+SKT0001 DC   C'     Skipping tests: '
0000023E  A961C199 838889A3                      189+         DC   C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                      190+         DC   C' (bit 129) is not installed.'
                            0000004E  00000001   191+SKL0001 EQU  *-SKT0001
                                                 192+*                                              facility bits
00000278  00000000 00000000                      193+         DS   FD                               gap
00000280  00000000 00000000                      194+FB0001 DS   4FD
000002A0  00000000 00000000                      195+         DS   FD                               gap
                                                 196+*
                            000002A8  00000001   197+X0001 EQU  *
000002A8  4100 0004                   00000004   198+         LA     R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                   00000280   199+         STFLE  FB0001                          get facility bits
000002B0  B982 0000                              200+         XGR    R0,R0
000002B4  4300 8090                   00000290   201+         IC     R0,FB0001+16                    get fbit byte
000002B8  5400 8344                   00000544   202+         N      R0,=F'64'                       is bit set?
000002BC  4770 80D0                   000002D0   203+         BNZ    XC0001
                                                 204+*
                                                 205+* facility bit not set, issue message and exit
                                                 206+*
000002C0  4100 004E                   0000004E   207+         LA     R0,SKL0001                      message length
000002C4  4110 802A                   0000022A   208+         LA     R1,SKT0001                      message address
000002C8  4520 8258                   00000458   209+         BAL    R2,MSG
000002CC  47F0 8320                   00000520   210+         B      EOJ
                            000002D0  00000001   211+XC0001 EQU  *
```

```
  LOC        OBJECT CODE      ADDR1      ADDR2      STMT

                                                    213 **********************************************************************
                                                    214 * Is z/Architecture vector facility installed  (bit 198)
                                                    215 **********************************************************************
                                                    216
                                                    217           FCHECK 198,'Vector-enhancements facility 3'
000002D0   47F0 8158                      00000358   218+          B      X0002
                                                    219+*                                      Fcheck data area
                                                    220+*                                      skip messgae
000002D4   40404040 E2928997                         221+SKT0002   DC     C'    Skipping tests: '
000002E8   E58583A3 96996085                         222+          DC     C'Vector-enhancements facility 3'
00000306   404D8289 A340F1F9                         223+          DC     C' (bit 198) is not installed.'
                      0000004E   00000001   224+SKL0002   EQU    *-SKT0002
                                                    225+*                                      facility bits
00000328   00000000 00000000                         226+          DS     FD                   gap
00000330   00000000 00000000                         227+FB0002    DS     4FD
00000350   00000000 00000000                         228+          DS     FD                   gap
                                                    229+*
                      00000358   00000001   230+X0002     EQU    *
00000358   4100 0004                      00000004   231+          LA     R0,((X0002-FB0002)/8)-1
0000035C   B2B0 8130                      00000330   232+          STFLE  FB0002               get facility bits
00000360   B982 0000                                 233+          XGR    R0,R0
00000364   4300 8148                      00000348   234+          IC     R0,FB0002+24         get fbit byte
00000368   5400 8348                      00000548   235+          N      R0,=F'2'             is bit set?
0000036C   4770 8180                      00000380   236+          BNZ    XC0002
                                                    237+*
                                                    238+* facility bit not set, issue message and exit
                                                    239+*
00000370   4100 004E                      0000004E   240+          LA     R0,SKL0002           message length
00000374   4110 80D4                      000002D4   241+          LA     R1,SKT0002           message address
00000378   4520 8258                      00000458   242+          BAL    R2,MSG
0000037C   47F0 8320                      00000520   243+          B      EOJ
                      00000380   00000001   244+XC0002    EQU    *
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                   246 ****************************************************************************
                                                   247 *              Do tests in the E7TESTS table
                                                   248 ****************************************************************************
                                                   249
00000380   58C0 834C                    0000054C   250           L      R12,=A(E7TESTS)      get table of test addresses
                                                   251
                        00000384       00000001    252 NEXTE7    EQU    *
00000384   5850 C000                    00000000   253           L      R5,0(0,R12)          get test address
00000388   1255                                    254           LTR    R5,R5                   have a test?
0000038A   4780 81CE                    000003CE   255           BZ     ENDTEST                  done?
                                                   256
0000038E                   00000000                257           USING  E7TEST,R5
                                                   258
0000038E   4800 5004                    00000004   259           LH     R0,TNUM              save current test number
00000392   5000 8E04                    00001004   260           ST     R0,TESTING           for easy reference
                                                   261
00000396   E710 8E94 0006               00001094   262           VL     V1,V1FUDGE
0000039C   58B0 5000                    00000000   263           L      R11,TSUB             get address of test routine
000003A0   05BB                                    264           BALR   R11,R11              do test
                                                   265
000003A2   E310 5020 0014               00000020   266           LGF    R1,READDR            get address of expected result
000003A8   D50F 5030 1000   00000030    00000000   267           CLC    V10UTPUT,0(R1)       valid?
000003AE   4770 81BA                    000003BA   268           BNE    FAILMSG                 no, issue failed message
                                                   269
000003B2   41C0 C004                    00000004   270           LA     R12,4(0,R12)         next test address
000003B6   47F0 8184                    00000384   271           B      NEXTE7
```

```
  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

                                                 273 ****************************************************************************
                                                 274 * result not as expected:
                                                 275 *          issue message with test number, instruction under test
                                                 276 *                  and instruction m4
                                                 277 ****************************************************************************
                             000003BA  00000001  278 FAILMSG  EQU     *
000003BA   45F0 81DC                    000003DC  279          BAL     R15,RPTERROR


                                                 281 ****************************************************************************
                                                 282 * continue after a failed test
                                                 283 ****************************************************************************
                             000003BE  00000001  284 FAILCONT EQU     *
000003BE   5800 8350                    00000550  285          L       R0,=F'1'              set failed test indicator
000003C2   5000 8E00                    00001000  286          ST      R0,FAILED
                                                 287
000003C6   41C0 C004                    00000004  288          LA      R12,4(0,R12)      next test address
000003CA   47F0 8184                    00000384  289          B       NEXTE7


                                                 291 ****************************************************************************
                                                 292 * end of testing; set ending psw
                                                 293 ****************************************************************************
                             000003CE  00000001  294 ENDTEST  EQU     *
000003CE   5810 8E00                    00001000  295          L       R1,FAILED             did a test fail?
000003D2   1211                                   296          LTR     R1,R1
000003D4   4780 8320                    00000520  297          BZ      EOJ                     No, exit
000003D8   47F0 8338                    00000538  298          B       FAILTEST                Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  300  ****************************************************************
                                                  301  *         RPTERROR                    Report instruction test in error
                                                  302  ****************************************************************

000003DC   50F0 8240                    00000440  304  RPTERROR ST    R15,RPTSAVE            Save return address
000003E0   5050 8244                    00000444  305           ST    R5,RPTSVR5             Save R5
                                                  306  *
000003E4   4820 5004                    00000004  307           LH    R2,TNUM                get test number and convert
000003E8   4E20 8E73                    00001073  308           CVD   R2,DECNUM
000003EC   D211 8E5D 8E47     0000105D  00001047  309           MVC   PRT3,EDIT
000003F2   DE11 8E5D 8E73     0000105D  00001073  310           ED    PRT3,DECNUM
000003F8   D202 8E18 8E6A     00001018  0000106A  311           MVC   PRTNUM(3),PRT3+13      fill in message with test #
                                                  312
000003FE   D207 8E33 5008     00001033  00000008  313           MVC   PRTNAME,OPNAME         fill in message with instruction
                                                  314  *
00000404   E320 5007 0076               00000007  315           LB    R2,m5                  get m5 and convert
0000040A   4E20 8E73                    00001073  316           CVD   R2,DECNUM
0000040E   D211 8E5D 8E47     0000105D  00001047  317           MVC   PRT3,EDIT
00000414   DE11 8E5D 8E73     0000105D  00001073  318           ED    PRT3,DECNUM
0000041A   D201 8E44 8E6B     00001044  0000106B  319           MVC   PRTM5(2),PRT3+14       fill in message with m4 field

                                                  321  *
                                                  322  *         Use Hercules Diagnose for Message to console
                                                  323  *
00000420   9002 8248                    00000448  324           STM   R0,R2,RPTDWSAV         save regs used by MSG
00000424   4100 003F                    0000003F  325           LA    R0,PRTLNG              message length
00000428   4110 8E08                    00001008  326           LA    R1,PRTLINE             messagfe address
0000042C   4520 8258                    00000458  327           BAL   R2,MSG                 call Hercules console MSG display
00000430   9802 8248                    00000448  328           LM    R0,R2,RPTDWSAV         restore regs


00000434   5850 8244                    00000444  330           L     R5,RPTSVR5             Restore R5
00000438   58F0 8240                    00000440  331           L     R15,RPTSAVE            Restore return address
0000043C   07FF                                   332           BR    R15                    Return to caller

00000440   00000000                               334  RPTSAVE  DC    F'0'                   R15 save area
00000444   00000000                               335  RPTSVR5  DC    F'0'                   R5 save area

00000448   00000000 00000000                      337  RPTDWSAV DC    2D'0'                  R0-R2 save area for MSG call
```

```
  LOC          OBJECT CODE        ADDR1     ADDR2     STMT

                                                      339 ****************************************************************************
                                                      340 *          Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                      341 *               R2 = return address
                                                      342 ****************************************************************************

00000458   4900 8354                        00000554  344 MSG      CH      R0,=H'0'            Do we even HAVE a message?
0000045C   07D2                                       345          BNHR    R2                  No, ignore

0000045E   9002 8294                        00000494  347          STM     R0,R2,MSGSAVE       Save registers

00000462   4900 8356                        00000556  349          CH      R0,=AL2(L'MSGMSG)   Message length within limits?
00000466   47D0 826E                        0000046E  350          BNH     MSGOK               Yes, continue
0000046A   4100 005F                        0000005F  351          LA      R0,L'MSGMSG         No, set to maximum

0000046E   1820                                       353 MSGOK    LR      R2,R0               Copy length to work register
00000470   0620                                       354          BCTR    R2,0                Minus-1 for execute
00000472   4420 82A0                        000004A0  355          EX      R2,MSGMVC           Copy message to O/P buffer

00000476   4120 200A                        0000000A  357          LA      R2,1+L'MSGCMD(,R2)  Calculate true command length
0000047A   4110 82A6                        000004A6  358          LA      R1,MSGCMD           Point to true command

0000047E   83120008                                   360          DC      X'83',X'12',X'0008' Issue Hercules Diagnose X'008'
00000482   4780 828E                        0000048E  361          BZ      MSGRET              Return if successful
                                                      362
00000486   1222                                       363          LTR     R2,R2               Is Diag8 Ry (R2) 0?
00000488   4780 828E                        0000048E  364          BZ      MSGRET               an error occurred but coninue
                                                      365
0000048C   0000                                       366          DC      H'0'                CRASH for debugging purposes

0000048E   9802 8294                        00000494  368 MSGRET   LM      R0,R2,MSGSAVE       Restore registers
00000492   07F2                                       369          BR      R2                  Return to caller




00000494   00000000 00000000                          371 MSGSAVE  DC      3F'0'               Registers save area
000004A0   D200 82AF 1000       000004AF   00000000  372 MSGMVC   MVC     MSGMSG(0),0(R1)     Executed instruction

000004A6   D4E2C7D5 D6C8405C                          374 MSGCMD   DC      C'MSGNOH * '        *** HERCULES MESSAGE COMMAND ***
000004AF   40404040 40404040                          375 MSGMSG   DC      CL95' '             The message text to be displayed
                                                      376
```

```
 LOC          OBJECT CODE        ADDR1      ADDR2     STMT

                                                      378 ********************************************************************
                                                      379 *        Normal completion or Abnormal termination PSWs
                                                      380 ********************************************************************


00000510   00020001 80000000                          382 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000520   B2B2 8310                      00000510     384 EOJ      LPSWE EOJPSW                Normal completion


00000528   00020001 80000000                          386 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

00000538   B2B2 8328                      00000528     388 FAILTEST LPSWE FAILPSW               Abnormal termination



                                                      390 ********************************************************************
                                                      391 *        Working Storage
                                                      392 ********************************************************************


0000053C   00000000                                   394 CTLR0    DS    F                     CR0
00000540   00000000                                   395          DS    F

00000544                                              397          LTORG ,                     Literals pool
00000544   00000040                                   398                =F'64'
00000548   00000002                                   399                =F'2'
0000054C   00008084                                   400                =A(E7TESTS)
00000550   00000001                                   401                =F'1'
00000554   0000                                       402                =H'0'
00000556   005F                                       403                =AL2(L'MSGMSG)
                                                      404
                                                      405 *        some constants
                                                      406
                            00000400    00000001      407 K        EQU   1024                  One KB
                            00001000    00000001      408 PAGE     EQU   (4*K)                 Size of one page
                            00010000    00000001      409 K64      EQU   (64*K)                64 KB
                            00100000    00000001      410 MB       EQU   (K*K)                 1 MB
                                                      411
                            AABBCCDD    00000001      412 REG2PATT EQU   X'AABBCCDD'            Polluted Register pattern
                            000000DD    00000001      413 REG2LOW  EQU         X'DD'           (last byte above)
```

```
  LOC        OBJECT CODE      ADDR1      ADDR2     STMT

                                                    415 *=============================================================================
                                                    416 *
                                                    417 *   NOTE: start data on an address that is easy to display
                                                    418 *         within Hercules
                                                    419 *
                                                    420 *=============================================================================
                                                    421
00000558                       00000558  00001000   422            ORG    ZVE7TST+X'1000'
00001000   00000000                                 423 FAILED   DC     F'0'                         some test failed?
00001004   00000000                                 424 TESTING  DC     F'0'                         current test number

                                                    426 *
                                                    427 *           failed message and associated editting
                                                    428 *
00001008   40404040 40404040                        429 PRTLINE  DC     C'          Test # '
00001018   A7A7A7                                    430 PRTNUM   DC     C'xxx'
0000101B   40868189 93858440                         431           DC     c' failed for instruction '
00001033   A7A7A7A7 A7A7A7A7                         432 PRTNAME  DC     CL8'xxxxxxxx'
0000103B   40A689A3 884094F5                         433           DC     C' with m5='
00001044   A7A7                                      434 PRTM5    DC     C'xx'
00001046   4B                                        435           DC     C'.'
                               0000003F  00000001   436 PRTLNG   EQU    *-PRTLINE
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  438 ************************************************************************
                                                  439 *         TEST failed : message working storge
                                                  440 ************************************************************************
00001047   40212020 20202020                      441 EDIT     DC    XL18'402120202020202020202020202020202020'
                                                  442
00001059   7E7E7E6E                               443          DC    C' ===>'
0000105D   40404040 40404040                      444 PRT3     DC    CL18' '
0000106F   4C7E7E7E                               445          DC    C' <==='
00001073   00000000 00000000                      446 DECNUM   DS    CL16


                                                  448 ************************************************************************
                                                  449 *         Vector instruction results, pollution and input
                                                  450 ************************************************************************
00001084                                          451          DS    0F
00001084   00000000 00000000                      452          DS    XL16                                          gap
00001094   FFFFFFFF FFFFFFFF                       453 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'     V1 FUDGE
000010A4   00000000 00000000                      454          DS    XL16
```

```
    LOC         OBJECT CODE      ADDR1     ADDR2     STMT

                                                     456 ****************************************************************************
                                                     457 *          E7TEST DSECT
                                                     458 ****************************************************************************

                                                     460 E7TEST    DSECT ,
00000000   00000000                                  461 TSUB      DC    A(0)              pointer  to test
00000004   0000                                      462 TNUM      DC    H'00'             Test Number
00000006   00                                        463           DC    X'00'
00000007   00                                        464 M5        DC    HL1'00'           m4 used
                                                     465
00000008   40404040 40404040                         466 OPNAME    DC    CL8' '            E7 name
00000010   00000000                                  467 V2ADDR    DC    A(0)              address of v2 source
00000014   00000000                                  468 V3ADDR    DC    A(0)              address of v3 source
00000018   00000000                                  469 V4ADDR    DC    A(0)              address of v4 source
0000001C   00000000                                  470 RELEN     DC    A(0)              RESULT LENGTH
00000020   00000000                                  471 READDR    DC    A(0)              result (expected) address
00000028   00000000 00000000                         472           DS    FD                  gap
00000030   00000000 00000000                         473 V1OUTPUT  DS    XL16              V1 Output
00000040   00000000 00000000                         474           DS    FD                  gap
                                                     475
                                                     476 *          test routine will be here (from VRR-d macro)
                                                     477 *
                                                     478 *          followed by
                                                     479 *               EXPECTED RESULT

                        00000000  000082E7           481 ZVE7TST   CSECT ,
000010B4                                              482           DS    0F

                                                     484 ****************************************************************************
                                                     485 *     Macros to help build test tables
                                                     486 ****************************************************************************


                                                     488 *
                                                     489 * macro to generate individual test
                                                     490 *
                                                     491           MACRO
                                                     492           VRR_D &INST,&M5
                                                     493 .*                                 &INST   - VRR-d instruction under test
                                                     494 .*                                 &m5     - m5 field
                                                     495
                                                     496           GBLA  &TNUM
                                                     497 &TNUM     SETA  &TNUM+1
                                                     498
                                                     499           DS    0FD
                                                     500           USING *,R5             base for test data and test routine
                                                     501
                                                     502 T&TNUM    DC    A(X&TNUM)         address of test routine
                                                     503           DC    H'&TNUM'         test number
                                                     504           DC    X'00'
                                                     505           DC    HL1'&M5'         m5
                                                     506           DC    CL8'&INST'       instruction name
```

```
 LOC           OBJECT CODE      ADDR1     ADDR2      STMT
                                                     507              DC     A(RE&TNUM+16)        address of v2 source
                                                     508              DC     A(RE&TNUM+32)        address of v3 source
                                                     509              DC     A(RE&TNUM+48)        address of v4 source
                                                     510              DC     A(16)                result length
                                                     511 REA&TNUM DC     A(RE&TNUM)           result address
                                                     512              DS     FD                   gap
                                                     513 V10&TNUM DS     XL16                 V1 output
                                                     514              DS     FD                   gap
                                                     515 .*
                                                     516 *
                                                     517 X&TNUM    DS     0F
                                                     518              LGF    R1,V2ADDR            load v2 source
                                                     519              VL     v22,0(R1)            use v22 to test decoder
                                                     520
                                                     521              LGF    R1,V3ADDR            load v3 source
                                                     522              VL     v23,0(R1)            use v23 to test decoder
                                                     523
                                                     524              LGF    R1,V4ADDR            load v4 source
                                                     525              VL     v24,0(R1)            use v24 to test decoder
                                                     526
                                                     527              &INST V22,V22,V23,V24,&M5  test instruction (dest is a source)
                                                     528              VST    V22,V10&TNUM          save v1 output
                                                     529
                                                     530              BR     R11                  return
                                                     531
                                                     532 RE&TNUM   DC     0F                   xl16 expected result
                                                     533
                                                     534              DROP   R5
                                                     535              MEND


                                                     537 *
                                                     538 * macro to generate table of pointers to individual tests
                                                     539 *
                                                     540              MACRO
                                                     541              PTTABLE
                                                     542              GBLA   &TNUM
                                                     543              LCLA   &CUR
                                                     544 &CUR      SETA   1
                                                     545 .*
                                                     546 TTABLE    DS     0F
                                                     547 .LOOP     ANOP
                                                     548 .*
                                                     549              DC     A(T&CUR)
                                                     550 .*
                                                     551 &CUR      SETA   &CUR+1
                                                     552              AIF    (&CUR LE &TNUM).LOOP
                                                     553 *
                                                     554              DC     A(0)                 END OF TABLE
                                                     555              DC     A(0)
                                                     556 .*
                                                     557              MEND
                                                     558
```

```
  LOC         OBJECT CODE      ADDR1      ADDR2     STMT

                                                    560 *****************************************************************************
                                                    561 *          E7 VRR-d tests
                                                    562 *****************************************************************************
                                                    563           PRINT DATA
 000010B8   00000000 00000000                        564           DS    FD
                                                    565 *
                                                    566 *    E7A9 VMALH  - Vector Multiply and Add Logical High
                                                    567 *    E7AA VMAL   - Vector Multiply and Add Low
                                                    568 *    E7AB VMAH   - Vector Multiply and Add High
                                                    569 *    E7AC VMALE  - Vector Multiply and Add Logical Even
                                                    570 *    E7AD VMALO  - Vector Multiply and Add Logical Odd
                                                    571 *    E7AE VMAE   - Vector Multiply and Add Even
                                                    572 *    E7AF VMAO   - Vector Multiply and Add Odd
                                                    573 *
                                                    574 *          VRR-d instruction, m5
                                                    575 *              followed by
                                                    576 *                 16 byte expected result (V1)
                                                    577 *                 16 byte V2 source
                                                    578 *                 16 byte V3 source
                                                    579 *                 16 byte V4 source
                                                    580 *-------------------------------------------------------------------------
                                                    581 *   VMALH  - Vector Multiply and Add Logical High
                                                    582 *-------------------------------------------------------------------------
                                                    583 * Byte
                                                    584           VRR_D VMALH,0
 000010C0                                             585+          DS    0FD
 000010C0                         000010C0           586+          USING *,R5                base for test data and test routine
 000010C0   00001108                                 587+T1        DC    A(X1)               address of test routine
 000010C4   0001                                     588+          DC    H'1'                test number
 000010C6   00                                       589+          DC    X'00'
 000010C7   00                                       590+          DC    HL1'0'              m5
 000010C8   E5D4C1D3 C8404040                         591+          DC    CL8'VMALH'          instruction name
 000010D0   0000114C                                 592+          DC    A(RE1+16)           address of v2 source
 000010D4   0000115C                                 593+          DC    A(RE1+32)           address of v3 source
 000010D8   0000116C                                 594+          DC    A(RE1+48)           address of v4 source
 000010DC   00000010                                 595+          DC    A(16)               result length
 000010E0   0000113C                                 596+REA1      DC    A(RE1)              result address
 000010E8   00000000 00000000                         597+          DS    FD                  gap
 000010F0   00000000 00000000                         598+V101      DS    XL16                V1 output
 000010F8   00000000 00000000
 00001100   00000000 00000000                         599+          DS    FD                  gap
                                                    600+*
 00001108                                             601+X1        DS    0F
 00001108   E310 5010 0014                00000010    602+          LGF   R1,V2ADDR           load v2 source
 0000110E   E761 0000 0806                00000000    603+          VL    v22,0(R1)           use v22 to test decoder
 00001114   E310 5014 0014                00000014    604+          LGF   R1,V3ADDR           load v3 source
 0000111A   E771 0000 0806                00000000    605+          VL    v23,0(R1)           use v23 to test decoder
 00001120   E310 5018 0014                00000018    606+          LGF   R1,V4ADDR           load v4 source
 00001126   E781 0000 0806                00000000    607+          VL    v24,0(R1)           use v24 to test decoder
 0000112C   E766 7000 8FA9                            608+          VMALH V22,V22,V23,V24,0      test instruction (dest is a source)
 00001132   E760 5030 080E                000010F0    609+          VST   V22,V101             save v1 output
 00001138   07FB                                      610+          BR    R11                 return
 0000113C                                             611+RE1       DC    0F                  xl16 expected result
 0000113C                                             612+          DROP  R5
 0000113C   FE000000 00000002                         613           DC    XL16'FE00000000000002 0000000C000000F4'    result
 00001144   0000000C 000000F4
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000114C	FF000000 00000019			614	DC	XL16'FF00000000000019 00000038000000FA'	v2
00001154	00000038 000000FA						
0000115C	FF000000 00000019			615	DC	XL16'FF00000000000019 00000038000000FA'	v3
00001164	00000038 000000FA						
0000116C	00000000 00000000			616	DC	XL16'0000000000000000 0000000000000000'	v4
00001174	00000000 00000000						
				617			
				618	VRR_D	VMALH,0	
00001180				619+	DS	0FD	
00001180		00001180		620+	USING	*,R5	base for test data and test routine
00001180	000011C8			621+T2	DC	A(X2)	address of test routine
00001184	0002			622+	DC	H'2'	test number
00001186	00			623+	DC	X'00'	
00001187	00			624+	DC	HL1'0'	m5
00001188	E5D4C1D3 C8404040			625+	DC	CL8'VMALH'	instruction name
00001190	0000120C			626+	DC	A(RE2+16)	address of v2 source
00001194	0000121C			627+	DC	A(RE2+32)	address of v3 source
00001198	0000122C			628+	DC	A(RE2+48)	address of v4 source
0000119C	00000010			629+	DC	A(16)	result length
000011A0	000011FC			630+REA2	DC	A(RE2)	result address
000011A8	00000000 00000000			631+	DS	FD	gap
000011B0	00000000 00000000			632+V1O2	DS	XL16	V1 output
000011B8	00000000 00000000						
000011C0	00000000 00000000			633+	DS	FD	gap
				634+*			
000011C8				635+X2	DS	0F	
000011C8	E310 5010 0014		00000010	636+	LGF	R1,V2ADDR	load v2 source
000011CE	E761 0000 0806		00000000	637+	VL	v22,0(R1)	use v22 to test decoder
000011D4	E310 5014 0014		00000014	638+	LGF	R1,V3ADDR	load v3 source
000011DA	E771 0000 0806		00000000	639+	VL	v23,0(R1)	use v23 to test decoder
000011E0	E310 5018 0014		00000018	640+	LGF	R1,V4ADDR	load v4 source
000011E6	E781 0000 0806		00000000	641+	VL	v24,0(R1)	use v24 to test decoder
000011EC	E766 7000 8FA9			642+	VMALH	V22,V22,V23,V24,0	test instruction (dest is a source)
000011F2	E760 5030 080E		000011B0	643+	VST	V22,V1O2	save v1 output
000011F8	07FB			644+	BR	R11	return
000011FC				645+RE2	DC	0F	xl16 expected result
000011FC				646+	DROP	R5	
000011FC	FE000001 00000006			647	DC	XL16'FE00000100000006 0000000C000000F4'	result
00001204	0000000C 000000F4						
0000120C	FF0000FF 00000029			648	DC	XL16'FF0000FF00000029 00000038000000FA'	v2
00001214	00000038 000000FA						
0000121C	FF000001 00000029			649	DC	XL16'FF00000100000029 00000038000000FA'	v3
00001224	00000038 000000FA						
0000122C	00000001 0000002F			650	DC	XL16'000000010000002F 0000000000000002'	v4
00001234	00000000 00000002						
				651			
				652	VRR_D	VMALH,0	
00001240				653+	DS	0FD	
00001240		00001240		654+	USING	*,R5	base for test data and test routine
00001240	00001288			655+T3	DC	A(X3)	address of test routine
00001244	0003			656+	DC	H'3'	test number
00001246	00			657+	DC	X'00'	
00001247	00			658+	DC	HL1'0'	m5
00001248	E5D4C1D3 C8404040			659+	DC	CL8'VMALH'	instruction name
00001250	000012CC			660+	DC	A(RE3+16)	address of v2 source
00001254	000012DC			661+	DC	A(RE3+32)	address of v3 source

```
  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

00001258   000012EC                                662+        DC    A(RE3+48)        address of v4 source
0000125C   00000010                                663+        DC    A(16)            result length
00001260   000012BC                                664+REA3    DC    A(RE3)           result address
00001268   00000000 00000000                       665+        DS    FD               gap
00001270   00000000 00000000                       666+V103    DS    XL16             V1 output
00001278   00000000 00000000
00001280   00000000 00000000                       667+        DS    FD               gap
                                                   668+*
00001288                                           669+X3      DS    0F
00001288   E310 5010 0014              00000010    670+        LGF   R1,V2ADDR        load v2 source
0000128E   E761 0000 0806              00000000    671+        VL    v22,0(R1)        use v22 to test decoder
00001294   E310 5014 0014              00000014    672+        LGF   R1,V3ADDR        load v3 source
0000129A   E771 0000 0806              00000000    673+        VL    v23,0(R1)        use v23 to test decoder
000012A0   E310 5018 0014              00000018    674+        LGF   R1,V4ADDR        load v4 source
000012A6   E781 0000 0806              00000000    675+        VL    v24,0(R1)        use v24 to test decoder
000012AC   E766 7000 8FA9                          676+        VMALH V22,V22,V23,V24,0    test instruction (dest is a source)
000012B2   E760 5030 080E              00001270    677+        VST   V22,V103          save v1 output
000012B8   07FB                                    678+        BR    R11              return
000012BC                                           679+RE3     DC    0F               xl16 expected result
000012BC                                           680+        DROP  R5
000012BC   FF000000 00000000                       681         DC    XL16'FF00000000000000 0000000000000001'     result
000012C4   00000000 00000001
000012CC   FF020304 05060708                       682         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
000012D4   090A0B0C 0D0E0F10
000012DC   FF020304 05060708                       683         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v3
000012E4   090A0B0C 0D0E0F10
000012EC   FF020304 05060708                       684         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v4
000012F4   090A0B0C 0D0E0F10
                                                   685
                                                   686         VRR_D VMALH,0
00001300                                           687+        DS    0FD
00001300                            00001300       688+        USING *,R5            base for test data and test routine
00001300   00001348                                689+T4      DC    A(X4)            address of test routine
00001304   0004                                    690+        DC    H'4'             test number
00001306   00                                      691+        DC    X'00'
00001307   00                                      692+        DC    HL1'0'           m5
00001308   E5D4C1D3 C8404040                        693+        DC    CL8'VMALH'       instruction name
00001310   0000138C                                694+        DC    A(RE4+16)        address of v2 source
00001314   0000139C                                695+        DC    A(RE4+32)        address of v3 source
00001318   000013AC                                696+        DC    A(RE4+48)        address of v4 source
0000131C   00000010                                697+        DC    A(16)            result length
00001320   0000137C                                698+REA4    DC    A(RE4)           result address
00001328   00000000 00000000                       699+        DS    FD               gap
00001330   00000000 00000000                       700+V104    DS    XL16             V1 output
00001338   00000000 00000000
00001340   00000000 00000000                       701+        DS    FD               gap
                                                   702+*
00001348                                           703+X4      DS    0F
00001348   E310 5010 0014              00000010    704+        LGF   R1,V2ADDR        load v2 source
0000134E   E761 0000 0806              00000000    705+        VL    v22,0(R1)        use v22 to test decoder
00001354   E310 5014 0014              00000014    706+        LGF   R1,V3ADDR        load v3 source
0000135A   E771 0000 0806              00000000    707+        VL    v23,0(R1)        use v23 to test decoder
00001360   E310 5018 0014              00000018    708+        LGF   R1,V4ADDR        load v4 source
00001366   E781 0000 0806              00000000    709+        VL    v24,0(R1)        use v24 to test decoder
0000136C   E766 7000 8FA9                          710+        VMALH V22,V22,V23,V24,0    test instruction (dest is a source)
00001372   E760 5030 080E              00001330    711+        VST   V22,V104          save v1 output
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001378	07FB			712+	BR	R11		return
0000137C				713+RE4	DC	0F		xl16 expected result
0000137C				714+	DROP	R5		
0000137C	FF000000 00000000			715	DC	XL16'FF00000000000000 0000000000000000'		result
00001384	00000000 00000000							
0000138C	FF020304 05060708			716	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'		v2
00001394	090A0B0C 0D0E0F10							
0000139C	FF010102 02030304			717	DC	XL16'FF01010202030304 0405050606070708'		v3
000013A4	04050506 06070708							
000013AC	FF020304 05060708			718	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'		v4
000013B4	090A0B0C 0D0E0F10							
				719				
				720	VRR_D	VMALH,0		
000013C0				721+	DS	0FD		
000013C0		000013C0		722+	USING	*,R5		base for test data and test routine
000013C0	00001408			723+T5	DC	A(X5)		address of test routine
000013C4	0005			724+	DC	H'5'		test number
000013C6	00			725+	DC	X'00'		
000013C7	00			726+	DC	HL1'0'		m5
000013C8	E5D4C1D3 C8404040			727+	DC	CL8'VMALH'		instruction name
000013D0	0000144C			728+	DC	A(RE5+16)		address of v2 source
000013D4	0000145C			729+	DC	A(RE5+32)		address of v3 source
000013D8	0000146C			730+	DC	A(RE5+48)		address of v4 source
000013DC	00000010			731+	DC	A(16)		result length
000013E0	0000143C			732+REA5	DC	A(RE5)		result address
000013E8	00000000 00000000			733+	DS	FD		gap
000013F0	00000000 00000000			734+V105	DS	XL16		V1 output
000013F8	00000000 00000000							
00001400	00000000 00000000			735+	DS	FD		gap
				736+*				
00001408				737+X5	DS	0F		
00001408	E310 5010 0014		00000010	738+	LGF	R1,V2ADDR		load v2 source
0000140E	E761 0000 0806		00000000	739+	VL	v22,0(R1)		use v22 to test decoder
00001414	E310 5014 0014		00000014	740+	LGF	R1,V3ADDR		load v3 source
0000141A	E771 0000 0806		00000000	741+	VL	v23,0(R1)		use v23 to test decoder
00001420	E310 5018 0014		00000018	742+	LGF	R1,V4ADDR		load v4 source
00001426	E781 0000 0806		00000000	743+	VL	v24,0(R1)		use v24 to test decoder
0000142C	E766 7000 8FA9			744+	VMALH	V22,V22,V23,V24,0		test instruction (dest is a source)
00001432	E760 5030 080E		000013F0	745+	VST	V22,V105		save v1 output
00001438	07FB			746+	BR	R11		return
0000143C				747+RE5	DC	0F		xl16 expected result
0000143C				748+	DROP	R5		
0000143C	FF000000 00000000			749	DC	XL16'FF00000000000000 0000000000000000'		result
00001444	00000000 00000000							
0000144C	FF020304 05060708			750	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'		v2
00001454	090A0B0C 0D0E0F10							
0000145C	FF000000 00000001			751	DC	XL16'FF00000000000001 0101010101010102'		v3
00001464	01010101 01010102							
0000146C	FF020304 05060708			752	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'		v4
00001474	090A0B0C 0D0E0F10							
				753				
				754	* Halfword			
				755	VRR_D	VMALH,1		
00001480				756+	DS	0FD		
00001480		00001480		757+	USING	*,R5		base for test data and test routine
00001480	000014C8			758+T6	DC	A(X6)		address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001484	0006			759+	DC	H'6'		test number
00001486	00			760+	DC	X'00'		
00001487	01			761+	DC	HL1'1'		m5
00001488	E5D4C1D3 C8404040			762+	DC	CL8'VMALH'		instruction name
00001490	0000150C			763+	DC	A(RE6+16)		address of v2 source
00001494	0000151C			764+	DC	A(RE6+32)		address of v3 source
00001498	0000152C			765+	DC	A(RE6+48)		address of v4 source
0000149C	00000010			766+	DC	A(16)		result length
000014A0	000014FC			767+REA6	DC	A(RE6)		result address
000014A8	00000000 00000000			768+	DS	FD		gap
000014B0	00000000 00000000			769+V106	DS	XL16		V1 output
000014B8	00000000 00000000							
000014C0	00000000 00000000			770+	DS	FD		gap
				771+*				
000014C8				772+X6	DS	0F		
000014C8	E310 5010 0014		00000010	773+	LGF	R1,V2ADDR		load v2 source
000014CE	E761 0000 0806		00000000	774+	VL	v22,0(R1)		use v22 to test decoder
000014D4	E310 5014 0014		00000014	775+	LGF	R1,V3ADDR		load v3 source
000014DA	E771 0000 0806		00000000	776+	VL	v23,0(R1)		use v23 to test decoder
000014E0	E310 5018 0014		00000018	777+	LGF	R1,V4ADDR		load v4 source
000014E6	E781 0000 0806		00000000	778+	VL	v24,0(R1)		use v24 to test decoder
000014EC	E766 7100 8FA9			779+	VMALH V22,V22,V23,V24,1			test instruction (dest is a source)
000014F2	E760 5030 080E		000014B0	780+	VST	V22,V106		save v1 output
000014F8	07FB			781+	BR	R11		return
000014FC				782+RE6	DC	0F		xl16 expected result
000014FC				783+	DROP	R5		
000014FC	FE010000 00000000			784	DC	XL16'FE01000000000000 0000000000000000'		result
00001504	00000000 00000000							
0000150C	FF000000 00000019			785	DC	XL16'FF00000000000019 00000038000000FA'		v2
00001514	00000038 000000FA							
0000151C	FF000000 00000019			786	DC	XL16'FF00000000000019 00000038000000FA'		v3
00001524	00000038 000000FA							
0000152C	00000000 00000000			787	DC	XL16'0000000000000000 0000000000000000'		v4
00001534	00000000 00000000							
				788				
				789	VRR_D VMALH,1			
00001540				790+	DS	0FD		
00001540		00001540		791+	USING *,R5			base for test data and test routine
00001540	00001588			792+T7	DC	A(X7)		address of test routine
00001544	0007			793+	DC	H'7'		test number
00001546	00			794+	DC	X'00'		
00001547	01			795+	DC	HL1'1'		m5
00001548	E5D4C1D3 C8404040			796+	DC	CL8'VMALH'		instruction name
00001550	000015CC			797+	DC	A(RE7+16)		address of v2 source
00001554	000015DC			798+	DC	A(RE7+32)		address of v3 source
00001558	000015EC			799+	DC	A(RE7+48)		address of v4 source
0000155C	00000010			800+	DC	A(16)		result length
00001560	000015BC			801+REA7	DC	A(RE7)		result address
00001568	00000000 00000000			802+	DS	FD		gap
00001570	00000000 00000000			803+V107	DS	XL16		V1 output
00001578	00000000 00000000							
00001580	00000000 00000000			804+	DS	FD		gap
				805+*				
00001588				806+X7	DS	0F		
00001588	E310 5010 0014		00000010	807+	LGF	R1,V2ADDR		load v2 source
0000158E	E761 0000 0806		00000000	808+	VL	v22,0(R1)		use v22 to test decoder

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  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

00001594  E310 5014 0014             00000014  809+        LGF   R1,V3ADDR            load v3 source
0000159A  E771 0000 0806             00000000  810+        VL    v23,0(R1)            use v23 to test decoder
000015A0  E310 5018 0014             00000018  811+        LGF   R1,V4ADDR            load v4 source
000015A6  E781 0000 0806             00000000  812+        VL    v24,0(R1)            use v24 to test decoder
000015AC  E766 7100 8FA9                       813+        VMALH V22,V22,V23,V24,1     test instruction (dest is a source)
000015B2  E760 5030 080E             00001570  814+        VST   V22,V107              save v1 output
000015B8  07FB                                 815+        BR    R11                  return
000015BC                                       816+RE7     DC    0F                   xl16 expected result
000015BC                                       817+        DROP  R5
000015BC  FE010000 00000000                    818         DC    XL16'FE01000000000000 0000000000000000'   result
000015C4  00000000 00000000
000015CC  FF0000FF 00000029                    819         DC    XL16'FF0000FF00000029 00000038000000FA'   v2
000015D4  00000038 000000FA
000015DC  FF000001 00000029                    820         DC    XL16'FF00000100000029 00000038000000FA'   v3
000015E4  00000038 000000FA
000015EC  00000001 0000002F                    821         DC    XL16'000000010000002F 0000000000000002'   v4
000015F4  00000000 00000002
                                               822
                                               823         VRR_D VMALH,1
00001600                                       824+        DS    0FD
00001600                    00001600           825+        USING *,R5               base for test data and test routine
00001600  00001648                             826+T8      DC    A(X8)                address of test routine
00001604  0008                                 827+        DC    H'8'                 test number
00001606  00                                   828+        DC    X'00'
00001607  01                                   829+        DC    HL1'1'               m5
00001608  E5D4C1D3 C8404040                    830+        DC    CL8'VMALH'           instruction name
00001610  0000168C                             831+        DC    A(RE8+16)            address of v2 source
00001614  0000169C                             832+        DC    A(RE8+32)            address of v3 source
00001618  000016AC                             833+        DC    A(RE8+48)            address of v4 source
0000161C  00000010                             834+        DC    A(16)                result length
00001620  0000167C                             835+REA8    DC    A(RE8)               result address
00001628  00000000 00000000                    836+        DS    FD                   gap
00001630  00000000 00000000                    837+V108    DS    XL16                 V1 output
00001638  00000000 00000000
00001640  00000000 00000000                    838+        DS    FD                   gap
                                               839+*
00001648                                       840+X8      DS    0F
00001648  E310 5010 0014             00000010  841+        LGF   R1,V2ADDR            load v2 source
0000164E  E761 0000 0806             00000000  842+        VL    v22,0(R1)            use v22 to test decoder
00001654  E310 5014 0014             00000014  843+        LGF   R1,V3ADDR            load v3 source
0000165A  E771 0000 0806             00000000  844+        VL    v23,0(R1)            use v23 to test decoder
00001660  E310 5018 0014             00000018  845+        LGF   R1,V4ADDR            load v4 source
00001666  E781 0000 0806             00000000  846+        VL    v24,0(R1)            use v24 to test decoder
0000166C  E766 7100 8FA9                       847+        VMALH V22,V22,V23,V24,1     test instruction (dest is a source)
00001672  E760 5030 080E             00001630  848+        VST   V22,V108              save v1 output
00001678  07FB                                 849+        BR    R11                  return
0000167C                                       850+RE8     DC    0F                   xl16 expected result
0000167C                                       851+        DROP  R5
0000167C  FE050009 00190031                    852         DC    XL16'FE05000900190031 0051007A00AA00E2'   result
00001684  0051007A 00AA00E2
0000168C  FF020304 05060708                    853         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001694  090A0B0C 0D0E0F10
0000169C  FF020304 05060708                    854         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
000016A4  090A0B0C 0D0E0F10
000016AC  FF020304 05060708                    855         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000016B4  090A0B0C 0D0E0F10
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				856			
				857		VRR_D VMALH,1	
000016C0				858+	DS	0FD	
000016C0		000016C0		859+	USING	*,R5	base for test data and test routine
000016C0	00001708			860+T9	DC	A(X9)	address of test routine
000016C4	0009			861+	DC	H'9'	test number
000016C6	00			862+	DC	X'00'	
000016C7	01			863+	DC	HL1'1'	m5
000016C8	E5D4C1D3 C8404040			864+	DC	CL8'VMALH'	instruction name
000016D0	0000174C			865+	DC	A(RE9+16)	address of v2 source
000016D4	0000175C			866+	DC	A(RE9+32)	address of v3 source
000016D8	0000176C			867+	DC	A(RE9+48)	address of v4 source
000016DC	00000010			868+	DC	A(16)	result length
000016E0	0000173C			869+REA9	DC	A(RE9)	result address
000016E8	00000000 00000000			870+	DS	FD	gap
000016F0	00000000 00000000			871+V109	DS	XL16	V1 output
000016F8	00000000 00000000						
00001700	00000000 00000000			872+	DS	FD	gap
				873+*			
00001708				874+X9	DS	0F	
00001708	E310 5010 0014		00000010	875+	LGF	R1,V2ADDR	load v2 source
0000170E	E761 0000 0806		00000000	876+	VL	v22,0(R1)	use v22 to test decoder
00001714	E310 5014 0014		00000014	877+	LGF	R1,V3ADDR	load v3 source
0000171A	E771 0000 0806		00000000	878+	VL	v23,0(R1)	use v23 to test decoder
00001720	E310 5018 0014		00000018	879+	LGF	R1,V4ADDR	load v4 source
00001726	E781 0000 0806		00000000	880+	VL	v24,0(R1)	use v24 to test decoder
0000172C	E766 7100 8FA9			881+	VMALH V22,V22,V23,V24,1		test instruction (dest is a source)
00001732	E760 5030 080E		000016F0	882+	VST	V22,V109	save v1 output
00001738	07FB			883+	BR	R11	return
0000173C				884+RE9	DC	0F	xl16 expected result
0000173C				885+	DROP	R5	
0000173C	FE040003 000A0015			886	DC	XL16'FE040003000A0015 00240037004E0069'	result
00001744	00240037 004E0069						
0000174C	FF020304 05060708			887	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00001754	090A0B0C 0D0E0F10						
0000175C	FF010102 02030304			888	DC	XL16'FF01010202030304 0405050606070708'	v3
00001764	04050506 06070708						
0000176C	FF020304 05060708			889	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00001774	090A0B0C 0D0E0F10						
				890			
				891		VRR_D VMALH,1	
00001780				892+	DS	0FD	
00001780		00001780		893+	USING	*,R5	base for test data and test routine
00001780	000017C8			894+T10	DC	A(X10)	address of test routine
00001784	000A			895+	DC	H'10'	test number
00001786	00			896+	DC	X'00'	
00001787	01			897+	DC	HL1'1'	m5
00001788	E5D4C1D3 C8404040			898+	DC	CL8'VMALH'	instruction name
00001790	0000180C			899+	DC	A(RE10+16)	address of v2 source
00001794	0000181C			900+	DC	A(RE10+32)	address of v3 source
00001798	0000182C			901+	DC	A(RE10+48)	address of v4 source
0000179C	00000010			902+	DC	A(16)	result length
000017A0	000017FC			903+REA10	DC	A(RE10)	result address
000017A8	00000000 00000000			904+	DS	FD	gap
000017B0	00000000 00000000			905+V1010	DS	XL16	V1 output
000017B8	00000000 00000000						

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   LOC        OBJECT CODE      ADDR1     ADDR2     STMT

000017C0  00000000 00000000                       906+        DS    FD              gap
                                                  907+*
000017C8                                          908+X10     DS    0F
000017C8  E310 5010 0014                 00000010  909+        LGF   R1,V2ADDR       load v2 source
000017CE  E761 0000 0806                 00000000  910+        VL    v22,0(R1)       use v22 to test decoder
000017D4  E310 5014 0014                 00000014  911+        LGF   R1,V3ADDR       load v3 source
000017DA  E771 0000 0806                 00000000  912+        VL    v23,0(R1)       use v23 to test decoder
000017E0  E310 5018 0014                 00000018  913+        LGF   R1,V4ADDR       load v4 source
000017E6  E781 0000 0806                 00000000  914+        VL    v24,0(R1)       use v24 to test decoder
000017EC  E766 7100 8FA9                            915+        VMALH V22,V22,V23,V24,1    test instruction (dest is a source)
000017F2  E760 5030 080E                 000017B0  916+        VST   V22,V1010        save v1 output
000017F8  07FB                                     917+        BR    R11             return
000017FC                                           918+RE10    DC    0F              xl16 expected result
000017FC                                           919+        DROP  R5
000017FC  FE030000 00000000                        920         DC    XL16'FE03000000000000 0009000B000D000F'    result
00001804  0009000B 000D000F
0000180C  FF020304 05060708                        921         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00001814  090A0B0C 0D0E0F10
0000181C  FF000000 00000001                        922         DC    XL16'FF00000000000001 0101010101010102'    v3
00001824  01010101 01010102
0000182C  FF020304 05060708                        923         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00001834  090A0B0C 0D0E0F10

                                                  924
                                                  925 * Word
                                                  926         VRR_D VMALH,2
00001840                                           927+        DS    0FD
00001840                          00001840         928+        USING *,R5            base for test data and test routine
00001840  00001888                                 929+T11     DC    A(X11)          address of test routine
00001844  000B                                     930+        DC    H'11'           test number
00001846  00                                       931+        DC    X'00'
00001847  02                                       932+        DC    HL1'2'          m5
00001848  E5D4C1D3 C8404040                        933+        DC    CL8'VMALH'      instruction name
00001850  000018CC                                 934+        DC    A(RE11+16)      address of v2 source
00001854  000018DC                                 935+        DC    A(RE11+32)      address of v3 source
00001858  000018EC                                 936+        DC    A(RE11+48)      address of v4 source
0000185C  00000010                                 937+        DC    A(16)           result length
00001860  000018BC                                 938+REA11   DC    A(RE11)         result address
00001868  00000000 00000000                        939+        DS    FD              gap
00001870  00000000 00000000                        940+V1011   DS    XL16            V1 output
00001878  00000000 00000000
00001880  00000000 00000000                        941+        DS    FD              gap
                                                  942+*
00001888                                           943+X11     DS    0F
00001888  E310 5010 0014                 00000010  944+        LGF   R1,V2ADDR       load v2 source
0000188E  E761 0000 0806                 00000000  945+        VL    v22,0(R1)       use v22 to test decoder
00001894  E310 5014 0014                 00000014  946+        LGF   R1,V3ADDR       load v3 source
0000189A  E771 0000 0806                 00000000  947+        VL    v23,0(R1)       use v23 to test decoder
000018A0  E310 5018 0014                 00000018  948+        LGF   R1,V4ADDR       load v4 source
000018A6  E781 0000 0806                 00000000  949+        VL    v24,0(R1)       use v24 to test decoder
000018AC  E766 7200 8FA9                            950+        VMALH V22,V22,V23,V24,2    test instruction (dest is a source)
000018B2  E760 5030 080E                 00001870  951+        VST   V22,V1011        save v1 output
000018B8  07FB                                     952+        BR    R11             return
000018BC                                           953+RE11    DC    0F              xl16 expected result
000018BC                                           954+        DROP  R5
000018BC  FE010000 00000000                        955         DC    XL16'FE01000000000000 0000000000000000'    result
000018C4  00000000 00000000
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000018CC   FF000000 00000019               956          DC      XL16'FF00000000000019 00000038000000FA'    v2
000018D4   00000038 000000FA
000018DC   FF000000 00000019               957          DC      XL16'FF00000000000019 00000038000000FA'    v3
000018E4   00000038 000000FA
000018EC   00000000 00000000               958          DC      XL16'0000000000000000 0000000000000000'    v4
000018F4   00000000 00000000
                                           959
                                           960          VRR_D   VMALH,2
00001900                                   961+         DS      0FD
00001900                        00001900   962+         USING   *,R5                  base for test data and test routine
00001900   00001948                        963+T12      DC      A(X12)                address of test routine
00001904   000C                            964+         DC      H'12'                 test number
00001906   00                              965+         DC      X'00'
00001907   02                              966+         DC      HL1'2'                m5
00001908   E5D4C1D3 C8404040               967+         DC      CL8'VMALH'            instruction name
00001910   0000198C                        968+         DC      A(RE12+16)            address of v2 source
00001914   0000199C                        969+         DC      A(RE12+32)            address of v3 source
00001918   000019AC                        970+         DC      A(RE12+48)            address of v4 source
0000191C   00000010                        971+         DC      A(16)                 result length
00001920   0000197C                        972+REA12    DC      A(RE12)               result address
00001928   00000000 00000000               973+         DS      FD                    gap
00001930   00000000 00000000               974+V1012    DS      XL16                  V1 output
00001938   00000000 00000000
00001940   00000000 00000000               975+         DS      FD                    gap
                                           976+*
00001948                                   977+X12      DS      0F
00001948   E310 5010 0014       00000010   978+         LGF     R1,V2ADDR             load v2 source
0000194E   E761 0000 0806       00000000   979+         VL      v22,0(R1)             use v22 to test decoder
00001954   E310 5014 0014       00000014   980+         LGF     R1,V3ADDR             load v3 source
0000195A   E771 0000 0806       00000000   981+         VL      v23,0(R1)             use v23 to test decoder
00001960   E310 5018 0014       00000018   982+         LGF     R1,V4ADDR             load v4 source
00001966   E781 0000 0806       00000000   983+         VL      v24,0(R1)             use v24 to test decoder
0000196C   E766 7200 8FA9                  984+         VMALH   V22,V22,V23,V24,2       test instruction (dest is a source)
00001972   E760 5030 080E       00001930   985+         VST     V22,V1012              save v1 output
00001978   07FB                            986+         BR      R11                   return
0000197C                                   987+RE12     DC      0F                    xl16 expected result
0000197C                                   988+         DROP    R5
0000197C   FE0100FF 00000000               989          DC      XL16'FE0100FF00000000 0000000000000000'    result
00001984   00000000 00000000
0000198C   FF0000FF 00000029               990          DC      XL16'FF0000FF00000029 00000038000000FA'    v2
00001994   00000038 000000FA
0000199C   FF000001 00000029               991          DC      XL16'FF00000100000029 00000038000000FA'    v3
000019A4   00000038 000000FA
000019AC   00000001 0000002F               992          DC      XL16'000000010000002F 0000000000000002'    v4
000019B4   00000000 00000002
                                           993
                                           994          VRR_D   VMALH,2
000019C0                                   995+         DS      0FD
000019C0                        000019C0   996+         USING   *,R5                  base for test data and test routine
000019C0   00001A08                        997+T13      DC      A(X13)                address of test routine
000019C4   000D                            998+         DC      H'13'                 test number
000019C6   00                              999+         DC      X'00'
000019C7   02                              1000+        DC      HL1'2'                m5
000019C8   E5D4C1D3 C8404040               1001+        DC      CL8'VMALH'            instruction name
000019D0   00001A4C                        1002+        DC      A(RE13+16)            address of v2 source
000019D4   00001A5C                        1003+        DC      A(RE13+32)            address of v3 source
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   LOC        OBJECT CODE       ADDR1     ADDR2     STMT

 000019D8   00001A6C                              1004+        DC      A(RE13+48)       address of v4 source
 000019DC   00000010                              1005+        DC      A(16)            result length
 000019E0   00001A3C                              1006+REA13   DC      A(RE13)          result address
 000019E8   00000000 00000000                     1007+        DS      FD               gap
 000019F0   00000000 00000000                     1008+V1013   DS      XL16             V1 output
 000019F8   00000000 00000000
 00001A00   00000000 00000000                     1009+        DS      FD               gap
                                                  1010+*
 00001A08                                         1011+X13     DS      0F
 00001A08   E310 5010 0014              00000010   1012+        LGF     R1,V2ADDR        load v2 source
 00001A0E   E761 0000 0806              00000000   1013+        VL      v22,0(R1)        use v22 to test decoder
 00001A14   E310 5014 0014              00000014   1014+        LGF     R1,V3ADDR        load v3 source
 00001A1A   E771 0000 0806              00000000   1015+        VL      v23,0(R1)        use v23 to test decoder
 00001A20   E310 5018 0014              00000018   1016+        LGF     R1,V4ADDR        load v4 source
 00001A26   E781 0000 0806              00000000   1017+        VL      v24,0(R1)        use v24 to test decoder
 00001A2C   E766 7200 8FA9                         1018+        VMALH   V22,V22,V23,V24,2   test instruction (dest is a source)
 00001A32   E760 5030 080E              000019F0   1019+        VST     V22,V1013           save v1 output
 00001A38   07FB                                   1020+        BR      R11              return
 00001A3C                                          1021+RE13    DC      0F               xl16 expected result
 00001A3C                                          1022+        DROP    R5
 00001A3C   FE050207 00193C6A                      1023         DC      XL16'FE05020700193C6A 0051B52B00AA6E4D'     result
 00001A44   0051B52B 00AA6E4D
 00001A4C   FF020304 05060708                      1024         DC      XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
 00001A54   090A0B0C 0D0E0F10
 00001A5C   FF020304 05060708                      1025         DC      XL16'FF02030405060708 090A0B0C0D0E0F10'     v3
 00001A64   090A0B0C 0D0E0F10
 00001A6C   FF020304 05060708                      1026         DC      XL16'FF02030405060708 090A0B0C0D0E0F10'     v4
 00001A74   090A0B0C 0D0E0F10

                                                  1027
                                                  1028         VRR_D   VMALH,2
 00001A80                                          1029+        DS      0FD
 00001A80                         00001A80         1030+        USING   *,R5             base for test data and test routine
 00001A80   00001AC8                               1031+T14     DC      A(X14)           address of test routine
 00001A84   000E                                   1032+        DC      H'14'            test number
 00001A86   00                                     1033+        DC      X'00'
 00001A87   02                                     1034+        DC      HL1'2'           m5
 00001A88   E5D4C1D3 C8404040                      1035+        DC      CL8'VMALH'       instruction name
 00001A90   00001B0C                               1036+        DC      A(RE14+16)       address of v2 source
 00001A94   00001B1C                               1037+        DC      A(RE14+32)       address of v3 source
 00001A98   00001B2C                               1038+        DC      A(RE14+48)       address of v4 source
 00001A9C   00000010                               1039+        DC      A(16)            result length
 00001AA0   00001AFC                               1040+REA14   DC      A(RE14)          result address
 00001AA8   00000000 00000000                      1041+        DS      FD               gap
 00001AB0   00000000 00000000                      1042+V1014   DS      XL16             V1 output
 00001AB8   00000000 00000000
 00001AC0   00000000 00000000                      1043+        DS      FD               gap
                                                  1044+*
 00001AC8                                          1045+X14     DS      0F
 00001AC8   E310 5010 0014              00000010   1046+        LGF     R1,V2ADDR        load v2 source
 00001ACE   E761 0000 0806              00000000   1047+        VL      v22,0(R1)        use v22 to test decoder
 00001AD4   E310 5014 0014              00000014   1048+        LGF     R1,V3ADDR        load v3 source
 00001ADA   E771 0000 0806              00000000   1049+        VL      v23,0(R1)        use v23 to test decoder
 00001AE0   E310 5018 0014              00000018   1050+        LGF     R1,V4ADDR        load v4 source
 00001AE6   E781 0000 0806              00000000   1051+        VL      v24,0(R1)        use v24 to test decoder
 00001AEC   E766 7200 8FA9                         1052+        VMALH   V22,V22,V23,V24,2   test instruction (dest is a source)
 00001AF2   E760 5030 080E              00001AB0   1053+        VST     V22,V1014           save v1 output
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001AF8	07FB			1054+	BR	R11	return	
00001AFC				1055+RE14	DC	0F	xl16 expected result	
00001AFC				1056+	DROP	R5		
00001AFC	FE040104 000A1B2F			1057	DC	XL16'FE040104000A1B2F 0024558B004EB018'	result
00001B04	0024558B 004EB018							
00001B0C	FF020304 05060708			1058	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00001B14	090A0B0C 0D0E0F10							
00001B1C	FF010102 02030304			1059	DC	XL16'FF01010202030304 0405050606070708'	v3
00001B24	04050506 06070708							
00001B2C	FF020304 05060708			1060	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00001B34	090A0B0C 0D0E0F10							
				1061				
				1062	VRR_D	VMALH, 2		
00001B40				1063+	DS	0FD		
00001B40		00001B40		1064+	USING	*,R5	base for test data and test routine	
00001B40	00001B88			1065+T15	DC	A(X15)	address of test routine	
00001B44	000F			1066+	DC	H'15'	test number	
00001B46	00			1067+	DC	X'00'		
00001B47	02			1068+	DC	HL1'2'	m5	
00001B48	E5D4C1D3 C8404040			1069+	DC	CL8'VMALH'	instruction name	
00001B50	00001BCC			1070+	DC	A(RE15+16)	address of v2 source	
00001B54	00001BDC			1071+	DC	A(RE15+32)	address of v3 source	
00001B58	00001BEC			1072+	DC	A(RE15+48)	address of v4 source	
00001B5C	00000010			1073+	DC	A(16)	result length	
00001B60	00001BBC			1074+REA15	DC	A(RE15)	result address	
00001B68	00000000 00000000			1075+	DS	FD	gap	
00001B70	00000000 00000000			1076+V1015	DS	XL16	V1 output	
00001B78	00000000 00000000							
00001B80	00000000 00000000			1077+	DS	FD	gap	
				1078+*				
00001B88				1079+X15	DS	0F		
00001B88	E310 5010 0014		00000010	1080+	LGF	R1,V2ADDR	load v2 source	
00001B8E	E761 0000 0806		00000000	1081+	VL	v22,0(R1)	use v22 to test decoder	
00001B94	E310 5014 0014		00000014	1082+	LGF	R1,V3ADDR	load v3 source	
00001B9A	E771 0000 0806		00000000	1083+	VL	v23,0(R1)	use v23 to test decoder	
00001BA0	E310 5018 0014		00000018	1084+	LGF	R1,V4ADDR	load v4 source	
00001BA6	E781 0000 0806		00000000	1085+	VL	v24,0(R1)	use v24 to test decoder	
00001BAC	E766 7200 8FA9			1086+	VMALH	V22,V22,V23,V24,2	test instruction (dest is a source)	
00001BB2	E760 5030 080E		00001B70	1087+	VST	V22,V1015	save v1 output	
00001BB8	07FB			1088+	BR	R11	return	
00001BBC				1089+RE15	DC	0F	xl16 expected result	
00001BBC				1090+	DROP	R5		
00001BBC	FE030101 00000000			1091	DC	XL16'FE03010100000000 0009131E000D1B2A'	result
00001BC4	0009131E 000D1B2A							
00001BCC	FF020304 05060708			1092	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00001BD4	090A0B0C 0D0E0F10							
00001BDC	FF000000 00000001			1093	DC	XL16'FF00000000000001 0101010101010102'	v3
00001BE4	01010101 01010102							
00001BEC	FF020304 05060708			1094	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00001BF4	090A0B0C 0D0E0F10							
				1095				
				1096	* Doubleword			
				1097	VRR_D	VMALH, 3		
00001C00				1098+	DS	0FD		
00001C00		00001C00		1099+	USING	*,R5	base for test data and test routine	
00001C00	00001C48			1100+T16	DC	A(X16)	address of test routine	

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  LOC          OBJECT CODE       ADDR1     ADDR2      STMT

00001C04  0010                                        1101+         DC    H'16'              test number
00001C06  00                                          1102+         DC    X'00'
00001C07  03                                          1103+         DC    HL1'3'             m5
00001C08  E5D4C1D3 C8404040                            1104+         DC    CL8'VMALH'         instruction name
00001C10  00001C8C                                    1105+         DC    A(RE16+16)         address of v2 source
00001C14  00001C9C                                    1106+         DC    A(RE16+32)         address of v3 source
00001C18  00001CAC                                    1107+         DC    A(RE16+48)         address of v4 source
00001C1C  00000010                                    1108+         DC    A(16)              result length
00001C20  00001C7C                                    1109+REA16     DC    A(RE16)            result address
00001C28  00000000 00000000                           1110+         DS    FD                 gap
00001C30  00000000 00000000                           1111+V1016     DS    XL16               V1 output
00001C38  00000000 00000000
00001C40  00000000 00000000                           1112+         DS    FD                 gap
                                                      1113+*
00001C48                                              1114+X16       DS    0F
00001C48  E310 5010 0014                  00000010    1115+         LGF   R1,V2ADDR          load v2 source
00001C4E  E761 0000 0806                  00000000    1116+         VL    v22,0(R1)          use v22 to test decoder
00001C54  E310 5014 0014                  00000014    1117+         LGF   R1,V3ADDR          load v3 source
00001C5A  E771 0000 0806                  00000000    1118+         VL    v23,0(R1)          use v23 to test decoder
00001C60  E310 5018 0014                  00000018    1119+         LGF   R1,V4ADDR          load v4 source
00001C66  E781 0000 0806                  00000000    1120+         VL    v24,0(R1)          use v24 to test decoder
00001C6C  E766 7300 8FA9                              1121+         VMALH V22,V22,V23,V24,3     test instruction (dest is a source)
00001C72  E760 5030 080E                  00001C30    1122+         VST   V22,V1016            save v1 output
00001C78  07FB                                        1123+         BR    R11                return
00001C7C                                              1124+RE16      DC    0F                 xl16 expected result
00001C7C                                              1125+         DROP  R5
00001C7C  FFFFFFFE 00032000                           1126          DC    XL16'FFFFFFFE00032000 0000000000000C77'     result
00001C84  00000000 00000C77
00001C8C  FFFFFFFF 00019000                           1127          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'     v2
00001C94  00000038 EEEEEEFA
00001C9C  FFFFFFFF 00019000                           1128          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'     v3
00001CA4  00000038 0EEEEEFA
00001CAC  00000000 00000000                           1129          DC    XL16'0000000000000000 0000000000000000'     v4
00001CB4  00000000 00000000
                                                      1130
                                                      1131          VRR_D VMALH,3
00001CC0                                              1132+         DS    0FD
00001CC0                             00001CC0          1133+         USING *,R5                base for test data and test routine
00001CC0  00001D08                                    1134+T17       DC    A(X17)             address of test routine
00001CC4  0011                                        1135+         DC    H'17'              test number
00001CC6  00                                          1136+         DC    X'00'
00001CC7  03                                          1137+         DC    HL1'3'             m5
00001CC8  E5D4C1D3 C8404040                            1138+         DC    CL8'VMALH'         instruction name
00001CD0  00001D4C                                    1139+         DC    A(RE17+16)         address of v2 source
00001CD4  00001D5C                                    1140+         DC    A(RE17+32)         address of v3 source
00001CD8  00001D6C                                    1141+         DC    A(RE17+48)         address of v4 source
00001CDC  00000010                                    1142+         DC    A(16)              result length
00001CE0  00001D3C                                    1143+REA17     DC    A(RE17)            result address
00001CE8  00000000 00000000                           1144+         DS    FD                 gap
00001CF0  00000000 00000000                           1145+V1017     DS    XL16               V1 output
00001CF8  00000000 00000000
00001D00  00000000 00000000                           1146+         DS    FD                 gap
                                                      1147+*
00001D08                                              1148+X17       DS    0F
00001D08  E310 5010 0014                  00000010    1149+         LGF   R1,V2ADDR          load v2 source
00001D0E  E761 0000 0806                  00000000    1150+         VL    v22,0(R1)          use v22 to test decoder
```

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  LOC         OBJECT CODE      ADDR1    ADDR2    STMT

00001D14   E310 5014 0014             00000014  1151+         LGF   R1,V3ADDR          load v3 source
00001D1A   E771 0000 0806             00000000  1152+         VL    v23,0(R1)          use v23 to test decoder
00001D20   E310 5018 0014             00000018  1153+         LGF   R1,V4ADDR          load v4 source
00001D26   E781 0000 0806             00000000  1154+         VL    v24,0(R1)          use v24 to test decoder
00001D2C   E766 7300 8FA9                       1155+         VMALH V22,V22,V23,V24,3     test instruction (dest is a source)
00001D32   E760 5030 080E             00001CF0  1156+         VST   V22,V1017            save v1 output
00001D38   07FB                                 1157+         BR    R11                return
00001D3C                                        1158+RE17     DC    0F                 xl16 expected result
00001D3C                                        1159+         DROP  R5
00001D3C   01010308 111F3397                    1160          DC    XL16'01010308111F3397 0051B52F8692B4F6'      result
00001D44   0051B52F 8692B4F6
00001D4C   FF020304 05060750                    1161          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'      v2
00001D54   090A0B0C 0D0E0F7F
00001D5C   01020304 05060750                    1162          DC    XL16'0102030405060750 090A0B780D0E0F7F'      v3
00001D64   090A0B78 0D0E0F7F
00001D6C   FF000000 00000000                    1163          DC    XL16'FF00000000000000 2000000000000000'      v4
00001D74   20000000 00000000
                                                1164
                                                1165          VRR_D VMALH,3
00001D80                                        1166+         DS    0FD
00001D80                       00001D80         1167+         USING *,R5                base for test data and test routine
00001D80   00001DC8                             1168+T18      DC    A(X18)              address of test routine
00001D84   0012                                 1169+         DC    H'18'               test number
00001D86   00                                   1170+         DC    X'00'
00001D87   03                                   1171+         DC    HL1'3'              m5
00001D88   E5D4C1D3 C8404040                    1172+         DC    CL8'VMALH'          instruction name
00001D90   00001E0C                             1173+         DC    A(RE18+16)          address of v2 source
00001D94   00001E1C                             1174+         DC    A(RE18+32)          address of v3 source
00001D98   00001E2C                             1175+         DC    A(RE18+48)          address of v4 source
00001D9C   00000010                             1176+         DC    A(16)               result length
00001DA0   00001DFC                             1177+REA18    DC    A(RE18)             result address
00001DA8   00000000 00000000                    1178+         DS    FD                  gap
00001DB0   00000000 00000000                    1179+V1018    DS    XL16                V1 output
00001DB8   00000000 00000000
00001DC0   00000000 00000000                    1180+         DS    FD                  gap
                                                1181+*
00001DC8                                        1182+X18      DS    0F
00001DC8   E310 5010 0014             00000010  1183+         LGF   R1,V2ADDR          load v2 source
00001DCE   E761 0000 0806             00000000  1184+         VL    v22,0(R1)          use v22 to test decoder
00001DD4   E310 5014 0014             00000014  1185+         LGF   R1,V3ADDR          load v3 source
00001DDA   E771 0000 0806             00000000  1186+         VL    v23,0(R1)          use v23 to test decoder
00001DE0   E310 5018 0014             00000018  1187+         LGF   R1,V4ADDR          load v4 source
00001DE6   E781 0000 0806             00000000  1188+         VL    v24,0(R1)          use v24 to test decoder
00001DEC   E766 7300 8FA9                       1189+         VMALH V22,V22,V23,V24,3     test instruction (dest is a source)
00001DF2   E760 5030 080E             00001DB0  1190+         VST   V22,V1018            save v1 output
00001DF8   07FB                                 1191+         BR    R11                return
00001DFC                                        1192+RE18     DC    0F                 xl16 expected result
00001DFC                                        1193+         DROP  R5
00001DFC   00010003 050C1344                    1194          DC    XL16'00010003050C1344 0024558DB838C863'      result
00001E04   0024558D B838C863
00001E0C   FF020304 05060750                    1195          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'      v2
00001E14   090A0B0C 0D0E0F7F
00001E1C   00010102 02030328                    1196          DC    XL16'0001010202030328 0405053C0607073F'      v3
00001E24   0405053C 0607073F
00001E2C   7FFFFFFF FFFFFFFF                     1197          DC    XL16'7FFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'      v4
00001E34   FFFFFFFF FFFFFFFF
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  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

                                                    1198
                                                    1199              VRR_D VMALH,3
00001E40                                            1200+             DS    0FD
00001E40                                 00001E40   1201+             USING *,R5                base for test data and test routine
00001E40    00001E88                                1202+T19          DC    A(X19)              address of test routine
00001E44    0013                                    1203+             DC    H'19'               test number
00001E46    00                                      1204+             DC    X'00'
00001E47    03                                      1205+             DC    HL1'3'              m5
00001E48    E5D4C1D3 C8404040                        1206+             DC    CL8'VMALH'          instruction name
00001E50    00001ECC                                1207+             DC    A(RE19+16)          address of v2 source
00001E54    00001EDC                                1208+             DC    A(RE19+32)          address of v3 source
00001E58    00001EEC                                1209+             DC    A(RE19+48)          address of v4 source
00001E5C    00000010                                1210+             DC    A(16)               result length
00001E60    00001EBC                                1211+REA19        DC    A(RE19)             result address
00001E68    00000000 00000000                        1212+             DS    FD                  gap
00001E70    00000000 00000000                        1213+V1019        DS    XL16                V1 output
00001E78    00000000 00000000
00001E80    00000000 00000000                        1214+             DS    FD                  gap
                                                    1215+*
00001E88                                            1216+X19          DS    0F
00001E88    E310 5010 0014                00000010   1217+             LGF   R1,V2ADDR           load v2 source
00001E8E    E761 0000 0806                00000000   1218+             VL    v22,0(R1)           use v22 to test decoder
00001E94    E310 5014 0014                00000014   1219+             LGF   R1,V3ADDR           load v3 source
00001E9A    E771 0000 0806                00000000   1220+             VL    v23,0(R1)           use v23 to test decoder
00001EA0    E310 5018 0014                00000018   1221+             LGF   R1,V4ADDR           load v4 source
00001EA6    E781 0000 0806                00000000   1222+             VL    v24,0(R1)           use v24 to test decoder
00001EAC    E766 7300 8FA9                          1223+             VMALH V22,V22,V23,V24,3    test instruction (dest is a source)
00001EB2    E760 5030 080E                00001E70   1224+             VST   V22,V1019           save v1 output
00001EB8    07FB                                    1225+             BR    R11                 return
00001EBC                                            1226+RE19         DC    0F                  xl16 expected result
00001EBC                                            1227+             DROP  R5
00001EBC    00000000 0000000A                        1228              DC    XL16'000000000000000A 0009131EA8C3DFFE'    result
00001EC4    0009131E A8C3DFFE
00001ECC    FF020304 05060750                        1229              DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00001ED4    090A0B0C 0D0E0F7F
00001EDC    00000000 0000000A                        1230              DC    XL16'000000000000000A 0101010F0101010F'    v3
00001EE4    0101010F 0101010F
00001EEC    FFFFFFFF FFFFFFFF                        1231              DC    XL16'FFFFFFFFFFFFFFFF 7FFFFFFFFFFFFFFF'    v4
00001EF4    7FFFFFFF FFFFFFFF
                                                    1232
                                                    1233 * Quadword
                                                    1234              VRR_D VMALH,4
00001F00                                            1235+             DS    0FD
00001F00                                 00001F00   1236+             USING *,R5                base for test data and test routine
00001F00    00001F48                                1237+T20          DC    A(X20)              address of test routine
00001F04    0014                                    1238+             DC    H'20'               test number
00001F06    00                                      1239+             DC    X'00'
00001F07    04                                      1240+             DC    HL1'4'              m5
00001F08    E5D4C1D3 C8404040                        1241+             DC    CL8'VMALH'          instruction name
00001F10    00001F8C                                1242+             DC    A(RE20+16)          address of v2 source
00001F14    00001F9C                                1243+             DC    A(RE20+32)          address of v3 source
00001F18    00001FAC                                1244+             DC    A(RE20+48)          address of v4 source
00001F1C    00000010                                1245+             DC    A(16)               result length
00001F20    00001F7C                                1246+REA20        DC    A(RE20)             result address
00001F28    00000000 00000000                        1247+             DS    FD                  gap
00001F30    00000000 00000000                        1248+V1020        DS    XL16                V1 output
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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00001F38   00000000 00000000
00001F40   00000000 00000000              1249+           DS      FD                     gap
                                          1250+*
00001F48                                  1251+X20        DS      0F
00001F48   E310 5010 0014           00000010  1252+        LGF     R1,V2ADDR              load v2 source
00001F4E   E761 0000 0806           00000000  1253+        VL      v22,0(R1)              use v22 to test decoder
00001F54   E310 5014 0014           00000014  1254+        LGF     R1,V3ADDR              load v3 source
00001F5A   E771 0000 0806           00000000  1255+        VL      v23,0(R1)              use v23 to test decoder
00001F60   E310 5018 0014           00000018  1256+        LGF     R1,V4ADDR              load v4 source
00001F66   E781 0000 0806           00000000  1257+        VL      v24,0(R1)              use v24 to test decoder
00001F6C   E766 7400 8FA9                1258+           VMALH   V22,V22,V23,V24,4    test instruction (dest is a source)
00001F72   E760 5030 080E           00001F30  1259+        VST     V22,V1020             save v1 output
00001F78   07FB                         1260+           BR      R11                    return
00001F7C                                 1261+RE20        DC      0F                     xl16 expected result
00001F7C                                 1262+           DROP    R5
00001F7C   FFFFFFFE 00032000            1263            DC      XL16'FFFFFFFE00032000 FFFCE0736EDDDD83'    result
00001F84   FFFCE073 6EDDDD83
00001F8C   FFFFFFFF 00019000            1264            DC      XL16'FFFFFFFF00019000 00000038EEEEEEFA'    v2
00001F94   00000038 EEEEEEFA
00001F9C   FFFFFFFF 00019000            1265            DC      XL16'FFFFFFFF00019000 000000380EEEEEFA'    v3
00001FA4   00000038 0EEEEEFA
00001FAC   00000000 00000000            1266            DC      XL16'0000000000000000 0000000000000000'    v4
00001FB4   00000000 00000000
                                         1267
                                         1268            VRR_D   VMALH,4
00001FC0                                 1269+           DS      0FD
00001FC0                      00001FC0   1270+           USING   *,R5                   base for test data and test routine
00001FC0   00002008                      1271+T21        DC      A(X21)                 address of test routine
00001FC4   0015                          1272+           DC      H'21'                  test number
00001FC6   00                            1273+           DC      X'00'
00001FC7   04                            1274+           DC      HL1'4'                 m5
00001FC8   E5D4C1D3 C8404040            1275+           DC      CL8'VMALH'             instruction name
00001FD0   0000204C                      1276+           DC      A(RE21+16)             address of v2 source
00001FD4   0000205C                      1277+           DC      A(RE21+32)             address of v3 source
00001FD8   0000206C                      1278+           DC      A(RE21+48)             address of v4 source
00001FDC   00000010                      1279+           DC      A(16)                  result length
00001FE0   0000203C                      1280+REA21      DC      A(RE21)                result address
00001FE8   00000000 00000000            1281+           DS      FD                     gap
00001FF0   00000000 00000000            1282+V1021       DS      XL16                   V1 output
00001FF8   00000000 00000000
00002000   00000000 00000000            1283+           DS      FD                     gap
                                         1284+*
00002008                                 1285+X21        DS      0F
00002008   E310 5010 0014           00000010  1286+        LGF     R1,V2ADDR              load v2 source
0000200E   E761 0000 0806           00000000  1287+        VL      v22,0(R1)              use v22 to test decoder
00002014   E310 5014 0014           00000014  1288+        LGF     R1,V3ADDR              load v3 source
0000201A   E771 0000 0806           00000000  1289+        VL      v23,0(R1)              use v23 to test decoder
00002020   E310 5018 0014           00000018  1290+        LGF     R1,V4ADDR              load v4 source
00002026   E781 0000 0806           00000000  1291+        VL      v24,0(R1)              use v24 to test decoder
0000202C   E766 7400 8FA9                1292+           VMALH   V22,V22,V23,V24,4    test instruction (dest is a source)
00002032   E760 5030 080E           00001FF0  1293+        VST     V22,V1021             save v1 output
00002038   07FB                         1294+           BR      R11                    return
0000203C                                 1295+RE21        DC      0F                     xl16 expected result
0000203C                                 1296+           DROP    R5
0000203C   01010308 111F3396            1297            DC      XL16'01010308111F3396 72BF86C3CAFA7484'    result
00002044   72BF86C3 CAFA7484
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  LOC        OBJECT CODE     ADDR1    ADDR2    STMT

0000204C  FF020304 05060750                  1298         DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'      v2
00002054  090A0B0C 0D0E0F7F
0000205C  01020304 05060750                  1299         DC     XL16'0102030405060750 090A0B780D0E0F7F'      v3
00002064  090A0B78 0D0E0F7F
0000206C  FF000000 00000000                  1300         DC     XL16'FF00000000000000 2000000000000000'      v4
00002074  20000000 00000000
                                             1301
                                             1302         VRR_D VMALH,4
00002080                                     1303+        DS     0FD
00002080                     00002080        1304+        USING *,R5                base for test data and test routine
00002080  000020C8                           1305+T22     DC     A(X22)              address of test routine
00002084  0016                               1306+        DC     H'22'               test number
00002086  00                                 1307+        DC     X'00'
00002087  04                                 1308+        DC     HL1'4'                                        m5
00002088  E5D4C1D3 C8404040                  1309+        DC     CL8'VMALH'          instruction name
00002090  0000210C                           1310+        DC     A(RE22+16)          address of v2 source
00002094  0000211C                           1311+        DC     A(RE22+32)          address of v3 source
00002098  0000212C                           1312+        DC     A(RE22+48)          address of v4 source
0000209C  00000010                           1313+        DC     A(16)               result length
000020A0  000020FC                           1314+REA22   DC     A(RE22)             result address
000020A8  00000000 00000000                  1315+        DS     FD                  gap
000020B0  00000000 00000000                  1316+V1022   DS     XL16                V1 output
000020B8  00000000 00000000
000020C0  00000000 00000000                  1317+        DS     FD                  gap
                                             1318+*
000020C8                                     1319+X22     DS     0F
000020C8  E310 5010 0014          00000010   1320+        LGF    R1,V2ADDR           load v2 source
000020CE  E761 0000 0806          00000000   1321+        VL     v22,0(R1)           use v22 to test decoder
000020D4  E310 5014 0014          00000014   1322+        LGF    R1,V3ADDR           load v3 source
000020DA  E771 0000 0806          00000000   1323+        VL     v23,0(R1)           use v23 to test decoder
000020E0  E310 5018 0014          00000018   1324+        LGF    R1,V4ADDR           load v4 source
000020E6  E781 0000 0806          00000000   1325+        VL     v24,0(R1)           use v24 to test decoder
000020EC  E766 7400 8FA9                     1326+        VMALH V22,V22,V23,V24,4    test instruction (dest is a source)
000020F2  E760 5030 080E          000020B0   1327+        VST    V22,V1022            save v1 output
000020F8  07FB                               1328+        BR     R11                 return
000020FC                                     1329+RE22    DC     0F                  xl16 expected result
000020FC                                     1330+        DROP   R5
000020FC  00010003 050C1344                  1331         DC     XL16'00010003050C1344 0AD40FD0ABE579A2'      result
00002104  0AD40FD0 ABE579A2
0000210C  FF020304 05060750                  1332         DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'      v2
00002114  090A0B0C 0D0E0F7F
0000211C  00010102 02030328                  1333         DC     XL16'0001010202030328 0405053C0607073F'      v3
00002124  0405053C 0607073F
0000212C  7FFFFFFF FFFFFFFF                   1334         DC     XL16'7FFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'      v4
00002134  FFFFFFFF FFFFFFFF
                                             1335
                                             1336         VRR_D VMALH,4
00002140                                     1337+        DS     0FD
00002140                     00002140        1338+        USING *,R5                base for test data and test routine
00002140  00002188                           1339+T23     DC     A(X23)              address of test routine
00002144  0017                               1340+        DC     H'23'               test number
00002146  00                                 1341+        DC     X'00'
00002147  04                                 1342+        DC     HL1'4'                                        m5
00002148  E5D4C1D3 C8404040                  1343+        DC     CL8'VMALH'          instruction name
00002150  000021CC                           1344+        DC     A(RE23+16)          address of v2 source
00002154  000021DC                           1345+        DC     A(RE23+32)          address of v3 source
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  LOC        OBJECT CODE        ADDR1      ADDR2      STMT

00002158   000021EC                                  1346+          DC      A(RE23+48)         address of v4 source
0000215C   00000010                                  1347+          DC      A(16)              result length
00002160   000021BC                                  1348+REA23     DC      A(RE23)            result address
00002168   00000000 00000000                         1349+          DS      FD                 gap
00002170   00000000 00000000                         1350+V1023     DS      XL16               V1 output
00002178   00000000 00000000
00002180   00000000 00000000                         1351+          DS      FD                 gap
                                                     1352+*
00002188                                             1353+X23       DS      0F
00002188   E310 5010 0014                 00000010   1354+          LGF     R1,V2ADDR          load v2 source
0000218E   E761 0000 0806                 00000000   1355+          VL      v22,0(R1)          use v22 to test decoder
00002194   E310 5014 0014                 00000014   1356+          LGF     R1,V3ADDR          load v3 source
0000219A   E771 0000 0806                 00000000   1357+          VL      v23,0(R1)          use v23 to test decoder
000021A0   E310 5018 0014                 00000018   1358+          LGF     R1,V4ADDR          load v4 source
000021A6   E781 0000 0806                 00000000   1359+          VL      v24,0(R1)          use v24 to test decoder
000021AC   E766 7400 8FA9                             1360+          VMALH   V22,V22,V23,V24,4    test instruction (dest is a source)
000021B2   E760 5030 080E                 00002170   1361+          VST     V22,V1023            save v1 output
000021B8   07FB                                       1362+          BR      R11                return
000021BC                                              1363+RE23      DC      0F                 xl16 expected result
000021BC                                              1364+          DROP    R5
000021BC   00000000 00000009                          1365           DC      XL16'0000000000000009 F714203B2D668782'    result
000021C4   F714203B 2D668782
000021CC   FF020304 05060750                          1366           DC      XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
000021D4   090A0B0C 0D0E0F7F
000021DC   00000000 0000000A                          1367           DC      XL16'000000000000000A 0101010F0101010F'    v3
000021E4   0101010F 0101010F
000021EC   FFFFFFFF FFFFFFFF                          1368           DC      XL16'FFFFFFFFFFFFFFFF 7FFFFFFFFFFFFFFF'    v4
000021F4   7FFFFFFF FFFFFFFF

                                                     1369
                                                     1370 *-------------------------------------------------------------------------
                                                     1371 *   VMAL   - Vector Multiply and Add Low
                                                     1372 *-------------------------------------------------------------------------
                                                     1373 * Byte
                                                     1374           VRR_D  VMAL,0
00002200                                             1375+          DS      0FD
00002200                             00002200         1376+          USING   *,R5               base for test data and test routine
00002200   00002248                                  1377+T24       DC      A(X24)             address of test routine
00002204   0018                                      1378+          DC      H'24'              test number
00002206   00                                        1379+          DC      X'00'
00002207   00                                        1380+          DC      HL1'0'             m5
00002208   E5D4C1D3 40404040                          1381+          DC      CL8'VMAL'          instruction name
00002210   0000228C                                  1382+          DC      A(RE24+16)         address of v2 source
00002214   0000229C                                  1383+          DC      A(RE24+32)         address of v3 source
00002218   000022AC                                  1384+          DC      A(RE24+48)         address of v4 source
0000221C   00000010                                  1385+          DC      A(16)              result length
00002220   0000227C                                  1386+REA24     DC      A(RE24)            result address
00002228   00000000 00000000                         1387+          DS      FD                 gap
00002230   00000000 00000000                         1388+V1024     DS      XL16               V1 output
00002238   00000000 00000000
00002240   00000000 00000000                         1389+          DS      FD                 gap
                                                     1390+*
00002248                                             1391+X24       DS      0F
00002248   E310 5010 0014                 00000010   1392+          LGF     R1,V2ADDR          load v2 source
0000224E   E761 0000 0806                 00000000   1393+          VL      v22,0(R1)          use v22 to test decoder
00002254   E310 5014 0014                 00000014   1394+          LGF     R1,V3ADDR          load v3 source
0000225A   E771 0000 0806                 00000000   1395+          VL      v23,0(R1)          use v23 to test decoder
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002260	E310 5018 0014		00000018	1396+	LGF	R1, V4ADDR	load v4 source
00002266	E781 0000 0806		00000000	1397+	VL	v24, 0(R1)	use v24 to test decoder
0000226C	E766 7000 8FAA			1398+	VMAL	V22, V22, V23, V24, 0	test instruction (dest is a source)
00002272	E760 A030 080E		00002230	1399+	VST	V22, V1024	save v1 output
00002278	07FB			1400+	BR	R11	return
0000227C				1401+RE24	DC	0F	xl16 expected result
0000227C				1402+	DROP	R5	
0000227C	01000000 00000071			1403	DC	XL16' 010000000000071 0000004000000024'	result
00002284	00000040 00000024						
0000228C	FF000000 00000019			1404	DC	XL16' FF00000000000019 00000038000000FA'	v2
00002294	00000038 000000FA						
0000229C	FF000000 00000019			1405	DC	XL16' FF00000000000019 00000038000000FA'	v3
000022A4	00000038 000000FA						
000022AC	00000000 00000000			1406	DC	XL16' 0000000000000000 0000000000000000'	v4
000022B4	00000000 00000000						
				1407			
				1408	VRR_D	VMAL, 0	
000022C0				1409+	DS	0FD	
000022C0		000022C0		1410+	USING	*, R5	base for test data and test routine
000022C0	00002308			1411+T25	DC	A(X25)	address of test routine
000022C4	0019			1412+	DC	H' 25'	test number
000022C6	00			1413+	DC	X' 00'	
000022C7	00			1414+	DC	HL1' 0'	m5
000022C8	E5D4C1D3 40404040			1415+	DC	CL8' VMAL'	instruction name
000022D0	0000234C			1416+	DC	A(RE25+16)	address of v2 source
000022D4	0000235C			1417+	DC	A(RE25+32)	address of v3 source
000022D8	0000236C			1418+	DC	A(RE25+48)	address of v4 source
000022DC	00000010			1419+	DC	A(16)	result length
000022E0	0000233C			1420+REA25	DC	A(RE25)	result address
000022E8	00000000 00000000			1421+	DS	FD	gap
000022F0	00000000 00000000			1422+V1025	DS	XL16	V1 output
000022F8	00000000 00000000						
00002300	00000000 00000000			1423+	DS	FD	gap
				1424+*			
00002308				1425+X25	DS	0F	
00002308	E310 5010 0014		00000010	1426+	LGF	R1, V2ADDR	load v2 source
0000230E	E761 0000 0806		00000000	1427+	VL	v22, 0(R1)	use v22 to test decoder
00002314	E310 5014 0014		00000014	1428+	LGF	R1, V3ADDR	load v3 source
0000231A	E771 0000 0806		00000000	1429+	VL	v23, 0(R1)	use v23 to test decoder
00002320	E310 5018 0014		00000018	1430+	LGF	R1, V4ADDR	load v4 source
00002326	E781 0000 0806		00000000	1431+	VL	v24, 0(R1)	use v24 to test decoder
0000232C	E766 7000 8FAA			1432+	VMAL	V22, V22, V23, V24, 0	test instruction (dest is a source)
00002332	E760 5030 080E		000022F0	1433+	VST	V22, V1025	save v1 output
00002338	07FB			1434+	BR	R11	return
0000233C				1435+RE25	DC	0F	xl16 expected result
0000233C				1436+	DROP	R5	
0000233C	01000000 000000C0			1437	DC	XL16' 01000000000000C0 0000004300000026'	result
00002344	00000043 00000026						
0000234C	FF0000FF 00000029			1438	DC	XL16' FF0000FF00000029 00000038000000FA'	v2
00002354	00000038 000000FA						
0000235C	FF000001 00000029			1439	DC	XL16' FF00000100000029 00000038000000FA'	v3
00002364	00000038 000000FA						
0000236C	00000001 0000002F			1440	DC	XL16' 000000010000002F 0000000300000002'	v4
00002374	00000003 00000002						
				1441			
				1442	VRR_D	VMAL, 0	

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  LOC          OBJECT CODE       ADDR1     ADDR2     STMT

 00002380                                            1443+          DS     0FD
 00002380                        00002380            1444+          USING  *,R5               base for test data and test routine
 00002380   000023C8                                 1445+T26       DC     A(X26)             address of test routine
 00002384   001A                                     1446+          DC     H'26'              test number
 00002386   00                                       1447+          DC     X'00'
 00002387   00                                       1448+          DC     HL1'0'             m5
 00002388   E5D4C1D3 40404040                        1449+          DC     CL8'VMAL'          instruction name
 00002390   0000240C                                 1450+          DC     A(RE26+16)         address of v2 source
 00002394   0000241C                                 1451+          DC     A(RE26+32)         address of v3 source
 00002398   0000242C                                 1452+          DC     A(RE26+48)         address of v4 source
 0000239C   00000010                                 1453+          DC     A(16)              result length
 000023A0   000023FC                                 1454+REA26     DC     A(RE26)            result address
 000023A8   00000000 00000000                        1455+          DS     FD                 gap
 000023B0   00000000 00000000                        1456+V1026     DS     XL16               V1 output
 000023B8   00000000 00000000
 000023C0   00000000 00000000                        1457+          DS     FD                 gap
                                                     1458+*
 000023C8                                            1459+X26       DS     0F
 000023C8   E310 5010 0014              00000010     1460+          LGF    R1,V2ADDR          load v2 source
 000023CE   E761 0000 0806              00000000     1461+          VL     v22,0(R1)          use v22 to test decoder
 000023D4   E310 5014 0014              00000014     1462+          LGF    R1,V3ADDR          load v3 source
 000023DA   E771 0000 0806              00000000     1463+          VL     v23,0(R1)          use v23 to test decoder
 000023E0   E310 5018 0014              00000018     1464+          LGF    R1,V4ADDR          load v4 source
 000023E6   E781 0000 0806              00000000     1465+          VL     v24,0(R1)          use v24 to test decoder
 000023EC   E766 7000 8FAA                           1466+          VMAL   V22,V22,V23,V24,0   test instruction (dest is a source)
 000023F2   E760 5030 080E              000023B0     1467+          VST    V22,V1026           save v1 output
 000023F8   07FB                                     1468+          BR     R11                return
 000023FC                                            1469+RE26      DC     0F                 xl16 expected result
 000023FC                                            1470+          DROP   R5
 000023FC   00060C14 1E2A3848                         1471          DC     XL16'00060C141E2A3848 5A6E849CB6D2F010'    result
 00002404   5A6E849C B6D2F010
 0000240C   FF020304 05060708                         1472          DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
 00002414   090A0B0C 0D0E0F10
 0000241C   FF020304 05060708                         1473          DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v3
 00002424   090A0B0C 0D0E0F10
 0000242C   FF020304 05060708                         1474          DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
 00002434   090A0B0C 0D0E0F10
                                                      1475
                                                      1476          VRR_D  VMAL,0
 00002440                                            1477+          DS     0FD
 00002440                        00002440            1478+          USING  *,R5               base for test data and test routine
 00002440   00002488                                 1479+T27       DC     A(X27)             address of test routine
 00002444   001B                                     1480+          DC     H'27'              test number
 00002446   00                                       1481+          DC     X'00'
 00002447   00                                       1482+          DC     HL1'0'             m5
 00002448   E5D4C1D3 40404040                        1483+          DC     CL8'VMAL'          instruction name
 00002450   000024CC                                 1484+          DC     A(RE27+16)         address of v2 source
 00002454   000024DC                                 1485+          DC     A(RE27+32)         address of v3 source
 00002458   000024EC                                 1486+          DC     A(RE27+48)         address of v4 source
 0000245C   00000010                                 1487+          DC     A(16)              result length
 00002460   000024BC                                 1488+REA27     DC     A(RE27)            result address
 00002468   00000000 00000000                        1489+          DS     FD                 gap
 00002470   00000000 00000000                        1490+V1027     DS     XL16               V1 output
 00002478   00000000 00000000
 00002480   00000000 00000000                        1491+          DS     FD                 gap
                                                     1492+*
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002488				1493+X27	DS	0F	
00002488	E310 5010 0014		00000010	1494+	LGF	R1,V2ADDR	load v2 source
0000248E	E761 0000 0806		00000000	1495+	VL	v22,0(R1)	use v22 to test decoder
00002494	E310 5014 0014		00000014	1496+	LGF	R1,V3ADDR	load v3 source
0000249A	E771 0000 0806		00000000	1497+	VL	v23,0(R1)	use v23 to test decoder
000024A0	E310 5018 0014		00000018	1498+	LGF	R1,V4ADDR	load v4 source
000024A6	E781 0000 0806		00000000	1499+	VL	v24,0(R1)	use v24 to test decoder
000024AC	E766 7000 8FAA			1500+	VMAL	V22,V22,V23,V24,0	test instruction (dest is a source)
000024B2	E760 5030 080E		00002470	1501+	VST	V22,V1027	save v1 output
000024B8	07FB			1502+	BR	R11	return
000024BC				1503+RE27	DC	0F	xl16 expected result
000024BC				1504+	DROP	R5	
000024BC	0004060C 0F181C28			1505	DC	XL16'0004060C0F181C28 2D3C42545B707890'	result
000024C4	2D3C4254 5B707890						
000024CC	FF020304 05060708			1506	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
000024D4	090A0B0C 0D0E0F10						
000024DC	FF010102 02030304			1507	DC	XL16'FF01010202030304 0405050606070708'	v3
000024E4	04050506 06070708						
000024EC	FF020304 05060708			1508	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
000024F4	090A0B0C 0D0E0F10						
				1509			
				1510	VRR_D	VMAL,0	
00002500				1511+	DS	0FD	
00002500		00002500		1512+	USING	*,R5	base for test data and test routine
00002500	00002548			1513+T28	DC	A(X28)	address of test routine
00002504	001C			1514+	DC	H'28'	test number
00002506	00			1515+	DC	X'00'	
00002507	00			1516+	DC	HL1'0'	m5
00002508	E5D4C1D3 40404040			1517+	DC	CL8'VMAL'	instruction name
00002510	0000258C			1518+	DC	A(RE28+16)	address of v2 source
00002514	0000259C			1519+	DC	A(RE28+32)	address of v3 source
00002518	000025AC			1520+	DC	A(RE28+48)	address of v4 source
0000251C	00000010			1521+	DC	A(16)	result length
00002520	0000257C			1522+REA28	DC	A(RE28)	result address
00002528	00000000 00000000			1523+	DS	FD	gap
00002530	00000000 00000000			1524+V1028	DS	XL16	V1 output
00002538	00000000 00000000						
00002540	00000000 00000000			1525+	DS	FD	gap
				1526+*			
00002548				1527+X28	DS	0F	
00002548	E310 5010 0014		00000010	1528+	LGF	R1,V2ADDR	load v2 source
0000254E	E761 0000 0806		00000000	1529+	VL	v22,0(R1)	use v22 to test decoder
00002554	E310 5014 0014		00000014	1530+	LGF	R1,V3ADDR	load v3 source
0000255A	E771 0000 0806		00000000	1531+	VL	v23,0(R1)	use v23 to test decoder
00002560	E310 5018 0014		00000018	1532+	LGF	R1,V4ADDR	load v4 source
00002566	E781 0000 0806		00000000	1533+	VL	v24,0(R1)	use v24 to test decoder
0000256C	E766 7000 8FAA			1534+	VMAL	V22,V22,V23,V24,0	test instruction (dest is a source)
00002572	E760 5030 080E		00002530	1535+	VST	V22,V1028	save v1 output
00002578	07FB			1536+	BR	R11	return
0000257C				1537+RE28	DC	0F	xl16 expected result
0000257C				1538+	DROP	R5	
0000257C	00020304 05060710			1539	DC	XL16'0002030405060710 121416181A1C1E30'	result
00002584	12141618 1A1C1E30						
0000258C	FF020304 05060708			1540	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00002594	090A0B0C 0D0E0F10						
0000259C	FF000000 00000001			1541	DC	XL16'FF00000000000001 0101010101010102'	v3

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000025A4	01010101 01010102						
000025AC	FF020304 05060708			1542	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
000025B4	090A0B0C 0D0E0F10						
				1543			
				1544	* Halfword		
				1545	VRR_D	VMAL,1	
000025C0				1546+	DS	0FD	
000025C0		000025C0		1547+	USING	*,R5	base for test data and test routine
000025C0	00002608			1548+T29	DC	A(X29)	address of test routine
000025C4	001D			1549+	DC	H'29'	test number
000025C6	00			1550+	DC	X'00'	
000025C7	01			1551+	DC	HL1'1'	m5
000025C8	E5D4C1D3 40404040			1552+	DC	CL8'VMAL'	instruction name
000025D0	0000264C			1553+	DC	A(RE29+16)	address of v2 source
000025D4	0000265C			1554+	DC	A(RE29+32)	address of v3 source
000025D8	0000266C			1555+	DC	A(RE29+48)	address of v4 source
000025DC	00000010			1556+	DC	A(16)	result length
000025E0	0000263C			1557+REA29	DC	A(RE29)	result address
000025E8	00000000 00000000			1558+	DS	FD	gap
000025F0	00000000 00000000			1559+V1029	DS	XL16	V1 output
000025F8	00000000 00000000						
00002600	00000000 00000000			1560+	DS	FD	gap
				1561+*			
00002608				1562+X29	DS	0F	
00002608	E310 5010 0014		00000010	1563+	LGF	R1,V2ADDR	load v2 source
0000260E	E761 0000 0806		00000000	1564+	VL	v22,0(R1)	use v22 to test decoder
00002614	E310 5014 0014		00000014	1565+	LGF	R1,V3ADDR	load v3 source
0000261A	E771 0000 0806		00000000	1566+	VL	v23,0(R1)	use v23 to test decoder
00002620	E310 5018 0014		00000018	1567+	LGF	R1,V4ADDR	load v4 source
00002626	E781 0000 0806		00000000	1568+	VL	v24,0(R1)	use v24 to test decoder
0000262C	E766 7100 8FAA			1569+	VMAL	V22,V22,V23,V24,1	test instruction (dest is a source)
00002632	E760 5030 080E		000025F0	1570+	VST	V22,V1029	save v1 output
00002638	07FB			1571+	BR	R11	return
0000263C				1572+RE29	DC	0F	xl16 expected result
0000263C				1573+	DROP	R5	
0000263C	00000000 00000271			1574	DC	XL16'0000000000000271 00000C400000F424'	result
00002644	00000C40 0000F424						
0000264C	FF000000 00000019			1575	DC	XL16'FF00000000000019 00000038000000FA'	v2
00002654	00000038 000000FA						
0000265C	FF000000 00000019			1576	DC	XL16'FF00000000000019 00000038000000FA'	v3
00002664	00000038 000000FA						
0000266C	00000000 00000000			1577	DC	XL16'0000000000000000 0000000000000000'	v4
00002674	00000000 00000000						
				1578			
				1579	VRR_D	VMAL,1	
00002680				1580+	DS	0FD	
00002680		00002680		1581+	USING	*,R5	base for test data and test routine
00002680	000026C8			1582+T30	DC	A(X30)	address of test routine
00002684	001E			1583+	DC	H'30'	test number
00002686	00			1584+	DC	X'00'	
00002687	01			1585+	DC	HL1'1'	m5
00002688	E5D4C1D3 40404040			1586+	DC	CL8'VMAL'	instruction name
00002690	0000270C			1587+	DC	A(RE30+16)	address of v2 source
00002694	0000271C			1588+	DC	A(RE30+32)	address of v3 source
00002698	0000272C			1589+	DC	A(RE30+48)	address of v4 source
0000269C	00000010			1590+	DC	A(16)	result length

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  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

000026A0   000026FC                               1591+REA30   DC    A(RE30)               result address
000026A8   00000000 00000000                      1592+        DS    FD                    gap
000026B0   00000000 00000000                      1593+V1030   DS    XL16                  V1 output
000026B8   00000000 00000000
000026C0   00000000 00000000                      1594+        DS    FD                    gap
                                                  1595+*
000026C8                                          1596+X30     DS    0F
000026C8   E310 5010 0014             00000010    1597+        LGF   R1,V2ADDR             load v2 source
000026CE   E761 0000 0806             00000000    1598+        VL    v22,0(R1)             use v22 to test decoder
000026D4   E310 5014 0014             00000014    1599+        LGF   R1,V3ADDR             load v3 source
000026DA   E771 0000 0806             00000000    1600+        VL    v23,0(R1)             use v23 to test decoder
000026E0   E310 5018 0014             00000018    1601+        LGF   R1,V4ADDR             load v4 source
000026E6   E781 0000 0806             00000000    1602+        VL    v24,0(R1)             use v24 to test decoder
000026EC   E766 7100 8FAA                         1603+        VMAL  V22,V22,V23,V24,1     test instruction (dest is a source)
000026F2   E760 5030 080E             000026B0    1604+        VST   V22,V1030            save v1 output
000026F8   07FB                                   1605+        BR    R11                   return
000026FC                                          1606+RE30    DC    0F                    xl16 expected result
000026FC                                          1607+        DROP  R5
000026FC   00000100 000006C0                      1608         DC    XL16'00000100000006C0 00000C430000F426'    result
00002704   00000C43 0000F426
0000270C   FF0000FF 00000029                      1609         DC    XL16'FF0000FF00000029 00000038000000FA'    v2
00002714   00000038 000000FA
0000271C   FF000001 00000029                      1610         DC    XL16'FF00000100000029 00000038000000FA'    v3
00002724   00000038 000000FA
0000272C   00000001 0000002F                      1611         DC    XL16'000000010000002F 0000000300000002'    v4
00002734   00000003 00000002

                                                  1612
                                                  1613         VRR_D VMAL,1
00002740                                          1614+        DS    0FD
00002740                         00002740         1615+        USING *,R5                  base for test data and test routine
00002740   00002788                               1616+T31     DC    A(X31)                address of test routine
00002744   001F                                   1617+        DC    H'31'                 test number
00002746   00                                     1618+        DC    X'00'
00002747   01                                     1619+        DC    HL1'1'                m5
00002748   E5D4C1D3 40404040                      1620+        DC    CL8'VMAL'             instruction name
00002750   000027CC                               1621+        DC    A(RE31+16)            address of v2 source
00002754   000027DC                               1622+        DC    A(RE31+32)            address of v3 source
00002758   000027EC                               1623+        DC    A(RE31+48)            address of v4 source
0000275C   00000010                               1624+        DC    A(16)                 result length
00002760   000027BC                               1625+REA31   DC    A(RE31)               result address
00002768   00000000 00000000                      1626+        DS    FD                    gap
00002770   00000000 00000000                      1627+V1031   DS    XL16                  V1 output
00002778   00000000 00000000
00002780   00000000 00000000                      1628+        DS    FD                    gap
                                                  1629+*
00002788                                          1630+X31     DS    0F
00002788   E310 5010 0014             00000010    1631+        LGF   R1,V2ADDR             load v2 source
0000278E   E761 0000 0806             00000000    1632+        VL    v22,0(R1)             use v22 to test decoder
00002794   E310 5014 0014             00000014    1633+        LGF   R1,V3ADDR             load v3 source
0000279A   E771 0000 0806             00000000    1634+        VL    v23,0(R1)             use v23 to test decoder
000027A0   E310 5018 0014             00000018    1635+        LGF   R1,V4ADDR             load v4 source
000027A6   E781 0000 0806             00000000    1636+        VL    v24,0(R1)             use v24 to test decoder
000027AC   E766 7100 8FAA                         1637+        VMAL  V22,V22,V23,V24,1     test instruction (dest is a source)
000027B2   E760 5030 080E             00002770    1638+        VST   V22,V1031            save v1 output
000027B8   07FB                                   1639+        BR    R11                   return
000027BC                                          1640+RE31    DC    0F                    xl16 expected result
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000027BC				1641+	DROP	R5	
000027BC	FB061B14 412A7748			1642	DC	XL16'FB061B14412A7748 BD6E139C79D2F010'	result
000027C4	BD6E139C 79D2F010						
000027CC	FF020304 05060708			1643	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
000027D4	090A0B0C 0D0E0F10						
000027DC	FF020304 05060708			1644	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3
000027E4	090A0B0C 0D0E0F10						
000027EC	FF020304 05060708			1645	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
000027F4	090A0B0C 0D0E0F10						
				1646			
				1647	VRR_D	VMAL,1	
00002800				1648+	DS	0FD	
00002800		00002800		1649+	USING	*,R5	base for test data and test routine
00002800	00002848			1650+T32	DC	A(X32)	address of test routine
00002804	0020			1651+	DC	H'32'	test number
00002806	00			1652+	DC	X'00'	
00002807	01			1653+	DC	HL1'1'	m5
00002808	E5D4C1D3 40404040			1654+	DC	CL8'VMAL'	instruction name
00002810	0000288C			1655+	DC	A(RE32+16)	address of v2 source
00002814	0000289C			1656+	DC	A(RE32+32)	address of v3 source
00002818	000028AC			1657+	DC	A(RE32+48)	address of v4 source
0000281C	00000010			1658+	DC	A(16)	result length
00002820	0000287C			1659+REA32	DC	A(RE32)	result address
00002828	00000000 00000000			1660+	DS	FD	gap
00002830	00000000 00000000			1661+V1032	DS	XL16	V1 output
00002838	00000000 00000000						
00002840	00000000 00000000			1662+	DS	FD	gap
				1663+*			
00002848				1664+X32	DS	0F	
00002848	E310 5010 0014		00000010	1665+	LGF	R1,V2ADDR	load v2 source
0000284E	E761 0000 0806		00000000	1666+	VL	v22,0(R1)	use v22 to test decoder
00002854	E310 5014 0014		00000014	1667+	LGF	R1,V3ADDR	load v3 source
0000285A	E771 0000 0806		00000000	1668+	VL	v23,0(R1)	use v23 to test decoder
00002860	E310 5018 0014		00000018	1669+	LGF	R1,V4ADDR	load v4 source
00002866	E781 0000 0806		00000000	1670+	VL	v24,0(R1)	use v24 to test decoder
0000286C	E766 7100 8FAA			1671+	VMAL	V22,V22,V23,V24,1	test instruction (dest is a source)
00002872	E760 5030 080E		00002830	1672+	VST	V22,V1032	save v1 output
00002878	07FB			1673+	BR	R11	return
0000287C				1674+RE32	DC	0F	xl16 expected result
0000287C				1675+	DROP	R5	
0000287C	FC040D0C 20183B28			1676	DC	XL16'FC040D0C20183B28 5E3C8954BC70F790'	result
00002884	5E3C8954 BC70F790						
0000288C	FF020304 05060708			1677	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00002894	090A0B0C 0D0E0F10						
0000289C	FF010102 02030304			1678	DC	XL16'FF01010202030304 0405050606070708'	v3
000028A4	04050506 06070708						
000028AC	FF020304 05060708			1679	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
000028B4	090A0B0C 0D0E0F10						
				1680			
				1681	VRR_D	VMAL,1	
000028C0				1682+	DS	0FD	
000028C0		000028C0		1683+	USING	*,R5	base for test data and test routine
000028C0	00002908			1684+T33	DC	A(X33)	address of test routine
000028C4	0021			1685+	DC	H'33'	test number
000028C6	00			1686+	DC	X'00'	
000028C7	01			1687+	DC	HL1'1'	m5

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000028C8   E5D4C1D3 40404040                        1688+          DC      CL8'VMAL'              instruction name
000028D0   0000294C                                 1689+          DC      A(RE33+16)            address of v2 source
000028D4   0000295C                                 1690+          DC      A(RE33+32)            address of v3 source
000028D8   0000296C                                 1691+          DC      A(RE33+48)            address of v4 source
000028DC   00000010                                 1692+          DC      A(16)                 result length
000028E0   0000293C                                 1693+REA33     DC      A(RE33)               result address
000028E8   00000000 00000000                        1694+          DS      FD                    gap
000028F0   00000000 00000000                        1695+V1033     DS      XL16                  V1 output
000028F8   00000000 00000000
00002900   00000000 00000000                        1696+          DS      FD                    gap
                                                    1697+*
00002908                                            1698+X33       DS      0F
00002908   E310 5010 0014                 00000010  1699+          LGF     R1,V2ADDR             load v2 source
0000290E   E761 0000 0806                 00000000  1700+          VL      v22,0(R1)             use v22 to test decoder
00002914   E310 5014 0014                 00000014  1701+          LGF     R1,V3ADDR             load v3 source
0000291A   E771 0000 0806                 00000000  1702+          VL      v23,0(R1)             use v23 to test decoder
00002920   E310 5018 0014                 00000018  1703+          LGF     R1,V4ADDR             load v4 source
00002926   E781 0000 0806                 00000000  1704+          VL      v24,0(R1)             use v24 to test decoder
0000292C   E766 7100 8FAA                           1705+          VMAL    V22,V22,V23,V24,1      test instruction (dest is a source)
00002932   E760 5030 080E                 000028F0  1706+          VST     V22,V1033              save v1 output
00002938   07FB                                     1707+          BR      R11                   return
0000293C                                            1708+RE33      DC      0F                    xl16 expected result
0000293C                                            1709+          DROP    R5
0000293C   FD020304 05060E10                        1710           DC      XL16'FD02030405060E10 1C142218281C3D30'     result
00002944   1C142218 281C3D30
0000294C   FF020304 05060708                        1711           DC      XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
00002954   090A0B0C 0D0E0F10
0000295C   FF000000 00000001                        1712           DC      XL16'FF00000000000001 0101010101010102'     v3
00002964   01010101 01010102
0000296C   FF020304 05060708                        1713           DC      XL16'FF02030405060708 090A0B0C0D0E0F10'     v4
00002974   090A0B0C 0D0E0F10

                                                    1714
                                                    1715 * Word
                                                    1716           VRR_D   VMAL,2
00002980                                            1717+          DS      0FD
00002980                           00002980         1718+          USING   *,R5                  base for test data and test routine
00002980   000029C8                                 1719+T34       DC      A(X34)                address of test routine
00002984   0022                                     1720+          DC      H'34'                 test number
00002986   00                                       1721+          DC      X'00'
00002987   02                                       1722+          DC      HL1'2'                m5
00002988   E5D4C1D3 40404040                        1723+          DC      CL8'VMAL'             instruction name
00002990   00002A0C                                 1724+          DC      A(RE34+16)            address of v2 source
00002994   00002A1C                                 1725+          DC      A(RE34+32)            address of v3 source
00002998   00002A2C                                 1726+          DC      A(RE34+48)            address of v4 source
0000299C   00000010                                 1727+          DC      A(16)                 result length
000029A0   000029FC                                 1728+REA34     DC      A(RE34)               result address
000029A8   00000000 00000000                        1729+          DS      FD                    gap
000029B0   00000000 00000000                        1730+V1034     DS      XL16                  V1 output
000029B8   00000000 00000000
000029C0   00000000 00000000                        1731+          DS      FD                    gap
                                                    1732+*
000029C8                                            1733+X34       DS      0F
000029C8   E310 5010 0014                 00000010  1734+          LGF     R1,V2ADDR             load v2 source
000029CE   E761 0000 0806                 00000000  1735+          VL      v22,0(R1)             use v22 to test decoder
000029D4   E310 5014 0014                 00000014  1736+          LGF     R1,V3ADDR             load v3 source
000029DA   E771 0000 0806                 00000000  1737+          VL      v23,0(R1)             use v23 to test decoder
```

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  LOC        OBJECT CODE        ADDR1     ADDR2     STMT

000029E0   E310 5018 0014                 00000018  1738+        LGF     R1,V4ADDR           load v4 source
000029E6   E781 0000 0806                 00000000  1739+        VL      v24,0(R1)           use v24 to test decoder
000029EC   E766 7200 8FAA                           1740+        VMAL    V22,V22,V23,V24,2     test instruction (dest is a source)
000029F2   E760 5030 080E                 000029B0  1741+        VST     V22,V1034            save v1 output
000029F8   07FB                                     1742+        BR      R11                 return
000029FC                                            1743+RE34    DC      0F                  xl16 expected result
000029FC                                            1744+        DROP    R5
000029FC   00000000 00000271                        1745         DC      XL16'0000000000000271 00000C400000F424'     result
00002A04   00000C40 0000F424
00002A0C   FF000000 00000019                        1746         DC      XL16'FF00000000000019 00000038000000FA'     v2
00002A14   00000038 000000FA
00002A1C   FF000000 00000019                        1747         DC      XL16'FF00000000000019 00000038000000FA'     v3
00002A24   00000038 000000FA
00002A2C   00000000 00000000                        1748         DC      XL16'0000000000000000 0000000000000000'     v4
00002A34   00000000 00000000

                                                    1749
                                                    1750         VRR_D VMAL,2
00002A40                                            1751+        DS      0FD
00002A40                          00002A40          1752+        USING   *,R5                base for test data and test routine
00002A40   00002A88                                 1753+T35     DC      A(X35)              address of test routine
00002A44   0023                                     1754+        DC      H'35'               test number
00002A46   00                                       1755+        DC      X'00'
00002A47   02                                       1756+        DC      HL1'2'              m5
00002A48   E5D4C1D3 40404040                        1757+        DC      CL8'VMAL'           instruction name
00002A50   00002ACC                                 1758+        DC      A(RE35+16)          address of v2 source
00002A54   00002ADC                                 1759+        DC      A(RE35+32)          address of v3 source
00002A58   00002AEC                                 1760+        DC      A(RE35+48)          address of v4 source
00002A5C   00000010                                 1761+        DC      A(16)               result length
00002A60   00002ABC                                 1762+REA35   DC      A(RE35)             result address
00002A68   00000000 00000000                        1763+        DS      FD                  gap
00002A70   00000000 00000000                        1764+V1035   DS      XL16                V1 output
00002A78   00000000 00000000
00002A80   00000000 00000000                        1765+        DS      FD                  gap
                                                    1766+*
00002A88                                            1767+X35     DS      0F
00002A88   E310 5010 0014                 00000010  1768+        LGF     R1,V2ADDR           load v2 source
00002A8E   E761 0000 0806                 00000000  1769+        VL      v22,0(R1)           use v22 to test decoder
00002A94   E310 5014 0014                 00000014  1770+        LGF     R1,V3ADDR           load v3 source
00002A9A   E771 0000 0806                 00000000  1771+        VL      v23,0(R1)           use v23 to test decoder
00002AA0   E310 5018 0014                 00000018  1772+        LGF     R1,V4ADDR           load v4 source
00002AA6   E781 0000 0806                 00000000  1773+        VL      v24,0(R1)           use v24 to test decoder
00002AAC   E766 7200 8FAA                           1774+        VMAL    V22,V22,V23,V24,2     test instruction (dest is a source)
00002AB2   E760 5030 080E                 00002A70  1775+        VST     V22,V1035            save v1 output
00002AB8   07FB                                     1776+        BR      R11                 return
00002ABC                                            1777+RE35    DC      0F                  xl16 expected result
00002ABC                                            1778+        DROP    R5
00002ABC   00000100 000006C0                        1779         DC      XL16'00000100000006C0 00000C430000F426'     result
00002AC4   00000C43 0000F426
00002ACC   FF0000FF 00000029                        1780         DC      XL16'FF0000FF00000029 00000038000000FA'     v2
00002AD4   00000038 000000FA
00002ADC   FF000001 00000029                        1781         DC      XL16'FF00000100000029 00000038000000FA'     v3
00002AE4   00000038 000000FA
00002AEC   00000001 0000002F                        1782         DC      XL16'000000010000002F 0000000300000002'     v4
00002AF4   00000003 00000002

                                                    1783
                                                    1784         VRR_D VMAL,2
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
00002B00				1785+	DS	0FD
00002B00		00002B00		1786+	USING *,R5	base for test data and test routine
00002B00	00002B48			1787+T36	DC	A(X36)	address of test routine
00002B04	0024			1788+	DC	H'36'	test number
00002B06	00			1789+	DC	X'00'
00002B07	02			1790+	DC	HL1'2'	m5
00002B08	E5D4C1D3 40404040			1791+	DC	CL8'VMAL'	instruction name
00002B10	00002B8C			1792+	DC	A(RE36+16)	address of v2 source
00002B14	00002B9C			1793+	DC	A(RE36+32)	address of v3 source
00002B18	00002BAC			1794+	DC	A(RE36+48)	address of v4 source
00002B1C	00000010			1795+	DC	A(16)	result length
00002B20	00002B7C			1796+REA36	DC	A(RE36)	result address
00002B28	00000000 00000000			1797+	DS	FD	gap
00002B30	00000000 00000000			1798+V1036	DS	XL16	V1 output
00002B38	00000000 00000000					
00002B40	00000000 00000000			1799+	DS	FD	gap
				1800+*		
00002B48				1801+X36	DS	0F
00002B48	E310 5010 0014		00000010	1802+	LGF	R1,V2ADDR	load v2 source
00002B4E	E761 0000 0806		00000000	1803+	VL	v22,0(R1)	use v22 to test decoder
00002B54	E310 5014 0014		00000014	1804+	LGF	R1,V3ADDR	load v3 source
00002B5A	E771 0000 0806		00000000	1805+	VL	v23,0(R1)	use v23 to test decoder
00002B60	E310 5018 0014		00000018	1806+	LGF	R1,V4ADDR	load v4 source
00002B66	E781 0000 0806		00000000	1807+	VL	v24,0(R1)	use v24 to test decoder
00002B6C	E766 7200 8FAA			1808+	VMAL	V22,V22,V23,V24,2	test instruction (dest is a source)
00002B72	E760 5030 080E		00002B30	1809+	VST	V22,V1036	save v1 output
00002B78	07FB			1810+	BR	R11	return
00002B7C				1811+RE36	DC	0F	xl16 expected result
00002B7C				1812+	DROP	R5
00002B7C	031B1B14 A9977748			1813	DC	XL16'031B1B14A9977748 BE74139C53B0F010' result
00002B84	BE74139C 53B0F010					
00002B8C	FF020304 05060708			1814	DC	XL16'FF02030405060708 090A0B0C0D0E0F10' v2
00002B94	090A0B0C 0D0E0F10					
00002B9C	FF020304 05060708			1815	DC	XL16'FF02030405060708 090A0B0C0D0E0F10' v3
00002BA4	090A0B0C 0D0E0F10					
00002BAC	FF020304 05060708			1816	DC	XL16'FF02030405060708 090A0B0C0D0E0F10' v4
00002BB4	090A0B0C 0D0E0F10					
				1817		
00002BC0				1818	VRR_D VMAL,2
00002BC0				1819+	DS	0FD
00002BC0		00002BC0		1820+	USING *,R5	base for test data and test routine
00002BC0	00002C08			1821+T37	DC	A(X37)	address of test routine
00002BC4	0025			1822+	DC	H'37'	test number
00002BC6	00			1823+	DC	X'00'
00002BC7	02			1824+	DC	HL1'2'	m5
00002BC8	E5D4C1D3 40404040			1825+	DC	CL8'VMAL'	instruction name
00002BD0	00002C4C			1826+	DC	A(RE37+16)	address of v2 source
00002BD4	00002C5C			1827+	DC	A(RE37+32)	address of v3 source
00002BD8	00002C6C			1828+	DC	A(RE37+48)	address of v4 source
00002BDC	00000010			1829+	DC	A(16)	result length
00002BE0	00002C3C			1830+REA37	DC	A(RE37)	result address
00002BE8	00000000 00000000			1831+	DS	FD	gap
00002BF0	00000000 00000000			1832+V1037	DS	XL16	V1 output
00002BF8	00000000 00000000					
00002C00	00000000 00000000			1833+	DS	FD	gap
				1834+*		

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  LOC         OBJECT CODE     ADDR1     ADDR2     STMT

00002C08                                          1835+X37      DS     0F
00002C08    E310 5010 0014              00000010  1836+         LGF    R1,V2ADDR         load v2 source
00002C0E    E761 0000 0806              00000000  1837+         VL     v22,0(R1)         use v22 to test decoder
00002C14    E310 5014 0014              00000014  1838+         LGF    R1,V3ADDR         load v3 source
00002C1A    E771 0000 0806              00000000  1839+         VL     v23,0(R1)         use v23 to test decoder
00002C20    E310 5018 0014              00000018  1840+         LGF    R1,V4ADDR         load v4 source
00002C26    E781 0000 0806              00000000  1841+         VL     v24,0(R1)         use v24 to test decoder
00002C2C    E766 7200 8FAA                        1842+         VMAL   V22,V22,V23,V24,2    test instruction (dest is a source)
00002C32    E760 5030 080E              00002BF0  1843+         VST    V22,V1037          save v1 output
00002C38    07FB                                  1844+         BR     R11               return
00002C3C                                          1845+RE37     DC     0F                xl16 expected result
00002C3C                                          1846+         DROP   R5
00002C3C    FE0D0D0C 504B3B28                     1847          DC     XL16'FE0D0D0C504B3B28 D8B98954A157F790'     result
00002C44    D8B98954 A157F790
00002C4C    FF020304 05060708                     1848          DC     XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
00002C54    090A0B0C 0D0E0F10
00002C5C    FF010102 02030304                     1849          DC     XL16'FF01010202030304 0405050606070708'     v3
00002C64    04050506 06070708
00002C6C    FF020304 05060708                     1850          DC     XL16'FF02030405060708 090A0B0C0D0E0F10'     v4
00002C74    090A0B0C 0D0E0F10

                                                  1851
                                                  1852          VRR_D  VMAL,2
00002C80                                          1853+         DS     0FD
00002C80                         00002C80         1854+         USING  *,R5              base for test data and test routine
00002C80    00002CC8                              1855+T38      DC     A(X38)            address of test routine
00002C84    0026                                  1856+         DC     H'38'             test number
00002C86    00                                    1857+         DC     X'00'
00002C87    02                                    1858+         DC     HL1'2'            m5
00002C88    E5D4C1D3 40404040                     1859+         DC     CL8'VMAL'         instruction name
00002C90    00002D0C                              1860+         DC     A(RE38+16)        address of v2 source
00002C94    00002D1C                              1861+         DC     A(RE38+32)        address of v3 source
00002C98    00002D2C                              1862+         DC     A(RE38+48)        address of v4 source
00002C9C    00000010                              1863+         DC     A(16)             result length
00002CA0    00002CFC                              1864+REA38    DC     A(RE38)           result address
00002CA8    00000000 00000000                     1865+         DS     FD                gap
00002CB0    00000000 00000000                     1866+V1038    DS     XL16              V1 output
00002CB8    00000000 00000000
00002CC0    00000000 00000000                     1867+         DS     FD                gap

                                                  1868+*
00002CC8                                          1869+X38      DS     0F
00002CC8    E310 5010 0014              00000010  1870+         LGF    R1,V2ADDR         load v2 source
00002CCE    E761 0000 0806              00000000  1871+         VL     v22,0(R1)         use v22 to test decoder
00002CD4    E310 5014 0014              00000014  1872+         LGF    R1,V3ADDR         load v3 source
00002CDA    E771 0000 0806              00000000  1873+         VL     v23,0(R1)         use v23 to test decoder
00002CE0    E310 5018 0014              00000018  1874+         LGF    R1,V4ADDR         load v4 source
00002CE6    E781 0000 0806              00000000  1875+         VL     v24,0(R1)         use v24 to test decoder
00002CEC    E766 7200 8FAA                        1876+         VMAL   V22,V22,V23,V24,2    test instruction (dest is a source)
00002CF2    E760 5030 080E              00002CB0  1877+         VST    V22,V1038          save v1 output
00002CF8    07FB                                  1878+         BR     R11               return
00002CFC                                          1879+RE38     DC     0F                xl16 expected result
00002CFC                                          1880+         DROP   R5
00002CFC    FB020304 0A0C0E10                     1881          DC     XL16'FB0203040A0C0E10 332B221854493D30'     result
00002D04    332B2218 54493D30
00002D0C    FF020304 05060708                     1882          DC     XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
00002D14    090A0B0C 0D0E0F10
00002D1C    FF000000 00000001                     1883          DC     XL16'FF00000000000001 0101010101010102'     v3
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002D24	01010101 01010102							
00002D2C	FF020304 05060708			1884		DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00002D34	090A0B0C 0D0E0F10							
				1885				
				1886	* Doubleword			
				1887		VRR_D VMAL,3		
00002D40				1888+		DS	0FD	
00002D40		00002D40		1889+		USING	*,R5	base for test data and test routine
00002D40	00002D88			1890+T39		DC	A(X39)	address of test routine
00002D44	0027			1891+		DC	H'39'	test number
00002D46	00			1892+		DC	X'00'	
00002D47	03			1893+		DC	HL1'3'	m5
00002D48	E5D4C1D3 40404040			1894+		DC	CL8'VMAL'	instruction name
00002D50	00002DCC			1895+		DC	A(RE39+16)	address of v2 source
00002D54	00002DDC			1896+		DC	A(RE39+32)	address of v3 source
00002D58	00002DEC			1897+		DC	A(RE39+48)	address of v4 source
00002D5C	00000010			1898+		DC	A(16)	result length
00002D60	00002DBC			1899+REA39		DC	A(RE39)	result address
00002D68	00000000 00000000			1900+		DS	FD	gap
00002D70	00000000 00000000			1901+V1039		DS	XL16	V1 output
00002D78	00000000 00000000							
00002D80	00000000 00000000			1902+		DS	FD	gap
				1903+*				
00002D88				1904+X39		DS	0F	
00002D88	E310 5010 0014		00000010	1905+		LGF	R1,V2ADDR	load v2 source
00002D8E	E761 0000 0806		00000000	1906+		VL	v22,0(R1)	use v22 to test decoder
00002D94	E310 5014 0014		00000014	1907+		LGF	R1,V3ADDR	load v3 source
00002D9A	E771 0000 0806		00000000	1908+		VL	v23,0(R1)	use v23 to test decoder
00002DA0	E310 5018 0014		00000018	1909+		LGF	R1,V4ADDR	load v4 source
00002DA6	E781 0000 0806		00000000	1910+		VL	v24,0(R1)	use v24 to test decoder
00002DAC	E766 7300 8FAA			1911+		VMAL	V22,V22,V23,V24,3	test instruction (dest is a source)
00002DB2	E760 5030 080E		00002D70	1912+		VST	V22,V1039	save v1 output
00002DB8	07FB			1913+		BR	R11	return
00002DBC				1914+RE39		DC	0F	xl16 expected result
00002DBC				1915+		DROP	R5	
00002DBC	FFFCE002 71000000			1916		DC	XL16'FFFCE00271000000 96789F9F4FEDCC24'	result
00002DC4	96789F9F 4FEDCC24							
00002DCC	FFFFFFFF 00019000			1917		DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00002DD4	00000038 EEEEEEFA							
00002DDC	FFFFFFFF 00019000			1918		DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00002DE4	00000038 0EEEEEFA							
00002DEC	00000000 00000000			1919		DC	XL16'0000000000000000 0000000000000000'	v4
00002DF4	00000000 00000000							
				1920				
				1921		VRR_D VMAL,3		
00002E00				1922+		DS	0FD	
00002E00		00002E00		1923+		USING	*,R5	base for test data and test routine
00002E00	00002E48			1924+T40		DC	A(X40)	address of test routine
00002E04	0028			1925+		DC	H'40'	test number
00002E06	00			1926+		DC	X'00'	
00002E07	03			1927+		DC	HL1'3'	m5
00002E08	E5D4C1D3 40404040			1928+		DC	CL8'VMAL'	instruction name
00002E10	00002E8C			1929+		DC	A(RE40+16)	address of v2 source
00002E14	00002E9C			1930+		DC	A(RE40+32)	address of v3 source
00002E18	00002EAC			1931+		DC	A(RE40+48)	address of v4 source
00002E1C	00000010			1932+		DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002E20	00002E7C			1933+REA40	DC	A(RE40)	result address
00002E28	00000000 00000000			1934+	DS	FD	gap
00002E30	00000000 00000000			1935+V1040	DS	XL16	V1 output
00002E38	00000000 00000000						
00002E40	00000000 00000000			1936+	DS	FD	gap
				1937+*			
00002E48				1938+X40	DS	0F	
00002E48	E310 5010 0014		00000010	1939+	LGF	R1,V2ADDR	load v2 source
00002E4E	E761 0000 0806		00000000	1940+	VL	v22,0(R1)	use v22 to test decoder
00002E54	E310 5014 0014		00000014	1941+	LGF	R1,V3ADDR	load v3 source
00002E5A	E771 0000 0806		00000000	1942+	VL	v23,0(R1)	use v23 to test decoder
00002E60	E310 5018 0014		00000018	1943+	LGF	R1,V4ADDR	load v4 source
00002E66	E781 0000 0806		00000000	1944+	VL	v24,0(R1)	use v24 to test decoder
00002E6C	E766 7300 8FAA			1945+	VMAL	V22,V22,V23,V24,3	test instruction (dest is a source)
00002E72	E760 5030 080E		00002E30	1946+	VST	V22,V1040	save v1 output
00002E78	07FB			1947+	BR	R11	return
00002E7C				1948+RE40	DC	0F	xl16 expected result
00002E7C				1949+	DROP	R5	
00002E7C	69B556ED 77F57901			1950	DC	XL16'69B556ED77F57901 152B55D498D42102'	result
00002E84	152B55D4 98D42102						
00002E8C	FF020304 05060750			1951	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00002E94	090A0B0C 0D0E0F7F						
00002E9C	01020304 05060750			1952	DC	XL16'0102030405060750 090A0B780D0E0F7F'	v3
00002EA4	090A0B78 0D0E0F7F						
00002EAC	00000000 00000001			1953	DC	XL16'0000000000000001 0000000000000001'	v4
00002EB4	00000000 00000001						
				1954			
				1955	VRR_D	VMAL,3	
00002EC0				1956+	DS	0FD	
00002EC0		00002EC0		1957+	USING	*,R5	base for test data and test routine
00002EC0	00002F08			1958+T41	DC	A(X41)	address of test routine
00002EC4	0029			1959+	DC	H'41'	test number
00002EC6	00			1960+	DC	X'00'	
00002EC7	03			1961+	DC	HL1'3'	m5
00002EC8	E5D4C1D3 40404040			1962+	DC	CL8'VMAL'	instruction name
00002ED0	00002F4C			1963+	DC	A(RE41+16)	address of v2 source
00002ED4	00002F5C			1964+	DC	A(RE41+32)	address of v3 source
00002ED8	00002F6C			1965+	DC	A(RE41+48)	address of v4 source
00002EDC	00000010			1966+	DC	A(16)	result length
00002EE0	00002F3C			1967+REA41	DC	A(RE41)	result address
00002EE8	00000000 00000000			1968+	DS	FD	gap
00002EF0	00000000 00000000			1969+V1041	DS	XL16	V1 output
00002EF8	00000000 00000000						
00002F00	00000000 00000000			1970+	DS	FD	gap
				1971+*			
00002F08				1972+X41	DS	0F	
00002F08	E310 5010 0014		00000010	1973+	LGF	R1,V2ADDR	load v2 source
00002F0E	E761 0000 0806		00000000	1974+	VL	v22,0(R1)	use v22 to test decoder
00002F14	E310 5014 0014		00000014	1975+	LGF	R1,V3ADDR	load v3 source
00002F1A	E771 0000 0806		00000000	1976+	VL	v23,0(R1)	use v23 to test decoder
00002F20	E310 5018 0014		00000018	1977+	LGF	R1,V4ADDR	load v4 source
00002F26	E781 0000 0806		00000000	1978+	VL	v24,0(R1)	use v24 to test decoder
00002F2C	E766 7300 8FAA			1979+	VMAL	V22,V22,V23,V24,3	test instruction (dest is a source)
00002F32	E760 5030 080E		00002EF0	1980+	VST	V22,V1041	save v1 output
00002F38	07FB			1981+	BR	R11	return
00002F3C				1982+RE41	DC	0F	xl16 expected result

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   LOC        OBJECT CODE      ADDR1    ADDR2    STMT

 00002F3C                                       1983+        DROP   R5
 00002F3C   26D2FE70 90F71480                   1984         DC     XL16'26D2FE7090F71480 B47CD8D5FF5B4940'    result
 00002F44   B47CD8D5 FF5B4940
 00002F4C   FF020304 05060750                   1985         DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
 00002F54   090A0B0C 0D0E0F7F
 00002F5C   00010102 02030328                   1986         DC     XL16'0001010202030328 0405053C0607073F'    v3
 00002F64   0405053C 0607073F
 00002F6C   20000000 00000000                   1987         DC     XL16'2000000000000000 FFFFFFFFFFFFFFFF'    v4
 00002F74   FFFFFFFF FFFFFFFF
                                                1988
                                                1989         VRR_D  VMAL,3
 00002F80                                       1990+        DS     0FD
 00002F80                      00002F80         1991+        USING  *,R5                  base for test data and test routine
 00002F80   00002FC8                            1992+T42     DC     A(X42)                address of test routine
 00002F84   002A                                1993+        DC     H'42'                 test number
 00002F86   00                                  1994+        DC     X'00'
 00002F87   03                                  1995+        DC     HL1'3'                m5
 00002F88   E5D4C1D3 40404040                   1996+        DC     CL8'VMAL'             instruction name
 00002F90   0000300C                            1997+        DC     A(RE42+16)            address of v2 source
 00002F94   0000301C                            1998+        DC     A(RE42+32)            address of v3 source
 00002F98   0000302C                            1999+        DC     A(RE42+48)            address of v4 source
 00002F9C   00000010                            2000+        DC     A(16)                 result length
 00002FA0   00002FFC                            2001+REA42   DC     A(RE42)               result address
 00002FA8   00000000 00000000                   2002+        DS     FD                    gap
 00002FB0   00000000 00000000                   2003+V1042   DS     XL16                  V1 output
 00002FB8   00000000 00000000
 00002FC0   00000000 00000000                   2004+        DS     FD                    gap
                                                2005+*
 00002FC8                                       2006+X42     DS     0F
 00002FC8   E310 5010 0014           00000010   2007+        LGF    R1,V2ADDR             load v2 source
 00002FCE   E761 0000 0806           00000000   2008+        VL     v22,0(R1)             use v22 to test decoder
 00002FD4   E310 5014 0014           00000014   2009+        LGF    R1,V3ADDR             load v3 source
 00002FDA   E771 0000 0806           00000000   2010+        VL     v23,0(R1)             use v23 to test decoder
 00002FE0   E310 5018 0014           00000018   2011+        LGF    R1,V4ADDR             load v4 source
 00002FE6   E781 0000 0806           00000000   2012+        VL     v24,0(R1)             use v24 to test decoder
 00002FEC   E766 7300 8FAA                      2013+        VMAL   V22,V22,V23,V24,3      test instruction (dest is a source)
 00002FF2   E760 5030 080E           00002FB0   2014+        VST    V22,V1042             save v1 output
 00002FF8   07FB                                2015+        BR     R11                   return
 00002FFC                                       2016+RE42    DC     0F                    xl16 expected result
 00002FFC                                       2017+        DROP   R5
 00002FFC   F6142E28 323C4921                   2018         DC     XL16'F6142E28323C4921 191C345060616772'    result
 00003004   191C3450 60616772
 0000300C   FF020304 05060750                   2019         DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
 00003014   090A0B0C 0D0E0F7F
 0000301C   00000000 0000000A                   2020         DC     XL16'000000000000000A 0101010F0101010F'    v3
 00003024   0101010F 0101010F
 0000302C   00001000 00000001                   2021         DC     XL16'0000100000000001 1000000000000001'    v4
 00003034   10000000 00000001
                                                2022
                                                2023 * Quadword
                                                2024         VRR_D  VMAL,4
 00003040                                       2025+        DS     0FD
 00003040                      00003040         2026+        USING  *,R5                  base for test data and test routine
 00003040   00003088                            2027+T43     DC     A(X43)                address of test routine
 00003044   002B                                2028+        DC     H'43'                 test number
 00003046   00                                  2029+        DC     X'00'
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  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

00003047  04                                   2030+        DC    HL1'4'                  m5
00003048  E5D4C1D3 40404040                    2031+        DC    CL8'VMAL'               instruction name
00003050  000030CC                             2032+        DC    A(RE43+16)              address of v2 source
00003054  000030DC                             2033+        DC    A(RE43+32)              address of v3 source
00003058  000030EC                             2034+        DC    A(RE43+48)              address of v4 source
0000305C  00000010                             2035+        DC    A(16)                   result length
00003060  000030BC                             2036+REA43   DC    A(RE43)                 result address
00003068  00000000 00000000                    2037+        DS    FD                      gap
00003070  00000000 00000000                    2038+V1043   DS    XL16                    V1 output
00003078  00000000 00000000
00003080  00000000 00000000                    2039+        DS    FD                      gap
                                               2040+*
00003088                                       2041+X43     DS    0F
00003088  E310 5010 0014              00000010  2042+        LGF   R1,V2ADDR               load v2 source
0000308E  E761 0000 0806              00000000  2043+        VL    v22,0(R1)               use v22 to test decoder
00003094  E310 5014 0014              00000014  2044+        LGF   R1,V3ADDR               load v3 source
0000309A  E771 0000 0806              00000000  2045+        VL    v23,0(R1)               use v23 to test decoder
000030A0  E310 5018 0014              00000018  2046+        LGF   R1,V4ADDR               load v4 source
000030A6  E781 0000 0806              00000000  2047+        VL    v24,0(R1)               use v24 to test decoder
000030AC  E766 7400 8FAA                        2048+        VMAL  V22,V22,V23,V24,4    test instruction (dest is a source)
000030B2  E760 5030 080E              00003070  2049+        VST   V22,V1043             save v1 output
000030B8  07FB                                  2050+        BR    R11                     return
000030BC                                        2051+RE43    DC    0F                      xl16 expected result
000030BC                                        2052+        DROP  R5
000030BC  02D2AEB6 AACD4C77                     2053         DC    XL16'02D2AEB6AACD4C77 96789F9F4FEDCC24'    result
000030C4  96789F9F 4FEDCC24
000030CC  FFFFFFFF 00019000                     2054         DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'    v2
000030D4  00000038 EEEEEEFA
000030DC  FFFFFFFF 00019000                     2055         DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'    v3
000030E4  00000038 0EEEEEFA
000030EC  00000000 00000000                     2056         DC    XL16'0000000000000000 0000000000000000'    v4
000030F4  00000000 00000000
                                               2057
                                               2058         VRR_D VMAL,4
00003100                                        2059+        DS    0FD
00003100                    00003100            2060+        USING *,R5               base for test data and test routine
00003100  00003148                              2061+T44     DC    A(X44)                  address of test routine
00003104  002C                                  2062+        DC    H'44'                   test number
00003106  00                                    2063+        DC    X'00'
00003107  04                                    2064+        DC    HL1'4'                  m5
00003108  E5D4C1D3 40404040                     2065+        DC    CL8'VMAL'               instruction name
00003110  0000318C                              2066+        DC    A(RE44+16)              address of v2 source
00003114  0000319C                              2067+        DC    A(RE44+32)              address of v3 source
00003118  000031AC                              2068+        DC    A(RE44+48)              address of v4 source
0000311C  00000010                              2069+        DC    A(16)                   result length
00003120  0000317C                              2070+REA44   DC    A(RE44)                 result address
00003128  00000000 00000000                     2071+        DS    FD                      gap
00003130  00000000 00000000                     2072+V1044   DS    XL16                    V1 output
00003138  00000000 00000000
00003140  00000000 00000000                     2073+        DS    FD                      gap
                                               2074+*
00003148                                        2075+X44     DS    0F
00003148  E310 5010 0014              00000010  2076+        LGF   R1,V2ADDR               load v2 source
0000314E  E761 0000 0806              00000000  2077+        VL    v22,0(R1)               use v22 to test decoder
00003154  E310 5014 0014              00000014  2078+        LGF   R1,V3ADDR               load v3 source
0000315A  E771 0000 0806              00000000  2079+        VL    v23,0(R1)               use v23 to test decoder
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003160   E310 5018 0014              00000018  2080+          LGF    R1,V4ADDR          load v4 source
00003166   E781 0000 0806              00000000  2081+          VL     v24,0(R1)          use v24 to test decoder
0000316C   E766 7400 8FAA                        2082+          VMAL   V22,V22,V23,V24,4    test instruction (dest is a source)
00003172   E760 5030 080E              00003130  2083+          VST    V22,V1044           save v1 output
00003178   07FB                                  2084+          BR     R11                return
0000317C                                         2085+RE44      DC     0F                 xl16 expected result
0000317C                                         2086+          DROP   R5
0000317C   599AFA6A 24295657                     2087           DC     XL16'599AFA6A24295657 252B55D498D42102'    result
00003184   252B55D4 98D42102
0000318C   FF020304 05060750                     2088           DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00003194   090A0B0C 0D0E0F7F
0000319C   01020304 05060750                     2089           DC     XL16'0102030405060750 090A0B780D0E0F7F'    v3
000031A4   090A0B78 0D0E0F7F
000031AC   10000000 00000001                     2090           DC     XL16'1000000000000001 1000000000000001'    v4
000031B4   10000000 00000001
                                                 2091
                                                 2092           VRR_D  VMAL,4
000031C0                                         2093+          DS     0FD
000031C0                        000031C0         2094+          USING  *,R5               base for test data and test routine
000031C0   00003208                              2095+T45       DC     A(X45)             address of test routine
000031C4   002D                                  2096+          DC     H'45'              test number
000031C6   00                                    2097+          DC     X'00'
000031C7   04                                    2098+          DC     HL1'4'             m5
000031C8   E5D4C1D3 40404040                     2099+          DC     CL8'VMAL'          instruction name
000031D0   0000324C                              2100+          DC     A(RE45+16)         address of v2 source
000031D4   0000325C                              2101+          DC     A(RE45+32)         address of v3 source
000031D8   0000326C                              2102+          DC     A(RE45+48)         address of v4 source
000031DC   00000010                              2103+          DC     A(16)              result length
000031E0   0000323C                              2104+REA45     DC     A(RE45)            result address
000031E8   00000000 00000000                     2105+          DS     FD                 gap
000031F0   00000000 00000000                     2106+V1045     DS     XL16               V1 output
000031F8   00000000 00000000
00003200   00000000 00000000                     2107+          DS     FD                 gap
                                                 2108+*
00003208                                         2109+X45       DS     0F
00003208   E310 5010 0014              00000010  2110+          LGF    R1,V2ADDR          load v2 source
0000320E   E761 0000 0806              00000000  2111+          VL     v22,0(R1)          use v22 to test decoder
00003214   E310 5014 0014              00000014  2112+          LGF    R1,V3ADDR          load v3 source
0000321A   E771 0000 0806              00000000  2113+          VL     v23,0(R1)          use v23 to test decoder
00003220   E310 5018 0014              00000018  2114+          LGF    R1,V4ADDR          load v4 source
00003226   E781 0000 0806              00000000  2115+          VL     v24,0(R1)          use v24 to test decoder
0000322C   E766 7400 8FAA                        2116+          VMAL   V22,V22,V23,V24,4    test instruction (dest is a source)
00003232   E760 5030 080E              000031F0  2117+          VST    V22,V1045           save v1 output
00003238   07FB                                  2118+          BR     R11                return
0000323C                                         2119+RE45      DC     0F                 xl16 expected result
0000323C                                         2120+          DROP   R5
0000323C   A5AC7D14 92F5ADEA                     2121           DC     XL16'A5AC7D1492F5ADEA B47CD8D5FF5B4940'    result
00003244   B47CD8D5 FF5B4940
0000324C   FF020304 05060750                     2122           DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00003254   090A0B0C 0D0E0F7F
0000325C   00010102 02030328                     2123           DC     XL16'0001010202030328 0405053C0607073F'    v3
00003264   0405053C 0607073F
0000326C   FFFFFFFF FFFFFFFF                     2124           DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v4
00003274   FFFFFFFF FFFFFFFF
                                                 2125
                                                 2126           VRR_D  VMAL,4
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   LOC         OBJECT CODE      ADDR1     ADDR2      STMT

00003280                                             2127+          DS     0FD
00003280                        00000280             2128+          USING  *,R5                      base for test data and test routine
00003280   000032C8                                  2129+T46       DC     A(X46)                     address of test routine
00003284   002E                                      2130+          DC     H'46'                      test number
00003286   00                                        2131+          DC     X'00'
00003287   04                                        2132+          DC     HL1'4'                     m5
00003288   E5D4C1D3 40404040                          2133+          DC     CL8'VMAL'                  instruction name
00003290   0000330C                                  2134+          DC     A(RE46+16)                 address of v2 source
00003294   0000331C                                  2135+          DC     A(RE46+32)                 address of v3 source
00003298   0000332C                                  2136+          DC     A(RE46+48)                 address of v4 source
0000329C   00000010                                  2137+          DC     A(16)                      result length
000032A0   000032FC                                  2138+REA46     DC     A(RE46)                    result address
000032A8   00000000 00000000                          2139+          DS     FD                         gap
000032B0   00000000 00000000                          2140+V1046     DS     XL16                       V1 output
000032B8   00000000 00000000
000032C0   00000000 00000000                          2141+          DS     FD                         gap
                                                     2142+*
000032C8                                             2143+X46        DS     0F
000032C8   E310 5010 0014            00000010        2144+          LGF    R1,V2ADDR                  load v2 source
000032CE   E761 0000 0806            00000000        2145+          VL     v22,0(R1)                  use v22 to test decoder
000032D4   E310 5014 0014            00000014        2146+          LGF    R1,V3ADDR                  load v3 source
000032DA   E771 0000 0806            00000000        2147+          VL     v23,0(R1)                  use v23 to test decoder
000032E0   E310 5018 0014            00000018        2148+          LGF    R1,V4ADDR                  load v4 source
000032E6   E781 0000 0806            00000000        2149+          VL     v24,0(R1)                  use v24 to test decoder
000032EC   E766 7400 8FAA                            2150+          VMAL   V22,V22,V23,V24,4          test instruction (dest is a source)
000032F2   E760 5030 080E            000032B0        2151+          VST    V22,V1046                  save v1 output
000032F8   07FB                                      2152+          BR     R11                        return
000032FC                                             2153+RE46      DC     0F                         xl16 expected result
000032FC                                             2154+          DROP   R5
000032FC   FD497B95 D40238A4                          2155           DC     XL16'FD497B95D40238A4 091C34506061676E'     result
00003304   091C3450 6061676E
0000330C   FF020304 05060750                          2156           DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'     v2
00003314   090A0B0C 0D0E0F7F
0000331C   00000000 0000000A                          2157           DC     XL16'000000000000000A 0101010F0101010F'     v3
00003324   0101010F 0101010F
0000332C   FFFFFFFF FFFFFFFF                          2158           DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFD'     v4
00003334   FFFFFFFF FFFFFFFD
                                                     2159
                                                     2160 *-------------------------------------------------------------
                                                     2161 *   VMAH   - Vector Multiply and Add High
                                                     2162 *-------------------------------------------------------------
                                                     2163 * Byte
                                                     2164          VRR_D  VMAH,0
00003340                                             2165+          DS     0FD
00003340                        00003340             2166+          USING  *,R5                      base for test data and test routine
00003340   00003388                                  2167+T47       DC     A(X47)                     address of test routine
00003344   002F                                      2168+          DC     H'47'                      test number
00003346   00                                        2169+          DC     X'00'
00003347   00                                        2170+          DC     HL1'0'                     m5
00003348   E5D4C1C8 40404040                          2171+          DC     CL8'VMAH'                  instruction name
00003350   000033CC                                  2172+          DC     A(RE47+16)                 address of v2 source
00003354   000033DC                                  2173+          DC     A(RE47+32)                 address of v3 source
00003358   000033EC                                  2174+          DC     A(RE47+48)                 address of v4 source
0000335C   00000010                                  2175+          DC     A(16)                      result length
00003360   000033BC                                  2176+REA47     DC     A(RE47)                    result address
00003368   00000000 00000000                          2177+          DS     FD                         gap
```

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  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

00003370  00000000 00000000                   2178+V1047  DS    XL16              V1 output
00003378  00000000 00000000
00003380  00000000 00000000                   2179+       DS    FD                gap
                                              2180+*
00003388                                      2181+X47    DS    0F
00003388  E310 5010 0014             00000010 2182+       LGF   R1,V2ADDR         load v2 source
0000338E  E761 0000 0806             00000000 2183+       VL    v22,0(R1)         use v22 to test decoder
00003394  E310 5014 0014             00000014 2184+       LGF   R1,V3ADDR         load v3 source
0000339A  E771 0000 0806             00000000 2185+       VL    v23,0(R1)         use v23 to test decoder
000033A0  E310 5018 0014             00000018 2186+       LGF   R1,V4ADDR         load v4 source
000033A6  E781 0000 0806             00000000 2187+       VL    v24,0(R1)         use v24 to test decoder
000033AC  E766 7000 8FAB                      2188+       VMAH  V22,V22,V23,V24,0  test instruction (dest is a source)
000033B2  E760 5030 080E             00003370 2189+       VST   V22,V1047          save v1 output
000033B8  07FB                                2190+       BR    R11               return
000033BC                                      2191+RE47   DC    0F                xl16 expected result
000033BC                                      2192+       DROP  R5
000033BC  00000000 00000002                   2193       DC    XL16'0000000000000002 0000000C00000000'   result
000033C4  0000000C 00000000
000033CC  FF000000 00000019                   2194       DC    XL16'FF00000000000019 00000038000000FA'   v2
000033D4  00000038 000000FA
000033DC  FF000000 00000019                   2195       DC    XL16'FF00000000000019 00000038000000FA'   v3
000033E4  00000038 000000FA
000033EC  00000000 00000000                   2196       DC    XL16'0000000000000000 0000000000000000'   v4
000033F4  00000000 00000000
                                              2197
                                              2198       VRR_D VMAH,0
00003400                                      2199+       DS    0FD
00003400               00003400               2200+       USING *,R5             base for test data and test routine
00003400  00003448                            2201+T48    DC    A(X48)            address of test routine
00003404  0030                                2202+       DC    H'48'             test number
00003406  00                                  2203+       DC    X'00'
00003407  00                                  2204+       DC    HL1'0'            m5
00003408  E5D4C1C8 40404040                   2205+       DC    CL8'VMAH'         instruction name
00003410  0000348C                            2206+       DC    A(RE48+16)        address of v2 source
00003414  0000349C                            2207+       DC    A(RE48+32)        address of v3 source
00003418  000034AC                            2208+       DC    A(RE48+48)        address of v4 source
0000341C  00000010                            2209+       DC    A(16)             result length
00003420  0000347C                            2210+REA48  DC    A(RE48)           result address
00003428  00000000 00000000                   2211+       DS    FD                gap
00003430  00000000 00000000                   2212+V1048  DS    XL16              V1 output
00003438  00000000 00000000
00003440  00000000 00000000                   2213+       DS    FD                gap
                                              2214+*
00003448                                      2215+X48    DS    0F
00003448  E310 5010 0014             00000010 2216+       LGF   R1,V2ADDR         load v2 source
0000344E  E761 0000 0806             00000000 2217+       VL    v22,0(R1)         use v22 to test decoder
00003454  E310 5014 0014             00000014 2218+       LGF   R1,V3ADDR         load v3 source
0000345A  E771 0000 0806             00000000 2219+       VL    v23,0(R1)         use v23 to test decoder
00003460  E310 5018 0014             00000018 2220+       LGF   R1,V4ADDR         load v4 source
00003466  E781 0000 0806             00000000 2221+       VL    v24,0(R1)         use v24 to test decoder
0000346C  E766 7000 8FAB                      2222+       VMAH  V22,V22,V23,V24,0  test instruction (dest is a source)
00003472  E760 5030 080E             00003430 2223+       VST   V22,V1048          save v1 output
00003478  07FB                                2224+       BR    R11               return
0000347C                                      2225+RE48   DC    0F                xl16 expected result
0000347C                                      2226+       DROP  R5
0000347C  00000000 00000006                   2227       DC    XL16'0000000000000006 0000000C00000000'   result
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003484	0000000C 00000000						
0000348C	FF0000FF 00000029			2228	DC	XL16'FF0000FF00000029 00000038000000FA'	v2
00003494	00000038 000000FA						
0000349C	FF000001 00000029			2229	DC	XL16'FF00000100000029 00000038000000FA'	v3
000034A4	00000038 000000FA						
000034AC	00000001 0000002F			2230	DC	XL16'000000010000002F 0000000300000002'	v4
000034B4	00000003 00000002						
				2231			
				2232	VRR_D	VMAH, 0	
000034C0				2233+	DS	0FD	
000034C0		000034C0		2234+	USING	*,R5	base for test data and test routine
000034C0	00003508			2235+T49	DC	A(X49)	address of test routine
000034C4	0031			2236+	DC	H'49'	test number
000034C6	00			2237+	DC	X'00'	
000034C7	00			2238+	DC	HL1'0'	m5
000034C8	E5D4C1C8 40404040			2239+	DC	CL8'VMAH'	instruction name
000034D0	0000354C			2240+	DC	A(RE49+16)	address of v2 source
000034D4	0000355C			2241+	DC	A(RE49+32)	address of v3 source
000034D8	0000356C			2242+	DC	A(RE49+48)	address of v4 source
000034DC	00000010			2243+	DC	A(16)	result length
000034E0	0000353C			2244+REA49	DC	A(RE49)	result address
000034E8	00000000 00000000			2245+	DS	FD	gap
000034F0	00000000 00000000			2246+V1049	DS	XL16	V1 output
000034F8	00000000 00000000						
00003500	00000000 00000000			2247+	DS	FD	gap
				2248+*			
00003508				2249+X49	DS	0F	
00003508	E310 5010 0014		00000010	2250+	LGF	R1, V2ADDR	load v2 source
0000350E	E761 0000 0806		00000000	2251+	VL	v22, 0(R1)	use v22 to test decoder
00003514	E310 5014 0014		00000014	2252+	LGF	R1, V3ADDR	load v3 source
0000351A	E771 0000 0806		00000000	2253+	VL	v23, 0(R1)	use v23 to test decoder
00003520	E310 5018 0014		00000018	2254+	LGF	R1, V4ADDR	load v4 source
00003526	E781 0000 0806		00000000	2255+	VL	v24, 0(R1)	use v24 to test decoder
0000352C	E766 7000 8FAB			2256+	VMAH	V22, V22, V23, V24, 0	test instruction (dest is a source)
00003532	E760 5030 080E		000034F0	2257+	VST	V22, V1049	save v1 output
00003538	07FB			2258+	BR	R11	return
0000353C				2259+RE49	DC	0F	xl16 expected result
0000353C				2260+	DROP	R5	
0000353C	FF000000 00000000			2261	DC	XL16'FF00000000000000 00000000000000FF'	result
00003544	00000000 000000FF						
0000354C	FF020304 05060708			2262	DC	XL16'FF02030405060708 090A0B0C0D0E0FF0'	v2
00003554	090A0B0C 0D0E0FF0						
0000355C	01020304 05060708			2263	DC	XL16'0102030405060708 090A0B0C0D0E0F10'	v3
00003564	090A0B0C 0D0E0F10						
0000356C	FF020304 05060708			2264	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00003574	090A0B0C 0D0E0F10						
				2265			
				2266	VRR_D	VMAH, 0	
00003580				2267+	DS	0FD	
00003580		00003580		2268+	USING	*,R5	base for test data and test routine
00003580	000035C8			2269+T50	DC	A(X50)	address of test routine
00003584	0032			2270+	DC	H'50'	test number
00003586	00			2271+	DC	X'00'	
00003587	00			2272+	DC	HL1'0'	m5
00003588	E5D4C1C8 40404040			2273+	DC	CL8'VMAH'	instruction name
00003590	0000360C			2274+	DC	A(RE50+16)	address of v2 source

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   LOC        OBJECT CODE      ADDR1     ADDR2      STMT

00003594   0000361C                                2275+         DC     A(RE50+32)       address of v3 source
00003598   0000362C                                2276+         DC     A(RE50+48)       address of v4 source
0000359C   00000010                                2277+         DC     A(16)            result length
000035A0   000035FC                                2278+REA50    DC     A(RE50)          result address
000035A8   00000000 00000000                       2279+         DS     FD               gap
000035B0   00000000 00000000                       2280+V1050    DS     XL16             V1 output
000035B8   00000000 00000000
000035C0   00000000 00000000                       2281+         DS     FD               gap

                                                   2282+*
000035C8                                           2283+X50      DS     0F
000035C8   E310 5010 0014              00000010     2284+        LGF    R1,V2ADDR        load v2 source
000035CE   E761 0000 0806              00000000     2285+        VL     v22,0(R1)        use v22 to test decoder
000035D4   E310 5014 0014              00000014     2286+        LGF    R1,V3ADDR        load v3 source
000035DA   E771 0000 0806              00000000     2287+        VL     v23,0(R1)        use v23 to test decoder
000035E0   E310 5018 0014              00000018     2288+        LGF    R1,V4ADDR        load v4 source
000035E6   E781 0000 0806              00000000     2289+        VL     v24,0(R1)        use v24 to test decoder
000035EC   E766 7000 8FAB                           2290+        VMAH   V22,V22,V23,V24,0   test instruction (dest is a source)
000035F2   E760 5030 080E              000035B0     2291+        VST    V22,V1050         save v1 output
000035F8   07FB                                     2292+        BR     R11              return
000035FC                                            2293+RE50    DC     0F               xl16 expected result
000035FC                                            2294+        DROP   R5
000035FC   FF000000 00000000                        2295         DC     XL16'FF00000000000000 00000000000000FF'    result
00003604   00000000 000000FF
0000360C   FF020304 05060708                        2296         DC     XL16'FF02030405060708 090A0B0C0D0E0FF0'    v2
00003614   090A0B0C 0D0E0FF0
0000361C   00010102 02030304                        2297         DC     XL16'0001010202030304 0405050606070708'    v3
00003624   04050506 06070708
0000362C   FF020304 05060708                        2298         DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00003634   090A0B0C 0D0E0F10

                                                   2299
                                                   2300          VRR_D  VMAH,0
00003640                                           2301+         DS     0FD
00003640                          00003640          2302+        USING  *,R5             base for test data and test routine
00003640   00003688                                 2303+T51     DC     A(X51)           address of test routine
00003644   0033                                     2304+        DC     H'51'            test number
00003646   00                                       2305+        DC     X'00'
00003647   00                                       2306+        DC     HL1'0'           m5
00003648   E5D4C1C8 40404040                        2307+        DC     CL8'VMAH'        instruction name
00003650   000036CC                                 2308+        DC     A(RE51+16)       address of v2 source
00003654   000036DC                                 2309+        DC     A(RE51+32)       address of v3 source
00003658   000036EC                                 2310+        DC     A(RE51+48)       address of v4 source
0000365C   00000010                                 2311+        DC     A(16)            result length
00003660   000036BC                                 2312+REA51   DC     A(RE51)          result address
00003668   00000000 00000000                        2313+        DS     FD               gap
00003670   00000000 00000000                        2314+V1051   DS     XL16             V1 output
00003678   00000000 00000000
00003680   00000000 00000000                        2315+        DS     FD               gap

                                                   2316+*
00003688                                           2317+X51      DS     0F
00003688   E310 5010 0014              00000010     2318+        LGF    R1,V2ADDR        load v2 source
0000368E   E761 0000 0806              00000000     2319+        VL     v22,0(R1)        use v22 to test decoder
00003694   E310 5014 0014              00000014     2320+        LGF    R1,V3ADDR        load v3 source
0000369A   E771 0000 0806              00000000     2321+        VL     v23,0(R1)        use v23 to test decoder
000036A0   E310 5018 0014              00000018     2322+        LGF    R1,V4ADDR        load v4 source
000036A6   E781 0000 0806              00000000     2323+        VL     v24,0(R1)        use v24 to test decoder
000036AC   E766 7000 8FAB                           2324+        VMAH   V22,V22,V23,V24,0   test instruction (dest is a source)
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000036B2	E760 5030 080E		00003670	2325+	VST	V22,V1051	save v1 output
000036B8	07FB			2326+	BR	R11	return
000036BC				2327+RE51	DC	0F	xl16 expected result
000036BC				2328+	DROP	R5	
000036BC	FF000000 00000000			2329	DC	XL16'FF00000000000000 00000000000000FF'	result
000036C4	00000000 000000FF						
000036CC	FF020304 05060708			2330	DC	XL16'FF02030405060708 090A0B0C0D0E0FF0'	v2
000036D4	090A0B0C 0D0E0FF0						
000036DC	00000000 00000001			2331	DC	XL16'0000000000000001 0101010101010102'	v3
000036E4	01010101 01010102						
000036EC	FF020304 05060708			2332	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
000036F4	090A0B0C 0D0E0F10						
				2333			
				2334	* Halfword		
				2335	VRR_D	VMAH,1	
00003700				2336+	DS	0FD	
00003700		00003700		2337+	USING	*,R5	base for test data and test routine
00003700	00003748			2338+T52	DC	A(X52)	address of test routine
00003704	0034			2339+	DC	H'52'	test number
00003706	00			2340+	DC	X'00'	
00003707	01			2341+	DC	HL1'1'	m5
00003708	E5D4C1C8 40404040			2342+	DC	CL8'VMAH'	instruction name
00003710	0000378C			2343+	DC	A(RE52+16)	address of v2 source
00003714	0000379C			2344+	DC	A(RE52+32)	address of v3 source
00003718	000037AC			2345+	DC	A(RE52+48)	address of v4 source
0000371C	00000010			2346+	DC	A(16)	result length
00003720	0000377C			2347+REA52	DC	A(RE52)	result address
00003728	00000000 00000000			2348+	DS	FD	gap
00003730	00000000 00000000			2349+V1052	DS	XL16	V1 output
00003738	00000000 00000000						
00003740	00000000 00000000			2350+	DS	FD	gap
				2351+*			
00003748				2352+X52	DS	0F	
00003748	E310 5010 0014		00000010	2353+	LGF	R1,V2ADDR	load v2 source
0000374E	E761 0000 0806		00000000	2354+	VL	v22,0(R1)	use v22 to test decoder
00003754	E310 5014 0014		00000014	2355+	LGF	R1,V3ADDR	load v3 source
0000375A	E771 0000 0806		00000000	2356+	VL	v23,0(R1)	use v23 to test decoder
00003760	E310 5018 0014		00000018	2357+	LGF	R1,V4ADDR	load v4 source
00003766	E781 0000 0806		00000000	2358+	VL	v24,0(R1)	use v24 to test decoder
0000376C	E766 7100 8FAB			2359+	VMAH	V22,V22,V23,V24,1	test instruction (dest is a source)
00003772	E760 5030 080E		00003730	2360+	VST	V22,V1052	save v1 output
00003778	07FB			2361+	BR	R11	return
0000377C				2362+RE52	DC	0F	xl16 expected result
0000377C				2363+	DROP	R5	
0000377C	00010000 00000000			2364	DC	XL16'0001000000000000 0000000000000000'	result
00003784	00000000 00000000						
0000378C	FF000000 00000019			2365	DC	XL16'FF00000000000019 00000038000000FA'	v2
00003794	00000038 000000FA						
0000379C	FF000000 00000019			2366	DC	XL16'FF00000000000019 00000038000000FA'	v3
000037A4	00000038 000000FA						
000037AC	00000000 00000000			2367	DC	XL16'0000000000000000 0000000000000000'	v4
000037B4	00000000 00000000						
				2368			
				2369	VRR_D	VMAH,1	
000037C0				2370+	DS	0FD	
000037C0		000037C0		2371+	USING	*,R5	base for test data and test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000037C0	00003808			2372+T53	DC	A(X53)	address of test routine
000037C4	0035			2373+	DC	H'53'	test number
000037C6	00			2374+	DC	X'00'	
000037C7	01			2375+	DC	HL1'1'	m5
000037C8	E5D4C1C8 40404040			2376+	DC	CL8'VMAH'	instruction name
000037D0	0000384C			2377+	DC	A(RE53+16)	address of v2 source
000037D4	0000385C			2378+	DC	A(RE53+32)	address of v3 source
000037D8	0000386C			2379+	DC	A(RE53+48)	address of v4 source
000037DC	00000010			2380+	DC	A(16)	result length
000037E0	0000383C			2381+REA53	DC	A(RE53)	result address
000037E8	00000000 00000000			2382+	DS	FD	gap
000037F0	00000000 00000000			2383+V1053	DS	XL16	V1 output
000037F8	00000000 00000000						
00003800	00000000 00000000			2384+	DS	FD	gap
				2385+*			
00003808				2386+X53	DS	0F	
00003808	E310 5010 0014		00000010	2387+	LGF	R1,V2ADDR	load v2 source
0000380E	E761 0000 0806		00000000	2388+	VL	v22,0(R1)	use v22 to test decoder
00003814	E310 5014 0014		00000014	2389+	LGF	R1,V3ADDR	load v3 source
0000381A	E771 0000 0806		00000000	2390+	VL	v23,0(R1)	use v23 to test decoder
00003820	E310 5018 0014		00000018	2391+	LGF	R1,V4ADDR	load v4 source
00003826	E781 0000 0806		00000000	2392+	VL	v24,0(R1)	use v24 to test decoder
0000382C	E766 7100 8FAB			2393+	VMAH	V22,V22,V23,V24,1	test instruction (dest is a source)
00003832	E760 5030 080E		000037F0	2394+	VST	V22,V1053	save v1 output
00003838	07FB			2395+	BR	R11	return
0000383C				2396+RE53	DC	0F	xl16 expected result
0000383C				2397+	DROP	R5	
0000383C	00010000 00000000			2398	DC	XL16'0001000000000000 0000000000000000'	result
00003844	00000000 00000000						
0000384C	FF0000FF 00000029			2399	DC	XL16'FF0000FF00000029 00000038000000FA'	v2
00003854	00000038 000000FA						
0000385C	FF000001 00000029			2400	DC	XL16'FF00000100000029 00000038000000FA'	v3
00003864	00000038 000000FA						
0000386C	00000001 0000002F			2401	DC	XL16'000000010000002F 0000000300000002'	v4
00003874	00000003 00000002						
				2402			
				2403	VRR_D	VMAH,1	
00003880				2404+	DS	0FD	
00003880		00003880		2405+	USING	*,R5	base for test data and test routine
00003880	000038C8			2406+T54	DC	A(X54)	address of test routine
00003884	0036			2407+	DC	H'54'	test number
00003886	00			2408+	DC	X'00'	
00003887	01			2409+	DC	HL1'1'	m5
00003888	E5D4C1C8 40404040			2410+	DC	CL8'VMAH'	instruction name
00003890	0000390C			2411+	DC	A(RE54+16)	address of v2 source
00003894	0000391C			2412+	DC	A(RE54+32)	address of v3 source
00003898	0000392C			2413+	DC	A(RE54+48)	address of v4 source
0000389C	00000010			2414+	DC	A(16)	result length
000038A0	000038FC			2415+REA54	DC	A(RE54)	result address
000038A8	00000000 00000000			2416+	DS	FD	gap
000038B0	00000000 00000000			2417+V1054	DS	XL16	V1 output
000038B8	00000000 00000000						
000038C0	00000000 00000000			2418+	DS	FD	gap
				2419+*			
000038C8				2420+X54	DS	0F	
000038C8	E310 5010 0014		00000010	2421+	LGF	R1,V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000038CE	E761 0000 0806		00000000	2422+	VL	v22,0(R1)	use v22 to test decoder
000038D4	E310 5014 0014		00000014	2423+	LGF	R1,V3ADDR	load v3 source
000038DA	E771 0000 0806		00000000	2424+	VL	v23,0(R1)	use v23 to test decoder
000038E0	E310 5018 0014		00000018	2425+	LGF	R1,V4ADDR	load v4 source
000038E6	E781 0000 0806		00000000	2426+	VL	v24,0(R1)	use v24 to test decoder
000038EC	E766 7100 8FAB			2427+	VMAH	V22,V22,V23,V24,1	test instruction (dest is a source)
000038F2	E760 5030 080E		000038B0	2428+	VST	V22,V1054	save v1 output
000038F8	07FB			2429+	BR	R11	return
000038FC				2430+RE54	DC	0F	xl16 expected result
000038FC				2431+	DROP	R5	
000038FC	FFFE0009 00190031			2432	DC	XL16'FFFE000900190031 0051007AFF57FF1F'	result
00003904	0051007A FF57FF1F						
0000390C	FF020304 05060708			2433	DC	XL16'FF02030405060708 090A0B0CF30EF110'	v2
00003914	090A0B0C F30EF110						
0000391C	01020304 05060708			2434	DC	XL16'0102030405060708 090A0B0C0D0E0F10'	v3
00003924	090A0B0C 0D0E0F10						
0000392C	FF020304 05060708			2435	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00003934	090A0B0C 0D0E0F10						
				2436			
				2437	VRR_D	VMAH,1	
00003940				2438+	DS	0FD	
00003940		00003940		2439+	USING	*,R5	base for test data and test routine
00003940	00003988			2440+T55	DC	A(X55)	address of test routine
00003944	0037			2441+	DC	H'55'	test number
00003946	00			2442+	DC	X'00'	
00003947	01			2443+	DC	HL1'1'	m5
00003948	E5D4C1C8 40404040			2444+	DC	CL8'VMAH'	instruction name
00003950	000039CC			2445+	DC	A(RE55+16)	address of v2 source
00003954	000039DC			2446+	DC	A(RE55+32)	address of v3 source
00003958	000039EC			2447+	DC	A(RE55+48)	address of v4 source
0000395C	00000010			2448+	DC	A(16)	result length
00003960	000039BC			2449+REA55	DC	A(RE55)	result address
00003968	00000000 00000000			2450+	DS	FD	gap
00003970	00000000 00000000			2451+V1055	DS	XL16	V1 output
00003978	00000000 00000000						
00003980	00000000 00000000			2452+	DS	FD	gap
				2453+*			
00003988				2454+X55	DS	0F	
00003988	E310 5010 0014		00000010	2455+	LGF	R1,V2ADDR	load v2 source
0000398E	E761 0000 0806		00000000	2456+	VL	v22,0(R1)	use v22 to test decoder
00003994	E310 5014 0014		00000014	2457+	LGF	R1,V3ADDR	load v3 source
0000399A	E771 0000 0806		00000000	2458+	VL	v23,0(R1)	use v23 to test decoder
000039A0	E310 5018 0014		00000018	2459+	LGF	R1,V4ADDR	load v4 source
000039A6	E781 0000 0806		00000000	2460+	VL	v24,0(R1)	use v24 to test decoder
000039AC	E766 7100 8FAB			2461+	VMAH	V22,V22,V23,V24,1	test instruction (dest is a source)
000039B2	E760 5030 080E		00003970	2462+	VST	V22,V1055	save v1 output
000039B8	07FB			2463+	BR	R11	return
000039BC				2464+RE55	DC	0F	xl16 expected result
000039BC				2465+	DROP	R5	
000039BC	FFFF0003 000A0015			2466	DC	XL16'FFFF0003000A0015 00240037FFB2FF97'	result
000039C4	00240037 FFB2FF97						
000039CC	FF020304 05060708			2467	DC	XL16'FF02030405060708 090A0B0CF30EF110'	v2
000039D4	090A0B0C F30EF110						
000039DC	00010102 02030304			2468	DC	XL16'0001010202030304 0405050606070708'	v3
000039E4	04050506 06070708						
000039EC	FF020304 05060708			2469	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000039F4	090A0B0C 0D0E0F10						
				2470			
				2471	VRR_D	VMAH, 1	
00003A00				2472+	DS	0FD	
00003A00		00003A00		2473+	USING	*, R5	base for test data and test routine
00003A00	00003A48			2474+T56	DC	A(X56)	address of test routine
00003A04	0038			2475+	DC	H'56'	test number
00003A06	00			2476+	DC	X'00'	
00003A07	01			2477+	DC	HL1'1'	m5
00003A08	E5D4C1C8 40404040			2478+	DC	CL8'VMAH'	instruction name
00003A10	00003A8C			2479+	DC	A(RE56+16)	address of v2 source
00003A14	00003A9C			2480+	DC	A(RE56+32)	address of v3 source
00003A18	00003AAC			2481+	DC	A(RE56+48)	address of v4 source
00003A1C	00000010			2482+	DC	A(16)	result length
00003A20	00003A7C			2483+REA56	DC	A(RE56)	result address
00003A28	00000000 00000000			2484+	DS	FD	gap
00003A30	00000000 00000000			2485+V1056	DS	XL16	V1 output
00003A38	00000000 00000000						
00003A40	00000000 00000000			2486+	DS	FD	gap
				2487+*			
00003A48				2488+X56	DS	0F	
00003A48	E310 5010 0014		00000010	2489+	LGF	R1, V2ADDR	load v2 source
00003A4E	E761 0000 0806		00000000	2490+	VL	v22, 0(R1)	use v22 to test decoder
00003A54	E310 5014 0014		00000014	2491+	LGF	R1, V3ADDR	load v3 source
00003A5A	E771 0000 0806		00000000	2492+	VL	v23, 0(R1)	use v23 to test decoder
00003A60	E310 5018 0014		00000018	2493+	LGF	R1, V4ADDR	load v4 source
00003A66	E781 0000 0806		00000000	2494+	VL	v24, 0(R1)	use v24 to test decoder
00003A6C	E766 7100 8FAB			2495+	VMAH	V22, V22, V23, V24, 1	test instruction (dest is a source)
00003A72	E760 5030 080E		00003A30	2496+	VST	V22, V1056	save v1 output
00003A78	07FB			2497+	BR	R11	return
00003A7C				2498+RE56	DC	0F	xl16 expected result
00003A7C				2499+	DROP	R5	
00003A7C	FFFF0000 00000000			2500	DC	XL16'FFFF000000000000 0009000BFFF3FFF1'	result
00003A84	0009000B FFF3FFF1						
00003A8C	FF020304 05060708			2501	DC	XL16'FF02030405060708 090A0B0CF30EF110'	v2
00003A94	090A0B0C F30EF110						
00003A9C	00000000 00000001			2502	DC	XL16'0000000000000001 0101010101010102'	v3
00003AA4	01010101 01010102						
00003AAC	FF020304 05060708			2503	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00003AB4	090A0B0C 0D0E0F10						
				2504			
				2505	* Word		
				2506	VRR_D	VMAH, 2	
00003AC0				2507+	DS	0FD	
00003AC0		00003AC0		2508+	USING	*, R5	base for test data and test routine
00003AC0	00003B08			2509+T57	DC	A(X57)	address of test routine
00003AC4	0039			2510+	DC	H'57'	test number
00003AC6	00			2511+	DC	X'00'	
00003AC7	02			2512+	DC	HL1'2'	m5
00003AC8	E5D4C1C8 40404040			2513+	DC	CL8'VMAH'	instruction name
00003AD0	00003B4C			2514+	DC	A(RE57+16)	address of v2 source
00003AD4	00003B5C			2515+	DC	A(RE57+32)	address of v3 source
00003AD8	00003B6C			2516+	DC	A(RE57+48)	address of v4 source
00003ADC	00000010			2517+	DC	A(16)	result length
00003AE0	00003B3C			2518+REA57	DC	A(RE57)	result address
00003AE8	00000000 00000000			2519+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003AF0	00000000 00000000			2520+V1057	DS	XL16	V1 output
00003AF8	00000000 00000000						
00003B00	00000000 00000000			2521+	DS	FD	gap
				2522+*			
00003B08				2523+X57	DS	0F	
00003B08	E310 5010 0014		00000010	2524+	LGF	R1,V2ADDR	load v2 source
00003B0E	E761 0000 0806		00000000	2525+	VL	v22,0(R1)	use v22 to test decoder
00003B14	E310 5014 0014		00000014	2526+	LGF	R1,V3ADDR	load v3 source
00003B1A	E771 0000 0806		00000000	2527+	VL	v23,0(R1)	use v23 to test decoder
00003B20	E310 5018 0014		00000018	2528+	LGF	R1,V4ADDR	load v4 source
00003B26	E781 0000 0806		00000000	2529+	VL	v24,0(R1)	use v24 to test decoder
00003B2C	E766 7200 8FAB			2530+	VMAH	V22,V22,V23,V24,2	test instruction (dest is a source)
00003B32	E760 5030 080E		00003AF0	2531+	VST	V22,V1057	save v1 output
00003B38	07FB			2532+	BR	R11	return
00003B3C				2533+RE57	DC	0F	xl16 expected result
00003B3C				2534+	DROP	R5	
00003B3C	00010000 00000000			2535	DC	XL16'0001000000000000 0000000000000000'	result
00003B44	00000000 00000000						
00003B4C	FF000000 00000019			2536	DC	XL16'FF00000000000019 00000038000000FA'	v2
00003B54	00000038 000000FA						
00003B5C	FF000000 00000019			2537	DC	XL16'FF00000000000019 00000038000000FA'	v3
00003B64	00000038 000000FA						
00003B6C	00000000 00000000			2538	DC	XL16'0000000000000000 0000000000000000'	v4
00003B74	00000000 00000000						
				2539			
				2540	VRR_D	VMAH,2	
00003B80				2541+	DS	0FD	
00003B80		00003B80		2542+	USING	*,R5	base for test data and test routine
00003B80	00003BC8			2543+T58	DC	A(X58)	address of test routine
00003B84	003A			2544+	DC	H'58'	test number
00003B86	00			2545+	DC	X'00'	
00003B87	02			2546+	DC	HL1'2'	m5
00003B88	E5D4C1C8 40404040			2547+	DC	CL8'VMAH'	instruction name
00003B90	00003C0C			2548+	DC	A(RE58+16)	address of v2 source
00003B94	00003C1C			2549+	DC	A(RE58+32)	address of v3 source
00003B98	00003C2C			2550+	DC	A(RE58+48)	address of v4 source
00003B9C	00000010			2551+	DC	A(16)	result length
00003BA0	00003BFC			2552+REA58	DC	A(RE58)	result address
00003BA8	00000000 00000000			2553+	DS	FD	gap
00003BB0	00000000 00000000			2554+V1058	DS	XL16	V1 output
00003BB8	00000000 00000000						
00003BC0	00000000 00000000			2555+	DS	FD	gap
				2556+*			
00003BC8				2557+X58	DS	0F	
00003BC8	E310 5010 0014		00000010	2558+	LGF	R1,V2ADDR	load v2 source
00003BCE	E761 0000 0806		00000000	2559+	VL	v22,0(R1)	use v22 to test decoder
00003BD4	E310 5014 0014		00000014	2560+	LGF	R1,V3ADDR	load v3 source
00003BDA	E771 0000 0806		00000000	2561+	VL	v23,0(R1)	use v23 to test decoder
00003BE0	E310 5018 0014		00000018	2562+	LGF	R1,V4ADDR	load v4 source
00003BE6	E781 0000 0806		00000000	2563+	VL	v24,0(R1)	use v24 to test decoder
00003BEC	E766 7200 8FAB			2564+	VMAH	V22,V22,V23,V24,2	test instruction (dest is a source)
00003BF2	E760 5030 080E		00003BB0	2565+	VST	V22,V1058	save v1 output
00003BF8	07FB			2566+	BR	R11	return
00003BFC				2567+RE58	DC	0F	xl16 expected result
00003BFC				2568+	DROP	R5	
00003BFC	0000FFFF 00000000			2569	DC	XL16'0000FFFF00000000 0000000000000000'	result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003C04	00000000 00000000						
00003C0C	FF0000FF 00000029			2570	DC	XL16'FF0000FF00000029 00000038000000FA'	v2
00003C14	00000038 000000FA						
00003C1C	FF000001 00000029			2571	DC	XL16'FF00000100000029 00000038000000FA'	v3
00003C24	00000038 000000FA						
00003C2C	00000001 0000002F			2572	DC	XL16'000000010000002F 0000000300000002'	v4
00003C34	00000003 00000002						
				2573			
				2574		VRR_D VMAH, 2	
00003C40				2575+	DS	0FD	
00003C40		00003C40		2576+	USING	*, R5	base for test data and test routine
00003C40	00003C88			2577+T59	DC	A(X59)	address of test routine
00003C44	003B			2578+	DC	H'59'	test number
00003C46	00			2579+	DC	X'00'	
00003C47	02			2580+	DC	HL1'2'	m5
00003C48	E5D4C1C8 40404040			2581+	DC	CL8'VMAH'	instruction name
00003C50	00003CCC			2582+	DC	A(RE59+16)	address of v2 source
00003C54	00003CDC			2583+	DC	A(RE59+32)	address of v3 source
00003C58	00003CEC			2584+	DC	A(RE59+48)	address of v4 source
00003C5C	00000010			2585+	DC	A(16)	result length
00003C60	00003CBC			2586+REA59	DC	A(RE59)	result address
00003C68	00000000 00000000			2587+	DS	FD	gap
00003C70	00000000 00000000			2588+V1059	DS	XL16	V1 output
00003C78	00000000 00000000						
00003C80	00000000 00000000			2589+	DS	FD	gap
				2590+*			
00003C88				2591+X59	DS	0F	
00003C88	E310 5010 0014		00000010	2592+	LGF	R1, V2ADDR	load v2 source
00003C8E	E761 0000 0806		00000000	2593+	VL	v22, 0(R1)	use v22 to test decoder
00003C94	E310 5014 0014		00000014	2594+	LGF	R1, V3ADDR	load v3 source
00003C9A	E771 0000 0806		00000000	2595+	VL	v23, 0(R1)	use v23 to test decoder
00003CA0	E310 5018 0014		00000018	2596+	LGF	R1, V4ADDR	load v4 source
00003CA6	E781 0000 0806		00000000	2597+	VL	v24, 0(R1)	use v24 to test decoder
00003CAC	E766 7200 8FAB			2598+	VMAH	V22, V22, V23, V24, 2	test instruction (dest is a source)
00003CB2	E760 5030 080E		00003C70	2599+	VST	V22, V1059	save v1 output
00003CB8	07FB			2600+	BR	R11	return
00003CBC				2601+RE59	DC	0F	xl16 expected result
00003CBC				2602+	DROP	R5	
00003CBC	FFFF0004 00193C6A			2603	DC	XL16'FFFF000400193C6A 0051B52BFF5700C5'	result
00003CC4	0051B52B FF5700C5						
00003CCC	FF020304 05060708			2604	DC	XL16'FF02030405060708 090A0B0CF30E0F10'	v2
00003CD4	090A0B0C F30E0F10						
00003CDC	01020304 05060708			2605	DC	XL16'0102030405060708 090A0B0C0D0E0F10'	v3
00003CE4	090A0B0C 0D0E0F10						
00003CEC	FF020304 05060708			2606	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00003CF4	090A0B0C 0D0E0F10						
				2607			
				2608		VRR_D VMAH, 2	
00003D00				2609+	DS	0FD	
00003D00		00003D00		2610+	USING	*, R5	base for test data and test routine
00003D00	00003D48			2611+T60	DC	A(X60)	address of test routine
00003D04	003C			2612+	DC	H'60'	test number
00003D06	00			2613+	DC	X'00'	
00003D07	02			2614+	DC	HL1'2'	m5
00003D08	E5D4C1C8 40404040			2615+	DC	CL8'VMAH'	instruction name
00003D10	00003D8C			2616+	DC	A(RE60+16)	address of v2 source

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  LOC          OBJECT CODE       ADDR1     ADDR2     STMT

00003D14    00003D9C                                2617+        DC     A(RE60+32)          address of v3 source
00003D18    00003DAC                                2618+        DC     A(RE60+48)          address of v4 source
00003D1C    00000010                                2619+        DC     A(16)               result length
00003D20    00003D7C                                2620+REA60   DC     A(RE60)             result address
00003D28    00000000 00000000                       2621+        DS     FD                  gap
00003D30    00000000 00000000                       2622+V1060   DS     XL16                V1 output
00003D38    00000000 00000000
00003D40    00000000 00000000                       2623+        DS     FD                  gap
                                                    2624+*
00003D48                                            2625+X60     DS     0F
00003D48    E310 5010 0014              00000010    2626+        LGF    R1,V2ADDR           load v2 source
00003D4E    E761 0000 0806              00000000    2627+        VL     v22,0(R1)           use v22 to test decoder
00003D54    E310 5014 0014              00000014    2628+        LGF    R1,V3ADDR           load v3 source
00003D5A    E771 0000 0806              00000000    2629+        VL     v23,0(R1)           use v23 to test decoder
00003D60    E310 5018 0014              00000018    2630+        LGF    R1,V4ADDR           load v4 source
00003D66    E781 0000 0806              00000000    2631+        VL     v24,0(R1)           use v24 to test decoder
00003D6C    E766 7200 8FAB                          2632+        VMAH   V22,V22,V23,V24,2     test instruction (dest is a source)
00003D72    E760 5030 080E              00003D30    2633+        VST    V22,V1060            save v1 output
00003D78    07FB                                    2634+        BR     R11                 return
00003D7C                                            2635+RE60    DC     0F                  xl16 expected result
00003D7C                                            2636+        DROP   R5
00003D7C    FFFFFF01 000A1B2F                       2637         DC     XL16'FFFFFF01000A1B2F 0024558BFFB1F961'    result
00003D84    0024558B FFB1F961
00003D8C    FF020304 05060708                       2638         DC     XL16'FF02030405060708 090A0B0CF30E0F10'    v2
00003D94    090A0B0C F30E0F10
00003D9C    00010102 02030304                       2639         DC     XL16'0001010202030304 0405050606070708'    v3
00003DA4    04050506 06070708
00003DAC    FF020304 05060708                       2640         DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00003DB4    090A0B0C 0D0E0F10
                                                    2641
                                                    2642         VRR_D  VMAH,2
00003DC0                                            2643+        DS     0FD
00003DC0                  00003DC0                  2644+        USING  *,R5                base for test data and test routine
00003DC0    00003E08                                2645+T61     DC     A(X61)              address of test routine
00003DC4    003D                                    2646+        DC     H'61'               test number
00003DC6    00                                      2647+        DC     X'00'
00003DC7    02                                      2648+        DC     HL1'2'              m5
00003DC8    E5D4C1C8 40404040                       2649+        DC     CL8'VMAH'           instruction name
00003DD0    00003E4C                                2650+        DC     A(RE61+16)          address of v2 source
00003DD4    00003E5C                                2651+        DC     A(RE61+32)          address of v3 source
00003DD8    00003E6C                                2652+        DC     A(RE61+48)          address of v4 source
00003DDC    00000010                                2653+        DC     A(16)               result length
00003DE0    00003E3C                                2654+REA61   DC     A(RE61)             result address
00003DE8    00000000 00000000                       2655+        DS     FD                  gap
00003DF0    00000000 00000000                       2656+V1061   DS     XL16                V1 output
00003DF8    00000000 00000000
00003E00    00000000 00000000                       2657+        DS     FD                  gap
                                                    2658+*
00003E08                                            2659+X61     DS     0F
00003E08    E310 5010 0014              00000010    2660+        LGF    R1,V2ADDR           load v2 source
00003E0E    E761 0000 0806              00000000    2661+        VL     v22,0(R1)           use v22 to test decoder
00003E14    E310 5014 0014              00000014    2662+        LGF    R1,V3ADDR           load v3 source
00003E1A    E771 0000 0806              00000000    2663+        VL     v23,0(R1)           use v23 to test decoder
00003E20    E310 5018 0014              00000018    2664+        LGF    R1,V4ADDR           load v4 source
00003E26    E781 0000 0806              00000000    2665+        VL     v24,0(R1)           use v24 to test decoder
00003E2C    E766 7200 8FAB                          2666+        VMAH   V22,V22,V23,V24,2     test instruction (dest is a source)
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003E32	E760 5030 080E		00003DF0	2667+	VST	V22,V1061	save v1 output
00003E38	07FB			2668+	BR	R11	return
00003E3C				2669+RE61	DC	0F	xl16 expected result
00003E3C				2670+	DROP	R5	
00003E3C	FFFFFFFF 00000000			2671	DC	XL16'FFFFFFFF00000000 0009131EFFF30110'	result
00003E44	0009131E FFF30110						
00003E4C	FF020304 05060708			2672	DC	XL16'FF02030405060708 090A0B0CF30E0F10'	v2
00003E54	090A0B0C F30E0F10						
00003E5C	00000000 00000001			2673	DC	XL16'0000000000000001 0101010101010102'	v3
00003E64	01010101 01010102						
00003E6C	FF020304 05060708			2674	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00003E74	090A0B0C 0D0E0F10						
				2675			
				2676	* Doubleword		
				2677		VRR_D VMAH,3	
00003E80				2678+	DS	0FD	
00003E80			00003E80	2679+	USING	*,R5	base for test data and test routine
00003E80	00003EC8			2680+T62	DC	A(X62)	address of test routine
00003E84	003E			2681+	DC	H'62'	test number
00003E86	00			2682+	DC	X'00'	
00003E87	03			2683+	DC	HL1'3'	m5
00003E88	E5D4C1C8 40404040			2684+	DC	CL8'VMAH'	instruction name
00003E90	00003F0C			2685+	DC	A(RE62+16)	address of v2 source
00003E94	00003F1C			2686+	DC	A(RE62+32)	address of v3 source
00003E98	00003F2C			2687+	DC	A(RE62+48)	address of v4 source
00003E9C	00000010			2688+	DC	A(16)	result length
00003EA0	00003EFC			2689+REA62	DC	A(RE62)	result address
00003EA8	00000000 00000000			2690+	DS	FD	gap
00003EB0	00000000 00000000			2691+V1062	DS	XL16	V1 output
00003EB8	00000000 00000000						
00003EC0	00000000 00000000			2692+	DS	FD	gap
				2693+*			
00003EC8				2694+X62	DS	0F	
00003EC8	E310 5010 0014		00000010	2695+	LGF	R1,V2ADDR	load v2 source
00003ECE	E761 0000 0806		00000000	2696+	VL	v22,0(R1)	use v22 to test decoder
00003ED4	E310 5014 0014		00000014	2697+	LGF	R1,V3ADDR	load v3 source
00003EDA	E771 0000 0806		00000000	2698+	VL	v23,0(R1)	use v23 to test decoder
00003EE0	E310 5018 0014		00000018	2699+	LGF	R1,V4ADDR	load v4 source
00003EE6	E781 0000 0806		00000000	2700+	VL	v24,0(R1)	use v24 to test decoder
00003EEC	E766 7300 8FAB			2701+	VMAH	V22,V22,V23,V24,3	test instruction (dest is a source)
00003EF2	E760 5030 080E		00003EB0	2702+	VST	V22,V1062	save v1 output
00003EF8	07FB			2703+	BR	R11	return
00003EFC				2704+RE62	DC	0F	xl16 expected result
00003EFC				2705+	DROP	R5	
00003EFC	00000000 00000000			2706	DC	XL16'0000000000000000 0000000000000C77'	result
00003F04	00000000 00000C77						
00003F0C	FFFFFFFF 00019000			2707	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00003F14	00000038 EEEEEEFA						
00003F1C	FFFFFFFF 00019000			2708	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00003F24	00000038 0EEEEEFA						
00003F2C	00000000 00000000			2709	DC	XL16'0000000000000000 0000000000000000'	v4
00003F34	00000000 00000000						
				2710			
				2711		VRR_D VMAH,3	
00003F40				2712+	DS	0FD	
00003F40			00003F40	2713+	USING	*,R5	base for test data and test routine

```
  LOC        OBJECT CODE     ADDR1      ADDR2     STMT

00003F40   00003F88                              2714+T63    DC     A(X63)              address of test routine
00003F44   003F                                  2715+       DC     H'63'               test number
00003F46   00                                    2716+       DC     X'00'
00003F47   03                                    2717+       DC     HL1'3'              m5
00003F48   E5D4C1C8 40404040                     2718+       DC     CL8'VMAH'           instruction name
00003F50   00003FCC                              2719+       DC     A(RE63+16)          address of v2 source
00003F54   00003FDC                              2720+       DC     A(RE63+32)          address of v3 source
00003F58   00003FEC                              2721+       DC     A(RE63+48)          address of v4 source
00003F5C   00000010                              2722+       DC     A(16)               result length
00003F60   00003FBC                              2723+REA63  DC     A(RE63)             result address
00003F68   00000000 00000000                     2724+       DS     FD                  gap
00003F70   00000000 00000000                     2725+V1063  DS     XL16                V1 output
00003F78   00000000 00000000
00003F80   00000000 00000000                     2726+       DS     FD                  gap
                                                 2727+*
00003F88                                         2728+X63    DS     0F
00003F88   E310 5010 0014              00000010  2729+       LGF    R1,V2ADDR           load v2 source
00003F8E   E761 0000 0806              00000000  2730+       VL     v22,0(R1)           use v22 to test decoder
00003F94   E310 5014 0014              00000014  2731+       LGF    R1,V3ADDR           load v3 source
00003F9A   E771 0000 0806              00000000  2732+       VL     v23,0(R1)           use v23 to test decoder
00003FA0   E310 5018 0014              00000018  2733+       LGF    R1,V4ADDR           load v4 source
00003FA6   E781 0000 0806              00000000  2734+       VL     v24,0(R1)           use v24 to test decoder
00003FAC   E766 7300 8FAB                        2735+       VMAH   V22,V22,V23,V24,3    test instruction (dest is a source)
00003FB2   E760 5030 080E              00003F70  2736+       VST    V22,V1063            save v1 output
00003FB8   07FB                                  2737+       BR     R11                 return
00003FBC                                         2738+RE63   DC     0F                  xl16 expected result
00003FBC                                         2739+       DROP   R5
00003FBC   FFFF0004 0C192C46                     2740        DC     XL16'FFFF00040C192C46 0051B52F8692B4F6'    result
00003FC4   0051B52F 8692B4F6
00003FCC   FF020304 05060750                     2741        DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00003FD4   090A0B0C 0D0E0F7F
00003FDC   01020304 05060750                     2742        DC     XL16'0102030405060750 090A0B780D0E0F7F'    v3
00003FE4   090A0B78 0D0E0F7F
00003FEC   00000000 00000001                     2743        DC     XL16'0000000000000001 0000000000000001'    v4
00003FF4   00000000 00000001
                                                 2744
                                                 2745        VRR_D  VMAH,3
00004000                                         2746+       DS     0FD
00004000               00004000                  2747+       USING  *,R5                base for test data and test routine
00004000   00004048                              2748+T64    DC     A(X64)              address of test routine
00004004   0040                                  2749+       DC     H'64'               test number
00004006   00                                    2750+       DC     X'00'
00004007   03                                    2751+       DC     HL1'3'              m5
00004008   E5D4C1C8 40404040                     2752+       DC     CL8'VMAH'           instruction name
00004010   0000408C                              2753+       DC     A(RE64+16)          address of v2 source
00004014   0000409C                              2754+       DC     A(RE64+32)          address of v3 source
00004018   000040AC                              2755+       DC     A(RE64+48)          address of v4 source
0000401C   00000010                              2756+       DC     A(16)               result length
00004020   0000407C                              2757+REA64  DC     A(RE64)             result address
00004028   00000000 00000000                     2758+       DS     FD                  gap
00004030   00000000 00000000                     2759+V1064  DS     XL16                V1 output
00004038   00000000 00000000
00004040   00000000 00000000                     2760+       DS     FD                  gap
                                                 2761+*
00004048                                         2762+X64    DS     0F
00004048   E310 5010 0014              00000010  2763+       LGF    R1,V2ADDR           load v2 source
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000404E	E761 0000 0806		00000000	2764+	VL	v22,0(R1)	use v22 to test decoder
00004054	E310 5014 0014		00000014	2765+	LGF	R1,V3ADDR	load v3 source
0000405A	E771 0000 0806		00000000	2766+	VL	v23,0(R1)	use v23 to test decoder
00004060	E310 5018 0014		00000018	2767+	LGF	R1,V4ADDR	load v4 source
00004066	E781 0000 0806		00000000	2768+	VL	v24,0(R1)	use v24 to test decoder
0000406C	E766 7300 8FAB			2769+	VMAH	V22,V22,V23,V24,3	test instruction (dest is a source)
00004072	E760 5030 080E		00004030	2770+	VST	V22,V1064	save v1 output
00004078	07FB			2771+	BR	R11	return
0000407C				2772+RE64	DC	0F	xl16 expected result
0000407C				2773+	DROP	R5	
0000407C	FFFFFF01 0309101C			2774	DC	XL16'FFFFFF010309101C 0024558DB838C862'	result
00004084	0024558D B838C862						
0000408C	FF020304 05060750			2775	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00004094	090A0B0C 0D0E0F7F						
0000409C	00010102 02030328			2776	DC	XL16'0001010202030328 0405053C0607073F'	v3
000040A4	0405053C 0607073F						
000040AC	20000000 00000000			2777	DC	XL16'2000000000000000 FFFFFFFFFFFFFFFF'	v4
000040B4	FFFFFFFF FFFFFFFF						
				2778			
				2779	VRR_D	VMAH,3	
000040C0				2780+	DS	0FD	
000040C0		000040C0		2781+	USING	*,R5	base for test data and test routine
000040C0	00004108			2782+T65	DC	A(X65)	address of test routine
000040C4	0041			2783+	DC	H'65'	test number
000040C6	00			2784+	DC	X'00'	
000040C7	03			2785+	DC	HL1'3'	m5
000040C8	E5D4C1C8 40404040			2786+	DC	CL8'VMAH'	instruction name
000040D0	0000414C			2787+	DC	A(RE65+16)	address of v2 source
000040D4	0000415C			2788+	DC	A(RE65+32)	address of v3 source
000040D8	0000416C			2789+	DC	A(RE65+48)	address of v4 source
000040DC	00000010			2790+	DC	A(16)	result length
000040E0	0000413C			2791+REA65	DC	A(RE65)	result address
000040E8	00000000 00000000			2792+	DS	FD	gap
000040F0	00000000 00000000			2793+V1065	DS	XL16	V1 output
000040F8	00000000 00000000						
00004100	00000000 00000000			2794+	DS	FD	gap
				2795+*			
00004108				2796+X65	DS	0F	
00004108	E310 5010 0014		00000010	2797+	LGF	R1,V2ADDR	load v2 source
0000410E	E761 0000 0806		00000000	2798+	VL	v22,0(R1)	use v22 to test decoder
00004114	E310 5014 0014		00000014	2799+	LGF	R1,V3ADDR	load v3 source
0000411A	E771 0000 0806		00000000	2800+	VL	v23,0(R1)	use v23 to test decoder
00004120	E310 5018 0014		00000018	2801+	LGF	R1,V4ADDR	load v4 source
00004126	E781 0000 0806		00000000	2802+	VL	v24,0(R1)	use v24 to test decoder
0000412C	E766 7300 8FAB			2803+	VMAH	V22,V22,V23,V24,3	test instruction (dest is a source)
00004132	E760 5030 080E		000040F0	2804+	VST	V22,V1065	save v1 output
00004138	07FB			2805+	BR	R11	return
0000413C				2806+RE65	DC	0F	xl16 expected result
0000413C				2807+	DROP	R5	
0000413C	FFFFFFFF FFFFFFFF			2808	DC	XL16'FFFFFFFFFFFFFFFF 0009131EA8C3DFFE'	result
00004144	0009131E A8C3DFFE						
0000414C	FF020304 05060750			2809	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00004154	090A0B0C 0D0E0F7F						
0000415C	00000000 0000000A			2810	DC	XL16'000000000000000A 0101010F0101010F'	v3
00004164	0101010F 0101010F						
0000416C	00001000 00000001			2811	DC	XL16'0000100000000001 1000000000000001'	v4

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004174	10000000 00000001						
				2812			
				2813	* Quadword		
				2814		VRR_D	VMAH, 4
00004180				2815+	DS	0FD	
00004180		00004180		2816+	USING	*,R5	base for test data and test routine
00004180	000041C8			2817+T66	DC	A(X66)	address of test routine
00004184	0042			2818+	DC	H'66'	test number
00004186	00			2819+	DC	X'00'	
00004187	04			2820+	DC	HL1'4'	m5
00004188	E5D4C1C8 40404040			2821+	DC	CL8'VMAH'	instruction name
00004190	0000420C			2822+	DC	A(RE66+16)	address of v2 source
00004194	0000421C			2823+	DC	A(RE66+32)	address of v3 source
00004198	0000422C			2824+	DC	A(RE66+48)	address of v4 source
0000419C	00000010			2825+	DC	A(16)	result length
000041A0	000041FC			2826+REA66	DC	A(RE66)	result address
000041A8	00000000 00000000			2827+	DS	FD	gap
000041B0	00000000 00000000			2828+V1066	DS	XL16	V1 output
000041B8	00000000 00000000						
000041C0	00000000 00000000			2829+	DS	FD	gap
				2830+*			
000041C8				2831+X66	DS	0F	
000041C8	E310 5010 0014		00000010	2832+	LGF	R1, V2ADDR	load v2 source
000041CE	E761 0000 0806		00000000	2833+	VL	v22, 0(R1)	use v22 to test decoder
000041D4	E310 5014 0014		00000014	2834+	LGF	R1, V3ADDR	load v3 source
000041DA	E771 0000 0806		00000000	2835+	VL	v23, 0(R1)	use v23 to test decoder
000041E0	E310 5018 0014		00000018	2836+	LGF	R1, V4ADDR	load v4 source
000041E6	E781 0000 0806		00000000	2837+	VL	v24, 0(R1)	use v24 to test decoder
000041EC	E766 7400 8FAB			2838+	VMAH	V22, V22, V23, V24, 4	test instruction (dest is a source)
000041F2	E760 5030 080E		000041B0	2839+	VST	V22, V1066	save v1 output
000041F8	07FB			2840+	BR	R11	return
000041FC				2841+RE66	DC	0F	xl16 expected result
000041FC				2842+	DROP	R5	
000041FC	00000000 00000001			2843	DC	XL16'0000000000000001 FFFCE00270FFFF8F'	result
00004204	FFFCE002 70FFFF8F						
0000420C	FFFFFFFF 00019000			2844	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00004214	00000038 EEEEEEFA						
0000421C	FFFFFFFF 00019000			2845	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00004224	00000038 0EEEEEFA						
0000422C	00000000 00000000			2846	DC	XL16'0000000000000000 0000000000000000'	v4
00004234	00000000 00000000						
				2847			
				2848		VRR_D	VMAH, 4
00004240				2849+	DS	0FD	
00004240		00004240		2850+	USING	*,R5	base for test data and test routine
00004240	00004288			2851+T67	DC	A(X67)	address of test routine
00004244	0043			2852+	DC	H'67'	test number
00004246	00			2853+	DC	X'00'	
00004247	04			2854+	DC	HL1'4'	m5
00004248	E5D4C1C8 40404040			2855+	DC	CL8'VMAH'	instruction name
00004250	000042CC			2856+	DC	A(RE67+16)	address of v2 source
00004254	000042DC			2857+	DC	A(RE67+32)	address of v3 source
00004258	000042EC			2858+	DC	A(RE67+48)	address of v4 source
0000425C	00000010			2859+	DC	A(16)	result length
00004260	000042BC			2860+REA67	DC	A(RE67)	result address
00004268	00000000 00000000			2861+	DS	FD	gap

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  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

00004270  00000000 00000000                       2862+V1067   DS    XL16              V1 output
00004278  00000000 00000000
00004280  00000000 00000000                       2863+        DS    FD                gap
                                                  2864+*
00004288                                          2865+X67     DS    OF
00004288  E310 5010 0014              00000010    2866+        LGF   R1,V2ADDR         load v2 source
0000428E  E761 0000 0806              00000000    2867+        VL    v22,0(R1)         use v22 to test decoder
00004294  E310 5014 0014              00000014    2868+        LGF   R1,V3ADDR         load v3 source
0000429A  E771 0000 0806              00000000    2869+        VL    v23,0(R1)         use v23 to test decoder
000042A0  E310 5018 0014              00000018    2870+        LGF   R1,V4ADDR         load v4 source
000042A6  E781 0000 0806              00000000    2871+        VL    v24,0(R1)         use v24 to test decoder
000042AC  E766 7400 8FAB                          2872+        VMAH  V22,V22,V23,V24,4   test instruction (dest is a source)
000042B2  E760 5030 080E              00004270    2873+        VST   V22,V1067          save v1 output
000042B8  07FB                                    2874+        BR    R11               return
000042BC                                          2875+RE67    DC    OF                xl16 expected result
000042BC                                          2876+        DROP  R5
000042BC  FFFF0004 0C192C45                        2877         DC    XL16'FFFF00040C192C45 69B57B4BBDEC6504'    result
000042C4  69B57B4B BDEC6504
000042CC  FF020304 05060750                        2878         DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
000042D4  090A0B0C 0D0E0F7F
000042DC  01020304 05060750                        2879         DC    XL16'0102030405060750 090A0B780D0E0F7F'    v3
000042E4  090A0B78 0D0E0F7F
000042EC  10000000 00000001                        2880         DC    XL16'1000000000000001 1000000000000001'    v4
000042F4  10000000 00000001
                                                   2881
                                                   2882                VRR_D VMAH,4
00004300                                           2883+        DS    OFD
00004300                        00004300           2884+        USING *,R5             base for test data and test routine
00004300  00004348                                 2885+T68     DC    A(X68)            address of test routine
00004304  0044                                     2886+        DC    H'68'             test number
00004306  00                                       2887+        DC    X'00'
00004307  04                                       2888+        DC    HL1'4'            m5
00004308  E5D4C1C8 40404040                         2889+        DC    CL8'VMAH'         instruction name
00004310  0000438C                                 2890+        DC    A(RE68+16)        address of v2 source
00004314  0000439C                                 2891+        DC    A(RE68+32)        address of v3 source
00004318  000043AC                                 2892+        DC    A(RE68+48)        address of v4 source
0000431C  00000010                                 2893+        DC    A(16)             result length
00004320  0000437C                                 2894+REA68   DC    A(RE68)           result address
00004328  00000000 00000000                         2895+        DS    FD                gap
00004330  00000000 00000000                         2896+V1068   DS    XL16              V1 output
00004338  00000000 00000000
00004340  00000000 00000000                         2897+        DS    FD                gap
                                                    2898+*
00004348                                           2899+X68     DS    OF
00004348  E310 5010 0014              00000010    2900+        LGF   R1,V2ADDR         load v2 source
0000434E  E761 0000 0806              00000000    2901+        VL    v22,0(R1)         use v22 to test decoder
00004354  E310 5014 0014              00000014    2902+        LGF   R1,V3ADDR         load v3 source
0000435A  E771 0000 0806              00000000    2903+        VL    v23,0(R1)         use v23 to test decoder
00004360  E310 5018 0014              00000018    2904+        LGF   R1,V4ADDR         load v4 source
00004366  E781 0000 0806              00000000    2905+        VL    v24,0(R1)         use v24 to test decoder
0000436C  E766 7400 8FAB                          2906+        VMAH  V22,V22,V23,V24,4   test instruction (dest is a source)
00004372  E760 5030 080E              00004330    2907+        VST   V22,V1068          save v1 output
00004378  07FB                                    2908+        BR    R11               return
0000437C                                          2909+RE68    DC    OF                xl16 expected result
0000437C                                          2910+        DROP  R5
0000437C  FFFFFF01 0309101B                         2911         DC    XL16'FFFFFF010309101B 06CF0A94A5DE7262'    result
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  LOC           OBJECT CODE       ADDR1     ADDR2     STMT

00004384  06CF0A94 A5DE7262
0000438C  FF020304 05060750                          2912          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'     v2
00004394  090A0B0C 0D0E0F7F
0000439C  00010102 02030328                          2913          DC    XL16'0001010202030328 0405053C0607073F'     v3
000043A4  0405053C 0607073F
000043AC  FFFFFFFF FFFFFFFF                           2914          DC    XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'     v4
000043B4  FFFFFFFF FFFFFFFF
                                                      2915
                                                      2916          VRR_D VMAH, 4
000043C0                                              2917+         DS    0FD
000043C0                          000043C0            2918+         USING *, R5                 base for test data and test routine
000043C0  00004408                                    2919+T69      DC    A(X69)                 address of test routine
000043C4  0045                                        2920+         DC    H'69'                  test number
000043C6  00                                          2921+         DC    X'00'
000043C7  04                                          2922+         DC    HL1'4'                 m5
000043C8  E5D4C1C8 40404040                           2923+         DC    CL8'VMAH'              instruction name
000043D0  0000444C                                    2924+         DC    A(RE69+16)             address of v2 source
000043D4  0000445C                                    2925+         DC    A(RE69+32)             address of v3 source
000043D8  0000446C                                    2926+         DC    A(RE69+48)             address of v4 source
000043DC  00000010                                    2927+         DC    A(16)                  result length
000043E0  0000443C                                    2928+REA69    DC    A(RE69)                result address
000043E8  00000000 00000000                           2929+         DS    FD                     gap
000043F0  00000000 00000000                           2930+V1069    DS    XL16                   V1 output
000043F8  00000000 00000000
00004400  00000000 00000000                           2931+         DS    FD                     gap
                                                      2932+*
00004408                                              2933+X69      DS    0F
00004408  E310 5010 0014                   00000010   2934+         LGF   R1, V2ADDR             load v2 source
0000440E  E761 0000 0806                   00000000   2935+         VL    v22, 0(R1)             use v22 to test decoder
00004414  E310 5014 0014                   00000014   2936+         LGF   R1, V3ADDR             load v3 source
0000441A  E771 0000 0806                   00000000   2937+         VL    v23, 0(R1)             use v23 to test decoder
00004420  E310 5018 0014                   00000018   2938+         LGF   R1, V4ADDR             load v4 source
00004426  E781 0000 0806                   00000000   2939+         VL    v24, 0(R1)             use v24 to test decoder
0000442C  E766 7400 8FAB                               2940+         VMAH  V22, V22, V23, V24, 4    test instruction (dest is a source)
00004432  E760 5030 080E                   000043F0   2941+         VST   V22, V1069             save v1 output
00004438  07FB                                         2942+         BR    R11                    return
0000443C                                              2943+RE69     DC    0F                     xl16 expected result
0000443C                                              2944+         DROP  R5
0000443C  FFFFFFFF FFFFFFFE                           2945          DC    XL16'FFFFFFFFFFFFFFFE F6131F2C2C658673'     result
00004444  F6131F2C 2C658673
0000444C  FF020304 05060750                           2946          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'     v2
00004454  090A0B0C 0D0E0F7F
0000445C  00000000 0000000A                           2947          DC    XL16'000000000000000A 0101010F0101010F'     v3
00004464  0101010F 0101010F
0000446C  7FFFFFFF FFFFFFFF                           2948          DC    XL16'7FFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'     v4
00004474  FFFFFFFF FFFFFFFF
                                                      2949
                                                      2950 *-------------------------------------------------------------------
                                                      2951 *   VMALE  - Vector Multiply and Add Logical Even
                                                      2952 *-------------------------------------------------------------------
                                                      2953 * Byte
                                                      2954          VRR_D VMALE, 0
00004480                                              2955+         DS    0FD
00004480                          00004480            2956+         USING *, R5                 base for test data and test routine
00004480  000044C8                                    2957+T70      DC    A(X70)                 address of test routine
00004484  0046                                        2958+         DC    H'70'                  test number
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  LOC          OBJECT CODE      ADDR1      ADDR2      STMT

00004486  00                                          2959+          DC      X'00'
00004487  00                                          2960+          DC      HL1'0'                  m5
00004488  E5D4C1D3 C5404040                           2961+          DC      CL8'VMALE'              instruction name
00004490  0000450C                                    2962+          DC      A(RE70+16)              address of v2 source
00004494  0000451C                                    2963+          DC      A(RE70+32)              address of v3 source
00004498  0000452C                                    2964+          DC      A(RE70+48)              address of v4 source
0000449C  00000010                                    2965+          DC      A(16)                   result length
000044A0  000044FC                                    2966+REA70     DC      A(RE70)                 result address
000044A8  00000000 00000000                           2967+          DS      FD                      gap
000044B0  00000000 00000000                           2968+V1070     DS      XL16                    V1 output
000044B8  00000000 00000000
000044C0  00000000 00000000                           2969+          DS      FD                      gap
                                                      2970+*
000044C8                                              2971+X70       DS      0F
000044C8  E310 5010 0014                   00000010   2972+          LGF     R1,V2ADDR               load v2 source
000044CE  E761 0000 0806                   00000000   2973+          VL      v22,0(R1)               use v22 to test decoder
000044D4  E310 5014 0014                   00000014   2974+          LGF     R1,V3ADDR               load v3 source
000044DA  E771 0000 0806                   00000000   2975+          VL      v23,0(R1)               use v23 to test decoder
000044E0  E310 5018 0014                   00000018   2976+          LGF     R1,V4ADDR               load v4 source
000044E6  E781 0000 0806                   00000000   2977+          VL      v24,0(R1)               use v24 to test decoder
000044EC  E766 7000 8FAC                              2978+          VMALE   V22,V22,V23,V24,0    test instruction (dest is a source)
000044F2  E760 5030 080E                   000044B0   2979+          VST     V22,V1070            save v1 output
000044F8  07FB                                        2980+          BR      R11                     return
000044FC                                              2981+RE70      DC      0F                      xl16 expected result
000044FC                                              2982+          DROP    R5
000044FC  FE010000 00000000                           2983           DC      XL16'FE01000000000000 0000000000000000'   result
00004504  00000000 00000000
0000450C  FF000000 00000019                           2984           DC      XL16'FF00000000000019 00000038000000FA'   v2
00004514  00000038 000000FA
0000451C  FF000000 00000019                           2985           DC      XL16'FF00000000000019 00000038000000FA'   v3
00004524  00000038 000000FA
0000452C  00000000 00000000                           2986           DC      XL16'0000000000000000 0000000000000000'   v4
00004534  00000000 00000000
                                                      2987
                                                      2988           VRR_D   VMALE,0
00004540                                              2989+          DS      0FD
00004540                        00004540              2990+          USING   *,R5                    base for test data and test routine
00004540  00004588                                    2991+T71       DC      A(X71)                  address of test routine
00004544  0047                                        2992+          DC      H'71'                   test number
00004546  00                                          2993+          DC      X'00'
00004547  00                                          2994+          DC      HL1'0'                  m5
00004548  E5D4C1D3 C5404040                           2995+          DC      CL8'VMALE'              instruction name
00004550  000045CC                                    2996+          DC      A(RE71+16)              address of v2 source
00004554  000045DC                                    2997+          DC      A(RE71+32)              address of v3 source
00004558  000045EC                                    2998+          DC      A(RE71+48)              address of v4 source
0000455C  00000010                                    2999+          DC      A(16)                   result length
00004560  000045BC                                    3000+REA71     DC      A(RE71)                 result address
00004568  00000000 00000000                           3001+          DS      FD                      gap
00004570  00000000 00000000                           3002+V1071     DS      XL16                    V1 output
00004578  00000000 00000000
00004580  00000000 00000000                           3003+          DS      FD                      gap
                                                      3004+*
00004588                                              3005+X71       DS      0F
00004588  E310 5010 0014                   00000010   3006+          LGF     R1,V2ADDR               load v2 source
0000458E  E761 0000 0806                   00000000   3007+          VL      v22,0(R1)               use v22 to test decoder
00004594  E310 5014 0014                   00000014   3008+          LGF     R1,V3ADDR               load v3 source
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
0000459A	E771 0000 0806		00000000	3009+	VL	v23,0(R1)	use v23 to test decoder	
000045A0	E310 5018 0014		00000018	3010+	LGF	R1,V4ADDR	load v4 source	
000045A6	E781 0000 0806		00000000	3011+	VL	v24,0(R1)	use v24 to test decoder	
000045AC	E766 7000 8FAC			3012+	VMALE	V22,V22,V23,V24,0	test instruction (dest is a source)	
000045B2	E760 5030 080E		00004570	3013+	VST	V22,V1071	save v1 output	
000045B8	07FB			3014+	BR	R11	return	
000045BC				3015+RE71	DC	0F	xl16 expected result	
000045BC				3016+	DROP	R5		
000045BC	FE030001 0000002F			3017	DC	XL16'FE0300010000002F 0000000300000002'	result	
000045C4	00000003 00000002							
000045CC	FF0000FF 00000029			3018	DC	XL16'FF0000FF00000029 00000038000000FA'	v2	
000045D4	00000038 000000FA							
000045DC	FF000001 00000029			3019	DC	XL16'FF00000100000029 00000038000000FA'	v3	
000045E4	00000038 000000FA							
000045EC	00020001 0000002F			3020	DC	XL16'000200010000002F 0000000300000002'	v4	
000045F4	00000003 00000002							
				3021				
				3022	VRR_D	VMALE,0		
00004600				3023+	DS	0FD		
00004600		00004600		3024+	USING	*,R5	base for test data and test routine	
00004600	00004648			3025+T72	DC	A(X72)	address of test routine	
00004604	0048			3026+	DC	H'72'	test number	
00004606	00			3027+	DC	X'00'		
00004607	00			3028+	DC	HL1'0'	m5	
00004608	E5D4C1D3 C5404040			3029+	DC	CL8'VMALE'	instruction name	
00004610	0000468C			3030+	DC	A(RE72+16)	address of v2 source	
00004614	0000469C			3031+	DC	A(RE72+32)	address of v3 source	
00004618	000046AC			3032+	DC	A(RE72+48)	address of v4 source	
0000461C	00000010			3033+	DC	A(16)	result length	
00004620	0000467C			3034+REA72	DC	A(RE72)	result address	
00004628	00000000 00000000			3035+	DS	FD	gap	
00004630	00000000 00000000			3036+V1072	DS	XL16	V1 output	
00004638	00000000 00000000							
00004640	00000000 00000000			3037+	DS	FD	gap	
				3038+*				
00004648				3039+X72	DS	0F		
00004648	E310 5010 0014		00000010	3040+	LGF	R1,V2ADDR	load v2 source	
0000464E	E761 0000 0806		00000000	3041+	VL	v22,0(R1)	use v22 to test decoder	
00004654	E310 5014 0014		00000014	3042+	LGF	R1,V3ADDR	load v3 source	
0000465A	E771 0000 0806		00000000	3043+	VL	v23,0(R1)	use v23 to test decoder	
00004660	E310 5018 0014		00000018	3044+	LGF	R1,V4ADDR	load v4 source	
00004666	E781 0000 0806		00000000	3045+	VL	v24,0(R1)	use v24 to test decoder	
0000466C	E766 7000 8FAC			3046+	VMALE	V22,V22,V23,V24,0	test instruction (dest is a source)	
00004672	E760 5030 080E		00004630	3047+	VST	V22,V1072	save v1 output	
00004678	07FB			3048+	BR	R11	return	
0000467C				3049+RE72	DC	0F	xl16 expected result	
0000467C				3050+	DROP	R5		
0000467C	FD03030D 051F0739			3051	DC	XL16'FD03030D051F0739 095B0B850DB70FF1'	result	
00004684	095B0B85 0DB70FF1							
0000468C	FF020304 05060708			3052	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2	
00004694	090A0B0C 0D0E0F10							
0000469C	FF020304 05060708			3053	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3	
000046A4	090A0B0C 0D0E0F10							
000046AC	FF020304 05060708			3054	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4	
000046B4	090A0B0C 0D0E0F10							
				3055				

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT


                                                  3056              VRR_D VMALE,0
000046C0                                          3057+             DS    0FD
000046C0                       000046C0           3058+             USING *,R5                   base for test data and test routine
000046C0   00004708                               3059+T73          DC    A(X73)                 address of test routine
000046C4   0049                                   3060+             DC    H'73'                  test number
000046C6   00                                     3061+             DC    X'00'
000046C7   00                                     3062+             DC    HL1'0'                 m5
000046C8   E5D4C1D3 C5404040                       3063+            DC    CL8'VMALE'             instruction name
000046D0   0000474C                               3064+             DC    A(RE73+16)             address of v2 source
000046D4   0000475C                               3065+             DC    A(RE73+32)             address of v3 source
000046D8   0000476C                               3066+             DC    A(RE73+48)             address of v4 source
000046DC   00000010                               3067+             DC    A(16)                  result length
000046E0   0000473C                               3068+REA73        DC    A(RE73)                result address
000046E8   00000000 00000000                       3069+            DS    FD                     gap
000046F0   00000000 00000000                       3070+V1073       DS    XL16                   V1 output
000046F8   00000000 00000000
00004700   00000000 00000000                       3071+            DS    FD                     gap
                                                  3072+*
00004708                                          3073+X73          DS    0F
00004708   E310 5010 0014            00000010     3074+             LGF   R1,V2ADDR              load v2 source
0000470E   E761 0000 0806            00000000     3075+             VL    v22,0(R1)              use v22 to test decoder
00004714   E310 5014 0014            00000014     3076+             LGF   R1,V3ADDR              load v3 source
0000471A   E771 0000 0806            00000000     3077+             VL    v23,0(R1)              use v23 to test decoder
00004720   E310 5018 0014            00000018     3078+             LGF   R1,V4ADDR              load v4 source
00004726   E781 0000 0806            00000000     3079+             VL    v24,0(R1)              use v24 to test decoder
0000472C   E766 7000 8FAC                          3080+            VMALE V22,V22,V23,V24,0   test instruction (dest is a source)
00004732   E760 5030 080E            000046F0     3081+             VST   V22,V1073               save v1 output
00004738   07FB                                   3082+             BR    R11                    return
0000473C                                          3083+RE73         DC    0F                     xl16 expected result
0000473C                                          3084+             DROP  R5
0000473C   FD030307 0510071D                       3085             DC    XL16'FD0303070510071D 092E0B430D5C0F79'    result
00004744   092E0B43 0D5C0F79
0000474C   FF020304 05060708                       3086             DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00004754   090A0B0C 0D0E0F10
0000475C   FF010102 02030304                       3087             DC    XL16'FF01010202030304 0405050606070708'    v3
00004764   04050506 06070708
0000476C   FF020304 05060708                       3088             DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00004774   090A0B0C 0D0E0F10
                                                  3089
                                                  3090              VRR_D VMALE,0
00004780                                          3091+             DS    0FD
00004780                       00004780           3092+             USING *,R5                   base for test data and test routine
00004780   000047C8                               3093+T74          DC    A(X74)                 address of test routine
00004784   004A                                   3094+             DC    H'74'                  test number
00004786   00                                     3095+             DC    X'00'
00004787   00                                     3096+             DC    HL1'0'                 m5
00004788   E5D4C1D3 C5404040                       3097+            DC    CL8'VMALE'             instruction name
00004790   0000480C                               3098+             DC    A(RE74+16)             address of v2 source
00004794   0000481C                               3099+             DC    A(RE74+32)             address of v3 source
00004798   0000482C                               3100+             DC    A(RE74+48)             address of v4 source
0000479C   00000010                               3101+             DC    A(16)                  result length
000047A0   000047FC                               3102+REA74        DC    A(RE74)                result address
000047A8   00000000 00000000                       3103+            DS    FD                     gap
000047B0   00000000 00000000                       3104+V1074       DS    XL16                   V1 output
000047B8   00000000 00000000
000047C0   00000000 00000000                       3105+            DS    FD                     gap
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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT


                                                  3106+*
000047C8                                          3107+X74      DS    0F
000047C8   E310 5010 0014              00000010   3108+         LGF   R1,V2ADDR      load v2 source
000047CE   E761 0000 0806              00000000   3109+         VL    v22,0(R1)      use v22 to test decoder
000047D4   E310 5014 0014              00000014   3110+         LGF   R1,V3ADDR      load v3 source
000047DA   E771 0000 0806              00000000   3111+         VL    v23,0(R1)      use v23 to test decoder
000047E0   E310 5018 0014              00000018   3112+         LGF   R1,V4ADDR      load v4 source
000047E6   E781 0000 0806              00000000   3113+         VL    v24,0(R1)      use v24 to test decoder
000047EC   E766 7000 8FAC                         3114+         VMALE V22,V22,V23,V24,0    test instruction (dest is a source)
000047F2   E760 5030 080E              000047B0   3115+         VST   V22,V1074       save v1 output
000047F8   07FB                                   3116+         BR    R11            return
000047FC                                          3117+RE74     DC    0F             xl16 expected result
000047FC                                          3118+         DROP  R5
000047FC   FD030304 05060708                      3119          DC    XL16'FD03030405060708 09130B170D1B0F1F'    result
00004804   09130B17 0D1B0F1F
0000480C   FF020304 05060708                      3120          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00004814   090A0B0C 0D0E0F10
0000481C   FF000000 00000001                      3121          DC    XL16'FF00000000000001 0101010101010102'    v3
00004824   01010101 01010102
0000482C   FF020304 05060708                      3122          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00004834   090A0B0C 0D0E0F10
                                                  3123
                                                  3124  * Halfword
                                                  3125          VRR_D VMALE,1
00004840                                          3126+         DS    0FD
00004840                         00004840         3127+         USING *,R5            base for test data and test routine
00004840   00004888                               3128+T75      DC    A(X75)           address of test routine
00004844   004B                                   3129+         DC    H'75'            test number
00004846   00                                     3130+         DC    X'00'
00004847   01                                     3131+         DC    HL1'1'           m5
00004848   E5D4C1D3 C5404040                      3132+         DC    CL8'VMALE'       instruction name
00004850   000048CC                               3133+         DC    A(RE75+16)       address of v2 source
00004854   000048DC                               3134+         DC    A(RE75+32)       address of v3 source
00004858   000048EC                               3135+         DC    A(RE75+48)       address of v4 source
0000485C   00000010                               3136+         DC    A(16)            result length
00004860   000048BC                               3137+REA75    DC    A(RE75)          result address
00004868   00000000 00000000                      3138+         DS    FD               gap
00004870   00000000 00000000                      3139+V1075    DS    XL16             V1 output
00004878   00000000 00000000
00004880   00000000 00000000                      3140+         DS    FD               gap
                                                  3141+*
00004888                                          3142+X75      DS    0F
00004888   E310 5010 0014              00000010   3143+         LGF   R1,V2ADDR      load v2 source
0000488E   E761 0000 0806              00000000   3144+         VL    v22,0(R1)      use v22 to test decoder
00004894   E310 5014 0014              00000014   3145+         LGF   R1,V3ADDR      load v3 source
0000489A   E771 0000 0806              00000000   3146+         VL    v23,0(R1)      use v23 to test decoder
000048A0   E310 5018 0014              00000018   3147+         LGF   R1,V4ADDR      load v4 source
000048A6   E781 0000 0806              00000000   3148+         VL    v24,0(R1)      use v24 to test decoder
000048AC   E766 7100 8FAC                         3149+         VMALE V22,V22,V23,V24,1    test instruction (dest is a source)
000048B2   E760 5030 080E              00004870   3150+         VST   V22,V1075       save v1 output
000048B8   07FB                                   3151+         BR    R11            return
000048BC                                          3152+RE75     DC    0F             xl16 expected result
000048BC                                          3153+         DROP  R5
000048BC   FE010000 00000000                      3154          DC    XL16'FE01000000000000 0000000000000000'    result
000048C4   00000000 00000000
000048CC   FF000000 00000019                      3155          DC    XL16'FF00000000000019 00000038000000FA'    v2
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000048D4	00000038 000000FA							
000048DC	FF000000 00000019			3156		DC	XL16'FF00000000000019 00000038000000FA'	v3
000048E4	00000038 000000FA							
000048EC	00000000 00000000			3157		DC	XL16'0000000000000000 0000000000000000'	v4
000048F4	00000000 00000000							
				3158				
				3159		VRR_D	VMALE,1	
00004900				3160+		DS	0FD	
00004900		00004900		3161+		USING	*,R5	base for test data and test routine
00004900	00004948			3162+T76		DC	A(X76)	address of test routine
00004904	004C			3163+		DC	H'76'	test number
00004906	00			3164+		DC	X'00'	
00004907	01			3165+		DC	HL1'1'	m5
00004908	E5D4C1D3 C5404040			3166+		DC	CL8'VMALE'	instruction name
00004910	0000498C			3167+		DC	A(RE76+16)	address of v2 source
00004914	0000499C			3168+		DC	A(RE76+32)	address of v3 source
00004918	000049AC			3169+		DC	A(RE76+48)	address of v4 source
0000491C	00000010			3170+		DC	A(16)	result length
00004920	0000497C			3171+REA76		DC	A(RE76)	result address
00004928	00000000 00000000			3172+		DS	FD	gap
00004930	00000000 00000000			3173+V1076		DS	XL16	V1 output
00004938	00000000 00000000							
00004940	00000000 00000000			3174+		DS	FD	gap
				3175+*				
00004948				3176+X76		DS	0F	
00004948	E310 5010 0014		00000010	3177+		LGF	R1,V2ADDR	load v2 source
0000494E	E761 0000 0806		00000000	3178+		VL	v22,0(R1)	use v22 to test decoder
00004954	E310 5014 0014		00000014	3179+		LGF	R1,V3ADDR	load v3 source
0000495A	E771 0000 0806		00000000	3180+		VL	v23,0(R1)	use v23 to test decoder
00004960	E310 5018 0014		00000018	3181+		LGF	R1,V4ADDR	load v4 source
00004966	E781 0000 0806		00000000	3182+		VL	v24,0(R1)	use v24 to test decoder
0000496C	E766 7100 8FAC			3183+		VMALE	V22,V22,V23,V24,1	test instruction (dest is a source)
00004972	E760 5030 080E		00004930	3184+		VST	V22,V1076	save v1 output
00004978	07FB			3185+		BR	R11	return
0000497C				3186+RE76		DC	0F	xl16 expected result
0000497C				3187+		DROP	R5	
0000497C	FE030001 0000002F			3188		DC	XL16'FE0300010000002F 0000000300000002'	result
00004984	00000003 00000002							
0000498C	FF0000FF 00000029			3189		DC	XL16'FF0000FF00000029 00000038000000FA'	v2
00004994	00000038 000000FA							
0000499C	FF000001 00000029			3190		DC	XL16'FF00000100000029 00000038000000FA'	v3
000049A4	00000038 000000FA							
000049AC	00020001 0000002F			3191		DC	XL16'000200010000002F 0000000300000002'	v4
000049B4	00000003 00000002							
				3192				
				3193		VRR_D	VMALE,1	
000049C0				3194+		DS	0FD	
000049C0		000049C0		3195+		USING	*,R5	base for test data and test routine
000049C0	00004A08			3196+T77		DC	A(X77)	address of test routine
000049C4	004D			3197+		DC	H'77'	test number
000049C6	00			3198+		DC	X'00'	
000049C7	01			3199+		DC	HL1'1'	m5
000049C8	E5D4C1D3 C5404040			3200+		DC	CL8'VMALE'	instruction name
000049D0	00004A4C			3201+		DC	A(RE77+16)	address of v2 source
000049D4	00004A5C			3202+		DC	A(RE77+32)	address of v3 source
000049D8	00004A6C			3203+		DC	A(RE77+48)	address of v4 source

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  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

 000049DC  00000010                                3204+          DC      A(16)              result length
 000049E0  00004A3C                                3205+REA77     DC      A(RE77)            result address
 000049E8  00000000 00000000                       3206+          DS      FD                 gap
 000049F0  00000000 00000000                       3207+V1077     DS      XL16               V1 output
 000049F8  00000000 00000000
 00004A00  00000000 00000000                       3208+          DS      FD                 gap
                                                   3209+*
 00004A08                                          3210+X77       DS      0F
 00004A08  E310 5010 0014              00000010     3211+          LGF     R1,V2ADDR          load v2 source
 00004A0E  E761 0000 0806              00000000     3212+          VL      v22,0(R1)          use v22 to test decoder
 00004A14  E310 5014 0014              00000014     3213+          LGF     R1,V3ADDR          load v3 source
 00004A1A  E771 0000 0806              00000000     3214+          VL      v23,0(R1)          use v23 to test decoder
 00004A20  E310 5018 0014              00000018     3215+          LGF     R1,V4ADDR          load v4 source
 00004A26  E781 0000 0806              00000000     3216+          VL      v24,0(R1)          use v24 to test decoder
 00004A2C  E766 7100 8FAC                           3217+          VMALE   V22,V22,V23,V24,1    test instruction (dest is a source)
 00004A32  E760 5030 080E              000049F0     3218+          VST     V22,V1077           save v1 output
 00004A38  07FB                                     3219+          BR      R11                return
 00004A3C                                           3220+RE77      DC      0F                 xl16 expected result
 00004A3C                                           3221+          DROP    R5
 00004A3C  FD06FF08 051F432C                        3222           DC      XL16'FD06FF08051F432C 095BBF700DB87BD4'    result
 00004A44  095BBF70 0DB87BD4
 00004A4C  FF020304 05060708                        3223           DC      XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
 00004A54  090A0B0C 0D0E0F10
 00004A5C  FF020304 05060708                        3224           DC      XL16'FF02030405060708 090A0B0C0D0E0F10'    v3
 00004A64  090A0B0C 0D0E0F10
 00004A6C  FF020304 05060708                        3225           DC      XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
 00004A74  090A0B0C 0D0E0F10
                                                   3226
                                                   3227           VRR_D   VMALE,1
 00004A80                                           3228+          DS      0FD
 00004A80              00004A80                     3229+          USING   *,R5               base for test data and test routine
 00004A80  00004AC8                                 3230+T78       DC      A(X78)             address of test routine
 00004A84  004E                                     3231+          DC      H'78'              test number
 00004A86  00                                       3232+          DC      X'00'
 00004A87  01                                       3233+          DC      HL1'1'             m5
 00004A88  E5D4C1D3 C5404040                        3234+          DC      CL8'VMALE'         instruction name
 00004A90  00004B0C                                 3235+          DC      A(RE78+16)         address of v2 source
 00004A94  00004B1C                                 3236+          DC      A(RE78+32)         address of v3 source
 00004A98  00004B2C                                 3237+          DC      A(RE78+48)         address of v4 source
 00004A9C  00000010                                 3238+          DC      A(16)              result length
 00004AA0  00004AFC                                 3239+REA78     DC      A(RE78)            result address
 00004AA8  00000000 00000000                       3240+          DS      FD                 gap
 00004AB0  00000000 00000000                       3241+V1078     DS      XL16               V1 output
 00004AB8  00000000 00000000
 00004AC0  00000000 00000000                       3242+          DS      FD                 gap
                                                   3243+*
 00004AC8                                          3244+X78        DS      0F
 00004AC8  E310 5010 0014              00000010     3245+          LGF     R1,V2ADDR          load v2 source
 00004ACE  E761 0000 0806              00000000     3246+          VL      v22,0(R1)          use v22 to test decoder
 00004AD4  E310 5014 0014              00000014     3247+          LGF     R1,V3ADDR          load v3 source
 00004ADA  E771 0000 0806              00000000     3248+          VL      v23,0(R1)          use v23 to test decoder
 00004AE0  E310 5018 0014              00000018     3249+          LGF     R1,V4ADDR          load v4 source
 00004AE6  E781 0000 0806              00000000     3250+          VL      v24,0(R1)          use v24 to test decoder
 00004AEC  E766 7100 8FAC                           3251+          VMALE   V22,V22,V23,V24,1    test instruction (dest is a source)
 00004AF2  E760 5030 080E              00004AB0     3252+          VST     V22,V1078           save v1 output
 00004AF8  07FB                                     3253+          BR      R11                return
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00004AFC                                          3254+RE78    DC    0F                  xl16 expected result
00004AFC                                          3255+        DROP  R5
00004AFC   FD060006 0510221A                      3256         DC    XL16'FD0600060510221A 092E603E0D5CBE72'    result
00004B04   092E603E 0D5CBE72
00004B0C   FF020304 05060708                      3257         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00004B14   090A0B0C 0D0E0F10
00004B1C   FF010102 02030304                      3258         DC    XL16'FF01010202030304 0405050606070708'    v3
00004B24   04050506 06070708
00004B2C   FF020304 05060708                      3259         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00004B34   090A0B0C 0D0E0F10

                                                  3260
                                                  3261         VRR_D VMALE,1
00004B40                                          3262+        DS    0FD
00004B40                                00004B40  3263+        USING *,R5               base for test data and test routine
00004B40   00004B88                               3264+T79     DC    A(X79)             address of test routine
00004B44   004F                                   3265+        DC    H'79'              test number
00004B46   00                                     3266+        DC    X'00'
00004B47   01                                     3267+        DC    HL1'1'             m5
00004B48   E5D4C1D3 C5404040                       3268+        DC    CL8'VMALE'         instruction name
00004B50   00004BCC                               3269+        DC    A(RE79+16)         address of v2 source
00004B54   00004BDC                               3270+        DC    A(RE79+32)         address of v3 source
00004B58   00004BEC                               3271+        DC    A(RE79+48)         address of v4 source
00004B5C   00000010                               3272+        DC    A(16)              result length
00004B60   00004BBC                               3273+REA79   DC    A(RE79)            result address
00004B68   00000000 00000000                      3274+        DS    FD                 gap
00004B70   00000000 00000000                      3275+V1079   DS    XL16               V1 output
00004B78   00000000 00000000
00004B80   00000000 00000000                      3276+        DS    FD                 gap
                                                  3277+*
00004B88                                          3278+X79     DS    0F
00004B88   E310 5010 0014          00000010       3279+        LGF   R1,V2ADDR          load v2 source
00004B8E   E761 0000 0806          00000000       3280+        VL    v22,0(R1)          use v22 to test decoder
00004B94   E310 5014 0014          00000014       3281+        LGF   R1,V3ADDR          load v3 source
00004B9A   E771 0000 0806          00000000       3282+        VL    v23,0(R1)          use v23 to test decoder
00004BA0   E310 5018 0014          00000018       3283+        LGF   R1,V4ADDR          load v4 source
00004BA6   E781 0000 0806          00000000       3284+        VL    v24,0(R1)          use v24 to test decoder
00004BAC   E766 7100 8FAC                          3285+        VMALE V22,V22,V23,V24,1    test instruction (dest is a source)
00004BB2   E760 5030 080E          00004B70       3286+        VST   V22,V1079           save v1 output
00004BB8   07FB                                   3287+        BR    R11                return
00004BBC                                          3288+RE79    DC    0F                 xl16 expected result
00004BBC                                          3289+        DROP  R5
00004BBC   FD050104 05060708                      3290         DC    XL16'FD05010405060708 09131E160D1B2A1E'    result
00004BC4   09131E16 0D1B2A1E
00004BCC   FF020304 05060708                      3291         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00004BD4   090A0B0C 0D0E0F10
00004BDC   FF000000 00000001                      3292         DC    XL16'FF00000000000001 0101010101010102'    v3
00004BE4   01010101 01010102
00004BEC   FF020304 05060708                      3293         DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00004BF4   090A0B0C 0D0E0F10

                                                  3294
                                                  3295 * Word
                                                  3296         VRR_D VMALE,2
00004C00                                          3297+        DS    0FD
00004C00                                00004C00  3298+        USING *,R5               base for test data and test routine
00004C00   00004C48                               3299+T80     DC    A(X80)             address of test routine
00004C04   0050                                   3300+        DC    H'80'              test number
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004C06	00			3301+	DC	X'00'	
00004C07	02			3302+	DC	HL1'2'	m5
00004C08	E5D4C1D3 C5404040			3303+	DC	CL8'VMALE'	instruction name
00004C10	00004C8C			3304+	DC	A(RE80+16)	address of v2 source
00004C14	00004C9C			3305+	DC	A(RE80+32)	address of v3 source
00004C18	00004CAC			3306+	DC	A(RE80+48)	address of v4 source
00004C1C	00000010			3307+	DC	A(16)	result length
00004C20	00004C7C			3308+REA80	DC	A(RE80)	result address
00004C28	00000000 00000000			3309+	DS	FD	gap
00004C30	00000000 00000000			3310+V1080	DS	XL16	V1 output
00004C38	00000000 00000000						
00004C40	00000000 00000000			3311+	DS	FD	gap
				3312+*			
00004C48				3313+X80	DS	0F	
00004C48	E310 5010 0014		00000010	3314+	LGF	R1,V2ADDR	load v2 source
00004C4E	E761 0000 0806		00000000	3315+	VL	v22,0(R1)	use v22 to test decoder
00004C54	E310 5014 0014		00000014	3316+	LGF	R1,V3ADDR	load v3 source
00004C5A	E771 0000 0806		00000000	3317+	VL	v23,0(R1)	use v23 to test decoder
00004C60	E310 5018 0014		00000018	3318+	LGF	R1,V4ADDR	load v4 source
00004C66	E781 0000 0806		00000000	3319+	VL	v24,0(R1)	use v24 to test decoder
00004C6C	E766 7200 8FAC			3320+	VMALE	V22,V22,V23,V24,2	test instruction (dest is a source)
00004C72	E760 5030 080E		00004C30	3321+	VST	V22,V1080	save v1 output
00004C78	07FB			3322+	BR	R11	return
00004C7C				3323+RE80	DC	0F	xl16 expected result
00004C7C				3324+	DROP	R5	
00004C7C	FE010000 00000000			3325	DC	XL16'FE0100000000000 0000000000000C40'	result
00004C84	00000000 00000C40						
00004C8C	FF000000 00000019			3326	DC	XL16'FF00000000000019 00000038000000FA'	v2
00004C94	00000038 000000FA						
00004C9C	FF000000 00000019			3327	DC	XL16'FF00000000000019 00000038000000FA'	v3
00004CA4	00000038 000000FA						
00004CAC	00000000 00000000			3328	DC	XL16'0000000000000000 0000000000000000'	v4
00004CB4	00000000 00000000						
				3329			
				3330	VRR_D	VMALE,2	
00004CC0				3331+	DS	0FD	
00004CC0		00004CC0		3332+	USING	*,R5	base for test data and test routine
00004CC0	00004D08			3333+T81	DC	A(X81)	address of test routine
00004CC4	0051			3334+	DC	H'81'	test number
00004CC6	00			3335+	DC	X'00'	
00004CC7	02			3336+	DC	HL1'2'	m5
00004CC8	E5D4C1D3 C5404040			3337+	DC	CL8'VMALE'	instruction name
00004CD0	00004D4C			3338+	DC	A(RE81+16)	address of v2 source
00004CD4	00004D5C			3339+	DC	A(RE81+32)	address of v3 source
00004CD8	00004D6C			3340+	DC	A(RE81+48)	address of v4 source
00004CDC	00000010			3341+	DC	A(16)	result length
00004CE0	00004D3C			3342+REA81	DC	A(RE81)	result address
00004CE8	00000000 00000000			3343+	DS	FD	gap
00004CF0	00000000 00000000			3344+V1081	DS	XL16	V1 output
00004CF8	00000000 00000000						
00004D00	00000000 00000000			3345+	DS	FD	gap
				3346+*			
00004D08				3347+X81	DS	0F	
00004D08	E310 5010 0014		00000010	3348+	LGF	R1,V2ADDR	load v2 source
00004D0E	E761 0000 0806		00000000	3349+	VL	v22,0(R1)	use v22 to test decoder
00004D14	E310 5014 0014		00000014	3350+	LGF	R1,V3ADDR	load v3 source

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  LOC        OBJECT CODE      ADDR1      ADDR2    STMT

00004D1A  E771 0000 0806             00000000   3351+        VL      v23,0(R1)             use v23 to test decoder
00004D20  E310 5018 0014             00000018   3352+        LGF     R1,V4ADDR             load v4 source
00004D26  E781 0000 0806             00000000   3353+        VL      v24,0(R1)             use v24 to test decoder
00004D2C  E766 7200 8FAC                        3354+        VMALE   V22,V22,V23,V24,2       test instruction (dest is a source)
00004D32  E760 5030 080E             00004CF0   3355+        VST     V22,V1081             save v1 output
00004D38  07FB                                  3356+        BR      R11                   return
00004D3C                                        3357+RE81    DC      0F                    xl16 expected result
00004D3C                                        3358+        DROP    R5
00004D3C  FE030100 0000012E                     3359         DC      XL16'FE0301000000012E 0000000300000C42'    result
00004D44  00000003 00000C42
00004D4C  FF0000FF 00000029                     3360         DC      XL16'FF0000FF00000029 00000038000000FA'    v2
00004D54  00000038 000000FA
00004D5C  FF000001 00000029                     3361         DC      XL16'FF00000100000029 00000038000000FA'    v3
00004D64  00000038 000000FA
00004D6C  00020001 0000002F                     3362         DC      XL16'000200010000002F 0000000300000002'    v4
00004D74  00000003 00000002
                                                3363
                                                3364         VRR_D   VMALE,2
00004D80                                        3365+        DS      0FD
00004D80                         00004D80       3366+        USING   *,R5                  base for test data and test routine
00004D80  00004DC8                              3367+T82     DC      A(X82)                address of test routine
00004D84  0052                                  3368+        DC      H'82'                 test number
00004D86  00                                    3369+        DC      X'00'
00004D87  02                                    3370+        DC      HL1'2'                m5
00004D88  E5D4C1D3 C5404040                     3371+        DC      CL8'VMALE'            instruction name
00004D90  00004E0C                              3372+        DC      A(RE82+16)            address of v2 source
00004D94  00004E1C                              3373+        DC      A(RE82+32)            address of v3 source
00004D98  00004E2C                              3374+        DC      A(RE82+48)            address of v4 source
00004D9C  00000010                              3375+        DC      A(16)                 result length
00004DA0  00004DFC                              3376+REA82   DC      A(RE82)               result address
00004DA8  00000000 00000000                     3377+        DS      FD                    gap
00004DB0  00000000 00000000                     3378+V1082   DS      XL16                  V1 output
00004DB8  00000000 00000000
00004DC0  00000000 00000000                     3379+        DS      FD                    gap
                                                3380+*
00004DC8                                        3381+X82     DS      0F
00004DC8  E310 5010 0014             00000010   3382+        LGF     R1,V2ADDR             load v2 source
00004DCE  E761 0000 0806             00000000   3383+        VL      v22,0(R1)             use v22 to test decoder
00004DD4  E310 5014 0014             00000014   3384+        LGF     R1,V3ADDR             load v3 source
00004DDA  E771 0000 0806             00000000   3385+        VL      v23,0(R1)             use v23 to test decoder
00004DE0  E310 5018 0014             00000018   3386+        LGF     R1,V4ADDR             load v4 source
00004DE6  E781 0000 0806             00000000   3387+        VL      v24,0(R1)             use v24 to test decoder
00004DEC  E766 7200 8FAC                        3388+        VMALE   V22,V22,V23,V24,2       test instruction (dest is a source)
00004DF2  E760 5030 080E             00004DB0   3389+        VST     V22,V1082             save v1 output
00004DF8  07FB                                  3390+        BR      R11                   return
00004DFC                                        3391+RE82    DC      0F                    xl16 expected result
00004DFC                                        3392+        DROP    R5
00004DFC  FD07050A 091F1F18                     3393         DC      XL16'FD07050A091F1F18 095BC037C27817A0'    result
00004E04  095BC037 C27817A0
00004E0C  FF020304 05060708                     3394         DC      XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00004E14  090A0B0C 0D0E0F10
00004E1C  FF020304 05060708                     3395         DC      XL16'FF02030405060708 090A0B0C0D0E0F10'    v3
00004E24  090A0B0C 0D0E0F10
00004E2C  FF020304 05060708                     3396         DC      XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00004E34  090A0B0C 0D0E0F10
                                                3397
```

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   LOC        OBJECT CODE      ADDR1    ADDR2     STMT

                                                  3398            VRR_D VMALE,2
00004E40                                          3399+           DS    0FD
00004E40                        00004E40          3400+           USING *,R5              base for test data and test routine
00004E40   00004E88                               3401+T83        DC    A(X83)            address of test routine
00004E44   0053                                   3402+           DC    H'83'             test number
00004E46   00                                     3403+           DC    X'00'
00004E47   02                                     3404+           DC    HL1'2'            m5
00004E48   E5D4C1D3 C5404040                       3405+           DC    CL8'VMALE'        instruction name
00004E50   00004ECC                               3406+           DC    A(RE83+16)        address of v2 source
00004E54   00004EDC                               3407+           DC    A(RE83+32)        address of v3 source
00004E58   00004EEC                               3408+           DC    A(RE83+48)        address of v4 source
00004E5C   00000010                               3409+           DC    A(16)             result length
00004E60   00004EBC                               3410+REA83      DC    A(RE83)           result address
00004E68   00000000 00000000                       3411+           DS    FD                gap
00004E70   00000000 00000000                       3412+V1083      DS    XL16              V1 output
00004E78   00000000 00000000
00004E80   00000000 00000000                       3413+           DS    FD                gap
                                                  3414+*
00004E88                                          3415+X83        DS    0F
00004E88   E310 5010 0014                00000010 3416+           LGF   R1,V2ADDR         load v2 source
00004E8E   E761 0000 0806                00000000 3417+           VL    v22,0(R1)         use v22 to test decoder
00004E94   E310 5014 0014                00000014 3418+           LGF   R1,V3ADDR         load v3 source
00004E9A   E771 0000 0806                00000000 3419+           VL    v23,0(R1)         use v23 to test decoder
00004EA0   E310 5018 0014                00000018 3420+           LGF   R1,V4ADDR         load v4 source
00004EA6   E781 0000 0806                00000000 3421+           VL    v24,0(R1)         use v24 to test decoder
00004EAC   E766 7200 8FAC                          3422+           VMALE V22,V22,V23,V24,2   test instruction (dest is a source)
00004EB2   E760 5030 080E                00004E70 3423+           VST   V22,V1083          save v1 output
00004EB8   07FB                                    3424+           BR    R11               return
00004EBC                                          3425+RE83       DC    0F                xl16 expected result
00004EBC                                          3426+           DROP  R5
00004EBC   FD060408 04111110                       3427            DC    XL16'FD06040804111110 092E6097DCBD8D58'     result
00004EC4   092E6097 DCBD8D58
00004ECC   FF020304 05060708                       3428            DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
00004ED4   090A0B0C 0D0E0F10
00004EDC   FF010102 02030304                       3429            DC    XL16'FF01010202030304 0405050606070708'     v3
00004EE4   04050506 06070708
00004EEC   FF020304 05060708                       3430            DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v4
00004EF4   090A0B0C 0D0E0F10
                                                  3431
                                                  3432            VRR_D VMALE,2
00004F00                                          3433+           DS    0FD
00004F00                        00004F00          3434+           USING *,R5              base for test data and test routine
00004F00   00004F48                               3435+T84        DC    A(X84)            address of test routine
00004F04   0054                                   3436+           DC    H'84'             test number
00004F06   00                                     3437+           DC    X'00'
00004F07   02                                     3438+           DC    HL1'2'            m5
00004F08   E5D4C1D3 C5404040                       3439+           DC    CL8'VMALE'        instruction name
00004F10   00004F8C                               3440+           DC    A(RE84+16)        address of v2 source
00004F14   00004F9C                               3441+           DC    A(RE84+32)        address of v3 source
00004F18   00004FAC                               3442+           DC    A(RE84+48)        address of v4 source
00004F1C   00000010                               3443+           DC    A(16)             result length
00004F20   00004F7C                               3444+REA84      DC    A(RE84)           result address
00004F28   00000000 00000000                       3445+           DS    FD                gap
00004F30   00000000 00000000                       3446+V1084      DS    XL16              V1 output
00004F38   00000000 00000000
00004F40   00000000 00000000                       3447+           DS    FD                gap
```

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  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

                                                   3448+*
00004F48                                           3449+X84      DS      0F
00004F48   E310 5010 0014                00000010  3450+         LGF     R1,V2ADDR           load v2 source
00004F4E   E761 0000 0806                00000000  3451+         VL      v22,0(R1)           use v22 to test decoder
00004F54   E310 5014 0014                00000014  3452+         LGF     R1,V3ADDR           load v3 source
00004F5A   E771 0000 0806                00000000  3453+         VL      v23,0(R1)           use v23 to test decoder
00004F60   E310 5018 0014                00000018  3454+         LGF     R1,V4ADDR           load v4 source
00004F66   E781 0000 0806                00000000  3455+         VL      v24,0(R1)           use v24 to test decoder
00004F6C   E766 7200 8FAC                          3456+         VMALE   V22,V22,V23,V24,2     test instruction (dest is a source)
00004F72   E760 5030 080E                00004F30  3457+         VST     V22,V1084            save v1 output
00004F78   07FB                                    3458+         BR      R11                 return
00004F7C                                           3459+RE84     DC      0F                  xl16 expected result
00004F7C                                           3460+         DROP    R5
00004F7C   FD050405 01060708                       3461          DC      XL16'FD05040501060708 09131E2A372F261C'     result
00004F84   09131E2A 372F261C
00004F8C   FF020304 05060708                       3462          DC      XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
00004F94   090A0B0C 0D0E0F10
00004F9C   FF000000 00000001                       3463          DC      XL16'FF00000000000001 0101010101010102'     v3
00004FA4   01010101 01010102
00004FAC   FF020304 05060708                       3464          DC      XL16'FF02030405060708 090A0B0C0D0E0F10'     v4
00004FB4   090A0B0C 0D0E0F10
                                                   3465
                                                   3466  * Doubleword
                                                   3467          VRR_D  VMALE,3
00004FC0                                           3468+         DS      0FD
00004FC0                              00004FC0     3469+         USING  *,R5                 base for test data and test routine
00004FC0   00005008                                3470+T85      DC      A(X85)              address of test routine
00004FC4   0055                                    3471+         DC      H'85'               test number
00004FC6   00                                      3472+         DC      X'00'
00004FC7   03                                      3473+         DC      HL1'3'              m5
00004FC8   E5D4C1D3 C5404040                       3474+         DC      CL8'VMALE'          instruction name
00004FD0   0000504C                                3475+         DC      A(RE85+16)          address of v2 source
00004FD4   0000505C                                3476+         DC      A(RE85+32)          address of v3 source
00004FD8   0000506C                                3477+         DC      A(RE85+48)          address of v4 source
00004FDC   00000010                                3478+         DC      A(16)               result length
00004FE0   0000503C                                3479+REA85    DC      A(RE85)             result address
00004FE8   00000000 00000000                       3480+         DS      FD                  gap
00004FF0   00000000 00000000                       3481+V1085    DS      XL16                V1 output
00004FF8   00000000 00000000
00005000   00000000 00000000                       3482+         DS      FD                  gap
                                                   3483+*
00005008                                           3484+X85      DS      0F
00005008   E310 5010 0014                00000010  3485+         LGF     R1,V2ADDR           load v2 source
0000500E   E761 0000 0806                00000000  3486+         VL      v22,0(R1)           use v22 to test decoder
00005014   E310 5014 0014                00000014  3487+         LGF     R1,V3ADDR           load v3 source
0000501A   E771 0000 0806                00000000  3488+         VL      v23,0(R1)           use v23 to test decoder
00005020   E310 5018 0014                00000018  3489+         LGF     R1,V4ADDR           load v4 source
00005026   E781 0000 0806                00000000  3490+         VL      v24,0(R1)           use v24 to test decoder
0000502C   E766 7300 8FAC                          3491+         VMALE   V22,V22,V23,V24,3     test instruction (dest is a source)
00005032   E760 5030 080E                00004FF0  3492+         VST     V22,V1085            save v1 output
00005038   07FB                                    3493+         BR      R11                 return
0000503C                                           3494+RE85     DC      0F                  xl16 expected result
0000503C                                           3495+         DROP    R5
0000503C   FFFFFFFE 00032000                       3496          DC      XL16'FFFFFFFE00032000 FFFCE00271000000'     result
00005044   FFFCE002 71000000
0000504C   FFFFFFFF 00019000                       3497          DC      XL16'FFFFFFFF00019000 00000038EEEEEEFA'     v2
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005054	00000038 EEEEEEFA						
0000505C	FFFFFFFF 00019000			3498	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00005064	00000038 0EEEEEFA						
0000506C	00000000 00000000			3499	DC	XL16'0000000000000000 0000000000000000'	v4
00005074	00000000 00000000						
				3500			
				3501	VRR_D	VMALE, 3	
00005080				3502+	DS	0FD	
00005080		00005080		3503+	USING	*,R5	base for test data and test routine
00005080	000050C8			3504+T86	DC	A(X86)	address of test routine
00005084	0056			3505+	DC	H'86'	test number
00005086	00			3506+	DC	X'00'	
00005087	03			3507+	DC	HL1'3'	m5
00005088	E5D4C1D3 C5404040			3508+	DC	CL8'VMALE'	instruction name
00005090	0000510C			3509+	DC	A(RE86+16)	address of v2 source
00005094	0000511C			3510+	DC	A(RE86+32)	address of v3 source
00005098	0000512C			3511+	DC	A(RE86+48)	address of v4 source
0000509C	00000010			3512+	DC	A(16)	result length
000050A0	000050FC			3513+REA86	DC	A(RE86)	result address
000050A8	00000000 00000000			3514+	DS	FD	gap
000050B0	00000000 00000000			3515+V1086	DS	XL16	V1 output
000050B8	00000000 00000000						
000050C0	00000000 00000000			3516+	DS	FD	gap
				3517+*			
000050C8				3518+X86	DS	0F	
000050C8	E310 5010 0014		00000010	3519+	LGF	R1, V2ADDR	load v2 source
000050CE	E761 0000 0806		00000000	3520+	VL	v22, 0(R1)	use v22 to test decoder
000050D4	E310 5014 0014		00000014	3521+	LGF	R1, V3ADDR	load v3 source
000050DA	E771 0000 0806		00000000	3522+	VL	v23, 0(R1)	use v23 to test decoder
000050E0	E310 5018 0014		00000018	3523+	LGF	R1, V4ADDR	load v4 source
000050E6	E781 0000 0806		00000000	3524+	VL	v24, 0(R1)	use v24 to test decoder
000050EC	E766 7300 8FAC			3525+	VMALE	V22, V22, V23, V24, 3	test instruction (dest is a source)
000050F2	E760 5030 080E		000050B0	3526+	VST	V22, V1086	save v1 output
000050F8	07FB			3527+	BR	R11	return
000050FC				3528+RE86	DC	0F	xl16 expected result
000050FC				3529+	DROP	R5	
000050FC	11010308 111F3397			3530	DC	XL16'11010308111F3397 79B556ED77F57901'	result
00005104	79B556ED 77F57901						
0000510C	FF020304 05060750			3531	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00005114	090A0B0C 0D0E0F7F						
0000511C	01020304 05060750			3532	DC	XL16'0102030405060750 090A0B780D0E0F7F'	v3
00005124	090A0B78 0D0E0F7F						
0000512C	10000000 00000001			3533	DC	XL16'1000000000000001 1000000000000001'	v4
00005134	10000000 00000001						
				3534			
				3535	VRR_D	VMALE, 3	
00005140				3536+	DS	0FD	
00005140		00005140		3537+	USING	*,R5	base for test data and test routine
00005140	00005188			3538+T87	DC	A(X87)	address of test routine
00005144	0057			3539+	DC	H'87'	test number
00005146	00			3540+	DC	X'00'	
00005147	03			3541+	DC	HL1'3'	m5
00005148	E5D4C1D3 C5404040			3542+	DC	CL8'VMALE'	instruction name
00005150	000051CC			3543+	DC	A(RE87+16)	address of v2 source
00005154	000051DC			3544+	DC	A(RE87+32)	address of v3 source
00005158	000051EC			3545+	DC	A(RE87+48)	address of v4 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000515C	00000010			3546+	DC	A(16)	result length
00005160	000051BC			3547+REA87	DC	A(RE87)	result address
00005168	00000000 00000000			3548+	DS	FD	gap
00005170	00000000 00000000			3549+V1087	DS	XL16	V1 output
00005178	00000000 00000000						
00005180	00000000 00000000			3550+	DS	FD	gap
				3551+*			
00005188				3552+X87	DS	0F	
00005188	E310 5010 0014		00000010	3553+	LGF	R1,V2ADDR	load v2 source
0000518E	E761 0000 0806		00000000	3554+	VL	v22,0(R1)	use v22 to test decoder
00005194	E310 5014 0014		00000014	3555+	LGF	R1,V3ADDR	load v3 source
0000519A	E771 0000 0806		00000000	3556+	VL	v23,0(R1)	use v23 to test decoder
000051A0	E310 5018 0014		00000018	3557+	LGF	R1,V4ADDR	load v4 source
000051A6	E781 0000 0806		00000000	3558+	VL	v24,0(R1)	use v24 to test decoder
000051AC	E766 7300 8FAC			3559+	VMALE	V22,V22,V23,V24,3	test instruction (dest is a source)
000051B2	E760 5030 080E		00005170	3560+	VST	V22,V1087	save v1 output
000051B8	07FB			3561+	BR	R11	return
000051BC				3562+RE87	DC	0F	xl16 expected result
000051BC				3563+	DROP	R5	
000051BC	EE010003 050C1352			3564	DC	XL16'EE010003050C1352 E6D2FE7090F7148E'	result
000051C4	E6D2FE70 90F7148E						
000051CC	FF020304 05060750			3565	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
000051D4	090A0B0C 0D0E0F7F						
000051DC	00010102 02030328			3566	DC	XL16'0001010202030328 0405053C0607073F'	v3
000051E4	0405053C 0607073F						
000051EC	EE000000 0000000E			3567	DC	XL16'EE0000000000000E E00000000000000E'	v4
000051F4	E0000000 0000000E						
				3568			
				3569	VRR_D	VMALE,3	
00005200				3570+	DS	0FD	
00005200		00005200		3571+	USING	*,R5	base for test data and test routine
00005200	00005248			3572+T88	DC	A(X88)	address of test routine
00005204	0058			3573+	DC	H'88'	test number
00005206	00			3574+	DC	X'00'	
00005207	03			3575+	DC	HL1'3'	m5
00005208	E5D4C1D3 C5404040			3576+	DC	CL8'VMALE'	instruction name
00005210	0000528C			3577+	DC	A(RE88+16)	address of v2 source
00005214	0000529C			3578+	DC	A(RE88+32)	address of v3 source
00005218	000052AC			3579+	DC	A(RE88+48)	address of v4 source
0000521C	00000010			3580+	DC	A(16)	result length
00005220	0000527C			3581+REA88	DC	A(RE88)	result address
00005228	00000000 00000000			3582+	DS	FD	gap
00005230	00000000 00000000			3583+V1088	DS	XL16	V1 output
00005238	00000000 00000000						
00005240	00000000 00000000			3584+	DS	FD	gap
				3585+*			
00005248				3586+X88	DS	0F	
00005248	E310 5010 0014		00000010	3587+	LGF	R1,V2ADDR	load v2 source
0000524E	E761 0000 0806		00000000	3588+	VL	v22,0(R1)	use v22 to test decoder
00005254	E310 5014 0014		00000014	3589+	LGF	R1,V3ADDR	load v3 source
0000525A	E771 0000 0806		00000000	3590+	VL	v23,0(R1)	use v23 to test decoder
00005260	E310 5018 0014		00000018	3591+	LGF	R1,V4ADDR	load v4 source
00005266	E781 0000 0806		00000000	3592+	VL	v24,0(R1)	use v24 to test decoder
0000526C	E766 7300 8FAC			3593+	VMALE	V22,V22,V23,V24,3	test instruction (dest is a source)
00005272	E760 5030 080E		00005230	3594+	VST	V22,V1088	save v1 output
00005278	07FB			3595+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000527C				3596+RE88	DC	0F	xl16 expected result
0000527C				3597+	DROP	R5	
0000527C	FFF00000 00000009			3598	DC	XL16'FFF0000000000009 F6141E28323C492F'	result
00005284	F6141E28 323C492F						
0000528C	FF020304 05060750			3599	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00005294	090A0B0C 0D0E0F7F						
0000529C	00000000 0000000A			3600	DC	XL16'000000000000000A 0101010F0101010F'	v3
000052A4	0101010F 0101010F						
000052AC	FFF00000 00000000			3601	DC	XL16'FFF0000000000000 000000000000000F'	v4
000052B4	00000000 0000000F						
				3602			
				3603	VRR_D	VMALE, 3	
000052C0				3604+	DS	0FD	
000052C0			000052C0	3605+	USING	*,R5	base for test data and test routine
000052C0	00005308			3606+T89	DC	A(X89)	address of test routine
000052C4	0059			3607+	DC	H'89'	test number
000052C6	00			3608+	DC	X'00'	
000052C7	03			3609+	DC	HL1'3'	m5
000052C8	E5D4C1D3 C5404040			3610+	DC	CL8'VMALE'	instruction name
000052D0	0000534C			3611+	DC	A(RE89+16)	address of v2 source
000052D4	0000535C			3612+	DC	A(RE89+32)	address of v3 source
000052D8	0000536C			3613+	DC	A(RE89+48)	address of v4 source
000052DC	00000010			3614+	DC	A(16)	result length
000052E0	0000533C			3615+REA89	DC	A(RE89)	result address
000052E8	00000000 00000000			3616+	DS	FD	gap
000052F0	00000000 00000000			3617+V1089	DS	XL16	V1 output
000052F8	00000000 00000000						
00005300	00000000 00000000			3618+	DS	FD	gap
				3619+*			
00005308				3620+X89	DS	0F	
00005308	E310 5010 0014		00000010	3621+	LGF	R1,V2ADDR	load v2 source
0000530E	E761 0000 0806		00000000	3622+	VL	v22,0(R1)	use v22 to test decoder
00005314	E310 5014 0014		00000014	3623+	LGF	R1,V3ADDR	load v3 source
0000531A	E771 0000 0806		00000000	3624+	VL	v23,0(R1)	use v23 to test decoder
00005320	E310 5018 0014		00000018	3625+	LGF	R1,V4ADDR	load v4 source
00005326	E781 0000 0806		00000000	3626+	VL	v24,0(R1)	use v24 to test decoder
0000532C	E766 7300 8FAC			3627+	VMALE	V22,V22,V23,V24,3	test instruction (dest is a source)
00005332	E760 5030 080E		000052F0	3628+	VST	V22,V1089	save v1 output
00005338	07FB			3629+	BR	R11	return
0000533C				3630+RE89	DC	0F	xl16 expected result
0000533C				3631+	DROP	R5	
0000533C	1009131E A8C3DFFF			3632	DC	XL16'1009131EA8C3DFFF 191C345060616772'	result
00005344	191C3450 60616772						
0000534C	090A0B0C 0D0E0F7F			3633	DC	XL16'090A0B0C0D0E0F7F FF02030405060750'	v2
00005354	FF020304 05060750						
0000535C	0101010F 0101010F			3634	DC	XL16'0101010F0101010F 000000000000000A'	v3
00005364	00000000 0000000A						
0000536C	10000000 00000001			3635	DC	XL16'1000000000000001 1000000000000001'	v4
00005374	10000000 00000001						
				3636			
				3637	*---		
				3638	* VMALO - Vector Multiply and Add Logical Odd		
				3639	*---		
				3640	* Byte		
				3641	VRR_D	VMALO, 0	
00005380				3642+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005380		00005380		3643+		USING *,R5	base for test data and test routine
00005380	000053C8			3644+T90	DC	A(X90)	address of test routine
00005384	005A			3645+	DC	H'90'	test number
00005386	00			3646+	DC	X'00'	
00005387	00			3647+	DC	HL1'0'	m5
00005388	E5D4C1D3 D6404040			3648+	DC	CL8'VMALO'	instruction name
00005390	0000540C			3649+	DC	A(RE90+16)	address of v2 source
00005394	0000541C			3650+	DC	A(RE90+32)	address of v3 source
00005398	0000542C			3651+	DC	A(RE90+48)	address of v4 source
0000539C	00000010			3652+	DC	A(16)	result length
000053A0	000053FC			3653+REA90	DC	A(RE90)	result address
000053A8	00000000 00000000			3654+	DS	FD	gap
000053B0	00000000 00000000			3655+V1090	DS	XL16	V1 output
000053B8	00000000 00000000						
000053C0	00000000 00000000			3656+	DS	FD	gap
				3657+*			
000053C8				3658+X90	DS	0F	
000053C8	E310 5010 0014		00000010	3659+	LGF	R1,V2ADDR	load v2 source
000053CE	E761 0000 0806		00000000	3660+	VL	v22,0(R1)	use v22 to test decoder
000053D4	E310 5014 0014		00000014	3661+	LGF	R1,V3ADDR	load v3 source
000053DA	E771 0000 0806		00000000	3662+	VL	v23,0(R1)	use v23 to test decoder
000053E0	E310 5018 0014		00000018	3663+	LGF	R1,V4ADDR	load v4 source
000053E6	E781 0000 0806		00000000	3664+	VL	v24,0(R1)	use v24 to test decoder
000053EC	E766 7000 8FAD			3665+	VMALO	V22,V22,V23,V24,0	test instruction (dest is a source)
000053F2	E760 5030 080E		000053B0	3666+	VST	V22,V1090	save v1 output
000053F8	07FB			3667+	BR	R11	return
000053FC				3668+RE90	DC	0F	xl16 expected result
000053FC				3669+	DROP	R5	
000053FC	00000000 00000271			3670	DC	XL16'0000000000000271 00000C400000F424'	result
00005404	00000C40 0000F424						
0000540C	FF000000 00000019			3671	DC	XL16'FF00000000000019 00000038000000FA'	v2
00005414	00000038 000000FA						
0000541C	FF000000 00000019			3672	DC	XL16'FF00000000000019 00000038000000FA'	v3
00005424	00000038 000000FA						
0000542C	00000000 00000000			3673	DC	XL16'0000000000000000 0000000000000000'	v4
00005434	00000000 00000000						
				3674			
				3675		VRR_D VMALO,0	
00005440				3676+	DS	0FD	
00005440		00005440		3677+		USING *,R5	base for test data and test routine
00005440	00005488			3678+T91	DC	A(X91)	address of test routine
00005444	005B			3679+	DC	H'91'	test number
00005446	00			3680+	DC	X'00'	
00005447	00			3681+	DC	HL1'0'	m5
00005448	E5D4C1D3 D6404040			3682+	DC	CL8'VMALO'	instruction name
00005450	000054CC			3683+	DC	A(RE91+16)	address of v2 source
00005454	000054DC			3684+	DC	A(RE91+32)	address of v3 source
00005458	000054EC			3685+	DC	A(RE91+48)	address of v4 source
0000545C	00000010			3686+	DC	A(16)	result length
00005460	000054BC			3687+REA91	DC	A(RE91)	result address
00005468	00000000 00000000			3688+	DS	FD	gap
00005470	00000000 00000000			3689+V1091	DS	XL16	V1 output
00005478	00000000 00000000						
00005480	00000000 00000000			3690+	DS	FD	gap
				3691+*			
00005488				3692+X91	DS	0F	

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  LOC          OBJECT CODE       ADDR1     ADDR2     STMT

00005488  E310 5010 0014               00000010  3693+        LGF     R1,V2ADDR       load v2 source
0000548E  E761 0000 0806               00000000  3694+        VL      v22,0(R1)       use v22 to test decoder
00005494  E310 5014 0014               00000014  3695+        LGF     R1,V3ADDR       load v3 source
0000549A  E771 0000 0806               00000000  3696+        VL      v23,0(R1)       use v23 to test decoder
000054A0  E310 5018 0014               00000018  3697+        LGF     R1,V4ADDR       load v4 source
000054A6  E781 0000 0806               00000000  3698+        VL      v24,0(R1)       use v24 to test decoder
000054AC  E766 7000 8FAD                         3699+        VMALO   V22,V22,V23,V24,0    test instruction (dest is a source)
000054B2  E760 5030 080E               00005470  3700+        VST     V22,V1091       save v1 output
000054B8  07FB                                   3701+        BR      R11             return
000054BC                                         3702+RE91    DC      0F              xl16 expected result
000054BC                                         3703+        DROP    R5
000054BC  00020100 000006C0                      3704         DC      XL16'00020100000006C0 00000C430000F426'    result
000054C4  00000C43 0000F426
000054CC  FF0000FF 00000029                      3705         DC      XL16'FF0000FF00000029 00000038000000FA'    v2
000054D4  00000038 000000FA
000054DC  FF000001 00000029                      3706         DC      XL16'FF00000100000029 00000038000000FA'    v3
000054E4  00000038 000000FA
000054EC  00020001 0000002F                      3707         DC      XL16'000200010000002F 0000000300000002'    v4
000054F4  00000003 00000002

                                                 3708
                                                 3709         VRR_D VMALO,0
00005500                                         3710+        DS      0FD
00005500                             00005500    3711+        USING   *,R5            base for test data and test routine
00005500  00005548                              3712+T92     DC      A(X92)          address of test routine
00005504  005C                                  3713+        DC      H'92'           test number
00005506  00                                    3714+        DC      X'00'
00005507  00                                    3715+        DC      HL1'0'          m5
00005508  E5D4C1D3 D6404040                      3716+        DC      CL8'VMALO'      instruction name
00005510  0000558C                              3717+        DC      A(RE92+16)      address of v2 source
00005514  0000559C                              3718+        DC      A(RE92+32)      address of v3 source
00005518  000055AC                              3719+        DC      A(RE92+48)      address of v4 source
0000551C  00000010                              3720+        DC      A(16)           result length
00005520  0000557C                              3721+REA92   DC      A(RE92)         result address
00005528  00000000 00000000                      3722+        DS      FD              gap
00005530  00000000 00000000                      3723+V1092   DS      XL16            V1 output
00005538  00000000 00000000
00005540  00000000 00000000                      3724+        DS      FD              gap
                                                 3725+*
00005548                                         3726+X92     DS      0F
00005548  E310 5010 0014               00000010  3727+        LGF     R1,V2ADDR       load v2 source
0000554E  E761 0000 0806               00000000  3728+        VL      v22,0(R1)       use v22 to test decoder
00005554  E310 5014 0014               00000014  3729+        LGF     R1,V3ADDR       load v3 source
0000555A  E771 0000 0806               00000000  3730+        VL      v23,0(R1)       use v23 to test decoder
00005560  E310 5018 0014               00000018  3731+        LGF     R1,V4ADDR       load v4 source
00005566  E781 0000 0806               00000000  3732+        VL      v24,0(R1)       use v24 to test decoder
0000556C  E766 7000 8FAD                         3733+        VMALO   V22,V22,V23,V24,0    test instruction (dest is a source)
00005572  E760 5030 080E               00005530  3734+        VST     V22,V1092       save v1 output
00005578  07FB                                   3735+        BR      R11             return
0000557C                                         3736+RE92    DC      0F              xl16 expected result
0000557C                                         3737+        DROP    R5
0000557C  FF060314 052A0748                      3738         DC      XL16'FF060314052A0748 096E0B9C0DD21010'    result
00005584  096E0B9C 0DD21010
0000558C  FF020304 05060708                      3739         DC      XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00005594  090A0B0C 0D0E0F10
0000559C  FF020304 05060708                      3740         DC      XL16'FF02030405060708 090A0B0C0D0E0F10'    v3
000055A4  090A0B0C 0D0E0F10
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000055AC	FF020304 05060708			3741	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
000055B4	090A0B0C 0D0E0F10						
				3742			
				3743	VRR_D	VMALO,0	
000055C0				3744+	DS	0FD	
000055C0		000055C0		3745+	USING	*,R5	base for test data and test routine
000055C0	00005608			3746+T93	DC	A(X93)	address of test routine
000055C4	005D			3747+	DC	H'93'	test number
000055C6	00			3748+	DC	X'00'	
000055C7	00			3749+	DC	HL1'0'	m5
000055C8	E5D4C1D3 D6404040			3750+	DC	CL8'VMALO'	instruction name
000055D0	0000564C			3751+	DC	A(RE93+16)	address of v2 source
000055D4	0000565C			3752+	DC	A(RE93+32)	address of v3 source
000055D8	0000566C			3753+	DC	A(RE93+48)	address of v4 source
000055DC	00000010			3754+	DC	A(16)	result length
000055E0	0000563C			3755+REA93	DC	A(RE93)	result address
000055E8	00000000 00000000			3756+	DS	FD	gap
000055F0	00000000 00000000			3757+V1093	DS	XL16	V1 output
000055F8	00000000 00000000						
00005600	00000000 00000000			3758+	DS	FD	gap
				3759+*			
00005608				3760+X93	DS	0F	
00005608	E310 5010 0014		00000010	3761+	LGF	R1,V2ADDR	load v2 source
0000560E	E761 0000 0806		00000000	3762+	VL	v22,0(R1)	use v22 to test decoder
00005614	E310 5014 0014		00000014	3763+	LGF	R1,V3ADDR	load v3 source
0000561A	E771 0000 0806		00000000	3764+	VL	v23,0(R1)	use v23 to test decoder
00005620	E310 5018 0014		00000018	3765+	LGF	R1,V4ADDR	load v4 source
00005626	E781 0000 0806		00000000	3766+	VL	v24,0(R1)	use v24 to test decoder
0000562C	E766 7000 8FAD			3767+	VMALO	V22,V22,V23,V24,0	test instruction (dest is a source)
00005632	E760 5030 080E		000055F0	3768+	VST	V22,V1093	save v1 output
00005638	07FB			3769+	BR	R11	return
0000563C				3770+RE93	DC	0F	xl16 expected result
0000563C				3771+	DROP	R5	
0000563C	FF04030C 05180728			3772	DC	XL16'FF04030C05180728 093C0B540D700F90'	result
00005644	093C0B54 0D700F90						
0000564C	FF020304 05060708			3773	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00005654	090A0B0C 0D0E0F10						
0000565C	FF010102 02030304			3774	DC	XL16'FF01010202030304 0405050606070708'	v3
00005664	04050506 06070708						
0000566C	FF020304 05060708			3775	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00005674	090A0B0C 0D0E0F10						
				3776			
				3777	VRR_D	VMALO,0	
00005680				3778+	DS	0FD	
00005680		00005680		3779+	USING	*,R5	base for test data and test routine
00005680	000056C8			3780+T94	DC	A(X94)	address of test routine
00005684	005E			3781+	DC	H'94'	test number
00005686	00			3782+	DC	X'00'	
00005687	00			3783+	DC	HL1'0'	m5
00005688	E5D4C1D3 D6404040			3784+	DC	CL8'VMALO'	instruction name
00005690	0000570C			3785+	DC	A(RE94+16)	address of v2 source
00005694	0000571C			3786+	DC	A(RE94+32)	address of v3 source
00005698	0000572C			3787+	DC	A(RE94+48)	address of v4 source
0000569C	00000010			3788+	DC	A(16)	result length
000056A0	000056FC			3789+REA94	DC	A(RE94)	result address
000056A8	00000000 00000000			3790+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000056B0	00000000 00000000			3791+V1094	DS	XL16	V1 output
000056B8	00000000 00000000						
000056C0	00000000 00000000			3792+	DS	FD	gap
				3793+*			
000056C8				3794+X94	DS	0F	
000056C8	E310 5010 0014		00000010	3795+	LGF	R1,V2ADDR	load v2 source
000056CE	E761 0000 0806		00000000	3796+	VL	v22,0(R1)	use v22 to test decoder
000056D4	E310 5014 0014		00000014	3797+	LGF	R1,V3ADDR	load v3 source
000056DA	E771 0000 0806		00000000	3798+	VL	v23,0(R1)	use v23 to test decoder
000056E0	E310 5018 0014		00000018	3799+	LGF	R1,V4ADDR	load v4 source
000056E6	E781 0000 0806		00000000	3800+	VL	v24,0(R1)	use v24 to test decoder
000056EC	E766 7000 8FAD			3801+	VMALO	V22,V22,V23,V24,0	test instruction (dest is a source)
000056F2	E760 5030 080E		000056B0	3802+	VST	V22,V1094	save v1 output
000056F8	07FB			3803+	BR	R11	return
000056FC				3804+RE94	DC	0F	xl16 expected result
000056FC				3805+	DROP	R5	
000056FC	FF020304 05060710			3806	DC	XL16'FF02030405060710 09140B180D1C0F30'	result
00005704	09140B18 0D1C0F30						
0000570C	FF020304 05060708			3807	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00005714	090A0B0C 0D0E0F10						
0000571C	FF000000 00000001			3808	DC	XL16'FF00000000000001 0101010101010102'	v3
00005724	01010101 01010102						
0000572C	FF020304 05060708			3809	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00005734	090A0B0C 0D0E0F10						
				3810			
				3811	* Halfword		
				3812	VRR_D	VMALO,1	
00005740				3813+	DS	0FD	
00005740			00005740	3814+	USING	*,R5	base for test data and test routine
00005740	00005788			3815+T95	DC	A(X95)	address of test routine
00005744	005F			3816+	DC	H'95'	test number
00005746	00			3817+	DC	X'00'	
00005747	01			3818+	DC	HL1'1'	m5
00005748	E5D4C1D3 D6404040			3819+	DC	CL8'VMALO'	instruction name
00005750	000057CC			3820+	DC	A(RE95+16)	address of v2 source
00005754	000057DC			3821+	DC	A(RE95+32)	address of v3 source
00005758	000057EC			3822+	DC	A(RE95+48)	address of v4 source
0000575C	00000010			3823+	DC	A(16)	result length
00005760	000057BC			3824+REA95	DC	A(RE95)	result address
00005768	00000000 00000000			3825+	DS	FD	gap
00005770	00000000 00000000			3826+V1095	DS	XL16	V1 output
00005778	00000000 00000000						
00005780	00000000 00000000			3827+	DS	FD	gap
				3828+*			
00005788				3829+X95	DS	0F	
00005788	E310 5010 0014		00000010	3830+	LGF	R1,V2ADDR	load v2 source
0000578E	E761 0000 0806		00000000	3831+	VL	v22,0(R1)	use v22 to test decoder
00005794	E310 5014 0014		00000014	3832+	LGF	R1,V3ADDR	load v3 source
0000579A	E771 0000 0806		00000000	3833+	VL	v23,0(R1)	use v23 to test decoder
000057A0	E310 5018 0014		00000018	3834+	LGF	R1,V4ADDR	load v4 source
000057A6	E781 0000 0806		00000000	3835+	VL	v24,0(R1)	use v24 to test decoder
000057AC	E766 7100 8FAD			3836+	VMALO	V22,V22,V23,V24,1	test instruction (dest is a source)
000057B2	E760 5030 080E		00005770	3837+	VST	V22,V1095	save v1 output
000057B8	07FB			3838+	BR	R11	return
000057BC				3839+RE95	DC	0F	xl16 expected result
000057BC				3840+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000057BC	00000000 00000271			3841	DC	XL16'0000000000000271 00000C400000F424'	result
000057C4	00000C40 0000F424						
000057CC	FF000000 00000019			3842	DC	XL16'FF00000000000019 00000038000000FA'	v2
000057D4	00000038 000000FA						
000057DC	FF000000 00000019			3843	DC	XL16'FF00000000000019 00000038000000FA'	v3
000057E4	00000038 000000FA						
000057EC	00000000 00000000			3844	DC	XL16'0000000000000000 0000000000000000'	v4
000057F4	00000000 00000000						
				3845			
				3846	VRR_D	VMALO,1	
00005800				3847+	DS	0FD	
00005800		00005800		3848+	USING	*,R5	base for test data and test routine
00005800	00005848			3849+T96	DC	A(X96)	address of test routine
00005804	0060			3850+	DC	H'96'	test number
00005806	00			3851+	DC	X'00'	
00005807	01			3852+	DC	HL1'1'	m5
00005808	E5D4C1D3 D6404040			3853+	DC	CL8'VMALO'	instruction name
00005810	0000588C			3854+	DC	A(RE96+16)	address of v2 source
00005814	0000589C			3855+	DC	A(RE96+32)	address of v3 source
00005818	000058AC			3856+	DC	A(RE96+48)	address of v4 source
0000581C	00000010			3857+	DC	A(16)	result length
00005820	0000587C			3858+REA96	DC	A(RE96)	result address
00005828	00000000 00000000			3859+	DS	FD	gap
00005830	00000000 00000000			3860+V1096	DS	XL16	V1 output
00005838	00000000 00000000						
00005840	00000000 00000000			3861+	DS	FD	gap
				3862+*			
00005848				3863+X96	DS	0F	
00005848	E310 5010 0014		00000010	3864+	LGF	R1,V2ADDR	load v2 source
0000584E	E761 0000 0806		00000000	3865+	VL	v22,0(R1)	use v22 to test decoder
00005854	E310 5014 0014		00000014	3866+	LGF	R1,V3ADDR	load v3 source
0000585A	E771 0000 0806		00000000	3867+	VL	v23,0(R1)	use v23 to test decoder
00005860	E310 5018 0014		00000018	3868+	LGF	R1,V4ADDR	load v4 source
00005866	E781 0000 0806		00000000	3869+	VL	v24,0(R1)	use v24 to test decoder
0000586C	E766 7100 8FAD			3870+	VMALO	V22,V22,V23,V24,1	test instruction (dest is a source)
00005872	E760 5030 080E		00005830	3871+	VST	V22,V1096	save v1 output
00005878	07FB			3872+	BR	R11	return
0000587C				3873+RE96	DC	0F	xl16 expected result
0000587C				3874+	DROP	R5	
0000587C	00020100 000006C0			3875	DC	XL16'00020100000006C0 00000C430000F426'	result
00005884	00000C43 0000F426						
0000588C	FF0000FF 00000029			3876	DC	XL16'FF0000FF00000029 00000038000000FA'	v2
00005894	00000038 000000FA						
0000589C	FF000001 00000029			3877	DC	XL16'FF00000100000029 00000038000000FA'	v3
000058A4	00000038 000000FA						
000058AC	00020001 0000002F			3878	DC	XL16'000200010000002F 0000000300000002'	v4
000058B4	00000003 00000002						
				3879			
				3880	VRR_D	VMALO,1	
000058C0				3881+	DS	0FD	
000058C0		000058C0		3882+	USING	*,R5	base for test data and test routine
000058C0	00005908			3883+T97	DC	A(X97)	address of test routine
000058C4	0061			3884+	DC	H'97'	test number
000058C6	00			3885+	DC	X'00'	
000058C7	01			3886+	DC	HL1'1'	m5
000058C8	E5D4C1D3 D6404040			3887+	DC	CL8'VMALO'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000058D0	0000594C			3888+	DC	A(RE97+16)	address of v2 source
000058D4	0000595C			3889+	DC	A(RE97+32)	address of v3 source
000058D8	0000596C			3890+	DC	A(RE97+48)	address of v4 source
000058DC	00000010			3891+	DC	A(16)	result length
000058E0	0000593C			3892+REA97	DC	A(RE97)	result address
000058E8	00000000 00000000			3893+	DS	FD	gap
000058F0	00000000 00000000			3894+V1097	DS	XL16	V1 output
000058F8	00000000 00000000						
00005900	00000000 00000000			3895+	DS	FD	gap
				3896+*			
00005908				3897+X97	DS	0F	
00005908	E310 5010 0014		00000010	3898+	LGF	R1,V2ADDR	load v2 source
0000590E	E761 0000 0806		00000000	3899+	VL	v22,0(R1)	use v22 to test decoder
00005914	E310 5014 0014		00000014	3900+	LGF	R1,V3ADDR	load v3 source
0000591A	E771 0000 0806		00000000	3901+	VL	v23,0(R1)	use v23 to test decoder
00005920	E310 5018 0014		00000018	3902+	LGF	R1,V4ADDR	load v4 source
00005926	E781 0000 0806		00000000	3903+	VL	v24,0(R1)	use v24 to test decoder
0000592C	E766 7100 8FAD			3904+	VMALO	V22,V22,V23,V24,1	test instruction (dest is a source)
00005932	E760 5030 080E		000058F0	3905+	VST	V22,V1097	save v1 output
00005938	07FB			3906+	BR	R11	return
0000593C				3907+RE97	DC	0F	xl16 expected result
0000593C				3908+	DROP	R5	
0000593C	FF0B1B14 05377748			3909	DC	XL16'FF0B1B1405377748 0984139C0DF0F010'	result
00005944	0984139C 0DF0F010						
0000594C	FF020304 05060708			3910	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00005954	090A0B0C 0D0E0F10						
0000595C	FF020304 05060708			3911	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3
00005964	090A0B0C 0D0E0F10						
0000596C	FF020304 05060708			3912	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00005974	090A0B0C 0D0E0F10						
				3913			
				3914	VRR_D	VMAL0,1	
00005980				3915+	DS	0FD	
00005980		00005980		3916+	USING	*,R5	base for test data and test routine
00005980	000059C8			3917+T98	DC	A(X98)	address of test routine
00005984	0062			3918+	DC	H'98'	test number
00005986	00			3919+	DC	X'00'	
00005987	01			3920+	DC	HL1'1'	m5
00005988	E5D4C1D3 D6404040			3921+	DC	CL8'VMAL0'	instruction name
00005990	00005A0C			3922+	DC	A(RE98+16)	address of v2 source
00005994	00005A1C			3923+	DC	A(RE98+32)	address of v3 source
00005998	00005A2C			3924+	DC	A(RE98+48)	address of v4 source
0000599C	00000010			3925+	DC	A(16)	result length
000059A0	000059FC			3926+REA98	DC	A(RE98)	result address
000059A8	00000000 00000000			3927+	DS	FD	gap
000059B0	00000000 00000000			3928+V1098	DS	XL16	V1 output
000059B8	00000000 00000000						
000059C0	00000000 00000000			3929+	DS	FD	gap
				3930+*			
000059C8				3931+X98	DS	0F	
000059C8	E310 5010 0014		00000010	3932+	LGF	R1,V2ADDR	load v2 source
000059CE	E761 0000 0806		00000000	3933+	VL	v22,0(R1)	use v22 to test decoder
000059D4	E310 5014 0014		00000014	3934+	LGF	R1,V3ADDR	load v3 source
000059DA	E771 0000 0806		00000000	3935+	VL	v23,0(R1)	use v23 to test decoder
000059E0	E310 5018 0014		00000018	3936+	LGF	R1,V4ADDR	load v4 source
000059E6	E781 0000 0806		00000000	3937+	VL	v24,0(R1)	use v24 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000059EC	E766 7100 8FAD			3938+		VMALO	V22,V22,V23,V24,1	test instruction (dest is a source)
000059F2	E760 5030 080E		000059B0	3939+		VST	V22,V1098	save v1 output
000059F8	07FB			3940+		BR	R11	return
000059FC				3941+RE98		DC	0F	xl16 expected result
000059FC				3942+		DROP	R5	
000059FC	FF050D0C 051B3B28			3943		DC	XL16'FF050D0C051B3B28 094189540D77F790'	result
00005A04	09418954 0D77F790							
00005A0C	FF020304 05060708			3944		DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00005A14	090A0B0C 0D0E0F10							
00005A1C	FF010102 02030304			3945		DC	XL16'FF01010202030304 0405050606070708'	v3
00005A24	04050506 06070708							
00005A2C	FF020304 05060708			3946		DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00005A34	090A0B0C 0D0E0F10							
				3947				
				3948		VRR_D	VMALO,1	
00005A40				3949+		DS	0FD	
00005A40			00005A40	3950+		USING	*,R5	base for test data and test routine
00005A40	00005A88			3951+T99		DC	A(X99)	address of test routine
00005A44	0063			3952+		DC	H'99'	test number
00005A46	00			3953+		DC	X'00'	
00005A47	01			3954+		DC	HL1'1'	m5
00005A48	E5D4C1D3 D6404040			3955+		DC	CL8'VMALO'	instruction name
00005A50	00005ACC			3956+		DC	A(RE99+16)	address of v2 source
00005A54	00005ADC			3957+		DC	A(RE99+32)	address of v3 source
00005A58	00005AEC			3958+		DC	A(RE99+48)	address of v4 source
00005A5C	00000010			3959+		DC	A(16)	result length
00005A60	00005ABC			3960+REA99		DC	A(RE99)	result address
00005A68	00000000 00000000			3961+		DS	FD	gap
00005A70	00000000 00000000			3962+V1099		DS	XL16	V1 output
00005A78	00000000 00000000							
00005A80	00000000 00000000			3963+		DS	FD	gap
				3964+*				
00005A88				3965+X99		DS	0F	
00005A88	E310 5010 0014		00000010	3966+		LGF	R1,V2ADDR	load v2 source
00005A8E	E761 0000 0806		00000000	3967+		VL	v22,0(R1)	use v22 to test decoder
00005A94	E310 5014 0014		00000014	3968+		LGF	R1,V3ADDR	load v3 source
00005A9A	E771 0000 0806		00000000	3969+		VL	v23,0(R1)	use v23 to test decoder
00005AA0	E310 5018 0014		00000018	3970+		LGF	R1,V4ADDR	load v4 source
00005AA6	E781 0000 0806		00000000	3971+		VL	v24,0(R1)	use v24 to test decoder
00005AAC	E766 7100 8FAD			3972+		VMALO	V22,V22,V23,V24,1	test instruction (dest is a source)
00005AB2	E760 5030 080E		00005A70	3973+		VST	V22,V1099	save v1 output
00005AB8	07FB			3974+		BR	R11	return
00005ABC				3975+RE99		DC	0F	xl16 expected result
00005ABC				3976+		DROP	R5	
00005ABC	FF020304 05060E10			3977		DC	XL16'FF02030405060E10 091522180D1D3D30'	result
00005AC4	09152218 0D1D3D30							
00005ACC	FF020304 05060708			3978		DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00005AD4	090A0B0C 0D0E0F10							
00005ADC	FF000000 00000001			3979		DC	XL16'FF00000000000001 0101010101010102'	v3
00005AE4	01010101 01010102							
00005AEC	FF020304 05060708			3980		DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00005AF4	090A0B0C 0D0E0F10							
				3981				
				3982 * Word				
				3983		VRR_D	VMALO,2	
00005B00				3984+		DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005B00		00005B00		3985+		USING *,R5	base for test data and test routine
00005B00	00005B48			3986+T100	DC	A(X100)	address of test routine
00005B04	0064			3987+	DC	H'100'	test number
00005B06	00			3988+	DC	X'00'	
00005B07	02			3989+	DC	HL1'2'	m5
00005B08	E5D4C1D3 D6404040			3990+	DC	CL8'VMALO'	instruction name
00005B10	00005B8C			3991+	DC	A(RE100+16)	address of v2 source
00005B14	00005B9C			3992+	DC	A(RE100+32)	address of v3 source
00005B18	00005BAC			3993+	DC	A(RE100+48)	address of v4 source
00005B1C	00000010			3994+	DC	A(16)	result length
00005B20	00005B7C			3995+REA100	DC	A(RE100)	result address
00005B28	00000000 00000000			3996+	DS	FD	gap
00005B30	00000000 00000000			3997+V10100	DS	XL16	V1 output
00005B38	00000000 00000000						
00005B40	00000000 00000000			3998+	DS	FD	gap
				3999+*			
00005B48				4000+X100	DS	0F	
00005B48	E310 5010 0014		00000010	4001+	LGF	R1,V2ADDR	load v2 source
00005B4E	E761 0000 0806		00000000	4002+	VL	v22,0(R1)	use v22 to test decoder
00005B54	E310 5014 0014		00000014	4003+	LGF	R1,V3ADDR	load v3 source
00005B5A	E771 0000 0806		00000000	4004+	VL	v23,0(R1)	use v23 to test decoder
00005B60	E310 5018 0014		00000018	4005+	LGF	R1,V4ADDR	load v4 source
00005B66	E781 0000 0806		00000000	4006+	VL	v24,0(R1)	use v24 to test decoder
00005B6C	E766 7200 8FAD			4007+	VMALO	V22,V22,V23,V24,2	test instruction (dest is a source)
00005B72	E760 5030 080E		00005B30	4008+	VST	V22,V10100	save v1 output
00005B78	07FB			4009+	BR	R11	return
00005B7C				4010+RE100	DC	0F	xl16 expected result
00005B7C				4011+	DROP	R5	
00005B7C	00000000 00000271			4012	DC	XL16'0000000000000271 000000000000F424'	result
00005B84	00000000 0000F424						
00005B8C	FF000000 00000019			4013	DC	XL16'FF00000000000019 0000038000000FA'	v2
00005B94	00000038 000000FA						
00005B9C	FF000000 00000019			4014	DC	XL16'FF00000000000019 0000038000000FA'	v3
00005BA4	00000038 000000FA						
00005BAC	00000000 00000000			4015	DC	XL16'0000000000000000 0000000000000000'	v4
00005BB4	00000000 00000000						
				4016			
				4017	VRR_D	VMALO,2	
00005BC0				4018+	DS	0FD	
00005BC0		00005BC0		4019+	USING *,R5		base for test data and test routine
00005BC0	00005C08			4020+T101	DC	A(X101)	address of test routine
00005BC4	0065			4021+	DC	H'101'	test number
00005BC6	00			4022+	DC	X'00'	
00005BC7	02			4023+	DC	HL1'2'	m5
00005BC8	E5D4C1D3 D6404040			4024+	DC	CL8'VMALO'	instruction name
00005BD0	00005C4C			4025+	DC	A(RE101+16)	address of v2 source
00005BD4	00005C5C			4026+	DC	A(RE101+32)	address of v3 source
00005BD8	00005C6C			4027+	DC	A(RE101+48)	address of v4 source
00005BDC	00000010			4028+	DC	A(16)	result length
00005BE0	00005C3C			4029+REA101	DC	A(RE101)	result address
00005BE8	00000000 00000000			4030+	DS	FD	gap
00005BF0	00000000 00000000			4031+V10101	DS	XL16	V1 output
00005BF8	00000000 00000000						
00005C00	00000000 00000000			4032+	DS	FD	gap
				4033+*			
00005C08				4034+X101	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005C08	E310 5010 0014		00000010	4035+	LGF	R1,V2ADDR	load v2 source
00005C0E	E761 0000 0806		00000000	4036+	VL	v22,0(R1)	use v22 to test decoder
00005C14	E310 5014 0014		00000014	4037+	LGF	R1,V3ADDR	load v3 source
00005C1A	E771 0000 0806		00000000	4038+	VL	v23,0(R1)	use v23 to test decoder
00005C20	E310 5018 0014		00000018	4039+	LGF	R1,V4ADDR	load v4 source
00005C26	E781 0000 0806		00000000	4040+	VL	v24,0(R1)	use v24 to test decoder
00005C2C	E766 7200 8FAD			4041+	VMALO	V22,V22,V23,V24,2	test instruction (dest is a source)
00005C32	E760 5030 080E		00005BF0	4042+	VST	V22,V10101	save v1 output
00005C38	07FB			4043+	BR	R11	return
00005C3C				4044+RE101	DC	0F	xl16 expected result
00005C3C				4045+	DROP	R5	
00005C3C	00020001 000006C0			4046	DC	XL16'00020001000006C0 000000030000F426'	result
00005C44	00000003 0000F426						
00005C4C	FF0000FF 00000029			4047	DC	XL16'FF0000FF00000029 00000038000000FA'	v2
00005C54	00000038 000000FA						
00005C5C	FF000001 00000029			4048	DC	XL16'FF00000100000029 00000038000000FA'	v3
00005C64	00000038 000000FA						
00005C6C	00020001 0000002F			4049	DC	XL16'000200010000002F 0000000300000002'	v4
00005C74	00000003 00000002						
				4050			
00005C80				4051	VRR_D	VMALO,2	
00005C80				4052+	DS	0FD	
00005C80		00005C80		4053+	USING	*,R5	base for test data and test routine
00005C80	00005CC8			4054+T102	DC	A(X102)	address of test routine
00005C84	0066			4055+	DC	H'102'	test number
00005C86	00			4056+	DC	X'00'	
00005C87	02			4057+	DC	HL1'2'	m5
00005C88	E5D4C1D3 D6404040			4058+	DC	CL8'VMALO'	instruction name
00005C90	00005D0C			4059+	DC	A(RE102+16)	address of v2 source
00005C94	00005D1C			4060+	DC	A(RE102+32)	address of v3 source
00005C98	00005D2C			4061+	DC	A(RE102+48)	address of v4 source
00005C9C	00000010			4062+	DC	A(16)	result length
00005CA0	00005CFC			4063+REA102	DC	A(RE102)	result address
00005CA8	00000000 00000000			4064+	DS	FD	gap
00005CB0	00000000 00000000			4065+V10102	DS	XL16	V1 output
00005CB8	00000000 00000000						
00005CC0	00000000 00000000			4066+	DS	FD	gap
				4067+*			
00005CC8				4068+X102	DS	0F	
00005CC8	E310 5010 0014		00000010	4069+	LGF	R1,V2ADDR	load v2 source
00005CCE	E761 0000 0806		00000000	4070+	VL	v22,0(R1)	use v22 to test decoder
00005CD4	E310 5014 0014		00000014	4071+	LGF	R1,V3ADDR	load v3 source
00005CDA	E771 0000 0806		00000000	4072+	VL	v23,0(R1)	use v23 to test decoder
00005CE0	E310 5018 0014		00000018	4073+	LGF	R1,V4ADDR	load v4 source
00005CE6	E781 0000 0806		00000000	4074+	VL	v24,0(R1)	use v24 to test decoder
00005CEC	E766 7200 8FAD			4075+	VMALO	V22,V22,V23,V24,2	test instruction (dest is a source)
00005CF2	E760 5030 080E		00005CB0	4076+	VST	V22,V10102	save v1 output
00005CF8	07FB			4077+	BR	R11	return
00005CFC				4078+RE102	DC	0F	xl16 expected result
00005CFC				4079+	DROP	R5	
00005CFC	FF1B3F6E A9977748			4080	DC	XL16'FF1B3F6EA9977748 09B4795953B0F010'	result
00005D04	09B47959 53B0F010						
00005D0C	FF020304 05060708			4081	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00005D14	090A0B0C 0D0E0F10						
00005D1C	FF020304 05060708			4082	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3
00005D24	090A0B0C 0D0E0F10						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005D2C	FF020304 05060708			4083	DC	XL16'FF02030405060708 090A0B0C0D0E0F10' v4	
00005D34	090A0B0C 0D0E0F10						
				4084			
				4085	VRR_D	VMALO,2	
00005D40				4086+	DS	0FD	
00005D40		00005D40		4087+	USING	*,R5	base for test data and test routine
00005D40	00005D88			4088+T103	DC	A(X103)	address of test routine
00005D44	0067			4089+	DC	H'103'	test number
00005D46	00			4090+	DC	X'00'	
00005D47	02			4091+	DC	HL1'2'	m5
00005D48	E5D4C1D3 D6404040			4092+	DC	CL8'VMALO'	instruction name
00005D50	00005DCC			4093+	DC	A(RE103+16)	address of v2 source
00005D54	00005DDC			4094+	DC	A(RE103+32)	address of v3 source
00005D58	00005DEC			4095+	DC	A(RE103+48)	address of v4 source
00005D5C	00000010			4096+	DC	A(16)	result length
00005D60	00005DBC			4097+REA103	DC	A(RE103)	result address
00005D68	00000000 00000000			4098+	DS	FD	gap
00005D70	00000000 00000000			4099+V10103	DS	XL16	V1 output
00005D78	00000000 00000000						
00005D80	00000000 00000000			4100+	DS	FD	gap
				4101+*			
00005D88				4102+X103	DS	0F	
00005D88	E310 5010 0014		00000010	4103+	LGF	R1,V2ADDR	load v2 source
00005D8E	E761 0000 0806		00000000	4104+	VL	v22,0(R1)	use v22 to test decoder
00005D94	E310 5014 0014		00000014	4105+	LGF	R1,V3ADDR	load v3 source
00005D9A	E771 0000 0806		00000000	4106+	VL	v23,0(R1)	use v23 to test decoder
00005DA0	E310 5018 0014		00000018	4107+	LGF	R1,V4ADDR	load v4 source
00005DA6	E781 0000 0806		00000000	4108+	VL	v24,0(R1)	use v24 to test decoder
00005DAC	E766 7200 8FAD			4109+	VMALO	V22,V22,V23,V24,2	test instruction (dest is a source)
00005DB2	E760 5030 080E		00005D70	4110+	VST	V22,V10103	save v1 output
00005DB8	07FB			4111+	BR	R11	return
00005DBC				4112+RE103	DC	0F	xl16 expected result
00005DBC				4113+	DROP	R5	
00005DBC	FF0C1E33 504B3B28			4114	DC	XL16'FF0C1E33504B3B28 0958BB24A157F790' result	
00005DC4	0958BB24 A157F790						
00005DCC	FF020304 05060708			4115	DC	XL16'FF02030405060708 090A0B0C0D0E0F10' v2	
00005DD4	090A0B0C 0D0E0F10						
00005DDC	FF010102 02030304			4116	DC	XL16'FF01010202030304 0405050606070708' v3	
00005DE4	04050506 06070708						
00005DEC	FF020304 05060708			4117	DC	XL16'FF02030405060708 090A0B0C0D0E0F10' v4	
00005DF4	090A0B0C 0D0E0F10						
				4118			
				4119	VRR_D	VMALO,2	
00005E00				4120+	DS	0FD	
00005E00		00005E00		4121+	USING	*,R5	base for test data and test routine
00005E00	00005E48			4122+T104	DC	A(X104)	address of test routine
00005E04	0068			4123+	DC	H'104'	test number
00005E06	00			4124+	DC	X'00'	
00005E07	02			4125+	DC	HL1'2'	m5
00005E08	E5D4C1D3 D6404040			4126+	DC	CL8'VMALO'	instruction name
00005E10	00005E8C			4127+	DC	A(RE104+16)	address of v2 source
00005E14	00005E9C			4128+	DC	A(RE104+32)	address of v3 source
00005E18	00005EAC			4129+	DC	A(RE104+48)	address of v4 source
00005E1C	00000010			4130+	DC	A(16)	result length
00005E20	00005E7C			4131+REA104	DC	A(RE104)	result address
00005E28	00000000 00000000			4132+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005E30	00000000 00000000			4133+V10104	DS	XL16	V1 output
00005E38	00000000 00000000						
00005E40	00000000 00000000			4134+	DS	FD	gap
				4135+*			
00005E48				4136+X104	DS	0F	
00005E48	E310 5010 0014		00000010	4137+	LGF	R1,V2ADDR	load v2 source
00005E4E	E761 0000 0806		00000000	4138+	VL	v22,0(R1)	use v22 to test decoder
00005E54	E310 5014 0014		00000014	4139+	LGF	R1,V3ADDR	load v3 source
00005E5A	E771 0000 0806		00000000	4140+	VL	v23,0(R1)	use v23 to test decoder
00005E60	E310 5018 0014		00000018	4141+	LGF	R1,V4ADDR	load v4 source
00005E66	E781 0000 0806		00000000	4142+	VL	v24,0(R1)	use v24 to test decoder
00005E6C	E766 7200 8FAD			4143+	VMALO	V22,V22,V23,V24,2	test instruction (dest is a source)
00005E72	E760 5030 080E		00005E30	4144+	VST	V22,V10104	save v1 output
00005E78	07FB			4145+	BR	R11	return
00005E7C				4146+RE104	DC	0F	xl16 expected result
00005E7C				4147+	DROP	R5	
00005E7C	FF020304 0A0C0E10			4148	DC	XL16'FF0203040A0C0E10 09172636544493D30'	result
00005E84	09172636 54493D30						
00005E8C	FF020304 05060708			4149	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00005E94	090A0B0C 0D0E0F10						
00005E9C	FF000000 00000001			4150	DC	XL16'FF00000000000001 0101010101010102'	v3
00005EA4	01010101 01010102						
00005EAC	FF020304 05060708			4151	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00005EB4	090A0B0C 0D0E0F10						
				4152			
				4153 * Doubleword			
				4154	VRR_D	VMAL0,3	
00005EC0				4155+	DS	0FD	
00005EC0		00005EC0		4156+	USING	*,R5	base for test data and test routine
00005EC0	00005F08			4157+T105	DC	A(X105)	address of test routine
00005EC4	0069			4158+	DC	H'105'	test number
00005EC6	00			4159+	DC	X'00'	
00005EC7	03			4160+	DC	HL1'3'	m5
00005EC8	E5D4C1D3 D6404040			4161+	DC	CL8'VMAL0'	instruction name
00005ED0	00005F4C			4162+	DC	A(RE105+16)	address of v2 source
00005ED4	00005F5C			4163+	DC	A(RE105+32)	address of v3 source
00005ED8	00005F6C			4164+	DC	A(RE105+48)	address of v4 source
00005EDC	00000010			4165+	DC	A(16)	result length
00005EE0	00005F3C			4166+REA105	DC	A(RE105)	result address
00005EE8	00000000 00000000			4167+	DS	FD	gap
00005EF0	00000000 00000000			4168+V10105	DS	XL16	V1 output
00005EF8	00000000 00000000						
00005F00	00000000 00000000			4169+	DS	FD	gap
				4170+*			
00005F08				4171+X105	DS	0F	
00005F08	E310 5010 0014		00000010	4172+	LGF	R1,V2ADDR	load v2 source
00005F0E	E761 0000 0806		00000000	4173+	VL	v22,0(R1)	use v22 to test decoder
00005F14	E310 5014 0014		00000014	4174+	LGF	R1,V3ADDR	load v3 source
00005F1A	E771 0000 0806		00000000	4175+	VL	v23,0(R1)	use v23 to test decoder
00005F20	E310 5018 0014		00000018	4176+	LGF	R1,V4ADDR	load v4 source
00005F26	E781 0000 0806		00000000	4177+	VL	v24,0(R1)	use v24 to test decoder
00005F2C	E766 7300 8FAD			4178+	VMALO	V22,V22,V23,V24,3	test instruction (dest is a source)
00005F32	E760 5030 080E		00005EF0	4179+	VST	V22,V10105	save v1 output
00005F38	07FB			4180+	BR	R11	return
00005F3C				4181+RE105	DC	0F	xl16 expected result
00005F3C				4182+	DROP	R5	

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  LOC        OBJECT CODE      ADDR1    ADDR2     STMT

00005F3C  00000000 00000C77                      4183         DC      XL16'0000000000000C77 96789F9F4FEDCC24'      result
00005F44  96789F9F 4FEDCC24
00005F4C  FFFFFFFF 00019000                      4184         DC      XL16'FFFFFFFF00019000 00000038EEEEEEFA'      v2
00005F54  00000038 EEEEEEFA
00005F5C  FFFFFFFF 00019000                      4185         DC      XL16'FFFFFFFF00019000 000000380EEEEEFA'      v3
00005F64  00000038 0EEEEEFA
00005F6C  00000000 00000000                      4186         DC      XL16'0000000000000000 0000000000000000'      v4
00005F74  00000000 00000000
                                                 4187
                                                 4188         VRR_D   VMALO,3
00005F80                                         4189+        DS      0FD
00005F80                      00005F80           4190+        USING   *,R5                      base for test data and test routine
00005F80  00005FC8                               4191+T106    DC      A(X106)                   address of test routine
00005F84  006A                                   4192+        DC      H'106'                    test number
00005F86  00                                     4193+        DC      X'00'
00005F87  03                                     4194+        DC      HL1'3'                    m5
00005F88  E5D4C1D3 D6404040                       4195+        DC      CL8'VMALO'                instruction name
00005F90  0000600C                               4196+        DC      A(RE106+16)               address of v2 source
00005F94  0000601C                               4197+        DC      A(RE106+32)               address of v3 source
00005F98  0000602C                               4198+        DC      A(RE106+48)               address of v4 source
00005F9C  00000010                               4199+        DC      A(16)                     result length
00005FA0  00005FFC                               4200+REA106  DC      A(RE106)                  result address
00005FA8  00000000 00000000                      4201+        DS      FD                        gap
00005FB0  00000000 00000000                      4202+V10106  DS      XL16                      V1 output
00005FB8  00000000 00000000
00005FC0  00000000 00000000                      4203+        DS      FD                        gap
                                                 4204+*
00005FC8                                         4205+X106    DS      0F
00005FC8  E310 5010 0014               00000010  4206+        LGF     R1,V2ADDR                 load v2 source
00005FCE  E761 0000 0806               00000000  4207+        VL      v22,0(R1)                 use v22 to test decoder
00005FD4  E310 5014 0014               00000014  4208+        LGF     R1,V3ADDR                 load v3 source
00005FDA  E771 0000 0806               00000000  4209+        VL      v23,0(R1)                 use v23 to test decoder
00005FE0  E310 5018 0014               00000018  4210+        LGF     R1,V4ADDR                 load v4 source
00005FE6  E781 0000 0806               00000000  4211+        VL      v24,0(R1)                 use v24 to test decoder
00005FEC  E766 7300 8FAD                         4212+        VMALO   V22,V22,V23,V24,3         test instruction (dest is a source)
00005FF2  E760 5030 080E               00005FB0  4213+        VST     V22,V10106                save v1 output
00005FF8  07FB                                   4214+        BR      R11                       return
00005FFC                                         4215+RE106   DC      0F                        xl16 expected result
00005FFC                                         4216+        DROP    R5
00005FFC  1051B52F 8692B4F7                      4217         DC      XL16'1051B52F8692B4F7 252B55D498D42102'      result
00006004  252B55D4 98D42102
0000600C  FF020304 05060750                      4218         DC      XL16'FF02030405060750 090A0B0C0D0E0F7F'      v2
00006014  090A0B0C 0D0E0F7F
0000601C  01020304 05060750                      4219         DC      XL16'0102030405060750 090A0B780D0E0F7F'      v3
00006024  090A0B78 0D0E0F7F
0000602C  10000000 00000001                      4220         DC      XL16'1000000000000001 1000000000000001'      v4
00006034  10000000 00000001
                                                 4221
                                                 4222         VRR_D   VMALO,3
00006040                                         4223+        DS      0FD
00006040                      00006040           4224+        USING   *,R5                      base for test data and test routine
00006040  00006088                               4225+T107    DC      A(X107)                   address of test routine
00006044  006B                                   4226+        DC      H'107'                    test number
00006046  00                                     4227+        DC      X'00'
00006047  03                                     4228+        DC      HL1'3'                    m5
00006048  E5D4C1D3 D6404040                       4229+        DC      CL8'VMALO'                instruction name
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00006050	000060CC			4230+	DC	A(RE107+16)	address of v2 source	
00006054	000060DC			4231+	DC	A(RE107+32)	address of v3 source	
00006058	000060EC			4232+	DC	A(RE107+48)	address of v4 source	
0000605C	00000010			4233+	DC	A(16)	result length	
00006060	000060BC			4234+REA107	DC	A(RE107)	result address	
00006068	00000000 00000000			4235+	DS	FD	gap	
00006070	00000000 00000000			4236+V10107	DS	XL16	V1 output	
00006078	00000000 00000000							
00006080	00000000 00000000			4237+	DS	FD	gap	
				4238+*				
00006088				4239+X107	DS	0F		
00006088	E310 5010 0014		00000010	4240+	LGF	R1,V2ADDR	load v2 source	
0000608E	E761 0000 0806		00000000	4241+	VL	v22,0(R1)	use v22 to test decoder	
00006094	E310 5014 0014		00000014	4242+	LGF	R1,V3ADDR	load v3 source	
0000609A	E771 0000 0806		00000000	4243+	VL	v23,0(R1)	use v23 to test decoder	
000060A0	E310 5018 0014		00000018	4244+	LGF	R1,V4ADDR	load v4 source	
000060A6	E781 0000 0806		00000000	4245+	VL	v24,0(R1)	use v24 to test decoder	
000060AC	E766 7300 8FAD			4246+	VMALO	V22,V22,V23,V24,3	test instruction (dest is a source)	
000060B2	E760 5030 080E		00006070	4247+	VST	V22,V10107	save v1 output	
000060B8	07FB			4248+	BR	R11	return	
000060BC				4249+RE107	DC	0F	xl16 expected result	
000060BC				4250+	DROP	R5		
000060BC	F024558D B838C872			4251	DC	XL16'F024558DB838C872 A47CD8D5FF5B4950'	result	
000060C4	A47CD8D5 FF5B4950							
000060CC	FF020304 05060750			4252	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2	
000060D4	090A0B0C 0D0E0F7F							
000060DC	00010102 02030328			4253	DC	XL16'0001010202030328 0405053C0607073F'	v3	
000060E4	0405053C 0607073F							
000060EC	F0000000 0000000F			4254	DC	XL16'F0000000000000000F F0000000000000000F'	v4	
000060F4	F0000000 0000000F							
				4255				
				4256	VRR_D	VMALO,3		
00006100				4257+	DS	0FD		
00006100		00006100		4258+	USING	*,R5	base for test data and test routine	
00006100	00006148			4259+T108	DC	A(X108)	address of test routine	
00006104	006C			4260+	DC	H'108'	test number	
00006106	00			4261+	DC	X'00'		
00006107	03			4262+	DC	HL1'3'	m5	
00006108	E5D4C1D3 D6404040			4263+	DC	CL8'VMALO'	instruction name	
00006110	0000618C			4264+	DC	A(RE108+16)	address of v2 source	
00006114	0000619C			4265+	DC	A(RE108+32)	address of v3 source	
00006118	000061AC			4266+	DC	A(RE108+48)	address of v4 source	
0000611C	00000010			4267+	DC	A(16)	result length	
00006120	0000617C			4268+REA108	DC	A(RE108)	result address	
00006128	00000000 00000000			4269+	DS	FD	gap	
00006130	00000000 00000000			4270+V10108	DS	XL16	V1 output	
00006138	00000000 00000000							
00006140	00000000 00000000			4271+	DS	FD	gap	
				4272+*				
00006148				4273+X108	DS	0F		
00006148	E310 5010 0014		00000010	4274+	LGF	R1,V2ADDR	load v2 source	
0000614E	E761 0000 0806		00000000	4275+	VL	v22,0(R1)	use v22 to test decoder	
00006154	E310 5014 0014		00000014	4276+	LGF	R1,V3ADDR	load v3 source	
0000615A	E771 0000 0806		00000000	4277+	VL	v23,0(R1)	use v23 to test decoder	
00006160	E310 5018 0014		00000018	4278+	LGF	R1,V4ADDR	load v4 source	
00006166	E781 0000 0806		00000000	4279+	VL	v24,0(R1)	use v24 to test decoder	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000616C	E766 7300 8FAD			4280+	VMALO	V22,V22,V23,V24,3	test instruction (dest is a source)
00006172	E760 5030 080E		00006130	4281+	VST	V22,V10108	save v1 output
00006178	07FB			4282+	BR	R11	return
0000617C				4283+RE108	DC	0F	xl16 expected result
0000617C				4284+	DROP	R5	
0000617C	DD09131E A8C3DFFE			4285	DC	XL16'DD09131EA8C3DFFE D91C345D6D616771'	result
00006184	D91C345D 6D616771						
0000618C	FF020304 05060750			4286	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00006194	090A0B0C 0D0E0F7F						
0000619C	00000000 0000000A			4287	DC	XL16'000000000000000A 0101010F0101010F'	v3
000061A4	0101010F 0101010F						
000061AC	DD000000 00000000			4288	DC	XL16'DD00000000000000 D000000D0D000000'	v4
000061B4	D000000D 0D000000						
				4289			
				4290	VRR_D	VMALO,3	
000061C0				4291+	DS	0FD	
000061C0		000061C0		4292+	USING	*,R5	base for test data and test routine
000061C0	00006208			4293+T109	DC	A(X109)	address of test routine
000061C4	006D			4294+	DC	H'109'	test number
000061C6	00			4295+	DC	X'00'	
000061C7	03			4296+	DC	HL1'3'	m5
000061C8	E5D4C1D3 D6404040			4297+	DC	CL8'VMALO'	instruction name
000061D0	0000624C			4298+	DC	A(RE109+16)	address of v2 source
000061D4	0000625C			4299+	DC	A(RE109+32)	address of v3 source
000061D8	0000626C			4300+	DC	A(RE109+48)	address of v4 source
000061DC	00000010			4301+	DC	A(16)	result length
000061E0	0000623C			4302+REA109	DC	A(RE109)	result address
000061E8	00000000 00000000			4303+	DS	FD	gap
000061F0	00000000 00000000			4304+V10109	DS	XL16	V1 output
000061F8	00000000 00000000						
00006200	00000000 00000000			4305+	DS	FD	gap
				4306+*			
00006208				4307+X109	DS	0F	
00006208	E310 5010 0014		00000010	4308+	LGF	R1,V2ADDR	load v2 source
0000620E	E761 0000 0806		00000000	4309+	VL	v22,0(R1)	use v22 to test decoder
00006214	E310 5014 0014		00000014	4310+	LGF	R1,V3ADDR	load v3 source
0000621A	E771 0000 0806		00000000	4311+	VL	v23,0(R1)	use v23 to test decoder
00006220	E310 5018 0014		00000018	4312+	LGF	R1,V4ADDR	load v4 source
00006226	E781 0000 0806		00000000	4313+	VL	v24,0(R1)	use v24 to test decoder
0000622C	E766 7300 8FAD			4314+	VMALO	V22,V22,V23,V24,3	test instruction (dest is a source)
00006232	E760 5030 080E		000061F0	4315+	VST	V22,V10109	save v1 output
00006238	07FB			4316+	BR	R11	return
0000623C				4317+RE109	DC	0F	xl16 expected result
0000623C				4318+	DROP	R5	
0000623C	FED00000 00000009			4319	DC	XL16'FED0000000000009 F6141E28323C492C'	result
00006244	F6141E28 323C492C						
0000624C	090A0B0C 0D0E0F7F			4320	DC	XL16'090A0B0C0D0E0F7F FF02030405060750'	v2
00006254	FF020304 05060750						
0000625C	0101010F 0101010F			4321	DC	XL16'0101010F0101010F 000000000000000A'	v3
00006264	00000000 0000000A						
0000626C	FED00000 00000000			4322	DC	XL16'FED0000000000000 000000000000000C'	v4
00006274	00000000 0000000C						
				4323			
				4324	*---		
				4325	* VMAE	- Vector Multiply and Add Even	
				4326	*---		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				4327	* Byte		
				4328		VRR_D VMAE,0	
00006280				4329+	DS	0FD	
00006280		00006280		4330+	USING	*,R5	base for test data and test routine
00006280	000062C8			4331+T110	DC	A(X110)	address of test routine
00006284	006E			4332+	DC	H'110'	test number
00006286	00			4333+	DC	X'00'	
00006287	00			4334+	DC	HL1'0'	m5
00006288	E5D4C1C5 40404040			4335+	DC	CL8'VMAE'	instruction name
00006290	0000630C			4336+	DC	A(RE110+16)	address of v2 source
00006294	0000631C			4337+	DC	A(RE110+32)	address of v3 source
00006298	0000632C			4338+	DC	A(RE110+48)	address of v4 source
0000629C	00000010			4339+	DC	A(16)	result length
000062A0	000062FC			4340+REA110	DC	A(RE110)	result address
000062A8	00000000 00000000			4341+	DS	FD	gap
000062B0	00000000 00000000			4342+V10110	DS	XL16	V1 output
000062B8	00000000 00000000						
000062C0	00000000 00000000			4343+	DS	FD	gap
				4344+*			
000062C8				4345+X110	DS	0F	
000062C8	E310 5010 0014		00000010	4346+	LGF	R1,V2ADDR	load v2 source
000062CE	E761 0000 0806		00000000	4347+	VL	v22,0(R1)	use v22 to test decoder
000062D4	E310 5014 0014		00000014	4348+	LGF	R1,V3ADDR	load v3 source
000062DA	E771 0000 0806		00000000	4349+	VL	v23,0(R1)	use v23 to test decoder
000062E0	E310 5018 0014		00000018	4350+	LGF	R1,V4ADDR	load v4 source
000062E6	E781 0000 0806		00000000	4351+	VL	v24,0(R1)	use v24 to test decoder
000062EC	E766 7000 8FAE			4352+	VMAE	V22,V22,V23,V24,0	test instruction (dest is a source)
000062F2	E760 5030 080E		000062B0	4353+	VST	V22,V10110	save v1 output
000062F8	07FB			4354+	BR	R11	return
000062FC				4355+RE110	DC	0F	xl16 expected result
000062FC				4356+	DROP	R5	
000062FC	00010000 00000000			4357	DC	XL16'0001000000000000 0000000000000000'	result
00006304	00000000 00000000						
0000630C	FF000000 00000019			4358	DC	XL16'FF00000000000019 00000038000000FA'	v2
00006314	00000038 000000FA						
0000631C	FF000000 00000019			4359	DC	XL16'FF00000000000019 00000038000000FA'	v3
00006324	00000038 000000FA						
0000632C	00000000 00000000			4360	DC	XL16'0000000000000000 0000000000000000'	v4
00006334	00000000 00000000						
				4361			
				4362		VRR_D VMAE,0	
00006340				4363+	DS	0FD	
00006340		00006340		4364+	USING	*,R5	base for test data and test routine
00006340	00006388			4365+T111	DC	A(X111)	address of test routine
00006344	006F			4366+	DC	H'111'	test number
00006346	00			4367+	DC	X'00'	
00006347	00			4368+	DC	HL1'0'	m5
00006348	E5D4C1C5 40404040			4369+	DC	CL8'VMAE'	instruction name
00006350	000063CC			4370+	DC	A(RE111+16)	address of v2 source
00006354	000063DC			4371+	DC	A(RE111+32)	address of v3 source
00006358	000063EC			4372+	DC	A(RE111+48)	address of v4 source
0000635C	00000010			4373+	DC	A(16)	result length
00006360	000063BC			4374+REA111	DC	A(RE111)	result address
00006368	00000000 00000000			4375+	DS	FD	gap
00006370	00000000 00000000			4376+V10111	DS	XL16	V1 output
00006378	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006380	00000000 00000000			4377+	DS	FD	gap
				4378+*			
00006388				4379+X111	DS	0F	
00006388	E310 5010 0014		00000010	4380+	LGF	R1,V2ADDR	load v2 source
0000638E	E761 0000 0806		00000000	4381+	VL	v22,0(R1)	use v22 to test decoder
00006394	E310 5014 0014		00000014	4382+	LGF	R1,V3ADDR	load v3 source
0000639A	E771 0000 0806		00000000	4383+	VL	v23,0(R1)	use v23 to test decoder
000063A0	E310 5018 0014		00000018	4384+	LGF	R1,V4ADDR	load v4 source
000063A6	E781 0000 0806		00000000	4385+	VL	v24,0(R1)	use v24 to test decoder
000063AC	E766 7000 8FAE			4386+	VMAE	V22,V22,V23,V24,0	test instruction (dest is a source)
000063B2	E760 5030 080E		00006370	4387+	VST	V22,V10111	save v1 output
000063B8	07FB			4388+	BR	R11	return
000063BC				4389+RE111	DC	0F	xl16 expected result
000063BC				4390+	DROP	R5	
000063BC	00030001 0000002F			4391	DC	XL16'000300010000002F 0000000300000002'	result
000063C4	00000003 00000002						
000063CC	FF0000FF 00000029			4392	DC	XL16'FF0000FF00000029 00000038000000FA'	v2
000063D4	00000038 000000FA						
000063DC	FF000001 00000029			4393	DC	XL16'FF00000100000029 00000038000000FA'	v3
000063E4	00000038 000000FA						
000063EC	00020001 0000002F			4394	DC	XL16'000200010000002F 0000000300000002'	v4
000063F4	00000003 00000002						
				4395			
				4396	VRR_D	VMAE,0	
00006400				4397+	DS	0FD	
00006400		00006400		4398+	USING	*,R5	base for test data and test routine
00006400	00006448			4399+T112	DC	A(X112)	address of test routine
00006404	0070			4400+	DC	H'112'	test number
00006406	00			4401+	DC	X'00'	
00006407	00			4402+	DC	HL1'0'	m5
00006408	E5D4C1C5 40404040			4403+	DC	CL8'VMAE'	instruction name
00006410	0000648C			4404+	DC	A(RE112+16)	address of v2 source
00006414	0000649C			4405+	DC	A(RE112+32)	address of v3 source
00006418	000064AC			4406+	DC	A(RE112+48)	address of v4 source
0000641C	00000010			4407+	DC	A(16)	result length
00006420	0000647C			4408+REA112	DC	A(RE112)	result address
00006428	00000000 00000000			4409+	DS	FD	gap
00006430	00000000 00000000			4410+V10112	DS	XL16	V1 output
00006438	00000000 00000000						
00006440	00000000 00000000			4411+	DS	FD	gap
				4412+*			
00006448				4413+X112	DS	0F	
00006448	E310 5010 0014		00000010	4414+	LGF	R1,V2ADDR	load v2 source
0000644E	E761 0000 0806		00000000	4415+	VL	v22,0(R1)	use v22 to test decoder
00006454	E310 5014 0014		00000014	4416+	LGF	R1,V3ADDR	load v3 source
0000645A	E771 0000 0806		00000000	4417+	VL	v23,0(R1)	use v23 to test decoder
00006460	E310 5018 0014		00000018	4418+	LGF	R1,V4ADDR	load v4 source
00006466	E781 0000 0806		00000000	4419+	VL	v24,0(R1)	use v24 to test decoder
0000646C	E766 7000 8FAE			4420+	VMAE	V22,V22,V23,V24,0	test instruction (dest is a source)
00006472	E760 5030 080E		00006430	4421+	VST	V22,V10112	save v1 output
00006478	07FB			4422+	BR	R11	return
0000647C				4423+RE112	DC	0F	xl16 expected result
0000647C				4424+	DROP	R5	
0000647C	FF03030D 051F0739			4425	DC	XL16'FF03030D051F0739 095B0B850DB70FF1'	result
00006484	095B0B85 0DB70FF1						
0000648C	FF020304 05060708			4426	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00006494  090A0B0C 0D0E0F10
0000649C  FF020304 05060708              4427          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v3
000064A4  090A0B0C 0D0E0F10
000064AC  FF020304 05060708              4428          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v4
000064B4  090A0B0C 0D0E0F10
                                         4429
                                         4430          VRR_D VMAE,0
000064C0                                 4431+         DS    0FD
000064C0                      000064C0   4432+         USING *,R5                   base for test data and test routine
000064C0  00006508                       4433+T113     DC    A(X113)                address of test routine
000064C4  0071                           4434+         DC    H'113'                 test number
000064C6  00                             4435+         DC    X'00'
000064C7  00                             4436+         DC    HL1'0'                 m5
000064C8  E5D4C1C5 40404040              4437+         DC    CL8'VMAE'              instruction name
000064D0  0000654C                       4438+         DC    A(RE113+16)            address of v2 source
000064D4  0000655C                       4439+         DC    A(RE113+32)            address of v3 source
000064D8  0000656C                       4440+         DC    A(RE113+48)            address of v4 source
000064DC  00000010                       4441+         DC    A(16)                  result length
000064E0  0000653C                       4442+REA113   DC    A(RE113)               result address
000064E8  00000000 00000000              4443+         DS    FD                     gap
000064F0  00000000 00000000              4444+V10113   DS    XL16                   V1 output
000064F8  00000000 00000000
00006500  00000000 00000000              4445+         DS    FD                     gap
                                         4446+*
00006508                                 4447+X113     DS    0F
00006508  E310 5010 0014      00000010   4448+         LGF   R1,V2ADDR              load v2 source
0000650E  E761 0000 0806      00000000   4449+         VL    v22,0(R1)              use v22 to test decoder
00006514  E310 5014 0014      00000014   4450+         LGF   R1,V3ADDR              load v3 source
0000651A  E771 0000 0806      00000000   4451+         VL    v23,0(R1)              use v23 to test decoder
00006520  E310 5018 0014      00000018   4452+         LGF   R1,V4ADDR              load v4 source
00006526  E781 0000 0806      00000000   4453+         VL    v24,0(R1)              use v24 to test decoder
0000652C  E766 7000 8FAE                 4454+         VMAE  V22,V22,V23,V24,0    test instruction (dest is a source)
00006532  E760 5030 080E      000064F0   4455+         VST   V22,V10113             save v1 output
00006538  07FB                           4456+         BR    R11                    return
0000653C                                 4457+RE113    DC    0F                     xl16 expected result
0000653C                                 4458+         DROP  R5
0000653C  FF030307 0510071D              4459          DC    XL16'FF0303070510071D 092E0B430D5C0F79'     result
00006544  092E0B43 0D5C0F79
0000654C  FF020304 05060708              4460          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
00006554  090A0B0C 0D0E0F10
0000655C  FF010102 02030304              4461          DC    XL16'FF01010202030304 0405050606070708'     v3
00006564  04050506 06070708
0000656C  FF020304 05060708              4462          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v4
00006574  090A0B0C 0D0E0F10
                                         4463
                                         4464          VRR_D VMAE,0
00006580                                 4465+         DS    0FD
00006580                      00006580   4466+         USING *,R5                   base for test data and test routine
00006580  000065C8                       4467+T114     DC    A(X114)                address of test routine
00006584  0072                           4468+         DC    H'114'                 test number
00006586  00                             4469+         DC    X'00'
00006587  00                             4470+         DC    HL1'0'                 m5
00006588  E5D4C1C5 40404040              4471+         DC    CL8'VMAE'              instruction name
00006590  0000660C                       4472+         DC    A(RE114+16)            address of v2 source
00006594  0000661C                       4473+         DC    A(RE114+32)            address of v3 source
00006598  0000662C                       4474+         DC    A(RE114+48)            address of v4 source
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000659C	00000010			4475+	DC	A(16)	result length
000065A0	000065FC			4476+REA114	DC	A(RE114)	result address
000065A8	00000000 00000000			4477+	DS	FD	gap
000065B0	00000000 00000000			4478+V10114	DS	XL16	V1 output
000065B8	00000000 00000000						
000065C0	00000000 00000000			4479+	DS	FD	gap
				4480+*			
000065C8				4481+X114	DS	0F	
000065C8	E310 5010 0014		00000010	4482+	LGF	R1,V2ADDR	load v2 source
000065CE	E761 0000 0806		00000000	4483+	VL	v22,0(R1)	use v22 to test decoder
000065D4	E310 5014 0014		00000014	4484+	LGF	R1,V3ADDR	load v3 source
000065DA	E771 0000 0806		00000000	4485+	VL	v23,0(R1)	use v23 to test decoder
000065E0	E310 5018 0014		00000018	4486+	LGF	R1,V4ADDR	load v4 source
000065E6	E781 0000 0806		00000000	4487+	VL	v24,0(R1)	use v24 to test decoder
000065EC	E766 7000 8FAE			4488+	VMAE	V22,V22,V23,V24,0	test instruction (dest is a source)
000065F2	E760 5030 080E		000065B0	4489+	VST	V22,V10114	save v1 output
000065F8	07FB			4490+	BR	R11	return
000065FC				4491+RE114	DC	0F	xl16 expected result
000065FC				4492+	DROP	R5	
000065FC	FF030304 05060708			4493	DC	XL16'FF03030405060708 09130B170D1B0F1F'	result
00006604	09130B17 0D1B0F1F						
0000660C	FF020304 05060708			4494	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00006614	090A0B0C 0D0E0F10						
0000661C	FF000000 00000001			4495	DC	XL16'FF00000000000001 0101010101010102'	v3
00006624	01010101 01010102						
0000662C	FF020304 05060708			4496	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00006634	090A0B0C 0D0E0F10						
				4497			
				4498 * Halfword			
				4499	VRR_D	VMAE,1	
00006640				4500+	DS	0FD	
00006640		00006640		4501+	USING	*,R5	base for test data and test routine
00006640	00006688			4502+T115	DC	A(X115)	address of test routine
00006644	0073			4503+	DC	H'115'	test number
00006646	00			4504+	DC	X'00'	
00006647	01			4505+	DC	HL1'1'	m5
00006648	E5D4C1C5 40404040			4506+	DC	CL8'VMAE'	instruction name
00006650	000066CC			4507+	DC	A(RE115+16)	address of v2 source
00006654	000066DC			4508+	DC	A(RE115+32)	address of v3 source
00006658	000066EC			4509+	DC	A(RE115+48)	address of v4 source
0000665C	00000010			4510+	DC	A(16)	result length
00006660	000066BC			4511+REA115	DC	A(RE115)	result address
00006668	00000000 00000000			4512+	DS	FD	gap
00006670	00000000 00000000			4513+V10115	DS	XL16	V1 output
00006678	00000000 00000000						
00006680	00000000 00000000			4514+	DS	FD	gap
				4515+*			
00006688				4516+X115	DS	0F	
00006688	E310 5010 0014		00000010	4517+	LGF	R1,V2ADDR	load v2 source
0000668E	E761 0000 0806		00000000	4518+	VL	v22,0(R1)	use v22 to test decoder
00006694	E310 5014 0014		00000014	4519+	LGF	R1,V3ADDR	load v3 source
0000669A	E771 0000 0806		00000000	4520+	VL	v23,0(R1)	use v23 to test decoder
000066A0	E310 5018 0014		00000018	4521+	LGF	R1,V4ADDR	load v4 source
000066A6	E781 0000 0806		00000000	4522+	VL	v24,0(R1)	use v24 to test decoder
000066AC	E766 7100 8FAE			4523+	VMAE	V22,V22,V23,V24,1	test instruction (dest is a source)
000066B2	E760 5030 080E		00006670	4524+	VST	V22,V10115	save v1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000066B8	07FB			4525+	BR	R11		return
000066BC				4526+RE115	DC	0F		xl16 expected result
000066BC				4527+	DROP	R5		
000066BC	00010000 00000000			4528	DC	XL16'0001000000000000 0000000000000000'		result
000066C4	00000000 00000000							
000066CC	FF000000 00000019			4529	DC	XL16'FF00000000000019 00000038000000FA'		v2
000066D4	00000038 000000FA							
000066DC	FF000000 00000019			4530	DC	XL16'FF00000000000019 00000038000000FA'		v3
000066E4	00000038 000000FA							
000066EC	00000000 00000000			4531	DC	XL16'0000000000000000 0000000000000000'		v4
000066F4	00000000 00000000							
				4532				
				4533	VRR_D	VMAE, 1		
00006700				4534+	DS	0FD		
00006700		00006700		4535+	USING	*, R5		base for test data and test routine
00006700	00006748			4536+T116	DC	A(X116)		address of test routine
00006704	0074			4537+	DC	H'116'		test number
00006706	00			4538+	DC	X'00'		
00006707	01			4539+	DC	HL1'1'		m5
00006708	E5D4C1C5 40404040			4540+	DC	CL8'VMAE'		instruction name
00006710	0000678C			4541+	DC	A(RE116+16)		address of v2 source
00006714	0000679C			4542+	DC	A(RE116+32)		address of v3 source
00006718	000067AC			4543+	DC	A(RE116+48)		address of v4 source
0000671C	00000010			4544+	DC	A(16)		result length
00006720	0000677C			4545+REA116	DC	A(RE116)		result address
00006728	00000000 00000000			4546+	DS	FD		gap
00006730	00000000 00000000			4547+V10116	DS	XL16		V1 output
00006738	00000000 00000000							
00006740	00000000 00000000			4548+	DS	FD		gap
				4549+*				
00006748				4550+X116	DS	0F		
00006748	E310 5010 0014		00000010	4551+	LGF	R1, V2ADDR		load v2 source
0000674E	E761 0000 0806		00000000	4552+	VL	v22, 0(R1)		use v22 to test decoder
00006754	E310 5014 0014		00000014	4553+	LGF	R1, V3ADDR		load v3 source
0000675A	E771 0000 0806		00000000	4554+	VL	v23, 0(R1)		use v23 to test decoder
00006760	E310 5018 0014		00000018	4555+	LGF	R1, V4ADDR		load v4 source
00006766	E781 0000 0806		00000000	4556+	VL	v24, 0(R1)		use v24 to test decoder
0000676C	E766 7100 8FAE			4557+	VMAE	V22, V22, V23, V24, 1		test instruction (dest is a source)
00006772	E760 5030 080E		00006730	4558+	VST	V22, V10116		save v1 output
00006778	07FB			4559+	BR	R11		return
0000677C				4560+RE116	DC	0F		xl16 expected result
0000677C				4561+	DROP	R5		
0000677C	00030001 0000002F			4562	DC	XL16'000300010000002F 0000000300000002'		result
00006784	00000003 00000002							
0000678C	FF0000FF 00000029			4563	DC	XL16'FF0000FF00000029 00000038000000FA'		v2
00006794	00000038 000000FA							
0000679C	FF000001 00000029			4564	DC	XL16'FF00000100000029 00000038000000FA'		v3
000067A4	00000038 000000FA							
000067AC	00020001 0000002F			4565	DC	XL16'000200010000002F 0000000300000002'		v4
000067B4	00000003 00000002							
				4566				
				4567	VRR_D	VMAE, 1		
000067C0				4568+	DS	0FD		
000067C0		000067C0		4569+	USING	*, R5		base for test data and test routine
000067C0	00006808			4570+T117	DC	A(X117)		address of test routine
000067C4	0075			4571+	DC	H'117'		test number

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

000067C6  00                                      4572+          DC    X'00'
000067C7  01                                      4573+          DC    HL1'1'              m5
000067C8  E5D4C1C5 40404040                        4574+          DC    CL8'VMAE'           instruction name
000067D0  0000684C                                 4575+          DC    A(RE117+16)         address of v2 source
000067D4  0000685C                                 4576+          DC    A(RE117+32)         address of v3 source
000067D8  0000686C                                 4577+          DC    A(RE117+48)         address of v4 source
000067DC  00000010                                 4578+          DC    A(16)               result length
000067E0  0000683C                                 4579+REA117    DC    A(RE117)            result address
000067E8  00000000 00000000                        4580+          DS    FD                  gap
000067F0  00000000 00000000                        4581+V10117    DS    XL16                V1 output
000067F8  00000000 00000000
00006800  00000000 00000000                        4582+          DS    FD                  gap
                                                   4583+*
00006808                                           4584+X117      DS    0F
00006808  E310 5010 0014                00000010   4585+          LGF   R1,V2ADDR           load v2 source
0000680E  E761 0000 0806                00000000   4586+          VL    v22,0(R1)           use v22 to test decoder
00006814  E310 5014 0014                00000014   4587+          LGF   R1,V3ADDR           load v3 source
0000681A  E771 0000 0806                00000000   4588+          VL    v23,0(R1)           use v23 to test decoder
00006820  E310 5018 0014                00000018   4589+          LGF   R1,V4ADDR           load v4 source
00006826  E781 0000 0806                00000000   4590+          VL    v24,0(R1)           use v24 to test decoder
0000682C  E766 7100 8FAE                           4591+          VMAE  V22,V22,V23,V24,1    test instruction (dest is a source)
00006832  E760 5030 080E                000067F0   4592+          VST   V22,V10117           save v1 output
00006838  07FB                                     4593+          BR    R11                 return
0000683C                                           4594+RE117     DC    0F                  xl16 expected result
0000683C                                           4595+          DROP  R5
0000683C  FF02FF08 051F432C                        4596           DC    XL16'FF02FF08051F432C 095BBF700DB87BD4'    result
00006844  095BBF70 0DB87BD4
0000684C  FF020304 05060708                        4597           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00006854  090A0B0C 0D0E0F10
0000685C  FF020304 05060708                        4598           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v3
00006864  090A0B0C 0D0E0F10
0000686C  FF020304 05060708                        4599           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00006874  090A0B0C 0D0E0F10
                                                   4600
                                                   4601           VRR_D VMAE,1
00006880                                           4602+          DS    0FD
00006880                      00006880             4603+          USING *,R5                base for test data and test routine
00006880  000068C8                                 4604+T118      DC    A(X118)             address of test routine
00006884  0076                                     4605+          DC    H'118'              test number
00006886  00                                       4606+          DC    X'00'
00006887  01                                       4607+          DC    HL1'1'              m5
00006888  E5D4C1C5 40404040                        4608+          DC    CL8'VMAE'           instruction name
00006890  0000690C                                 4609+          DC    A(RE118+16)         address of v2 source
00006894  0000691C                                 4610+          DC    A(RE118+32)         address of v3 source
00006898  0000692C                                 4611+          DC    A(RE118+48)         address of v4 source
0000689C  00000010                                 4612+          DC    A(16)               result length
000068A0  000068FC                                 4613+REA118    DC    A(RE118)            result address
000068A8  00000000 00000000                        4614+          DS    FD                  gap
000068B0  00000000 00000000                        4615+V10118    DS    XL16                V1 output
000068B8  00000000 00000000
000068C0  00000000 00000000                        4616+          DS    FD                  gap
                                                   4617+*
000068C8                                           4618+X118      DS    0F
000068C8  E310 5010 0014                00000010   4619+          LGF   R1,V2ADDR           load v2 source
000068CE  E761 0000 0806                00000000   4620+          VL    v22,0(R1)           use v22 to test decoder
000068D4  E310 5014 0014                00000014   4621+          LGF   R1,V3ADDR           load v3 source
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000068DA	E771 0000 0806		00000000	4622+	VL	v23,0(R1)	use v23 to test decoder
000068E0	E310 5018 0014		00000018	4623+	LGF	R1,V4ADDR	load v4 source
000068E6	E781 0000 0806		00000000	4624+	VL	v24,0(R1)	use v24 to test decoder
000068EC	E766 7100 8FAE			4625+	VMAE	V22,V22,V23,V24,1	test instruction (dest is a source)
000068F2	E760 5030 080E		000068B0	4626+	VST	V22,V10118	save v1 output
000068F8	07FB			4627+	BR	R11	return
000068FC				4628+RE118	DC	0F	xl16 expected result
000068FC				4629+	DROP	R5	
000068FC	FF030006 0510221A			4630	DC	XL16'FF0300060510221A 092E603E0D5CBE72'	result
00006904	092E603E 0D5CBE72						
0000690C	FF020304 05060708			4631	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00006914	090A0B0C 0D0E0F10						
0000691C	FF010102 02030304			4632	DC	XL16'FF01010202030304 0405050606070708'	v3
00006924	04050506 06070708						
0000692C	FF020304 05060708			4633	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00006934	090A0B0C 0D0E0F10						
				4634			
				4635	VRR_D	VMAE,1	
00006940				4636+	DS	0FD	
00006940		00006940		4637+	USING	*,R5	base for test data and test routine
00006940	00006988			4638+T119	DC	A(X119)	address of test routine
00006944	0077			4639+	DC	H'119'	test number
00006946	00			4640+	DC	X'00'	
00006947	01			4641+	DC	HL1'1'	m5
00006948	E5D4C1C5 40404040			4642+	DC	CL8'VMAE'	instruction name
00006950	000069CC			4643+	DC	A(RE119+16)	address of v2 source
00006954	000069DC			4644+	DC	A(RE119+32)	address of v3 source
00006958	000069EC			4645+	DC	A(RE119+48)	address of v4 source
0000695C	00000010			4646+	DC	A(16)	result length
00006960	000069BC			4647+REA119	DC	A(RE119)	result address
00006968	00000000 00000000			4648+	DS	FD	gap
00006970	00000000 00000000			4649+V10119	DS	XL16	V1 output
00006978	00000000 00000000						
00006980	00000000 00000000			4650+	DS	FD	gap
				4651+*			
00006988				4652+X119	DS	0F	
00006988	E310 5010 0014		00000010	4653+	LGF	R1,V2ADDR	load v2 source
0000698E	E761 0000 0806		00000000	4654+	VL	v22,0(R1)	use v22 to test decoder
00006994	E310 5014 0014		00000014	4655+	LGF	R1,V3ADDR	load v3 source
0000699A	E771 0000 0806		00000000	4656+	VL	v23,0(R1)	use v23 to test decoder
000069A0	E310 5018 0014		00000018	4657+	LGF	R1,V4ADDR	load v4 source
000069A6	E781 0000 0806		00000000	4658+	VL	v24,0(R1)	use v24 to test decoder
000069AC	E766 7100 8FAE			4659+	VMAE	V22,V22,V23,V24,1	test instruction (dest is a source)
000069B2	E760 5030 080E		00006970	4660+	VST	V22,V10119	save v1 output
000069B8	07FB			4661+	BR	R11	return
000069BC				4662+RE119	DC	0F	xl16 expected result
000069BC				4663+	DROP	R5	
000069BC	FF030104 05060708			4664	DC	XL16'FF03010405060708 09131E160D1B2A1E'	result
000069C4	09131E16 0D1B2A1E						
000069CC	FF020304 05060708			4665	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
000069D4	090A0B0C 0D0E0F10						
000069DC	FF000000 00000000			4666	DC	XL16'FF00000000000001 0101010101010102'	v3
000069E4	01010101 01010102						
000069EC	FF020304 05060708			4667	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
000069F4	090A0B0C 0D0E0F10						
				4668			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				4669	* Word		
				4670		VRR_D VMAE,2	
00006A00				4671+	DS	0FD	
00006A00		00006A00		4672+	USING	*,R5	base for test data and test routine
00006A00	00006A48			4673+T120	DC	A(X120)	address of test routine
00006A04	0078			4674+	DC	H'120'	test number
00006A06	00			4675+	DC	X'00'	
00006A07	02			4676+	DC	HL1'2'	m5
00006A08	E5D4C1C5 40404040			4677+	DC	CL8'VMAE'	instruction name
00006A10	00006A8C			4678+	DC	A(RE120+16)	address of v2 source
00006A14	00006A9C			4679+	DC	A(RE120+32)	address of v3 source
00006A18	00006AAC			4680+	DC	A(RE120+48)	address of v4 source
00006A1C	00000010			4681+	DC	A(16)	result length
00006A20	00006A7C			4682+REA120	DC	A(RE120)	result address
00006A28	00000000 00000000			4683+	DS	FD	gap
00006A30	00000000 00000000			4684+V10120	DS	XL16	V1 output
00006A38	00000000 00000000						
00006A40	00000000 00000000			4685+	DS	FD	gap
				4686+*			
00006A48				4687+X120	DS	0F	
00006A48	E310 5010 0014		00000010	4688+	LGF	R1,V2ADDR	load v2 source
00006A4E	E761 0000 0806		00000000	4689+	VL	v22,0(R1)	use v22 to test decoder
00006A54	E310 5014 0014		00000014	4690+	LGF	R1,V3ADDR	load v3 source
00006A5A	E771 0000 0806		00000000	4691+	VL	v23,0(R1)	use v23 to test decoder
00006A60	E310 5018 0014		00000018	4692+	LGF	R1,V4ADDR	load v4 source
00006A66	E781 0000 0806		00000000	4693+	VL	v24,0(R1)	use v24 to test decoder
00006A6C	E766 7200 8FAE			4694+	VMAE	V22,V22,V23,V24,2	test instruction (dest is a source)
00006A72	E760 5030 080E		00006A30	4695+	VST	V22,V10120	save v1 output
00006A78	07FB			4696+	BR	R11	return
00006A7C				4697+RE120	DC	0F	xl16 expected result
00006A7C				4698+	DROP	R5	
00006A7C	00010000 00000000			4699	DC	XL16'0001000000000000 0000000000000C40'	result
00006A84	00000000 00000C40						
00006A8C	FF000000 00000019			4700	DC	XL16'FF00000000000019 00000038000000FA'	v2
00006A94	00000038 000000FA						
00006A9C	FF000000 00000019			4701	DC	XL16'FF00000000000019 00000038000000FA'	v3
00006AA4	00000038 000000FA						
00006AAC	00000000 00000000			4702	DC	XL16'0000000000000000 0000000000000000'	v4
00006AB4	00000000 00000000						
				4703			
				4704		VRR_D VMAE,2	
00006AC0				4705+	DS	0FD	
00006AC0		00006AC0		4706+	USING	*,R5	base for test data and test routine
00006AC0	00006B08			4707+T121	DC	A(X121)	address of test routine
00006AC4	0079			4708+	DC	H'121'	test number
00006AC6	00			4709+	DC	X'00'	
00006AC7	02			4710+	DC	HL1'2'	m5
00006AC8	E5D4C1C5 40404040			4711+	DC	CL8'VMAE'	instruction name
00006AD0	00006B4C			4712+	DC	A(RE121+16)	address of v2 source
00006AD4	00006B5C			4713+	DC	A(RE121+32)	address of v3 source
00006AD8	00006B6C			4714+	DC	A(RE121+48)	address of v4 source
00006ADC	00000010			4715+	DC	A(16)	result length
00006AE0	00006B3C			4716+REA121	DC	A(RE121)	result address
00006AE8	00000000 00000000			4717+	DS	FD	gap
00006AF0	00000000 00000000			4718+V10121	DS	XL16	V1 output
00006AF8	00000000 00000000						

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  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

00006B00   00000000 00000000                     4719+        DS     FD              gap
                                                 4720+*
00006B08                                         4721+X121    DS     OF
00006B08   E310 5010 0014              00000010   4722+        LGF    R1,V2ADDR       load v2 source
00006B0E   E761 0000 0806              00000000   4723+        VL     v22,0(R1)       use v22 to test decoder
00006B14   E310 5014 0014              00000014   4724+        LGF    R1,V3ADDR       load v3 source
00006B1A   E771 0000 0806              00000000   4725+        VL     v23,0(R1)       use v23 to test decoder
00006B20   E310 5018 0014              00000018   4726+        LGF    R1,V4ADDR       load v4 source
00006B26   E781 0000 0806              00000000   4727+        VL     v24,0(R1)       use v24 to test decoder
00006B2C   E766 7200 8FAE                         4728+        VMAE   V22,V22,V23,V24,2    test instruction (dest is a source)
00006B32   E760 5030 080E              00006AF0   4729+        VST    V22,V10121       save v1 output
00006B38   07FB                                   4730+        BR     R11             return
00006B3C                                          4731+RE121   DC     0F              xl16 expected result
00006B3C                                          4732+        DROP   R5
00006B3C   00030000 0000012E                      4733         DC     XL16'000300000000012E 0000000300000C42'    result
00006B44   00000003 00000C42
00006B4C   FF0000FF 00000029                      4734         DC     XL16'FF0000FF00000029 00000038000000FA'    v2
00006B54   00000038 000000FA
00006B5C   FF000001 00000029                      4735         DC     XL16'FF00000100000029 00000038000000FA'    v3
00006B64   00000038 000000FA
00006B6C   00020001 0000002F                      4736         DC     XL16'000200010000002F 0000000300000002'    v4
00006B74   00000003 00000002
                                                  4737
                                                  4738         VRR_D  VMAE,2
00006B80                                          4739+        DS     OFD
00006B80                       00006B80           4740+        USING  *,R5            base for test data and test routine
00006B80   00006BC8                               4741+T122    DC     A(X122)         address of test routine
00006B84   007A                                   4742+        DC     H'122'          test number
00006B86   00                                     4743+        DC     X'00'
00006B87   02                                     4744+        DC     HL1'2'          m5
00006B88   E5D4C1C5 40404040                      4745+        DC     CL8'VMAE'       instruction name
00006B90   00006C0C                               4746+        DC     A(RE122+16)     address of v2 source
00006B94   00006C1C                               4747+        DC     A(RE122+32)     address of v3 source
00006B98   00006C2C                               4748+        DC     A(RE122+48)     address of v4 source
00006B9C   00000010                               4749+        DC     A(16)           result length
00006BA0   00006BFC                               4750+REA122  DC     A(RE122)        result address
00006BA8   00000000 00000000                      4751+        DS     FD              gap
00006BB0   00000000 00000000                      4752+V10122  DS     XL16            V1 output
00006BB8   00000000 00000000
00006BC0   00000000 00000000                      4753+        DS     FD              gap
                                                  4754+*
00006BC8                                          4755+X122    DS     OF
00006BC8   E310 5010 0014              00000010   4756+        LGF    R1,V2ADDR       load v2 source
00006BCE   E761 0000 0806              00000000   4757+        VL     v22,0(R1)       use v22 to test decoder
00006BD4   E310 5014 0014              00000014   4758+        LGF    R1,V3ADDR       load v3 source
00006BDA   E771 0000 0806              00000000   4759+        VL     v23,0(R1)       use v23 to test decoder
00006BE0   E310 5018 0014              00000018   4760+        LGF    R1,V4ADDR       load v4 source
00006BE6   E781 0000 0806              00000000   4761+        VL     v24,0(R1)       use v24 to test decoder
00006BEC   E766 7200 8FAE                         4762+        VMAE   V22,V22,V23,V24,2    test instruction (dest is a source)
00006BF2   E760 5030 080E              00006BB0   4763+        VST    V22,V10122       save v1 output
00006BF8   07FB                                   4764+        BR     R11             return
00006BFC                                          4765+RE122   DC     0F              xl16 expected result
00006BFC                                          4766+        DROP   R5
00006BFC   FF02FF02 091F1F18                      4767         DC     XL16'FF02FF02091F1F18 095BC037C27817A0'    result
00006C04   095BC037 C27817A0
00006C0C   FF020304 05060708                      4768         DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006C14	090A0B0C 0D0E0F10						
00006C1C	FF020304 05060708			4769	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3
00006C24	090A0B0C 0D0E0F10						
00006C2C	FF020304 05060708			4770	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00006C34	090A0B0C 0D0E0F10						
				4771			
				4772	VRR_D	VMAE, 2	
00006C40				4773+	DS	0FD	
00006C40		00006C40		4774+	USING	*,R5	base for test data and test routine
00006C40	00006C88			4775+T123	DC	A(X123)	address of test routine
00006C44	007B			4776+	DC	H'123'	test number
00006C46	00			4777+	DC	X'00'	
00006C47	02			4778+	DC	HL1'2'	m5
00006C48	E5D4C1C5 40404040			4779+	DC	CL8'VMAE'	instruction name
00006C50	00006CCC			4780+	DC	A(RE123+16)	address of v2 source
00006C54	00006CDC			4781+	DC	A(RE123+32)	address of v3 source
00006C58	00006CEC			4782+	DC	A(RE123+48)	address of v4 source
00006C5C	00000010			4783+	DC	A(16)	result length
00006C60	00006CBC			4784+REA123	DC	A(RE123)	result address
00006C68	00000000 00000000			4785+	DS	FD	gap
00006C70	00000000 00000000			4786+V10123	DS	XL16	V1 output
00006C78	00000000 00000000						
00006C80	00000000 00000000			4787+	DS	FD	gap
				4788+*			
00006C88				4789+X123	DS	0F	
00006C88	E310 5010 0014		00000010	4790+	LGF	R1,V2ADDR	load v2 source
00006C8E	E761 0000 0806		00000000	4791+	VL	v22,0(R1)	use v22 to test decoder
00006C94	E310 5014 0014		00000014	4792+	LGF	R1,V3ADDR	load v3 source
00006C9A	E771 0000 0806		00000000	4793+	VL	v23,0(R1)	use v23 to test decoder
00006CA0	E310 5018 0014		00000018	4794+	LGF	R1,V4ADDR	load v4 source
00006CA6	E781 0000 0806		00000000	4795+	VL	v24,0(R1)	use v24 to test decoder
00006CAC	E766 7200 8FAE			4796+	VMAE	V22,V22,V23,V24,2	test instruction (dest is a source)
00006CB2	E760 5030 080E		00006C70	4797+	VST	V22,V10123	save v1 output
00006CB8	07FB			4798+	BR	R11	return
00006CBC				4799+RE123	DC	0F	xl16 expected result
00006CBC				4800+	DROP	R5	
00006CBC	FF030002 04111110			4801	DC	XL16'FF03000204111110 092E6097DCBD8D58'	result
00006CC4	092E6097 DCBD8D58						
00006CCC	FF020304 05060708			4802	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00006CD4	090A0B0C 0D0E0F10						
00006CDC	FF010102 02030304			4803	DC	XL16'FF01010202030304 0405050606070708'	v3
00006CE4	04050506 06070708						
00006CEC	FF020304 05060708			4804	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00006CF4	090A0B0C 0D0E0F10						
				4805			
				4806	VRR_D	VMAE, 2	
00006D00				4807+	DS	0FD	
00006D00		00006D00		4808+	USING	*,R5	base for test data and test routine
00006D00	00006D48			4809+T124	DC	A(X124)	address of test routine
00006D04	007C			4810+	DC	H'124'	test number
00006D06	00			4811+	DC	X'00'	
00006D07	02			4812+	DC	HL1'2'	m5
00006D08	E5D4C1C5 40404040			4813+	DC	CL8'VMAE'	instruction name
00006D10	00006D8C			4814+	DC	A(RE124+16)	address of v2 source
00006D14	00006D9C			4815+	DC	A(RE124+32)	address of v3 source
00006D18	00006DAC			4816+	DC	A(RE124+48)	address of v4 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006D1C	00000010			4817+	DC	A(16)	result length
00006D20	00006D7C			4818+REA124	DC	A(RE124)	result address
00006D28	00000000 00000000			4819+	DS	FD	gap
00006D30	00000000 00000000			4820+V10124	DS	XL16	V1 output
00006D38	00000000 00000000						
00006D40	00000000 00000000			4821+	DS	FD	gap
				4822+*			
00006D48				4823+X124	DS	0F	
00006D48	E310 5010 0014		00000010	4824+	LGF	R1,V2ADDR	load v2 source
00006D4E	E761 0000 0806		00000000	4825+	VL	v22,0(R1)	use v22 to test decoder
00006D54	E310 5014 0014		00000014	4826+	LGF	R1,V3ADDR	load v3 source
00006D5A	E771 0000 0806		00000000	4827+	VL	v23,0(R1)	use v23 to test decoder
00006D60	E310 5018 0014		00000018	4828+	LGF	R1,V4ADDR	load v4 source
00006D66	E781 0000 0806		00000000	4829+	VL	v24,0(R1)	use v24 to test decoder
00006D6C	E766 7200 8FAE			4830+	VMAE	V22,V22,V23,V24,2	test instruction (dest is a source)
00006D72	E760 5030 080E		00006D30	4831+	VST	V22,V10124	save v1 output
00006D78	07FB			4832+	BR	R11	return
00006D7C				4833+RE124	DC	0F	xl16 expected result
00006D7C				4834+	DROP	R5	
00006D7C	FF030101 01060708			4835	DC	XL16'FF03010101060708 09131E2A372F261C'	result
00006D84	09131E2A 372F261C						
00006D8C	FF020304 05060708			4836	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00006D94	090A0B0C 0D0E0F10						
00006D9C	FF000000 00000001			4837	DC	XL16'FF00000000000001 0101010101010102'	v3
00006DA4	01010101 01010102						
00006DAC	FF020304 05060708			4838	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00006DB4	090A0B0C 0D0E0F10						
				4839			
				4840 * Doubleword			
				4841	VRR_D	VMAE,3	
00006DC0				4842+	DS	0FD	
00006DC0		00006DC0		4843+	USING	*,R5	base for test data and test routine
00006DC0	00006E08			4844+T125	DC	A(X125)	address of test routine
00006DC4	007D			4845+	DC	H'125'	test number
00006DC6	00			4846+	DC	X'00'	
00006DC7	03			4847+	DC	HL1'3'	m5
00006DC8	E5D4C1C5 40404040			4848+	DC	CL8'VMAE'	instruction name
00006DD0	00006E4C			4849+	DC	A(RE125+16)	address of v2 source
00006DD4	00006E5C			4850+	DC	A(RE125+32)	address of v3 source
00006DD8	00006E6C			4851+	DC	A(RE125+48)	address of v4 source
00006DDC	00000010			4852+	DC	A(16)	result length
00006DE0	00006E3C			4853+REA125	DC	A(RE125)	result address
00006DE8	00000000 00000000			4854+	DS	FD	gap
00006DF0	00000000 00000000			4855+V10125	DS	XL16	V1 output
00006DF8	00000000 00000000						
00006E00	00000000 00000000			4856+	DS	FD	gap
				4857+*			
00006E08				4858+X125	DS	0F	
00006E08	E310 5010 0014		00000010	4859+	LGF	R1,V2ADDR	load v2 source
00006E0E	E761 0000 0806		00000000	4860+	VL	v22,0(R1)	use v22 to test decoder
00006E14	E310 5014 0014		00000014	4861+	LGF	R1,V3ADDR	load v3 source
00006E1A	E771 0000 0806		00000000	4862+	VL	v23,0(R1)	use v23 to test decoder
00006E20	E310 5018 0014		00000018	4863+	LGF	R1,V4ADDR	load v4 source
00006E26	E781 0000 0806		00000000	4864+	VL	v24,0(R1)	use v24 to test decoder
00006E2C	E766 7300 8FAE			4865+	VMAE	V22,V22,V23,V24,3	test instruction (dest is a source)
00006E32	E760 5030 080E		00006DF0	4866+	VST	V22,V10125	save v1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00006E38	07FB			4867+	BR	R11		return
00006E3C				4868+RE125	DC	0F		xl16 expected result
00006E3C				4869+	DROP	R5		
00006E3C	00000000 00000000			4870	DC	XL16'0000000000000000 FFFCE00271000000'		result
00006E44	FFFCE002 71000000							
00006E4C	FFFFFFFF 00019000			4871	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'		v2
00006E54	00000038 EEEEEEFA							
00006E5C	FFFFFFFF 00019000			4872	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'		v3
00006E64	00000038 0EEEEEFA							
00006E6C	00000000 00000000			4873	DC	XL16'0000000000000000 0000000000000000'		v4
00006E74	00000000 00000000							
				4874				
				4875	VRR_D	VMAE, 3		
00006E80				4876+	DS	0FD		
00006E80		00006E80		4877+	USING	*,R5		base for test data and test routine
00006E80	00006EC8			4878+T126	DC	A(X126)		address of test routine
00006E84	007E			4879+	DC	H'126'		test number
00006E86	00			4880+	DC	X'00'		
00006E87	03			4881+	DC	HL1'3'		m5
00006E88	E5D4C1C5 40404040			4882+	DC	CL8'VMAE'		instruction name
00006E90	00006F0C			4883+	DC	A(RE126+16)		address of v2 source
00006E94	00006F1C			4884+	DC	A(RE126+32)		address of v3 source
00006E98	00006F2C			4885+	DC	A(RE126+48)		address of v4 source
00006E9C	00000010			4886+	DC	A(16)		result length
00006EA0	00006EFC			4887+REA126	DC	A(RE126)		result address
00006EA8	00000000 00000000			4888+	DS	FD		gap
00006EB0	00000000 00000000			4889+V10126	DS	XL16		V1 output
00006EB8	00000000 00000000							
00006EC0	00000000 00000000			4890+	DS	FD		gap
				4891+*				
00006EC8				4892+X126	DS	0F		
00006EC8	E310 5010 0014		00000010	4893+	LGF	R1,V2ADDR		load v2 source
00006ECE	E761 0000 0806		00000000	4894+	VL	v22,0(R1)		use v22 to test decoder
00006ED4	E310 5014 0014		00000014	4895+	LGF	R1,V3ADDR		load v3 source
00006EDA	E771 0000 0806		00000000	4896+	VL	v23,0(R1)		use v23 to test decoder
00006EE0	E310 5018 0014		00000018	4897+	LGF	R1,V4ADDR		load v4 source
00006EE6	E781 0000 0806		00000000	4898+	VL	v24,0(R1)		use v24 to test decoder
00006EEC	E766 7300 8FAE			4899+	VMAE	V22,V22,V23,V24,3		test instruction (dest is a source)
00006EF2	E760 5030 080E		00006EB0	4900+	VST	V22,V10126		save v1 output
00006EF8	07FB			4901+	BR	R11		return
00006EFC				4902+RE126	DC	0F		xl16 expected result
00006EFC				4903+	DROP	R5		
00006EFC	FFFF0004 0C192C46			4904	DC	XL16'FFFF00040C192C46 69B556ED77F578FF'		result
00006F04	69B556ED 77F578FF							
00006F0C	FF020304 05060750			4905	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'		v2
00006F14	090A0B0C 0D0E0F7F							
00006F1C	01020304 05060750			4906	DC	XL16'0102030405060750 090A0B780D0E0F7F'		v3
00006F24	090A0B78 0D0E0F7F							
00006F2C	FFFFFFFF FFFFFFFF			4907	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'		v4
00006F34	FFFFFFFF FFFFFFFF							
				4908				
				4909	VRR_D	VMAE, 3		
00006F40				4910+	DS	0FD		
00006F40		00006F40		4911+	USING	*,R5		base for test data and test routine
00006F40	00006F88			4912+T127	DC	A(X127)		address of test routine
00006F44	007F			4913+	DC	H'127'		test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00006F46	00			4914+	DC	X'00'		
00006F47	03			4915+	DC	HL1'3'	m5	
00006F48	E5D4C1C5 40404040			4916+	DC	CL8'VMAE'	instruction name	
00006F50	00006FCC			4917+	DC	A(RE127+16)	address of v2 source	
00006F54	00006FDC			4918+	DC	A(RE127+32)	address of v3 source	
00006F58	00006FEC			4919+	DC	A(RE127+48)	address of v4 source	
00006F5C	00000010			4920+	DC	A(16)	result length	
00006F60	00006FBC			4921+REA127	DC	A(RE127)	result address	
00006F68	00000000 00000000			4922+	DS	FD	gap	
00006F70	00000000 00000000			4923+V10127	DS	XL16	V1 output	
00006F78	00000000 00000000							
00006F80	00000000 00000000			4924+	DS	FD	gap	
				4925+*				
00006F88				4926+X127	DS	0F		
00006F88	E310 5010 0014		00000010	4927+	LGF	R1,V2ADDR	load v2 source	
00006F8E	E761 0000 0806		00000000	4928+	VL	v22,0(R1)	use v22 to test decoder	
00006F94	E310 5014 0014		00000014	4929+	LGF	R1,V3ADDR	load v3 source	
00006F9A	E771 0000 0806		00000000	4930+	VL	v23,0(R1)	use v23 to test decoder	
00006FA0	E310 5018 0014		00000018	4931+	LGF	R1,V4ADDR	load v4 source	
00006FA6	E781 0000 0806		00000000	4932+	VL	v24,0(R1)	use v24 to test decoder	
00006FAC	E766 7300 8FAE			4933+	VMAE	V22,V22,V23,V24,3	test instruction (dest is a source)	
00006FB2	E760 5030 080E		00006F70	4934+	VST	V22,V10127	save v1 output	
00006FB8	07FB			4935+	BR	R11	return	
00006FBC				4936+RE127	DC	0F	xl16 expected result	
00006FBC				4937+	DROP	R5		
00006FBC	FFFFFF01 0309101D			4938	DC	XL16'FFFFFF010309101D 06D2FE7090F71480'	result	
00006FC4	06D2FE70 90F71480							
00006FCC	FF020304 05060750			4939	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2	
00006FD4	090A0B0C 0D0E0F7F							
00006FDC	00010102 02030328			4940	DC	XL16'0001010202030328 0405053C0607073F'	v3	
00006FE4	0405053C 0607073F							
00006FEC	00000000 00000001			4941	DC	XL16'0000000000000001 0000000000000000'	v4	
00006FF4	00000000 00000000							
				4942				
				4943		VRR_D VMAE,3		
00007000				4944+	DS	0FD		
00007000		00007000		4945+	USING	*,R5	base for test data and test routine	
00007000	00007048			4946+T128	DC	A(X128)	address of test routine	
00007004	0080			4947+	DC	H'128'	test number	
00007006	00			4948+	DC	X'00'		
00007007	03			4949+	DC	HL1'3'	m5	
00007008	E5D4C1C5 40404040			4950+	DC	CL8'VMAE'	instruction name	
00007010	0000708C			4951+	DC	A(RE128+16)	address of v2 source	
00007014	0000709C			4952+	DC	A(RE128+32)	address of v3 source	
00007018	000070AC			4953+	DC	A(RE128+48)	address of v4 source	
0000701C	00000010			4954+	DC	A(16)	result length	
00007020	0000707C			4955+REA128	DC	A(RE128)	result address	
00007028	00000000 00000000			4956+	DS	FD	gap	
00007030	00000000 00000000			4957+V10128	DS	XL16	V1 output	
00007038	00000000 00000000							
00007040	00000000 00000000			4958+	DS	FD	gap	
				4959+*				
00007048				4960+X128	DS	0F		
00007048	E310 5010 0014		00000010	4961+	LGF	R1,V2ADDR	load v2 source	
0000704E	E761 0000 0806		00000000	4962+	VL	v22,0(R1)	use v22 to test decoder	
00007054	E310 5014 0014		00000014	4963+	LGF	R1,V3ADDR	load v3 source	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000705A	E771 0000 0806		00000000	4964+	VL	v23,0(R1)	use v23 to test decoder
00007060	E310 5018 0014		00000018	4965+	LGF	R1,V4ADDR	load v4 source
00007066	E781 0000 0806		00000000	4966+	VL	v24,0(R1)	use v24 to test decoder
0000706C	E766 7300 8FAE			4967+	VMAE	V22,V22,V23,V24,3	test instruction (dest is a source)
00007072	E760 5030 080E		00007030	4968+	VST	V22,V10128	save v1 output
00007078	07FB			4969+	BR	R11	return
0000707C				4970+RE128	DC	0F	xl16 expected result
0000707C				4971+	DROP	R5	
0000707C	FFFFFFFF FFFFFFFF			4972	DC	XL16'FFFFFFFFFFFFFFFF F6141E28323C491C'	result
00007084	F6141E28 323C491C						
0000708C	FF020304 05060750			4973	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00007094	090A0B0C 0D0E0F7F						
0000709C	00000000 0000000A			4974	DC	XL16'000000000000000A 0101010F0101010F'	v3
000070A4	0101010F 0101010F						
000070AC	FFFFFFFF FFFFFFFF			4975	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFC'	v4
000070B4	FFFFFFFF FFFFFFFC						
				4976			
				4977	VRR_D	VMAE,3	
000070C0				4978+	DS	0FD	
000070C0		000070C0		4979+	USING	*,R5	base for test data and test routine
000070C0	00007108			4980+T129	DC	A(X129)	address of test routine
000070C4	0081			4981+	DC	H'129'	test number
000070C6	00			4982+	DC	X'00'	
000070C7	03			4983+	DC	HL1'3'	m5
000070C8	E5D4C1C5 40404040			4984+	DC	CL8'VMAE'	instruction name
000070D0	0000714C			4985+	DC	A(RE129+16)	address of v2 source
000070D4	0000715C			4986+	DC	A(RE129+32)	address of v3 source
000070D8	0000716C			4987+	DC	A(RE129+48)	address of v4 source
000070DC	00000010			4988+	DC	A(16)	result length
000070E0	0000713C			4989+REA129	DC	A(RE129)	result address
000070E8	00000000 00000000			4990+	DS	FD	gap
000070F0	00000000 00000000			4991+V10129	DS	XL16	V1 output
000070F8	00000000 00000000						
00007100	00000000 00000000			4992+	DS	FD	gap
				4993+*			
00007108				4994+X129	DS	0F	
00007108	E310 5010 0014		00000010	4995+	LGF	R1,V2ADDR	load v2 source
0000710E	E761 0000 0806		00000000	4996+	VL	v22,0(R1)	use v22 to test decoder
00007114	E310 5014 0014		00000014	4997+	LGF	R1,V3ADDR	load v3 source
0000711A	E771 0000 0806		00000000	4998+	VL	v23,0(R1)	use v23 to test decoder
00007120	E310 5018 0014		00000018	4999+	LGF	R1,V4ADDR	load v4 source
00007126	E781 0000 0806		00000000	5000+	VL	v24,0(R1)	use v24 to test decoder
0000712C	E766 7300 8FAE			5001+	VMAE	V22,V22,V23,V24,3	test instruction (dest is a source)
00007132	E760 5030 080E		000070F0	5002+	VST	V22,V10129	save v1 output
00007138	07FB			5003+	BR	R11	return
0000713C				5004+RE129	DC	0F	xl16 expected result
0000713C				5005+	DROP	R5	
0000713C	7709131E A8C3DFFE			5006	DC	XL16'7709131EA8C3DFFE F91C345060616771'	result
00007144	F91C3450 60616771						
0000714C	090A0B0C 0D0E0F7F			5007	DC	XL16'090A0B0C0D0E0F7F FF02030405060750'	v2
00007154	FF020304 05060750						
0000715C	0101010F 0101010F			5008	DC	XL16'0101010F0101010F 000000000000000A'	v3
00007164	00000000 0000000A						
0000716C	77000000 00000000			5009	DC	XL16'7700000000000000 F000000000000000'	v4
00007174	F0000000 00000000						
				5010			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				5011 *--			
				5012 * VMAO - Vector Multiply and Add Odd			
				5013 *--			
				5014 * Byte			
				5015	VRR_D	VMAO,0	
00007180				5016+	DS	0FD	
00007180		00007180		5017+	USING	*,R5	base for test data and test routine
00007180	000071C8			5018+T130	DC	A(X130)	address of test routine
00007184	0082			5019+	DC	H'130'	test number
00007186	00			5020+	DC	X'00'	
00007187	00			5021+	DC	HL1'0'	m5
00007188	E5D4C1D6 40404040			5022+	DC	CL8'VMAO'	instruction name
00007190	0000720C			5023+	DC	A(RE130+16)	address of v2 source
00007194	0000721C			5024+	DC	A(RE130+32)	address of v3 source
00007198	0000722C			5025+	DC	A(RE130+48)	address of v4 source
0000719C	00000010			5026+	DC	A(16)	result length
000071A0	000071FC			5027+REA130	DC	A(RE130)	result address
000071A8	00000000 00000000			5028+	DS	FD	gap
000071B0	00000000 00000000			5029+V10130	DS	XL16	V1 output
000071B8	00000000 00000000						
000071C0	00000000 00000000			5030+	DS	FD	gap
				5031+*			
000071C8				5032+X130	DS	0F	
000071C8	E310 5010 0014		00000010	5033+	LGF	R1,V2ADDR	load v2 source
000071CE	E761 0000 0806		00000000	5034+	VL	v22,0(R1)	use v22 to test decoder
000071D4	E310 5014 0014		00000014	5035+	LGF	R1,V3ADDR	load v3 source
000071DA	E771 0000 0806		00000000	5036+	VL	v23,0(R1)	use v23 to test decoder
000071E0	E310 5018 0014		00000018	5037+	LGF	R1,V4ADDR	load v4 source
000071E6	E781 0000 0806		00000000	5038+	VL	v24,0(R1)	use v24 to test decoder
000071EC	E766 7000 8FAF			5039+	VMAO	V22,V22,V23,V24,0	test instruction (dest is a source)
000071F2	E760 5030 080E		000071B0	5040+	VST	V22,V10130	save v1 output
000071F8	07FB			5041+	BR	R11	return
000071FC				5042+RE130	DC	0F	xl16 expected result
000071FC				5043+	DROP	R5	
000071FC	00000000 00000271			5044	DC	XL16'0000000000000271 00000C4000000024' result	
00007204	00000C40 00000024						
0000720C	FF000000 00000019			5045	DC	XL16'FF00000000000019 00000038000000FA' v2	
00007214	00000038 000000FA						
0000721C	FF000000 00000019			5046	DC	XL16'FF00000000000019 00000038000000FA' v3	
00007224	00000038 000000FA						
0000722C	00000000 00000000			5047	DC	XL16'0000000000000000 0000000000000000' v4	
00007234	00000000 00000000						
				5048			
				5049	VRR_D	VMAO,0	
00007240				5050+	DS	0FD	
00007240		00007240		5051+	USING	*,R5	base for test data and test routine
00007240	00007288			5052+T131	DC	A(X131)	address of test routine
00007244	0083			5053+	DC	H'131'	test number
00007246	00			5054+	DC	X'00'	
00007247	00			5055+	DC	HL1'0'	m5
00007248	E5D4C1D6 40404040			5056+	DC	CL8'VMAO'	instruction name
00007250	000072CC			5057+	DC	A(RE131+16)	address of v2 source
00007254	000072DC			5058+	DC	A(RE131+32)	address of v3 source
00007258	000072EC			5059+	DC	A(RE131+48)	address of v4 source
0000725C	00000010			5060+	DC	A(16)	result length
00007260	000072BC			5061+REA131	DC	A(RE131)	result address

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00007268   00000000 00000000                     5062+        DS    FD                gap
00007270   00000000 00000000                     5063+V10131   DS    XL16              V1 output
00007278   00000000 00000000
00007280   00000000 00000000                     5064+        DS    FD                gap
                                                 5065+*
00007288                                         5066+X131     DS    0F
00007288   E310 5010 0014                00000010 5067+        LGF   R1,V2ADDR         load v2 source
0000728E   E761 0000 0806                00000000 5068+        VL    v22,0(R1)         use v22 to test decoder
00007294   E310 5014 0014                00000014 5069+        LGF   R1,V3ADDR         load v3 source
0000729A   E771 0000 0806                00000000 5070+        VL    v23,0(R1)         use v23 to test decoder
000072A0   E310 5018 0014                00000018 5071+        LGF   R1,V4ADDR         load v4 source
000072A6   E781 0000 0806                00000000 5072+        VL    v24,0(R1)         use v24 to test decoder
000072AC   E766 7000 8FAF                         5073+        VMA0  V22,V22,V23,V24,0   test instruction (dest is a source)
000072B2   E760 5030 080E                00007270 5074+        VST   V22,V10131         save v1 output
000072B8   07FB                                   5075+        BR    R11               return
000072BC                                          5076+RE131   DC    0F                xl16 expected result
000072BC                                          5077+        DROP  R5
000072BC   00020000 000006C0                      5078         DC    XL16'00020000000006C0 00000C4300000026'   result
000072C4   00000C43 00000026
000072CC   FF0000FF 00000029                      5079         DC    XL16'FF0000FF00000029 00000038000000FA'   v2
000072D4   00000038 000000FA
000072DC   FF000001 00000029                      5080         DC    XL16'FF00000100000029 00000038000000FA'   v3
000072E4   00000038 000000FA
000072EC   00020001 0000002F                      5081         DC    XL16'000200010000002F 0000000300000002'   v4
000072F4   00000003 00000002
                                                 5082
                                                 5083         VRR_D VMA0,0
00007300                                          5084+        DS    0FD
00007300                               00007300   5085+        USING *,R5             base for test data and test routine
00007300   00007348                               5086+T132    DC    A(X132)           address of test routine
00007304   0084                                   5087+        DC    H'132'            test number
00007306   00                                     5088+        DC    X'00'
00007307   00                                     5089+        DC    HL1'0'            m5
00007308   E5D4C1D6 40404040                       5090+        DC    CL8'VMA0'         instruction name
00007310   0000738C                               5091+        DC    A(RE132+16)       address of v2 source
00007314   0000739C                               5092+        DC    A(RE132+32)       address of v3 source
00007318   000073AC                               5093+        DC    A(RE132+48)       address of v4 source
0000731C   00000010                               5094+        DC    A(16)             result length
00007320   0000737C                               5095+REA132  DC    A(RE132)          result address
00007328   00000000 00000000                      5096+        DS    FD                gap
00007330   00000000 00000000                      5097+V10132  DS    XL16              V1 output
00007338   00000000 00000000
00007340   00000000 00000000                      5098+        DS    FD                gap
                                                 5099+*
00007348                                          5100+X132     DS    0F
00007348   E310 5010 0014                00000010 5101+        LGF   R1,V2ADDR         load v2 source
0000734E   E761 0000 0806                00000000 5102+        VL    v22,0(R1)         use v22 to test decoder
00007354   E310 5014 0014                00000014 5103+        LGF   R1,V3ADDR         load v3 source
0000735A   E771 0000 0806                00000000 5104+        VL    v23,0(R1)         use v23 to test decoder
00007360   E310 5018 0014                00000018 5105+        LGF   R1,V4ADDR         load v4 source
00007366   E781 0000 0806                00000000 5106+        VL    v24,0(R1)         use v24 to test decoder
0000736C   E766 7000 8FAF                         5107+        VMA0  V22,V22,V23,V24,0   test instruction (dest is a source)
00007372   E760 5030 080E                00007330 5108+        VST   V22,V10132         save v1 output
00007378   07FB                                   5109+        BR    R11               return
0000737C                                          5110+RE132   DC    0F                xl16 expected result
0000737C                                          5111+        DROP  R5
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000737C	FF060314 052A0748			5112	DC	XL16'FF060314052A0748 096E0B9C0DD21010'	result
00007384	096E0B9C 0DD21010						
0000738C	FF020304 05060708			5113	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00007394	090A0B0C 0D0E0F10						
0000739C	FF020304 05060708			5114	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3
000073A4	090A0B0C 0D0E0F10						
000073AC	FF020304 05060708			5115	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
000073B4	090A0B0C 0D0E0F10						
				5116			
				5117	VRR_D	VMA0,0	
000073C0				5118+	DS	0FD	
000073C0		000073C0		5119+	USING	*,R5	base for test data and test routine
000073C0	00007408			5120+T133	DC	A(X133)	address of test routine
000073C4	0085			5121+	DC	H'133'	test number
000073C6	00			5122+	DC	X'00'	
000073C7	00			5123+	DC	HL1'0'	m5
000073C8	E5D4C1D6 40404040			5124+	DC	CL8'VMA0'	instruction name
000073D0	0000744C			5125+	DC	A(RE133+16)	address of v2 source
000073D4	0000745C			5126+	DC	A(RE133+32)	address of v3 source
000073D8	0000746C			5127+	DC	A(RE133+48)	address of v4 source
000073DC	00000010			5128+	DC	A(16)	result length
000073E0	0000743C			5129+REA133	DC	A(RE133)	result address
000073E8	00000000 00000000			5130+	DS	FD	gap
000073F0	00000000 00000000			5131+V10133	DS	XL16	V1 output
000073F8	00000000 00000000						
00007400	00000000 00000000			5132+	DS	FD	gap
				5133+*			
00007408				5134+X133	DS	0F	
00007408	E310 5010 0014		00000010	5135+	LGF	R1,V2ADDR	load v2 source
0000740E	E761 0000 0806		00000000	5136+	VL	v22,0(R1)	use v22 to test decoder
00007414	E310 5014 0014		00000014	5137+	LGF	R1,V3ADDR	load v3 source
0000741A	E771 0000 0806		00000000	5138+	VL	v23,0(R1)	use v23 to test decoder
00007420	E310 5018 0014		00000018	5139+	LGF	R1,V4ADDR	load v4 source
00007426	E781 0000 0806		00000000	5140+	VL	v24,0(R1)	use v24 to test decoder
0000742C	E766 7000 8FAF			5141+	VMA0	V22,V22,V23,V24,0	test instruction (dest is a source)
00007432	E760 5030 080E		000073F0	5142+	VST	V22,V10133	save v1 output
00007438	07FB			5143+	BR	R11	return
0000743C				5144+RE133	DC	0F	xl16 expected result
0000743C				5145+	DROP	R5	
0000743C	FF04030C 05180728			5146	DC	XL16'FF04030C05180728 093C0B540D700F90'	result
00007444	093C0B54 0D700F90						
0000744C	FF020304 05060708			5147	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00007454	090A0B0C 0D0E0F10						
0000745C	FF010102 02030304			5148	DC	XL16'FF01010202030304 0405050606070708'	v3
00007464	04050506 06070708						
0000746C	FF020304 05060708			5149	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00007474	090A0B0C 0D0E0F10						
				5150			
				5151	VRR_D	VMA0,0	
00007480				5152+	DS	0FD	
00007480		00007480		5153+	USING	*,R5	base for test data and test routine
00007480	000074C8			5154+T134	DC	A(X134)	address of test routine
00007484	0086			5155+	DC	H'134'	test number
00007486	00			5156+	DC	X'00'	
00007487	00			5157+	DC	HL1'0'	m5
00007488	E5D4C1D6 40404040			5158+	DC	CL8'VMA0'	instruction name

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  LOC        OBJECT CODE      ADDR1     ADDR2      STMT

00007490  0000750C                                5159+        DC     A(RE134+16)      address of v2 source
00007494  0000751C                                5160+        DC     A(RE134+32)      address of v3 source
00007498  0000752C                                5161+        DC     A(RE134+48)      address of v4 source
0000749C  00000010                                5162+        DC     A(16)            result length
000074A0  000074FC                                5163+REA134  DC     A(RE134)         result address
000074A8  00000000 00000000                       5164+        DS     FD               gap
000074B0  00000000 00000000                       5165+V10134  DS     XL16             V1 output
000074B8  00000000 00000000
000074C0  00000000 00000000                       5166+        DS     FD               gap
                                                  5167+*
000074C8                                          5168+X134    DS     0F
000074C8  E310 5010 0014              00000010     5169+        LGF    R1,V2ADDR        load v2 source
000074CE  E761 0000 0806              00000000     5170+        VL     v22,0(R1)        use v22 to test decoder
000074D4  E310 5014 0014              00000014     5171+        LGF    R1,V3ADDR        load v3 source
000074DA  E771 0000 0806              00000000     5172+        VL     v23,0(R1)        use v23 to test decoder
000074E0  E310 5018 0014              00000018     5173+        LGF    R1,V4ADDR        load v4 source
000074E6  E781 0000 0806              00000000     5174+        VL     v24,0(R1)        use v24 to test decoder
000074EC  E766 7000 8FAF                           5175+        VMAO   V22,V22,V23,V24,0   test instruction (dest is a source)
000074F2  E760 5030 080E              000074B0     5176+        VST    V22,V10134         save v1 output
000074F8  07FB                                     5177+        BR     R11              return
000074FC                                           5178+RE134   DC     0F               xl16 expected result
000074FC                                           5179+        DROP   R5
000074FC  FF020304 05060710                        5180         DC     XL16'FF02030405060710 09140B180D1C0F30'    result
00007504  09140B18 0D1C0F30
0000750C  FF020304 05060708                        5181         DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00007514  090A0B0C 0D0E0F10
0000751C  FF000000 00000001                        5182         DC     XL16'FF00000000000001 0101010101010102'    v3
00007524  01010101 01010102
0000752C  FF020304 05060708                        5183         DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00007534  090A0B0C 0D0E0F10

                                                  5184
                                                  5185  * Halfword
                                                  5186         VRR_D  VMAO,1
00007540                                          5187+        DS     0FD
00007540                            00007540       5188+        USING  *,R5             base for test data and test routine
00007540  00007588                                5189+T135    DC     A(X135)          address of test routine
00007544  0087                                     5190+        DC     H'135'           test number
00007546  00                                       5191+        DC     X'00'
00007547  01                                       5192+        DC     HL1'1'           m5
00007548  E5D4C1D6 40404040                        5193+        DC     CL8'VMAO'        instruction name
00007550  000075CC                                 5194+        DC     A(RE135+16)      address of v2 source
00007554  000075DC                                 5195+        DC     A(RE135+32)      address of v3 source
00007558  000075EC                                 5196+        DC     A(RE135+48)      address of v4 source
0000755C  00000010                                 5197+        DC     A(16)            result length
00007560  000075BC                                 5198+REA135  DC     A(RE135)         result address
00007568  00000000 00000000                       5199+        DS     FD               gap
00007570  00000000 00000000                       5200+V10135  DS     XL16             V1 output
00007578  00000000 00000000
00007580  00000000 00000000                       5201+        DS     FD               gap
                                                  5202+*
00007588                                          5203+X135    DS     0F
00007588  E310 5010 0014              00000010     5204+        LGF    R1,V2ADDR        load v2 source
0000758E  E761 0000 0806              00000000     5205+        VL     v22,0(R1)        use v22 to test decoder
00007594  E310 5014 0014              00000014     5206+        LGF    R1,V3ADDR        load v3 source
0000759A  E771 0000 0806              00000000     5207+        VL     v23,0(R1)        use v23 to test decoder
000075A0  E310 5018 0014              00000018     5208+        LGF    R1,V4ADDR        load v4 source
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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT


 000075A6  E781 0000 0806                 00000000  5209+               VL    v24,0(R1)           use v24 to test decoder
 000075AC  E766 7100 8FAF                           5210+               VMA0  V22,V22,V23,V24,1    test instruction (dest is a source)
 000075B2  E760 5030 080E                 00007570  5211+               VST   V22,V10135           save v1 output
 000075B8  07FB                                     5212+               BR    R11                  return
 000075BC                                           5213+RE135          DC    0F                   xl16 expected result
 000075BC                                           5214+               DROP  R5
 000075BC  00000000 00000271                        5215                DC    XL16'0000000000000271 00000C400000F424'    result
 000075C4  00000C40 0000F424
 000075CC  FF000000 00000019                        5216                DC    XL16'FF00000000000019 00000038000000FA'    v2
 000075D4  00000038 000000FA
 000075DC  FF000000 00000019                        5217                DC    XL16'FF00000000000019 00000038000000FA'    v3
 000075E4  00000038 000000FA
 000075EC  00000000 00000000                        5218                DC    XL16'0000000000000000 0000000000000000'    v4
 000075F4  00000000 00000000
                                                    5219
                                                    5220                VRR_D VMA0,1
 00007600                                           5221+               DS    0FD
 00007600                     00007600              5222+               USING *,R5                 base for test data and test routine
 00007600  00007648                                 5223+T136           DC    A(X136)              address of test routine
 00007604  0088                                     5224+               DC    H'136'               test number
 00007606  00                                       5225+               DC    X'00'
 00007607  01                                       5226+               DC    HL1'1'               m5
 00007608  E5D4C1D6 40404040                        5227+               DC    CL8'VMA0'            instruction name
 00007610  0000768C                                 5228+               DC    A(RE136+16)          address of v2 source
 00007614  0000769C                                 5229+               DC    A(RE136+32)          address of v3 source
 00007618  000076AC                                 5230+               DC    A(RE136+48)          address of v4 source
 0000761C  00000010                                 5231+               DC    A(16)                result length
 00007620  0000767C                                 5232+REA136         DC    A(RE136)             result address
 00007628  00000000 00000000                        5233+               DS    FD                   gap
 00007630  00000000 00000000                        5234+V10136         DS    XL16                 V1 output
 00007638  00000000 00000000
 00007640  00000000 00000000                        5235+               DS    FD                   gap
                                                    5236+*
 00007648                                           5237+X136           DS    0F
 00007648  E310 5010 0014                 00000010  5238+               LGF   R1,V2ADDR            load v2 source
 0000764E  E761 0000 0806                 00000000  5239+               VL    v22,0(R1)            use v22 to test decoder
 00007654  E310 5014 0014                 00000014  5240+               LGF   R1,V3ADDR            load v3 source
 0000765A  E771 0000 0806                 00000000  5241+               VL    v23,0(R1)            use v23 to test decoder
 00007660  E310 5018 0014                 00000018  5242+               LGF   R1,V4ADDR            load v4 source
 00007666  E781 0000 0806                 00000000  5243+               VL    v24,0(R1)            use v24 to test decoder
 0000766C  E766 7100 8FAF                           5244+               VMA0  V22,V22,V23,V24,1    test instruction (dest is a source)
 00007672  E760 5030 080E                 00007630  5245+               VST   V22,V10136           save v1 output
 00007678  07FB                                     5246+               BR    R11                  return
 0000767C                                           5247+RE136          DC    0F                   xl16 expected result
 0000767C                                           5248+               DROP  R5
 0000767C  00020100 000006C0                        5249                DC    XL16'00020100000006C0 00000C430000F426'    result
 00007684  00000C43 0000F426
 0000768C  FF0000FF 00000029                        5250                DC    XL16'FF0000FF00000029 00000038000000FA'    v2
 00007694  00000038 000000FA
 0000769C  FF000001 00000029                        5251                DC    XL16'FF00000100000029 00000038000000FA'    v3
 000076A4  00000038 000000FA
 000076AC  00020001 0000002F                        5252                DC    XL16'000200010000002F 0000000300000002'    v4
 000076B4  00000003 00000002
                                                    5253
                                                    5254                VRR_D VMA0,1
 000076C0                                           5255+               DS    0FD
```

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  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

000076C0                        000076C0            5256+              USING *,R5              base for test data and test routine
000076C0   00007708                                 5257+T137     DC   A(X137)                address of test routine
000076C4   0089                                      5258+         DC   H'137'                 test number
000076C6   00                                        5259+         DC   X'00'
000076C7   01                                        5260+         DC   HL1'1'                 m5
000076C8   E5D4C1D6 40404040                         5261+         DC   CL8'VMAO'              instruction name
000076D0   0000774C                                  5262+         DC   A(RE137+16)            address of v2 source
000076D4   0000775C                                  5263+         DC   A(RE137+32)            address of v3 source
000076D8   0000776C                                  5264+         DC   A(RE137+48)            address of v4 source
000076DC   00000010                                  5265+         DC   A(16)                  result length
000076E0   0000773C                                  5266+REA137   DC   A(RE137)               result address
000076E8   00000000 00000000                         5267+         DS   FD                     gap
000076F0   00000000 00000000                         5268+V10137   DS   XL16                   V1 output
000076F8   00000000 00000000
00007700   00000000 00000000                         5269+         DS   FD                     gap
                                                     5270+*
00007708                                             5271+X137     DS   0F
00007708   E310 5010 0014                 00000010   5272+         LGF   R1,V2ADDR             load v2 source
0000770E   E761 0000 0806                 00000000   5273+         VL    v22,0(R1)             use v22 to test decoder
00007714   E310 5014 0014                 00000014   5274+         LGF   R1,V3ADDR             load v3 source
0000771A   E771 0000 0806                 00000000   5275+         VL    v23,0(R1)             use v23 to test decoder
00007720   E310 5018 0014                 00000018   5276+         LGF   R1,V4ADDR             load v4 source
00007726   E781 0000 0806                 00000000   5277+         VL    v24,0(R1)             use v24 to test decoder
0000772C   E766 7100 8FAF                             5278+         VMAO  V22,V22,V23,V24,1     test instruction (dest is a source)
00007732   E760 5030 080E                 000076F0   5279+         VST   V22,V10137            save v1 output
00007738   07FB                                       5280+         BR    R11                   return
0000773C                                             5281+RE137    DC   0F                     xl16 expected result
0000773C                                             5282+         DROP  R5
0000773C   FF0B1B14 05377748                         5283         DC   XL16'FF0B1B1405377748 0984139C0DF0F010'     result
00007744   0984139C 0DF0F010
0000774C   FF020304 05060708                         5284         DC   XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
00007754   090A0B0C 0D0E0F10
0000775C   FF020304 05060708                         5285         DC   XL16'FF02030405060708 090A0B0C0D0E0F10'     v3
00007764   090A0B0C 0D0E0F10
0000776C   FF020304 05060708                         5286         DC   XL16'FF02030405060708 090A0B0C0D0E0F10'     v4
00007774   090A0B0C 0D0E0F10
                                                     5287
                                                     5288              VRR_D VMAO,1
00007780                                             5289+         DS   0FD
00007780                        00007780            5290+         USING *,R5              base for test data and test routine
00007780   000077C8                                 5291+T138     DC   A(X138)                address of test routine
00007784   008A                                      5292+         DC   H'138'                 test number
00007786   00                                        5293+         DC   X'00'
00007787   01                                        5294+         DC   HL1'1'                 m5
00007788   E5D4C1D6 40404040                         5295+         DC   CL8'VMAO'              instruction name
00007790   0000780C                                  5296+         DC   A(RE138+16)            address of v2 source
00007794   0000781C                                  5297+         DC   A(RE138+32)            address of v3 source
00007798   0000782C                                  5298+         DC   A(RE138+48)            address of v4 source
0000779C   00000010                                  5299+         DC   A(16)                  result length
000077A0   000077FC                                  5300+REA138   DC   A(RE138)               result address
000077A8   00000000 00000000                         5301+         DS   FD                     gap
000077B0   00000000 00000000                         5302+V10138   DS   XL16                   V1 output
000077B8   00000000 00000000
000077C0   00000000 00000000                         5303+         DS   FD                     gap
                                                     5304+*
000077C8                                             5305+X138     DS   0F
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  LOC        OBJECT CODE       ADDR1    ADDR2    STMT

000077C8  E310 5010 0014             00000010  5306+          LGF    R1,V2ADDR       load v2 source
000077CE  E761 0000 0806             00000000  5307+          VL     v22,0(R1)       use v22 to test decoder
000077D4  E310 5014 0014             00000014  5308+          LGF    R1,V3ADDR       load v3 source
000077DA  E771 0000 0806             00000000  5309+          VL     v23,0(R1)       use v23 to test decoder
000077E0  E310 5018 0014             00000018  5310+          LGF    R1,V4ADDR       load v4 source
000077E6  E781 0000 0806             00000000  5311+          VL     v24,0(R1)       use v24 to test decoder
000077EC  E766 7100 8FAF                       5312+          VMAO   V22,V22,V23,V24,1    test instruction (dest is a source)
000077F2  E760 5030 080E             000077B0  5313+          VST    V22,V10138      save v1 output
000077F8  07FB                                 5314+          BR     R11             return
000077FC                                       5315+RE138     DC     0F              xl16 expected result
000077FC                                       5316+          DROP   R5
000077FC  FF050D0C 051B3B28                    5317           DC     XL16'FF050D0C051B3B28 094189540D77F790'    result
00007804  09418954 0D77F790
0000780C  FF020304 05060708                    5318           DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
00007814  090A0B0C 0D0E0F10
0000781C  FF010102 02030304                    5319           DC     XL16'FF01010202030304 0405050606070708'    v3
00007824  04050506 06070708
0000782C  FF020304 05060708                    5320           DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v4
00007834  090A0B0C 0D0E0F10

                                               5321
                                               5322           VRR_D  VMAO,1
00007840                                       5323+          DS     0FD
00007840                    00007840           5324+          USING  *,R5            base for test data and test routine
00007840  00007888                             5325+T139      DC     A(X139)         address of test routine
00007844  008B                                 5326+          DC     H'139'          test number
00007846  00                                   5327+          DC     X'00'
00007847  01                                   5328+          DC     HL1'1'          m5
00007848  E5D4C1D6 40404040                    5329+          DC     CL8'VMAO'       instruction name
00007850  000078CC                             5330+          DC     A(RE139+16)     address of v2 source
00007854  000078DC                             5331+          DC     A(RE139+32)     address of v3 source
00007858  000078EC                             5332+          DC     A(RE139+48)     address of v4 source
0000785C  00000010                             5333+          DC     A(16)           result length
00007860  000078BC                             5334+REA139    DC     A(RE139)        result address
00007868  00000000 00000000                    5335+          DS     FD              gap
00007870  00000000 00000000                    5336+V10139    DS     XL16            V1 output
00007878  00000000 00000000
00007880  00000000 00000000                    5337+          DS     FD              gap
                                               5338+*
00007888                                       5339+X139      DS     0F
00007888  E310 5010 0014             00000010  5340+          LGF    R1,V2ADDR       load v2 source
0000788E  E761 0000 0806             00000000  5341+          VL     v22,0(R1)       use v22 to test decoder
00007894  E310 5014 0014             00000014  5342+          LGF    R1,V3ADDR       load v3 source
0000789A  E771 0000 0806             00000000  5343+          VL     v23,0(R1)       use v23 to test decoder
000078A0  E310 5018 0014             00000018  5344+          LGF    R1,V4ADDR       load v4 source
000078A6  E781 0000 0806             00000000  5345+          VL     v24,0(R1)       use v24 to test decoder
000078AC  E766 7100 8FAF                       5346+          VMAO   V22,V22,V23,V24,1    test instruction (dest is a source)
000078B2  E760 5030 080E             00007870  5347+          VST    V22,V10139      save v1 output
000078B8  07FB                                 5348+          BR     R11             return
000078BC                                       5349+RE139     DC     0F              xl16 expected result
000078BC                                       5350+          DROP   R5
000078BC  FF020304 05060E10                    5351           DC     XL16'FF02030405060E10 091522180D1D3D30'    result
000078C4  09152218 0D1D3D30
000078CC  FF020304 05060708                    5352           DC     XL16'FF02030405060708 090A0B0C0D0E0F10'    v2
000078D4  090A0B0C 0D0E0F10
000078DC  FF000000 00000001                    5353           DC     XL16'FF00000000000001 0101010101010102'    v3
000078E4  01010101 01010102
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000078EC	FF020304 05060708			5354		DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
000078F4	090A0B0C 0D0E0F10							
				5355				
				5356	* Word			
				5357		VRR_D	VMAO,2	
00007900				5358+		DS	0FD	
00007900		00007900		5359+		USING	*,R5	base for test data and test routine
00007900	00007948			5360+T140		DC	A(X140)	address of test routine
00007904	008C			5361+		DC	H'140'	test number
00007906	00			5362+		DC	X'00'	
00007907	02			5363+		DC	HL1'2'	m5
00007908	E5D4C1D6 40404040			5364+		DC	CL8'VMAO'	instruction name
00007910	0000798C			5365+		DC	A(RE140+16)	address of v2 source
00007914	0000799C			5366+		DC	A(RE140+32)	address of v3 source
00007918	000079AC			5367+		DC	A(RE140+48)	address of v4 source
0000791C	00000010			5368+		DC	A(16)	result length
00007920	0000797C			5369+REA140		DC	A(RE140)	result address
00007928	00000000 00000000			5370+		DS	FD	gap
00007930	00000000 00000000			5371+V10140		DS	XL16	V1 output
00007938	00000000 00000000							
00007940	00000000 00000000			5372+		DS	FD	gap
				5373+*				
00007948				5374+X140		DS	0F	
00007948	E310 5010 0014		00000010	5375+		LGF	R1,V2ADDR	load v2 source
0000794E	E761 0000 0806		00000000	5376+		VL	v22,0(R1)	use v22 to test decoder
00007954	E310 5014 0014		00000014	5377+		LGF	R1,V3ADDR	load v3 source
0000795A	E771 0000 0806		00000000	5378+		VL	v23,0(R1)	use v23 to test decoder
00007960	E310 5018 0014		00000018	5379+		LGF	R1,V4ADDR	load v4 source
00007966	E781 0000 0806		00000000	5380+		VL	v24,0(R1)	use v24 to test decoder
0000796C	E766 7200 8FAF			5381+		VMAO	V22,V22,V23,V24,2	test instruction (dest is a source)
00007972	E760 5030 080E		00007930	5382+		VST	V22,V10140	save v1 output
00007978	07FB			5383+		BR	R11	return
0000797C				5384+RE140		DC	0F	xl16 expected result
0000797C				5385+		DROP	R5	
0000797C	00000000 00000271			5386		DC	XL16'0000000000000271 000000000000F424'	result
00007984	00000000 0000F424							
0000798C	FF000000 00000019			5387		DC	XL16'FF00000000000019 00000038000000FA'	v2
00007994	00000038 000000FA							
0000799C	FF000000 00000019			5388		DC	XL16'FF00000000000019 00000038000000FA'	v3
000079A4	00000038 000000FA							
000079AC	00000000 00000000			5389		DC	XL16'0000000000000000 0000000000000000'	v4
000079B4	00000000 00000000							
				5390				
				5391		VRR_D	VMAO,2	
000079C0				5392+		DS	0FD	
000079C0		000079C0		5393+		USING	*,R5	base for test data and test routine
000079C0	00007A08			5394+T141		DC	A(X141)	address of test routine
000079C4	008D			5395+		DC	H'141'	test number
000079C6	00			5396+		DC	X'00'	
000079C7	02			5397+		DC	HL1'2'	m5
000079C8	E5D4C1D6 40404040			5398+		DC	CL8'VMAO'	instruction name
000079D0	00007A4C			5399+		DC	A(RE141+16)	address of v2 source
000079D4	00007A5C			5400+		DC	A(RE141+32)	address of v3 source
000079D8	00007A6C			5401+		DC	A(RE141+48)	address of v4 source
000079DC	00000010			5402+		DC	A(16)	result length
000079E0	00007A3C			5403+REA141		DC	A(RE141)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000079E8	00000000 00000000			5404+	DS	FD	gap
000079F0	00000000 00000000			5405+V10141	DS	XL16	V1 output
000079F8	00000000 00000000						
00007A00	00000000 00000000			5406+	DS	FD	gap
				5407+*			
00007A08				5408+X141	DS	0F	
00007A08	E310 5010 0014		00000010	5409+	LGF	R1,V2ADDR	load v2 source
00007A0E	E761 0000 0806		00000000	5410+	VL	v22,0(R1)	use v22 to test decoder
00007A14	E310 5014 0014		00000014	5411+	LGF	R1,V3ADDR	load v3 source
00007A1A	E771 0000 0806		00000000	5412+	VL	v23,0(R1)	use v23 to test decoder
00007A20	E310 5018 0014		00000018	5413+	LGF	R1,V4ADDR	load v4 source
00007A26	E781 0000 0806		00000000	5414+	VL	v24,0(R1)	use v24 to test decoder
00007A2C	E766 7200 8FAF			5415+	VMAO	V22,V22,V23,V24,2	test instruction (dest is a source)
00007A32	E760 5030 080E		000079F0	5416+	VST	V22,V10141	save v1 output
00007A38	07FB			5417+	BR	R11	return
00007A3C				5418+RE141	DC	0F	xl16 expected result
00007A3C				5419+	DROP	R5	
00007A3C	00020001 000006C0			5420	DC	XL16'00020001000006C0 000000030000F426'	result
00007A44	00000003 0000F426						
00007A4C	FF0000FF 00000029			5421	DC	XL16'FF0000FF00000029 00000038000000FA'	v2
00007A54	00000038 000000FA						
00007A5C	FF000001 00000029			5422	DC	XL16'FF00000100000029 00000038000000FA'	v3
00007A64	00000038 000000FA						
00007A6C	00020001 0000002F			5423	DC	XL16'000200010000002F 0000000300000002'	v4
00007A74	00000003 00000002						
				5424			
				5425	VRR_D	VMAO,2	
00007A80				5426+	DS	0FD	
00007A80		00007A80		5427+	USING	*,R5	base for test data and test routine
00007A80	00007AC8			5428+T142	DC	A(X142)	address of test routine
00007A84	008E			5429+	DC	H'142'	test number
00007A86	00			5430+	DC	X'00'	
00007A87	02			5431+	DC	HL1'2'	m5
00007A88	E5D4C1D6 40404040			5432+	DC	CL8'VMAO'	instruction name
00007A90	00007B0C			5433+	DC	A(RE142+16)	address of v2 source
00007A94	00007B1C			5434+	DC	A(RE142+32)	address of v3 source
00007A98	00007B2C			5435+	DC	A(RE142+48)	address of v4 source
00007A9C	00000010			5436+	DC	A(16)	result length
00007AA0	00007AFC			5437+REA142	DC	A(RE142)	result address
00007AA8	00000000 00000000			5438+	DS	FD	gap
00007AB0	00000000 00000000			5439+V10142	DS	XL16	V1 output
00007AB8	00000000 00000000						
00007AC0	00000000 00000000			5440+	DS	FD	gap
				5441+*			
00007AC8				5442+X142	DS	0F	
00007AC8	E310 5010 0014		00000010	5443+	LGF	R1,V2ADDR	load v2 source
00007ACE	E761 0000 0806		00000000	5444+	VL	v22,0(R1)	use v22 to test decoder
00007AD4	E310 5014 0014		00000014	5445+	LGF	R1,V3ADDR	load v3 source
00007ADA	E771 0000 0806		00000000	5446+	VL	v23,0(R1)	use v23 to test decoder
00007AE0	E310 5018 0014		00000018	5447+	LGF	R1,V4ADDR	load v4 source
00007AE6	E781 0000 0806		00000000	5448+	VL	v24,0(R1)	use v24 to test decoder
00007AEC	E766 7200 8FAF			5449+	VMAO	V22,V22,V23,V24,2	test instruction (dest is a source)
00007AF2	E760 5030 080E		00007AB0	5450+	VST	V22,V10142	save v1 output
00007AF8	07FB			5451+	BR	R11	return
00007AFC				5452+RE142	DC	0F	xl16 expected result
00007AFC				5453+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007AFC	FF1B3F6E A9977748			5454	DC	XL16'FF1B3F6EA9977748 09B4795953B0F010'	result
00007B04	09B47959 53B0F010						
00007B0C	FF020304 05060708			5455	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00007B14	090A0B0C 0D0E0F10						
00007B1C	FF020304 05060708			5456	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3
00007B24	090A0B0C 0D0E0F10						
00007B2C	FF020304 05060708			5457	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00007B34	090A0B0C 0D0E0F10						
				5458			
				5459	VRR_D	VMA0,2	
00007B40				5460+	DS	0FD	
00007B40		00007B40		5461+	USING	*,R5	base for test data and test routine
00007B40	00007B88			5462+T143	DC	A(X143)	address of test routine
00007B44	008F			5463+	DC	H'143'	test number
00007B46	00			5464+	DC	X'00'	
00007B47	02			5465+	DC	HL1'2'	m5
00007B48	E5D4C1D6 40404040			5466+	DC	CL8'VMA0'	instruction name
00007B50	00007BCC			5467+	DC	A(RE143+16)	address of v2 source
00007B54	00007BDC			5468+	DC	A(RE143+32)	address of v3 source
00007B58	00007BEC			5469+	DC	A(RE143+48)	address of v4 source
00007B5C	00000010			5470+	DC	A(16)	result length
00007B60	00007BBC			5471+REA143	DC	A(RE143)	result address
00007B68	00000000 00000000			5472+	DS	FD	gap
00007B70	00000000 00000000			5473+V10143	DS	XL16	V1 output
00007B78	00000000 00000000						
00007B80	00000000 00000000			5474+	DS	FD	gap
				5475+*			
00007B88				5476+X143	DS	0F	
00007B88	E310 5010 0014		00000010	5477+	LGF	R1,V2ADDR	load v2 source
00007B8E	E761 0000 0806		00000000	5478+	VL	v22,0(R1)	use v22 to test decoder
00007B94	E310 5014 0014		00000014	5479+	LGF	R1,V3ADDR	load v3 source
00007B9A	E771 0000 0806		00000000	5480+	VL	v23,0(R1)	use v23 to test decoder
00007BA0	E310 5018 0014		00000018	5481+	LGF	R1,V4ADDR	load v4 source
00007BA6	E781 0000 0806		00000000	5482+	VL	v24,0(R1)	use v24 to test decoder
00007BAC	E766 7200 8FAF			5483+	VMA0	V22,V22,V23,V24,2	test instruction (dest is a source)
00007BB2	E760 5030 080E		00007B70	5484+	VST	V22,V10143	save v1 output
00007BB8	07FB			5485+	BR	R11	return
00007BBC				5486+RE143	DC	0F	xl16 expected result
00007BBC				5487+	DROP	R5	
00007BBC	FF0C1E33 504B3B28			5488	DC	XL16'FF0C1E33504B3B28 0958BB24A157F790'	result
00007BC4	0958BB24 A157F790						
00007BCC	FF020304 05060708			5489	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00007BD4	090A0B0C 0D0E0F10						
00007BDC	FF010102 02030304			5490	DC	XL16'FF01010202030304 0405050606070708'	v3
00007BE4	04050506 06070708						
00007BEC	FF020304 05060708			5491	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v4
00007BF4	090A0B0C 0D0E0F10						
				5492			
				5493	VRR_D	VMA0,2	
00007C00				5494+	DS	0FD	
00007C00		00007C00		5495+	USING	*,R5	base for test data and test routine
00007C00	00007C48			5496+T144	DC	A(X144)	address of test routine
00007C04	0090			5497+	DC	H'144'	test number
00007C06	00			5498+	DC	X'00'	
00007C07	02			5499+	DC	HL1'2'	m5
00007C08	E5D4C1D6 40404040			5500+	DC	CL8'VMA0'	instruction name

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00007C10   00007C8C                              5501+          DC     A(RE144+16)       address of v2 source
00007C14   00007C9C                              5502+          DC     A(RE144+32)       address of v3 source
00007C18   00007CAC                              5503+          DC     A(RE144+48)       address of v4 source
00007C1C   00000010                              5504+          DC     A(16)             result length
00007C20   00007C7C                              5505+REA144    DC     A(RE144)          result address
00007C28   00000000 00000000                     5506+          DS     FD                gap
00007C30   00000000 00000000                     5507+V10144    DS     XL16              V1 output
00007C38   00000000 00000000
00007C40   00000000 00000000                     5508+          DS     FD                gap
                                                 5509+*
00007C48                                         5510+X144      DS     0F
00007C48   E310 5010 0014              00000010  5511+          LGF    R1,V2ADDR         load v2 source
00007C4E   E761 0000 0806              00000000  5512+          VL     v22,0(R1)         use v22 to test decoder
00007C54   E310 5014 0014              00000014  5513+          LGF    R1,V3ADDR         load v3 source
00007C5A   E771 0000 0806              00000000  5514+          VL     v23,0(R1)         use v23 to test decoder
00007C60   E310 5018 0014              00000018  5515+          LGF    R1,V4ADDR         load v4 source
00007C66   E781 0000 0806              00000000  5516+          VL     v24,0(R1)         use v24 to test decoder
00007C6C   E766 7200 8FAF                        5517+          VMAO   V22,V22,V23,V24,2   test instruction (dest is a source)
00007C72   E760 5030 080E              00007C30  5518+          VST    V22,V10144         save v1 output
00007C78   07FB                                  5519+          BR     R11               return
00007C7C                                         5520+RE144     DC     0F                xl16 expected result
00007C7C                                         5521+          DROP   R5
00007C7C   FF020304 0A0C0E10                     5522           DC     XL16'FF0203040A0C0E10 09172636 54493D30'       result
00007C84   09172636 54493D30
00007C8C   FF020304 05060708                     5523           DC     XL16'FF02030405060708 090A0B0C0D0E0F10'       v2
00007C94   090A0B0C 0D0E0F10
00007C9C   FF000000 00000001                     5524           DC     XL16'FF00000000000001 0101010101010102'       v3
00007CA4   01010101 01010102
00007CAC   FF020304 05060708                     5525           DC     XL16'FF02030405060708 090A0B0C0D0E0F10'       v4
00007CB4   090A0B0C 0D0E0F10
                                                 5526
                                                 5527 * Doubleword
                                                 5528           VRR_D  VMAO,3
00007CC0                                         5529+          DS     0FD
00007CC0                         00007CC0        5530+          USING  *,R5             base for test data and test routine
00007CC0   00007D08                              5531+T145      DC     A(X145)           address of test routine
00007CC4   0091                                  5532+          DC     H'145'            test number
00007CC6   00                                    5533+          DC     X'00'
00007CC7   03                                    5534+          DC     HL1'3'            m5
00007CC8   E5D4C1D6 40404040                     5535+          DC     CL8'VMAO'         instruction name
00007CD0   00007D4C                              5536+          DC     A(RE145+16)       address of v2 source
00007CD4   00007D5C                              5537+          DC     A(RE145+32)       address of v3 source
00007CD8   00007D6C                              5538+          DC     A(RE145+48)       address of v4 source
00007CDC   00000010                              5539+          DC     A(16)             result length
00007CE0   00007D3C                              5540+REA145    DC     A(RE145)          result address
00007CE8   00000000 00000000                     5541+          DS     FD                gap
00007CF0   00000000 00000000                     5542+V10145    DS     XL16              V1 output
00007CF8   00000000 00000000
00007D00   00000000 00000000                     5543+          DS     FD                gap
                                                 5544+*
00007D08                                         5545+X145      DS     0F
00007D08   E310 5010 0014              00000010  5546+          LGF    R1,V2ADDR         load v2 source
00007D0E   E761 0000 0806              00000000  5547+          VL     v22,0(R1)         use v22 to test decoder
00007D14   E310 5014 0014              00000014  5548+          LGF    R1,V3ADDR         load v3 source
00007D1A   E771 0000 0806              00000000  5549+          VL     v23,0(R1)         use v23 to test decoder
00007D20   E310 5018 0014              00000018  5550+          LGF    R1,V4ADDR         load v4 source
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007D26	E781 0000 0806		00000000	5551+	VL	v24,0(R1)	use v24 to test decoder
00007D2C	E766 7300 8FAF			5552+	VMA0	V22,V22,V23,V24,3	test instruction (dest is a source)
00007D32	E760 5030 080E		00007CF0	5553+	VST	V22,V10145	save v1 output
00007D38	07FB			5554+	BR	R11	return
00007D3C				5555+RE145	DC	0F	xl16 expected result
00007D3C				5556+	DROP	R5	
00007D3C	00000000 00000C77			5557	DC	XL16'0000000000000C77 96789F9F4FEDCC24'	result
00007D44	96789F9F 4FEDCC24						
00007D4C	FFFFFFFF 00019000			5558	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00007D54	00000038 EEEEEEFA						
00007D5C	FFFFFFFF 00019000			5559	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00007D64	00000038 0EEEEEFA						
00007D6C	00000000 00000000			5560	DC	XL16'0000000000000000 0000000000000000'	v4
00007D74	00000000 00000000						
				5561			
				5562	VRR_D	VMA0,3	
00007D80				5563+	DS	0FD	
00007D80		00007D80		5564+	USING	*,R5	base for test data and test routine
00007D80	00007DC8			5565+T146	DC	A(X146)	address of test routine
00007D84	0092			5566+	DC	H'146'	test number
00007D86	00			5567+	DC	X'00'	
00007D87	03			5568+	DC	HL1'3'	m5
00007D88	E5D4C1D6 40404040			5569+	DC	CL8'VMA0'	instruction name
00007D90	00007E0C			5570+	DC	A(RE146+16)	address of v2 source
00007D94	00007E1C			5571+	DC	A(RE146+32)	address of v3 source
00007D98	00007E2C			5572+	DC	A(RE146+48)	address of v4 source
00007D9C	00000010			5573+	DC	A(16)	result length
00007DA0	00007DFC			5574+REA146	DC	A(RE146)	result address
00007DA8	00000000 00000000			5575+	DS	FD	gap
00007DB0	00000000 00000000			5576+V10146	DS	XL16	V1 output
00007DB8	00000000 00000000						
00007DC0	00000000 00000000			5577+	DS	FD	gap
				5578+*			
00007DC8				5579+X146	DS	0F	
00007DC8	E310 5010 0014		00000010	5580+	LGF	R1,V2ADDR	load v2 source
00007DCE	E761 0000 0806		00000000	5581+	VL	v22,0(R1)	use v22 to test decoder
00007DD4	E310 5014 0014		00000014	5582+	LGF	R1,V3ADDR	load v3 source
00007DDA	E771 0000 0806		00000000	5583+	VL	v23,0(R1)	use v23 to test decoder
00007DE0	E310 5018 0014		00000018	5584+	LGF	R1,V4ADDR	load v4 source
00007DE6	E781 0000 0806		00000000	5585+	VL	v24,0(R1)	use v24 to test decoder
00007DEC	E766 7300 8FAF			5586+	VMA0	V22,V22,V23,V24,3	test instruction (dest is a source)
00007DF2	E760 5030 080E		00007DB0	5587+	VST	V22,V10146	save v1 output
00007DF8	07FB			5588+	BR	R11	return
00007DFC				5589+RE146	DC	0F	xl16 expected result
00007DFC				5590+	DROP	R5	
00007DFC	7051B52F 8692B4F6			5591	DC	XL16'7051B52F8692B4F6 152B55D498D421F1'	result
00007E04	152B55D4 98D421F1						
00007E0C	FF020304 05060750			5592	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00007E14	090A0B0C 0D0E0F7F						
00007E1C	01020304 05060750			5593	DC	XL16'0102030405060750 090A0B780D0E0F7F'	v3
00007E24	090A0B78 0D0E0F7F						
00007E2C	70000000 00000000			5594	DC	XL16'7000000000000000 0000000000000F0'	v4
00007E34	00000000 000000F0						
				5595			
				5596	VRR_D	VMA0,3	
00007E40				5597+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007E40		00007E40		5598+	USING	*,R5	base for test data and test routine
00007E40	00007E88			5599+T147	DC	A(X147)	address of test routine
00007E44	0093			5600+	DC	H'147'	test number
00007E46	00			5601+	DC	X'00'	
00007E47	03			5602+	DC	HL1'3'	m5
00007E48	E5D4C1D6 40404040			5603+	DC	CL8'VMAO'	instruction name
00007E50	00007ECC			5604+	DC	A(RE147+16)	address of v2 source
00007E54	00007EDC			5605+	DC	A(RE147+32)	address of v3 source
00007E58	00007EEC			5606+	DC	A(RE147+48)	address of v4 source
00007E5C	00000010			5607+	DC	A(16)	result length
00007E60	00007EBC			5608+REA147	DC	A(RE147)	result address
00007E68	00000000 00000000			5609+	DS	FD	gap
00007E70	00000000 00000000			5610+V10147	DS	XL16	V1 output
00007E78	00000000 00000000						
00007E80	00000000 00000000			5611+	DS	FD	gap
				5612+*			
00007E88				5613+X147	DS	0F	
00007E88	E310 5010 0014		00000010	5614+	LGF	R1,V2ADDR	load v2 source
00007E8E	E761 0000 0806		00000000	5615+	VL	v22,0(R1)	use v22 to test decoder
00007E94	E310 5014 0014		00000014	5616+	LGF	R1,V3ADDR	load v3 source
00007E9A	E771 0000 0806		00000000	5617+	VL	v23,0(R1)	use v23 to test decoder
00007EA0	E310 5018 0014		00000018	5618+	LGF	R1,V4ADDR	load v4 source
00007EA6	E781 0000 0806		00000000	5619+	VL	v24,0(R1)	use v24 to test decoder
00007EAC	E766 7300 8FAF			5620+	VMAO	V22,V22,V23,V24,3	test instruction (dest is a source)
00007EB2	E760 5030 080E		00007E70	5621+	VST	V22,V10147	save v1 output
00007EB8	07FB			5622+	BR	R11	return
00007EBC				5623+RE147	DC	0F	xl16 expected result
00007EBC				5624+	DROP	R5	
00007EBC	0024558D B838C862			5625	DC	XL16'0024558DB838C862 B47CD8D5FF5B4940'	result
00007EC4	B47CD8D5 FF5B4940						
00007ECC	FF020304 05060750			5626	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00007ED4	090A0B0C 0D0E0F7F						
00007EDC	00010102 02030328			5627	DC	XL16'0001010202030328 0405053C0607073F'	v3
00007EE4	0405053C 0607073F						
00007EEC	FFFFFFFF FFFFFFFF			5628	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v4
00007EF4	FFFFFFFF FFFFFFFF						
				5629			
				5630	VRR_D	VMAO,3	
00007F00				5631+	DS	0FD	
00007F00		00007F00		5632+	USING	*,R5	base for test data and test routine
00007F00	00007F48			5633+T148	DC	A(X148)	address of test routine
00007F04	0094			5634+	DC	H'148'	test number
00007F06	00			5635+	DC	X'00'	
00007F07	03			5636+	DC	HL1'3'	m5
00007F08	E5D4C1D6 40404040			5637+	DC	CL8'VMAO'	instruction name
00007F10	00007F8C			5638+	DC	A(RE148+16)	address of v2 source
00007F14	00007F9C			5639+	DC	A(RE148+32)	address of v3 source
00007F18	00007FAC			5640+	DC	A(RE148+48)	address of v4 source
00007F1C	00000010			5641+	DC	A(16)	result length
00007F20	00007F7C			5642+REA148	DC	A(RE148)	result address
00007F28	00000000 00000000			5643+	DS	FD	gap
00007F30	00000000 00000000			5644+V10148	DS	XL16	V1 output
00007F38	00000000 00000000						
00007F40	00000000 00000000			5645+	DS	FD	gap
				5646+*			
00007F48				5647+X148	DS	0F	

```
  LOC        OBJECT CODE      ADDR1    ADDR2     STMT

00007F48  E310 5010 0014            00000010  5648+        LGF    R1,V2ADDR          load v2 source
00007F4E  E761 0000 0806            00000000  5649+        VL     v22,0(R1)          use v22 to test decoder
00007F54  E310 5014 0014            00000014  5650+        LGF    R1,V3ADDR          load v3 source
00007F5A  E771 0000 0806            00000000  5651+        VL     v23,0(R1)          use v23 to test decoder
00007F60  E310 5018 0014            00000018  5652+        LGF    R1,V4ADDR          load v4 source
00007F66  E781 0000 0806            00000000  5653+        VL     v24,0(R1)          use v24 to test decoder
00007F6C  E766 7300 8FAF                      5654+        VMAO   V22,V22,V23,V24,3    test instruction (dest is a source)
00007F72  E760 5030 080E            00007F30  5655+        VST    V22,V10148         save v1 output
00007F78  07FB                                5656+        BR     R11                return
00007F7C                                      5657+RE148   DC     0F                 xl16 expected result
00007F7C                                      5658+        DROP   R5
00007F7C  7009131E A8C3DFFE                   5659         DC     XL16'7009131EA8C3DFFE F91C345060616771'   result
00007F84  F91C3450 60616771
00007F8C  FF020304 05060750                   5660         DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00007F94  090A0B0C 0D0E0F7F
00007F9C  00000000 0000000A                   5661         DC     XL16'000000000000000A 0101010F0101010F'   v3
00007FA4  0101010F 0101010F
00007FAC  70000000 00000000                   5662         DC     XL16'7000000000000000 F000000000000000'   v4
00007FB4  F0000000 00000000
                                              5663
                                              5664         VRR_D  VMAO,3
00007FC0                                      5665+        DS     0FD
00007FC0                          00007FC0    5666+        USING  *,R5               base for test data and test routine
00007FC0  00008008                            5667+T149    DC     A(X149)            address of test routine
00007FC4  0095                                5668+        DC     H'149'             test number
00007FC6  00                                  5669+        DC     X'00'
00007FC7  03                                  5670+        DC     HL1'3'             m5
00007FC8  E5D4C1D6 40404040                   5671+        DC     CL8'VMAO'          instruction name
00007FD0  0000804C                            5672+        DC     A(RE149+16)        address of v2 source
00007FD4  0000805C                            5673+        DC     A(RE149+32)        address of v3 source
00007FD8  0000806C                            5674+        DC     A(RE149+48)        address of v4 source
00007FDC  00000010                            5675+        DC     A(16)              result length
00007FE0  0000803C                            5676+REA149  DC     A(RE149)           result address
00007FE8  00000000 00000000                   5677+        DS     FD                 gap
00007FF0  00000000 00000000                   5678+V10149  DS     XL16               V1 output
00007FF8  00000000 00000000
00008000  00000000 00000000                   5679+        DS     FD                 gap
                                              5680+*
00008008                                      5681+X149    DS     0F
00008008  E310 5010 0014            00000010  5682+        LGF    R1,V2ADDR          load v2 source
0000800E  E761 0000 0806            00000000  5683+        VL     v22,0(R1)          use v22 to test decoder
00008014  E310 5014 0014            00000014  5684+        LGF    R1,V3ADDR          load v3 source
0000801A  E771 0000 0806            00000000  5685+        VL     v23,0(R1)          use v23 to test decoder
00008020  E310 5018 0014            00000018  5686+        LGF    R1,V4ADDR          load v4 source
00008026  E781 0000 0806            00000000  5687+        VL     v24,0(R1)          use v24 to test decoder
0000802C  E766 7300 8FAF                      5688+        VMAO   V22,V22,V23,V24,3    test instruction (dest is a source)
00008032  E760 5030 080E            00007FF0  5689+        VST    V22,V10149         save v1 output
00008038  07FB                                5690+        BR     R11                return
0000803C                                      5691+RE149   DC     0F                 xl16 expected result
0000803C                                      5692+        DROP   R5
0000803C  FFFFFFFF FFFFFFFF                   5693         DC     XL16'FFFFFFFFFFFFFFFF F6141E28323C491C'   result
00008044  F6141E28 323C491C
0000804C  090A0B0C 0D0E0F7F                   5694         DC     XL16'090A0B0C0D0E0F7F FF02030405060750'   v2
00008054  FF020304 05060750
0000805C  0101010F 0101010F                   5695         DC     XL16'0101010F0101010F 000000000000000A'   v3
00008064  00000000 0000000A
```

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  LOC           OBJECT CODE       ADDR1     ADDR2     STMT

0000806C  FFFFFFFF FFFFFFFF                          5696           DC    XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFC'    v4
00008074  FFFFFFFF FFFFFFFC
                                                     5697
                                                     5698
0000807C  00000000                                   5699           DC    F'0'       END OF TABLE
00008080  00000000                                   5700           DC    F'0'
                                                     5701 *
                                                     5702 * table of pointers to individual load test
                                                     5703 *
00008084                                             5704 E7TESTS  DS    0F
                                                     5705           PTTABLE
00008084                                             5706+TTABLE   DS    0F
00008084  000010C0                                   5707+         DC    A(T1)
00008088  00001180                                   5708+         DC    A(T2)
0000808C  00001240                                   5709+         DC    A(T3)
00008090  00001300                                   5710+         DC    A(T4)
00008094  000013C0                                   5711+         DC    A(T5)
00008098  00001480                                   5712+         DC    A(T6)
0000809C  00001540                                   5713+         DC    A(T7)
000080A0  00001600                                   5714+         DC    A(T8)
000080A4  000016C0                                   5715+         DC    A(T9)
000080A8  00001780                                   5716+         DC    A(T10)
000080AC  00001840                                   5717+         DC    A(T11)
000080B0  00001900                                   5718+         DC    A(T12)
000080B4  000019C0                                   5719+         DC    A(T13)
000080B8  00001A80                                   5720+         DC    A(T14)
000080BC  00001B40                                   5721+         DC    A(T15)
000080C0  00001C00                                   5722+         DC    A(T16)
000080C4  00001CC0                                   5723+         DC    A(T17)
000080C8  00001D80                                   5724+         DC    A(T18)
000080CC  00001E40                                   5725+         DC    A(T19)
000080D0  00001F00                                   5726+         DC    A(T20)
000080D4  00001FC0                                   5727+         DC    A(T21)
000080D8  00002080                                   5728+         DC    A(T22)
000080DC  00002140                                   5729+         DC    A(T23)
000080E0  00002200                                   5730+         DC    A(T24)
000080E4  000022C0                                   5731+         DC    A(T25)
000080E8  00002380                                   5732+         DC    A(T26)
000080EC  00002440                                   5733+         DC    A(T27)
000080F0  00002500                                   5734+         DC    A(T28)
000080F4  000025C0                                   5735+         DC    A(T29)
000080F8  00002680                                   5736+         DC    A(T30)
000080FC  00002740                                   5737+         DC    A(T31)
00008100  00002800                                   5738+         DC    A(T32)
00008104  000028C0                                   5739+         DC    A(T33)
00008108  00002980                                   5740+         DC    A(T34)
0000810C  00002A40                                   5741+         DC    A(T35)
00008110  00002B00                                   5742+         DC    A(T36)
00008114  00002BC0                                   5743+         DC    A(T37)
00008118  00002C80                                   5744+         DC    A(T38)
0000811C  00002D40                                   5745+         DC    A(T39)
00008120  00002E00                                   5746+         DC    A(T40)
00008124  00002EC0                                   5747+         DC    A(T41)
00008128  00002F80                                   5748+         DC    A(T42)
0000812C  00003040                                   5749+         DC    A(T43)
00008130  00003100                                   5750+         DC    A(T44)
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00008134	000031C0			5751+	DC	A(T45)
00008138	00003280			5752+	DC	A(T46)
0000813C	00003340			5753+	DC	A(T47)
00008140	00003400			5754+	DC	A(T48)
00008144	000034C0			5755+	DC	A(T49)
00008148	00003580			5756+	DC	A(T50)
0000814C	00003640			5757+	DC	A(T51)
00008150	00003700			5758+	DC	A(T52)
00008154	000037C0			5759+	DC	A(T53)
00008158	00003880			5760+	DC	A(T54)
0000815C	00003940			5761+	DC	A(T55)
00008160	00003A00			5762+	DC	A(T56)
00008164	00003AC0			5763+	DC	A(T57)
00008168	00003B80			5764+	DC	A(T58)
0000816C	00003C40			5765+	DC	A(T59)
00008170	00003D00			5766+	DC	A(T60)
00008174	00003DC0			5767+	DC	A(T61)
00008178	00003E80			5768+	DC	A(T62)
0000817C	00003F40			5769+	DC	A(T63)
00008180	00004000			5770+	DC	A(T64)
00008184	000040C0			5771+	DC	A(T65)
00008188	00004180			5772+	DC	A(T66)
0000818C	00004240			5773+	DC	A(T67)
00008190	00004300			5774+	DC	A(T68)
00008194	000043C0			5775+	DC	A(T69)
00008198	00004480			5776+	DC	A(T70)
0000819C	00004540			5777+	DC	A(T71)
000081A0	00004600			5778+	DC	A(T72)
000081A4	000046C0			5779+	DC	A(T73)
000081A8	00004780			5780+	DC	A(T74)
000081AC	00004840			5781+	DC	A(T75)
000081B0	00004900			5782+	DC	A(T76)
000081B4	000049C0			5783+	DC	A(T77)
000081B8	00004A80			5784+	DC	A(T78)
000081BC	00004B40			5785+	DC	A(T79)
000081C0	00004C00			5786+	DC	A(T80)
000081C4	00004CC0			5787+	DC	A(T81)
000081C8	00004D80			5788+	DC	A(T82)
000081CC	00004E40			5789+	DC	A(T83)
000081D0	00004F00			5790+	DC	A(T84)
000081D4	00004FC0			5791+	DC	A(T85)
000081D8	00005080			5792+	DC	A(T86)
000081DC	00005140			5793+	DC	A(T87)
000081E0	00005200			5794+	DC	A(T88)
000081E4	000052C0			5795+	DC	A(T89)
000081E8	00005380			5796+	DC	A(T90)
000081EC	00005440			5797+	DC	A(T91)
000081F0	00005500			5798+	DC	A(T92)
000081F4	000055C0			5799+	DC	A(T93)
000081F8	00005680			5800+	DC	A(T94)
000081FC	00005740			5801+	DC	A(T95)
00008200	00005800			5802+	DC	A(T96)
00008204	000058C0			5803+	DC	A(T97)
00008208	00005980			5804+	DC	A(T98)
0000820C	00005A40			5805+	DC	A(T99)
00008210	00005B00			5806+	DC	A(T100)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008214	00005BC0			5807+	DC	A(T101)	
00008218	00005C80			5808+	DC	A(T102)	
0000821C	00005D40			5809+	DC	A(T103)	
00008220	00005E00			5810+	DC	A(T104)	
00008224	00005EC0			5811+	DC	A(T105)	
00008228	00005F80			5812+	DC	A(T106)	
0000822C	00006040			5813+	DC	A(T107)	
00008230	00006100			5814+	DC	A(T108)	
00008234	000061C0			5815+	DC	A(T109)	
00008238	00006280			5816+	DC	A(T110)	
0000823C	00006340			5817+	DC	A(T111)	
00008240	00006400			5818+	DC	A(T112)	
00008244	000064C0			5819+	DC	A(T113)	
00008248	00006580			5820+	DC	A(T114)	
0000824C	00006640			5821+	DC	A(T115)	
00008250	00006700			5822+	DC	A(T116)	
00008254	000067C0			5823+	DC	A(T117)	
00008258	00006880			5824+	DC	A(T118)	
0000825C	00006940			5825+	DC	A(T119)	
00008260	00006A00			5826+	DC	A(T120)	
00008264	00006AC0			5827+	DC	A(T121)	
00008268	00006B80			5828+	DC	A(T122)	
0000826C	00006C40			5829+	DC	A(T123)	
00008270	00006D00			5830+	DC	A(T124)	
00008274	00006DC0			5831+	DC	A(T125)	
00008278	00006E80			5832+	DC	A(T126)	
0000827C	00006F40			5833+	DC	A(T127)	
00008280	00007000			5834+	DC	A(T128)	
00008284	000070C0			5835+	DC	A(T129)	
00008288	00007180			5836+	DC	A(T130)	
0000828C	00007240			5837+	DC	A(T131)	
00008290	00007300			5838+	DC	A(T132)	
00008294	000073C0			5839+	DC	A(T133)	
00008298	00007480			5840+	DC	A(T134)	
0000829C	00007540			5841+	DC	A(T135)	
000082A0	00007600			5842+	DC	A(T136)	
000082A4	000076C0			5843+	DC	A(T137)	
000082A8	00007780			5844+	DC	A(T138)	
000082AC	00007840			5845+	DC	A(T139)	
000082B0	00007900			5846+	DC	A(T140)	
000082B4	000079C0			5847+	DC	A(T141)	
000082B8	00007A80			5848+	DC	A(T142)	
000082BC	00007B40			5849+	DC	A(T143)	
000082C0	00007C00			5850+	DC	A(T144)	
000082C4	00007CC0			5851+	DC	A(T145)	
000082C8	00007D80			5852+	DC	A(T146)	
000082CC	00007E40			5853+	DC	A(T147)	
000082D0	00007F00			5854+	DC	A(T148)	
000082D4	00007FC0			5855+	DC	A(T149)	
				5856+*			
000082D8	00000000			5857+	DC	A(0)	END OF TABLE
000082DC	00000000			5858+	DC	A(0)	
				5859			
000082E0	00000000			5860	DC	F'0'	END OF TABLE
000082E4	00000000			5861	DC	F'0'	

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 LOC        OBJECT CODE      ADDR1      ADDR2      STMT

                                                   5863 ***********************************************************************
                                                   5864 *         Register equates
                                                   5865 ***********************************************************************

                            00000000   00000001    5867 R0          EQU    0
                            00000001   00000001    5868 R1          EQU    1
                            00000002   00000001    5869 R2          EQU    2
                            00000003   00000001    5870 R3          EQU    3
                            00000004   00000001    5871 R4          EQU    4
                            00000005   00000001    5872 R5          EQU    5
                            00000006   00000001    5873 R6          EQU    6
                            00000007   00000001    5874 R7          EQU    7
                            00000008   00000001    5875 R8          EQU    8
                            00000009   00000001    5876 R9          EQU    9
                            0000000A   00000001    5877 R10         EQU    10
                            0000000B   00000001    5878 R11         EQU    11
                            0000000C   00000001    5879 R12         EQU    12
                            0000000D   00000001    5880 R13         EQU    13
                            0000000E   00000001    5881 R14         EQU    14
                            0000000F   00000001    5882 R15         EQU    15




                                                   5884 ***********************************************************************
                                                   5885 *         Register equates
                                                   5886 ***********************************************************************

                            00000000   00000001    5888 V0          EQU    0
                            00000001   00000001    5889 V1          EQU    1
                            00000002   00000001    5890 V2          EQU    2
                            00000003   00000001    5891 V3          EQU    3
                            00000004   00000001    5892 V4          EQU    4
                            00000005   00000001    5893 V5          EQU    5
                            00000006   00000001    5894 V6          EQU    6
                            00000007   00000001    5895 V7          EQU    7
                            00000008   00000001    5896 V8          EQU    8
                            00000009   00000001    5897 V9          EQU    9
                            0000000A   00000001    5898 V10         EQU    10
                            0000000B   00000001    5899 V11         EQU    11
                            0000000C   00000001    5900 V12         EQU    12
                            0000000D   00000001    5901 V13         EQU    13
                            0000000E   00000001    5902 V14         EQU    14
                            0000000F   00000001    5903 V15         EQU    15
                            00000010   00000001    5904 V16         EQU    16
                            00000011   00000001    5905 V17         EQU    17
                            00000012   00000001    5906 V18         EQU    18
                            00000013   00000001    5907 V19         EQU    19
                            00000014   00000001    5908 V20         EQU    20
                            00000015   00000001    5909 V21         EQU    21
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
		00000016	00000001	5910	V22	EQU	22
		00000017	00000001	5911	V23	EQU	23
		00000018	00000001	5912	V24	EQU	24
		00000019	00000001	5913	V25	EQU	25
		0000001A	00000001	5914	V26	EQU	26
		0000001B	00000001	5915	V27	EQU	27
		0000001C	00000001	5916	V28	EQU	28
		0000001D	00000001	5917	V29	EQU	29
		0000001E	00000001	5918	V30	EQU	30
		0000001F	00000001	5919	V31	EQU	31
				5920			
				5921		END	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES											
BEGIN	I	00000200	2	165	131	161	162	163								
CTLR0	F	0000053C	4	394	175	176	177	178								
DECNUM	C	00001073	16	446	308	310	316	318								
E7TEST	4	00000000	72	460	257											
E7TESTS	F	00008084	4	5704	250											
EDIT	X	00001047	18	441	309	317										
ENDTEST	U	000003CE	1	294	255											
EOJ	I	00000520	4	384	210	243	297									
EOJPSW	D	00000510	8	382	384											
FAILCONT	U	000003BE	1	284												
FAILED	F	00001000	4	423	286	295										
FAILMSG	U	000003BA	1	278	268											
FAILPSW	D	00000528	8	386	388											
FAILTEST	I	00000538	4	388	298											
FB0001	F	00000280	8	194	198	199	201									
FB0002	F	00000330	8	227	231	232	234									
IMAGE	1	00000000	33512	0												
K	U	00000400	1	407	408	409	410									
K64	U	00010000	1	409												
M5	U	00000007	1	464	315											
MB	U	00100000	1	410												
MSG	I	00000458	4	344	209	242	327									
MSGCMD	C	000004A6	9	374	357	358										
MSGMSG	C	000004AF	95	375	351	372	349									
MSGMVC	I	000004A0	6	372	355											
MSGOK	I	0000046E	2	353	350											
MSGRET	I	0000048E	4	368	361	364										
MSGSAVE	F	00000494	4	371	347	368										
NEXTE7	U	00000384	1	252	271	289										
OPNAME	C	00000008	8	466	313											
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PRTLINE	C	00001008	16	429	436	326										
PRTLNG	U	0000003F	1	436	325											
PRTM5	C	00001044	2	434	319											
PRTNAME	C	00001033	8	432	313											
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
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R11	U	0000000B	1	5878	263	264	610	644	678	712	746	781	815	849	883	917	952
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES

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R13     U    0000000D    1   5880
R14     U    0000000E    1   5881
R15     U    0000000F    1   5882    279   304   331   332
R2      U    00000002    1   5869    209   242   307   308   315   316   324   327   328   345   347   353   354
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R3      U    00000003    1   5870
R4      U    00000004    1   5871
R5      U    00000005    1   5872    253   254   257   305   330   586   612   620   646   654   680   688   714
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R6      U    00000006    1   5873
R7      U    00000007    1   5874
R8      U    00000008    1   5875    161   165   166   167   169
R9      U    00000009    1   5876    162   169   170   172
RE1     F    0000113C    4    611    592   593   594   596
RE10    F    000017FC    4    918    899   900   901   903
RE100   F    00005B7C    4   4010   3991  3992  3993  3995
RE101   F    00005C3C    4   4044   4025  4026  4027  4029
RE102   F    00005CFC    4   4078   4059  4060  4061  4063
RE103   F    00005DBC    4   4112   4093  4094  4095  4097
RE104   F    00005E7C    4   4146   4127  4128  4129  4131
RE105   F    00005F3C    4   4181   4162  4163  4164  4166
RE106   F    00005FFC    4   4215   4196  4197  4198  4200
RE107   F    000060BC    4   4249   4230  4231  4232  4234
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
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RE109	F	0000623C	4	4317	4298	4299	4300	4302
RE11	F	000018BC	4	953	934	935	936	938
RE110	F	000062FC	4	4355	4336	4337	4338	4340
RE111	F	000063BC	4	4389	4370	4371	4372	4374
RE112	F	0000647C	4	4423	4404	4405	4406	4408
RE113	F	0000653C	4	4457	4438	4439	4440	4442
RE114	F	000065FC	4	4491	4472	4473	4474	4476
RE115	F	000066BC	4	4526	4507	4508	4509	4511
RE116	F	0000677C	4	4560	4541	4542	4543	4545
RE117	F	0000683C	4	4594	4575	4576	4577	4579
RE118	F	000068FC	4	4628	4609	4610	4611	4613
RE119	F	000069BC	4	4662	4643	4644	4645	4647
RE12	F	0000197C	4	987	968	969	970	972
RE120	F	00006A7C	4	4697	4678	4679	4680	4682
RE121	F	00006B3C	4	4731	4712	4713	4714	4716
RE122	F	00006BFC	4	4765	4746	4747	4748	4750
RE123	F	00006CBC	4	4799	4780	4781	4782	4784
RE124	F	00006D7C	4	4833	4814	4815	4816	4818
RE125	F	00006E3C	4	4868	4849	4850	4851	4853
RE126	F	00006EFC	4	4902	4883	4884	4885	4887
RE127	F	00006FBC	4	4936	4917	4918	4919	4921
RE128	F	0000707C	4	4970	4951	4952	4953	4955
RE129	F	0000713C	4	5004	4985	4986	4987	4989
RE13	F	00001A3C	4	1021	1002	1003	1004	1006
RE130	F	000071FC	4	5042	5023	5024	5025	5027
RE131	F	000072BC	4	5076	5057	5058	5059	5061
RE132	F	0000737C	4	5110	5091	5092	5093	5095
RE133	F	0000743C	4	5144	5125	5126	5127	5129
RE134	F	000074FC	4	5178	5159	5160	5161	5163
RE135	F	000075BC	4	5213	5194	5195	5196	5198
RE136	F	0000767C	4	5247	5228	5229	5230	5232
RE137	F	0000773C	4	5281	5262	5263	5264	5266
RE138	F	000077FC	4	5315	5296	5297	5298	5300
RE139	F	000078BC	4	5349	5330	5331	5332	5334
RE14	F	00001AFC	4	1055	1036	1037	1038	1040
RE140	F	0000797C	4	5384	5365	5366	5367	5369
RE141	F	00007A3C	4	5418	5399	5400	5401	5403
RE142	F	00007AFC	4	5452	5433	5434	5435	5437
RE143	F	00007BBC	4	5486	5467	5468	5469	5471
RE144	F	00007C7C	4	5520	5501	5502	5503	5505
RE145	F	00007D3C	4	5555	5536	5537	5538	5540
RE146	F	00007DFC	4	5589	5570	5571	5572	5574
RE147	F	00007EBC	4	5623	5604	5605	5606	5608
RE148	F	00007F7C	4	5657	5638	5639	5640	5642
RE149	F	0000803C	4	5691	5672	5673	5674	5676
RE15	F	00001BBC	4	1089	1070	1071	1072	1074
RE16	F	00001C7C	4	1124	1105	1106	1107	1109
RE17	F	00001D3C	4	1158	1139	1140	1141	1143
RE18	F	00001DFC	4	1192	1173	1174	1175	1177
RE19	F	00001EBC	4	1226	1207	1208	1209	1211
RE2	F	000011FC	4	645	626	627	628	630
RE20	F	00001F7C	4	1261	1242	1243	1244	1246
RE21	F	0000203C	4	1295	1276	1277	1278	1280
RE22	F	000020FC	4	1329	1310	1311	1312	1314
RE23	F	000021BC	4	1363	1344	1345	1346	1348

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
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RE27	F	000024BC	4	1503	1484	1485	1486	1488
RE28	F	0000257C	4	1537	1518	1519	1520	1522
RE29	F	0000263C	4	1572	1553	1554	1555	1557
RE3	F	000012BC	4	679	660	661	662	664
RE30	F	000026FC	4	1606	1587	1588	1589	1591
RE31	F	000027BC	4	1640	1621	1622	1623	1625
RE32	F	0000287C	4	1674	1655	1656	1657	1659
RE33	F	0000293C	4	1708	1689	1690	1691	1693
RE34	F	000029FC	4	1743	1724	1725	1726	1728
RE35	F	00002ABC	4	1777	1758	1759	1760	1762
RE36	F	00002B7C	4	1811	1792	1793	1794	1796
RE37	F	00002C3C	4	1845	1826	1827	1828	1830
RE38	F	00002CFC	4	1879	1860	1861	1862	1864
RE39	F	00002DBC	4	1914	1895	1896	1897	1899
RE4	F	0000137C	4	713	694	695	696	698
RE40	F	00002E7C	4	1948	1929	1930	1931	1933
RE41	F	00002F3C	4	1982	1963	1964	1965	1967
RE42	F	00002FFC	4	2016	1997	1998	1999	2001
RE43	F	000030BC	4	2051	2032	2033	2034	2036
RE44	F	0000317C	4	2085	2066	2067	2068	2070
RE45	F	0000323C	4	2119	2100	2101	2102	2104
RE46	F	000032FC	4	2153	2134	2135	2136	2138
RE47	F	000033BC	4	2191	2172	2173	2174	2176
RE48	F	0000347C	4	2225	2206	2207	2208	2210
RE49	F	0000353C	4	2259	2240	2241	2242	2244
RE5	F	0000143C	4	747	728	729	730	732
RE50	F	000035FC	4	2293	2274	2275	2276	2278
RE51	F	000036BC	4	2327	2308	2309	2310	2312
RE52	F	0000377C	4	2362	2343	2344	2345	2347
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RE55	F	000039BC	4	2464	2445	2446	2447	2449
RE56	F	00003A7C	4	2498	2479	2480	2481	2483
RE57	F	00003B3C	4	2533	2514	2515	2516	2518
RE58	F	00003BFC	4	2567	2548	2549	2550	2552
RE59	F	00003CBC	4	2601	2582	2583	2584	2586
RE6	F	000014FC	4	782	763	764	765	767
RE60	F	00003D7C	4	2635	2616	2617	2618	2620
RE61	F	00003E3C	4	2669	2650	2651	2652	2654
RE62	F	00003EFC	4	2704	2685	2686	2687	2689
RE63	F	00003FBC	4	2738	2719	2720	2721	2723
RE64	F	0000407C	4	2772	2753	2754	2755	2757
RE65	F	0000413C	4	2806	2787	2788	2789	2791
RE66	F	000041FC	4	2841	2822	2823	2824	2826
RE67	F	000042BC	4	2875	2856	2857	2858	2860
RE68	F	0000437C	4	2909	2890	2891	2892	2894
RE69	F	0000443C	4	2943	2924	2925	2926	2928
RE7	F	000015BC	4	816	797	798	799	801
RE70	F	000044FC	4	2981	2962	2963	2964	2966
RE71	F	000045BC	4	3015	2996	2997	2998	3000
RE72	F	0000467C	4	3049	3030	3031	3032	3034
RE73	F	0000473C	4	3083	3064	3065	3066	3068
RE74	F	000047FC	4	3117	3098	3099	3100	3102

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE75	F	000048BC	4	3152	3133	3134	3135	3137
RE76	F	0000497C	4	3186	3167	3168	3169	3171
RE77	F	00004A3C	4	3220	3201	3202	3203	3205
RE78	F	00004AFC	4	3254	3235	3236	3237	3239
RE79	F	00004BBC	4	3288	3269	3270	3271	3273
RE8	F	0000167C	4	850	831	832	833	835
RE80	F	00004C7C	4	3323	3304	3305	3306	3308
RE81	F	00004D3C	4	3357	3338	3339	3340	3342
RE82	F	00004DFC	4	3391	3372	3373	3374	3376
RE83	F	00004EBC	4	3425	3406	3407	3408	3410
RE84	F	00004F7C	4	3459	3440	3441	3442	3444
RE85	F	0000503C	4	3494	3475	3476	3477	3479
RE86	F	000050FC	4	3528	3509	3510	3511	3513
RE87	F	000051BC	4	3562	3543	3544	3545	3547
RE88	F	0000527C	4	3596	3577	3578	3579	3581
RE89	F	0000533C	4	3630	3611	3612	3613	3615
RE9	F	0000173C	4	884	865	866	867	869
RE90	F	000053FC	4	3668	3649	3650	3651	3653
RE91	F	000054BC	4	3702	3683	3684	3685	3687
RE92	F	0000557C	4	3736	3717	3718	3719	3721
RE93	F	0000563C	4	3770	3751	3752	3753	3755
RE94	F	000056FC	4	3804	3785	3786	3787	3789
RE95	F	000057BC	4	3839	3820	3821	3822	3824
RE96	F	0000587C	4	3873	3854	3855	3856	3858
RE97	F	0000593C	4	3907	3888	3889	3890	3892
RE98	F	000059FC	4	3941	3922	3923	3924	3926
RE99	F	00005ABC	4	3975	3956	3957	3958	3960
REA1	A	000010E0	4	596				
REA10	A	000017A0	4	903				
REA100	A	00005B20	4	3995				
REA101	A	00005BE0	4	4029				
REA102	A	00005CA0	4	4063				
REA103	A	00005D60	4	4097				
REA104	A	00005E20	4	4131				
REA105	A	00005EE0	4	4166				
REA106	A	00005FA0	4	4200				
REA107	A	00006060	4	4234				
REA108	A	00006120	4	4268				
REA109	A	000061E0	4	4302				
REA11	A	00001860	4	938				
REA110	A	000062A0	4	4340				
REA111	A	00006360	4	4374				
REA112	A	00006420	4	4408				
REA113	A	000064E0	4	4442				
REA114	A	000065A0	4	4476				
REA115	A	00006660	4	4511				
REA116	A	00006720	4	4545				
REA117	A	000067E0	4	4579				
REA118	A	000068A0	4	4613				
REA119	A	00006960	4	4647				
REA12	A	00001920	4	972				
REA120	A	00006A20	4	4682				
REA121	A	00006AE0	4	4716				
REA122	A	00006BA0	4	4750				
REA123	A	00006C60	4	4784				
REA124	A	00006D20	4	4818				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA125	A	00006DE0	4	4853	
REA126	A	00006EA0	4	4887	
REA127	A	00006F60	4	4921	
REA128	A	00007020	4	4955	
REA129	A	000070E0	4	4989	
REA13	A	000019E0	4	1006	
REA130	A	000071A0	4	5027	
REA131	A	00007260	4	5061	
REA132	A	00007320	4	5095	
REA133	A	000073E0	4	5129	
REA134	A	000074A0	4	5163	
REA135	A	00007560	4	5198	
REA136	A	00007620	4	5232	
REA137	A	000076E0	4	5266	
REA138	A	000077A0	4	5300	
REA139	A	00007860	4	5334	
REA14	A	00001AA0	4	1040	
REA140	A	00007920	4	5369	
REA141	A	000079E0	4	5403	
REA142	A	00007AA0	4	5437	
REA143	A	00007B60	4	5471	
REA144	A	00007C20	4	5505	
REA145	A	00007CE0	4	5540	
REA146	A	00007DA0	4	5574	
REA147	A	00007E60	4	5608	
REA148	A	00007F20	4	5642	
REA149	A	00007FE0	4	5676	
REA15	A	00001B60	4	1074	
REA16	A	00001C20	4	1109	
REA17	A	00001CE0	4	1143	
REA18	A	00001DA0	4	1177	
REA19	A	00001E60	4	1211	
REA2	A	000011A0	4	630	
REA20	A	00001F20	4	1246	
REA21	A	00001FE0	4	1280	
REA22	A	000020A0	4	1314	
REA23	A	00002160	4	1348	
REA24	A	00002220	4	1386	
REA25	A	000022E0	4	1420	
REA26	A	000023A0	4	1454	
REA27	A	00002460	4	1488	
REA28	A	00002520	4	1522	
REA29	A	000025E0	4	1557	
REA3	A	00001260	4	664	
REA30	A	000026A0	4	1591	
REA31	A	00002760	4	1625	
REA32	A	00002820	4	1659	
REA33	A	000028E0	4	1693	
REA34	A	000029A0	4	1728	
REA35	A	00002A60	4	1762	
REA36	A	00002B20	4	1796	
REA37	A	00002BE0	4	1830	
REA38	A	00002CA0	4	1864	
REA39	A	00002D60	4	1899	
REA4	A	00001320	4	698	
REA40	A	00002E20	4	1933	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA41	A	00002EE0	4	1967	
REA42	A	00002FA0	4	2001	
REA43	A	00003060	4	2036	
REA44	A	00003120	4	2070	
REA45	A	000031E0	4	2104	
REA46	A	000032A0	4	2138	
REA47	A	00003360	4	2176	
REA48	A	00003420	4	2210	
REA49	A	000034E0	4	2244	
REA5	A	000013E0	4	732	
REA50	A	000035A0	4	2278	
REA51	A	00003660	4	2312	
REA52	A	00003720	4	2347	
REA53	A	000037E0	4	2381	
REA54	A	000038A0	4	2415	
REA55	A	00003960	4	2449	
REA56	A	00003A20	4	2483	
REA57	A	00003AE0	4	2518	
REA58	A	00003BA0	4	2552	
REA59	A	00003C60	4	2586	
REA6	A	000014A0	4	767	
REA60	A	00003D20	4	2620	
REA61	A	00003DE0	4	2654	
REA62	A	00003EA0	4	2689	
REA63	A	00003F60	4	2723	
REA64	A	00004020	4	2757	
REA65	A	000040E0	4	2791	
REA66	A	000041A0	4	2826	
REA67	A	00004260	4	2860	
REA68	A	00004320	4	2894	
REA69	A	000043E0	4	2928	
REA7	A	00001560	4	801	
REA70	A	000044A0	4	2966	
REA71	A	00004560	4	3000	
REA72	A	00004620	4	3034	
REA73	A	000046E0	4	3068	
REA74	A	000047A0	4	3102	
REA75	A	00004860	4	3137	
REA76	A	00004920	4	3171	
REA77	A	000049E0	4	3205	
REA78	A	00004AA0	4	3239	
REA79	A	00004B60	4	3273	
REA8	A	00001620	4	835	
REA80	A	00004C20	4	3308	
REA81	A	00004CE0	4	3342	
REA82	A	00004DA0	4	3376	
REA83	A	00004E60	4	3410	
REA84	A	00004F20	4	3444	
REA85	A	00004FE0	4	3479	
REA86	A	000050A0	4	3513	
REA87	A	00005160	4	3547	
REA88	A	00005220	4	3581	
REA89	A	000052E0	4	3615	
REA9	A	000016E0	4	869	
REA90	A	000053A0	4	3653	
REA91	A	00005460	4	3687	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA92	A	00005520	4	3721		
REA93	A	000055E0	4	3755		
REA94	A	000056A0	4	3789		
REA95	A	00005760	4	3824		
REA96	A	00005820	4	3858		
REA97	A	000058E0	4	3892		
REA98	A	000059A0	4	3926		
REA99	A	00005A60	4	3960		
READDR	A	00000020	4	471	266	
REG2LOW	U	000000DD	1	413		
REG2PATT	U	AABBCCDD	1	412		
RELEN	A	0000001C	4	470		
RPTDWSAV	D	00000448	8	337	324	328
RPTERROR	I	000003DC	4	304	279	
RPTSAVE	F	00000440	4	334	304	331
RPTSVR5	F	00000444	4	335	305	330
SKL0001	U	0000004E	1	191	207	
SKL0002	U	0000004E	1	224	240	
SKT0001	C	0000022A	20	188	191	208
SKT0002	C	000002D4	20	221	224	241
SVOLDPSW	U	00000140	0	127		
T1	A	000010C0	4	587	5707	
T10	A	00001780	4	894	5716	
T100	A	00005B00	4	3986	5806	
T101	A	00005BC0	4	4020	5807	
T102	A	00005C80	4	4054	5808	
T103	A	00005D40	4	4088	5809	
T104	A	00005E00	4	4122	5810	
T105	A	00005EC0	4	4157	5811	
T106	A	00005F80	4	4191	5812	
T107	A	00006040	4	4225	5813	
T108	A	00006100	4	4259	5814	
T109	A	000061C0	4	4293	5815	
T11	A	00001840	4	929	5717	
T110	A	00006280	4	4331	5816	
T111	A	00006340	4	4365	5817	
T112	A	00006400	4	4399	5818	
T113	A	000064C0	4	4433	5819	
T114	A	00006580	4	4467	5820	
T115	A	00006640	4	4502	5821	
T116	A	00006700	4	4536	5822	
T117	A	000067C0	4	4570	5823	
T118	A	00006880	4	4604	5824	
T119	A	00006940	4	4638	5825	
T12	A	00001900	4	963	5718	
T120	A	00006A00	4	4673	5826	
T121	A	00006AC0	4	4707	5827	
T122	A	00006B80	4	4741	5828	
T123	A	00006C40	4	4775	5829	
T124	A	00006D00	4	4809	5830	
T125	A	00006DC0	4	4844	5831	
T126	A	00006E80	4	4878	5832	
T127	A	00006F40	4	4912	5833	
T128	A	00007000	4	4946	5834	
T129	A	000070C0	4	4980	5835	
T13	A	000019C0	4	997	5719	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T130	A	00007180	4	5018	5836
T131	A	00007240	4	5052	5837
T132	A	00007300	4	5086	5838
T133	A	000073C0	4	5120	5839
T134	A	00007480	4	5154	5840
T135	A	00007540	4	5189	5841
T136	A	00007600	4	5223	5842
T137	A	000076C0	4	5257	5843
T138	A	00007780	4	5291	5844
T139	A	00007840	4	5325	5845
T14	A	00001A80	4	1031	5720
T140	A	00007900	4	5360	5846
T141	A	000079C0	4	5394	5847
T142	A	00007A80	4	5428	5848
T143	A	00007B40	4	5462	5849
T144	A	00007C00	4	5496	5850
T145	A	00007CC0	4	5531	5851
T146	A	00007D80	4	5565	5852
T147	A	00007E40	4	5599	5853
T148	A	00007F00	4	5633	5854
T149	A	00007FC0	4	5667	5855
T15	A	00001B40	4	1065	5721
T16	A	00001C00	4	1100	5722
T17	A	00001CC0	4	1134	5723
T18	A	00001D80	4	1168	5724
T19	A	00001E40	4	1202	5725
T2	A	00001180	4	621	5708
T20	A	00001F00	4	1237	5726
T21	A	00001FC0	4	1271	5727
T22	A	00002080	4	1305	5728
T23	A	00002140	4	1339	5729
T24	A	00002200	4	1377	5730
T25	A	000022C0	4	1411	5731
T26	A	00002380	4	1445	5732
T27	A	00002440	4	1479	5733
T28	A	00002500	4	1513	5734
T29	A	000025C0	4	1548	5735
T3	A	00001240	4	655	5709
T30	A	00002680	4	1582	5736
T31	A	00002740	4	1616	5737
T32	A	00002800	4	1650	5738
T33	A	000028C0	4	1684	5739
T34	A	00002980	4	1719	5740
T35	A	00002A40	4	1753	5741
T36	A	00002B00	4	1787	5742
T37	A	00002BC0	4	1821	5743
T38	A	00002C80	4	1855	5744
T39	A	00002D40	4	1890	5745
T4	A	00001300	4	689	5710
T40	A	00002E00	4	1924	5746
T41	A	00002EC0	4	1958	5747
T42	A	00002F80	4	1992	5748
T43	A	00003040	4	2027	5749
T44	A	00003100	4	2061	5750
T45	A	000031C0	4	2095	5751
T46	A	00003280	4	2129	5752

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T47	A	00003340	4	2167	5753
T48	A	00003400	4	2201	5754
T49	A	000034C0	4	2235	5755
T5	A	000013C0	4	723	5711
T50	A	00003580	4	2269	5756
T51	A	00003640	4	2303	5757
T52	A	00003700	4	2338	5758
T53	A	000037C0	4	2372	5759
T54	A	00003880	4	2406	5760
T55	A	00003940	4	2440	5761
T56	A	00003A00	4	2474	5762
T57	A	00003AC0	4	2509	5763
T58	A	00003B80	4	2543	5764
T59	A	00003C40	4	2577	5765
T6	A	00001480	4	758	5712
T60	A	00003D00	4	2611	5766
T61	A	00003DC0	4	2645	5767
T62	A	00003E80	4	2680	5768
T63	A	00003F40	4	2714	5769
T64	A	00004000	4	2748	5770
T65	A	000040C0	4	2782	5771
T66	A	00004180	4	2817	5772
T67	A	00004240	4	2851	5773
T68	A	00004300	4	2885	5774
T69	A	000043C0	4	2919	5775
T7	A	00001540	4	792	5713
T70	A	00004480	4	2957	5776
T71	A	00004540	4	2991	5777
T72	A	00004600	4	3025	5778
T73	A	000046C0	4	3059	5779
T74	A	00004780	4	3093	5780
T75	A	00004840	4	3128	5781
T76	A	00004900	4	3162	5782
T77	A	000049C0	4	3196	5783
T78	A	00004A80	4	3230	5784
T79	A	00004B40	4	3264	5785
T8	A	00001600	4	826	5714
T80	A	00004C00	4	3299	5786
T81	A	00004CC0	4	3333	5787
T82	A	00004D80	4	3367	5788
T83	A	00004E40	4	3401	5789
T84	A	00004F00	4	3435	5790
T85	A	00004FC0	4	3470	5791
T86	A	00005080	4	3504	5792
T87	A	00005140	4	3538	5793
T88	A	00005200	4	3572	5794
T89	A	000052C0	4	3606	5795
T9	A	000016C0	4	860	5715
T90	A	00005380	4	3644	5796
T91	A	00005440	4	3678	5797
T92	A	00005500	4	3712	5798
T93	A	000055C0	4	3746	5799
T94	A	00005680	4	3780	5800
T95	A	00005740	4	3815	5801
T96	A	00005800	4	3849	5802
T97	A	000058C0	4	3883	5803

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
T98	A	00005980	4	3917	5804	
T99	A	00005A40	4	3951	5805	
TESTING	F	00001004	4	424	260	
TNUM	H	00000004	2	462	259	307
TSUB	A	00000000	4	461	263	
TTABLE	F	00008084	4	5706		
V0	U	00000000	1	5888		
V1	U	00000001	1	5889	262	
V10	U	0000000A	1	5898		
V11	U	0000000B	1	5899		
V12	U	0000000C	1	5900		
V13	U	0000000D	1	5901		
V14	U	0000000E	1	5902		
V15	U	0000000F	1	5903		
V16	U	00000010	1	5904		
V17	U	00000011	1	5905		
V18	U	00000012	1	5906		
V19	U	00000013	1	5907		
V1FUDGE	X	00001094	16	453	262	
V101	X	000010F0	16	598	609	
V1010	X	000017B0	16	905	916	
V10100	X	00005B30	16	3997	4008	
V10101	X	00005BF0	16	4031	4042	
V10102	X	00005CB0	16	4065	4076	
V10103	X	00005D70	16	4099	4110	
V10104	X	00005E30	16	4133	4144	
V10105	X	00005EF0	16	4168	4179	
V10106	X	00005FB0	16	4202	4213	
V10107	X	00006070	16	4236	4247	
V10108	X	00006130	16	4270	4281	
V10109	X	000061F0	16	4304	4315	
V1011	X	00001870	16	940	951	
V10110	X	000062B0	16	4342	4353	
V10111	X	00006370	16	4376	4387	
V10112	X	00006430	16	4410	4421	
V10113	X	000064F0	16	4444	4455	
V10114	X	000065B0	16	4478	4489	
V10115	X	00006670	16	4513	4524	
V10116	X	00006730	16	4547	4558	
V10117	X	000067F0	16	4581	4592	
V10118	X	000068B0	16	4615	4626	
V10119	X	00006970	16	4649	4660	
V1012	X	00001930	16	974	985	
V10120	X	00006A30	16	4684	4695	
V10121	X	00006AF0	16	4718	4729	
V10122	X	00006BB0	16	4752	4763	
V10123	X	00006C70	16	4786	4797	
V10124	X	00006D30	16	4820	4831	
V10125	X	00006DF0	16	4855	4866	
V10126	X	00006EB0	16	4889	4900	
V10127	X	00006F70	16	4923	4934	
V10128	X	00007030	16	4957	4968	
V10129	X	000070F0	16	4991	5002	
V1013	X	000019F0	16	1008	1019	
V10130	X	000071B0	16	5029	5040	
V10131	X	00007270	16	5063	5074	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V10132	X	00007330	16	5097	5108
V10133	X	000073F0	16	5131	5142
V10134	X	000074B0	16	5165	5176
V10135	X	00007570	16	5200	5211
V10136	X	00007630	16	5234	5245
V10137	X	000076F0	16	5268	5279
V10138	X	000077B0	16	5302	5313
V10139	X	00007870	16	5336	5347
V1014	X	00001AB0	16	1042	1053
V10140	X	00007930	16	5371	5382
V10141	X	000079F0	16	5405	5416
V10142	X	00007AB0	16	5439	5450
V10143	X	00007B70	16	5473	5484
V10144	X	00007C30	16	5507	5518
V10145	X	00007CF0	16	5542	5553
V10146	X	00007DB0	16	5576	5587
V10147	X	00007E70	16	5610	5621
V10148	X	00007F30	16	5644	5655
V10149	X	00007FF0	16	5678	5689
V1015	X	00001B70	16	1076	1087
V1016	X	00001C30	16	1111	1122
V1017	X	00001CF0	16	1145	1156
V1018	X	00001DB0	16	1179	1190
V1019	X	00001E70	16	1213	1224
V102	X	000011B0	16	632	643
V1020	X	00001F30	16	1248	1259
V1021	X	00001FF0	16	1282	1293
V1022	X	000020B0	16	1316	1327
V1023	X	00002170	16	1350	1361
V1024	X	00002230	16	1388	1399
V1025	X	000022F0	16	1422	1433
V1026	X	000023B0	16	1456	1467
V1027	X	00002470	16	1490	1501
V1028	X	00002530	16	1524	1535
V1029	X	000025F0	16	1559	1570
V103	X	00001270	16	666	677
V1030	X	000026B0	16	1593	1604
V1031	X	00002770	16	1627	1638
V1032	X	00002830	16	1661	1672
V1033	X	000028F0	16	1695	1706
V1034	X	000029B0	16	1730	1741
V1035	X	00002A70	16	1764	1775
V1036	X	00002B30	16	1798	1809
V1037	X	00002BF0	16	1832	1843
V1038	X	00002CB0	16	1866	1877
V1039	X	00002D70	16	1901	1912
V104	X	00001330	16	700	711
V1040	X	00002E30	16	1935	1946
V1041	X	00002EF0	16	1969	1980
V1042	X	00002FB0	16	2003	2014
V1043	X	00003070	16	2038	2049
V1044	X	00003130	16	2072	2083
V1045	X	000031F0	16	2106	2117
V1046	X	000032B0	16	2140	2151
V1047	X	00003370	16	2178	2189
V1048	X	00003430	16	2212	2223

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1049	X	000034F0	16	2246	2257
V105	X	000013F0	16	734	745
V1050	X	000035B0	16	2280	2291
V1051	X	00003670	16	2314	2325
V1052	X	00003730	16	2349	2360
V1053	X	000037F0	16	2383	2394
V1054	X	000038B0	16	2417	2428
V1055	X	00003970	16	2451	2462
V1056	X	00003A30	16	2485	2496
V1057	X	00003AF0	16	2520	2531
V1058	X	00003BB0	16	2554	2565
V1059	X	00003C70	16	2588	2599
V106	X	000014B0	16	769	780
V1060	X	00003D30	16	2622	2633
V1061	X	00003DF0	16	2656	2667
V1062	X	00003EB0	16	2691	2702
V1063	X	00003F70	16	2725	2736
V1064	X	00004030	16	2759	2770
V1065	X	000040F0	16	2793	2804
V1066	X	000041B0	16	2828	2839
V1067	X	00004270	16	2862	2873
V1068	X	00004330	16	2896	2907
V1069	X	000043F0	16	2930	2941
V107	X	00001570	16	803	814
V1070	X	000044B0	16	2968	2979
V1071	X	00004570	16	3002	3013
V1072	X	00004630	16	3036	3047
V1073	X	000046F0	16	3070	3081
V1074	X	000047B0	16	3104	3115
V1075	X	00004870	16	3139	3150
V1076	X	00004930	16	3173	3184
V1077	X	000049F0	16	3207	3218
V1078	X	00004AB0	16	3241	3252
V1079	X	00004B70	16	3275	3286
V108	X	00001630	16	837	848
V1080	X	00004C30	16	3310	3321
V1081	X	00004CF0	16	3344	3355
V1082	X	00004DB0	16	3378	3389
V1083	X	00004E70	16	3412	3423
V1084	X	00004F30	16	3446	3457
V1085	X	00004FF0	16	3481	3492
V1086	X	000050B0	16	3515	3526
V1087	X	00005170	16	3549	3560
V1088	X	00005230	16	3583	3594
V1089	X	000052F0	16	3617	3628
V109	X	000016F0	16	871	882
V1090	X	000053B0	16	3655	3666
V1091	X	00005470	16	3689	3700
V1092	X	00005530	16	3723	3734
V1093	X	000055F0	16	3757	3768
V1094	X	000056B0	16	3791	3802
V1095	X	00005770	16	3826	3837
V1096	X	00005830	16	3860	3871
V1097	X	000058F0	16	3894	3905
V1098	X	000059B0	16	3928	3939
V1099	X	00005A70	16	3962	3973

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V10UTPUT	X	00000030	16	473	267												
V2	U	00000002	1	5890													
V20	U	00000014	1	5908													
V21	U	00000015	1	5909													
V22	U	00000016	1	5910	603	608	609	637	642	643	671	676	677	705	710	711	739
					744	745	774	779	780	808	813	814	842	847	848	876	881
					882	910	915	916	945	950	951	979	984	985	1013	1018	1019
					1047	1052	1053	1081	1086	1087	1116	1121	1122	1150	1155	1156	1184
					1189	1190	1218	1223	1224	1253	1258	1259	1287	1292	1293	1321	1326
					1327	1355	1360	1361	1393	1398	1399	1427	1432	1433	1461	1466	1467
					1495	1500	1501	1529	1534	1535	1564	1569	1570	1598	1603	1604	1632
					1637	1638	1666	1671	1672	1700	1705	1706	1735	1740	1741	1769	1774
					1775	1803	1808	1809	1837	1842	1843	1871	1876	1877	1906	1911	1912
					1940	1945	1946	1974	1979	1980	2008	2013	2014	2043	2048	2049	2077
					2082	2083	2111	2116	2117	2145	2150	2151	2183	2188	2189	2217	2222
					2223	2251	2256	2257	2285	2290	2291	2319	2324	2325	2354	2359	2360
					2388	2393	2394	2422	2427	2428	2456	2461	2462	2490	2495	2496	2525
					2530	2531	2559	2564	2565	2593	2598	2599	2627	2632	2633	2661	2666
					2667	2696	2701	2702	2730	2735	2736	2764	2769	2770	2798	2803	2804
					2833	2838	2839	2867	2872	2873	2901	2906	2907	2935	2940	2941	2973
					2978	2979	3007	3012	3013	3041	3046	3047	3075	3080	3081	3109	3114
					3115	3144	3149	3150	3178	3183	3184	3212	3217	3218	3246	3251	3252
					3280	3285	3286	3315	3320	3321	3349	3354	3355	3383	3388	3389	3417
					3422	3423	3451	3456	3457	3486	3491	3492	3520	3525	3526	3554	3559
					3560	3588	3593	3594	3622	3627	3628	3660	3665	3666	3694	3699	3700
					3728	3733	3734	3762	3767	3768	3796	3801	3802	3831	3836	3837	3865
					3870	3871	3899	3904	3905	3933	3938	3939	3967	3972	3973	4002	4007
					4008	4036	4041	4042	4070	4075	4076	4104	4109	4110	4138	4143	4144
					4173	4178	4179	4207	4212	4213	4241	4246	4247	4275	4280	4281	4309
					4314	4315	4347	4352	4353	4381	4386	4387	4415	4420	4421	4449	4454
					4455	4483	4488	4489	4518	4523	4524	4552	4557	4558	4586	4591	4592
					4620	4625	4626	4654	4659	4660	4689	4694	4695	4723	4728	4729	4757
					4762	4763	4791	4796	4797	4825	4830	4831	4860	4865	4866	4894	4899
					4900	4928	4933	4934	4962	4967	4968	4996	5001	5002	5034	5039	5040
					5068	5073	5074	5102	5107	5108	5136	5141	5142	5170	5175	5176	5205
					5210	5211	5239	5244	5245	5273	5278	5279	5307	5312	5313	5341	5346
					5347	5376	5381	5382	5410	5415	5416	5444	5449	5450	5478	5483	5484
					5512	5517	5518	5547	5552	5553	5581	5586	5587	5615	5620	5621	5649
					5654	5655	5683	5688	5689								
V23	U	00000017	1	5911	605	608	639	642	673	676	707	710	741	744	776	779	810
					813	844	847	878	881	912	915	947	950	981	984	1015	1018
					1049	1052	1083	1086	1118	1121	1152	1155	1186	1189	1220	1223	1255
					1258	1289	1292	1323	1326	1357	1360	1395	1398	1429	1432	1463	1466
					1497	1500	1531	1534	1566	1569	1600	1603	1634	1637	1668	1671	1702
					1705	1737	1740	1771	1774	1805	1808	1839	1842	1873	1876	1908	1911
					1942	1945	1976	1979	2010	2013	2045	2048	2079	2082	2113	2116	2147
					2150	2185	2188	2219	2222	2253	2256	2287	2290	2321	2324	2356	2359
					2390	2393	2424	2427	2458	2461	2492	2495	2527	2530	2561	2564	2595
					2598	2629	2632	2663	2666	2698	2701	2732	2735	2766	2769	2800	2803
					2835	2838	2869	2872	2903	2906	2937	2940	2975	2978	3009	3012	3043
					3046	3077	3080	3111	3114	3146	3149	3180	3183	3214	3217	3248	3251
					3282	3285	3317	3320	3351	3354	3385	3388	3419	3422	3453	3456	3488
					3491	3522	3525	3556	3559	3590	3593	3624	3627	3662	3665	3696	3699
					3730	3733	3764	3767	3798	3801	3833	3836	3867	3870	3901	3904	3935
					3938	3969	3972	4004	4007	4038	4041	4072	4075	4106	4109	4140	4143
					4175	4178	4209	4212	4243	4246	4277	4280	4311	4314	4349	4352	4383

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					4386 4417 4420 4451 4454 4485 4488 4520 4523 4554 4557 4588 4591
					4622 4625 4656 4659 4691 4694 4725 4728 4759 4762 4793 4796 4827
					4830 4862 4865 4896 4899 4930 4933 4964 4967 4998 5001 5036 5039
					5070 5073 5104 5107 5138 5141 5172 5175 5207 5210 5241 5244 5275
					5278 5309 5312 5343 5346 5378 5381 5412 5415 5446 5449 5480 5483
					5514 5517 5549 5552 5583 5586 5617 5620 5651 5654 5685 5688
V24	U	00000018	1	5912	607 608 641 642 675 676 709 710 743 744 778 779 812
					813 846 847 880 881 914 915 949 950 983 984 1017 1018
					1051 1052 1085 1086 1120 1121 1154 1155 1188 1189 1222 1223 1257
					1258 1291 1292 1325 1326 1359 1360 1397 1398 1431 1432 1465 1466
					1499 1500 1533 1534 1568 1569 1602 1603 1636 1637 1670 1671 1704
					1705 1739 1740 1773 1774 1807 1808 1841 1842 1875 1876 1910 1911
					1944 1945 1978 1979 2012 2013 2047 2048 2081 2082 2115 2116 2149
					2150 2187 2188 2221 2222 2255 2256 2289 2290 2323 2324 2358 2359
					2392 2393 2426 2427 2460 2461 2494 2495 2529 2530 2563 2564 2597
					2598 2631 2632 2665 2666 2700 2701 2734 2735 2768 2769 2802 2803
					2837 2838 2871 2872 2905 2906 2939 2940 2977 2978 3011 3012 3045
					3046 3079 3080 3113 3114 3148 3149 3182 3183 3216 3217 3250 3251
					3284 3285 3319 3320 3353 3354 3387 3388 3421 3422 3455 3456 3490
					3491 3524 3525 3558 3559 3592 3593 3626 3627 3664 3665 3698 3699
					3732 3733 3766 3767 3800 3801 3835 3836 3869 3870 3903 3904 3937
					3938 3971 3972 4006 4007 4040 4041 4074 4075 4108 4109 4142 4143
					4177 4178 4211 4212 4245 4246 4279 4280 4313 4314 4351 4352 4385
					4386 4419 4420 4453 4454 4487 4488 4522 4523 4556 4557 4590 4591
					4624 4625 4658 4659 4693 4694 4727 4728 4761 4762 4795 4796 4829
					4830 4864 4865 4898 4899 4932 4933 4966 4967 5000 5001 5038 5039
					5072 5073 5106 5107 5140 5141 5174 5175 5209 5210 5243 5244 5277
					5278 5311 5312 5345 5346 5380 5381 5414 5415 5448 5449 5482 5483
					5516 5517 5551 5552 5585 5586 5619 5620 5653 5654 5687 5688
V25	U	00000019	1	5913	
V26	U	0000001A	1	5914	
V27	U	0000001B	1	5915	
V28	U	0000001C	1	5916	
V29	U	0000001D	1	5917	
V2ADDR	A	00000010	4	467	602 636 670 704 738 773 807 841 875 909 944 978 1012
					1046 1080 1115 1149 1183 1217 1252 1286 1320 1354 1392 1426 1460
					1494 1528 1563 1597 1631 1665 1699 1734 1768 1802 1836 1870 1905
					1939 1973 2007 2042 2076 2110 2144 2182 2216 2250 2284 2318 2353
					2387 2421 2455 2489 2524 2558 2592 2626 2660 2695 2729 2763 2797
					2832 2866 2900 2934 2972 3006 3040 3074 3108 3143 3177 3211 3245
					3279 3314 3348 3382 3416 3450 3485 3519 3553 3587 3621 3659 3693
					3727 3761 3795 3830 3864 3898 3932 3966 4001 4035 4069 4103 4137
					4172 4206 4240 4274 4308 4346 4380 4414 4448 4482 4517 4551 4585
					4619 4653 4688 4722 4756 4790 4824 4859 4893 4927 4961 4995 5033
					5067 5101 5135 5169 5204 5238 5272 5306 5340 5375 5409 5443 5477
					5511 5546 5580 5614 5648 5682
V3	U	00000003	1	5891	
V30	U	0000001E	1	5918	
V31	U	0000001F	1	5919	
V3ADDR	A	00000014	4	468	604 638 672 706 740 775 809 843 877 911 946 980 1014
					1048 1082 1117 1151 1185 1219 1254 1288 1322 1356 1394 1428 1462
					1496 1530 1565 1599 1633 1667 1701 1736 1770 1804 1838 1872 1907
					1941 1975 2009 2044 2078 2112 2146 2184 2218 2252 2286 2320 2355
					2389 2423 2457 2491 2526 2560 2594 2628 2662 2697 2731 2765 2799
					2834 2868 2902 2936 2974 3008 3042 3076 3110 3145 3179 3213 3247
					3281 3316 3350 3384 3418 3452 3487 3521 3555 3589 3623 3661 3695

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					3729	3763	3797	3832	3866	3900	3934	3968	4003	4037	4071	4105	4139
					4174	4208	4242	4276	4310	4348	4382	4416	4450	4484	4519	4553	4587
					4621	4655	4690	4724	4758	4792	4826	4861	4895	4929	4963	4997	5035
					5069	5103	5137	5171	5206	5240	5274	5308	5342	5377	5411	5445	5479
					5513	5548	5582	5616	5650	5684							
V4	U	00000004	1	5892													
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					1050	1084	1119	1153	1187	1221	1256	1290	1324	1358	1396	1430	1464
					1498	1532	1567	1601	1635	1669	1703	1738	1772	1806	1840	1874	1909
					1943	1977	2011	2046	2080	2114	2148	2186	2220	2254	2288	2322	2357
					2391	2425	2459	2493	2528	2562	2596	2630	2664	2699	2733	2767	2801
					2836	2870	2904	2938	2976	3010	3044	3078	3112	3147	3181	3215	3249
					3283	3318	3352	3386	3420	3454	3489	3523	3557	3591	3625	3663	3697
					3731	3765	3799	3834	3868	3902	3936	3970	4005	4039	4073	4107	4141
					4176	4210	4244	4278	4312	4350	4384	4418	4452	4486	4521	4555	4589
					4623	4657	4692	4726	4760	4794	4828	4863	4897	4931	4965	4999	5037
					5071	5105	5139	5173	5208	5242	5276	5310	5344	5379	5413	5447	5481
					5515	5550	5584	5618	5652	5686							
V5	U	00000005	1	5893													
V6	U	00000006	1	5894													
V7	U	00000007	1	5895													
V8	U	00000008	1	5896													
V9	U	00000009	1	5897													
X0001	U	000002A8	1	197	185	198											
X0002	U	00000358	1	230	218	231											
X1	F	00001108	4	601	587												
X10	F	000017C8	4	908	894												
X100	F	00005B48	4	4000	3986												
X101	F	00005C08	4	4034	4020												
X102	F	00005CC8	4	4068	4054												
X103	F	00005D88	4	4102	4088												
X104	F	00005E48	4	4136	4122												
X105	F	00005F08	4	4171	4157												
X106	F	00005FC8	4	4205	4191												
X107	F	00006088	4	4239	4225												
X108	F	00006148	4	4273	4259												
X109	F	00006208	4	4307	4293												
X11	F	00001888	4	943	929												
X110	F	000062C8	4	4345	4331												
X111	F	00006388	4	4379	4365												
X112	F	00006448	4	4413	4399												
X113	F	00006508	4	4447	4433												
X114	F	000065C8	4	4481	4467												
X115	F	00006688	4	4516	4502												
X116	F	00006748	4	4550	4536												
X117	F	00006808	4	4584	4570												
X118	F	000068C8	4	4618	4604												
X119	F	00006988	4	4652	4638												
X12	F	00001948	4	977	963												
X120	F	00006A48	4	4687	4673												
X121	F	00006B08	4	4721	4707												
X122	F	00006BC8	4	4755	4741												
X123	F	00006C88	4	4789	4775												
X124	F	00006D48	4	4823	4809												
X125	F	00006E08	4	4858	4844												
X126	F	00006EC8	4	4892	4878												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X127	F	00006F88	4	4926	4912
X128	F	00007048	4	4960	4946
X129	F	00007108	4	4994	4980
X13	F	00001A08	4	1011	997
X130	F	000071C8	4	5032	5018
X131	F	00007288	4	5066	5052
X132	F	00007348	4	5100	5086
X133	F	00007408	4	5134	5120
X134	F	000074C8	4	5168	5154
X135	F	00007588	4	5203	5189
X136	F	00007648	4	5237	5223
X137	F	00007708	4	5271	5257
X138	F	000077C8	4	5305	5291
X139	F	00007888	4	5339	5325
X14	F	00001AC8	4	1045	1031
X140	F	00007948	4	5374	5360
X141	F	00007A08	4	5408	5394
X142	F	00007AC8	4	5442	5428
X143	F	00007B88	4	5476	5462
X144	F	00007C48	4	5510	5496
X145	F	00007D08	4	5545	5531
X146	F	00007DC8	4	5579	5565
X147	F	00007E88	4	5613	5599
X148	F	00007F48	4	5647	5633
X149	F	00008008	4	5681	5667
X15	F	00001B88	4	1079	1065
X16	F	00001C48	4	1114	1100
X17	F	00001D08	4	1148	1134
X18	F	00001DC8	4	1182	1168
X19	F	00001E88	4	1216	1202
X2	F	000011C8	4	635	621
X20	F	00001F48	4	1251	1237
X21	F	00002008	4	1285	1271
X22	F	000020C8	4	1319	1305
X23	F	00002188	4	1353	1339
X24	F	00002248	4	1391	1377
X25	F	00002308	4	1425	1411
X26	F	000023C8	4	1459	1445
X27	F	00002488	4	1493	1479
X28	F	00002548	4	1527	1513
X29	F	00002608	4	1562	1548
X3	F	00001288	4	669	655
X30	F	000026C8	4	1596	1582
X31	F	00002788	4	1630	1616
X32	F	00002848	4	1664	1650
X33	F	00002908	4	1698	1684
X34	F	000029C8	4	1733	1719
X35	F	00002A88	4	1767	1753
X36	F	00002B48	4	1801	1787
X37	F	00002C08	4	1835	1821
X38	F	00002CC8	4	1869	1855
X39	F	00002D88	4	1904	1890
X4	F	00001348	4	703	689
X40	F	00002E48	4	1938	1924
X41	F	00002F08	4	1972	1958
X42	F	00002FC8	4	2006	1992

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X43	F	00003088	4	2041	2027
X44	F	00003148	4	2075	2061
X45	F	00003208	4	2109	2095
X46	F	000032C8	4	2143	2129
X47	F	00003388	4	2181	2167
X48	F	00003448	4	2215	2201
X49	F	00003508	4	2249	2235
X5	F	00001408	4	737	723
X50	F	000035C8	4	2283	2269
X51	F	00003688	4	2317	2303
X52	F	00003748	4	2352	2338
X53	F	00003808	4	2386	2372
X54	F	000038C8	4	2420	2406
X55	F	00003988	4	2454	2440
X56	F	00003A48	4	2488	2474
X57	F	00003B08	4	2523	2509
X58	F	00003BC8	4	2557	2543
X59	F	00003C88	4	2591	2577
X6	F	000014C8	4	772	758
X60	F	00003D48	4	2625	2611
X61	F	00003E08	4	2659	2645
X62	F	00003EC8	4	2694	2680
X63	F	00003F88	4	2728	2714
X64	F	00004048	4	2762	2748
X65	F	00004108	4	2796	2782
X66	F	000041C8	4	2831	2817
X67	F	00004288	4	2865	2851
X68	F	00004348	4	2899	2885
X69	F	00004408	4	2933	2919
X7	F	00001588	4	806	792
X70	F	000044C8	4	2971	2957
X71	F	00004588	4	3005	2991
X72	F	00004648	4	3039	3025
X73	F	00004708	4	3073	3059
X74	F	000047C8	4	3107	3093
X75	F	00004888	4	3142	3128
X76	F	00004948	4	3176	3162
X77	F	00004A08	4	3210	3196
X78	F	00004AC8	4	3244	3230
X79	F	00004B88	4	3278	3264
X8	F	00001648	4	840	826
X80	F	00004C48	4	3313	3299
X81	F	00004D08	4	3347	3333
X82	F	00004DC8	4	3381	3367
X83	F	00004E88	4	3415	3401
X84	F	00004F48	4	3449	3435
X85	F	00005008	4	3484	3470
X86	F	000050C8	4	3518	3504
X87	F	00005188	4	3552	3538
X88	F	00005248	4	3586	3572
X89	F	00005308	4	3620	3606
X9	F	00001708	4	874	860
X90	F	000053C8	4	3658	3644
X91	F	00005488	4	3692	3678
X92	F	00005548	4	3726	3712
X93	F	00005608	4	3760	3746

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
X94	F	000056C8	4	3794	3780				
X95	F	00005788	4	3829	3815				
X96	F	00005848	4	3863	3849				
X97	F	00005908	4	3897	3883				
X98	F	000059C8	4	3931	3917				
X99	F	00005A88	4	3965	3951				
XC0001	U	000002D0	1	211	203				
XC0002	U	00000380	1	244	236				
ZVE7TST	J	00000000	33512	124	127	129	133	137	422 125
=A(E7TESTS)	A	0000054C	4	400	250				
=AL2(L'MSGMSG)	R	00000556	2	403	349				
=F'1'	F	00000550	4	401	285				
=F'2'	F	00000548	4	399	235				
=F'64'	F	00000544	4	398	202				
=H'0'	H	00000554	2	402	344				

MACRO	DEFN	REFERENCES															
FCHECK	77	184	217														
PTTABLE	541	5705															
VRR_D	492	584	618	652	686	720	755	789	823	857	891	926	960	994	1028	1062	1097	1131
		1165	1199	1234	1268	1302	1336	1374	1408	1442	1476	1510	1545	1579	1613	1647	1681	1716
		1750	1784	1818	1852	1887	1921	1955	1989	2024	2058	2092	2126	2164	2198	2232	2266	2300
		2335	2369	2403	2437	2471	2506	2540	2574	2608	2642	2677	2711	2745	2779	2814	2848	2882
		2916	2954	2988	3022	3056	3090	3125	3159	3193	3227	3261	3296	3330	3364	3398	3432	3467
		3501	3535	3569	3603	3641	3675	3709	3743	3777	3812	3846	3880	3914	3948	3983	4017	4051
		4085	4119	4154	4188	4222	4256	4290	4328	4362	4396	4430	4464	4499	4533	4567	4601	4635
		4670	4704	4738	4772	4806	4841	4875	4909	4943	4977	5015	5049	5083	5117	5151	5186	5220
		5254	5288	5322	5357	5391	5425	5459	5493	5528	5562	5596	5630	5664				

DESC	SYMBOL	SIZE	POS	ADDR

Entry: 0

Image	IMAGE	33512	0000-82E7	0000-82E7
Region		33512	0000-82E7	0000-82E7
CSECT	ZVE7TST	33512	0000-82E7	0000-82E7

      STMT   FILE NAME

1   /home/tn529/sharedvfp/tests/zvector-e7-10-multiplyAdd.asm

** NO ERRORS FOUND **