| LOC | OBJECT CODE | ADDR1 | ADDR2 | STMT |

```
   2 ****************************************************************************
   3 *
   4 *    Zvector E7 instruction tests for VRR-c encoded:
   5 *
   6 *    E7F1 VACC   - Vector Add Compute Carry
   7 *    E7F3 VA     - Vector Add
   8 *    E7F5 VSCBI  - Vector Subtract Compute Borrow Indication
   9 *    E7F7 VS     - Vector Subtract
  10 *
  11 *        James Wekel March 2025
  12 ****************************************************************************

  14 ****************************************************************************
  15 *
  16 *        basic instruction tests
  17 *
  18 ****************************************************************************
  19 *   This program tests proper functioning of the z/arch E7 VRR-c Vector
  20 *   Add and Vector Subtract instructions.
  21 *
  22 *   Exceptions are not tested.
  23 *
  24 *   PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
  25 *   obvious coding errors.  None of the tests are thorough.  They are
  26 *   NOT designed to test all aspects of any of the instructions.
  27 *
  28 ****************************************************************************
  29 *
  30 *    *Testcase zvector-e7-17-AddSub
  31 *    *
  32 *    *    Zvector E7 instruction tests for VRR-c encoded:
  33 *    *
  34 *    *    E7F1 VACC   - Vector Add Compute Carry
  35 *    *    E7F3 VA     - Vector Add
  36 *    *    E7F5 VSCBI  - Vector Subtract Compute Borrow Indication
  37 *    *    E7F7 VS     - Vector Subtract
  38 *    *
  39 *    *    # -----------------------------------------------------------
  40 *    *    #  This tests only the basic function of the instructions.
  41 *    *    #  Exceptions are NOT tested.
  42 *    *    # -----------------------------------------------------------
  43 *    *
  44 *    mainsize    2
  45 *    numcpu      1
  46 *    sysclear
  47 *    archlvl     z/Arch
  48 *
  49 *    loadcore        "$(testpath)/zvector-e7-17-AddSub.core" 0x0
  50 *
  51 *    diag8cmd    enable    # (needed for messages to Hercules console)
  52 *    runtest     5
  53 *    diag8cmd    disable   # (reset back to default)
  54 *
  55 *    *Done
  56 *
```

 LOC   OBJECT CODE   ADDR1   ADDR2   STMT

                                                    57 **

```
  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

                                             59 ******************************************************************************
                                             60 *         FCHECK Macro - Is a Facility Bit set?
                                             61 *
                                             62 *         If the facility bit is NOT set, an message is issued and
                                             63 *         the test is skipped.
                                             64 *
                                             65 *         Fcheck uses R0, R1 and R2
                                             66 *
                                             67 * eg.     FCHECK 134,'vector-packed-decimal'
                                             68 ******************************************************************************
                                             69           MACRO
                                             70           FCHECK &BITNO,&NOTSETMSG
                                             71 .*                       &BITNO : facility bit number to check
                                             72 .*                       &NOTSETMSG : 'facility name'
                                             73           LCLA    &FBBYTE         Facility bit in Byte
                                             74           LCLA    &FBBIT          Facility bit within Byte
                                             75
                                             76           LCLA  &L(8)
                                             77 &L(1)     SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                             78
                                             79 &FBBYTE   SETA  &BITNO/8
                                             80 &FBBIT    SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                             81 .*        MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                             82
                                             83           B     X&SYSNDX
                                             84 *                                          Fcheck data area
                                             85 *                                          skip messgae
                                             86 SKT&SYSNDX DC  C'    Skipping tests: '
                                             87           DC    C&NOTSETMSG
                                             88           DC    C' (bit &BITNO) is not installed.'
                                             89 SKL&SYSNDX EQU *-SKT&SYSNDX
                                             90 *                                          facility bits
                                             91           DS    FD                         gap
                                             92 FB&SYSNDX DS  4FD
                                             93           DS    FD                         gap
                                             94 *
                                             95 X&SYSNDX EQU *
                                             96           LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                             97           STFLE FB&SYSNDX                get facility bits
                                             98
                                             99           XGR   R0,R0
                                            100           IC    R0,FB&SYSNDX+&FBBYTE    get fbit byte
                                            101           N     R0,=F'&FBBIT'           is bit set?
                                            102           BNZ   XC&SYSNDX
                                            103 *
                                            104 * facility bit not set, issue message and exit
                                            105 *
                                            106           LA    R0,SKL&SYSNDX           message length
                                            107           LA    R1,SKT&SYSNDX           message address
                                            108           BAL   R2,MSG
                                            109
                                            110           B     EOJ
                                            111 XC&SYSNDX EQU *
                                            112           MEND
```

```
 LOC          OBJECT CODE       ADDR1      ADDR2     STMT

                                                     114 ****************************************************************************
                                                     115 *       Low core PSWs
                                                     116 ****************************************************************************
                                00000000   0000355F  117 ZVE7TST   START 0
 00000000                       00000000             118           USING ZVE7TST,R0              Low core addressability
                                                     119
                                00000140   00000000  120 SVOLDPSW EQU     ZVE7TST+X'140'          z/Arch Supervisor call old PSW

 00000000                       00000000   000001A0  122           ORG   ZVE7TST+X'1A0'          z/Architecure RESTART PSW
 000001A0    00000001 80000000                       123           DC    X'0000000180000000'
 000001A8    00000000 00000200                       124           DC    AD(BEGIN)

 000001B0                       000001B0   000001D0  126           ORG   ZVE7TST+X'1D0'          z/Architecure PROGRAM CHECK PSW
 000001D0    00020001 80000000                       127           DC    X'0002000180000000'
 000001D8    00000000 0000DEAD                       128           DC    AD(X'DEAD')


 000001E0                       000001E0   00000200  130           ORG   ZVE7TST+X'200'          Start of actual test program..


                                                     132 ****************************************************************************
                                                     133 *                 The actual "ZVE7TST" program itself...
                                                     134 ****************************************************************************
                                                     135 *
                                                     136 *   Architecture Mode: z/Arch
                                                     137 *   Register Usage:
                                                     138 *
                                                     139 *    R0          (work)
                                                     140 *    R1-4        (work)
                                                     141 *    R5          Testing control table - current test base
                                                     142 *    R6-R7       (work)
                                                     143 *    R8          First base register
                                                     144 *    R9          Second base register
                                                     145 *    R10         Third base register
                                                     146 *    R11         E7TEST call return
                                                     147 *    R12         E7TESTS register
                                                     148 *    R13         (work)
                                                     149 *    R14         Subroutine call
                                                     150 *    R15         Secondary Subroutine call or work
                                                     151 *
                                                     152 ****************************************************************************

 00000200                       00000200             154           USING  BEGIN,R8              FIRST Base Register
 00000200                       00001200             155           USING  BEGIN+4096,R9         SECOND Base Register
 00000200                       00002200             156           USING  BEGIN+8192,R10        THIRD Base Register

 00000200    0580                                    158 BEGIN     BALR  R8,0                   Initialize FIRST base register
 00000202    0680                                    159           BCTR  R8,0                   Initialize FIRST base register
 00000204    0680                                    160           BCTR  R8,0                   Initialize FIRST base register

 00000206    4190 8800                     00000800  162           LA    R9,2048(,R8)           Initialize SECOND base register
 0000020A    4190 9800                     00000800  163           LA    R9,2048(,R9)           Initialize SECOND base register
                                                     164
```

```
  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

0000020E  41A0 9800                  00000800  165             LA     R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                  00000800  166             LA     R10,2048(,R10)   Initalize THIRD base register
                                               167
00000216  B600 828C                  0000048C  168             STCTL  R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 828D                  0000048D  169             OI     CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 828D                  0000048D  170             OI     CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 828C                  0000048C  171             LCTL   R0,R0,CTLR0      Reload updated CR0
                                               172
                                               173  *****************************************************************************
                                               174  * Is z/Architecture vector facility installed  (bit 129)
                                               175  *****************************************************************************
                                               176
                                               177             FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                  000002A8  178+            B      X0001
                                               179+*                                   Fcheck data area
                                               180+*                                   skip messgae
0000022A  40404040 E2928997                    181+SKT0001 DC     C'     Skipping tests: '
0000023E  A961C199 838889A3                    182+        DC     C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                    183+        DC     C' (bit 129) is not installed.'
                           0000004E  00000001  184+SKL0001 EQU    *-SKT0001
                                               185+*                                   facility bits
00000278  00000000 00000000                    186+        DS     FD               gap
00000280  00000000 00000000                    187+FB0001  DS     4FD
000002A0  00000000 00000000                    188+        DS     FD               gap
                                               189+*
                           000002A8  00000001  190+X0001   EQU    *
000002A8  4100 0004                  00000004  191+        LA     R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                  00000280  192+        STFLE  FB0001                get facility bits
000002B0  B982 0000                            193+        XGR    R0,R0
000002B4  4300 8090                  00000290  194+        IC     R0,FB0001+16          get fbit byte
000002B8  5400 8294                  00000494  195+        N      R0,=F'64'             is bit set?
000002BC  4770 80D0                  000002D0  196+        BNZ    XC0001
                                               197+*
                                               198+* facility bit not set, issue message and exit
                                               199+*
000002C0  4100 004E                  0000004E  200+        LA     R0,SKL0001            message length
000002C4  4110 802A                  0000022A  201+        LA     R1,SKT0001            message address
000002C8  4520 81A8                  000003A8  202+        BAL    R2,MSG
000002CC  47F0 8270                  00000470  203+        B      EOJ
                           000002D0  00000001  204+XC0001  EQU    *
```

```
  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

                                                 206 *******************************************************************
                                                 207 *              Do tests in the E7TESTS table
                                                 208 *******************************************************************
                                                 209
000002D0   58C0 8298                   00000498  210           L      R12,=A(E7TESTS)      get table of test addresses
                                                 211
                       000002D4  00000001        212 NEXTE7    EQU    *
000002D4   5850 C000                   00000000  213           L      R5,0(0,R12)          get test address
000002D8   1255                                  214           LTR    R5,R5                    have a test?
000002DA   4780 811E                   0000031E  215           BZ     ENDTEST                  done?
                                                 216
000002DE             00000000                    217           USING  E7TEST,R5
                                                 218
000002DE   4800 5004                   00000004  219           LH     R0,TNUM              save current test number
000002E2   5000 8E04                   00001004  220           ST     R0,TESTING           for easy reference
                                                 221
000002E6   E710 8E94 0006              00001094  222           VL     V1,V1FUDGE
000002EC   58B0 5000                   00000000  223           L      R11,TSUB             get address of test routine
000002F0   05BB                                  224           BALR   R11,R11              do test
                                                 225
000002F2   E310 501C 0014              0000001C  226           LGF    R1,READDR            get address of expected result
000002F8   D50F 5028 1000    00000028  00000000  227           CLC    V1OUTPUT,0(R1)       valid?
000002FE   4770 810A                   0000030A  228           BNE    FAILMSG                  no, issue failed message
                                                 229
00000302   41C0 C004                   00000004  230           LA     R12,4(0,R12)         next test address
00000306   47F0 80D4                   000002D4  231           B      NEXTE7
```

```
  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

                                                 233 ********************************************************************
                                                 234 * result not as expected:
                                                 235 *        issue message with test number, instruction under test
                                                 236 *                and instruction m4
                                                 237 ********************************************************************
                            0000030A  00000001   238 FAILMSG  EQU    *
0000030A  45F0 812C                     0000032C   239          BAL    R15,RPTERROR


                                                 241 ********************************************************************
                                                 242 * continue after a failed test
                                                 243 ********************************************************************
                            0000030E  00000001   244 FAILCONT EQU    *
0000030E  5800 829C                     0000049C   245          L      R0,=F'1'              set failed test indicator
00000312  5000 8E00                     00001000   246          ST     R0,FAILED
                                                 247
00000316  41C0 C004                     00000004   248          LA     R12,4(0,R12)      next test address
0000031A  47F0 80D4                     000002D4   249          B      NEXTE7


                                                 251 ********************************************************************
                                                 252 * end of testing; set ending psw
                                                 253 ********************************************************************
                            0000031E  00000001   254 ENDTEST  EQU    *
0000031E  5810 8E00                     00001000   255          L      R1,FAILED            did a test fail?
00000322  1211                                     256          LTR    R1,R1
00000324  4780 8270                     00000470   257          BZ     EOJ                  No, exit
00000328  47F0 8288                     00000488   258          B      FAILTEST             Yes, exit with BAD PSW
```

```
  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

                                                   260 ****************************************************************
                                                   261 *          RPTERROR                    Report instruction test in error
                                                   262 ****************************************************************
0000032C  50F0 8190                     00000390   264 RPTERROR ST    R15,RPTSAVE          Save return address
00000330  5050 8194                     00000394   265          ST    R5,RPTSVR5           Save R5
                                                   266 *
00000334  4820 5004                     00000004   267          LH    R2,TNUM              get test number and convert
00000338  4E20 8E73                     00001073   268          CVD   R2,DECNUM
0000033C  D211 8E5D 8E47      0000105D  00001047   269          MVC   PRT3,EDIT
00000342  DE11 8E5D 8E73      0000105D  00001073   270          ED    PRT3,DECNUM
00000348  D202 8E18 8E6A      00001018  0000106A   271          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                   272
0000034E  D207 8E33 5008      00001033  00000008   273          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                   274 *
00000354  E320 5007 0076                00000007   275          LB    R2,m4                get m4 and convert
0000035A  4E20 8E73                     00001073   276          CVD   R2,DECNUM
0000035E  D211 8E5D 8E47      0000105D  00001047   277          MVC   PRT3,EDIT
00000364  DE11 8E5D 8E73      0000105D  00001073   278          ED    PRT3,DECNUM
0000036A  D201 8E44 8E6B      00001044  0000106B   279          MVC   PRTM4(2),PRT3+14     fill in message with m4 field

                                                   281 *
                                                   282 *          Use Hercules Diagnose for Message to console
                                                   283 *
00000370  9002 8198                     00000398   284          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000374  4100 003F                     0000003F   285          LA    R0,PRTLNG            message length
00000378  4110 8E08                     00001008   286          LA    R1,PRTLINE           messagfe address
0000037C  4520 81A8                     000003A8   287          BAL   R2,MSG               call Hercules console MSG display
00000380  9802 8198                     00000398   288          LM    R0,R2,RPTDWSAV       restore regs


00000384  5850 8194                     00000394   290          L     R5,RPTSVR5           Restore R5
00000388  58F0 8190                     00000390   291          L     R15,RPTSAVE          Restore return address
0000038C  07FF                                     292          BR    R15                  Return to caller

00000390  00000000                                 294 RPTSAVE  DC    F'0'                 R15 save area
00000394  00000000                                 295 RPTSVR5  DC    F'0'                 R5 save area

00000398  00000000 00000000                        297 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE    ADDR1     ADDR2    STMT

                                               299 ****************************************************************************
                                               300 *          Issue HERCULES MESSAGE pointed to by R1, length in R0
                                               301 *               R2 = return address
                                               302 ****************************************************************************

000003A8  4900 82A0                  000004A0  304 MSG      CH    R0,=H'0'              Do we even HAVE a message?
000003AC  07D2                                 305          BNHR  R2                    No, ignore

000003AE  9002 81E4                  000003E4  307          STM   R0,R2,MSGSAVE         Save registers

000003B2  4900 82A2                  000004A2  309          CH    R0,=AL2(L'MSGMSG)     Message length within limits?
000003B6  47D0 81BE                  000003BE  310          BNH   MSGOK                 Yes, continue
000003BA  4100 005F                  0000005F  311          LA    R0,L'MSGMSG          No, set to maximum

000003BE  1820                                 313 MSGOK    LR    R2,R0                 Copy length to work register
000003C0  0620                                 314          BCTR  R2,0                  Minus-1 for execute
000003C2  4420 81F0                  000003F0  315          EX    R2,MSGMVC             Copy message to O/P buffer

000003C6  4120 200A                  0000000A  317          LA    R2,1+L'MSGCMD(,R2)    Calculate true command length
000003CA  4110 81F6                  000003F6  318          LA    R1,MSGCMD             Point to true command

000003CE  83120008                             320          DC    X'83',X'12',X'0008'   Issue Hercules Diagnose X'008'
000003D2  4780 81DE                  000003DE  321          BZ    MSGRET                Return if successful
                                               322
000003D6  1222                                 323          LTR   R2,R2                 Is Diag8 Ry (R2) 0?
000003D8  4780 81DE                  000003DE  324          BZ    MSGRET                 an error occurred but coninue
                                               325
000003DC  0000                                 326          DC    H'0'                  CRASH for debugging purposes

000003DE  9802 81E4                  000003E4  328 MSGRET   LM    R0,R2,MSGSAVE         Restore registers
000003E2  07F2                                 329          BR    R2                    Return to caller



000003E4  00000000 00000000                    331 MSGSAVE  DC    3F'0'                 Registers save area
000003F0  D200 81FF 1000   000003FF  00000000  332 MSGMVC   MVC   MSGMSG(0),0(R1)       Executed instruction

000003F6  D4E2C7D5 D6C8405C                     334 MSGCMD   DC    C'MSGNOH * '          *** HERCULES MESSAGE COMMAND ***
000003FF  40404040 40404040                     335 MSGMSG   DC    CL95' '              The message text to be displayed
                                               336
```

```
 LOC          OBJECT CODE      ADDR1     ADDR2    STMT

                                                  338 ****************************************************************************
                                                  339 *          Normal completion or Abnormal termination PSWs
                                                  340 ****************************************************************************


00000460    00020001 80000000                     342 EOJPSW   DC     0D'0',X'0002000180000000',AD(0)

00000470    B2B2 8260                   00000460   344 EOJ      LPSWE EOJPSW               Normal completion


00000478    00020001 80000000                     346 FAILPSW  DC     0D'0',X'0002000180000000',AD(X'BAD')

00000488    B2B2 8278                   00000478   348 FAILTEST LPSWE FAILPSW              Abnormal termination



                                                  350 ****************************************************************************
                                                  351 *          Working Storage
                                                  352 ****************************************************************************


0000048C    00000000                              354 CTLR0    DS     F                    CR0
00000490    00000000                              355          DS     F

00000494                                          357          LTORG ,                     Literals pool
00000494    00000040                              358                 =F'64'
00000498    00003460                              359                 =A(E7TESTS)
0000049C    00000001                              360                 =F'1'
000004A0    0000                                  361                 =H'0'
000004A2    005F                                  362                 =AL2(L'MSGMSG)
                                                  363
                                                  364 *          some constants
                                                  365
                         00000400    00000001     366 K        EQU    1024                 One KB
                         00001000    00000001     367 PAGE     EQU    (4*K)                Size of one page
                         00010000    00000001     368 K64      EQU    (64*K)               64 KB
                         00100000    00000001     369 MB       EQU    (K*K)                 1 MB
                                                  370
                         AABBCCDD    00000001     371 REG2PATT EQU    X'AABBCCDD'          Polluted Register pattern
                         000000DD    00000001     372 REG2LOW  EQU          X'DD'          (last byte above)
```

```
   LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  374 *=============================================================================
                                                  375 *
                                                  376 *   NOTE: start data on an address that is easy to display
                                                  377 *         within Hercules
                                                  378 *
                                                  379 *=============================================================================
                                                  380
000004A4                       000004A4  00001000 381           ORG    ZVE7TST+X'1000'
00001000   00000000                                382 FAILED    DC     F'0'                           some test failed?
00001004   00000000                                383 TESTING   DC     F'0'                           current test number

                                                  385 *
                                                  386 *          failed message and associated editting
                                                  387 *
00001008   40404040 40404040                       388 PRTLINE   DC     C'          Test # '
00001018   A7A7A7                                  389 PRTNUM    DC     C'xxx'
0000101B   40868189 93858440                       390           DC     c' failed for instruction '
00001033   A7A7A7A7 A7A7A7A7                        391 PRTNAME   DC     CL8'xxxxxxxx'
0000103B   40A689A3 884094F4                        392           DC     C' with m4='
00001044   A7A7                                    393 PRTm4     DC     C'xx'
00001046   4B                                      394           DC     C'.'
                               0000003F  00000001 395 PRTLNG    EQU    *-PRTLINE
```

```
  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

                                                   397 ********************************************************************
                                                   398 *          TEST failed : message working storge
                                                   399 ********************************************************************
00001047   40212020 20202020                       400 EDIT      DC     XL18'402120202020202020202020202020202020'
                                                   401
00001059   7E7E7E6E                                 402        DC     C' ===>'
0000105D   40404040 40404040                        403 PRT3      DC     CL18' '
0000106F   4C7E7E7E                                 404        DC     C' <==='
00001073   00000000 00000000                       405 DECNUM    DS     CL16


                                                   407 ********************************************************************
                                                   408 *          Vector instruction results, pollution and input
                                                   409 ********************************************************************
00001084                                           410        DS     0F
00001084   00000000 00000000                       411        DS     XL16                                            gap
00001094   FFFFFFFF FFFFFFFF                        412 V1FUDGE   DC     XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'      V1 FUDGE
000010A4   00000000 00000000                       413        DS     XL16
```

```
   LOC         OBJECT CODE      ADDR1     ADDR2    STMT

                                                   415 ****************************************************************************
                                                   416 *          E7TEST DSECT
                                                   417 ****************************************************************************

                                                   419 E7TEST    DSECT ,
00000000   00000000                                420 TSUB      DC     A(0)             pointer  to test
00000004   0000                                    421 TNUM      DC     H'00'            Test Number
00000006   00                                      422           DC     X'00'
00000007   00                                      423 M4        DC     HL1'00'          m4 used
                                                   424
00000008   40404040 40404040                       425 OPNAME    DC     CL8' '           E7 name
00000010   00000000                                426 V2ADDR    DC     A(0)             address of v2 source
00000014   00000000                                427 V3ADDR    DC     A(0)             address of v3 source
00000018   00000000                                428 RELEN     DC     A(0)             RESULT LENGTH
0000001C   00000000                                429 READDR    DC     A(0)             result (expected) address
00000020   00000000 00000000                       430           DS     FD                  gap
00000028   00000000 00000000                       431 V1OUTPUT  DS     XL16             V1 Output
00000038   00000000 00000000                       432           DS     FD                  gap
                                                   433
                                                   434 *          test routine will be here (from VRR-c macro)
                                                   435 *
                                                   436 *          followed by
                                                   437 *              EXPECTED RESULT

                        00000000  0000355F         439 ZVE7TST   CSECT ,
000010B4                                           440           DS     0F

                                                   442 ****************************************************************************
                                                   443 *     Macros to help build test tables
                                                   444 ****************************************************************************

                                                   446 *
                                                   447 * macro to generate individual test
                                                   448 *
                                                   449           MACRO
                                                   450           VRR_C &INST,&M4
                                                   451 .*                                  &INST   - VRR-c instruction under test
                                                   452 .*                                  &m4     - m4 field
                                                   453
                                                   454           GBLA   &TNUM
                                                   455 &TNUM     SETA   &TNUM+1
                                                   456
                                                   457           DS     0FD
                                                   458           USING *,R5               base for test data and test routine
                                                   459
                                                   460 T&TNUM    DC     A(X&TNUM)         address of test routine
                                                   461           DC     H'&TNUM'         test number
                                                   462           DC     X'00'
                                                   463           DC     HL1'&M4'         m4
                                                   464           DC     CL8'&INST'       instruction name
                                                   465           DC     A(RE&TNUM+16)    address of v2 source
```

```
  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

                                                466            DC      A(RE&TNUM+32)       address of v3 source
                                                467            DC      A(16)               result length
                                                468 REA&TNUM DC      A(RE&TNUM)          result address
                                                469            DS      FD                  gap
                                                470 V10&TNUM DS      XL16                V1 output
                                                471            DS      FD                  gap
                                                472 .*
                                                473 *
                                                474 X&TNUM    DS      0F
                                                475            LGF     R1,V2ADDR           load v2 source
                                                476            VL      v22,0(R1)           use v22 to test decoder
                                                477
                                                478            LGF     R1,V3ADDR           load v3 source
                                                479            VL      v23,0(R1)           use v23 to test decoder
                                                480
                                                481            &INST V22,V22,V23,&M4     test instruction (dest is a source)
                                                482            VST     V22,V10&TNUM       save v1 output
                                                483
                                                484            BR      R11                 return
                                                485
                                                486 RE&TNUM   DC      0F                  xl16 expected result
                                                487
                                                488            DROP    R5
                                                489            MEND


                                                491 *
                                                492 * macro to generate table of pointers to individual tests
                                                493 *
                                                494            MACRO
                                                495            PTTABLE
                                                496            GBLA    &TNUM
                                                497            LCLA    &CUR
                                                498 &CUR      SETA    1
                                                499 .*
                                                500 TTABLE    DS      0F
                                                501 .LOOP     ANOP
                                                502 .*
                                                503            DC      A(T&CUR)
                                                504 .*
                                                505 &CUR      SETA    &CUR+1
                                                506            AIF     (&CUR LE &TNUM).LOOP
                                                507 *
                                                508            DC      A(0)                END OF TABLE
                                                509            DC      A(0)
                                                510 .*
                                                511            MEND
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				513	***			
				514	*	E7 VRR-c tests		
				515	***			
				516		PRINT DATA		
				517	*			
				518	*	E7F1 VACC	- Vector Add Compute Carry	
				519	*	E7F3 VA	- Vector Add	
				520	*	E7F5 VSCBI	- Vector Subtract Compute Borrow Indication	
				521	*	E7F7 VS	- Vector Subtract	
				522	*			
				523	*		VRR-c instruction, m4	
				524	*		followed by	
				525	*		16 byte expected result (V1)	
				526	*		16 byte V2 source	
				527	*		16 byte V3 source	
				528	*			
				529	*--			
				530	* VA	- Vector Add		
				531	*--			
				532	*Byte			
				533		VRR_C VA,0		
000010B8				534+		DS	0FD	
000010B8			000010B8	535+		USING	*,R5	base for test data and test routine
000010B8	000010F8			536+T1		DC	A(X1)	address of test routine
000010BC	0001			537+		DC	H'1'	test number
000010BE	00			538+		DC	X'00'	
000010BF	00			539+		DC	HL1'0'	m4
000010C0	E5C14040 40404040			540+		DC	CL8'VA'	instruction name
000010C8	00001130			541+		DC	A(RE1+16)	address of v2 source
000010CC	00001140			542+		DC	A(RE1+32)	address of v3 source
000010D0	00000010			543+		DC	A(16)	result length
000010D4	00001120			544+REA1		DC	A(RE1)	result address
000010D8	00000000 00000000			545+		DS	FD	gap
000010E0	00000000 00000000			546+V101		DS	XL16	V1 output
000010E8	00000000 00000000							
000010F0	00000000 00000000			547+		DS	FD	gap
				548+*				
000010F8				549+X1		DS	0F	
000010F8	E310 5010 0014		00000010	550+		LGF	R1,V2ADDR	load v2 source
000010FE	E761 0000 0806		00000000	551+		VL	v22,0(R1)	use v22 to test decoder
00001104	E310 5014 0014		00000014	552+		LGF	R1,V3ADDR	load v3 source
0000110A	E771 0000 0806		00000000	553+		VL	v23,0(R1)	use v23 to test decoder
00001110	E766 7000 0EF3			554+		VA	V22,V22,V23,0	test instruction (dest is a source)
00001116	E760 5028 080E		000010E0	555+		VST	V22,V101	save v1 output
0000111C	07FB			556+		BR	R11	return
00001120				557+RE1		DC	0F	xl16 expected result
00001120				558+		DROP	R5	
00001120	00010203 04050607			559		DC	XL16'0001020304050607 0A0C0E1012141608'	result
00001128	0A0C0E10 12141608							
00001130	FFFFFFFF FFFFFFFF			560		DC	XL16'FFFFFFFFFFFFFFFF 0102030405060708'	v2
00001138	01020304 05060708							
00001140	01020304 05060708			561		DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v3
00001148	090A0B0C 0D0E0F00							
				562				
				563		VRR_C VA,0		
00001150				564+		DS	0FD	

```
  LOC         OBJECT CODE      ADDR1    ADDR2    STMT


00001150                      00001150          565+          USING *,R5              base for test data and test routine
00001150  00001190                              566+T2        DC    A(X2)            address of test routine
00001154  0002                                  567+          DC    H'2'             test number
00001156  00                                    568+          DC    X'00'
00001157  00                                    569+          DC    HL1'0'              m4
00001158  E5C14040 40404040                     570+          DC    CL8'VA'          instruction name
00001160  000011C8                              571+          DC    A(RE2+16)        address of v2 source
00001164  000011D8                              572+          DC    A(RE2+32)        address of v3 source
00001168  00000010                              573+          DC    A(16)            result length
0000116C  000011B8                              574+REA2      DC    A(RE2)           result address
00001170  00000000 00000000                     575+          DS    FD               gap
00001178  00000000 00000000                     576+V102      DS    XL16             V1 output
00001180  00000000 00000000
00001188  00000000 00000000                     577+          DS    FD               gap
                                                578+*
00001190                                        579+X2        DS    0F
00001190  E310 5010 0014                00000010 580+         LGF   R1,V2ADDR        load v2 source
00001196  E761 0000 0806                00000000 581+         VL    v22,0(R1)        use v22 to test decoder
0000119C  E310 5014 0014                00000014 582+         LGF   R1,V3ADDR        load v3 source
000011A2  E771 0000 0806                00000000 583+         VL    v23,0(R1)        use v23 to test decoder
000011A8  E766 7000 0EF3                         584+         VA    V22,V22,V23,0     test instruction (dest is a source)
000011AE  E760 5028 080E                00001178 585+         VST   V22,V102          save v1 output
000011B4  07FB                                   586+         BR    R11              return
000011B8                                         587+RE2      DC    0F               xl16 expected result
000011B8                                         588+         DROP  R5
000011B8  02040608 0A0C0E10                      589          DC    XL16'020406080A0C0E10 08090A0B0C0D0EFF'    result
000011C0  08090A0B 0C0D0EFF
000011C8  01020304 05060708                      590          DC    XL16'0102030405060708 090A0B0C0D0E0F00'    v2
000011D0  090A0B0C 0D0E0F00
000011D8  01020304 05060708                      591          DC    XL16'0102030405060708 FFFFFFFFFFFFFFFF'    v3
000011E0  FFFFFFFF FFFFFFFF
                                                 592
                                                 593          VRR_C VA,0
000011E8                                         594+         DS    0FD
000011E8                      000011E8          595+          USING *,R5              base for test data and test routine
000011E8  00001228                              596+T3        DC    A(X3)            address of test routine
000011EC  0003                                  597+          DC    H'3'             test number
000011EE  00                                    598+          DC    X'00'
000011EF  00                                    599+          DC    HL1'0'              m4
000011F0  E5C14040 40404040                     600+          DC    CL8'VA'          instruction name
000011F8  00001260                              601+          DC    A(RE3+16)        address of v2 source
000011FC  00001270                              602+          DC    A(RE3+32)        address of v3 source
00001200  00000010                              603+          DC    A(16)            result length
00001204  00001250                              604+REA3      DC    A(RE3)           result address
00001208  00000000 00000000                     605+          DS    FD               gap
00001210  00000000 00000000                     606+V103      DS    XL16             V1 output
00001218  00000000 00000000
00001220  00000000 00000000                     607+          DS    FD               gap
                                                 608+*
00001228                                        609+X3        DS    0F
00001228  E310 5010 0014                00000010 610+         LGF   R1,V2ADDR        load v2 source
0000122E  E761 0000 0806                00000000 611+         VL    v22,0(R1)        use v22 to test decoder
00001234  E310 5014 0014                00000014 612+         LGF   R1,V3ADDR        load v3 source
0000123A  E771 0000 0806                00000000 613+         VL    v23,0(R1)        use v23 to test decoder
00001240  E766 7000 0EF3                         614+         VA    V22,V22,V23,0     test instruction (dest is a source)
00001246  E760 9010 080E                00001210 615+         VST   V22,V103          save v1 output
```

```
  LOC          OBJECT CODE       ADDR1     ADDR2      STMT

0000124C  07FB                                        616+         BR    R11               return
00001250                                              617+RE3      DC    0F                xl16 expected result
00001250                                              618+         DROP  R5
00001250  FFFFFFFF FFFFFFFF                            619          DC    XL16'FFFFFFFFFFFFFFFF 07070707070707F7'    result
00001258  07070707 070707F7
00001260  FEFDFCFB FAF9F8F7                            620          DC    XL16'FEFDFCFBFAF9F8F7 090A0B0C0D0E0F00'    v2
00001268  090A0B0C 0D0E0F00
00001270  01020304 05060708                            621          DC    XL16'0102030405060708 FEFDFCFBFAF9F8F7'    v3
00001278  FEFDFCFB FAF9F8F7
                                                       622
                                                       623 *Halfword
                                                       624          VRR_C VA,1
00001280                                               625+         DS    0FD
00001280                               00001280        626+         USING *,R5               base for test data and test routine
00001280  000012C0                                     627+T4       DC    A(X4)              address of test routine
00001284  0004                                         628+         DC    H'4'               test number
00001286  00                                           629+         DC    X'00'
00001287  01                                           630+         DC    HL1'1'             m4
00001288  E5C14040 40404040                            631+         DC    CL8'VA'            instruction name
00001290  000012F8                                     632+         DC    A(RE4+16)          address of v2 source
00001294  00001308                                     633+         DC    A(RE4+32)          address of v3 source
00001298  00000010                                     634+         DC    A(16)              result length
0000129C  000012E8                                     635+REA4     DC    A(RE4)             result address
000012A0  00000000 00000000                            636+         DS    FD                gap
000012A8  00000000 00000000                            637+V104     DS    XL16              V1 output
000012B0  00000000 00000000
000012B8  00000000 00000000                            638+         DS    FD                gap
                                                       639+*
000012C0                                               640+X4       DS    0F
000012C0  E310 5010 0014              00000010         641+         LGF   R1,V2ADDR          load v2 source
000012C6  E761 0000 0806              00000000         642+         VL    v22,0(R1)          use v22 to test decoder
000012CC  E310 5014 0014              00000014         643+         LGF   R1,V3ADDR          load v3 source
000012D2  E771 0000 0806              00000000         644+         VL    v23,0(R1)          use v23 to test decoder
000012D8  E766 7000 1EF3                               645+         VA    V22,V22,V23,1       test instruction (dest is a source)
000012DE  E760 5028 080E              000012A8         646+         VST   V22,V104            save v1 output
000012E4  07FB                                         647+         BR    R11               return
000012E8                                               648+RE4      DC    0F                xl16 expected result
000012E8                                               649+         DROP  R5
000012E8  01010303 05050707                            650          DC    XL16'0101030305050707 0A0C0E1012141608'    result
000012F0  0A0C0E10 12141608
000012F8  FFFFFFFF FFFFFFFF                            651          DC    XL16'FFFFFFFFFFFFFFFF 0102030405060708'    v2
00001300  01020304 05060708
00001308  01020304 05060708                            652          DC    XL16'0102030405060708 090A0B0C0D0E0F00'    v3
00001310  090A0B0C 0D0E0F00
                                                       653
                                                       654          VRR_C VA,1
00001318                                               655+         DS    0FD
00001318                               00001318        656+         USING *,R5               base for test data and test routine
00001318  00001358                                     657+T5       DC    A(X5)              address of test routine
0000131C  0005                                         658+         DC    H'5'               test number
0000131E  00                                           659+         DC    X'00'
0000131F  01                                           660+         DC    HL1'1'             m4
00001320  E5C14040 40404040                            661+         DC    CL8'VA'            instruction name
00001328  00001390                                     662+         DC    A(RE5+16)          address of v2 source
0000132C  000013A0                                     663+         DC    A(RE5+32)          address of v3 source
00001330  00000010                                     664+         DC    A(16)              result length
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00001334   00001380                              665+REA5    DC     A(RE5)              result address
00001338   00000000 00000000                     666+        DS     FD                  gap
00001340   00000000 00000000                     667+V105    DS     XL16                V1 output
00001348   00000000 00000000
00001350   00000000 00000000                     668+        DS     FD                  gap
                                                 669+*
00001358                                         670+X5      DS     0F
00001358   E310 5010 0014              00000010  671+        LGF    R1,V2ADDR           load v2 source
0000135E   E761 0000 0806              00000000  672+        VL     v22,0(R1)           use v22 to test decoder
00001364   E310 5014 0014              00000014  673+        LGF    R1,V3ADDR           load v3 source
0000136A   E771 0000 0806              00000000  674+        VL     v23,0(R1)           use v23 to test decoder
00001370   E766 7000 1EF3                        675+        VA     V22,V22,V23,1        test instruction (dest is a source)
00001376   E760 5028 080E              00001340  676+        VST    V22,V105             save v1 output
0000137C   07FB                                  677+        BR     R11                 return
00001380                                         678+RE5     DC     0F                  xl16 expected result
00001380                                         679+        DROP   R5
00001380   02040608 0A0C0E10                     680         DC     XL16'020406080A0C0E10 09090B0B0D0D0EFF'    result
00001388   09090B0B 0D0D0EFF
00001390   01020304 05060708                     681         DC     XL16'0102030405060708 090A0B0C0D0E0F00'    v2
00001398   090A0B0C 0D0E0F00
000013A0   01020304 05060708                     682         DC     XL16'0102030405060708 FFFFFFFFFFFFFFFF'    v3
000013A8   FFFFFFFF FFFFFFFF

                                                 683
                                                 684         VRR_C  VA,1
000013B0                                         685+        DS     0FD
000013B0                          000013B0       686+        USING  *,R5                base for test data and test routine
000013B0   000013F0                              687+T6      DC     A(X6)               address of test routine
000013B4   0006                                  688+        DC     H'6'                test number
000013B6   00                                    689+        DC     X'00'
000013B7   01                                    690+        DC     HL1'1'              m4
000013B8   E5C14040 40404040                     691+        DC     CL8'VA'             instruction name
000013C0   00001428                              692+        DC     A(RE6+16)           address of v2 source
000013C4   00001438                              693+        DC     A(RE6+32)           address of v3 source
000013C8   00000010                              694+        DC     A(16)               result length
000013CC   00001418                              695+REA6    DC     A(RE6)              result address
000013D0   00000000 00000000                     696+        DS     FD                  gap
000013D8   00000000 00000000                     697+V106    DS     XL16                V1 output
000013E0   00000000 00000000
000013E8   00000000 00000000                     698+        DS     FD                  gap
                                                 699+*
000013F0                                         700+X6      DS     0F
000013F0   E310 5010 0014              00000010  701+        LGF    R1,V2ADDR           load v2 source
000013F6   E761 0000 0806              00000000  702+        VL     v22,0(R1)           use v22 to test decoder
000013FC   E310 5014 0014              00000014  703+        LGF    R1,V3ADDR           load v3 source
00001402   E771 0000 0806              00000000  704+        VL     v23,0(R1)           use v23 to test decoder
00001408   E766 7000 1EF3                        705+        VA     V22,V22,V23,1        test instruction (dest is a source)
0000140E   E760 5028 080E              000013D8  706+        VST    V22,V106             save v1 output
00001414   07FB                                  707+        BR     R11                 return
00001418                                         708+RE6     DC     0F                  xl16 expected result
00001418                                         709+        DROP   R5
00001418   FFFFFFFF FFFFFFFF                     710         DC     XL16'FFFFFFFFFFFFFFFF 08070807080707F7'    result
00001420   08070807 080707F7
00001428   FEFDFCFB FAF9F8F7                     711         DC     XL16'FEFDFCFBFAF9F8F7 090A0B0C0D0E0F00'    v2
00001430   090A0B0C 0D0E0F00
00001438   01020304 05060708                     712         DC     XL16'0102030405060708 FEFDFCFBFAF9F8F7'    v3
00001440   FEFDFCFB FAF9F8F7
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				713			
				714	*Word		
				715		VRR_C	VA,2
00001448				716+	DS	0FD	
00001448		00001448		717+	USING	*,R5	base for test data and test routine
00001448	00001488			718+T7	DC	A(X7)	address of test routine
0000144C	0007			719+	DC	H'7'	test number
0000144E	00			720+	DC	X'00'	
0000144F	02			721+	DC	HL1'2'	m4
00001450	E5C14040 40404040			722+	DC	CL8'VA'	instruction name
00001458	000014C0			723+	DC	A(RE7+16)	address of v2 source
0000145C	000014D0			724+	DC	A(RE7+32)	address of v3 source
00001460	00000010			725+	DC	A(16)	result length
00001464	000014B0			726+REA7	DC	A(RE7)	result address
00001468	00000000 00000000			727+	DS	FD	gap
00001470	00000000 00000000			728+V107	DS	XL16	V1 output
00001478	00000000 00000000						
00001480	00000000 00000000			729+	DS	FD	gap
				730+*			
00001488				731+X7	DS	0F	
00001488	E310 5010 0014		00000010	732+	LGF	R1,V2ADDR	load v2 source
0000148E	E761 0000 0806		00000000	733+	VL	v22,0(R1)	use v22 to test decoder
00001494	E310 5014 0014		00000014	734+	LGF	R1,V3ADDR	load v3 source
0000149A	E771 0000 0806		00000000	735+	VL	v23,0(R1)	use v23 to test decoder
000014A0	E766 7000 2EF3			736+	VA	V22,V22,V23,2	test instruction (dest is a source)
000014A6	E760 5028 080E		00001470	737+	VST	V22,V107	save v1 output
000014AC	07FB			738+	BR	R11	return
000014B0				739+RE7	DC	0F	xl16 expected result
000014B0				740+	DROP	R5	
000014B0	01020303 05060707			741	DC	XL16'0102030305060707 0A0C0E1012141608'	result
000014B8	0A0C0E10 12141608						
000014C0	FFFFFFFF FFFFFFFF			742	DC	XL16'FFFFFFFFFFFFFFFF 0102030405060708'	v2
000014C8	01020304 05060708						
000014D0	01020304 05060708			743	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v3
000014D8	090A0B0C 0D0E0F00						
				744			
				745		VRR_C	VA,2
000014E0				746+	DS	0FD	
000014E0		000014E0		747+	USING	*,R5	base for test data and test routine
000014E0	00001520			748+T8	DC	A(X8)	address of test routine
000014E4	0008			749+	DC	H'8'	test number
000014E6	00			750+	DC	X'00'	
000014E7	02			751+	DC	HL1'2'	m4
000014E8	E5C14040 40404040			752+	DC	CL8'VA'	instruction name
000014F0	00001558			753+	DC	A(RE8+16)	address of v2 source
000014F4	00001568			754+	DC	A(RE8+32)	address of v3 source
000014F8	00000010			755+	DC	A(16)	result length
000014FC	00001548			756+REA8	DC	A(RE8)	result address
00001500	00000000 00000000			757+	DS	FD	gap
00001508	00000000 00000000			758+V108	DS	XL16	V1 output
00001510	00000000 00000000						
00001518	00000000 00000000			759+	DS	FD	gap
				760+*			
00001520				761+X8	DS	0F	
00001520	E310 5010 0014		00000010	762+	LGF	R1,V2ADDR	load v2 source
00001526	E761 0000 0806		00000000	763+	VL	v22,0(R1)	use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000152C	E310 5014 0014		00000014	764+	LGF	R1,V3ADDR	load v3 source
00001532	E771 0000 0806		00000000	765+	VL	v23,0(R1)	use v23 to test decoder
00001538	E766 7000 2EF3			766+	VA	V22,V22,V23,2	test instruction (dest is a source)
0000153E	E760 5028 080E		00001508	767+	VST	V22,V108	save v1 output
00001544	07FB			768+	BR	R11	return
00001548				769+RE8	DC	0F	xl16 expected result
00001548				770+	DROP	R5	
00001548	02040608 0A0C0E10			771	DC	XL16'020406080A0C0E10 090A0B0B0D0E0EFF'	result
00001550	090A0B0B 0D0E0EFF						
00001558	01020304 05060708			772	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v2
00001560	090A0B0C 0D0E0F00						
00001568	01020304 05060708			773	DC	XL16'0102030405060708 FFFFFFFFFFFFFFFF'	v3
00001570	FFFFFFFF FFFFFFFF						
				774			
				775	VRR_C	VA,2	
00001578				776+	DS	0FD	
00001578			00001578	777+	USING	*,R5	base for test data and test routine
00001578	000015B8			778+T9	DC	A(X9)	address of test routine
0000157C	0009			779+	DC	H'9'	test number
0000157E	00			780+	DC	X'00'	
0000157F	02			781+	DC	HL1'2'	m4
00001580	E5C14040 40404040			782+	DC	CL8'VA'	instruction name
00001588	000015F0			783+	DC	A(RE9+16)	address of v2 source
0000158C	00001600			784+	DC	A(RE9+32)	address of v3 source
00001590	00000010			785+	DC	A(16)	result length
00001594	000015E0			786+REA9	DC	A(RE9)	result address
00001598	00000000 00000000			787+	DS	FD	gap
000015A0	00000000 00000000			788+V109	DS	XL16	V1 output
000015A8	00000000 00000000						
000015B0	00000000 00000000			789+	DS	FD	gap
				790+*			
000015B8				791+X9	DS	0F	
000015B8	E310 5010 0014		00000010	792+	LGF	R1,V2ADDR	load v2 source
000015BE	E761 0000 0806		00000000	793+	VL	v22,0(R1)	use v22 to test decoder
000015C4	E310 5014 0014		00000014	794+	LGF	R1,V3ADDR	load v3 source
000015CA	E771 0000 0806		00000000	795+	VL	v23,0(R1)	use v23 to test decoder
000015D0	E766 7000 2EF3			796+	VA	V22,V22,V23,2	test instruction (dest is a source)
000015D6	E760 5028 080E		000015A0	797+	VST	V22,V109	save v1 output
000015DC	07FB			798+	BR	R11	return
000015E0				799+RE9	DC	0F	xl16 expected result
000015E0				800+	DROP	R5	
000015E0	FFFFFFFF FFFFFFFF			801	DC	XL16'FFFFFFFFFFFFFFFF 08080807080807F7'	result
000015E8	08080807 080807F7						
000015F0	FEFDFCFB FAF9F8F7			802	DC	XL16'FEFDFCFBFAF9F8F7 090A0B0C0D0E0F00'	v2
000015F8	090A0B0C 0D0E0F00						
00001600	01020304 05060708			803	DC	XL16'0102030405060708 FEFDFCFBFAF9F8F7'	v3
00001608	FEFDFCFB FAF9F8F7						
				804			
				805	*Doubleword		
				806	VRR_C	VA,3	
00001610				807+	DS	0FD	
00001610			00001610	808+	USING	*,R5	base for test data and test routine
00001610	00001650			809+T10	DC	A(X10)	address of test routine
00001614	000A			810+	DC	H'10'	test number
00001616	00			811+	DC	X'00'	
00001617	03			812+	DC	HL1'3'	m4

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  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

00001618  E5C14040 40404040                    813+           DC      CL8'VA'            instruction name
00001620  00001688                             814+           DC      A(RE10+16)         address of v2 source
00001624  00001698                             815+           DC      A(RE10+32)         address of v3 source
00001628  00000010                             816+           DC      A(16)              result length
0000162C  00001678                             817+REA10      DC      A(RE10)            result address
00001630  00000000 00000000                    818+           DS      FD                 gap
00001638  00000000 00000000                    819+V1010      DS      XL16               V1 output
00001640  00000000 00000000
00001648  00000000 00000000                    820+           DS      FD                 gap
                                               821+*
00001650                                       822+X10        DS      0F
00001650  E310 5010 0014             00000010  823+           LGF     R1,V2ADDR          load v2 source
00001656  E761 0000 0806             00000000  824+           VL      v22,0(R1)          use v22 to test decoder
0000165C  E310 5014 0014             00000014  825+           LGF     R1,V3ADDR          load v3 source
00001662  E771 0000 0806             00000000  826+           VL      v23,0(R1)          use v23 to test decoder
00001668  E766 7000 3EF3                       827+           VA      V22,V22,V23,3       test instruction (dest is a source)
0000166E  E760 5028 080E             00001638  828+           VST     V22,V1010           save v1 output
00001674  07FB                                 829+           BR      R11                return
00001678                                       830+RE10       DC      0F                 xl16 expected result
00001678                                       831+           DROP    R5
00001678  01020304 05060707                    832            DC      XL16'0102030405060707 0A0C0E1012141608'    result
00001680  0A0C0E10 12141608
00001688  FFFFFFFF FFFFFFFF                     833            DC      XL16'FFFFFFFFFFFFFFFF 0102030405060708'    v2
00001690  01020304 05060708
00001698  01020304 05060708                     834            DC      XL16'0102030405060708 090A0B0C0D0E0F00'    v3
000016A0  090A0B0C 0D0E0F00
                                               835
                                               836            VRR_C   VA,3
000016A8                                       837+           DS      0FD
000016A8           000016A8                    838+           USING   *,R5               base for test data and test routine
000016A8  000016E8                             839+T11        DC      A(X11)             address of test routine
000016AC  000B                                 840+           DC      H'11'              test number
000016AE  00                                   841+           DC      X'00'
000016AF  03                                   842+           DC      HL1'3'             m4
000016B0  E5C14040 40404040                    843+           DC      CL8'VA'            instruction name
000016B8  00001720                             844+           DC      A(RE11+16)         address of v2 source
000016BC  00001730                             845+           DC      A(RE11+32)         address of v3 source
000016C0  00000010                             846+           DC      A(16)              result length
000016C4  00001710                             847+REA11      DC      A(RE11)            result address
000016C8  00000000 00000000                    848+           DS      FD                 gap
000016D0  00000000 00000000                    849+V1011      DS      XL16               V1 output
000016D8  00000000 00000000
000016E0  00000000 00000000                    850+           DS      FD                 gap
                                               851+*
000016E8                                       852+X11        DS      0F
000016E8  E310 5010 0014             00000010  853+           LGF     R1,V2ADDR          load v2 source
000016EE  E761 0000 0806             00000000  854+           VL      v22,0(R1)          use v22 to test decoder
000016F4  E310 5014 0014             00000014  855+           LGF     R1,V3ADDR          load v3 source
000016FA  E771 0000 0806             00000000  856+           VL      v23,0(R1)          use v23 to test decoder
00001700  E766 7000 3EF3                       857+           VA      V22,V22,V23,3       test instruction (dest is a source)
00001706  E760 5028 080E             000016D0  858+           VST     V22,V1011           save v1 output
0000170C  07FB                                 859+           BR      R11                return
00001710                                       860+RE11       DC      0F                 xl16 expected result
00001710                                       861+           DROP    R5
00001710  02040608 0A0C0E10                    862            DC      XL16'020406080A0C0E10 090A0B0C0D0E0EFF'    result
00001718  090A0B0C 0D0E0EFF
```

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  LOC        OBJECT CODE      ADDR1    ADDR2     STMT

00001720  01020304 05060708                      863        DC      XL16'0102030405060708 090A0B0C0D0E0F00'    v2
00001728  090A0B0C 0D0E0F00
00001730  01020304 05060708                      864        DC      XL16'0102030405060708 FFFFFFFFFFFFFFFF'    v3
00001738  FFFFFFFF FFFFFFFF
                                                 865
                                                 866        VRR_C VA,3
00001740                                         867+       DS      0FD
00001740                       00001740          868+       USING *,R5               base for test data and test routine
00001740  00001780                               869+T12    DC      A(X12)                   address of test routine
00001744  000C                                   870+       DC      H'12'                    test number
00001746  00                                     871+       DC      X'00'
00001747  03                                     872+       DC      HL1'3'                   m4
00001748  E5C14040 40404040                      873+       DC      CL8'VA'                  instruction name
00001750  000017B8                               874+       DC      A(RE12+16)               address of v2 source
00001754  000017C8                               875+       DC      A(RE12+32)               address of v3 source
00001758  00000010                               876+       DC      A(16)                    result length
0000175C  000017A8                               877+REA12  DC      A(RE12)                  result address
00001760  00000000 00000000                      878+       DS      FD                       gap
00001768  00000000 00000000                      879+V1012  DS      XL16                     V1 output
00001770  00000000 00000000
00001778  00000000 00000000                      880+       DS      FD                       gap
                                                 881+*
00001780                                         882+X12    DS      0F
00001780  E310 5010 0014              00000010   883+       LGF     R1,V2ADDR                load v2 source
00001786  E761 0000 0806              00000000   884+       VL      v22,0(R1)                use v22 to test decoder
0000178C  E310 5014 0014              00000014   885+       LGF     R1,V3ADDR                load v3 source
00001792  E771 0000 0806              00000000   886+       VL      v23,0(R1)                use v23 to test decoder
00001798  E766 7000 3EF3                         887+       VA      V22,V22,V23,3             test instruction (dest is a source)
0000179E  E760 5028 080E              00001768   888+       VST     V22,V1012                 save v1 output
000017A4  07FB                                   889+       BR      R11                      return
000017A8                                         890+RE12   DC      0F                       xl16 expected result
000017A8                                         891+       DROP    R5
000017A8  FFFFFFFF FFFFFFFF                      892        DC      XL16'FFFFFFFFFFFFFFFF 08080808080807F7'    result
000017B0  08080808 080807F7
000017B8  FEFDFCFB FAF9F8F7                      893        DC      XL16'FEFDFCFBFAF9F8F7 090A0B0C0D0E0F00'    v2
000017C0  090A0B0C 0D0E0F00
000017C8  01020304 05060708                      894        DC      XL16'0102030405060708 FEFDFCFBFAF9F8F7'    v3
000017D0  FEFDFCFB FAF9F8F7
                                                 895
                                                 896 *Quadword
                                                 897        VRR_C VA,4
000017D8                                         898+       DS      0FD
000017D8                       000017D8          899+       USING *,R5               base for test data and test routine
000017D8  00001818                               900+T13    DC      A(X13)                   address of test routine
000017DC  000D                                   901+       DC      H'13'                    test number
000017DE  00                                     902+       DC      X'00'
000017DF  04                                     903+       DC      HL1'4'                   m4
000017E0  E5C14040 40404040                      904+       DC      CL8'VA'                  instruction name
000017E8  00001850                               905+       DC      A(RE13+16)               address of v2 source
000017EC  00001860                               906+       DC      A(RE13+32)               address of v3 source
000017F0  00000010                               907+       DC      A(16)                    result length
000017F4  00001840                               908+REA13  DC      A(RE13)                  result address
000017F8  00000000 00000000                      909+       DS      FD                       gap
00001800  00000000 00000000                      910+V1013  DS      XL16                     V1 output
00001808  00000000 00000000
00001810  00000000 00000000                      911+       DS      FD                       gap
```

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT


                                                  912+*
00001818                                          913+X13       DS      0F
00001818   E310 5010 0014              00000010   914+          LGF     R1,V2ADDR          load v2 source
0000181E   E761 0000 0806              00000000   915+          VL      v22,0(R1)          use v22 to test decoder
00001824   E310 5014 0014              00000014   916+          LGF     R1,V3ADDR          load v3 source
0000182A   E771 0000 0806              00000000   917+          VL      v23,0(R1)          use v23 to test decoder
00001830   E766 7000 4EF3                         918+          VA      V22,V22,V23,4       test instruction (dest is a source)
00001836   E760 5028 080E              00001800   919+          VST     V22,V1013           save v1 output
0000183C   07FB                                   920+          BR      R11                return
00001840                                          921+RE13      DC      0F                 xl16 expected result
00001840                                          922+          DROP    R5
00001840   45E86604 9B0AAA33                      923           DC      XL16'45E866049B0AAA33 5E50126078F4F2F6'     result
00001848   5E501260 78F4F2F6
00001850   23487325 6A194F7D                      924           DC      XL16'234873256A194F7D 2F2641230FE5EC7D'     v2
00001858   2F264123 0FE5EC7D
00001860   229FF2DF 30F15AB6                      925           DC      XL16'229FF2DF30F15AB6 2F29D13D690F0679'     v3
00001868   2F29D13D 690F0679
                                                  926
                                                  927           VRR_C VA,4
00001870                                          928+          DS      0FD
00001870                            00001870      929+          USING   *,R5              base for test data and test routine
00001870   000018B0                               930+T14       DC      A(X14)            address of test routine
00001874   000E                                   931+          DC      H'14'             test number
00001876   00                                     932+          DC      X'00'
00001877   04                                     933+          DC      HL1'4'            m4
00001878   E5C14040 40404040                      934+          DC      CL8'VA'           instruction name
00001880   000018E8                               935+          DC      A(RE14+16)        address of v2 source
00001884   000018F8                               936+          DC      A(RE14+32)        address of v3 source
00001888   00000010                               937+          DC      A(16)             result length
0000188C   000018D8                               938+REA14     DC      A(RE14)           result address
00001890   00000000 00000000                      939+          DS      FD                gap
00001898   00000000 00000000                      940+V1014     DS      XL16              V1 output
000018A0   00000000 00000000
000018A8   00000000 00000000                      941+          DS      FD                gap
                                                  942+*
000018B0                                          943+X14       DS      0F
000018B0   E310 5010 0014              00000010   944+          LGF     R1,V2ADDR          load v2 source
000018B6   E761 0000 0806              00000000   945+          VL      v22,0(R1)          use v22 to test decoder
000018BC   E310 5014 0014              00000014   946+          LGF     R1,V3ADDR          load v3 source
000018C2   E771 0000 0806              00000000   947+          VL      v23,0(R1)          use v23 to test decoder
000018C8   E766 7000 4EF3                         948+          VA      V22,V22,V23,4       test instruction (dest is a source)
000018CE   E760 5028 080E              00001898   949+          VST     V22,V1014           save v1 output
000018D4   07FB                                   950+          BR      R11                return
000018D8                                          951+RE14      DC      0F                 xl16 expected result
000018D8                                          952+          DROP    R5
000018D8   6E609494 AA50147A                      953           DC      XL16'6E609494AA50147A EB9A297D6B603CC4'     result
000018E0   EB9A297D 6B603CC4
000018E8   27C4BF69 7F002B32                      954           DC      XL16'27C4BF697F002B32 78A31FDE2A6E7226'     v2
000018F0   78A31FDE 2A6E7226
000018F8   469BD52B 2B4FE948                      955           DC      XL16'469BD52B2B4FE948 72F7099F40F1CA9E'     v3
00001900   72F7099F 40F1CA9E
                                                  956
                                                  957           VRR_C VA,4
00001908                                          958+          DS      0FD
00001908                            00001908      959+          USING   *,R5              base for test data and test routine
00001908   00001948                               960+T15       DC      A(X15)            address of test routine
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   LOC        OBJECT CODE      ADDR1     ADDR2     STMT

0000190C  000F                                    961+          DC      H'15'               test number
0000190E  00                                      962+          DC      X'00'
0000190F  04                                      963+          DC      HL1'4'              m4
00001910  E5C14040 40404040                       964+          DC      CL8'VA'             instruction name
00001918  00001980                                965+          DC      A(RE15+16)          address of v2 source
0000191C  00001990                                966+          DC      A(RE15+32)          address of v3 source
00001920  00000010                                967+          DC      A(16)               result length
00001924  00001970                                968+REA15     DC      A(RE15)             result address
00001928  00000000 00000000                       969+          DS      FD                  gap
00001930  00000000 00000000                       970+V1015     DS      XL16                V1 output
00001938  00000000 00000000
00001940  00000000 00000000                       971+          DS      FD                  gap
                                                   972+*
00001948                                          973+X15       DS      0F
00001948  E310 5010 0014            00000010       974+          LGF     R1,V2ADDR           load v2 source
0000194E  E761 0000 0806            00000000       975+          VL      v22,0(R1)           use v22 to test decoder
00001954  E310 5014 0014            00000014       976+          LGF     R1,V3ADDR           load v3 source
0000195A  E771 0000 0806            00000000       977+          VL      v23,0(R1)           use v23 to test decoder
00001960  E766 7000 4EF3                           978+          VA      V22,V22,V23,4         test instruction (dest is a source)
00001966  E760 5028 080E            00001930       979+          VST     V22,V1015             save v1 output
0000196C  07FB                                     980+          BR      R11                 return
00001970                                           981+RE15      DC      0F                  xl16 expected result
00001970                                           982+          DROP    R5
00001970  A12EA3D0 33F9D386                        983           DC      XL16'A12EA3D033F9D386 7E18759E5885D28A'     result
00001978  7E18759E 5885D28A
00001980  6F160AB2 05F59815                        984           DC      XL16'6F160AB205F59815 4D5234A5064045A4'     v2
00001988  4D5234A5 064045A4
00001990  3218991E 2E043B71                        985           DC      XL16'3218991E2E043B71 30C640F952458CE6'     v3
00001998  30C640F9 52458CE6
                                                   986
                                                   987 *-------------------------------------------------------------------
                                                   988 *    VS      - Vector Subtract
                                                   989 *-------------------------------------------------------------------
                                                   990 *Byte
                                                   991           VRR_C VS,0
000019A0                                           992+          DS      0FD
000019A0                  000019A0                 993+          USING *,R5                 base for test data and test routine
000019A0  000019E0                                 994+T16       DC      A(X16)              address of test routine
000019A4  0010                                     995+          DC      H'16'               test number
000019A6  00                                       996+          DC      X'00'
000019A7  00                                       997+          DC      HL1'0'              m4
000019A8  E5E24040 40404040                        998+          DC      CL8'VS'             instruction name
000019B0  00001A18                                 999+          DC      A(RE16+16)          address of v2 source
000019B4  00001A28                                 1000+         DC      A(RE16+32)          address of v3 source
000019B8  00000010                                 1001+         DC      A(16)               result length
000019BC  00001A08                                 1002+REA16    DC      A(RE16)             result address
000019C0  00000000 00000000                        1003+         DS      FD                  gap
000019C8  00000000 00000000                        1004+V1016    DS      XL16                V1 output
000019D0  00000000 00000000
000019D8  00000000 00000000                        1005+         DS      FD                  gap
                                                   1006+*
000019E0                                           1007+X16      DS      0F
000019E0  E310 5010 0014            00000010       1008+         LGF     R1,V2ADDR           load v2 source
000019E6  E761 0000 0806            00000000       1009+         VL      v22,0(R1)           use v22 to test decoder
000019EC  E310 5014 0014            00000014       1010+         LGF     R1,V3ADDR           load v3 source
000019F2  E771 0000 0806            00000000       1011+         VL      v23,0(R1)           use v23 to test decoder
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000019F8	E766 7000 0EF7			1012+	VS	V22,V22,V23,0	test instruction (dest is a source)
000019FE	E760 5028 080E		000019C8	1013+	VST	V22,V1016	save v1 output
00001A04	07FB			1014+	BR	R11	return
00001A08				1015+RE16	DC	0F	xl16 expected result
00001A08				1016+	DROP	R5	
00001A08	FEFDFCFB FAF9F8F7			1017	DC	XL16'FEFDFCFBFAF9F8F7 F8F8F8F8F8F8F808'	result
00001A10	F8F8F8F8 F8F8F808						
00001A18	FFFFFFFF FFFFFFFF			1018	DC	XL16'FFFFFFFFFFFFFFFF 0102030405060708'	v2
00001A20	01020304 05060708						
00001A28	01020304 05060708			1019	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v3
00001A30	090A0B0C 0D0E0F00						
				1020			
				1021	VRR_C	VS,0	
00001A38				1022+	DS	0FD	
00001A38		00001A38		1023+	USING	*,R5	base for test data and test routine
00001A38	00001A78			1024+T17	DC	A(X17)	address of test routine
00001A3C	0011			1025+	DC	H'17'	test number
00001A3E	00			1026+	DC	X'00'	
00001A3F	00			1027+	DC	HL1'0'	m4
00001A40	E5E24040 40404040			1028+	DC	CL8'VS'	instruction name
00001A48	00001AB0			1029+	DC	A(RE17+16)	address of v2 source
00001A4C	00001AC0			1030+	DC	A(RE17+32)	address of v3 source
00001A50	00000010			1031+	DC	A(16)	result length
00001A54	00001AA0			1032+REA17	DC	A(RE17)	result address
00001A58	00000000 00000000			1033+	DS	FD	gap
00001A60	00000000 00000000			1034+V1017	DS	XL16	V1 output
00001A68	00000000 00000000						
00001A70	00000000 00000000			1035+	DS	FD	gap
				1036+*			
00001A78				1037+X17	DS	0F	
00001A78	E310 5010 0014		00000010	1038+	LGF	R1,V2ADDR	load v2 source
00001A7E	E761 0000 0806		00000000	1039+	VL	v22,0(R1)	use v22 to test decoder
00001A84	E310 5014 0014		00000014	1040+	LGF	R1,V3ADDR	load v3 source
00001A8A	E771 0000 0806		00000000	1041+	VL	v23,0(R1)	use v23 to test decoder
00001A90	E766 7000 0EF7			1042+	VS	V22,V22,V23,0	test instruction (dest is a source)
00001A96	E760 5028 080E		00001A60	1043+	VST	V22,V1017	save v1 output
00001A9C	07FB			1044+	BR	R11	return
00001AA0				1045+RE17	DC	0F	xl16 expected result
00001AA0				1046+	DROP	R5	
00001AA0	00000000 00000000			1047	DC	XL16'0000000000000000 0A0B0C0D0E0F1001'	result
00001AA8	0A0B0C0D 0E0F1001						
00001AB0	01020304 05060708			1048	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v2
00001AB8	090A0B0C 0D0E0F00						
00001AC0	01020304 05060708			1049	DC	XL16'0102030405060708 FFFFFFFFFFFFFFFF'	v3
00001AC8	FFFFFFFF FFFFFFFF						
				1050			
				1051	VRR_C	VS,0	
00001AD0				1052+	DS	0FD	
00001AD0		00001AD0		1053+	USING	*,R5	base for test data and test routine
00001AD0	00001B10			1054+T18	DC	A(X18)	address of test routine
00001AD4	0012			1055+	DC	H'18'	test number
00001AD6	00			1056+	DC	X'00'	
00001AD7	00			1057+	DC	HL1'0'	m4
00001AD8	E5E24040 40404040			1058+	DC	CL8'VS'	instruction name
00001AE0	00001B48			1059+	DC	A(RE18+16)	address of v2 source
00001AE4	00001B58			1060+	DC	A(RE18+32)	address of v3 source

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  LOC         OBJECT CODE        ADDR1     ADDR2     STMT

00001AE8  00000010                                  1061+         DC    A(16)              result length
00001AEC  00001B38                                  1062+REA18    DC    A(RE18)            result address
00001AF0  00000000 00000000                         1063+         DS    FD                 gap
00001AF8  00000000 00000000                         1064+V1018    DS    XL16               V1 output
00001B00  00000000 00000000
00001B08  00000000 00000000                         1065+         DS    FD                 gap
                                                    1066+*
00001B10                                            1067+X18      DS    0F
00001B10  E310 5010 0014              00000010      1068+         LGF   R1,V2ADDR          load v2 source
00001B16  E761 0000 0806              00000000      1069+         VL    v22,0(R1)          use v22 to test decoder
00001B1C  E310 5014 0014              00000014      1070+         LGF   R1,V3ADDR          load v3 source
00001B22  E771 0000 0806              00000000      1071+         VL    v23,0(R1)          use v23 to test decoder
00001B28  E766 7000 0EF7                            1072+         VS    V22,V22,V23,0       test instruction (dest is a source)
00001B2E  E760 5028 080E              00001AF8      1073+         VST   V22,V1018           save v1 output
00001B34  07FB                                      1074+         BR    R11                return
00001B38                                            1075+RE18     DC    0F                 xl16 expected result
00001B38                                            1076+         DROP  R5
00001B38  FDFBF9F7 F5F3F1EF                         1077          DC    XL16'FDFBF9F7F5F3F1EF 0B0D0F1113151709'   result
00001B40  0B0D0F11 13151709
00001B48  FEFDFCFB FAF9F8F7                         1078          DC    XL16'FEFDFCFBFAF9F8F7 090A0B0C0D0E0F00'   v2
00001B50  090A0B0C 0D0E0F00
00001B58  01020304 05060708                         1079          DC    XL16'0102030405060708 FEFDFCFBFAF9F8F7'   v3
00001B60  FEFDFCFB FAF9F8F7
                                                    1080
                                                    1081 *Halfword
                                                    1082          VRR_C VS,1
00001B68                                            1083+         DS    0FD
00001B68                        00001B68            1084+         USING *,R5               base for test data and test routine
00001B68  00001BA8                                  1085+T19      DC    A(X19)             address of test routine
00001B6C  0013                                      1086+         DC    H'19'              test number
00001B6E  00                                        1087+         DC    X'00'
00001B6F  01                                        1088+         DC    HL1'1'             m4
00001B70  E5E24040 40404040                         1089+         DC    CL8'VS'            instruction name
00001B78  00001BE0                                  1090+         DC    A(RE19+16)         address of v2 source
00001B7C  00001BF0                                  1091+         DC    A(RE19+32)         address of v3 source
00001B80  00000010                                  1092+         DC    A(16)              result length
00001B84  00001BD0                                  1093+REA19    DC    A(RE19)            result address
00001B88  00000000 00000000                         1094+         DS    FD                 gap
00001B90  00000000 00000000                         1095+V1019    DS    XL16               V1 output
00001B98  00000000 00000000
00001BA0  00000000 00000000                         1096+         DS    FD                 gap
                                                    1097+*
00001BA8                                            1098+X19      DS    0F
00001BA8  E310 5010 0014              00000010      1099+         LGF   R1,V2ADDR          load v2 source
00001BAE  E761 0000 0806              00000000      1100+         VL    v22,0(R1)          use v22 to test decoder
00001BB4  E310 5014 0014              00000014      1101+         LGF   R1,V3ADDR          load v3 source
00001BBA  E771 0000 0806              00000000      1102+         VL    v23,0(R1)          use v23 to test decoder
00001BC0  E766 7000 1EF7                            1103+         VS    V22,V22,V23,1       test instruction (dest is a source)
00001BC6  E760 5028 080E              00001B90      1104+         VST   V22,V1019           save v1 output
00001BCC  07FB                                      1105+         BR    R11                return
00001BD0                                            1106+RE19     DC    0F                 xl16 expected result
00001BD0                                            1107+         DROP  R5
00001BD0  FEFDFCFB FAF9F8F7                         1108          DC    XL16'FEFDFCFBFAF9F8F7 F7F8F7F8F7F8F808'   result
00001BD8  F7F8F7F8 F7F8F808
00001BE0  FFFFFFFF FFFFFFFF                         1109          DC    XL16'FFFFFFFFFFFFFFFF 0102030405060708'   v2
00001BE8  01020304 05060708
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001BF0	01020304 05060708			1110	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v3
00001BF8	090A0B0C 0D0E0F00						
				1111			
				1112	VRR_C	VS,1	
00001C00				1113+	DS	0FD	
00001C00		00001C00		1114+	USING	*,R5	base for test data and test routine
00001C00	00001C40			1115+T20	DC	A(X20)	address of test routine
00001C04	0014			1116+	DC	H'20'	test number
00001C06	00			1117+	DC	X'00'	
00001C07	01			1118+	DC	HL1'1'	m4
00001C08	E5E24040 40404040			1119+	DC	CL8'VS'	instruction name
00001C10	00001C78			1120+	DC	A(RE20+16)	address of v2 source
00001C14	00001C88			1121+	DC	A(RE20+32)	address of v3 source
00001C18	00000010			1122+	DC	A(16)	result length
00001C1C	00001C68			1123+REA20	DC	A(RE20)	result address
00001C20	00000000 00000000			1124+	DS	FD	gap
00001C28	00000000 00000000			1125+V1020	DS	XL16	V1 output
00001C30	00000000 00000000						
00001C38	00000000 00000000			1126+	DS	FD	gap
				1127+*			
00001C40				1128+X20	DS	0F	
00001C40	E310 5010 0014		00000010	1129+	LGF	R1,V2ADDR	load v2 source
00001C46	E761 0000 0806		00000000	1130+	VL	v22,0(R1)	use v22 to test decoder
00001C4C	E310 5014 0014		00000014	1131+	LGF	R1,V3ADDR	load v3 source
00001C52	E771 0000 0806		00000000	1132+	VL	v23,0(R1)	use v23 to test decoder
00001C58	E766 7000 1EF7			1133+	VS	V22,V22,V23,1	test instruction (dest is a source)
00001C5E	E760 5028 080E		00001C28	1134+	VST	V22,V1020	save v1 output
00001C64	07FB			1135+	BR	R11	return
00001C68				1136+RE20	DC	0F	xl16 expected result
00001C68				1137+	DROP	R5	
00001C68	00000000 00000000			1138	DC	XL16'0000000000000000 090B0B0D0D0F0F01'	result
00001C70	090B0B0D 0D0F0F01						
00001C78	01020304 05060708			1139	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v2
00001C80	090A0B0C 0D0E0F00						
00001C88	01020304 05060708			1140	DC	XL16'0102030405060708 FFFFFFFFFFFFFFFF'	v3
00001C90	FFFFFFFF FFFFFFFF						
				1141			
				1142	VRR_C	VS,1	
00001C98				1143+	DS	0FD	
00001C98		00001C98		1144+	USING	*,R5	base for test data and test routine
00001C98	00001CD8			1145+T21	DC	A(X21)	address of test routine
00001C9C	0015			1146+	DC	H'21'	test number
00001C9E	00			1147+	DC	X'00'	
00001C9F	01			1148+	DC	HL1'1'	m4
00001CA0	E5E24040 40404040			1149+	DC	CL8'VS'	instruction name
00001CA8	00001D10			1150+	DC	A(RE21+16)	address of v2 source
00001CAC	00001D20			1151+	DC	A(RE21+32)	address of v3 source
00001CB0	00000010			1152+	DC	A(16)	result length
00001CB4	00001D00			1153+REA21	DC	A(RE21)	result address
00001CB8	00000000 00000000			1154+	DS	FD	gap
00001CC0	00000000 00000000			1155+V1021	DS	XL16	V1 output
00001CC8	00000000 00000000						
00001CD0	00000000 00000000			1156+	DS	FD	gap
				1157+*			
00001CD8				1158+X21	DS	0F	
00001CD8	E310 5010 0014		00000010	1159+	LGF	R1,V2ADDR	load v2 source

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00001CDE  E761 0000 0806                00000000  1160+          VL      v22,0(R1)            use v22 to test decoder
00001CE4  E310 5014 0014                00000014  1161+          LGF     R1,V3ADDR            load v3 source
00001CEA  E771 0000 0806                00000000  1162+          VL      v23,0(R1)            use v23 to test decoder
00001CF0  E766 7000 1EF7                          1163+          VS      V22,V22,V23,1         test instruction (dest is a source)
00001CF6  E760 5028 080E                00001CC0  1164+          VST     V22,V1021            save v1 output
00001CFC  07FB                                    1165+          BR      R11                  return
00001D00                                          1166+RE21      DC      0F                   xl16 expected result
00001D00                                          1167+          DROP    R5
00001D00  FDFBF9F7 F5F3F1EF                        1168           DC      XL16'FDFBF9F7F5F3F1EF 0A0D0E1112151609'    result
00001D08  0A0D0E11 12151609
00001D10  FEFDFCFB FAF9F8F7                        1169           DC      XL16'FEFDFCFBFAF9F8F7 090A0B0C0D0E0F00'    v2
00001D18  090A0B0C 0D0E0F00
00001D20  01020304 05060708                        1170           DC      XL16'0102030405060708 FEFDFCFBFAF9F8F7'    v3
00001D28  FEFDFCFB FAF9F8F7
                                                  1171
                                                  1172 *Word
                                                  1173           VRR_C VS,2
00001D30                                          1174+          DS      0FD
00001D30                        00001D30          1175+          USING   *,R5                 base for test data and test routine
00001D30  00001D70                                1176+T22       DC      A(X22)               address of test routine
00001D34  0016                                    1177+          DC      H'22'                test number
00001D36  00                                      1178+          DC      X'00'
00001D37  02                                      1179+          DC      HL1'2'               m4
00001D38  E5E24040 40404040                        1180+          DC      CL8'VS'              instruction name
00001D40  00001DA8                                1181+          DC      A(RE22+16)           address of v2 source
00001D44  00001DB8                                1182+          DC      A(RE22+32)           address of v3 source
00001D48  00000010                                1183+          DC      A(16)                result length
00001D4C  00001D98                                1184+REA22     DC      A(RE22)              result address
00001D50  00000000 00000000                        1185+          DS      FD                   gap
00001D58  00000000 00000000                        1186+V1022     DS      XL16                 V1 output
00001D60  00000000 00000000
00001D68  00000000 00000000                        1187+          DS      FD                   gap
                                                  1188+*
00001D70                                          1189+X22       DS      0F
00001D70  E310 5010 0014                00000010  1190+          LGF     R1,V2ADDR            load v2 source
00001D76  E761 0000 0806                00000000  1191+          VL      v22,0(R1)            use v22 to test decoder
00001D7C  E310 5014 0014                00000014  1192+          LGF     R1,V3ADDR            load v3 source
00001D82  E771 0000 0806                00000000  1193+          VL      v23,0(R1)            use v23 to test decoder
00001D88  E766 7000 2EF7                          1194+          VS      V22,V22,V23,2         test instruction (dest is a source)
00001D8E  E760 5028 080E                00001D58  1195+          VST     V22,V1022            save v1 output
00001D94  07FB                                    1196+          BR      R11                  return
00001D98                                          1197+RE22      DC      0F                   xl16 expected result
00001D98                                          1198+          DROP    R5
00001D98  FEFDFCFB FAF9F8F7                        1199           DC      XL16'FEFDFCFBFAF9F8F7 F7F7F7F8F7F7F808'    result
00001DA0  F7F7F7F8 F7F7F808
00001DA8  FFFFFFFF FFFFFFFF                        1200           DC      XL16'FFFFFFFFFFFFFFFF 0102030405060708'    v2
00001DB0  01020304 05060708
00001DB8  01020304 05060708                        1201           DC      XL16'0102030405060708 090A0B0C0D0E0F00'    v3
00001DC0  090A0B0C 0D0E0F00
                                                  1202
                                                  1203           VRR_C VS,2
00001DC8                                          1204+          DS      0FD
00001DC8                        00001DC8          1205+          USING   *,R5                 base for test data and test routine
00001DC8  00001E08                                1206+T23       DC      A(X23)               address of test routine
00001DCC  0017                                    1207+          DC      H'23'                test number
00001DCE  00                                      1208+          DC      X'00'
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001DCF	02			1209+	DC	HL1'2'	m4
00001DD0	E5E24040 40404040			1210+	DC	CL8'VS'	instruction name
00001DD8	00001E40			1211+	DC	A(RE23+16)	address of v2 source
00001DDC	00001E50			1212+	DC	A(RE23+32)	address of v3 source
00001DE0	00000010			1213+	DC	A(16)	result length
00001DE4	00001E30			1214+REA23	DC	A(RE23)	result address
00001DE8	00000000 00000000			1215+	DS	FD	gap
00001DF0	00000000 00000000			1216+V1023	DS	XL16	V1 output
00001DF8	00000000 00000000						
00001E00	00000000 00000000			1217+	DS	FD	gap
				1218+*			
00001E08				1219+X23	DS	0F	
00001E08	E310 5010 0014		00000010	1220+	LGF	R1,V2ADDR	load v2 source
00001E0E	E761 0000 0806		00000000	1221+	VL	v22,0(R1)	use v22 to test decoder
00001E14	E310 5014 0014		00000014	1222+	LGF	R1,V3ADDR	load v3 source
00001E1A	E771 0000 0806		00000000	1223+	VL	v23,0(R1)	use v23 to test decoder
00001E20	E766 7000 2EF7			1224+	VS	V22,V22,V23,2	test instruction (dest is a source)
00001E26	E760 5028 080E		00001DF0	1225+	VST	V22,V1023	save v1 output
00001E2C	07FB			1226+	BR	R11	return
00001E30				1227+RE23	DC	0F	xl16 expected result
00001E30				1228+	DROP	R5	
00001E30	00000000 00000000			1229	DC	XL16'0000000000000000 090A0B0D0D0E0F01'	result
00001E38	090A0B0D 0D0E0F01						
00001E40	01020304 05060708			1230	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v2
00001E48	090A0B0C 0D0E0F00						
00001E50	01020304 05060708			1231	DC	XL16'0102030405060708 FFFFFFFFFFFFFFFF'	v3
00001E58	FFFFFFFF FFFFFFFF						
				1232			
				1233	VRR_C	VS,2	
00001E60				1234+	DS	0FD	
00001E60		00001E60		1235+	USING	*,R5	base for test data and test routine
00001E60	00001EA0			1236+T24	DC	A(X24)	address of test routine
00001E64	0018			1237+	DC	H'24'	test number
00001E66	00			1238+	DC	X'00'	
00001E67	02			1239+	DC	HL1'2'	m4
00001E68	E5E24040 40404040			1240+	DC	CL8'VS'	instruction name
00001E70	00001ED8			1241+	DC	A(RE24+16)	address of v2 source
00001E74	00001EE8			1242+	DC	A(RE24+32)	address of v3 source
00001E78	00000010			1243+	DC	A(16)	result length
00001E7C	00001EC8			1244+REA24	DC	A(RE24)	result address
00001E80	00000000 00000000			1245+	DS	FD	gap
00001E88	00000000 00000000			1246+V1024	DS	XL16	V1 output
00001E90	00000000 00000000						
00001E98	00000000 00000000			1247+	DS	FD	gap
				1248+*			
00001EA0				1249+X24	DS	0F	
00001EA0	E310 5010 0014		00000010	1250+	LGF	R1,V2ADDR	load v2 source
00001EA6	E761 0000 0806		00000000	1251+	VL	v22,0(R1)	use v22 to test decoder
00001EAC	E310 5014 0014		00000014	1252+	LGF	R1,V3ADDR	load v3 source
00001EB2	E771 0000 0806		00000000	1253+	VL	v23,0(R1)	use v23 to test decoder
00001EB8	E766 7000 2EF7			1254+	VS	V22,V22,V23,2	test instruction (dest is a source)
00001EBE	E760 5028 080E		00001E88	1255+	VST	V22,V1024	save v1 output
00001EC4	07FB			1256+	BR	R11	return
00001EC8				1257+RE24	DC	0F	xl16 expected result
00001EC8				1258+	DROP	R5	
00001EC8	FDFBF9F7 F5F3F1EF			1259	DC	XL16'FDFBF9F7F5F3F1EF 0A0C0E1112141609'	result

```
  LOC          OBJECT CODE      ADDR1     ADDR2      STMT

00001ED0  0A0C0E11 12141609
00001ED8  FEFDFCFB FAF9F8F7                          1260         DC     XL16'FEFDFCFBFAF9F8F7 090A0B0C0D0E0F00'    v2
00001EE0  090A0B0C 0D0E0F00
00001EE8  01020304 05060708                          1261         DC     XL16'0102030405060708 FEFDFCFBFAF9F8F7'    v3
00001EF0  FEFDFCFB FAF9F8F7
                                                     1262
                                                     1263 *Doubleword
                                                     1264         VRR_C VS,3
00001EF8                                             1265+        DS     0FD
00001EF8                       00001EF8              1266+        USING  *,R5                  base for test data and test routine
00001EF8  00001F38                                   1267+T25     DC     A(X25)                address of test routine
00001EFC  0019                                       1268+        DC     H'25'                 test number
00001EFE  00                                         1269+        DC     X'00'
00001EFF  03                                         1270+        DC     HL1'3'                m4
00001F00  E5E24040 40404040                          1271+        DC     CL8'VS'               instruction name
00001F08  00001F70                                   1272+        DC     A(RE25+16)            address of v2 source
00001F0C  00001F80                                   1273+        DC     A(RE25+32)            address of v3 source
00001F10  00000010                                   1274+        DC     A(16)                 result length
00001F14  00001F60                                   1275+REA25   DC     A(RE25)               result address
00001F18  00000000 00000000                          1276+        DS     FD                    gap
00001F20  00000000 00000000                          1277+V1025   DS     XL16                  V1 output
00001F28  00000000 00000000
00001F30  00000000 00000000                          1278+        DS     FD                    gap
                                                     1279+*
00001F38                                             1280+X25     DS     0F
00001F38  E310 5010 0014             00000010        1281+        LGF    R1,V2ADDR             load v2 source
00001F3E  E761 0000 0806             00000000        1282+        VL     v22,0(R1)             use v22 to test decoder
00001F44  E310 5014 0014             00000014        1283+        LGF    R1,V3ADDR             load v3 source
00001F4A  E771 0000 0806             00000000        1284+        VL     v23,0(R1)             use v23 to test decoder
00001F50  E766 7000 3EF7                             1285+        VS     V22,V22,V23,3          test instruction (dest is a source)
00001F56  E760 5028 080E             00001F20        1286+        VST    V22,V1025              save v1 output
00001F5C  07FB                                       1287+        BR     R11                   return
00001F60                                             1288+RE25    DC     0F                    xl16 expected result
00001F60                                             1289+        DROP   R5
00001F60  FEFDFCFB FAF9F8F7                          1290         DC     XL16'FEFDFCFBFAF9F8F7 F7F7F7F7F7F7F808'     result
00001F68  F7F7F7F7 F7F7F808
00001F70  FFFFFFFF FFFFFFFF                          1291         DC     XL16'FFFFFFFFFFFFFFFF 0102030405060708'    v2
00001F78  01020304 05060708
00001F80  01020304 05060708                          1292         DC     XL16'0102030405060708 090A0B0C0D0E0F00'    v3
00001F88  090A0B0C 0D0E0F00
                                                     1293
                                                     1294         VRR_C VS,3
00001F90                                             1295+        DS     0FD
00001F90                       00001F90              1296+        USING  *,R5                  base for test data and test routine
00001F90  00001FD0                                   1297+T26     DC     A(X26)                address of test routine
00001F94  001A                                       1298+        DC     H'26'                 test number
00001F96  00                                         1299+        DC     X'00'
00001F97  03                                         1300+        DC     HL1'3'                m4
00001F98  E5E24040 40404040                          1301+        DC     CL8'VS'               instruction name
00001FA0  00002008                                   1302+        DC     A(RE26+16)            address of v2 source
00001FA4  00002018                                   1303+        DC     A(RE26+32)            address of v3 source
00001FA8  00000010                                   1304+        DC     A(16)                 result length
00001FAC  00001FF8                                   1305+REA26   DC     A(RE26)               result address
00001FB0  00000000 00000000                          1306+        DS     FD                    gap
00001FB8  00000000 00000000                          1307+V1026   DS     XL16                  V1 output
00001FC0  00000000 00000000
```

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  LOC         OBJECT CODE      ADDR1      ADDR2      STMT

00001FC8   00000000 00000000                        1308+        DS     FD              gap
                                                     1309+*
00001FD0                                             1310+X26     DS     0F
00001FD0   E310 5010 0014               00000010     1311+        LGF    R1,V2ADDR       load v2 source
00001FD6   E761 0000 0806               00000000     1312+        VL     v22,0(R1)       use v22 to test decoder
00001FDC   E310 5014 0014               00000014     1313+        LGF    R1,V3ADDR       load v3 source
00001FE2   E771 0000 0806               00000000     1314+        VL     v23,0(R1)       use v23 to test decoder
00001FE8   E766 7000 3EF7                            1315+        VS     V22,V22,V23,3    test instruction (dest is a source)
00001FEE   E760 5028 080E               00001FB8     1316+        VST    V22,V1026        save v1 output
00001FF4   07FB                                      1317+        BR     R11             return
00001FF8                                             1318+RE26    DC     0F              xl16 expected result
00001FF8                                             1319+        DROP   R5
00001FF8   00000000 00000000                         1320         DC     XL16'0000000000000000 090A0B0C0D0E0F01'    result
00002000   090A0B0C 0D0E0F01
00002008   01020304 05060708                         1321         DC     XL16'0102030405060708 090A0B0C0D0E0F00'    v2
00002010   090A0B0C 0D0E0F00
00002018   01020304 05060708                         1322         DC     XL16'0102030405060708 FFFFFFFFFFFFFFFF'    v3
00002020   FFFFFFFF FFFFFFFF
                                                     1323
                                                     1324                VRR_C  VS,3
00002028                                             1325+        DS     0FD
00002028                      00002028               1326+        USING  *,R5            base for test data and test routine
00002028   00002068                                  1327+T27     DC     A(X27)          address of test routine
0000202C   001B                                      1328+        DC     H'27'           test number
0000202E   00                                        1329+        DC     X'00'
0000202F   03                                        1330+        DC     HL1'3'          m4
00002030   E5E24040 40404040                         1331+        DC     CL8'VS'         instruction name
00002038   000020A0                                  1332+        DC     A(RE27+16)      address of v2 source
0000203C   000020B0                                  1333+        DC     A(RE27+32)      address of v3 source
00002040   00000010                                  1334+        DC     A(16)           result length
00002044   00002090                                  1335+REA27   DC     A(RE27)         result address
00002048   00000000 00000000                         1336+        DS     FD              gap
00002050   00000000 00000000                         1337+V1027   DS     XL16            V1 output
00002058   00000000 00000000
00002060   00000000 00000000                         1338+        DS     FD              gap
                                                     1339+*
00002068                                             1340+X27     DS     0F
00002068   E310 5010 0014               00000010     1341+        LGF    R1,V2ADDR       load v2 source
0000206E   E761 0000 0806               00000000     1342+        VL     v22,0(R1)       use v22 to test decoder
00002074   E310 5014 0014               00000014     1343+        LGF    R1,V3ADDR       load v3 source
0000207A   E771 0000 0806               00000000     1344+        VL     v23,0(R1)       use v23 to test decoder
00002080   E766 7000 3EF7                            1345+        VS     V22,V22,V23,3    test instruction (dest is a source)
00002086   E760 5028 080E               00002050     1346+        VST    V22,V1027        save v1 output
0000208C   07FB                                      1347+        BR     R11             return
00002090                                             1348+RE27    DC     0F              xl16 expected result
00002090                                             1349+        DROP   R5
00002090   FDFBF9F7 F5F3F1EF                         1350         DC     XL16'FDFBF9F7F5F3F1EF 0A0C0E1012141609'    result
00002098   0A0C0E10 12141609
000020A0   FEFDFCFB FAF9F8F7                         1351         DC     XL16'FEFDFCFBFAF9F8F7 090A0B0C0D0E0F00'    v2
000020A8   090A0B0C 0D0E0F00
000020B0   01020304 05060708                         1352         DC     XL16'0102030405060708 FEFDFCFBFAF9F8F7'    v3
000020B8   FEFDFCFB FAF9F8F7
                                                     1353
                                                     1354 *Quadword
                                                     1355                VRR_C  VS,4
000020C0                                             1356+        DS     0FD
```

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  LOC           OBJECT CODE      ADDR1     ADDR2     STMT

000020C0                        000020C0            1357+           USING *,R5              base for test data and test routine
000020C0  00002100                                 1358+T28        DC    A(X28)             address of test routine
000020C4  001C                                     1359+           DC    H'28'              test number
000020C6  00                                       1360+           DC    X'00'
000020C7  04                                       1361+           DC    HL1'4'             m4
000020C8  E5E24040 40404040                        1362+           DC    CL8'VS'            instruction name
000020D0  00002138                                 1363+           DC    A(RE28+16)         address of v2 source
000020D4  00002148                                 1364+           DC    A(RE28+32)         address of v3 source
000020D8  00000010                                 1365+           DC    A(16)              result length
000020DC  00002128                                 1366+REA28      DC    A(RE28)            result address
000020E0  00000000 00000000                        1367+           DS    FD                 gap
000020E8  00000000 00000000                        1368+V1028      DS    XL16               V1 output
000020F0  00000000 00000000
000020F8  00000000 00000000                        1369+           DS    FD                 gap
                                                   1370+*
00002100                                           1371+X28        DS    0F
00002100  E310 5010 0014                 00000010  1372+           LGF   R1,V2ADDR          load v2 source
00002106  E761 0000 0806                 00000000  1373+           VL    v22,0(R1)          use v22 to test decoder
0000210C  E310 5014 0014                 00000014  1374+           LGF   R1,V3ADDR          load v3 source
00002112  E771 0000 0806                 00000000  1375+           VL    v23,0(R1)          use v23 to test decoder
00002118  E766 7000 4EF7                           1376+           VS    V22,V22,V23,4       test instruction (dest is a source)
0000211E  E760 5028 080E                 000020E8  1377+           VST   V22,V1028           save v1 output
00002124  07FB                                     1378+           BR    R11                return
00002128                                           1379+RE28       DC    0F                 xl16 expected result
00002128                                           1380+           DROP  R5
00002128  C1E547F1 479F6DB9                        1381            DC    XL16'C1E547F1479F6DB9 EE80435D2CCEA68C'    result
00002130  EE80435D 2CCEA68C
00002138  3A6F0F67 7D7C5F4B                        1382            DC    XL16'3A6F0F677D7C5F4B 17669C374BC86A57'    v2
00002140  17669C37 4BC86A57
00002148  7889C776 35DCF191                        1383            DC    XL16'7889C77635DCF191 28E658DA1EF9C3CB'    v3
00002150  28E658DA 1EF9C3CB
                                                   1384
                                                   1385            VRR_C VS,4
00002158                                           1386+           DS    0FD
00002158                        00002158            1387+           USING *,R5              base for test data and test routine
00002158  00002198                                 1388+T29        DC    A(X29)             address of test routine
0000215C  001D                                     1389+           DC    H'29'              test number
0000215E  00                                       1390+           DC    X'00'
0000215F  04                                       1391+           DC    HL1'4'             m4
00002160  E5E24040 40404040                        1392+           DC    CL8'VS'            instruction name
00002168  000021D0                                 1393+           DC    A(RE29+16)         address of v2 source
0000216C  000021E0                                 1394+           DC    A(RE29+32)         address of v3 source
00002170  00000010                                 1395+           DC    A(16)              result length
00002174  000021C0                                 1396+REA29      DC    A(RE29)            result address
00002178  00000000 00000000                        1397+           DS    FD                 gap
00002180  00000000 00000000                        1398+V1029      DS    XL16               V1 output
00002188  00000000 00000000
00002190  00000000 00000000                        1399+           DS    FD                 gap
                                                   1400+*
00002198                                           1401+X29        DS    0F
00002198  E310 5010 0014                 00000010  1402+           LGF   R1,V2ADDR          load v2 source
0000219E  E761 0000 0806                 00000000  1403+           VL    v22,0(R1)          use v22 to test decoder
000021A4  E310 5014 0014                 00000014  1404+           LGF   R1,V3ADDR          load v3 source
000021AA  E771 0000 0806                 00000000  1405+           VL    v23,0(R1)          use v23 to test decoder
000021B0  E766 7000 4EF7                           1406+           VS    V22,V22,V23,4       test instruction (dest is a source)
000021B6  E760 5028 080E                 00002180  1407+           VST   V22,V1029           save v1 output
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2    STMT

000021BC  07FB                                   1408+          BR    R11             return
000021C0                                         1409+RE29      DC    0F              xl16 expected result
000021C0                                         1410+          DROP  R5
000021C0  E735DE52 C7237496                       1411          DC    XL16'E735DE52C7237496 F7154F42306B40FD'   result
000021C8  F7154F42 306B40FD
000021D0  2FBDC758 100E357D                       1412          DC    XL16'2FBDC758100E357D 24E0AC354223EE33'   v2
000021D8  24E0AC35 4223EE33
000021E0  4887E905 48EAC0E6                       1413          DC    XL16'4887E90548EAC0E6 2DCB5CF311B8AD36'   v3
000021E8  2DCB5CF3 11B8AD36
                                                  1414
                                                  1415          VRR_C VS,4
000021F0                                         1416+          DS    0FD
000021F0                     000021F0             1417+          USING *,R5            base for test data and test routine
000021F0  00002230                                1418+T30      DC    A(X30)           address of test routine
000021F4  001E                                    1419+         DC    H'30'            test number
000021F6  00                                      1420+         DC    X'00'
000021F7  04                                      1421+         DC    HL1'4'           m4
000021F8  E5E24040 40404040                       1422+         DC    CL8'VS'          instruction name
00002200  00002268                                1423+         DC    A(RE30+16)       address of v2 source
00002204  00002278                                1424+         DC    A(RE30+32)       address of v3 source
00002208  00000010                                1425+         DC    A(16)            result length
0000220C  00002258                                1426+REA30    DC    A(RE30)          result address
00002210  00000000 00000000                       1427+         DS    FD               gap
00002218  00000000 00000000                       1428+V1030    DS    XL16             V1 output
00002220  00000000 00000000
00002228  00000000 00000000                       1429+         DS    FD               gap
                                                  1430+*
00002230                                         1431+X30      DS    0F
00002230  E310 5010 0014              00000010    1432+         LGF   R1,V2ADDR        load v2 source
00002236  E761 0000 0806              00000000    1433+         VL    v22,0(R1)        use v22 to test decoder
0000223C  E310 5014 0014              00000014    1434+         LGF   R1,V3ADDR        load v3 source
00002242  E771 0000 0806              00000000    1435+         VL    v23,0(R1)        use v23 to test decoder
00002248  E766 7000 4EF7                          1436+         VS    V22,V22,V23,4     test instruction (dest is a source)
0000224E  E760 A018 080E              00002218    1437+         VST   V22,V1030         save v1 output
00002254  07FB                                    1438+         BR    R11              return
00002258                                         1439+RE30     DC    0F               xl16 expected result
00002258                                         1440+          DROP  R5
00002258  ED66719B 01D1154D                       1441          DC    XL16'ED66719B01D1154D 34E3E6EED8D5204F'   result
00002260  34E3E6EE D8D5204F
00002268  3FC888C9 65137198                       1442          DC    XL16'3FC888C965137198 5F4985333946CE5C'   v2
00002270  5F498533 3946CE5C
00002278  5262172E 63425C4B                       1443          DC    XL16'5262172E63425C4B 2A659E446071AE0D'   v3
00002280  2A659E44 6071AE0D
                                                  1444
                                                  1445 *-------------------------------------------------------------
                                                  1446 *   VSCBI  - Vector Subtract Compute Borrow Indication
                                                  1447 *-------------------------------------------------------------
                                                  1448 *Byte
                                                  1449          VRR_C VSCBI,0
00002288                                         1450+          DS    0FD
00002288                     00002288             1451+          USING *,R5            base for test data and test routine
00002288  000022C8                                1452+T31      DC    A(X31)           address of test routine
0000228C  001F                                    1453+         DC    H'31'            test number
0000228E  00                                      1454+         DC    X'00'
0000228F  00                                      1455+         DC    HL1'0'           m4
00002290  E5E2C3C2 C9404040                       1456+         DC    CL8'VSCBI'       instruction name
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002298	00002300			1457+	DC	A(RE31+16)	address of v2 source
0000229C	00002310			1458+	DC	A(RE31+32)	address of v3 source
000022A0	00000010			1459+	DC	A(16)	result length
000022A4	000022F0			1460+REA31	DC	A(RE31)	result address
000022A8	00000000 00000000			1461+	DS	FD	gap
000022B0	00000000 00000000			1462+V1031	DS	XL16	V1 output
000022B8	00000000 00000000						
000022C0	00000000 00000000			1463+	DS	FD	gap
				1464+*			
000022C8				1465+X31	DS	0F	
000022C8	E310 5010 0014		00000010	1466+	LGF	R1,V2ADDR	load v2 source
000022CE	E761 0000 0806		00000000	1467+	VL	v22,0(R1)	use v22 to test decoder
000022D4	E310 5014 0014		00000014	1468+	LGF	R1,V3ADDR	load v3 source
000022DA	E771 0000 0806		00000000	1469+	VL	v23,0(R1)	use v23 to test decoder
000022E0	E766 7000 0EF5			1470+	VSCBI	V22,V22,V23,0	test instruction (dest is a source)
000022E6	E760 5028 080E		000022B0	1471+	VST	V22,V1031	save v1 output
000022EC	07FB			1472+	BR	R11	return
000022F0				1473+RE31	DC	0F	xl16 expected result
000022F0				1474+	DROP	R5	
000022F0	01010101 01010101			1475	DC	XL16'0101010101010101 0000000000000001'	result
000022F8	00000000 00000001						
00002300	FFFFFFFF FFFFFFFF			1476	DC	XL16'FFFFFFFFFFFFFFFF 0102030405060708'	v2
00002308	01020304 05060708						
00002310	01020304 05060708			1477	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v3
00002318	090A0B0C 0D0E0F00						
				1478			
				1479	VRR_C	VSCBI,0	
00002320				1480+	DS	0FD	
00002320		00002320		1481+	USING	*,R5	base for test data and test routine
00002320	00002360			1482+T32	DC	A(X32)	address of test routine
00002324	0020			1483+	DC	H'32'	test number
00002326	00			1484+	DC	X'00'	
00002327	00			1485+	DC	HL1'0'	m4
00002328	E5E2C3C2 C9404040			1486+	DC	CL8'VSCBI'	instruction name
00002330	00002398			1487+	DC	A(RE32+16)	address of v2 source
00002334	000023A8			1488+	DC	A(RE32+32)	address of v3 source
00002338	00000010			1489+	DC	A(16)	result length
0000233C	00002388			1490+REA32	DC	A(RE32)	result address
00002340	00000000 00000000			1491+	DS	FD	gap
00002348	00000000 00000000			1492+V1032	DS	XL16	V1 output
00002350	00000000 00000000						
00002358	00000000 00000000			1493+	DS	FD	gap
				1494+*			
00002360				1495+X32	DS	0F	
00002360	E310 5010 0014		00000010	1496+	LGF	R1,V2ADDR	load v2 source
00002366	E761 0000 0806		00000000	1497+	VL	v22,0(R1)	use v22 to test decoder
0000236C	E310 5014 0014		00000014	1498+	LGF	R1,V3ADDR	load v3 source
00002372	E771 0000 0806		00000000	1499+	VL	v23,0(R1)	use v23 to test decoder
00002378	E766 7000 0EF5			1500+	VSCBI	V22,V22,V23,0	test instruction (dest is a source)
0000237E	E760 5028 080E		00002348	1501+	VST	V22,V1032	save v1 output
00002384	07FB			1502+	BR	R11	return
00002388				1503+RE32	DC	0F	xl16 expected result
00002388				1504+	DROP	R5	
00002388	01010101 01010101			1505	DC	XL16'0101010101010101 0000000000000000'	result
00002390	00000000 00000000						
00002398	01020304 05060708			1506	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v2

```
  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

 000023A0   090A0B0C 0D0E0F00
 000023A8   01020304 05060708   1507            DC     XL16'0102030405060708 FFFFFFFFFFFFFFFF'     v3
 000023B0   FFFFFFFF FFFFFFFF

                                1508
                                1509            VRR_C VSCBI,0
 000023B8                       1510+           DS     0FD
 000023B8            000023B8   1511+           USING *,R5                base for test data and test routine
 000023B8   000023F8           1512+T33         DC     A(X33)             address of test routine
 000023BC   0021                1513+           DC     H'33'              test number
 000023BE   00                  1514+           DC     X'00'
 000023BF   00                  1515+           DC     HL1'0'             m4
 000023C0   E5E2C3C2 C9404040   1516+           DC     CL8'VSCBI'         instruction name
 000023C8   00002430            1517+           DC     A(RE33+16)         address of v2 source
 000023CC   00002440            1518+           DC     A(RE33+32)         address of v3 source
 000023D0   00000010            1519+           DC     A(16)              result length
 000023D4   00002420            1520+REA33      DC     A(RE33)            result address
 000023D8   00000000 00000000   1521+           DS     FD                 gap
 000023E0   00000000 00000000   1522+V1033      DS     XL16               V1 output
 000023E8   00000000 00000000
 000023F0   00000000 00000000   1523+           DS     FD                 gap

                                1524+*
 000023F8                       1525+X33         DS     0F
 000023F8   E310 5010 0014            00000010   1526+           LGF    R1,V2ADDR          load v2 source
 000023FE   E761 0000 0806            00000000   1527+           VL     v22,0(R1)          use v22 to test decoder
 00002404   E310 5014 0014            00000014   1528+           LGF    R1,V3ADDR          load v3 source
 0000240A   E771 0000 0806            00000000   1529+           VL     v23,0(R1)          use v23 to test decoder
 00002410   E766 7000 0EF5                       1530+           VSCBI V22,V22,V23,0        test instruction (dest is a source)
 00002416   E760 5028 080E            000023E0   1531+           VST    V22,V1033          save v1 output
 0000241C   07FB                                 1532+           BR     R11                return
 00002420                                        1533+RE33       DC     0F                 xl16 expected result
 00002420                                        1534+           DROP   R5
 00002420   01010001 01010100   1535            DC     XL16'0101000101010100 0000010000000000'     result
 00002428   00000100 00000000
 00002430   FEFD01FB FAF9F807   1536            DC     XL16'FEFD01FBFAF9F807 090AFB0C0D0E0F00'      v2
 00002438   090AFB0C 0D0E0F00
 00002440   01020304 05060708   1537            DC     XL16'0102030405060708 FEFDF0FBFAF9F8F7'     v3
 00002448   FEFDF0FB FAF9F8F7

                                1538
                                1539 *Halfword
                                1540            VRR_C VSCBI,1
 00002450                       1541+           DS     0FD
 00002450            00002450   1542+           USING *,R5                base for test data and test routine
 00002450   00002490            1543+T34         DC     A(X34)             address of test routine
 00002454   0022                1544+           DC     H'34'              test number
 00002456   00                  1545+           DC     X'00'
 00002457   01                  1546+           DC     HL1'1'             m4
 00002458   E5E2C3C2 C9404040   1547+           DC     CL8'VSCBI'         instruction name
 00002460   000024C8            1548+           DC     A(RE34+16)         address of v2 source
 00002464   000024D8            1549+           DC     A(RE34+32)         address of v3 source
 00002468   00000010            1550+           DC     A(16)              result length
 0000246C   000024B8            1551+REA34      DC     A(RE34)            result address
 00002470   00000000 00000000   1552+           DS     FD                 gap
 00002478   00000000 00000000   1553+V1034      DS     XL16               V1 output
 00002480   00000000 00000000
 00002488   00000000 00000000   1554+           DS     FD                 gap
                                1555+*
```

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  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

 00002490                                          1556+X34      DS    0F
 00002490  E310 5010 0014                00000010  1557+         LGF   R1,V2ADDR         load v2 source
 00002496  E761 0000 0806                00000000  1558+         VL    v22,0(R1)         use v22 to test decoder
 0000249C  E310 5014 0014                00000014  1559+         LGF   R1,V3ADDR         load v3 source
 000024A2  E771 0000 0806                00000000  1560+         VL    v23,0(R1)         use v23 to test decoder
 000024A8  E766 7000 1EF5                          1561+         VSCBI V22,V22,V23,1      test instruction (dest is a source)
 000024AE  E760 5028 080E                00002478  1562+         VST   V22,V1034         save v1 output
 000024B4  07FB                                    1563+         BR    R11               return
 000024B8                                          1564+RE34     DC    0F                xl16 expected result
 000024B8                                          1565+         DROP  R5
 000024B8  00010001 00010001                       1566          DC    XL16'0001000100010001 0000000000000000'    result
 000024C0  00000000 00000000
 000024C8  FFFFFFFF FFFFFFFF                        1567          DC    XL16'FFFFFFFFFFFFFFFF 0102030405060708'    v2
 000024D0  01020304 05060708
 000024D8  01020304 05060708                        1568          DC    XL16'0102030405060708 090A0B0C0D0E0F00'    v3
 000024E0  090A0B0C 0D0E0F00
                                                    1569
                                                    1570          VRR_C VSCBI,1
 000024E8                                           1571+         DS    0FD
 000024E8                      000024E8             1572+         USING *,R5             base for test data and test routine
 000024E8  00002528                                 1573+T35      DC    A(X35)            address of test routine
 000024EC  0023                                     1574+         DC    H'35'             test number
 000024EE  00                                       1575+         DC    X'00'
 000024EF  01                                       1576+         DC    HL1'1'            m4
 000024F0  E5E2C3C2 C9404040                         1577+         DC    CL8'VSCBI'        instruction name
 000024F8  00002560                                  1578+         DC    A(RE35+16)        address of v2 source
 000024FC  00002570                                  1579+         DC    A(RE35+32)        address of v3 source
 00002500  00000010                                  1580+         DC    A(16)             result length
 00002504  00002550                                  1581+REA35    DC    A(RE35)           result address
 00002508  00000000 00000000                         1582+         DS    FD                gap
 00002510  00000000 00000000                         1583+V1035    DS    XL16              V1 output
 00002518  00000000 00000000
 00002520  00000000 00000000                         1584+         DS    FD                gap
                                                     1585+*
 00002528                                            1586+X35      DS    0F
 00002528  E310 5010 0014                00000010   1587+         LGF   R1,V2ADDR         load v2 source
 0000252E  E761 0000 0806                00000000   1588+         VL    v22,0(R1)         use v22 to test decoder
 00002534  E310 5014 0014                00000014   1589+         LGF   R1,V3ADDR         load v3 source
 0000253A  E771 0000 0806                00000000   1590+         VL    v23,0(R1)         use v23 to test decoder
 00002540  E766 7000 1EF5                           1591+         VSCBI V22,V22,V23,1      test instruction (dest is a source)
 00002546  E760 5028 080E                00002510   1592+         VST   V22,V1035         save v1 output
 0000254C  07FB                                     1593+         BR    R11               return
 00002550                                           1594+RE35     DC    0F                xl16 expected result
 00002550                                           1595+         DROP  R5
 00002550  00010001 00010001                        1596          DC    XL16'0001000100010001 0000000000000001'    result
 00002558  00000000 00000001
 00002560  01020304 05060708                        1597          DC    XL16'0102030405060708 090A0B0C0D0E0F00'    v2
 00002568  090A0B0C 0D0E0F00
 00002570  01020304 05060708                        1598          DC    XL16'0102030405060708 FFFFFFFFFFFF00FF'    v3
 00002578  FFFFFFFF FFFF00FF
                                                    1599
                                                    1600          VRR_C VSCBI,1
 00002580                                           1601+         DS    0FD
 00002580                      00002580             1602+         USING *,R5             base for test data and test routine
 00002580  000025C0                                 1603+T36      DC    A(X36)            address of test routine
 00002584  0024                                     1604+         DC    H'36'             test number
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  LOC        OBJECT CODE     ADDR1    ADDR2    STMT

00002586  00                                  1605+         DC      X'00'
00002587  01                                  1606+         DC      HL1'1'            m4
00002588  E5E2C3C2 C9404040                    1607+         DC      CL8'VSCBI'        instruction name
00002590  000025F8                            1608+         DC      A(RE36+16)        address of v2 source
00002594  00002608                            1609+         DC      A(RE36+32)        address of v3 source
00002598  00000010                            1610+         DC      A(16)             result length
0000259C  000025E8                            1611+REA36     DC      A(RE36)           result address
000025A0  00000000 00000000                   1612+         DS      FD                gap
000025A8  00000000 00000000                   1613+V1036     DS      XL16              V1 output
000025B0  00000000 00000000
000025B8  00000000 00000000                   1614+         DS      FD                gap
                                              1615+*
000025C0                                      1616+X36       DS      0F
000025C0  E310 5010 0014              00000010 1617+         LGF     R1,V2ADDR         load v2 source
000025C6  E761 0000 0806              00000000 1618+         VL      v22,0(R1)         use v22 to test decoder
000025CC  E310 5014 0014              00000014 1619+         LGF     R1,V3ADDR         load v3 source
000025D2  E771 0000 0806              00000000 1620+         VL      v23,0(R1)         use v23 to test decoder
000025D8  E766 7000 1EF5                       1621+         VSCBI   V22,V22,V23,1      test instruction (dest is a source)
000025DE  E760 5028 080E              000025A8 1622+         VST     V22,V1036          save v1 output
000025E4  07FB                                 1623+         BR      R11               return
000025E8                                      1624+RE36      DC      0F                xl16 expected result
000025E8                                      1625+         DROP    R5
000025E8  00010001 00000001                   1626          DC      XL16'0001000100000001 0001000000000000'    result
000025F0  00010000 00000000
000025F8  FEFDFC0B 0AF9F8F7                    1627          DC      XL16'FEFDFC0B0AF9F8F7 B90A0B0C0D0E0F00'     v2
00002600  B90A0B0C 0D0E0F00
00002608  010203B4 B5060708                    1628          DC      XL16'010203B4B5060708 0EFDFCFBFAF9F8F7'     v3
00002610  0EFDFCFB FAF9F8F7
                                              1629
                                              1630 *Word
                                              1631          VRR_C   VSCBI,2
00002618                                      1632+         DS      0FD
00002618                           00002618   1633+         USING   *,R5              base for test data and test routine
00002618  00002658                            1634+T37      DC      A(X37)            address of test routine
0000261C  0025                                1635+         DC      H'37'             test number
0000261E  00                                  1636+         DC      X'00'
0000261F  02                                  1637+         DC      HL1'2'            m4
00002620  E5E2C3C2 C9404040                    1638+         DC      CL8'VSCBI'        instruction name
00002628  00002690                            1639+         DC      A(RE37+16)        address of v2 source
0000262C  000026A0                            1640+         DC      A(RE37+32)        address of v3 source
00002630  00000010                            1641+         DC      A(16)             result length
00002634  00002680                            1642+REA37     DC      A(RE37)           result address
00002638  00000000 00000000                   1643+         DS      FD                gap
00002640  00000000 00000000                   1644+V1037     DS      XL16              V1 output
00002648  00000000 00000000
00002650  00000000 00000000                   1645+         DS      FD                gap
                                              1646+*
00002658                                      1647+X37       DS      0F
00002658  E310 5010 0014              00000010 1648+         LGF     R1,V2ADDR         load v2 source
0000265E  E761 0000 0806              00000000 1649+         VL      v22,0(R1)         use v22 to test decoder
00002664  E310 5014 0014              00000014 1650+         LGF     R1,V3ADDR         load v3 source
0000266A  E771 0000 0806              00000000 1651+         VL      v23,0(R1)         use v23 to test decoder
00002670  E766 7000 2EF5                       1652+         VSCBI   V22,V22,V23,2      test instruction (dest is a source)
00002676  E760 5028 080E              00002640 1653+         VST     V22,V1037          save v1 output
0000267C  07FB                                 1654+         BR      R11               return
00002680                                      1655+RE37      DC      0F                xl16 expected result
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  LOC          OBJECT CODE      ADDR1     ADDR2     STMT


 00002680                                           1656+          DROP   R5
 00002680   00000001 00000001                       1657           DC     XL16'0000000100000001 0000000000000000'     result
 00002688   00000000 00000000
 00002690   FFFFFFFF FFFFFFFF                        1658           DC     XL16'FFFFFFFFFFFFFFFF 0102030405060708'      v2
 00002698   01020304 05060708
 000026A0   01020304 05060708                        1659           DC     XL16'0102030405060708 090A0B0C0D0E0F00'     v3
 000026A8   090A0B0C 0D0E0F00
                                                     1660
                                                     1661           VRR_C  VSCBI,2
 000026B0                                            1662+          DS     0FD
 000026B0                         000026B0           1663+          USING  *,R5                    base for test data and test routine
 000026B0   000026F0                                 1664+T38       DC     A(X38)                  address of test routine
 000026B4   0026                                     1665+          DC     H'38'                   test number
 000026B6   00                                       1666+          DC     X'00'
 000026B7   02                                       1667+          DC     HL1'2'                  m4
 000026B8   E5E2C3C2 C9404040                         1668+          DC     CL8'VSCBI'              instruction name
 000026C0   00002728                                 1669+          DC     A(RE38+16)              address of v2 source
 000026C4   00002738                                 1670+          DC     A(RE38+32)              address of v3 source
 000026C8   00000010                                 1671+          DC     A(16)                   result length
 000026CC   00002718                                 1672+REA38     DC     A(RE38)                 result address
 000026D0   00000000 00000000                        1673+          DS     FD                      gap
 000026D8   00000000 00000000                        1674+V1038     DS     XL16                    V1 output
 000026E0   00000000 00000000
 000026E8   00000000 00000000                        1675+          DS     FD                      gap
                                                     1676+*
 000026F0                                            1677+X38       DS     0F
 000026F0   E310 5010 0014                  00000010 1678+          LGF    R1,V2ADDR               load v2 source
 000026F6   E761 0000 0806                  00000000 1679+          VL     v22,0(R1)               use v22 to test decoder
 000026FC   E310 5014 0014                  00000014 1680+          LGF    R1,V3ADDR               load v3 source
 00002702   E771 0000 0806                  00000000 1681+          VL     v23,0(R1)               use v23 to test decoder
 00002708   E766 7000 2EF5                           1682+          VSCBI  V22,V22,V23,2            test instruction (dest is a source)
 0000270E   E760 5028 080E                  000026D8 1683+          VST    V22,V1038               save v1 output
 00002714   07FB                                     1684+          BR     R11                     return
 00002718                                            1685+RE38      DC     0F                      xl16 expected result
 00002718                                            1686+          DROP   R5
 00002718   00000001 00000001                        1687           DC     XL16'0000000100000001 0000000000000001'     result
 00002720   00000000 00000001
 00002728   91020304 05060708                        1688           DC     XL16'9102030405060708 090A0B0CAD0E0F00'     v2
 00002730   090A0B0C AD0E0F00
 00002738   01020304 05060708                        1689           DC     XL16'0102030405060708 FFFFFFFF0FFFFFFF'     v3
 00002740   FFFFFFFF 0FFFFFFF
                                                     1690
                                                     1691           VRR_C  VSCBI,2
 00002748                                            1692+          DS     0FD
 00002748                         00002748           1693+          USING  *,R5                    base for test data and test routine
 00002748   00002788                                 1694+T39       DC     A(X39)                  address of test routine
 0000274C   0027                                     1695+          DC     H'39'                   test number
 0000274E   00                                       1696+          DC     X'00'
 0000274F   02                                       1697+          DC     HL1'2'                  m4
 00002750   E5E2C3C2 C9404040                         1698+          DC     CL8'VSCBI'              instruction name
 00002758   000027C0                                 1699+          DC     A(RE39+16)              address of v2 source
 0000275C   000027D0                                 1700+          DC     A(RE39+32)              address of v3 source
 00002760   00000010                                 1701+          DC     A(16)                   result length
 00002764   000027B0                                 1702+REA39     DC     A(RE39)                 result address
 00002768   00000000 00000000                        1703+          DS     FD                      gap
 00002770   00000000 00000000                        1704+V1039     DS     XL16                    V1 output
```

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  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

00002778   00000000 00000000
00002780   00000000 00000000              1705+           DS     FD              gap
                                          1706+*
00002788                                  1707+X39        DS     0F
00002788   E310 5010 0014         00000010 1708+          LGF    R1,V2ADDR       load v2 source
0000278E   E761 0000 0806         00000000 1709+          VL     v22,0(R1)       use v22 to test decoder
00002794   E310 5014 0014         00000014 1710+          LGF    R1,V3ADDR       load v3 source
0000279A   E771 0000 0806         00000000 1711+          VL     v23,0(R1)       use v23 to test decoder
000027A0   E766 7000 2EF5                  1712+          VSCBI  V22,V22,V23,2    test instruction (dest is a source)
000027A6   E760 5028 080E         00002770 1713+          VST    V22,V1039       save v1 output
000027AC   07FB                             1714+         BR     R11             return
000027B0                                   1715+RE39      DC     0F              xl16 expected result
000027B0                                   1716+          DROP   R5
000027B0   00000001 00000000              1717           DC     XL16'0000000100000000 0000000000000001'    result
000027B8   00000000 00000001
000027C0   FEFDFCFB 00F9F8F7              1718           DC     XL16'FEFDFCFB00F9F8F7 090A0B0CFD0E0F00'    v2
000027C8   090A0B0C FD0E0F00
000027D0   01020304 05060708              1719           DC     XL16'0102030405060708 FEFDFCFBFAF9F8F7'    v3
000027D8   FEFDFCFB FAF9F8F7

                                          1720
                                          1721 *Doubleword
                                          1722           VRR_C  VSCBI,3
000027E0                                   1723+          DS     0FD
000027E0                         000027E0  1724+          USING  *,R5            base for test data and test routine
000027E0   00002820                       1725+T40        DC     A(X40)          address of test routine
000027E4   0028                           1726+          DC     H'40'           test number
000027E6   00                             1727+          DC     X'00'
000027E7   03                             1728+          DC     HL1'3'          m4
000027E8   E5E2C3C2 C9404040              1729+          DC     CL8'VSCBI'      instruction name
000027F0   00002858                       1730+          DC     A(RE40+16)      address of v2 source
000027F4   00002868                       1731+          DC     A(RE40+32)      address of v3 source
000027F8   00000010                       1732+          DC     A(16)           result length
000027FC   00002848                       1733+REA40      DC     A(RE40)         result address
00002800   00000000 00000000              1734+          DS     FD              gap
00002808   00000000 00000000              1735+V1040      DS     XL16            V1 output
00002810   00000000 00000000
00002818   00000000 00000000              1736+          DS     FD              gap
                                          1737+*
00002820                                   1738+X40        DS     0F
00002820   E310 5010 0014         00000010 1739+          LGF    R1,V2ADDR       load v2 source
00002826   E761 0000 0806         00000000 1740+          VL     v22,0(R1)       use v22 to test decoder
0000282C   E310 5014 0014         00000014 1741+          LGF    R1,V3ADDR       load v3 source
00002832   E771 0000 0806         00000000 1742+          VL     v23,0(R1)       use v23 to test decoder
00002838   E766 7000 3EF5                  1743+          VSCBI  V22,V22,V23,3    test instruction (dest is a source)
0000283E   E760 5028 080E         00002808 1744+          VST    V22,V1040       save v1 output
00002844   07FB                             1745+         BR     R11             return
00002848                                   1746+RE40      DC     0F              xl16 expected result
00002848                                   1747+          DROP   R5
00002848   00000000 00000001              1748           DC     XL16'0000000000000001 0000000000000000'    result
00002850   00000000 00000000
00002858   FFFFFFFF FFFFFFFF              1749           DC     XL16'FFFFFFFFFFFFFFFF 0102030405060708'    v2
00002860   01020304 05060708
00002868   01020304 05060708              1750           DC     XL16'0102030405060708 090A0B0C0D0E0F00'    v3
00002870   090A0B0C 0D0E0F00
                                          1751
                                          1752           VRR_C  VSCBI,3
```

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  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

00002878                                       1753+       DS     0FD
00002878                      00002878         1754+       USING  *,R5              base for test data and test routine
00002878  000028B8                             1755+T41    DC     A(X41)            address of test routine
0000287C  0029                                 1756+       DC     H'41'             test number
0000287E  00                                   1757+       DC     X'00'
0000287F  03                                   1758+       DC     HL1'3'            m4
00002880  E5E2C3C2 C9404040                    1759+       DC     CL8'VSCBI'        instruction name
00002888  000028F0                             1760+       DC     A(RE41+16)        address of v2 source
0000288C  00002900                             1761+       DC     A(RE41+32)        address of v3 source
00002890  00000010                             1762+       DC     A(16)             result length
00002894  000028E0                             1763+REA41  DC     A(RE41)           result address
00002898  00000000 00000000                    1764+       DS     FD                gap
000028A0  00000000 00000000                    1765+V1041  DS     XL16              V1 output
000028A8  00000000 00000000
000028B0  00000000 00000000                    1766+       DS     FD                gap
                                               1767+*
000028B8                                       1768+X41    DS     0F
000028B8  E310 5010 0014               00000010 1769+       LGF    R1,V2ADDR         load v2 source
000028BE  E761 0000 0806               00000000 1770+       VL     v22,0(R1)         use v22 to test decoder
000028C4  E310 5014 0014               00000014 1771+       LGF    R1,V3ADDR         load v3 source
000028CA  E771 0000 0806               00000000 1772+       VL     v23,0(R1)         use v23 to test decoder
000028D0  E766 7000 3EF5                        1773+       VSCBI  V22,V22,V23,3      test instruction (dest is a source)
000028D6  E760 5028 080E               000028A0 1774+       VST    V22,V1041         save v1 output
000028DC  07FB                                  1775+       BR     R11               return
000028E0                                        1776+RE41  DC     0F                xl16 expected result
000028E0                                        1777+       DROP   R5
000028E0  00000000 00000001                     1778        DC     XL16'00000000000000001 00000000000000001'   result
000028E8  00000000 00000001
000028F0  01020304 05060708                     1779        DC     XL16'0102030405060708 090A0B0C0D0E0F00'    v2
000028F8  090A0B0C 0D0E0F00
00002900  01020304 05060708                     1780        DC     XL16'0102030405060708 00FFFFFFFFFFFFFF'    v3
00002908  00FFFFFF FFFFFFFF
                                                1781
                                                1782        VRR_C  VSCBI,3
00002910                                        1783+       DS     0FD
00002910                      00002910          1784+       USING  *,R5              base for test data and test routine
00002910  00002950                              1785+T42    DC     A(X42)            address of test routine
00002914  002A                                  1786+       DC     H'42'             test number
00002916  00                                    1787+       DC     X'00'
00002917  03                                    1788+       DC     HL1'3'            m4
00002918  E5E2C3C2 C9404040                     1789+       DC     CL8'VSCBI'        instruction name
00002920  00002988                              1790+       DC     A(RE42+16)        address of v2 source
00002924  00002998                              1791+       DC     A(RE42+32)        address of v3 source
00002928  00000010                              1792+       DC     A(16)             result length
0000292C  00002978                              1793+REA42  DC     A(RE42)           result address
00002930  00000000 00000000                     1794+       DS     FD                gap
00002938  00000000 00000000                     1795+V1042  DS     XL16              V1 output
00002940  00000000 00000000
00002948  00000000 00000000                     1796+       DS     FD                gap
                                                1797+*
00002950                                        1798+X42    DS     0F
00002950  E310 5010 0014               00000010 1799+       LGF    R1,V2ADDR         load v2 source
00002956  E761 0000 0806               00000000 1800+       VL     v22,0(R1)         use v22 to test decoder
0000295C  E310 5014 0014               00000014 1801+       LGF    R1,V3ADDR         load v3 source
00002962  E771 0000 0806               00000000 1802+       VL     v23,0(R1)         use v23 to test decoder
00002968  E766 7000 3EF5                        1803+       VSCBI  V22,V22,V23,3      test instruction (dest is a source)
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  LOC          OBJECT CODE      ADDR1      ADDR2      STMT

0000296E  E760 5028 080E                 00002938   1804+          VST     V22,V1042           save v1 output
00002974  07FB                                      1805+          BR      R11                 return
00002978                                            1806+RE42      DC      0F                  xl16 expected result
00002978                                            1807+          DROP    R5
00002978  00000000 00000000                          1808          DC      XL16'0000000000000000 0000000000000001'   result
00002980  00000000 00000001
00002988  00FDFCFB FAF9F8F7                           1809          DC      XL16'00FDFCFBFAF9F8F7 090A0B0C0D0E0F00'   v2
00002990  090A0B0C 0D0E0F00
00002998  01020304 05060708                           1810          DC      XL16'0102030405060708 00FDFCFBFAF9F8F7'   v3
000029A0  00FDFCFB FAF9F8F7

                                                      1811
                                                      1812 *Quadword
                                                      1813          VRR_C   VSCBI,4
000029A8                                              1814+         DS      0FD
000029A8                                 000029A8     1815+         USING   *,R5                base for test data and test routine
000029A8  000029E8                                    1816+T43      DC      A(X43)              address of test routine
000029AC  002B                                        1817+         DC      H'43'               test number
000029AE  00                                          1818+         DC      X'00'
000029AF  04                                          1819+         DC      HL1'4'              m4
000029B0  E5E2C3C2 C9404040                            1820+         DC      CL8'VSCBI'          instruction name
000029B8  00002A20                                    1821+         DC      A(RE43+16)          address of v2 source
000029BC  00002A30                                    1822+         DC      A(RE43+32)          address of v3 source
000029C0  00000010                                    1823+         DC      A(16)               result length
000029C4  00002A10                                    1824+REA43    DC      A(RE43)             result address
000029C8  00000000 00000000                            1825+        DS      FD                  gap
000029D0  00000000 00000000                            1826+V1043   DS      XL16                V1 output
000029D8  00000000 00000000
000029E0  00000000 00000000                            1827+        DS      FD                  gap
                                                      1828+*
000029E8                                              1829+X43      DS      0F
000029E8  E310 5010 0014                 00000010     1830+         LGF     R1,V2ADDR           load v2 source
000029EE  E761 0000 0806                 00000000     1831+         VL      v22,0(R1)           use v22 to test decoder
000029F4  E310 5014 0014                 00000014     1832+         LGF     R1,V3ADDR           load v3 source
000029FA  E771 0000 0806                 00000000     1833+         VL      v23,0(R1)           use v23 to test decoder
00002A00  E766 7000 4EF5                              1834+         VSCBI   V22,V22,V23,4        test instruction (dest is a source)
00002A06  E760 5028 080E                 000029D0     1835+         VST     V22,V1043            save v1 output
00002A0C  07FB                                        1836+         BR      R11                 return
00002A10                                              1837+RE43     DC      0F                  xl16 expected result
00002A10                                              1838+         DROP    R5
00002A10  00000000 00000000                            1839          DC      XL16'0000000000000000 0000000000000001'   result
00002A18  00000000 00000001
00002A20  FFFFFFFF FFFFFFFF                            1840          DC      XL16'FFFFFFFFFFFFFFFF 0102030405060708'   v2
00002A28  01020304 05060708
00002A30  01020304 05060708                            1841          DC      XL16'0102030405060708 090A0B0C0D0E0F00'   v3
00002A38  090A0B0C 0D0E0F00

                                                      1842
                                                      1843          VRR_C   VSCBI,4
00002A40                                              1844+         DS      0FD
00002A40                                 00002A40     1845+         USING   *,R5                base for test data and test routine
00002A40  00002A80                                    1846+T44      DC      A(X44)              address of test routine
00002A44  002C                                        1847+         DC      H'44'               test number
00002A46  00                                          1848+         DC      X'00'
00002A47  04                                          1849+         DC      HL1'4'              m4
00002A48  E5E2C3C2 C9404040                            1850+         DC      CL8'VSCBI'          instruction name
00002A50  00002AB8                                    1851+         DC      A(RE44+16)          address of v2 source
00002A54  00002AC8                                    1852+         DC      A(RE44+32)          address of v3 source
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   LOC        OBJECT CODE      ADDR1      ADDR2    STMT

00002A58   00000010                              1853+        DC     A(16)              result length
00002A5C   00002AA8                              1854+REA44   DC     A(RE44)            result address
00002A60   00000000 00000000                     1855+        DS     FD                 gap
00002A68   00000000 00000000                     1856+V1044   DS     XL16               V1 output
00002A70   00000000 00000000
00002A78   00000000 00000000                     1857+        DS     FD                 gap
                                                 1858+*
00002A80                                         1859+X44     DS     0F
00002A80   E310 5010 0014             00000010   1860+        LGF    R1,V2ADDR          load v2 source
00002A86   E761 0000 0806             00000000   1861+        VL     v22,0(R1)          use v22 to test decoder
00002A8C   E310 5014 0014             00000014   1862+        LGF    R1,V3ADDR          load v3 source
00002A92   E771 0000 0806             00000000   1863+        VL     v23,0(R1)          use v23 to test decoder
00002A98   E766 7000 4EF5                        1864+        VSCBI  V22,V22,V23,4       test instruction (dest is a source)
00002A9E   E760 5028 080E             00002A68   1865+        VST    V22,V1044          save v1 output
00002AA4   07FB                                  1866+        BR     R11                return
00002AA8                                         1867+RE44    DC     0F                 xl16 expected result
00002AA8                                         1868+        DROP   R5
00002AA8   00000000 00000000                     1869         DC     XL16'0000000000000000 0000000000000001'   result
00002AB0   00000000 00000001
00002AB8   01020304 05060708                     1870         DC     XL16'0102030405060708 090A0B0C0D0E0F00'   v2
00002AC0   090A0B0C 0D0E0F00
00002AC8   01020304 05060708                     1871         DC     XL16'0102030405060708 00FFFFFFFFFFFFFF'   v3
00002AD0   00FFFFFF FFFFFFFF
                                                 1872
                                                 1873         VRR_C  VSCBI,4
00002AD8                                         1874+        DS     0FD
00002AD8                   00002AD8              1875+        USING  *,R5              base for test data and test routine
00002AD8   00002B18                              1876+T45     DC     A(X45)            address of test routine
00002ADC   002D                                  1877+        DC     H'45'             test number
00002ADE   00                                    1878+        DC     X'00'
00002ADF   04                                    1879+        DC     HL1'4'            m4
00002AE0   E5E2C3C2 C9404040                     1880+        DC     CL8'VSCBI'        instruction name
00002AE8   00002B50                              1881+        DC     A(RE45+16)        address of v2 source
00002AEC   00002B60                              1882+        DC     A(RE45+32)        address of v3 source
00002AF0   00000010                              1883+        DC     A(16)             result length
00002AF4   00002B40                              1884+REA45   DC     A(RE45)           result address
00002AF8   00000000 00000000                     1885+        DS     FD                gap
00002B00   00000000 00000000                     1886+V1045   DS     XL16              V1 output
00002B08   00000000 00000000
00002B10   00000000 00000000                     1887+        DS     FD                gap
                                                 1888+*
00002B18                                         1889+X45     DS     0F
00002B18   E310 5010 0014             00000010   1890+        LGF    R1,V2ADDR         load v2 source
00002B1E   E761 0000 0806             00000000   1891+        VL     v22,0(R1)         use v22 to test decoder
00002B24   E310 5014 0014             00000014   1892+        LGF    R1,V3ADDR         load v3 source
00002B2A   E771 0000 0806             00000000   1893+        VL     v23,0(R1)         use v23 to test decoder
00002B30   E766 7000 4EF5                        1894+        VSCBI  V22,V22,V23,4      test instruction (dest is a source)
00002B36   E760 5028 080E             00002B00   1895+        VST    V22,V1045         save v1 output
00002B3C   07FB                                  1896+        BR     R11               return
00002B40                                         1897+RE45    DC     0F                xl16 expected result
00002B40                                         1898+        DROP   R5
00002B40   00000000 00000000                     1899         DC     XL16'0000000000000000 0000000000000000'   result
00002B48   00000000 00000000
00002B50   00FDFCFB FAF9F8F7                     1900         DC     XL16'00FDFCFBFAF9F8F7 090A0B0C0D0E0F00'   v2
00002B58   090A0B0C 0D0E0F00
00002B60   01020304 05060708                     1901         DC     XL16'0102030405060708 00FDFCFBFAF9F8F7'   v3
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  LOC        OBJECT CODE      ADDR1      ADDR2     STMT

00002B68   00FDFCFB FAF9F8F7
                                                   1902
                                                   1903
                                                   1904 *----------------------------------------------------------------------
                                                   1905 *    VACC   - Vector Add Compute Carry
                                                   1906 *----------------------------------------------------------------------
                                                   1907 *Byte
                                                   1908         VRR_C VACC,0
00002B70                                           1909+        DS    0FD
00002B70                        00002B70           1910+        USING *,R5                  base for test data and test routine
00002B70   00002BB0                                1911+T46     DC    A(X46)                address of test routine
00002B74   002E                                    1912+        DC    H'46'                 test number
00002B76   00                                      1913+        DC    X'00'
00002B77   00                                      1914+        DC    HL1'0'                m4
00002B78   E5C1C3C3 40404040                       1915+        DC    CL8'VACC'             instruction name
00002B80   00002BE8                                1916+        DC    A(RE46+16)            address of v2 source
00002B84   00002BF8                                1917+        DC    A(RE46+32)            address of v3 source
00002B88   00000010                                1918+        DC    A(16)                 result length
00002B8C   00002BD8                                1919+REA46   DC    A(RE46)               result address
00002B90   00000000 00000000                       1920+        DS    FD                    gap
00002B98   00000000 00000000                       1921+V1046   DS    XL16                  V1 output
00002BA0   00000000 00000000
00002BA8   00000000 00000000                       1922+        DS    FD                    gap
                                                   1923+*
00002BB0                                           1924+X46     DS    0F
00002BB0   E310 5010 0014            00000010       1925+        LGF   R1,V2ADDR             load v2 source
00002BB6   E761 0000 0806            00000000       1926+        VL    v22,0(R1)             use v22 to test decoder
00002BBC   E310 5014 0014            00000014       1927+        LGF   R1,V3ADDR             load v3 source
00002BC2   E771 0000 0806            00000000       1928+        VL    v23,0(R1)             use v23 to test decoder
00002BC8   E766 7000 0EF1                           1929+        VACC  V22,V22,V23,0          test instruction (dest is a source)
00002BCE   E760 5028 080E            00002B98       1930+        VST   V22,V1046              save v1 output
00002BD4   07FB                                     1931+        BR    R11                   return
00002BD8                                            1932+RE46    DC    0F                    xl16 expected result
00002BD8                                            1933+        DROP  R5
00002BD8   01010101 01010101                        1934         DC    XL16'0101010101010101 0000000000000000'    result
00002BE0   00000000 00000000
00002BE8   FFFFFFFF FFFFFFFF                         1935         DC    XL16'FFFFFFFFFFFFFFFF 0102030405060708'    v2
00002BF0   01020304 05060708
00002BF8   01020304 05060708                         1936         DC    XL16'0102030405060708 090A0B0C0D0E0F00'    v3
00002C00   090A0B0C 0D0E0F00
                                                    1937
                                                    1938         VRR_C VACC,0
00002C08                                            1939+        DS    0FD
00002C08                        00002C08            1940+        USING *,R5                  base for test data and test routine
00002C08   00002C48                                 1941+T47     DC    A(X47)                address of test routine
00002C0C   002F                                     1942+        DC    H'47'                 test number
00002C0E   00                                       1943+        DC    X'00'
00002C0F   00                                       1944+        DC    HL1'0'                m4
00002C10   E5C1C3C3 40404040                        1945+        DC    CL8'VACC'             instruction name
00002C18   00002C80                                 1946+        DC    A(RE47+16)            address of v2 source
00002C1C   00002C90                                 1947+        DC    A(RE47+32)            address of v3 source
00002C20   00000010                                 1948+        DC    A(16)                 result length
00002C24   00002C70                                 1949+REA47   DC    A(RE47)               result address
00002C28   00000000 00000000                        1950+        DS    FD                    gap
00002C30   00000000 00000000                        1951+V1047   DS    XL16                  V1 output
00002C38   00000000 00000000
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT

```
00002C40  00000000 00000000                         1952+        DS     FD            gap
                                                     1953+*
00002C48                                             1954+X47     DS     0F
00002C48  E310 5010 0014                  00000010   1955+        LGF    R1,V2ADDR     load v2 source
00002C4E  E761 0000 0806                  00000000   1956+        VL     v22,0(R1)     use v22 to test decoder
00002C54  E310 5014 0014                  00000014   1957+        LGF    R1,V3ADDR     load v3 source
00002C5A  E771 0000 0806                  00000000   1958+        VL     v23,0(R1)     use v23 to test decoder
00002C60  E766 7000 0EF1                             1959+        VACC   V22,V22,V23,0  test instruction (dest is a source)
00002C66  E760 5028 080E                  00002C30   1960+        VST    V22,V1047      save v1 output
00002C6C  07FB                                       1961+        BR     R11           return
00002C70                                             1962+RE47    DC     0F            xl16 expected result
00002C70                                             1963+        DROP   R5
00002C70  00000000 00000000                          1964         DC     XL16'0000000000000000 0101010101010100'    result
00002C78  01010101 01010100
00002C80  01020304 05060708                          1965         DC     XL16'0102030405060708 090A0B0C0D0E0F00'    v2
00002C88  090A0B0C 0D0E0F00
00002C90  01020304 05060708                          1966         DC     XL16'0102030405060708 FFFFFFFFFFFFFFFF'    v3
00002C98  FFFFFFFF FFFFFFFF
                                                     1967
                                                     1968         VRR_C  VACC,0
00002CA0                                             1969+        DS     0FD
00002CA0                               00002CA0      1970+        USING  *,R5          base for test data and test routine
00002CA0  00002CE0                                   1971+T48     DC     A(X48)        address of test routine
00002CA4  0030                                       1972+        DC     H'48'         test number
00002CA6  00                                         1973+        DC     X'00'
00002CA7  00                                         1974+        DC     HL1'0'        m4
00002CA8  E5C1C3C3 40404040                          1975+        DC     CL8'VACC'     instruction name
00002CB0  00002D18                                   1976+        DC     A(RE48+16)    address of v2 source
00002CB4  00002D28                                   1977+        DC     A(RE48+32)    address of v3 source
00002CB8  00000010                                   1978+        DC     A(16)         result length
00002CBC  00002D08                                   1979+REA48   DC     A(RE48)       result address
00002CC0  00000000 00000000                          1980+        DS     FD            gap
00002CC8  00000000 00000000                          1981+V1048   DS     XL16          V1 output
00002CD0  00000000 00000000
00002CD8  00000000 00000000                          1982+        DS     FD            gap
                                                     1983+*
00002CE0                                             1984+X48     DS     0F
00002CE0  E310 5010 0014                  00000010   1985+        LGF    R1,V2ADDR     load v2 source
00002CE6  E761 0000 0806                  00000000   1986+        VL     v22,0(R1)     use v22 to test decoder
00002CEC  E310 5014 0014                  00000014   1987+        LGF    R1,V3ADDR     load v3 source
00002CF2  E771 0000 0806                  00000000   1988+        VL     v23,0(R1)     use v23 to test decoder
00002CF8  E766 7000 0EF1                             1989+        VACC   V22,V22,V23,0  test instruction (dest is a source)
00002CFE  E760 5028 080E                  00002CC8   1990+        VST    V22,V1048      save v1 output
00002D04  07FB                                       1991+        BR     R11           return
00002D08                                             1992+RE48    DC     0F            xl16 expected result
00002D08                                             1993+        DROP   R5
00002D08  00000000 00000101                          1994         DC     XL16'0000000000000101 0101010101010100'    result
00002D10  01010101 01010100
00002D18  FEFD01FB FAF9F8F7                          1995         DC     XL16'FEFD01FBFAF9F8F7 090AFB0C0D0E0F00'    v2
00002D20  090AFB0C 0D0E0F00
00002D28  01020304 0506B7F8                          1996         DC     XL16'010203040506B7F8 FEFDF0FBFAF9F8F7'    v3
00002D30  FEFDF0FB FAF9F8F7
                                                     1997
                                                     1998 *Halfword
                                                     1999         VRR_C  VACC,1
00002D38                                             2000+        DS     0FD
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002D38                      00002D38            2001+         USING *,R5              base for test data and test routine
00002D38   00002D78                               2002+T49      DC    A(X49)            address of test routine
00002D3C   0031                                   2003+         DC    H'49'             test number
00002D3E   00                                     2004+         DC    X'00'
00002D3F   01                                     2005+         DC    HL1'1'            m4
00002D40   E5C1C3C3 40404040                       2006+         DC    CL8'VACC'         instruction name
00002D48   00002DB0                               2007+         DC    A(RE49+16)        address of v2 source
00002D4C   00002DC0                               2008+         DC    A(RE49+32)        address of v3 source
00002D50   00000010                               2009+         DC    A(16)             result length
00002D54   00002DA0                               2010+REA49    DC    A(RE49)           result address
00002D58   00000000 00000000                       2011+         DS    FD                gap
00002D60   00000000 00000000                       2012+V1049    DS    XL16              V1 output
00002D68   00000000 00000000
00002D70   00000000 00000000                       2013+         DS    FD                gap
                                                   2014+*
00002D78                                           2015+X49      DS    0F
00002D78   E310 5010 0014                00000010  2016+         LGF   R1,V2ADDR         load v2 source
00002D7E   E761 0000 0806                00000000  2017+         VL    v22,0(R1)         use v22 to test decoder
00002D84   E310 5014 0014                00000014  2018+         LGF   R1,V3ADDR         load v3 source
00002D8A   E771 0000 0806                00000000  2019+         VL    v23,0(R1)         use v23 to test decoder
00002D90   E766 7000 1EF1                          2020+         VACC  V22,V22,V23,1      test instruction (dest is a source)
00002D96   E760 5028 080E                00002D60  2021+         VST   V22,V1049          save v1 output
00002D9C   07FB                                    2022+         BR    R11               return
00002DA0                                           2023+RE49     DC    0F                xl16 expected result
00002DA0                                           2024+         DROP  R5
00002DA0   00010001 00010001                       2025          DC    XL16'0001000100010001 0000000000000000'     result
00002DA8   00000000 00000000
00002DB0   FFFFFFFF FFFFFFFF                        2026          DC    XL16'FFFFFFFFFFFFFFFF 0102030405060708'     v2
00002DB8   01020304 05060708
00002DC0   01020304 05060708                        2027          DC    XL16'0102030405060708 090A0B0C0D0E0F00'     v3
00002DC8   090A0B0C 0D0E0F00
                                                   2028
                                                   2029          VRR_C VACC,1
00002DD0                                           2030+         DS    0FD
00002DD0                      00002DD0            2031+         USING *,R5              base for test data and test routine
00002DD0   00002E10                               2032+T50      DC    A(X50)            address of test routine
00002DD4   0032                                   2033+         DC    H'50'             test number
00002DD6   00                                     2034+         DC    X'00'
00002DD7   01                                     2035+         DC    HL1'1'            m4
00002DD8   E5C1C3C3 40404040                        2036+         DC    CL8'VACC'         instruction name
00002DE0   00002E48                               2037+         DC    A(RE50+16)        address of v2 source
00002DE4   00002E58                               2038+         DC    A(RE50+32)        address of v3 source
00002DE8   00000010                               2039+         DC    A(16)             result length
00002DEC   00002E38                               2040+REA50    DC    A(RE50)           result address
00002DF0   00000000 00000000                       2041+         DS    FD                gap
00002DF8   00000000 00000000                       2042+V1050    DS    XL16              V1 output
00002E00   00000000 00000000
00002E08   00000000 00000000                       2043+         DS    FD                gap
                                                   2044+*
00002E10                                           2045+X50      DS    0F
00002E10   E310 5010 0014                00000010  2046+         LGF   R1,V2ADDR         load v2 source
00002E16   E761 0000 0806                00000000  2047+         VL    v22,0(R1)         use v22 to test decoder
00002E1C   E310 5014 0014                00000014  2048+         LGF   R1,V3ADDR         load v3 source
00002E22   E771 0000 0806                00000000  2049+         VL    v23,0(R1)         use v23 to test decoder
00002E28   E766 7000 1EF1                          2050+         VACC  V22,V22,V23,1      test instruction (dest is a source)
00002E2E   E760 5028 080E                00002DF8  2051+         VST   V22,V1050          save v1 output
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00002E34  07FB                                    2052+         BR    R11              return
00002E38                                          2053+RE50     DC    0F               xl16 expected result
00002E38                                          2054+         DROP  R5
00002E38  00000000 00000000                       2055          DC    XL16'0000000000000000 0001000100010000'    result
00002E40  00010001 00010000
00002E48  01020304 05060708                       2056          DC    XL16'0102030405060708 090A0B0C0D0E0F00'    v2
00002E50  090A0B0C 0D0E0F00
00002E58  01020304 05060708                       2057          DC    XL16'0102030405060708 FFFFFFFFFFFF00FF'    v3
00002E60  FFFFFFFF FFFF00FF
                                                  2058
                                                  2059          VRR_C VACC,1
00002E68                                          2060+         DS    0FD
00002E68                              00002E68     2061+         USING *,R5            base for test data and test routine
00002E68  00002EA8                                2062+T51      DC    A(X51)           address of test routine
00002E6C  0033                                    2063+         DC    H'51'            test number
00002E6E  00                                      2064+         DC    X'00'
00002E6F  01                                      2065+         DC    HL1'1'           m4
00002E70  E5C1C3C3 40404040                       2066+         DC    CL8'VACC'        instruction name
00002E78  00002EE0                                2067+         DC    A(RE51+16)       address of v2 source
00002E7C  00002EF0                                2068+         DC    A(RE51+32)       address of v3 source
00002E80  00000010                                2069+         DC    A(16)            result length
00002E84  00002ED0                                2070+REA51    DC    A(RE51)          result address
00002E88  00000000 00000000                       2071+         DS    FD               gap
00002E90  00000000 00000000                       2072+V1051    DS    XL16             V1 output
00002E98  00000000 00000000
00002EA0  00000000 00000000                       2073+         DS    FD               gap
                                                  2074+*
00002EA8                                          2075+X51      DS    0F
00002EA8  E310 5010 0014                00000010   2076+         LGF   R1,V2ADDR        load v2 source
00002EAE  E761 0000 0806                00000000   2077+         VL    v22,0(R1)        use v22 to test decoder
00002EB4  E310 5014 0014                00000014   2078+         LGF   R1,V3ADDR        load v3 source
00002EBA  E771 0000 0806                00000000   2079+         VL    v23,0(R1)        use v23 to test decoder
00002EC0  E766 7000 1EF1                           2080+         VACC  V22,V22,V23,1     test instruction (dest is a source)
00002EC6  E760 5028 080E                00002E90   2081+         VST   V22,V1051        save v1 output
00002ECC  07FB                                    2082+         BR    R11              return
00002ED0                                          2083+RE51     DC    0F               xl16 expected result
00002ED0                                          2084+         DROP  R5
00002ED0  00000000 00010001                       2085          DC    XL16'0000000000010001 0000000100010001'    result
00002ED8  00000001 00010001
00002EE0  FEFDFC0B FAF9F8F7                       2086          DC    XL16'FEFDFC0BFAF9F8F7 B90A0B0C0D0E0F00'    v2
00002EE8  B90A0B0C 0D0E0F00
00002EF0  010203B4 B506F708                       2087          DC    XL16'010203B4B506F708 0EFDFCFBFAF9F8F7'    v3
00002EF8  0EFDFCFB FAF9F8F7
                                                  2088
                                                  2089 *Word
                                                  2090          VRR_C VACC,2
00002F00                                          2091+         DS    0FD
00002F00                              00002F00     2092+         USING *,R5            base for test data and test routine
00002F00  00002F40                                2093+T52      DC    A(X52)           address of test routine
00002F04  0034                                    2094+         DC    H'52'            test number
00002F06  00                                      2095+         DC    X'00'
00002F07  02                                      2096+         DC    HL1'2'           m4
00002F08  E5C1C3C3 40404040                       2097+         DC    CL8'VACC'        instruction name
00002F10  00002F78                                2098+         DC    A(RE52+16)       address of v2 source
00002F14  00002F88                                2099+         DC    A(RE52+32)       address of v3 source
00002F18  00000010                                2100+         DC    A(16)            result length
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002F1C	00002F68			2101+REA52	DC	A(RE52)	result address
00002F20	00000000 00000000			2102+	DS	FD	gap
00002F28	00000000 00000000			2103+V1052	DS	XL16	V1 output
00002F30	00000000 00000000						
00002F38	00000000 00000000			2104+	DS	FD	gap
				2105+*			
00002F40				2106+X52	DS	0F	
00002F40	E310 5010 0014		00000010	2107+	LGF	R1,V2ADDR	load v2 source
00002F46	E761 0000 0806		00000000	2108+	VL	v22,0(R1)	use v22 to test decoder
00002F4C	E310 5014 0014		00000014	2109+	LGF	R1,V3ADDR	load v3 source
00002F52	E771 0000 0806		00000000	2110+	VL	v23,0(R1)	use v23 to test decoder
00002F58	E766 7000 2EF1			2111+	VACC	V22,V22,V23,2	test instruction (dest is a source)
00002F5E	E760 5028 080E		00002F28	2112+	VST	V22,V1052	save v1 output
00002F64	07FB			2113+	BR	R11	return
00002F68				2114+RE52	DC	0F	xl16 expected result
00002F68				2115+	DROP	R5	
00002F68	00000001 00000001			2116	DC	XL16'0000000100000001 0000000000000000'	result
00002F70	00000000 00000000						
00002F78	FFFFFFFF FFFFFFFF			2117	DC	XL16'FFFFFFFFFFFFFFFF 0102030405060708'	v2
00002F80	01020304 05060708						
00002F88	01020304 05060708			2118	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v3
00002F90	090A0B0C 0D0E0F00						
				2119			
				2120	VRR_C	VACC,2	
00002F98				2121+	DS	0FD	
00002F98		00002F98		2122+	USING	*,R5	base for test data and test routine
00002F98	00002FD8			2123+T53	DC	A(X53)	address of test routine
00002F9C	0035			2124+	DC	H'53'	test number
00002F9E	00			2125+	DC	X'00'	
00002F9F	02			2126+	DC	HL1'2'	m4
00002FA0	E5C1C3C3 40404040			2127+	DC	CL8'VACC'	instruction name
00002FA8	00003010			2128+	DC	A(RE53+16)	address of v2 source
00002FAC	00003020			2129+	DC	A(RE53+32)	address of v3 source
00002FB0	00000010			2130+	DC	A(16)	result length
00002FB4	00003000			2131+REA53	DC	A(RE53)	result address
00002FB8	00000000 00000000			2132+	DS	FD	gap
00002FC0	00000000 00000000			2133+V1053	DS	XL16	V1 output
00002FC8	00000000 00000000						
00002FD0	00000000 00000000			2134+	DS	FD	gap
				2135+*			
00002FD8				2136+X53	DS	0F	
00002FD8	E310 5010 0014		00000010	2137+	LGF	R1,V2ADDR	load v2 source
00002FDE	E761 0000 0806		00000000	2138+	VL	v22,0(R1)	use v22 to test decoder
00002FE4	E310 5014 0014		00000014	2139+	LGF	R1,V3ADDR	load v3 source
00002FEA	E771 0000 0806		00000000	2140+	VL	v23,0(R1)	use v23 to test decoder
00002FF0	E766 7000 2EF1			2141+	VACC	V22,V22,V23,2	test instruction (dest is a source)
00002FF6	E760 5028 080E		00002FC0	2142+	VST	V22,V1053	save v1 output
00002FFC	07FB			2143+	BR	R11	return
00003000				2144+RE53	DC	0F	xl16 expected result
00003000				2145+	DROP	R5	
00003000	00000000 00000001			2146	DC	XL16'0000000000000001 0000000100000000'	result
00003008	00000001 00000000						
00003010	91020304 F5060708			2147	DC	XL16'91020304F5060708 090A0B0CAD0E0F00'	v2
00003018	090A0B0C AD0E0F00						
00003020	01020304 F5060708			2148	DC	XL16'01020304F5060708 FFFFFFFF0FFFFFFF'	v3
00003028	FFFFFFFF 0FFFFFFF						

```
  LOC        OBJECT CODE      ADDR1     ADDR2    STMT


                                                 2149
                                                 2150              VRR_C VACC, 2
00003030                                         2151+      DS     0FD
00003030                               00003030  2152+      USING *, R5                  base for test data and test routine
00003030    00003070                             2153+T54   DC     A(X54)                address of test routine
00003034    0036                                 2154+      DC     H'54'                 test number
00003036    00                                   2155+      DC     X'00'
00003037    02                                   2156+      DC     HL1'2'                m4
00003038    E5C1C3C3 40404040                     2157+      DC     CL8'VACC'             instruction name
00003040    000030A8                             2158+      DC     A(RE54+16)            address of v2 source
00003044    000030B8                             2159+      DC     A(RE54+32)            address of v3 source
00003048    00000010                             2160+      DC     A(16)                 result length
0000304C    00003098                             2161+REA54 DC     A(RE54)               result address
00003050    00000000 00000000                    2162+      DS     FD                    gap
00003058    00000000 00000000                    2163+V1054 DS     XL16                  V1 output
00003060    00000000 00000000
00003068    00000000 00000000                    2164+      DS     FD                    gap
                                                 2165+*
00003070                                         2166+X54   DS     0F
00003070    E310 5010 0014              00000010  2167+      LGF    R1, V2ADDR            load v2 source
00003076    E761 0000 0806              00000000  2168+      VL     v22, 0(R1)            use v22 to test decoder
0000307C    E310 5014 0014              00000014  2169+      LGF    R1, V3ADDR            load v3 source
00003082    E771 0000 0806              00000000  2170+      VL     v23, 0(R1)            use v23 to test decoder
00003088    E766 7000 2EF1                        2171+      VACC   V22, V22, V23, 2       test instruction (dest is a source)
0000308E    E760 5028 080E              00003058  2172+      VST    V22, V1054             save v1 output
00003094    07FB                                  2173+      BR     R11                   return
00003098                                          2174+RE54 DC     0F                    xl16 expected result
00003098                                          2175+      DROP   R5
00003098    00000000 00000000                     2176       DC     XL16'0000000000000000 0000000100000001'    result
000030A0    00000001 00000001
000030A8    FEFDFCFB 00F9F8F7                     2177       DC     XL16'FEFDFCFB00F9F8F7 090A0B0CFD0E0F00'     v2
000030B0    090A0B0C FD0E0F00
000030B8    01020304 05060708                     2178       DC     XL16'0102030405060708 FEFDFCFBFAF9F8F7'     v3
000030C0    FEFDFCFB FAF9F8F7
                                                 2179
                                                 2180  *Doubleword
                                                 2181              VRR_C VACC, 3
000030C8                                          2182+      DS     0FD
000030C8                               000030C8   2183+      USING *, R5                  base for test data and test routine
000030C8    00003108                             2184+T55   DC     A(X55)                address of test routine
000030CC    0037                                 2185+      DC     H'55'                 test number
000030CE    00                                   2186+      DC     X'00'
000030CF    03                                   2187+      DC     HL1'3'                m4
000030D0    E5C1C3C3 40404040                     2188+      DC     CL8'VACC'             instruction name
000030D8    00003140                             2189+      DC     A(RE55+16)            address of v2 source
000030DC    00003150                             2190+      DC     A(RE55+32)            address of v3 source
000030E0    00000010                             2191+      DC     A(16)                 result length
000030E4    00003130                             2192+REA55 DC     A(RE55)               result address
000030E8    00000000 00000000                    2193+      DS     FD                    gap
000030F0    00000000 00000000                    2194+V1055 DS     XL16                  V1 output
000030F8    00000000 00000000
00003100    00000000 00000000                    2195+      DS     FD                    gap
                                                 2196+*
00003108                                          2197+X55   DS     0F
00003108    E310 5010 0014              00000010  2198+      LGF    R1, V2ADDR            load v2 source
0000310E    E761 0000 0806              00000000  2199+      VL     v22, 0(R1)            use v22 to test decoder
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003114	E310 5014 0014		00000014	2200+	LGF	R1,V3ADDR	load v3 source
0000311A	E771 0000 0806		00000000	2201+	VL	v23,0(R1)	use v23 to test decoder
00003120	E766 7000 3EF1			2202+	VACC	V22,V22,V23,3	test instruction (dest is a source)
00003126	E760 5028 080E		000030F0	2203+	VST	V22,V1055	save v1 output
0000312C	07FB			2204+	BR	R11	return
00003130				2205+RE55	DC	0F	xl16 expected result
00003130				2206+	DROP	R5	
00003130	00000000 00000001			2207	DC	XL16'0000000000000001 0000000000000000'	result
00003138	00000000 00000000						
00003140	FFFFFFFF FFFFFFFF			2208	DC	XL16'FFFFFFFFFFFFFFFF 0102030405060708'	v2
00003148	01020304 05060708						
00003150	01020304 05060708			2209	DC	XL16'0102030405060708 090A0B0C0D0E0F00'	v3
00003158	090A0B0C 0D0E0F00						
				2210			
				2211	VRR_C VACC,3		
00003160				2212+	DS	0FD	
00003160		00003160		2213+	USING *,R5		base for test data and test routine
00003160	000031A0			2214+T56	DC	A(X56)	address of test routine
00003164	0038			2215+	DC	H'56'	test number
00003166	00			2216+	DC	X'00'	
00003167	03			2217+	DC	HL1'3'	m4
00003168	E5C1C3C3 40404040			2218+	DC	CL8'VACC'	instruction name
00003170	000031D8			2219+	DC	A(RE56+16)	address of v2 source
00003174	000031E8			2220+	DC	A(RE56+32)	address of v3 source
00003178	00000010			2221+	DC	A(16)	result length
0000317C	000031C8			2222+REA56	DC	A(RE56)	result address
00003180	00000000 00000000			2223+	DS	FD	gap
00003188	00000000 00000000			2224+V1056	DS	XL16	V1 output
00003190	00000000 00000000						
00003198	00000000 00000000			2225+	DS	FD	gap
				2226+*			
000031A0				2227+X56	DS	0F	
000031A0	E310 5010 0014		00000010	2228+	LGF	R1,V2ADDR	load v2 source
000031A6	E761 0000 0806		00000000	2229+	VL	v22,0(R1)	use v22 to test decoder
000031AC	E310 5014 0014		00000014	2230+	LGF	R1,V3ADDR	load v3 source
000031B2	E771 0000 0806		00000000	2231+	VL	v23,0(R1)	use v23 to test decoder
000031B8	E766 7000 3EF1			2232+	VACC	V22,V22,V23,3	test instruction (dest is a source)
000031BE	E760 5028 080E		00003188	2233+	VST	V22,V1056	save v1 output
000031C4	07FB			2234+	BR	R11	return
000031C8				2235+RE56	DC	0F	xl16 expected result
000031C8				2236+	DROP	R5	
000031C8	00000000 00000000			2237	DC	XL16'0000000000000000 0000000000000001'	result
000031D0	00000000 00000001						
000031D8	01020304 05060708			2238	DC	XL16'0102030405060708 F90A0B0C0D0E0F00'	v2
000031E0	F90A0B0C 0D0E0F00						
000031E8	01020304 05060708			2239	DC	XL16'0102030405060708 F0FFFFFFFFFFFFFF'	v3
000031F0	F0FFFFFF FFFFFFFF						
				2240			
				2241	VRR_C VACC,3		
000031F8				2242+	DS	0FD	
000031F8		000031F8		2243+	USING *,R5		base for test data and test routine
000031F8	00003238			2244+T57	DC	A(X57)	address of test routine
000031FC	0039			2245+	DC	H'57'	test number
000031FE	00			2246+	DC	X'00'	
000031FF	03			2247+	DC	HL1'3'	m4
00003200	E5C1C3C3 40404040			2248+	DC	CL8'VACC'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003208	00003270			2249+	DC	A(RE57+16)	address of v2 source
0000320C	00003280			2250+	DC	A(RE57+32)	address of v3 source
00003210	00000010			2251+	DC	A(16)	result length
00003214	00003260			2252+REA57	DC	A(RE57)	result address
00003218	00000000 00000000			2253+	DS	FD	gap
00003220	00000000 00000000			2254+V1057	DS	XL16	V1 output
00003228	00000000 00000000						
00003230	00000000 00000000			2255+	DS	FD	gap
				2256+*			
00003238				2257+X57	DS	0F	
00003238	E310 5010 0014		00000010	2258+	LGF	R1,V2ADDR	load v2 source
0000323E	E761 0000 0806		00000000	2259+	VL	v22,0(R1)	use v22 to test decoder
00003244	E310 5014 0014		00000014	2260+	LGF	R1,V3ADDR	load v3 source
0000324A	E771 0000 0806		00000000	2261+	VL	v23,0(R1)	use v23 to test decoder
00003250	E766 7000 3EF1			2262+	VACC	V22,V22,V23,3	test instruction (dest is a source)
00003256	E760 5028 080E		00003220	2263+	VST	V22,V1057	save v1 output
0000325C	07FB			2264+	BR	R11	return
00003260				2265+RE57	DC	0F	xl16 expected result
00003260				2266+	DROP	R5	
00003260	00000000 00000001			2267	DC	XL16'0000000000000001 0000000000000000'	result
00003268	00000000 00000000						
00003270	A0FDFCFB FAF9F8F7			2268	DC	XL16'A0FDFCFBFAF9F8F7 090A0B0C0D0E0F00'	v2
00003278	090A0B0C 0D0E0F00						
00003280	A1020304 05060708			2269	DC	XL16'A102030405060708 00FDFCFBFAF9F8F7'	v3
00003288	00FDFCFB FAF9F8F7						
				2270			
				2271 *Quadword			
				2272	VRR_C	VACC,4	
00003290				2273+	DS	0FD	
00003290		00003290		2274+	USING	*,R5	base for test data and test routine
00003290	000032D0			2275+T58	DC	A(X58)	address of test routine
00003294	003A			2276+	DC	H'58'	test number
00003296	00			2277+	DC	X'00'	
00003297	04			2278+	DC	HL1'4'	m4
00003298	E5C1C3C3 40404040			2279+	DC	CL8'VACC'	instruction name
000032A0	00003308			2280+	DC	A(RE58+16)	address of v2 source
000032A4	00003318			2281+	DC	A(RE58+32)	address of v3 source
000032A8	00000010			2282+	DC	A(16)	result length
000032AC	000032F8			2283+REA58	DC	A(RE58)	result address
000032B0	00000000 00000000			2284+	DS	FD	gap
000032B8	00000000 00000000			2285+V1058	DS	XL16	V1 output
000032C0	00000000 00000000						
000032C8	00000000 00000000			2286+	DS	FD	gap
				2287+*			
000032D0				2288+X58	DS	0F	
000032D0	E310 5010 0014		00000010	2289+	LGF	R1,V2ADDR	load v2 source
000032D6	E761 0000 0806		00000000	2290+	VL	v22,0(R1)	use v22 to test decoder
000032DC	E310 5014 0014		00000014	2291+	LGF	R1,V3ADDR	load v3 source
000032E2	E771 0000 0806		00000000	2292+	VL	v23,0(R1)	use v23 to test decoder
000032E8	E766 7000 4EF1			2293+	VACC	V22,V22,V23,4	test instruction (dest is a source)
000032EE	E760 5028 080E		000032B8	2294+	VST	V22,V1058	save v1 output
000032F4	07FB			2295+	BR	R11	return
000032F8				2296+RE58	DC	0F	xl16 expected result
000032F8				2297+	DROP	R5	
000032F8	00000000 00000000			2298	DC	XL16'0000000000000000 0000000000000001'	result
00003300	00000000 00000001						

```
   LOC        OBJECT CODE      ADDR1    ADDR2    STMT

00003308  FFFFFFFF FFFFFFFF                     2299         DC    XL16'FFFFFFFFFFFFFFFF 0102030405060708'    v2
00003310  01020304 05060708
00003318  01020304 05060708                     2300         DC    XL16'0102030405060708 090A0B0C0D0E0F00'    v3
00003320  090A0B0C 0D0E0F00
                                                2301
                                                2302         VRR_C VACC, 4
00003328                                        2303+        DS    0FD
00003328                        00003328        2304+        USING *, R5                    base for test data and test routine
00003328  00003368                              2305+T59     DC    A(X59)                    address of test routine
0000332C  003B                                  2306+        DC    H'59'                     test number
0000332E  00                                    2307+        DC    X'00'
0000332F  04                                    2308+        DC    HL1'4'                    m4
00003330  E5C1C3C3 40404040                     2309+        DC    CL8'VACC'                 instruction name
00003338  000033A0                              2310+        DC    A(RE59+16)                address of v2 source
0000333C  000033B0                              2311+        DC    A(RE59+32)                address of v3 source
00003340  00000010                              2312+        DC    A(16)                     result length
00003344  00003390                              2313+REA59   DC    A(RE59)                   result address
00003348  00000000 00000000                     2314+        DS    FD                        gap
00003350  00000000 00000000                     2315+V1059   DS    XL16                      V1 output
00003358  00000000 00000000
00003360  00000000 00000000                     2316+        DS    FD                        gap
                                                2317+*
00003368                                        2318+X59     DS    0F
00003368  E310 5010 0014              00000010  2319+        LGF   R1, V2ADDR                load v2 source
0000336E  E761 0000 0806              00000000  2320+        VL    v22, 0(R1)                use v22 to test decoder
00003374  E310 5014 0014              00000014  2321+        LGF   R1, V3ADDR                load v3 source
0000337A  E771 0000 0806              00000000  2322+        VL    v23, 0(R1)                use v23 to test decoder
00003380  E766 7000 4EF1                        2323+        VACC  V22, V22, V23, 4            test instruction (dest is a source)
00003386  E760 5028 080E              00003350  2324+        VST   V22, V1059                  save v1 output
0000338C  07FB                                  2325+        BR    R11                       return
00003390                                        2326+RE59    DC    0F                        xl16 expected result
00003390                                        2327+        DROP  R5
00003390  00000000 00000000                     2328         DC    XL16'0000000000000000 0000000000000000'    result
00003398  00000000 00000000
000033A0  01020304 05060708                     2329         DC    XL16'0102030405060708 F90A0B0C0D0E0F00'    v2
000033A8  F90A0B0C 0D0E0F00
000033B0  01020304 05060708                     2330         DC    XL16'0102030405060708 F0FFFFFFFFFFFFFF'    v3
000033B8  F0FFFFFF FFFFFFFF
                                                2331
                                                2332         VRR_C VACC, 4
000033C0                                        2333+        DS    0FD
000033C0                        000033C0        2334+        USING *, R5                    base for test data and test routine
000033C0  00003400                              2335+T60     DC    A(X60)                    address of test routine
000033C4  003C                                  2336+        DC    H'60'                     test number
000033C6  00                                    2337+        DC    X'00'
000033C7  04                                    2338+        DC    HL1'4'                    m4
000033C8  E5C1C3C3 40404040                     2339+        DC    CL8'VACC'                 instruction name
000033D0  00003438                              2340+        DC    A(RE60+16)                address of v2 source
000033D4  00003448                              2341+        DC    A(RE60+32)                address of v3 source
000033D8  00000010                              2342+        DC    A(16)                     result length
000033DC  00003428                              2343+REA60   DC    A(RE60)                   result address
000033E0  00000000 00000000                     2344+        DS    FD                        gap
000033E8  00000000 00000000                     2345+V1060   DS    XL16                      V1 output
000033F0  00000000 00000000
000033F8  00000000 00000000                     2346+        DS    FD                        gap
                                                2347+*
```

```
  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

  00003400                                          2348+X60     DS      0F
  00003400  E310 5010 0014                00000010  2349+        LGF     R1,V2ADDR       load v2 source
  00003406  E761 0000 0806                00000000  2350+        VL      v22,0(R1)       use v22 to test decoder
  0000340C  E310 5014 0014                00000014  2351+        LGF     R1,V3ADDR       load v3 source
  00003412  E771 0000 0806                00000000  2352+        VL      v23,0(R1)       use v23 to test decoder
  00003418  E766 7000 4EF1                          2353+        VACC    V22,V22,V23,4    test instruction (dest is a source)
  0000341E  E760 5028 080E                000033E8  2354+        VST     V22,V1060       save v1 output
  00003424  07FB                                    2355+        BR      R11             return
  00003428                                          2356+RE60    DC      0F              xl16 expected result
  00003428                                          2357+        DROP    R5
  00003428  00000000 00000000                       2358         DC      XL16'0000000000000000 0000000000000001'     result
  00003430  00000000 00000001
  00003438  A0FDFCFB FAF9F8F7                        2359         DC      XL16'A0FDFCFBFAF9F8F7 090A0B0C0D0E0F00'     v2
  00003440  090A0B0C 0D0E0F00
  00003448  A1020304 05060708                        2360         DC      XL16'A102030405060708 00FDFCFBFAF9F8F7'     v3
  00003450  00FDFCFB FAF9F8F7
                                                    2361
                                                    2362
                                                    2363
  00003458  00000000                                2364         DC      F'0'        END OF TABLE
  0000345C  00000000                                2365         DC      F'0'
                                                    2366 *
                                                    2367 * table of pointers to individual load test
                                                    2368 *
  00003460                                          2369 E7TESTS DS      0F
                                                    2370         PTTABLE
  00003460                                          2371+TTABLE  DS      0F
  00003460  000010B8                                2372+        DC      A(T1)
  00003464  00001150                                2373+        DC      A(T2)
  00003468  000011E8                                2374+        DC      A(T3)
  0000346C  00001280                                2375+        DC      A(T4)
  00003470  00001318                                2376+        DC      A(T5)
  00003474  000013B0                                2377+        DC      A(T6)
  00003478  00001448                                2378+        DC      A(T7)
  0000347C  000014E0                                2379+        DC      A(T8)
  00003480  00001578                                2380+        DC      A(T9)
  00003484  00001610                                2381+        DC      A(T10)
  00003488  000016A8                                2382+        DC      A(T11)
  0000348C  00001740                                2383+        DC      A(T12)
  00003490  000017D8                                2384+        DC      A(T13)
  00003494  00001870                                2385+        DC      A(T14)
  00003498  00001908                                2386+        DC      A(T15)
  0000349C  000019A0                                2387+        DC      A(T16)
  000034A0  00001A38                                2388+        DC      A(T17)
  000034A4  00001AD0                                2389+        DC      A(T18)
  000034A8  00001B68                                2390+        DC      A(T19)
  000034AC  00001C00                                2391+        DC      A(T20)
  000034B0  00001C98                                2392+        DC      A(T21)
  000034B4  00001D30                                2393+        DC      A(T22)
  000034B8  00001DC8                                2394+        DC      A(T23)
  000034BC  00001E60                                2395+        DC      A(T24)
  000034C0  00001EF8                                2396+        DC      A(T25)
  000034C4  00001F90                                2397+        DC      A(T26)
  000034C8  00002028                                2398+        DC      A(T27)
  000034CC  000020C0                                2399+        DC      A(T28)
  000034D0  00002158                                2400+        DC      A(T29)
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000034D4	000021F0			2401+	DC	A(T30)
000034D8	00002288			2402+	DC	A(T31)
000034DC	00002320			2403+	DC	A(T32)
000034E0	000023B8			2404+	DC	A(T33)
000034E4	00002450			2405+	DC	A(T34)
000034E8	000024E8			2406+	DC	A(T35)
000034EC	00002580			2407+	DC	A(T36)
000034F0	00002618			2408+	DC	A(T37)
000034F4	000026B0			2409+	DC	A(T38)
000034F8	00002748			2410+	DC	A(T39)
000034FC	000027E0			2411+	DC	A(T40)
00003500	00002878			2412+	DC	A(T41)
00003504	00002910			2413+	DC	A(T42)
00003508	000029A8			2414+	DC	A(T43)
0000350C	00002A40			2415+	DC	A(T44)
00003510	00002AD8			2416+	DC	A(T45)
00003514	00002B70			2417+	DC	A(T46)
00003518	00002C08			2418+	DC	A(T47)
0000351C	00002CA0			2419+	DC	A(T48)
00003520	00002D38			2420+	DC	A(T49)
00003524	00002DD0			2421+	DC	A(T50)
00003528	00002E68			2422+	DC	A(T51)
0000352C	00002F00			2423+	DC	A(T52)
00003530	00002F98			2424+	DC	A(T53)
00003534	00003030			2425+	DC	A(T54)
00003538	000030C8			2426+	DC	A(T55)
0000353C	00003160			2427+	DC	A(T56)
00003540	000031F8			2428+	DC	A(T57)
00003544	00003290			2429+	DC	A(T58)
00003548	00003328			2430+	DC	A(T59)
0000354C	000033C0			2431+	DC	A(T60)
				2432+*		
00003550	00000000			2433+	DC	A(0) END OF TABLE
00003554	00000000			2434+	DC	A(0)
				2435		
00003558	00000000			2436	DC	F'0' END OF TABLE
0000355C	00000000			2437	DC	F'0'

```
   LOC        OBJECT CODE      ADDR1      ADDR2     STMT
```

```
                                                   2439 ****************************************************************************
                                                   2440 *           Register equates
                                                   2441 ****************************************************************************

                                00000000   00000001 2443 R0        EQU   0
                                00000001   00000001 2444 R1        EQU   1
                                00000002   00000001 2445 R2        EQU   2
                                00000003   00000001 2446 R3        EQU   3
                                00000004   00000001 2447 R4        EQU   4
                                00000005   00000001 2448 R5        EQU   5
                                00000006   00000001 2449 R6        EQU   6
                                00000007   00000001 2450 R7        EQU   7
                                00000008   00000001 2451 R8        EQU   8
                                00000009   00000001 2452 R9        EQU   9
                                0000000A   00000001 2453 R10       EQU   10
                                0000000B   00000001 2454 R11       EQU   11
                                0000000C   00000001 2455 R12       EQU   12
                                0000000D   00000001 2456 R13       EQU   13
                                0000000E   00000001 2457 R14       EQU   14
                                0000000F   00000001 2458 R15       EQU   15




                                                   2460 ****************************************************************************
                                                   2461 *           Register equates
                                                   2462 ****************************************************************************

                                00000000   00000001 2464 V0        EQU   0
                                00000001   00000001 2465 V1        EQU   1
                                00000002   00000001 2466 V2        EQU   2
                                00000003   00000001 2467 V3        EQU   3
                                00000004   00000001 2468 V4        EQU   4
                                00000005   00000001 2469 V5        EQU   5
                                00000006   00000001 2470 V6        EQU   6
                                00000007   00000001 2471 V7        EQU   7
                                00000008   00000001 2472 V8        EQU   8
                                00000009   00000001 2473 V9        EQU   9
                                0000000A   00000001 2474 V10       EQU   10
                                0000000B   00000001 2475 V11       EQU   11
                                0000000C   00000001 2476 V12       EQU   12
                                0000000D   00000001 2477 V13       EQU   13
                                0000000E   00000001 2478 V14       EQU   14
                                0000000F   00000001 2479 V15       EQU   15
                                00000010   00000001 2480 V16       EQU   16
                                00000011   00000001 2481 V17       EQU   17
                                00000012   00000001 2482 V18       EQU   18
                                00000013   00000001 2483 V19       EQU   19
                                00000014   00000001 2484 V20       EQU   20
                                00000015   00000001 2485 V21       EQU   21
```

```
 LOC        OBJECT CODE      ADDR1      ADDR2     STMT

                         00000016   00000001   2486 V22        EQU    22
                         00000017   00000001   2487 V23        EQU    23
                         00000018   00000001   2488 V24        EQU    24
                         00000019   00000001   2489 V25        EQU    25
                         0000001A   00000001   2490 V26        EQU    26
                         0000001B   00000001   2491 V27        EQU    27
                         0000001C   00000001   2492 V28        EQU    28
                         0000001D   00000001   2493 V29        EQU    29
                         0000001E   00000001   2494 V30        EQU    30
                         0000001F   00000001   2495 V31        EQU    31
                                               2496
                                               2497            END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES											
BEGIN	I	00000200	2	158	124	154	155	156								
CTLR0	F	0000048C	4	354	168	169	170	171								
DECNUM	C	00001073	16	405	268	270	276	278								
E7TEST	4	00000000	64	419	217											
E7TESTS	F	00003460	4	2369	210											
EDIT	X	00001047	18	400	269	277										
ENDTEST	U	0000031E	1	254	215											
EOJ	I	00000470	4	344	203	257										
EOJPSW	D	00000460	8	342	344											
FAILCONT	U	0000030E	1	244												
FAILED	F	00001000	4	382	246	255										
FAILMSG	U	0000030A	1	238	228											
FAILPSW	D	00000478	8	346	348											
FAILTEST	I	00000488	4	348	258											
FB0001	F	00000280	8	187	191	192	194									
IMAGE	1	00000000	13664	0												
K	U	00000400	1	366	367	368	369									
K64	U	00010000	1	368												
M4	U	00000007	1	423	275											
MB	U	00100000	1	369												
MSG	I	000003A8	4	304	202	287										
MSGCMD	C	000003F6	9	334	317	318										
MSGMSG	C	000003FF	95	335	311	332	309									
MSGMVC	I	000003F0	6	332	315											
MSGOK	I	000003BE	2	313	310											
MSGRET	I	000003DE	4	328	321	324										
MSGSAVE	F	000003E4	4	331	307	328										
NEXTE7	U	000002D4	1	212	231	249										
OPNAME	C	00000008	8	425	273											
PAGE	U	00001000	1	367												
PRT3	C	0000105D	18	403	269	270	271	277	278	279						
PRTLINE	C	00001008	16	388	395	286										
PRTLNG	U	0000003F	1	395	285											
PRTM4	C	00001044	2	393	279											
PRTNAME	C	00001033	8	391	273											
PRTNUM	C	00001018	3	389	271											
R0	U	00000000	1	2443	118	168	171	191	193	194	195	200	219	220	245	246	284
					285	288	304	307	309	311	313	328				
R1	U	00000001	1	2444	201	226	227	255	256	286	318	332	550	551	552	553	580
					581	582	583	610	611	612	613	641	642	643	644	671	672
					673	674	701	702	703	704	732	733	734	735	762	763	764
					765	792	793	794	795	823	824	825	826	853	854	855	856
					883	884	885	886	914	915	916	917	944	945	946	947	974
					975	976	977	1008	1009	1010	1011	1038	1039	1040	1041	1068	1069
					1070	1071	1099	1100	1101	1102	1129	1130	1131	1132	1159	1160	1161
					1162	1190	1191	1192	1193	1220	1221	1222	1223	1250	1251	1252	1253
					1281	1282	1283	1284	1311	1312	1313	1314	1341	1342	1343	1344	1372
					1373	1374	1375	1402	1403	1404	1405	1432	1433	1434	1435	1466	1467
					1468	1469	1496	1497	1498	1499	1526	1527	1528	1529	1557	1558	1559
					1560	1587	1588	1589	1590	1617	1618	1619	1620	1648	1649	1650	1651
					1678	1679	1680	1681	1708	1709	1710	1711	1739	1740	1741	1742	1769
					1770	1771	1772	1799	1800	1801	1802	1830	1831	1832	1833	1860	1861
					1862	1863	1890	1891	1892	1893	1925	1926	1927	1928	1955	1956	1957
					1958	1985	1986	1987	1988	2016	2017	2018	2019	2046	2047	2048	2049
					2076	2077	2078	2079	2107	2108	2109	2110	2137	2138	2139	2140	2167
					2168	2169	2170	2198	2199	2200	2201	2228	2229	2230	2231	2258	2259

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					2260	2261	2289	2290	2291	2292	2319	2320	2321	2322	2349	2350	2351
					2352												
R10	U	0000000A	1	2453	156	165	166										
R11	U	0000000B	1	2454	223	224	556	586	616	647	677	707	738	768	798	829	859
					889	920	950	980	1014	1044	1074	1105	1135	1165	1196	1226	1256
					1287	1317	1347	1378	1408	1438	1472	1502	1532	1563	1593	1623	1654
					1684	1714	1745	1775	1805	1836	1866	1896	1931	1961	1991	2022	2052
					2082	2113	2143	2173	2204	2234	2264	2295	2325	2355			
R12	U	0000000C	1	2455	210	213	230	248									
R13	U	0000000D	1	2456													
R14	U	0000000E	1	2457													
R15	U	0000000F	1	2458	239	264	291	292									
R2	U	00000002	1	2445	202	267	268	275	276	284	287	288	305	307	313	314	315
					317	323	328	329									
R3	U	00000003	1	2446													
R4	U	00000004	1	2447													
R5	U	00000005	1	2448	213	214	217	265	290	535	558	565	588	595	618	626	649
					656	679	686	709	717	740	747	770	777	800	808	831	838
					861	868	891	899	922	929	952	959	982	993	1016	1023	1046
					1053	1076	1084	1107	1114	1137	1144	1167	1175	1198	1205	1228	1235
					1258	1266	1289	1296	1319	1326	1349	1357	1380	1387	1410	1417	1440
					1451	1474	1481	1504	1511	1534	1542	1565	1572	1595	1602	1625	1633
					1656	1663	1686	1693	1716	1724	1747	1754	1777	1784	1807	1815	1838
					1845	1868	1875	1898	1910	1933	1940	1963	1970	1993	2001	2024	2031
					2054	2061	2084	2092	2115	2122	2145	2152	2175	2183	2206	2213	2236
					2243	2266	2274	2297	2304	2327	2334	2357					
R6	U	00000006	1	2449													
R7	U	00000007	1	2450													
R8	U	00000008	1	2451	154	158	159	160	162								
R9	U	00000009	1	2452	155	162	163	165									
RE1	F	00001120	4	557	541	542	544										
RE10	F	00001678	4	830	814	815	817										
RE11	F	00001710	4	860	844	845	847										
RE12	F	000017A8	4	890	874	875	877										
RE13	F	00001840	4	921	905	906	908										
RE14	F	000018D8	4	951	935	936	938										
RE15	F	00001970	4	981	965	966	968										
RE16	F	00001A08	4	1015	999	1000	1002										
RE17	F	00001AA0	4	1045	1029	1030	1032										
RE18	F	00001B38	4	1075	1059	1060	1062										
RE19	F	00001BD0	4	1106	1090	1091	1093										
RE2	F	000011B8	4	587	571	572	574										
RE20	F	00001C68	4	1136	1120	1121	1123										
RE21	F	00001D00	4	1166	1150	1151	1153										
RE22	F	00001D98	4	1197	1181	1182	1184										
RE23	F	00001E30	4	1227	1211	1212	1214										
RE24	F	00001EC8	4	1257	1241	1242	1244										
RE25	F	00001F60	4	1288	1272	1273	1275										
RE26	F	00001FF8	4	1318	1302	1303	1305										
RE27	F	00002090	4	1348	1332	1333	1335										
RE28	F	00002128	4	1379	1363	1364	1366										
RE29	F	000021C0	4	1409	1393	1394	1396										
RE3	F	00001250	4	617	601	602	604										
RE30	F	00002258	4	1439	1423	1424	1426										
RE31	F	000022F0	4	1473	1457	1458	1460										
RE32	F	00002388	4	1503	1487	1488	1490										

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
RE33	F	00002420	4	1533	1517	1518	1520
RE34	F	000024B8	4	1564	1548	1549	1551
RE35	F	00002550	4	1594	1578	1579	1581
RE36	F	000025E8	4	1624	1608	1609	1611
RE37	F	00002680	4	1655	1639	1640	1642
RE38	F	00002718	4	1685	1669	1670	1672
RE39	F	000027B0	4	1715	1699	1700	1702
RE4	F	000012E8	4	648	632	633	635
RE40	F	00002848	4	1746	1730	1731	1733
RE41	F	000028E0	4	1776	1760	1761	1763
RE42	F	00002978	4	1806	1790	1791	1793
RE43	F	00002A10	4	1837	1821	1822	1824
RE44	F	00002AA8	4	1867	1851	1852	1854
RE45	F	00002B40	4	1897	1881	1882	1884
RE46	F	00002BD8	4	1932	1916	1917	1919
RE47	F	00002C70	4	1962	1946	1947	1949
RE48	F	00002D08	4	1992	1976	1977	1979
RE49	F	00002DA0	4	2023	2007	2008	2010
RE5	F	00001380	4	678	662	663	665
RE50	F	00002E38	4	2053	2037	2038	2040
RE51	F	00002ED0	4	2083	2067	2068	2070
RE52	F	00002F68	4	2114	2098	2099	2101
RE53	F	00003000	4	2144	2128	2129	2131
RE54	F	00003098	4	2174	2158	2159	2161
RE55	F	00003130	4	2205	2189	2190	2192
RE56	F	000031C8	4	2235	2219	2220	2222
RE57	F	00003260	4	2265	2249	2250	2252
RE58	F	000032F8	4	2296	2280	2281	2283
RE59	F	00003390	4	2326	2310	2311	2313
RE6	F	00001418	4	708	692	693	695
RE60	F	00003428	4	2356	2340	2341	2343
RE7	F	000014B0	4	739	723	724	726
RE8	F	00001548	4	769	753	754	756
RE9	F	000015E0	4	799	783	784	786
REA1	A	000010D4	4	544			
REA10	A	0000162C	4	817			
REA11	A	000016C4	4	847			
REA12	A	0000175C	4	877			
REA13	A	000017F4	4	908			
REA14	A	0000188C	4	938			
REA15	A	00001924	4	968			
REA16	A	000019BC	4	1002			
REA17	A	00001A54	4	1032			
REA18	A	00001AEC	4	1062			
REA19	A	00001B84	4	1093			
REA2	A	0000116C	4	574			
REA20	A	00001C1C	4	1123			
REA21	A	00001CB4	4	1153			
REA22	A	00001D4C	4	1184			
REA23	A	00001DE4	4	1214			
REA24	A	00001E7C	4	1244			
REA25	A	00001F14	4	1275			
REA26	A	00001FAC	4	1305			
REA27	A	00002044	4	1335			
REA28	A	000020DC	4	1366			
REA29	A	00002174	4	1396			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA3	A	00001204	4	604		
REA30	A	0000220C	4	1426		
REA31	A	000022A4	4	1460		
REA32	A	0000233C	4	1490		
REA33	A	000023D4	4	1520		
REA34	A	0000246C	4	1551		
REA35	A	00002504	4	1581		
REA36	A	0000259C	4	1611		
REA37	A	00002634	4	1642		
REA38	A	000026CC	4	1672		
REA39	A	00002764	4	1702		
REA4	A	0000129C	4	635		
REA40	A	000027FC	4	1733		
REA41	A	00002894	4	1763		
REA42	A	0000292C	4	1793		
REA43	A	000029C4	4	1824		
REA44	A	00002A5C	4	1854		
REA45	A	00002AF4	4	1884		
REA46	A	00002B8C	4	1919		
REA47	A	00002C24	4	1949		
REA48	A	00002CBC	4	1979		
REA49	A	00002D54	4	2010		
REA5	A	00001334	4	665		
REA50	A	00002DEC	4	2040		
REA51	A	00002E84	4	2070		
REA52	A	00002F1C	4	2101		
REA53	A	00002FB4	4	2131		
REA54	A	0000304C	4	2161		
REA55	A	000030E4	4	2192		
REA56	A	0000317C	4	2222		
REA57	A	00003214	4	2252		
REA58	A	000032AC	4	2283		
REA59	A	00003344	4	2313		
REA6	A	000013CC	4	695		
REA60	A	000033DC	4	2343		
REA7	A	00001464	4	726		
REA8	A	000014FC	4	756		
REA9	A	00001594	4	786		
READDR	A	0000001C	4	429	226	
REG2LOW	U	000000DD	1	372		
REG2PATT	U	AABBCCDD	1	371		
RELEN	A	00000018	4	428		
RPTDWSAV	D	00000398	8	297	284	288
RPTERROR	I	0000032C	4	264	239	
RPTSAVE	F	00000390	4	294	264	291
RPTSVR5	F	00000394	4	295	265	290
SKL0001	U	0000004E	1	184	200	
SKT0001	C	0000022A	20	181	184	201
SVOLDPSW	U	00000140	0	120		
T1	A	000010B8	4	536	2372	
T10	A	00001610	4	809	2381	
T11	A	000016A8	4	839	2382	
T12	A	00001740	4	869	2383	
T13	A	000017D8	4	900	2384	
T14	A	00001870	4	930	2385	
T15	A	00001908	4	960	2386	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
T16	A	000019A0	4	994	2387	
T17	A	00001A38	4	1024	2388	
T18	A	00001AD0	4	1054	2389	
T19	A	00001B68	4	1085	2390	
T2	A	00001150	4	566	2373	
T20	A	00001C00	4	1115	2391	
T21	A	00001C98	4	1145	2392	
T22	A	00001D30	4	1176	2393	
T23	A	00001DC8	4	1206	2394	
T24	A	00001E60	4	1236	2395	
T25	A	00001EF8	4	1267	2396	
T26	A	00001F90	4	1297	2397	
T27	A	00002028	4	1327	2398	
T28	A	000020C0	4	1358	2399	
T29	A	00002158	4	1388	2400	
T3	A	000011E8	4	596	2374	
T30	A	000021F0	4	1418	2401	
T31	A	00002288	4	1452	2402	
T32	A	00002320	4	1482	2403	
T33	A	000023B8	4	1512	2404	
T34	A	00002450	4	1543	2405	
T35	A	000024E8	4	1573	2406	
T36	A	00002580	4	1603	2407	
T37	A	00002618	4	1634	2408	
T38	A	000026B0	4	1664	2409	
T39	A	00002748	4	1694	2410	
T4	A	00001280	4	627	2375	
T40	A	000027E0	4	1725	2411	
T41	A	00002878	4	1755	2412	
T42	A	00002910	4	1785	2413	
T43	A	000029A8	4	1816	2414	
T44	A	00002A40	4	1846	2415	
T45	A	00002AD8	4	1876	2416	
T46	A	00002B70	4	1911	2417	
T47	A	00002C08	4	1941	2418	
T48	A	00002CA0	4	1971	2419	
T49	A	00002D38	4	2002	2420	
T5	A	00001318	4	657	2376	
T50	A	00002DD0	4	2032	2421	
T51	A	00002E68	4	2062	2422	
T52	A	00002F00	4	2093	2423	
T53	A	00002F98	4	2123	2424	
T54	A	00003030	4	2153	2425	
T55	A	000030C8	4	2184	2426	
T56	A	00003160	4	2214	2427	
T57	A	000031F8	4	2244	2428	
T58	A	00003290	4	2275	2429	
T59	A	00003328	4	2305	2430	
T6	A	000013B0	4	687	2377	
T60	A	000033C0	4	2335	2431	
T7	A	00001448	4	718	2378	
T8	A	000014E0	4	748	2379	
T9	A	00001578	4	778	2380	
TESTING	F	00001004	4	383	220	
TNUM	H	00000004	2	421	219	267
TSUB	A	00000000	4	420	223	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
TTABLE	F	00003460	4	2371	
V0	U	00000000	1	2464	
V1	U	00000001	1	2465	222
V10	U	0000000A	1	2474	
V11	U	0000000B	1	2475	
V12	U	0000000C	1	2476	
V13	U	0000000D	1	2477	
V14	U	0000000E	1	2478	
V15	U	0000000F	1	2479	
V16	U	00000010	1	2480	
V17	U	00000011	1	2481	
V18	U	00000012	1	2482	
V19	U	00000013	1	2483	
V1FUDGE	X	00001094	16	412	222
V101	X	000010E0	16	546	555
V1010	X	00001638	16	819	828
V1011	X	000016D0	16	849	858
V1012	X	00001768	16	879	888
V1013	X	00001800	16	910	919
V1014	X	00001898	16	940	949
V1015	X	00001930	16	970	979
V1016	X	000019C8	16	1004	1013
V1017	X	00001A60	16	1034	1043
V1018	X	00001AF8	16	1064	1073
V1019	X	00001B90	16	1095	1104
V102	X	00001178	16	576	585
V1020	X	00001C28	16	1125	1134
V1021	X	00001CC0	16	1155	1164
V1022	X	00001D58	16	1186	1195
V1023	X	00001DF0	16	1216	1225
V1024	X	00001E88	16	1246	1255
V1025	X	00001F20	16	1277	1286
V1026	X	00001FB8	16	1307	1316
V1027	X	00002050	16	1337	1346
V1028	X	000020E8	16	1368	1377
V1029	X	00002180	16	1398	1407
V103	X	00001210	16	606	615
V1030	X	00002218	16	1428	1437
V1031	X	000022B0	16	1462	1471
V1032	X	00002348	16	1492	1501
V1033	X	000023E0	16	1522	1531
V1034	X	00002478	16	1553	1562
V1035	X	00002510	16	1583	1592
V1036	X	000025A8	16	1613	1622
V1037	X	00002640	16	1644	1653
V1038	X	000026D8	16	1674	1683
V1039	X	00002770	16	1704	1713
V104	X	000012A8	16	637	646
V1040	X	00002808	16	1735	1744
V1041	X	000028A0	16	1765	1774
V1042	X	00002938	16	1795	1804
V1043	X	000029D0	16	1826	1835
V1044	X	00002A68	16	1856	1865
V1045	X	00002B00	16	1886	1895
V1046	X	00002B98	16	1921	1930
V1047	X	00002C30	16	1951	1960

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1048	X	00002CC8	16	1981	1990
V1049	X	00002D60	16	2012	2021
V105	X	00001340	16	667	676
V1050	X	00002DF8	16	2042	2051
V1051	X	00002E90	16	2072	2081
V1052	X	00002F28	16	2103	2112
V1053	X	00002FC0	16	2133	2142
V1054	X	00003058	16	2163	2172
V1055	X	000030F0	16	2194	2203
V1056	X	00003188	16	2224	2233
V1057	X	00003220	16	2254	2263
V1058	X	000032B8	16	2285	2294
V1059	X	00003350	16	2315	2324
V106	X	000013D8	16	697	706
V1060	X	000033E8	16	2345	2354
V107	X	00001470	16	728	737
V108	X	00001508	16	758	767
V109	X	000015A0	16	788	797
V10UTPUT	X	00000028	16	431	227
V2	U	00000002	1	2466	
V20	U	00000014	1	2484	
V21	U	00000015	1	2485	

V22   U   00000016   1   2486

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 551  554  555  581  584  585  611  614  615  642  645  646  672
 675  676  702  705  706  733  736  737  763  766  767  793  796
 797  824  827  828  854  857  858  884  887  888  915  918  919
 945  948  949  975  978  979 1009 1012 1013 1039 1042 1043 1069
1072 1073 1100 1103 1104 1130 1133 1134 1160 1163 1164 1191 1194
1195 1221 1224 1225 1251 1254 1255 1282 1285 1286 1312 1315 1316
1342 1345 1346 1373 1376 1377 1403 1406 1407 1433 1436 1437 1467
1470 1471 1497 1500 1501 1527 1530 1531 1558 1561 1562 1588 1591
1592 1618 1621 1622 1649 1652 1653 1679 1682 1683 1709 1712 1713
1740 1743 1744 1770 1773 1774 1800 1803 1804 1831 1834 1835 1861
1864 1865 1891 1894 1895 1926 1929 1930 1956 1959 1960 1986 1989
1990 2017 2020 2021 2047 2050 2051 2077 2080 2081 2108 2111 2112
2138 2141 2142 2168 2171 2172 2199 2202 2203 2229 2232 2233 2259
2262 2263 2290 2293 2294 2320 2323 2324 2350 2353 2354
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V23   U   00000017   1   2487

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 736  765  766  795  796  826  827  856  857  886  887  917  918
 947  948  977  978 1011 1012 1041 1042 1071 1072 1102 1103 1132
1133 1162 1163 1193 1194 1223 1224 1253 1254 1284 1285 1314 1315
1344 1345 1375 1376 1405 1406 1435 1436 1469 1470 1499 1500 1529
1530 1560 1561 1590 1591 1620 1621 1651 1652 1681 1682 1711 1712
1742 1743 1772 1773 1802 1803 1833 1834 1863 1864 1893 1894 1928
1929 1958 1959 1988 1989 2019 2020 2049 2050 2079 2080 2110 2111
2140 2141 2170 2171 2201 2202 2231 2232 2261 2262 2292 2293 2322
2323 2352 2353
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V24	U	00000018	1	2488	
V25	U	00000019	1	2489	
V26	U	0000001A	1	2490	
V27	U	0000001B	1	2491	
V28	U	0000001C	1	2492	
V29	U	0000001D	1	2493	

V2ADDR   A   00000010   4   426

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 550  580  610  641  671  701  732  762  792  823  853  883  914
 944  974 1008 1038 1068 1099 1129 1159 1190 1220 1250 1281 1311
1341 1372 1402 1432 1466 1496 1526 1557 1587 1617 1648 1678 1708
1739 1769 1799 1830 1860 1890 1925 1955 1985 2016 2046 2076 2107
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					2137	2167	2198	2228	2258	2289	2319	2349					
V3	U	00000003	1	2467													
V30	U	0000001E	1	2494													
V31	U	0000001F	1	2495													
V3ADDR	A	00000014	4	427	552	582	612	643	673	703	734	764	794	825	855	885	916
					946	976	1010	1040	1070	1101	1131	1161	1192	1222	1252	1283	1313
					1343	1374	1404	1434	1468	1498	1528	1559	1589	1619	1650	1680	1710
					1741	1771	1801	1832	1862	1892	1927	1957	1987	2018	2048	2078	2109
					2139	2169	2200	2230	2260	2291	2321	2351					
V4	U	00000004	1	2468													
V5	U	00000005	1	2469													
V6	U	00000006	1	2470													
V7	U	00000007	1	2471													
V8	U	00000008	1	2472													
V9	U	00000009	1	2473													
X0001	U	000002A8	1	190	178	191											
X1	F	000010F8	4	549	536												
X10	F	00001650	4	822	809												
X11	F	000016E8	4	852	839												
X12	F	00001780	4	882	869												
X13	F	00001818	4	913	900												
X14	F	000018B0	4	943	930												
X15	F	00001948	4	973	960												
X16	F	000019E0	4	1007	994												
X17	F	00001A78	4	1037	1024												
X18	F	00001B10	4	1067	1054												
X19	F	00001BA8	4	1098	1085												
X2	F	00001190	4	579	566												
X20	F	00001C40	4	1128	1115												
X21	F	00001CD8	4	1158	1145												
X22	F	00001D70	4	1189	1176												
X23	F	00001E08	4	1219	1206												
X24	F	00001EA0	4	1249	1236												
X25	F	00001F38	4	1280	1267												
X26	F	00001FD0	4	1310	1297												
X27	F	00002068	4	1340	1327												
X28	F	00002100	4	1371	1358												
X29	F	00002198	4	1401	1388												
X3	F	00001228	4	609	596												
X30	F	00002230	4	1431	1418												
X31	F	000022C8	4	1465	1452												
X32	F	00002360	4	1495	1482												
X33	F	000023F8	4	1525	1512												
X34	F	00002490	4	1556	1543												
X35	F	00002528	4	1586	1573												
X36	F	000025C0	4	1616	1603												
X37	F	00002658	4	1647	1634												
X38	F	000026F0	4	1677	1664												
X39	F	00002788	4	1707	1694												
X4	F	000012C0	4	640	627												
X40	F	00002820	4	1738	1725												
X41	F	000028B8	4	1768	1755												
X42	F	00002950	4	1798	1785												
X43	F	000029E8	4	1829	1816												
X44	F	00002A80	4	1859	1846												
X45	F	00002B18	4	1889	1876												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
X46	F	00002BB0	4	1924	1911				
X47	F	00002C48	4	1954	1941				
X48	F	00002CE0	4	1984	1971				
X49	F	00002D78	4	2015	2002				
X5	F	00001358	4	670	657				
X50	F	00002E10	4	2045	2032				
X51	F	00002EA8	4	2075	2062				
X52	F	00002F40	4	2106	2093				
X53	F	00002FD8	4	2136	2123				
X54	F	00003070	4	2166	2153				
X55	F	00003108	4	2197	2184				
X56	F	000031A0	4	2227	2214				
X57	F	00003238	4	2257	2244				
X58	F	000032D0	4	2288	2275				
X59	F	00003368	4	2318	2305				
X6	F	000013F0	4	700	687				
X60	F	00003400	4	2348	2335				
X7	F	00001488	4	731	718				
X8	F	00001520	4	761	748				
X9	F	000015B8	4	791	778				
XC0001	U	000002D0	1	204	196				
ZVE7TST	J	00000000	13664	117	120	122	126	130	381	118
=A(E7TESTS)	A	00000498	4	359	210				
=AL2(L'MSGMSG)	R	000004A2	2	362	309				
=F'1'	F	0000049C	4	360	245				
=F'64'	F	00000494	4	358	195				
=H'0'	H	000004A0	2	361	304				

MACRO	DEFN	REFERENCES															
FCHECK	70	177															
PTTABLE	495	2370															
VRR_C	450	533	563	593	624	654	684	715	745	775	806	836	866	897	927	957	991	1021
		1051	1082	1112	1142	1173	1203	1233	1264	1294	1324	1355	1385	1415	1449	1479	1509	1540
		1570	1600	1631	1661	1691	1722	1752	1782	1813	1843	1873	1908	1938	1968	1999	2029	2059
		2090	2120	2150	2181	2211	2241	2272	2302	2332								

DESC	SYMBOL	SIZE	POS	ADDR

Entry: 0

Image	IMAGE	13664	0000-355F	0000-355F
Region		13664	0000-355F	0000-355F
CSECT	ZVE7TST	13664	0000-355F	0000-355F

STMT   FILE NAME

1   /home/tn529/sharedvfp/tests/zvector-e7-17-AddSub.asm

** NO ERRORS FOUND **