LOC	OBJECT CODE	ADDR1	ADDR2	STMT

```
  2 ***************************************************************************
  3 *
  4 *    Zvector E7 instruction tests for VRR-c encoded:
  5 *
  6 *    E768 VN      - Vector AND
  7 *    E769 VNC     - Vector AND with Complement
  8 *    E76A VO      - Vector OR
  9 *    E76B VNO     - Vector NOR
 10 *    E76C VNX     - Vector Not Exclusive OR
 11 *    E76D VX      - Vector Exclusive OR
 12 *    E76E VNN     - Vector NAND
 13 *    E76F VOC     - Vector OR with Complement
 14 *
 15 *         James Wekel March 2025
 16 ***************************************************************************

 18 ***************************************************************************
 19 *
 20 *         basic instruction tests
 21 *
 22 ***************************************************************************
 23 *   This program tests proper functioning of the z/arch E7 VRR-c vector
 24 *   logical (and, and with complement, or, nor, not xor, xor, nand)
 25 *   instructions.
 26 *
 27 *   Exceptions are not tested.
 28 *
 29 *   PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
 30 *   obvious coding errors.   None of the tests are thorough.   They are
 31 *   NOT designed to test all aspects of any of the instructions.
 32 *
 33 ***************************************************************************
 34 *
 35 *    *Testcase zvector-e7-11-logical
 36 *    *
 37 *    *    Zvector E7 instruction tests for VRR-c encoded:
 38 *    *
 39 *    *    E768 VN      - Vector AND
 40 *    *    E769 VNC     - Vector AND with Complement
 41 *    *    E76A VO      - Vector OR
 42 *    *    E76B VNO     - Vector NOR
 43 *    *    E76C VNX     - Vector Not Exclusive OR
 44 *    *    E76D VX      - Vector Exclusive OR
 45 *    *    E76E VNN     - Vector NAND
 46 *    *    E76F VOC     - Vector OR with Complement
 47 *    *
 48 *    *    # ----------------------------------------------------------------
 49 *    *    #  This tests only the basic function of the instructions.
 50 *    *    #  Exceptions are NOT tested.
 51 *    *    # ----------------------------------------------------------------
 52 *    *
 53 *    mainsize    2
 54 *    numcpu      1
 55 *    sysclear
 56 *    archlvl     z/Arch
```

```
    LOC          OBJECT CODE      ADDR1      ADDR2      STMT

                                                      57 *
                                                      58 *    loadcore     "$(testpath)/zvector-e7-11-logical.core" 0x0
                                                      59 *
                                                      60 *    diag8cmd     enable     # (needed for messages to Hercules console)
                                                      61 *    runtest      2
                                                      62 *    diag8cmd     disable    # (reset back to default)
                                                      63 *
                                                      64 *    *Done
                                                      65 *
                                                      66 **********************************************************************
```

```
 LOC         OBJECT CODE      ADDR1    ADDR2    STMT

                                               68 ****************************************************************************
                                               69 *         FCHECK Macro - Is a Facility Bit set?
                                               70 *
                                               71 *         If the facility bit is NOT set, an message is issued and
                                               72 *         the test is skipped.
                                               73 *
                                               74 *         Fcheck uses R0, R1 and R2
                                               75 *
                                               76 * eg.     FCHECK 134,'vector-packed-decimal'
                                               77 ****************************************************************************
                                               78         MACRO
                                               79         FCHECK &BITNO,&NOTSETMSG
                                               80 .*                        &BITNO : facility bit number to check
                                               81 .*                        &NOTSETMSG : 'facility name'
                                               82         LCLA  &FBBYTE        Facility bit in Byte
                                               83         LCLA  &FBBIT         Facility bit within Byte
                                               84
                                               85         LCLA  &L(8)
                                               86 &L(1)   SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                               87
                                               88 &FBBYTE SETA  &BITNO/8
                                               89 &FBBIT  SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                               90 .*            MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                               91
                                               92         B     X&SYSNDX
                                               93 *                                       Fcheck data area
                                               94 *                                       skip messgae
                                               95 SKT&SYSNDX DC  C'    Skipping tests: '
                                               96         DC    C&NOTSETMSG
                                               97         DC    C' (bit &BITNO) is not installed.'
                                               98 SKL&SYSNDX EQU *-SKT&SYSNDX
                                               99 *                                       facility bits
                                              100         DS    FD               gap
                                              101 FB&SYSNDX DS  4FD
                                              102         DS    FD               gap
                                              103 *
                                              104 X&SYSNDX EQU *
                                              105         LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                              106         STFLE FB&SYSNDX             get facility bits
                                              107
                                              108         XGR   R0,R0
                                              109         IC    R0,FB&SYSNDX+&FBBYTE   get fbit byte
                                              110         N     R0,=F'&FBBIT'          is bit set?
                                              111         BNZ   XC&SYSNDX
                                              112 *
                                              113 * facility bit not set, issue message and exit
                                              114 *
                                              115         LA    R0,SKL&SYSNDX          message length
                                              116         LA    R1,SKT&SYSNDX          message address
                                              117         BAL   R2,MSG
                                              118
                                              119         B     EOJ
                                              120 XC&SYSNDX EQU *
                                              121         MEND
```

```
  LOC          OBJECT CODE         ADDR1      ADDR2      STMT

                                                         123 ********************************************************************************
                                                         124 *         Low core PSWs
                                                         125 ********************************************************************************
                                   00000000   0000291F   126 ZVE7TST  START 0
  00000000                         00000000              127          USING ZVE7TST,R0               Low core addressability
                                                         128
                                   00000140   00000000   129 SVOLDPSW EQU   ZVE7TST+X'140'            z/Arch Supervisor call old PSW

  00000000                         00000000   000001A0   131          ORG   ZVE7TST+X'1A0'            z/Architecure RESTART PSW
  000001A0    00000001 80000000                          132          DC    X'0000000180000000'
  000001A8    00000000 00000200                          133          DC    AD(BEGIN)

  000001B0                         000001B0   000001D0   135          ORG   ZVE7TST+X'1D0'            z/Architecure PROGRAM CHECK PSW
  000001D0    00020001 80000000                          136          DC    X'0002000180000000'
  000001D8    00000000 0000DEAD                          137          DC    AD(X'DEAD')


  000001E0                         000001E0   00000200   139          ORG   ZVE7TST+X'200'            Start of actual test program..


                                                         141 ********************************************************************************
                                                         142 *              The actual "ZVE7TST" program itself...
                                                         143 ********************************************************************************
                                                         144 *
                                                         145 *   Architecture Mode: z/Arch
                                                         146 *   Register Usage:
                                                         147 *
                                                         148 *    R0        (work)
                                                         149 *    R1-4      (work)
                                                         150 *    R5        Testing control table - current test base
                                                         151 *    R6-R7     (work)
                                                         152 *    R8        First base register
                                                         153 *    R9        Second base register
                                                         154 *    R10       Third base register
                                                         155 *    R11       E7TEST call return
                                                         156 *    R12       E7TESTS register
                                                         157 *    R13       (work)
                                                         158 *    R14       Subroutine call
                                                         159 *    R15       Secondary Subroutine call or work
                                                         160 *
                                                         161 ********************************************************************************

  00000200                         00000200              163          USING  BEGIN,R8            FIRST Base Register
  00000200                         00001200              164          USING  BEGIN+4096,R9       SECOND Base Register
  00000200                         00002200              165          USING  BEGIN+8192,R10      THIRD Base Register

  00000200    0580                                       167 BEGIN    BALR  R8,0                 Initialize FIRST base register
  00000202    0680                                       168          BCTR  R8,0                 Initialize FIRST base register
  00000204    0680                                       169          BCTR  R8,0                 Initialize FIRST base register

  00000206    4190 8800                        00000800  171          LA    R9,2048(,R8)         Initialize SECOND base register
  0000020A    4190 9800                        00000800  172          LA    R9,2048(,R9)         Initialize SECOND base register
                                                         173
```

```
  LOC        OBJECT CODE      ADDR1      ADDR2      STMT

0000020E   41A0 9800                    00000800   174            LA     R10,2048(,R9)      Initalize THIRD base register
00000212   41A0 A800                    00000800   175            LA     R10,2048(,R10)     Initalize THIRD base register
                                                   176
00000216   B600 8324                    00000524   177            STCTL  R0,R0,CTLR0        Store CR0 to enable AFP
0000021A   9604 8325                    00000525   178            OI     CTLR0+1,X'04'      Turn on AFP bit
0000021E   9602 8325                    00000525   179            OI     CTLR0+1,X'02'      Turn on Vector bit
00000222   B700 8324                    00000524   180            LCTL   R0,R0,CTLR0        Reload updated CR0
                                                   181
                                                   182  *************************************************************************
                                                   183  * Is z/Architecture vector facility installed  (bit 129)
                                                   184  *************************************************************************
                                                   185
                                                   186            FCHECK 129,'z/Architecture vector facility'
00000226   47F0 80A8                    000002A8   187+           B      X0001
                                                   188+*                                    Fcheck data area
                                                   189+*                                    skip messgae
0000022A   40404040 E2928997                       190+SKT0001    DC     C'     Skipping tests: '
0000023E   A961C199 838889A3                       191+           DC     C'z/Architecture vector facility'
0000025C   404D8289 A340F1F2                       192+           DC     C' (bit 129) is not installed.'
           0000004E  00000001                      193+SKL0001    EQU    *-SKT0001
                                                   194+*                                    facility bits
00000278   00000000 00000000                       195+           DS     FD                 gap
00000280   00000000 00000000                       196+FB0001     DS     4FD
000002A0   00000000 00000000                       197+           DS     FD                 gap
                                                   198+*
           000002A8  00000001                      199+X0001      EQU    *
000002A8   4100 0004                    00000004   200+           LA     R0,((X0001-FB0001)/8)-1
000002AC   B2B0 8080                    00000280   201+           STFLE  FB0001             get facility bits
000002B0   B982 0000                               202+           XGR    R0,R0
000002B4   4300 8090                    00000290   203+           IC     R0,FB0001+16       get fbit byte
000002B8   5400 832C                    0000052C   204+           N      R0,=F'64'          is bit set?
000002BC   4770 80D0                    000002D0   205+           BNZ    XC0001
                                                   206+*
                                                   207+* facility bit not set, issue message and exit
                                                   208+*
000002C0   4100 004E                    0000004E   209+           LA     R0,SKL0001         message length
000002C4   4110 802A                    0000022A   210+           LA     R1,SKT0001         message address
000002C8   4520 8240                    00000440   211+           BAL    R2,MSG
000002CC   47F0 8308                    00000508   212+           B      EOJ
           000002D0  00000001                      213+XC0001     EQU    *
                                                   214
                                                   215  *************************************************************************
                                                   216  * Is z/Architecture vector enhancements facility 1 installed  (bit 135)
                                                   217  * required by:
                                                   218  *    E76C VNX    - Vector Not Exclusive OR
                                                   219  *    E76E VNN    - Vector NAND
                                                   220  *************************************************************************
                                                   221
                                                   222            FCHECK 135,'z/Arch vector enhance facility 1'
000002D0   47F0 8158                    00000358   223+           B      X0002
                                                   224+*                                    Fcheck data area
                                                   225+*                                    skip messgae
000002D4   40404040 E2928997                       226+SKT0002    DC     C'     Skipping tests: '
000002E8   A961C199 838840A5                       227+           DC     C'z/Arch vector enhance facility 1'
00000308   404D8289 A340F1F3                       228+           DC     C' (bit 135) is not installed.'
           00000050  00000001                      229+SKL0002    EQU    *-SKT0002
```

```
  LOC         OBJECT CODE      ADDR1      ADDR2      STMT

                                                    230+*                                    facility bits
00000328  00000000 00000000                         231+        DS     FD                    gap
00000330  00000000 00000000                         232+FB0002  DS     4FD
00000350  00000000 00000000                         233+        DS     FD                    gap
                                                    234+*
                               00000358  00000001   235+X0002   EQU    *
00000358  4100 0004                       00000004  236+        LA     R0,((X0002-FB0002)/8)-1
0000035C  B2B0 8130                       00000330  237+        STFLE  FB0002                 get facility bits
00000360  B982 0000                                 238+        XGR    R0,R0
00000364  4300 8140                       00000340  239+        IC     R0,FB0002+16           get fbit byte
00000368  5400 8330                       00000530  240+        N      R0,=F'1'               is bit set?
0000036C  4770 8180                       00000380  241+        BNZ    XC0002
                                                    242+*
                                                    243+* facility bit not set, issue message and exit
                                                    244+*
00000370  4100 0050                       00000050  245+        LA     R0,SKL0002             message length
00000374  4110 80D4                       000002D4  246+        LA     R1,SKT0002             message address
00000378  4520 8240                       00000440  247+        BAL    R2,MSG
0000037C  47F0 8308                       00000508  248+        B      EOJ
                               00000380  00000001   249+XC0002  EQU    *
```

```
  LOC         OBJECT CODE     ADDR1     ADDR2     STMT

                                                  251 ****************************************************************************
                                                  252 *                Do tests in the E7TESTS table
                                                  253 ****************************************************************************
                                                  254
00000380    58C0 8334                   00000534  255          L      R12,=A(E7TESTS)       get table of test addresses
                                                  256
                            00000384    00000001  257 NEXTE7   EQU    *
00000384    5850 C000                   00000000  258          L      R5,0(0,R12)          get test address
00000388    1255                                  259          LTR    R5,R5                have a test?
0000038A    4780 81CE                   000003CE  260          BZ     ENDTEST                 done?
                                                  261
0000038E                    00000000              262          USING  E7TEST,R5
                                                  263
0000038E    4800 5004                   00000004  264          LH     R0,TNUM              save current test number
00000392    5000 8E04                   00001004  265          ST     R0,TESTING           for easy reference
                                                  266
00000396    E710 8E88 0006              00001088  267          VL     V1,V1FUDGE
0000039C    58B0 5000                   00000000  268          L      R11,TSUB             get address of test routine
000003A0    05BB                                  269          BALR   R11,R11              do test
                                                  270
000003A2    E310 501C 0014              0000001C  271          LGF    R1,READDR            get address of expected result
000003A8    D50F 5028 1000    00000028  00000000  272          CLC    V10UTPUT,0(R1)       valid?
000003AE    4770 81BA                   000003BA  273          BNE    FAILMSG                 no, issue failed message
                                                  274
000003B2    41C0 C004                   00000004  275          LA     R12,4(0,R12)         next test address
000003B6    47F0 8184                   00000384  276          B      NEXTE7
```

```
   LOC        OBJECT CODE      ADDR1      ADDR2     STMT

                                                    278 *******************************************************************************
                                                    279 * result not as expected:
                                                    280 *        issue message with test number, instruction under test
                                                    281 *             and instruction m4
                                                    282 *******************************************************************************
                              000003BA  00000001    283 FAILMSG  EQU   *
000003BA   45F0 81DC                     000003DC    284          BAL   R15,RPTERROR


                                                    286 *******************************************************************************
                                                    287 * continue after a failed test
                                                    288 *******************************************************************************
                              000003BE  00000001    289 FAILCONT EQU   *
000003BE   5800 8330                     00000530    290          L     R0,=F'1'            set failed test indicator
000003C2   5000 8E00                     00001000    291          ST    R0,FAILED
                                                    292
000003C6   41C0 C004                     00000004    293          LA    R12,4(0,R12)       next test address
000003CA   47F0 8184                     00000384    294          B     NEXTE7


                                                    296 *******************************************************************************
                                                    297 * end of testing; set ending psw
                                                    298 *******************************************************************************
                              000003CE  00000001    299 ENDTEST  EQU   *
000003CE   5810 8E00                     00001000    300          L     R1,FAILED          did a test fail?
000003D2   1211                                      301          LTR   R1,R1
000003D4   4780 8308                     00000508    302          BZ    EOJ                No, exit
000003D8   47F0 8320                     00000520    303          B     FAILTEST           Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

                                                305 ********************************************************************
                                                306 *         RPTERROR                  Report instruction test in error
                                                307 ********************************************************************

000003DC  50F0 8224                  00000424  309 RPTERROR ST    R15,RPTSAVE          Save return address
000003E0  5050 8228                  00000428  310          ST    R5,RPTSVR5           Save R5
                                                311 *
000003E4  4820 5004                  00000004  312          LH    R2,TNUM              get test number and convert
000003E8  4E20 8E67                  00001067  313          CVD   R2,DECNUM
000003EC  D211 8E51 8E3B    00001051  0000103B  314          MVC   PRT3,EDIT
000003F2  DE11 8E51 8E67    00001051  00001067  315          ED    PRT3,DECNUM
000003F8  D202 8E18 8E5E    00001018  0000105E  316          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                317
000003FE  D207 8E33 5008    00001033  00000008  318          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                319 *
                                                320 *         Use Hercules Diagnose for Message to console
                                                321 *
00000404  9002 8230                  00000430  322          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000408  4100 0033                  00000033  323          LA    R0,PRTLNG            message length
0000040C  4110 8E08                  00001008  324          LA    R1,PRTLINE           messagfe address
00000410  4520 8240                  00000440  325          BAL   R2,MSG               call Hercules console MSG display
00000414  9802 8230                  00000430  326          LM    R0,R2,RPTDWSAV       restore regs


00000418  5850 8228                  00000428  328          L     R5,RPTSVR5           Restore R5
0000041C  58F0 8224                  00000424  329          L     R15,RPTSAVE          Restore return address
00000420  07FF                                  330          BR    R15                  Return to caller

00000424  00000000                             332 RPTSAVE  DC    F'0'                 R15 save area
00000428  00000000                             333 RPTSVR5  DC    F'0'                 R5 save area

00000430  00000000 00000000                     335 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
   LOC        OBJECT CODE      ADDR1     ADDR2    STMT

                                                 337 ****************************************************************************
                                                 338 *          Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                 339 *               R2 = return address
                                                 340 ****************************************************************************

00000440   4900 8338                  00000538   342 MSG      CH     R0,=H'0'              Do we even HAVE a message?
00000444   07D2                                  343          BNHR   R2                    No, ignore

00000446   9002 827C                  0000047C   345          STM    R0,R2,MSGSAVE         Save registers

0000044A   4900 833A                  0000053A   347          CH     R0,=AL2(L'MSGMSG)     Message length within limits?
0000044E   47D0 8256                  00000456   348          BNH    MSGOK                 Yes, continue
00000452   4100 005F                  0000005F   349          LA     R0,L'MSGMSG           No, set to maximum

00000456   1820                                  351 MSGOK    LR     R2,R0                 Copy length to work register
00000458   0620                                  352          BCTR   R2,0                  Minus-1 for execute
0000045A   4420 8288                  00000488   353          EX     R2,MSGMVC             Copy message to O/P buffer

0000045E   4120 200A                  0000000A   355          LA     R2,1+L'MSGCMD(,R2)    Calculate true command length
00000462   4110 828E                  0000048E   356          LA     R1,MSGCMD             Point to true command

00000466   83120008                              358          DC     X'83',X'12',X'0008'   Issue Hercules Diagnose X'008'
0000046A   4780 8276                  00000476   359          BZ     MSGRET                Return if successful
                                                 360
0000046E   1222                                  361          LTR    R2,R2                 Is Diag8 Ry (R2) 0?
00000470   4780 8276                  00000476   362          BZ     MSGRET                 an error occurred but coninue
                                                 363
00000474   0000                                  364          DC     H'0'                  CRASH for debugging purposes

00000476   9802 827C                  0000047C   366 MSGRET   LM     R0,R2,MSGSAVE         Restore registers
0000047A   07F2                                  367          BR     R2                    Return to caller



0000047C   00000000 00000000                     369 MSGSAVE  DC     3F'0'                 Registers save area
00000488   D200 8297 1000   00000497  00000000   370 MSGMVC   MVC    MSGMSG(0),0(R1)       Executed instruction

0000048E   D4E2C7D5 D6C8405C                      372 MSGCMD   DC     C'MSGNOH * '          *** HERCULES MESSAGE COMMAND ***
00000497   40404040 40404040                      373 MSGMSG   DC     CL95' '               The message text to be displayed
                                                 374
```

```
 LOC          OBJECT CODE      ADDR1    ADDR2    STMT

                                                 376 **********************************************************************
                                                 377 *         Normal completion or Abnormal termination PSWs
                                                 378 **********************************************************************


000004F8   00020001 80000000                     380 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000508   B2B2 82F8                    000004F8  382 EOJ      LPSWE EOJPSW                   Normal completion


00000510   00020001 80000000                     384 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

00000520   B2B2 8310                    00000510  386 FAILTEST LPSWE FAILPSW                  Abnormal termination



                                                 388 **********************************************************************
                                                 389 *         Working Storage
                                                 390 **********************************************************************


00000524   00000000                              392 CTLR0    DS    F                    CR0
00000528   00000000                              393          DS    F

0000052C                                         395          LTORG ,                    Literals pool
0000052C   00000040                              396                =F'64'
00000530   00000001                              397                =F'1'
00000534   00002870                              398                =A(E7TESTS)
00000538   0000                                  399                =H'0'
0000053A   005F                                  400                =AL2(L'MSGMSG)
                                                 401
                                                 402 *        some constants
                                                 403
           00000400   00000001                   404 K        EQU   1024                 One KB
           00001000   00000001                   405 PAGE     EQU   (4*K)                Size of one page
           00010000   00000001                   406 K64      EQU   (64*K)               64 KB
           00100000   00000001                   407 MB       EQU   (K*K)                 1 MB
                                                 408
           AABBCCDD   00000001                   409 REG2PATT EQU   X'AABBCCDD'           Polluted Register pattern
           000000DD   00000001                   410 REG2LOW  EQU        X'DD'            (last byte above)
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  412 *===============================================================================
                                                  413 *
                                                  414 *   NOTE: start data on an address that is easy to display
                                                  415 *         within Hercules
                                                  416 *
                                                  417 *===============================================================================
                                                  418
0000053C                         0000053C  00001000  419          ORG    ZVE7TST+X'1000'
00001000  00000000                               420 FAILED   DC     F'0'                          some test failed?
00001004  00000000                               421 TESTING  DC     F'0'                          current test number

                                                  423 *
                                                  424 *          failed message and associated editting
                                                  425 *
00001008  40404040 40404040                      426 PRTLINE  DC     C'        Test # '
00001018  A7A7A7                                  427 PRTNUM   DC     C'xxx'
0000101B  40868189 93858440                       428          DC     c' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                       429 PRTNAME  DC     CL8'xxxxxxxx'
                                 00000033  00000001  430 PRTLNG   EQU    *-PRTLINE
```

```
   LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  432 ********************************************************************
                                                  433 *         TEST failed : message working storge
                                                  434 ********************************************************************
0000103B   40212020 20202020                       435 EDIT      DC     XL18'402120202020202020202020202020202020'
                                                  436
0000104D   7E7E7E6E                                 437          DC     C' ===>'
00001051   40404040 40404040                        438 PRT3     DC     CL18' '
00001063   4C7E7E7E                                 439          DC     C' <==='
00001067   00000000 00000000                        440 DECNUM   DS     CL16


                                                  442 ********************************************************************
                                                  443 *         Vector instruction results, pollution and input
                                                  444 ********************************************************************
00001078                                           445          DS     0F
00001078   00000000 00000000                        446          DS     XL16                                          gap
00001088   FFFFFFFF FFFFFFFF                        447 V1FUDGE  DC     XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'      V1 FUDGE
00001098   00000000 00000000                        448          DS     XL16
```

```
  LOC         OBJECT CODE        ADDR1      ADDR2      STMT

                                                       450 ****************************************************************************
                                                       451 *           E7TEST DSECT
                                                       452 ****************************************************************************


                                                       454 E7TEST    DSECT ,
00000000   00000000                                    455 TSUB      DC      A(0)               pointer  to test
00000004   0000                                        456 TNUM      DC      H'00'              Test Number
00000006   00                                           457           DC      X'00'
00000007   00                                           458           DC      HL1'00'            m field - not used
                                                       459
00000008   40404040 40404040                           460 OPNAME    DC      CL8' '             E7 name
00000010   00000000                                    461 V2ADDR    DC      A(0)               address of v2 source
00000014   00000000                                    462 V3ADDR    DC      A(0)               address of v3 source
00000018   00000000                                    463 RELEN     DC      A(0)               RESULT LENGTH
0000001C   00000000                                    464 READDR    DC      A(0)               result (expected) address
00000020   00000000 00000000                           465           DS      FD                  gap
00000028   00000000 00000000                           466 V1OUTPUT  DS      XL16               V1 Output
00000038   00000000 00000000                           467           DS      FD                  gap
                                                       468
                                                       469 *         test routine will be here (from VRR-c macro)
                                                       470 *
                                                       471 *         followed by
                                                       472 *              EXPECTED RESULT


              00000000   0000291F                       474 ZVE7TST   CSECT ,
000010A8                                                 475           DS      0F


                                                       477 ****************************************************************************
                                                       478 *     Macros to help build test tables
                                                       479 ****************************************************************************


                                                       481 *
                                                       482 * macro to generate individual test
                                                       483 *
                                                       484           MACRO
                                                       485           VRR_C &INST
                                                       486 .*                                    &INST   - VRR-c instruction under test
                                                       487 .*                                      no m fields
                                                       488
                                                       489           GBLA    &TNUM
                                                       490 &TNUM     SETA    &TNUM+1
                                                       491
                                                       492           DS      0FD
                                                       493           USING *,R5               base for test data and test routine
                                                       494
                                                       495 T&TNUM    DC      A(X&TNUM)          address of test routine
                                                       496           DC      H'&TNUM            test number
                                                       497           DC      X'00'
                                                       498           DC      HL1'00'            m field
                                                       499           DC      CL8'&INST'         instruction name
                                                       500           DC      A(RE&TNUM+16)      address of v2 source
```

```
   LOC        OBJECT CODE      ADDR1     ADDR2     STMT
```

```
                                                  501            DC      A(RE&TNUM+32)      address of v3 source
                                                  502            DC      A(16)             result length
                                                  503 REA&TNUM DC        A(RE&TNUM)        result address
                                                  504            DS      FD                gap
                                                  505 V10&TNUM DS        XL16              V1 output
                                                  506            DS      FD                gap
                                                  507 .*
                                                  508 *
                                                  509 X&TNUM     DS      0F
                                                  510            LGF     R1,V2ADDR         load v2 source
                                                  511            VL      v22,0(R1)         use v22 to test decoder
                                                  512
                                                  513            LGF     R1,V3ADDR         load v3 source
                                                  514            VL      v23,0(R1)         use v23 to test decoder
                                                  515
                                                  516            &INST V22,V22,V23         test instruction (dest is a source)
                                                  517            VST     V22,V10&TNUM       save v1 output
                                                  518
                                                  519            BR      R11               return
                                                  520
                                                  521 RE&TNUM    DC      0F                xl16 expected result
                                                  522
                                                  523            DROP    R5
                                                  524            MEND
                                                  
                                                  
                                                  526 *
                                                  527 * macro to generate table of pointers to individual tests
                                                  528 *
                                                  529            MACRO
                                                  530            PTTABLE
                                                  531            GBLA    &TNUM
                                                  532            LCLA    &CUR
                                                  533 &CUR       SETA    1
                                                  534 .*
                                                  535 TTABLE     DS      0F
                                                  536 .LOOP      ANOP
                                                  537 .*
                                                  538            DC      A(T&CUR)
                                                  539 .*
                                                  540 &CUR       SETA    &CUR+1
                                                  541            AIF     (&CUR LE &TNUM).LOOP
                                                  542 *
                                                  543            DC      A(0)              END OF TABLE
                                                  544            DC      A(0)
                                                  545 .*
                                                  546            MEND
                                                  547
```

```
  LOC         OBJECT CODE        ADDR1      ADDR2     STMT

                                                      549 *******************************************************************************
                                                      550 *          E7 VRR-c tests
                                                      551 *******************************************************************************
                                                      552           PRINT DATA
                                                      553
                                                      554 *     E768 VN      - Vector AND
                                                      555 *     E769 VNC     - Vector AND with Complement
                                                      556 *     E76A VO      - Vector OR
                                                      557 *     E76B VNO     - Vector NOR
                                                      558 *     E76C VNX     - Vector Not Exclusive OR
                                                      559 *     E76D VX      - Vector Exclusive OR
                                                      560 *     E76E VNN     - Vector NAND
                                                      561 *     E76F VOC     - Vector OR with Complement
                                                      562
                                                      563 *         VRR-c instruction
                                                      564 *             followed by
                                                      565 *                16 byte expected result (V1)
                                                      566 *                16 byte V2 source
                                                      567 *                16 byte V3 source
                                                      568 *-------------------------------------------------------------------------
                                                      569 *   VN      - Vector AND
                                                      570 *-------------------------------------------------------------------------
                                                      571
                                                      572           VRR_C VN
000010A8                                              573+          DS    0FD
000010A8                              000010A8         574+          USING *,R5                 base for test data and test routine
000010A8  000010E8                                    575+T1        DC    A(X1)                address of test routine
000010AC  0001                                        576+          DC    H'1'                 test number
000010AE  00                                          577+          DC    X'00'
000010AF  00                                          578+          DC    HL1'00'              m field
000010B0  E5D54040 40404040                           579+          DC    CL8'VN'              instruction name
000010B8  00001120                                    580+          DC    A(RE1+16)            address of v2 source
000010BC  00001130                                    581+          DC    A(RE1+32)            address of v3 source
000010C0  00000010                                    582+          DC    A(16)                result length
000010C4  00001110                                    583+REA1      DC    A(RE1)               result address
000010C8  00000000 00000000                           584+          DS    FD                   gap
000010D0  00000000 00000000                           585+V101      DS    XL16                 V1 output
000010D8  00000000 00000000
000010E0  00000000 00000000                           586+          DS    FD                   gap
                                                      587+*
000010E8                                              588+X1        DS    0F
000010E8  E310 5010 0014             00000010         589+          LGF   R1,V2ADDR            load v2 source
000010EE  E761 0000 0806             00000000         590+          VL    v22,0(R1)            use v22 to test decoder
000010F4  E310 5014 0014             00000014         591+          LGF   R1,V3ADDR            load v3 source
000010FA  E771 0000 0806             00000000         592+          VL    v23,0(R1)            use v23 to test decoder
00001100  E766 7000 0E68                              593+          VN    V22,V22,V23          test instruction (dest is a source)
00001106  E760 5028 080E             000010D0         594+          VST   V22,V101              save v1 output
0000110C  07FB                                        595+          BR    R11                  return
00001110                                              596+RE1       DC    0F                   xl16 expected result
00001110                                              597+          DROP  R5
00001110  00000000 00000000                           598           DC    XL16'0000000000000000 0000000000000000'   result
00001118  00000000 00000000
00001120  00000000 00000000                           599           DC    XL16'0000000000000000 0000000000000000'   v2
00001128  00000000 00000000
00001130  00000000 00000000                           600           DC    XL16'0000000000000000 0000000000000000'   v3
00001138  00000000 00000000
```

```
   LOC        OBJECT CODE      ADDR1     ADDR2     STMT


                                                   601
                                                   602          VRR_C VN
00001140                                           603+         DS    0FD
00001140                           00001140        604+         USING *,R5              base for test data and test routine
00001140   00001180                                605+T2       DC    A(X2)             address of test routine
00001144   0002                                    606+         DC    H'2'              test number
00001146   00                                      607+         DC    X'00'
00001147   00                                      608+         DC    HL1'00'           m field
00001148   E5D54040 40404040                        609+         DC    CL8'VN'           instruction name
00001150   000011B8                                610+         DC    A(RE2+16)         address of v2 source
00001154   000011C8                                611+         DC    A(RE2+32)         address of v3 source
00001158   00000010                                612+         DC    A(16)             result length
0000115C   000011A8                                613+REA2     DC    A(RE2)            result address
00001160   00000000 00000000                       614+         DS    FD                gap
00001168   00000000 00000000                       615+V102     DS    XL16              V1 output
00001170   00000000 00000000
00001178   00000000 00000000                       616+         DS    FD                gap
                                                   617+*
00001180                                           618+X2       DS    0F
00001180   E310 5010 0014              00000010    619+         LGF   R1,V2ADDR         load v2 source
00001186   E761 0000 0806              00000000    620+         VL    v22,0(R1)         use v22 to test decoder
0000118C   E310 5014 0014              00000014    621+         LGF   R1,V3ADDR         load v3 source
00001192   E771 0000 0806              00000000    622+         VL    v23,0(R1)         use v23 to test decoder
00001198   E766 7000 0E68                          623+         VN    V22,V22,V23       test instruction (dest is a source)
0000119E   E760 5028 080E              00001168    624+         VST   V22,V102           save v1 output
000011A4   07FB                                    625+         BR    R11               return
000011A8                                           626+RE2      DC    0F                xl16 expected result
000011A8                                           627+         DROP  R5
000011A8   FFFFFFFF FFFFFFFF                        628          DC    XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'     result
000011B0   FFFFFFFF FFFFFFFF
000011B8   FFFFFFFF FFFFFFFF                        629          DC    XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'     v2
000011C0   FFFFFFFF FFFFFFFF
000011C8   FFFFFFFF FFFFFFFF                        630          DC    XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'     v3
000011D0   FFFFFFFF FFFFFFFF
                                                   631
                                                   632          VRR_C VN
000011D8                                           633+         DS    0FD
000011D8                           000011D8        634+         USING *,R5              base for test data and test routine
000011D8   00001218                                635+T3       DC    A(X3)             address of test routine
000011DC   0003                                    636+         DC    H'3'              test number
000011DE   00                                      637+         DC    X'00'
000011DF   00                                      638+         DC    HL1'00'           m field
000011E0   E5D54040 40404040                        639+         DC    CL8'VN'           instruction name
000011E8   00001250                                640+         DC    A(RE3+16)         address of v2 source
000011EC   00001260                                641+         DC    A(RE3+32)         address of v3 source
000011F0   00000010                                642+         DC    A(16)             result length
000011F4   00001240                                643+REA3     DC    A(RE3)            result address
000011F8   00000000 00000000                       644+         DS    FD                gap
00001200   00000000 00000000                       645+V103     DS    XL16              V1 output
00001208   00000000 00000000
00001210   00000000 00000000                       646+         DS    FD                gap
                                                   647+*
00001218                                           648+X3       DS    0F
00001218   E310 5010 0014              00000010    649+         LGF   R1,V2ADDR         load v2 source
0000121E   E761 0000 0806              00000000    650+         VL    v22,0(R1)         use v22 to test decoder
00001224   E310 5014 0014              00000014    651+         LGF   R1,V3ADDR         load v3 source
```

```
  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

0000122A  E771 0000 0806              00000000     652+        VL      v23,0(R1)          use v23 to test decoder
00001230  E766 7000 0E68                           653+        VN      V22,V22,V23        test instruction (dest is a source)
00001236  E760 9000 080E              00001200     654+        VST     V22,V103            save v1 output
0000123C  07FB                                     655+        BR      R11                return
00001240                                           656+RE3     DC      0F                 xl16 expected result
00001240                                           657+        DROP    R5
00001240  00010203 04050607                        658         DC      XL16'0001020304050607 08090A0B0C0D0E0F'    result
00001248  08090A0B 0C0D0E0F
00001250  00010203 04050607                        659         DC      XL16'0001020304050607 08090A0B0C0D0E0F'    v2
00001258  08090A0B 0C0D0E0F
00001260  FFFFFFFF FFFFFFFF                         660         DC      XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v3
00001268  FFFFFFFF FFFFFFFF
                                                   661
                                                   662         VRR_C  VN
00001270                                           663+        DS      0FD
00001270                        00001270           664+        USING  *,R5               base for test data and test routine
00001270  000012B0                                 665+T4      DC      A(X4)              address of test routine
00001274  0004                                     666+        DC      H'4'               test number
00001276  00                                       667+        DC      X'00'
00001277  00                                       668+        DC      HL1'00'            m field
00001278  E5D54040 40404040                        669+        DC      CL8'VN'            instruction name
00001280  000012E8                                 670+        DC      A(RE4+16)          address of v2 source
00001284  000012F8                                 671+        DC      A(RE4+32)          address of v3 source
00001288  00000010                                 672+        DC      A(16)              result length
0000128C  000012D8                                 673+REA4    DC      A(RE4)             result address
00001290  00000000 00000000                        674+        DS      FD                 gap
00001298  00000000 00000000                        675+V104    DS      XL16               V1 output
000012A0  00000000 00000000
000012A8  00000000 00000000                        676+        DS      FD                 gap
                                                   677+*
000012B0                                           678+X4      DS      0F
000012B0  E310 5010 0014              00000010     679+        LGF     R1,V2ADDR          load v2 source
000012B6  E761 0000 0806              00000000     680+        VL      v22,0(R1)          use v22 to test decoder
000012BC  E310 5014 0014              00000014     681+        LGF     R1,V3ADDR          load v3 source
000012C2  E771 0000 0806              00000000     682+        VL      v23,0(R1)          use v23 to test decoder
000012C8  E766 7000 0E68                           683+        VN      V22,V22,V23        test instruction (dest is a source)
000012CE  E760 5028 080E              00001298     684+        VST     V22,V104            save v1 output
000012D4  07FB                                     685+        BR      R11                return
000012D8                                           686+RE4     DC      0F                 xl16 expected result
000012D8                                           687+        DROP    R5
000012D8  F0E0D0C0 B0A09080                        688         DC      XL16'F0E0D0C0B0A09080 7060504030201000'    result
000012E0  70605040 30201000
000012E8  FFFFFFFF FFFFFFFF                         689         DC      XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v2
000012F0  FFFFFFFF FFFFFFFF
000012F8  F0E0D0C0 B0A09080                         690         DC      XL16'F0E0D0C0B0A09080 7060504030201000'    v3
00001300  70605040 30201000
                                                   691
                                                   692         VRR_C  VN
00001308                                           693+        DS      0FD
00001308                        00001308           694+        USING  *,R5               base for test data and test routine
00001308  00001348                                 695+T5      DC      A(X5)              address of test routine
0000130C  0005                                     696+        DC      H'5'               test number
0000130E  00                                       697+        DC      X'00'
0000130F  00                                       698+        DC      HL1'00'            m field
00001310  E5D54040 40404040                        699+        DC      CL8'VN'            instruction name
00001318  00001380                                 700+        DC      A(RE5+16)          address of v2 source
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2      STMT

 0000131C   00001390                                701+          DC     A(RE5+32)        address of v3 source
 00001320   00000010                                702+          DC     A(16)            result length
 00001324   00001370                                703+REA5      DC     A(RE5)           result address
 00001328   00000000 00000000                       704+          DS     FD               gap
 00001330   00000000 00000000                       705+V105      DS     XL16             V1 output
 00001338   00000000 00000000
 00001340   00000000 00000000                       706+          DS     FD               gap
                                                    707+*
 00001348                                           708+X5        DS     0F
 00001348   E310 5010 0014               00000010   709+          LGF    R1,V2ADDR        load v2 source
 0000134E   E761 0000 0806               00000000   710+          VL     v22,0(R1)        use v22 to test decoder
 00001354   E310 5014 0014               00000014   711+          LGF    R1,V3ADDR        load v3 source
 0000135A   E771 0000 0806               00000000   712+          VL     v23,0(R1)        use v23 to test decoder
 00001360   E766 7000 0E68                          713+          VN     V22,V22,V23      test instruction (dest is a source)
 00001366   E760 5028 080E               00001330   714+          VST    V22,V105          save v1 output
 0000136C   07FB                                    715+          BR     R11              return
 00001370                                           716+RE5       DC     0F               xl16 expected result
 00001370                                           717+          DROP   R5
 00001370   F0E0D000 B0A09000                        718          DC     XL16'F0E0D000B0A09000 7060500030201000'    result
 00001378   70605000 30201000
 00001380   FFFFFF00 FFFFFF00                         719          DC     XL16'FFFFFF00FFFFFF00 FFFFFF00FFFFFFFF'    v2
 00001388   FFFFFF00 FFFFFFFF
 00001390   F0E0D0C0 B0A09080                         720          DC     XL16'F0E0D0C0B0A09080 7060504030201000'    v3
 00001398   70605040 30201000
                                                     721
                                                     722 *-------------------------------------------------------------------
                                                     723 *    VNC    - Vector AND with Complement
                                                     724 *-------------------------------------------------------------------
                                                     725
                                                     726          VRR_C VNC
 000013A0                                            727+          DS     0FD
 000013A0                            000013A0        728+          USING  *,R5             base for test data and test routine
 000013A0   000013E0                                 729+T6        DC     A(X6)            address of test routine
 000013A4   0006                                     730+          DC     H'6'             test number
 000013A6   00                                       731+          DC     X'00'
 000013A7   00                                       732+          DC     HL1'00'          m field
 000013A8   E5D5C340 40404040                        733+          DC     CL8'VNC'         instruction name
 000013B0   00001418                                 734+          DC     A(RE6+16)        address of v2 source
 000013B4   00001428                                 735+          DC     A(RE6+32)        address of v3 source
 000013B8   00000010                                 736+          DC     A(16)            result length
 000013BC   00001408                                 737+REA6      DC     A(RE6)           result address
 000013C0   00000000 00000000                        738+          DS     FD               gap
 000013C8   00000000 00000000                        739+V106      DS     XL16             V1 output
 000013D0   00000000 00000000
 000013D8   00000000 00000000                        740+          DS     FD               gap
                                                     741+*
 000013E0                                            742+X6        DS     0F
 000013E0   E310 5010 0014               00000010    743+          LGF    R1,V2ADDR        load v2 source
 000013E6   E761 0000 0806               00000000    744+          VL     v22,0(R1)        use v22 to test decoder
 000013EC   E310 5014 0014               00000014    745+          LGF    R1,V3ADDR        load v3 source
 000013F2   E771 0000 0806               00000000    746+          VL     v23,0(R1)        use v23 to test decoder
 000013F8   E766 7000 0E69                           747+          VNC    V22,V22,V23      test instruction (dest is a source)
 000013FE   E760 5028 080E               000013C8    748+          VST    V22,V106          save v1 output
 00001404   07FB                                     749+          BR     R11              return
 00001408                                            750+RE6       DC     0F               xl16 expected result
 00001408                                            751+          DROP   R5
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00001408   00000000 00000000                     752         DC     XL16'0000000000000000 0000000000000000'    result
00001410   00000000 00000000
00001418   00000000 00000000                     753         DC     XL16'0000000000000000 0000000000000000'    v2
00001420   00000000 00000000
00001428   00000000 00000000                     754         DC     XL16'0000000000000000 0000000000000000'    v3
00001430   00000000 00000000
                                                 755
                                                 756         VRR_C  VNC
00001438                                         757+        DS     0FD
00001438                          00001438       758+        USING  *,R5                    base for test data and test routine
00001438   00001478                              759+T7      DC     A(X7)                   address of test routine
0000143C   0007                                  760+        DC     H'7'                    test number
0000143E   00                                    761+        DC     X'00'
0000143F   00                                    762+        DC     HL1'00'                 m field
00001440   E5D5C340 40404040                     763+        DC     CL8'VNC'                instruction name
00001448   000014B0                              764+        DC     A(RE7+16)               address of v2 source
0000144C   000014C0                              765+        DC     A(RE7+32)               address of v3 source
00001450   00000010                              766+        DC     A(16)                   result length
00001454   000014A0                              767+REA7    DC     A(RE7)                  result address
00001458   00000000 00000000                     768+        DS     FD                      gap
00001460   00000000 00000000                     769+V107    DS     XL16                    V1 output
00001468   00000000 00000000
00001470   00000000 00000000                     770+        DS     FD                      gap
                                                 771+*
00001478                                         772+X7      DS     0F
00001478   E310 5010 0014             00000010   773+        LGF    R1,V2ADDR               load v2 source
0000147E   E761 0000 0806             00000000   774+        VL     v22,0(R1)               use v22 to test decoder
00001484   E310 5014 0014             00000014   775+        LGF    R1,V3ADDR               load v3 source
0000148A   E771 0000 0806             00000000   776+        VL     v23,0(R1)               use v23 to test decoder
00001490   E766 7000 0E69                        777+        VNC    V22,V22,V23             test instruction (dest is a source)
00001496   E760 5028 080E             00001460   778+        VST    V22,V107                 save v1 output
0000149C   07FB                                  779+        BR     R11                     return
000014A0                                         780+RE7     DC     0F                      xl16 expected result
000014A0                                         781+        DROP   R5
000014A0   00000000 00000000                     782         DC     XL16'0000000000000000 0000000000000000'    result
000014A8   00000000 00000000
000014B0   FFFFFFFF FFFFFFFF                      783         DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v2
000014B8   FFFFFFFF FFFFFFFF
000014C0   FFFFFFFF FFFFFFFF                      784         DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v3
000014C8   FFFFFFFF FFFFFFFF
                                                 785
                                                 786         VRR_C  VNC
000014D0                                         787+        DS     0FD
000014D0                          000014D0       788+        USING  *,R5                    base for test data and test routine
000014D0   00001510                              789+T8      DC     A(X8)                   address of test routine
000014D4   0008                                  790+        DC     H'8'                    test number
000014D6   00                                    791+        DC     X'00'
000014D7   00                                    792+        DC     HL1'00'                 m field
000014D8   E5D5C340 40404040                     793+        DC     CL8'VNC'                instruction name
000014E0   00001548                              794+        DC     A(RE8+16)               address of v2 source
000014E4   00001558                              795+        DC     A(RE8+32)               address of v3 source
000014E8   00000010                              796+        DC     A(16)                   result length
000014EC   00001538                              797+REA8    DC     A(RE8)                  result address
000014F0   00000000 00000000                     798+        DS     FD                      gap
000014F8   00000000 00000000                     799+V108    DS     XL16                    V1 output
00001500   00000000 00000000
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001508	00000000 00000000			800+	DS	FD	gap
				801+*			
00001510				802+X8	DS	0F	
00001510	E310 5010 0014		00000010	803+	LGF	R1,V2ADDR	load v2 source
00001516	E761 0000 0806		00000000	804+	VL	v22,0(R1)	use v22 to test decoder
0000151C	E310 5014 0014		00000014	805+	LGF	R1,V3ADDR	load v3 source
00001522	E771 0000 0806		00000000	806+	VL	v23,0(R1)	use v23 to test decoder
00001528	E766 7000 0E69			807+	VNC	V22,V22,V23	test instruction (dest is a source)
0000152E	E760 5028 080E		000014F8	808+	VST	V22,V108	save v1 output
00001534	07FB			809+	BR	R11	return
00001538				810+RE8	DC	0F	xl16 expected result
00001538				811+	DROP	R5	
00001538	00000000 00000000			812	DC	XL16'0000000000000000 0000000000000000'	result
00001540	00000000 00000000						
00001548	00010203 04050607			813	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	v2
00001550	08090A0B 0C0D0E0F						
00001558	FFFFFFFF FFFFFFFF			814	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
00001560	FFFFFFFF FFFFFFFF						
				815			
				816	VRR_C VNC		
00001568				817+	DS	0FD	
00001568		00001568		818+	USING	*,R5	base for test data and test routine
00001568	000015A8			819+T9	DC	A(X9)	address of test routine
0000156C	0009			820+	DC	H'9'	test number
0000156E	00			821+	DC	X'00'	
0000156F	00			822+	DC	HL1'00'	m field
00001570	E5D5C340 40404040			823+	DC	CL8'VNC'	instruction name
00001578	000015E0			824+	DC	A(RE9+16)	address of v2 source
0000157C	000015F0			825+	DC	A(RE9+32)	address of v3 source
00001580	00000010			826+	DC	A(16)	result length
00001584	000015D0			827+REA9	DC	A(RE9)	result address
00001588	00000000 00000000			828+	DS	FD	gap
00001590	00000000 00000000			829+V109	DS	XL16	V1 output
00001598	00000000 00000000						
000015A0	00000000 00000000			830+	DS	FD	gap
				831+*			
000015A8				832+X9	DS	0F	
000015A8	E310 5010 0014		00000010	833+	LGF	R1,V2ADDR	load v2 source
000015AE	E761 0000 0806		00000000	834+	VL	v22,0(R1)	use v22 to test decoder
000015B4	E310 5014 0014		00000014	835+	LGF	R1,V3ADDR	load v3 source
000015BA	E771 0000 0806		00000000	836+	VL	v23,0(R1)	use v23 to test decoder
000015C0	E766 7000 0E69			837+	VNC	V22,V22,V23	test instruction (dest is a source)
000015C6	E760 5028 080E		00001590	838+	VST	V22,V109	save v1 output
000015CC	07FB			839+	BR	R11	return
000015D0				840+RE9	DC	0F	xl16 expected result
000015D0				841+	DROP	R5	
000015D0	0F1F2F3F 4F5F6F7F			842	DC	XL16'0F1F2F3F4F5F6F7F 8F9FAFBFCFDFEFFF'	result
000015D8	8F9FAFBF CFDFEFFF						
000015E0	FFFFFFFF FFFFFFFF			843	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
000015E8	FFFFFFFF FFFFFFFF						
000015F0	F0E0D0C0 B0A09080			844	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3
000015F8	70605040 30201000						
				845			
				846	VRR_C VNC		
00001600				847+	DS	0FD	
00001600		00001600		848+	USING	*,R5	base for test data and test routine

```
  LOC        OBJECT CODE      ADDR1      ADDR2      STMT

00001600    00001640                               849+T10       DC      A(X10)           address of test routine
00001604    000A                                   850+          DC      H'10'            test number
00001606    00                                     851+          DC      X'00'
00001607    00                                     852+          DC      HL1'00'          m field
00001608    E5D5C340 40404040                       853+          DC      CL8'VNC'         instruction name
00001610    00001678                               854+          DC      A(RE10+16)       address of v2 source
00001614    00001688                               855+          DC      A(RE10+32)       address of v3 source
00001618    00000010                               856+          DC      A(16)            result length
0000161C    00001668                               857+REA10     DC      A(RE10)          result address
00001620    00000000 00000000                       858+          DS      FD               gap
00001628    00000000 00000000                       859+V1010     DS      XL16             V1 output
00001630    00000000 00000000
00001638    00000000 00000000                       860+          DS      FD               gap
                                                    861+*
00001640                                            862+X10       DS      0F
00001640    E310 5010 0014             00000010     863+          LGF     R1,V2ADDR        load v2 source
00001646    E761 0000 0806             00000000     864+          VL      v22,0(R1)        use v22 to test decoder
0000164C    E310 5014 0014             00000014     865+          LGF     R1,V3ADDR        load v3 source
00001652    E771 0000 0806             00000000     866+          VL      v23,0(R1)        use v23 to test decoder
00001658    E766 7000 0E69                          867+          VNC     V22,V22,V23      test instruction (dest is a source)
0000165E    E760 5028 080E             00001628     868+          VST     V22,V1010         save v1 output
00001664    07FB                                    869+          BR      R11              return
00001668                                            870+RE10      DC      0F               xl16 expected result
00001668                                            871+          DROP    R5
00001668    0F1F2F00 4F5F6F00                        872           DC      XL16'0F1F2F004F5F6F00 8F9FAF00CFDFEFFF'    result
00001670    8F9FAF00 CFDFEFFF
00001678    FFFFFF00 FFFFFF00                        873           DC      XL16'FFFFFF00FFFFFF00 FFFFFF00FFFFFFFF'    v2
00001680    FFFFFF00 FFFFFFFF
00001688    F0E0D0C0 B0A09080                        874           DC      XL16'F0E0D0C0B0A09080 7060504030201000'    v3
00001690    70605040 30201000
                                                    875
                                                    876 *-------------------------------------------------------------------
                                                    877 *   VO      - Vector OR
                                                    878 *-------------------------------------------------------------------
                                                    879
                                                    880           VRR_C VO
00001698                                            881+          DS      0FD
00001698                                 00001698   882+          USING *,R5              base for test data and test routine
00001698    000016D8                               883+T11       DC      A(X11)           address of test routine
0000169C    000B                                   884+          DC      H'11'            test number
0000169E    00                                     885+          DC      X'00'
0000169F    00                                     886+          DC      HL1'00'          m field
000016A0    E5D64040 40404040                       887+          DC      CL8'VO'          instruction name
000016A8    00001710                               888+          DC      A(RE11+16)       address of v2 source
000016AC    00001720                               889+          DC      A(RE11+32)       address of v3 source
000016B0    00000010                               890+          DC      A(16)            result length
000016B4    00001700                               891+REA11     DC      A(RE11)          result address
000016B8    00000000 00000000                       892+          DS      FD               gap
000016C0    00000000 00000000                       893+V1011     DS      XL16             V1 output
000016C8    00000000 00000000
000016D0    00000000 00000000                       894+          DS      FD               gap
                                                    895+*
000016D8                                            896+X11       DS      0F
000016D8    E310 5010 0014             00000010     897+          LGF     R1,V2ADDR        load v2 source
000016DE    E761 0000 0806             00000000     898+          VL      v22,0(R1)        use v22 to test decoder
000016E4    E310 5014 0014             00000014     899+          LGF     R1,V3ADDR        load v3 source
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000016EA	E771 0000 0806		00000000	900+	VL	v23,0(R1)	use v23 to test decoder
000016F0	E766 7000 0E6A			901+	VO	V22,V22,V23	test instruction (dest is a source)
000016F6	E760 5028 080E		000016C0	902+	VST	V22,V1011	save v1 output
000016FC	07FB			903+	BR	R11	return
00001700				904+RE11	DC	0F	xl16 expected result
00001700				905+	DROP	R5	
00001700	00000000 00000000			906	DC	XL16'0000000000000000 0000000000000000'	result
00001708	00000000 00000000						
00001710	00000000 00000000			907	DC	XL16'0000000000000000 0000000000000000'	v2
00001718	00000000 00000000						
00001720	00000000 00000000			908	DC	XL16'0000000000000000 0000000000000000'	v3
00001728	00000000 00000000						
				909			
				910	VRR_C	V0	
00001730				911+	DS	0FD	
00001730		00001730		912+	USING	*,R5	base for test data and test routine
00001730	00001770			913+T12	DC	A(X12)	address of test routine
00001734	000C			914+	DC	H'12'	test number
00001736	00			915+	DC	X'00'	
00001737	00			916+	DC	HL1'00'	m field
00001738	E5D64040 40404040			917+	DC	CL8'V0'	instruction name
00001740	000017A8			918+	DC	A(RE12+16)	address of v2 source
00001744	000017B8			919+	DC	A(RE12+32)	address of v3 source
00001748	00000010			920+	DC	A(16)	result length
0000174C	00001798			921+REA12	DC	A(RE12)	result address
00001750	00000000 00000000			922+	DS	FD	gap
00001758	00000000 00000000			923+V1012	DS	XL16	V1 output
00001760	00000000 00000000						
00001768	00000000 00000000			924+	DS	FD	gap
				925+*			
00001770				926+X12	DS	0F	
00001770	E310 5010 0014		00000010	927+	LGF	R1,V2ADDR	load v2 source
00001776	E761 0000 0806		00000000	928+	VL	v22,0(R1)	use v22 to test decoder
0000177C	E310 5014 0014		00000014	929+	LGF	R1,V3ADDR	load v3 source
00001782	E771 0000 0806		00000000	930+	VL	v23,0(R1)	use v23 to test decoder
00001788	E766 7000 0E6A			931+	VO	V22,V22,V23	test instruction (dest is a source)
0000178E	E760 5028 080E		00001758	932+	VST	V22,V1012	save v1 output
00001794	07FB			933+	BR	R11	return
00001798				934+RE12	DC	0F	xl16 expected result
00001798				935+	DROP	R5	
00001798	FFFFFFFF FFFFFFFF			936	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	result
000017A0	FFFFFFFF FFFFFFFF						
000017A8	FFFFFFFF FFFFFFFF			937	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
000017B0	FFFFFFFF FFFFFFFF						
000017B8	FFFFFFFF FFFFFFFF			938	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
000017C0	FFFFFFFF FFFFFFFF						
				939			
				940	VRR_C	V0	
000017C8				941+	DS	0FD	
000017C8		000017C8		942+	USING	*,R5	base for test data and test routine
000017C8	00001808			943+T13	DC	A(X13)	address of test routine
000017CC	000D			944+	DC	H'13'	test number
000017CE	00			945+	DC	X'00'	
000017CF	00			946+	DC	HL1'00'	m field
000017D0	E5D64040 40404040			947+	DC	CL8'V0'	instruction name
000017D8	00001840			948+	DC	A(RE13+16)	address of v2 source

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  LOC        OBJECT CODE     ADDR1     ADDR2    STMT

000017DC  00001850                              949+          DC     A(RE13+32)      address of v3 source
000017E0  00000010                              950+          DC     A(16)           result length
000017E4  00001830                              951+REA13     DC     A(RE13)         result address
000017E8  00000000 00000000                     952+          DS     FD              gap
000017F0  00000000 00000000                     953+V1013     DS     XL16            V1 output
000017F8  00000000 00000000
00001800  00000000 00000000                     954+          DS     FD              gap
                                                955+*
00001808                                        956+X13       DS     0F
00001808  E310 5010 0014              00000010  957+          LGF    R1,V2ADDR       load v2 source
0000180E  E761 0000 0806              00000000  958+          VL     v22,0(R1)       use v22 to test decoder
00001814  E310 5014 0014              00000014  959+          LGF    R1,V3ADDR       load v3 source
0000181A  E771 0000 0806              00000000  960+          VL     v23,0(R1)       use v23 to test decoder
00001820  E766 7000 0E6A                        961+          VO     V22,V22,V23     test instruction (dest is a source)
00001826  E760 5028 080E              000017F0  962+          VST    V22,V1013        save v1 output
0000182C  07FB                                  963+          BR     R11             return
00001830                                        964+RE13      DC     0F              xl16 expected result
00001830                                        965+          DROP   R5
00001830  FFFFFFFF FFFFFFFF                      966           DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    result
00001838  FFFFFFFF FFFFFFFF
00001840  00010203 04050607                      967           DC     XL16'0001020304050607 08090A0B0C0D0E0F'    v2
00001848  08090A0B 0C0D0E0F
00001850  FFFFFFFF FFFFFFFF                      968           DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v3
00001858  FFFFFFFF FFFFFFFF

                                                969
                                                970           VRR_C  VO
00001860                                        971+          DS     0FD
00001860                       00001860         972+          USING  *,R5            base for test data and test routine
00001860  000018A0                              973+T14       DC     A(X14)          address of test routine
00001864  000E                                  974+          DC     H'14'           test number
00001866  00                                    975+          DC     X'00'
00001867  00                                    976+          DC     HL1'00'         m field
00001868  E5D64040 40404040                     977+          DC     CL8'VO'         instruction name
00001870  000018D8                              978+          DC     A(RE14+16)      address of v2 source
00001874  000018E8                              979+          DC     A(RE14+32)      address of v3 source
00001878  00000010                              980+          DC     A(16)           result length
0000187C  000018C8                              981+REA14     DC     A(RE14)         result address
00001880  00000000 00000000                     982+          DS     FD              gap
00001888  00000000 00000000                     983+V1014     DS     XL16            V1 output
00001890  00000000 00000000
00001898  00000000 00000000                     984+          DS     FD              gap
                                                985+*
000018A0                                        986+X14       DS     0F
000018A0  E310 5010 0014              00000010  987+          LGF    R1,V2ADDR       load v2 source
000018A6  E761 0000 0806              00000000  988+          VL     v22,0(R1)       use v22 to test decoder
000018AC  E310 5014 0014              00000014  989+          LGF    R1,V3ADDR       load v3 source
000018B2  E771 0000 0806              00000000  990+          VL     v23,0(R1)       use v23 to test decoder
000018B8  E766 7000 0E6A                        991+          VO     V22,V22,V23     test instruction (dest is a source)
000018BE  E760 5028 080E              00001888  992+          VST    V22,V1014        save v1 output
000018C4  07FB                                  993+          BR     R11             return
000018C8                                        994+RE14      DC     0F              xl16 expected result
000018C8                                        995+          DROP   R5
000018C8  FFFFFFFF FFFFFFFF                      996           DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    result
000018D0  FFFFFFFF FFFFFFFF
000018D8  FFFFFFFF FFFFFFFF                      997           DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    v2
000018E0  FFFFFFFF FFFFFFFF
```

```
   LOC        OBJECT CODE      ADDR1    ADDR2    STMT

 000018E8  F0E0D0C0 B0A09080              998         DC     XL16'F0E0D0C0B0A09080 7060504030201000'   v3
 000018F0  70605040 30201000
                                          999
                                         1000         VRR_C  V0
 000018F8                                1001+        DS     0FD
 000018F8                      000018F8  1002+        USING  *,R5                    base for test data and test routine
 000018F8  00001938                      1003+T15     DC     A(X15)                  address of test routine
 000018FC  000F                          1004+        DC     H'15'                   test number
 000018FE  00                            1005+        DC     X'00'
 000018FF  00                            1006+        DC     HL1'00'                 m field
 00001900  E5D64040 40404040             1007+        DC     CL8'V0'                 instruction name
 00001908  00001970                      1008+        DC     A(RE15+16)              address of v2 source
 0000190C  00001980                      1009+        DC     A(RE15+32)              address of v3 source
 00001910  00000010                      1010+        DC     A(16)                   result length
 00001914  00001960                      1011+REA15   DC     A(RE15)                 result address
 00001918  00000000 00000000             1012+        DS     FD                      gap
 00001920  00000000 00000000             1013+V1015   DS     XL16                    V1 output
 00001928  00000000 00000000
 00001930  00000000 00000000             1014+        DS     FD                      gap
                                         1015+*
 00001938                                1016+X15     DS     0F
 00001938  E310 5010 0014       00000010 1017+        LGF    R1,V2ADDR               load v2 source
 0000193E  E761 0000 0806       00000000 1018+        VL     v22,0(R1)               use v22 to test decoder
 00001944  E310 5014 0014       00000014 1019+        LGF    R1,V3ADDR               load v3 source
 0000194A  E771 0000 0806       00000000 1020+        VL     v23,0(R1)               use v23 to test decoder
 00001950  E766 7000 0E6A                1021+        V0     V22,V22,V23             test instruction (dest is a source)
 00001956  E760 5028 080E       00001920 1022+        VST    V22,V1015                save v1 output
 0000195C  07FB                          1023+        BR     R11                     return
 00001960                                1024+RE15    DC     0F                      xl16 expected result
 00001960                                1025+        DROP   R5
 00001960  FFFFFFC0 FFFFFF80             1026         DC     XL16'FFFFFFC0FFFFFF80 FFFFFF40FFFFFFFF'    result
 00001968  FFFFFF40 FFFFFFFF
 00001970  FFFFFF00 FFFFFF00             1027         DC     XL16'FFFFFF00FFFFFF00 FFFFFF00FFFFFFFF'    v2
 00001978  FFFFFF00 FFFFFFFF
 00001980  F0E0D0C0 B0A09080             1028         DC     XL16'F0E0D0C0B0A09080 7060504030201000'   v3
 00001988  70605040 30201000
                                         1029
                                         1030 *----------------------------------------------------------------
                                         1031 *   VN0    - Vector NOR
                                         1032 *----------------------------------------------------------------
                                         1033
                                         1034         VRR_C  VN0
 00001990                                1035+        DS     0FD
 00001990                      00001990  1036+        USING  *,R5                    base for test data and test routine
 00001990  000019D0                      1037+T16     DC     A(X16)                  address of test routine
 00001994  0010                          1038+        DC     H'16'                   test number
 00001996  00                            1039+        DC     X'00'
 00001997  00                            1040+        DC     HL1'00'                 m field
 00001998  E5D5D640 40404040             1041+        DC     CL8'VN0'                instruction name
 000019A0  00001A08                      1042+        DC     A(RE16+16)              address of v2 source
 000019A4  00001A18                      1043+        DC     A(RE16+32)              address of v3 source
 000019A8  00000010                      1044+        DC     A(16)                   result length
 000019AC  000019F8                      1045+REA16   DC     A(RE16)                 result address
 000019B0  00000000 00000000             1046+        DS     FD                      gap
 000019B8  00000000 00000000             1047+V1016   DS     XL16                    V1 output
 000019C0  00000000 00000000
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000019C8	00000000 00000000			1048+	DS	FD	gap
				1049+*			
000019D0				1050+X16	DS	0F	
000019D0	E310 5010 0014		00000010	1051+	LGF	R1,V2ADDR	load v2 source
000019D6	E761 0000 0806		00000000	1052+	VL	v22,0(R1)	use v22 to test decoder
000019DC	E310 5014 0014		00000014	1053+	LGF	R1,V3ADDR	load v3 source
000019E2	E771 0000 0806		00000000	1054+	VL	v23,0(R1)	use v23 to test decoder
000019E8	E766 7000 0E6B			1055+	VNO	V22,V22,V23	test instruction (dest is a source)
000019EE	E760 5028 080E		000019B8	1056+	VST	V22,V1016	save v1 output
000019F4	07FB			1057+	BR	R11	return
000019F8				1058+RE16	DC	0F	xl16 expected result
000019F8				1059+	DROP	R5	
000019F8	FFFFFFFF FFFFFFFF			1060	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	result
00001A00	FFFFFFFF FFFFFFFF						
00001A08	00000000 00000000			1061	DC	XL16'0000000000000000 0000000000000000'	v2
00001A10	00000000 00000000						
00001A18	00000000 00000000			1062	DC	XL16'0000000000000000 0000000000000000'	v3
00001A20	00000000 00000000						
				1063			
				1064	VRR_C	VNO	
00001A28				1065+	DS	0FD	
00001A28		00001A28		1066+	USING	*,R5	base for test data and test routine
00001A28	00001A68			1067+T17	DC	A(X17)	address of test routine
00001A2C	0011			1068+	DC	H'17'	test number
00001A2E	00			1069+	DC	X'00'	
00001A2F	00			1070+	DC	HL1'00'	m field
00001A30	E5D5D640 40404040			1071+	DC	CL8'VNO'	instruction name
00001A38	00001AA0			1072+	DC	A(RE17+16)	address of v2 source
00001A3C	00001AB0			1073+	DC	A(RE17+32)	address of v3 source
00001A40	00000010			1074+	DC	A(16)	result length
00001A44	00001A90			1075+REA17	DC	A(RE17)	result address
00001A48	00000000 00000000			1076+	DS	FD	gap
00001A50	00000000 00000000			1077+V1017	DS	XL16	V1 output
00001A58	00000000 00000000						
00001A60	00000000 00000000			1078+	DS	FD	gap
				1079+*			
00001A68				1080+X17	DS	0F	
00001A68	E310 5010 0014		00000010	1081+	LGF	R1,V2ADDR	load v2 source
00001A6E	E761 0000 0806		00000000	1082+	VL	v22,0(R1)	use v22 to test decoder
00001A74	E310 5014 0014		00000014	1083+	LGF	R1,V3ADDR	load v3 source
00001A7A	E771 0000 0806		00000000	1084+	VL	v23,0(R1)	use v23 to test decoder
00001A80	E766 7000 0E6B			1085+	VNO	V22,V22,V23	test instruction (dest is a source)
00001A86	E760 5028 080E		00001A50	1086+	VST	V22,V1017	save v1 output
00001A8C	07FB			1087+	BR	R11	return
00001A90				1088+RE17	DC	0F	xl16 expected result
00001A90				1089+	DROP	R5	
00001A90	00000000 00000000			1090	DC	XL16'0000000000000000 0000000000000000'	result
00001A98	00000000 00000000						
00001AA0	FFFFFFFF FFFFFFFF			1091	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00001AA8	FFFFFFFF FFFFFFFF						
00001AB0	FFFFFFFF FFFFFFFF			1092	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
00001AB8	FFFFFFFF FFFFFFFF						
				1093			
				1094	VRR_C	VNO	
00001AC0				1095+	DS	0FD	
00001AC0		00001AC0		1096+	USING	*,R5	base for test data and test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001AC0	00001B00			1097+T18	DC	A(X18)	address of test routine
00001AC4	0012			1098+	DC	H'18'	test number
00001AC6	00			1099+	DC	X'00'	
00001AC7	00			1100+	DC	HL1'00'	m field
00001AC8	E5D5D640 40404040			1101+	DC	CL8'VNO'	instruction name
00001AD0	00001B38			1102+	DC	A(RE18+16)	address of v2 source
00001AD4	00001B48			1103+	DC	A(RE18+32)	address of v3 source
00001AD8	00000010			1104+	DC	A(16)	result length
00001ADC	00001B28			1105+REA18	DC	A(RE18)	result address
00001AE0	00000000 00000000			1106+	DS	FD	gap
00001AE8	00000000 00000000			1107+V1018	DS	XL16	V1 output
00001AF0	00000000 00000000						
00001AF8	00000000 00000000			1108+	DS	FD	gap
				1109+*			
00001B00				1110+X18	DS	0F	
00001B00	E310 5010 0014		00000010	1111+	LGF	R1,V2ADDR	load v2 source
00001B06	E761 0000 0806		00000000	1112+	VL	v22,0(R1)	use v22 to test decoder
00001B0C	E310 5014 0014		00000014	1113+	LGF	R1,V3ADDR	load v3 source
00001B12	E771 0000 0806		00000000	1114+	VL	v23,0(R1)	use v23 to test decoder
00001B18	E766 7000 0E6B			1115+	VNO	V22,V22,V23	test instruction (dest is a source)
00001B1E	E760 5028 080E		00001AE8	1116+	VST	V22,V1018	save v1 output
00001B24	07FB			1117+	BR	R11	return
00001B28				1118+RE18	DC	0F	xl16 expected result
00001B28				1119+	DROP	R5	
00001B28	00000000 00000000			1120	DC	XL16'0000000000000000 0000000000000000'	result
00001B30	00000000 00000000						
00001B38	00010203 04050607			1121	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	v2
00001B40	08090A0B 0C0D0E0F						
00001B48	FFFFFFFF FFFFFFFF			1122	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
00001B50	FFFFFFFF FFFFFFFF						
				1123			
				1124	VRR_C VNO		
00001B58				1125+	DS	0FD	
00001B58		00001B58		1126+	USING	*,R5	base for test data and test routine
00001B58	00001B98			1127+T19	DC	A(X19)	address of test routine
00001B5C	0013			1128+	DC	H'19'	test number
00001B5E	00			1129+	DC	X'00'	
00001B5F	00			1130+	DC	HL1'00'	m field
00001B60	E5D5D640 40404040			1131+	DC	CL8'VNO'	instruction name
00001B68	00001BD0			1132+	DC	A(RE19+16)	address of v2 source
00001B6C	00001BE0			1133+	DC	A(RE19+32)	address of v3 source
00001B70	00000010			1134+	DC	A(16)	result length
00001B74	00001BC0			1135+REA19	DC	A(RE19)	result address
00001B78	00000000 00000000			1136+	DS	FD	gap
00001B80	00000000 00000000			1137+V1019	DS	XL16	V1 output
00001B88	00000000 00000000						
00001B90	00000000 00000000			1138+	DS	FD	gap
				1139+*			
00001B98				1140+X19	DS	0F	
00001B98	E310 5010 0014		00000010	1141+	LGF	R1,V2ADDR	load v2 source
00001B9E	E761 0000 0806		00000000	1142+	VL	v22,0(R1)	use v22 to test decoder
00001BA4	E310 5014 0014		00000014	1143+	LGF	R1,V3ADDR	load v3 source
00001BAA	E771 0000 0806		00000000	1144+	VL	v23,0(R1)	use v23 to test decoder
00001BB0	E766 7000 0E6B			1145+	VNO	V22,V22,V23	test instruction (dest is a source)
00001BB6	E760 5028 080E		00001B80	1146+	VST	V22,V1019	save v1 output
00001BBC	07FB			1147+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001BC0				1148+RE19	DC	0F	xl16 expected result
00001BC0				1149+	DROP	R5	
00001BC0	00000000 00000000			1150	DC	XL16'0000000000000000 0000000000000000'	result
00001BC8	00000000 00000000						
00001BD0	FFFFFFFF FFFFFFFF			1151	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00001BD8	FFFFFFFF FFFFFFFF						
00001BE0	F0E0D0C0 B0A09080			1152	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3
00001BE8	70605040 30201000						
				1153			
				1154	VRR_C	VN0	
00001BF0				1155+	DS	0FD	
00001BF0		00001BF0		1156+	USING	*,R5	base for test data and test routine
00001BF0	00001C30			1157+T20	DC	A(X20)	address of test routine
00001BF4	0014			1158+	DC	H'20'	test number
00001BF6	00			1159+	DC	X'00'	
00001BF7	00			1160+	DC	HL1'00'	m field
00001BF8	E5D5D640 40404040			1161+	DC	CL8'VN0'	instruction name
00001C00	00001C68			1162+	DC	A(RE20+16)	address of v2 source
00001C04	00001C78			1163+	DC	A(RE20+32)	address of v3 source
00001C08	00000010			1164+	DC	A(16)	result length
00001C0C	00001C58			1165+REA20	DC	A(RE20)	result address
00001C10	00000000 00000000			1166+	DS	FD	gap
00001C18	00000000 00000000			1167+V1020	DS	XL16	V1 output
00001C20	00000000 00000000						
00001C28	00000000 00000000			1168+	DS	FD	gap
				1169+*			
00001C30				1170+X20	DS	0F	
00001C30	E310 5010 0014		00000010	1171+	LGF	R1,V2ADDR	load v2 source
00001C36	E761 0000 0806		00000000	1172+	VL	v22,0(R1)	use v22 to test decoder
00001C3C	E310 5014 0014		00000014	1173+	LGF	R1,V3ADDR	load v3 source
00001C42	E771 0000 0806		00000000	1174+	VL	v23,0(R1)	use v23 to test decoder
00001C48	E766 7000 0E6B			1175+	VN0	V22,V22,V23	test instruction (dest is a source)
00001C4E	E760 5028 080E		00001C18	1176+	VST	V22,V1020	save v1 output
00001C54	07FB			1177+	BR	R11	return
00001C58				1178+RE20	DC	0F	xl16 expected result
00001C58				1179+	DROP	R5	
00001C58	0000003F 0000007F			1180	DC	XL16'0000003F0000007F 000000BF00000000'	result
00001C60	000000BF 00000000						
00001C68	FFFFFF00 FFFFFF00			1181	DC	XL16'FFFFFF00FFFFFF00 FFFFFF00FFFFFFFF'	v2
00001C70	FFFFFF00 FFFFFFFF						
00001C78	F0E0D0C0 B0A09080			1182	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3
00001C80	70605040 30201000						
				1183			
				1184	*--		
				1185	* VNX - Vector Not Exclusive OR		
				1186	*--		
				1187			
				1188	VRR_C	VNX	
00001C88				1189+	DS	0FD	
00001C88		00001C88		1190+	USING	*,R5	base for test data and test routine
00001C88	00001CC8			1191+T21	DC	A(X21)	address of test routine
00001C8C	0015			1192+	DC	H'21'	test number
00001C8E	00			1193+	DC	X'00'	
00001C8F	00			1194+	DC	HL1'00'	m field
00001C90	E5D5E740 40404040			1195+	DC	CL8'VNX'	instruction name
00001C98	00001D00			1196+	DC	A(RE21+16)	address of v2 source

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00001C9C   00001D10                              1197+          DC     A(RE21+32)        address of v3 source
00001CA0   00000010                              1198+          DC     A(16)             result length
00001CA4   00001CF0                              1199+REA21     DC     A(RE21)           result address
00001CA8   00000000 00000000                     1200+          DS     FD                gap
00001CB0   00000000 00000000                     1201+V1021     DS     XL16              V1 output
00001CB8   00000000 00000000
00001CC0   00000000 00000000                     1202+          DS     FD                gap
                                                 1203+*
00001CC8                                         1204+X21       DS     0F
00001CC8   E310 5010 0014              00000010  1205+          LGF    R1,V2ADDR         load v2 source
00001CCE   E761 0000 0806              00000000  1206+          VL     v22,0(R1)         use v22 to test decoder
00001CD4   E310 5014 0014              00000014  1207+          LGF    R1,V3ADDR         load v3 source
00001CDA   E771 0000 0806              00000000  1208+          VL     v23,0(R1)         use v23 to test decoder
00001CE0   E766 7000 0E6C                        1209+          VNX    V22,V22,V23       test instruction (dest is a source)
00001CE6   E760 5028 080E              00001CB0  1210+          VST    V22,V1021          save v1 output
00001CEC   07FB                                  1211+          BR     R11               return
00001CF0                                         1212+RE21      DC     0F                xl16 expected result
00001CF0                                         1213+          DROP   R5
00001CF0   FFFFFFFF FFFFFFFF                     1214           DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'   result
00001CF8   FFFFFFFF FFFFFFFF
00001D00   00000000 00000000                     1215           DC     XL16'0000000000000000 0000000000000000'  v2
00001D08   00000000 00000000
00001D10   00000000 00000000                     1216           DC     XL16'0000000000000000 0000000000000000'  v3
00001D18   00000000 00000000
                                                 1217
                                                 1218          VRR_C VNX
00001D20                                         1219+          DS     0FD
00001D20                         00001D20        1220+          USING  *,R5             base for test data and test routine
00001D20   00001D60                              1221+T22       DC     A(X22)            address of test routine
00001D24   0016                                  1222+          DC     H'22'             test number
00001D26   00                                    1223+          DC     X'00'
00001D27   00                                    1224+          DC     HL1'00'           m field
00001D28   E5D5E740 40404040                     1225+          DC     CL8'VNX'          instruction name
00001D30   00001D98                              1226+          DC     A(RE22+16)        address of v2 source
00001D34   00001DA8                              1227+          DC     A(RE22+32)        address of v3 source
00001D38   00000010                              1228+          DC     A(16)             result length
00001D3C   00001D88                              1229+REA22     DC     A(RE22)           result address
00001D40   00000000 00000000                     1230+          DS     FD                gap
00001D48   00000000 00000000                     1231+V1022     DS     XL16              V1 output
00001D50   00000000 00000000
00001D58   00000000 00000000                     1232+          DS     FD                gap
                                                 1233+*
00001D60                                         1234+X22       DS     0F
00001D60   E310 5010 0014              00000010  1235+          LGF    R1,V2ADDR         load v2 source
00001D66   E761 0000 0806              00000000  1236+          VL     v22,0(R1)         use v22 to test decoder
00001D6C   E310 5014 0014              00000014  1237+          LGF    R1,V3ADDR         load v3 source
00001D72   E771 0000 0806              00000000  1238+          VL     v23,0(R1)         use v23 to test decoder
00001D78   E766 7000 0E6C                        1239+          VNX    V22,V22,V23       test instruction (dest is a source)
00001D7E   E760 5028 080E              00001D48  1240+          VST    V22,V1022          save v1 output
00001D84   07FB                                  1241+          BR     R11               return
00001D88                                         1242+RE22      DC     0F                xl16 expected result
00001D88                                         1243+          DROP   R5
00001D88   FFFFFFFF FFFFFFFF                     1244           DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'   result
00001D90   FFFFFFFF FFFFFFFF
00001D98   FFFFFFFF FFFFFFFF                     1245           DC     XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'   v2
00001DA0   FFFFFFFF FFFFFFFF
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001DA8	FFFFFFFF FFFFFFFF			1246	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
00001DB0	FFFFFFFF FFFFFFFF						
				1247			
				1248	VRR_C	VNX	
00001DB8				1249+	DS	0FD	
00001DB8		00001DB8		1250+	USING	*,R5	base for test data and test routine
00001DB8	00001DF8			1251+T23	DC	A(X23)	address of test routine
00001DBC	0017			1252+	DC	H'23'	test number
00001DBE	00			1253+	DC	X'00'	
00001DBF	00			1254+	DC	HL1'00'	m field
00001DC0	E5D5E740 40404040			1255+	DC	CL8'VNX'	instruction name
00001DC8	00001E30			1256+	DC	A(RE23+16)	address of v2 source
00001DCC	00001E40			1257+	DC	A(RE23+32)	address of v3 source
00001DD0	00000010			1258+	DC	A(16)	result length
00001DD4	00001E20			1259+REA23	DC	A(RE23)	result address
00001DD8	00000000 00000000			1260+	DS	FD	gap
00001DE0	00000000 00000000			1261+V1023	DS	XL16	V1 output
00001DE8	00000000 00000000						
00001DF0	00000000 00000000			1262+	DS	FD	gap
				1263+*			
00001DF8				1264+X23	DS	0F	
00001DF8	E310 5010 0014		00000010	1265+	LGF	R1,V2ADDR	load v2 source
00001DFE	E761 0000 0806		00000000	1266+	VL	v22,0(R1)	use v22 to test decoder
00001E04	E310 5014 0014		00000014	1267+	LGF	R1,V3ADDR	load v3 source
00001E0A	E771 0000 0806		00000000	1268+	VL	v23,0(R1)	use v23 to test decoder
00001E10	E766 7000 0E6C			1269+	VNX	V22,V22,V23	test instruction (dest is a source)
00001E16	E760 5028 080E		00001DE0	1270+	VST	V22,V1023	save v1 output
00001E1C	07FB			1271+	BR	R11	return
00001E20				1272+RE23	DC	0F	xl16 expected result
00001E20				1273+	DROP	R5	
00001E20	00010203 04050607			1274	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	result
00001E28	08090A0B 0C0D0E0F						
00001E30	00010203 04050607			1275	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	v2
00001E38	08090A0B 0C0D0E0F						
00001E40	FFFFFFFF FFFFFFFF			1276	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
00001E48	FFFFFFFF FFFFFFFF						
				1277			
				1278	VRR_C	VNX	
00001E50				1279+	DS	0FD	
00001E50		00001E50		1280+	USING	*,R5	base for test data and test routine
00001E50	00001E90			1281+T24	DC	A(X24)	address of test routine
00001E54	0018			1282+	DC	H'24'	test number
00001E56	00			1283+	DC	X'00'	
00001E57	00			1284+	DC	HL1'00'	m field
00001E58	E5D5E740 40404040			1285+	DC	CL8'VNX'	instruction name
00001E60	00001EC8			1286+	DC	A(RE24+16)	address of v2 source
00001E64	00001ED8			1287+	DC	A(RE24+32)	address of v3 source
00001E68	00000010			1288+	DC	A(16)	result length
00001E6C	00001EB8			1289+REA24	DC	A(RE24)	result address
00001E70	00000000 00000000			1290+	DS	FD	gap
00001E78	00000000 00000000			1291+V1024	DS	XL16	V1 output
00001E80	00000000 00000000						
00001E88	00000000 00000000			1292+	DS	FD	gap
				1293+*			
00001E90				1294+X24	DS	0F	
00001E90	E310 5010 0014		00000010	1295+	LGF	R1,V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001E96	E761 0000 0806		00000000	1296+	VL	v22,0(R1)	use v22 to test decoder
00001E9C	E310 5014 0014		00000014	1297+	LGF	R1,V3ADDR	load v3 source
00001EA2	E771 0000 0806		00000000	1298+	VL	v23,0(R1)	use v23 to test decoder
00001EA8	E766 7000 0E6C			1299+	VNX	V22,V22,V23	test instruction (dest is a source)
00001EAE	E760 5028 080E		00001E78	1300+	VST	V22,V1024	save v1 output
00001EB4	07FB			1301+	BR	R11	return
00001EB8				1302+RE24	DC	0F	xl16 expected result
00001EB8				1303+	DROP	R5	
00001EB8	F0E0D0C0 B0A09080			1304	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	result
00001EC0	70605040 30201000						
00001EC8	FFFFFFFF FFFFFFFF			1305	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00001ED0	FFFFFFFF FFFFFFFF						
00001ED8	F0E0D0C0 B0A09080			1306	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3
00001EE0	70605040 30201000						
				1307			
				1308	VRR_C VNX		
00001EE8				1309+	DS	0FD	
00001EE8		00001EE8		1310+	USING	*,R5	base for test data and test routine
00001EE8	00001F28			1311+T25	DC	A(X25)	address of test routine
00001EEC	0019			1312+	DC	H'25'	test number
00001EEE	00			1313+	DC	X'00'	
00001EEF	00			1314+	DC	HL1'00'	m field
00001EF0	E5D5E740 40404040			1315+	DC	CL8'VNX'	instruction name
00001EF8	00001F60			1316+	DC	A(RE25+16)	address of v2 source
00001EFC	00001F70			1317+	DC	A(RE25+32)	address of v3 source
00001F00	00000010			1318+	DC	A(16)	result length
00001F04	00001F50			1319+REA25	DC	A(RE25)	result address
00001F08	00000000 00000000			1320+	DS	FD	gap
00001F10	00000000 00000000			1321+V1025	DS	XL16	V1 output
00001F18	00000000 00000000						
00001F20	00000000 00000000			1322+	DS	FD	gap
				1323+*			
00001F28				1324+X25	DS	0F	
00001F28	E310 5010 0014		00000010	1325+	LGF	R1,V2ADDR	load v2 source
00001F2E	E761 0000 0806		00000000	1326+	VL	v22,0(R1)	use v22 to test decoder
00001F34	E310 5014 0014		00000014	1327+	LGF	R1,V3ADDR	load v3 source
00001F3A	E771 0000 0806		00000000	1328+	VL	v23,0(R1)	use v23 to test decoder
00001F40	E766 7000 0E6C			1329+	VNX	V22,V22,V23	test instruction (dest is a source)
00001F46	E760 5028 080E		00001F10	1330+	VST	V22,V1025	save v1 output
00001F4C	07FB			1331+	BR	R11	return
00001F50				1332+RE25	DC	0F	xl16 expected result
00001F50				1333+	DROP	R5	
00001F50	F0E0D03F B0A0907F			1334	DC	XL16'F0E0D03FB0A0907F 706050BF30201000'	result
00001F58	706050BF 30201000						
00001F60	FFFFFF00 FFFFFF00			1335	DC	XL16'FFFFFF00FFFFFF00 FFFFFF00FFFFFFFF'	v2
00001F68	FFFFFF00 FFFFFFFF						
00001F70	F0E0D0C0 B0A09080			1336	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3
00001F78	70605040 30201000						
				1337			
				1338	*--		
				1339	* VX - Vector Exclusive OR		
				1340	*--		
				1341			
				1342	VRR_C VX		
00001F80				1343+	DS	0FD	
00001F80		00001F80		1344+	USING	*,R5	base for test data and test routine

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00001F80   00001FC0                              1345+T26    DC     A(X26)              address of test routine
00001F84   001A                                  1346+       DC     H'26'               test number
00001F86   00                                    1347+       DC     X'00'
00001F87   00                                    1348+       DC     HL1'00'             m field
00001F88   E5E74040 40404040                     1349+       DC     CL8'VX'             instruction name
00001F90   00001FF8                              1350+       DC     A(RE26+16)          address of v2 source
00001F94   00002008                              1351+       DC     A(RE26+32)          address of v3 source
00001F98   00000010                              1352+       DC     A(16)               result length
00001F9C   00001FE8                              1353+REA26  DC     A(RE26)             result address
00001FA0   00000000 00000000                     1354+       DS     FD                  gap
00001FA8   00000000 00000000                     1355+V1026  DS     XL16                V1 output
00001FB0   00000000 00000000
00001FB8   00000000 00000000                     1356+       DS     FD                  gap
                                                 1357+*
00001FC0                                         1358+X26    DS     0F
00001FC0   E310 5010 0014              00000010  1359+       LGF    R1,V2ADDR           load v2 source
00001FC6   E761 0000 0806              00000000  1360+       VL     v22,0(R1)           use v22 to test decoder
00001FCC   E310 5014 0014              00000014  1361+       LGF    R1,V3ADDR           load v3 source
00001FD2   E771 0000 0806              00000000  1362+       VL     v23,0(R1)           use v23 to test decoder
00001FD8   E766 7000 0E6D                        1363+       VX     V22,V22,V23         test instruction (dest is a source)
00001FDE   E760 5028 080E              00001FA8  1364+       VST    V22,V1026            save v1 output
00001FE4   07FB                                  1365+       BR     R11                 return
00001FE8                                         1366+RE26   DC     0F                  xl16 expected result
00001FE8                                         1367+       DROP   R5
00001FE8   00000000 00000000                     1368        DC     XL16'0000000000000000 0000000000000000'    result
00001FF0   00000000 00000000
00001FF8   00000000 00000000                     1369        DC     XL16'0000000000000000 0000000000000000'    v2
00002000   00000000 00000000
00002008   00000000 00000000                     1370        DC     XL16'0000000000000000 0000000000000000'    v3
00002010   00000000 00000000

                                                 1371
                                                 1372        VRR_C VX
00002018                                         1373+       DS     0FD
00002018                    00002018             1374+       USING  *,R5                base for test data and test routine
00002018   00002058                              1375+T27    DC     A(X27)              address of test routine
0000201C   001B                                  1376+       DC     H'27'               test number
0000201E   00                                    1377+       DC     X'00'
0000201F   00                                    1378+       DC     HL1'00'             m field
00002020   E5E74040 40404040                     1379+       DC     CL8'VX'             instruction name
00002028   00002090                              1380+       DC     A(RE27+16)          address of v2 source
0000202C   000020A0                              1381+       DC     A(RE27+32)          address of v3 source
00002030   00000010                              1382+       DC     A(16)               result length
00002034   00002080                              1383+REA27  DC     A(RE27)             result address
00002038   00000000 00000000                     1384+       DS     FD                  gap
00002040   00000000 00000000                     1385+V1027  DS     XL16                V1 output
00002048   00000000 00000000
00002050   00000000 00000000                     1386+       DS     FD                  gap
                                                 1387+*
00002058                                         1388+X27    DS     0F
00002058   E310 5010 0014              00000010  1389+       LGF    R1,V2ADDR           load v2 source
0000205E   E761 0000 0806              00000000  1390+       VL     v22,0(R1)           use v22 to test decoder
00002064   E310 5014 0014              00000014  1391+       LGF    R1,V3ADDR           load v3 source
0000206A   E771 0000 0806              00000000  1392+       VL     v23,0(R1)           use v23 to test decoder
00002070   E766 7000 0E6D                        1393+       VX     V22,V22,V23         test instruction (dest is a source)
00002076   E760 5028 080E              00002040  1394+       VST    V22,V1027            save v1 output
0000207C   07FB                                  1395+       BR     R11                 return
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002080				1396+RE27	DC	0F	xl16 expected result
00002080				1397+	DROP	R5	
00002080	00000000 00000000			1398	DC	XL16'0000000000000000 0000000000000000'	result
00002088	00000000 00000000						
00002090	FFFFFFFF FFFFFFFF			1399	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00002098	FFFFFFFF FFFFFFFF						
000020A0	FFFFFFFF FFFFFFFF			1400	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
000020A8	FFFFFFFF FFFFFFFF						
				1401			
				1402	VRR_C	VX	
000020B0				1403+	DS	0FD	
000020B0		000020B0		1404+	USING	*,R5	base for test data and test routine
000020B0	000020F0			1405+T28	DC	A(X28)	address of test routine
000020B4	001C			1406+	DC	H'28'	test number
000020B6	00			1407+	DC	X'00'	
000020B7	00			1408+	DC	HL1'00'	m field
000020B8	E5E74040 40404040			1409+	DC	CL8'VX'	instruction name
000020C0	00002128			1410+	DC	A(RE28+16)	address of v2 source
000020C4	00002138			1411+	DC	A(RE28+32)	address of v3 source
000020C8	00000010			1412+	DC	A(16)	result length
000020CC	00002118			1413+REA28	DC	A(RE28)	result address
000020D0	00000000 00000000			1414+	DS	FD	gap
000020D8	00000000 00000000			1415+V1028	DS	XL16	V1 output
000020E0	00000000 00000000						
000020E8	00000000 00000000			1416+	DS	FD	gap
				1417+*			
000020F0				1418+X28	DS	0F	
000020F0	E310 5010 0014		00000010	1419+	LGF	R1,V2ADDR	load v2 source
000020F6	E761 0000 0806		00000000	1420+	VL	v22,0(R1)	use v22 to test decoder
000020FC	E310 5014 0014		00000014	1421+	LGF	R1,V3ADDR	load v3 source
00002102	E771 0000 0806		00000000	1422+	VL	v23,0(R1)	use v23 to test decoder
00002108	E766 7000 0E6D			1423+	VX	V22,V22,V23	test instruction (dest is a source)
0000210E	E760 5028 080E		000020D8	1424+	VST	V22,V1028	save v1 output
00002114	07FB			1425+	BR	R11	return
00002118				1426+RE28	DC	0F	xl16 expected result
00002118				1427+	DROP	R5	
00002118	FFFEFDFC FBFAF9F8			1428	DC	XL16'FFFEFDFCFBFAF9F8 F7F6F5F4F3F2F1F0'	result
00002120	F7F6F5F4 F3F2F1F0						
00002128	00010203 04050607			1429	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	v2
00002130	08090A0B 0C0D0E0F						
00002138	FFFFFFFF FFFFFFFF			1430	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
00002140	FFFFFFFF FFFFFFFF						
				1431			
				1432	VRR_C	VX	
00002148				1433+	DS	0FD	
00002148		00002148		1434+	USING	*,R5	base for test data and test routine
00002148	00002188			1435+T29	DC	A(X29)	address of test routine
0000214C	001D			1436+	DC	H'29'	test number
0000214E	00			1437+	DC	X'00'	
0000214F	00			1438+	DC	HL1'00'	m field
00002150	E5E74040 40404040			1439+	DC	CL8'VX'	instruction name
00002158	000021C0			1440+	DC	A(RE29+16)	address of v2 source
0000215C	000021D0			1441+	DC	A(RE29+32)	address of v3 source
00002160	00000010			1442+	DC	A(16)	result length
00002164	000021B0			1443+REA29	DC	A(RE29)	result address
00002168	00000000 00000000			1444+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002170	00000000 00000000			1445+V1029	DS	XL16	V1 output
00002178	00000000 00000000						
00002180	00000000 00000000			1446+	DS	FD	gap
				1447+*			
00002188				1448+X29	DS	0F	
00002188	E310 5010 0014		00000010	1449+	LGF	R1,V2ADDR	load v2 source
0000218E	E761 0000 0806		00000000	1450+	VL	v22,0(R1)	use v22 to test decoder
00002194	E310 5014 0014		00000014	1451+	LGF	R1,V3ADDR	load v3 source
0000219A	E771 0000 0806		00000000	1452+	VL	v23,0(R1)	use v23 to test decoder
000021A0	E766 7000 0E6D			1453+	VX	V22,V22,V23	test instruction (dest is a source)
000021A6	E760 5028 080E		00002170	1454+	VST	V22,V1029	save v1 output
000021AC	07FB			1455+	BR	R11	return
000021B0				1456+RE29	DC	0F	xl16 expected result
000021B0				1457+	DROP	R5	
000021B0	0F1F2F3F 4F5F6F7F			1458	DC	XL16'0F1F2F3F4F5F6F7F 8F9FAFBFCFDFEFFF'	result
000021B8	8F9FAFBF CFDFEFFF						
000021C0	FFFFFFFF FFFFFFFF			1459	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
000021C8	FFFFFFFF FFFFFFFF						
000021D0	F0E0D0C0 B0A09080			1460	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3
000021D8	70605040 30201000						
				1461			
				1462	VRR_C	VX	
000021E0				1463+	DS	0FD	
000021E0		000021E0		1464+	USING	*,R5	base for test data and test routine
000021E0	00002220			1465+T30	DC	A(X30)	address of test routine
000021E4	001E			1466+	DC	H'30'	test number
000021E6	00			1467+	DC	X'00'	
000021E7	00			1468+	DC	HL1'00'	m field
000021E8	E5E74040 40404040			1469+	DC	CL8'VX'	instruction name
000021F0	00002258			1470+	DC	A(RE30+16)	address of v2 source
000021F4	00002268			1471+	DC	A(RE30+32)	address of v3 source
000021F8	00000010			1472+	DC	A(16)	result length
000021FC	00002248			1473+REA30	DC	A(RE30)	result address
00002200	00000000 00000000			1474+	DS	FD	gap
00002208	00000000 00000000			1475+V1030	DS	XL16	V1 output
00002210	00000000 00000000						
00002218	00000000 00000000			1476+	DS	FD	gap
				1477+*			
00002220				1478+X30	DS	0F	
00002220	E310 5010 0014		00000010	1479+	LGF	R1,V2ADDR	load v2 source
00002226	E761 0000 0806		00000000	1480+	VL	v22,0(R1)	use v22 to test decoder
0000222C	E310 5014 0014		00000014	1481+	LGF	R1,V3ADDR	load v3 source
00002232	E771 0000 0806		00000000	1482+	VL	v23,0(R1)	use v23 to test decoder
00002238	E766 7000 0E6D			1483+	VX	V22,V22,V23	test instruction (dest is a source)
0000223E	E760 A008 080E		00002208	1484+	VST	V22,V1030	save v1 output
00002244	07FB			1485+	BR	R11	return
00002248				1486+RE30	DC	0F	xl16 expected result
00002248				1487+	DROP	R5	
00002248	0F1F2FC0 4F5F6F80			1488	DC	XL16'0F1F2FC04F5F6F80 8F9FAF40CFDFEFFF'	result
00002250	8F9FAF40 CFDFEFFF						
00002258	FFFFFF00 FFFFFF00			1489	DC	XL16'FFFFFF00FFFFFF00 FFFFFF00FFFFFFFF'	v2
00002260	FFFFFF00 FFFFFFFF						
00002268	F0E0D0C0 B0A09080			1490	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3
00002270	70605040 30201000						
				1491			
				1492	*---		

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  1493 *   VNN    - Vector NAND
                                                  1494 *-------------------------------------------------------------------
                                                  1495
                                                  1496           VRR_C VNN
00002278                                          1497+          DS    0FD
00002278                        00002278          1498+          USING *,R5                 base for test data and test routine
00002278  000022B8                                1499+T31       DC    A(X31)                address of test routine
0000227C  001F                                    1500+          DC    H'31'                 test number
0000227E  00                                      1501+          DC    X'00'
0000227F  00                                      1502+          DC    HL1'00'               m field
00002280  E5D5D540 40404040                        1503+          DC    CL8'VNN'              instruction name
00002288  000022F0                                1504+          DC    A(RE31+16)            address of v2 source
0000228C  00002300                                1505+          DC    A(RE31+32)            address of v3 source
00002290  00000010                                1506+          DC    A(16)                 result length
00002294  000022E0                                1507+REA31     DC    A(RE31)               result address
00002298  00000000 00000000                       1508+          DS    FD                    gap
000022A0  00000000 00000000                       1509+V1031     DS    XL16                  V1 output
000022A8  00000000 00000000
000022B0  00000000 00000000                       1510+          DS    FD                    gap
                                                  1511+*
000022B8                                          1512+X31       DS    0F
000022B8  E310 5010 0014                  00000010 1513+          LGF   R1,V2ADDR             load v2 source
000022BE  E761 0000 0806                  00000000 1514+          VL    v22,0(R1)             use v22 to test decoder
000022C4  E310 5014 0014                  00000014 1515+          LGF   R1,V3ADDR             load v3 source
000022CA  E771 0000 0806                  00000000 1516+          VL    v23,0(R1)             use v23 to test decoder
000022D0  E766 7000 0E6E                           1517+          VNN   V22,V22,V23           test instruction (dest is a source)
000022D6  E760 5028 080E                  000022A0 1518+          VST   V22,V1031              save v1 output
000022DC  07FB                                     1519+          BR    R11                   return
000022E0                                           1520+RE31     DC    0F                    xl16 expected result
000022E0                                           1521+          DROP  R5
000022E0  FFFFFFFF FFFFFFFF                         1522           DC    XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'    result
000022E8  FFFFFFFF FFFFFFFF
000022F0  00000000 00000000                         1523           DC    XL16'0000000000000000 0000000000000000'    v2
000022F8  00000000 00000000
00002300  00000000 00000000                         1524           DC    XL16'0000000000000000 0000000000000000'    v3
00002308  00000000 00000000
                                                  1525
                                                  1526           VRR_C VNN
00002310                                          1527+          DS    0FD
00002310                        00002310          1528+          USING *,R5                 base for test data and test routine
00002310  00002350                                1529+T32       DC    A(X32)                address of test routine
00002314  0020                                    1530+          DC    H'32'                 test number
00002316  00                                      1531+          DC    X'00'
00002317  00                                      1532+          DC    HL1'00'               m field
00002318  E5D5D540 40404040                        1533+          DC    CL8'VNN'              instruction name
00002320  00002388                                1534+          DC    A(RE32+16)            address of v2 source
00002324  00002398                                1535+          DC    A(RE32+32)            address of v3 source
00002328  00000010                                1536+          DC    A(16)                 result length
0000232C  00002378                                1537+REA32     DC    A(RE32)               result address
00002330  00000000 00000000                       1538+          DS    FD                    gap
00002338  00000000 00000000                       1539+V1032     DS    XL16                  V1 output
00002340  00000000 00000000
00002348  00000000 00000000                       1540+          DS    FD                    gap
                                                  1541+*
00002350                                          1542+X32       DS    0F
00002350  E310 5010 0014                  00000010 1543+          LGF   R1,V2ADDR             load v2 source
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002356	E761 0000 0806		00000000	1544+	VL	v22,0(R1)	use v22 to test decoder
0000235C	E310 5014 0014		00000014	1545+	LGF	R1,V3ADDR	load v3 source
00002362	E771 0000 0806		00000000	1546+	VL	v23,0(R1)	use v23 to test decoder
00002368	E766 7000 0E6E			1547+	VNN	V22,V22,V23	test instruction (dest is a source)
0000236E	E760 5028 080E		00002338	1548+	VST	V22,V1032	save v1 output
00002374	07FB			1549+	BR	R11	return
00002378				1550+RE32	DC	0F	xl16 expected result
00002378				1551+	DROP	R5	
00002378	00000000 00000000			1552	DC	XL16'0000000000000000 0000000000000000'	result
00002380	00000000 00000000						
00002388	FFFFFFFF FFFFFFFF			1553	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00002390	FFFFFFFF FFFFFFFF						
00002398	FFFFFFFF FFFFFFFF			1554	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
000023A0	FFFFFFFF FFFFFFFF						
				1555			
				1556	VRR_C	VNN	
000023A8				1557+	DS	0FD	
000023A8		000023A8		1558+	USING	*,R5	base for test data and test routine
000023A8	000023E8			1559+T33	DC	A(X33)	address of test routine
000023AC	0021			1560+	DC	H'33'	test number
000023AE	00			1561+	DC	X'00'	
000023AF	00			1562+	DC	HL1'00'	m field
000023B0	E5D5D540 40404040			1563+	DC	CL8'VNN'	instruction name
000023B8	00002420			1564+	DC	A(RE33+16)	address of v2 source
000023BC	00002430			1565+	DC	A(RE33+32)	address of v3 source
000023C0	00000010			1566+	DC	A(16)	result length
000023C4	00002410			1567+REA33	DC	A(RE33)	result address
000023C8	00000000 00000000			1568+	DS	FD	gap
000023D0	00000000 00000000			1569+V1033	DS	XL16	V1 output
000023D8	00000000 00000000						
000023E0	00000000 00000000			1570+	DS	FD	gap
				1571+*			
000023E8				1572+X33	DS	0F	
000023E8	E310 5010 0014		00000010	1573+	LGF	R1,V2ADDR	load v2 source
000023EE	E761 0000 0806		00000000	1574+	VL	v22,0(R1)	use v22 to test decoder
000023F4	E310 5014 0014		00000014	1575+	LGF	R1,V3ADDR	load v3 source
000023FA	E771 0000 0806		00000000	1576+	VL	v23,0(R1)	use v23 to test decoder
00002400	E766 7000 0E6E			1577+	VNN	V22,V22,V23	test instruction (dest is a source)
00002406	E760 5028 080E		000023D0	1578+	VST	V22,V1033	save v1 output
0000240C	07FB			1579+	BR	R11	return
00002410				1580+RE33	DC	0F	xl16 expected result
00002410				1581+	DROP	R5	
00002410	FFFEFDFC FBFAF9F8			1582	DC	XL16'FFFEFDFCFBFAF9F8 F7F6F5F4F3F2F1F0'	result
00002418	F7F6F5F4 F3F2F1F0						
00002420	00010203 04050607			1583	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	v2
00002428	08090A0B 0C0D0E0F						
00002430	FFFFFFFF FFFFFFFF			1584	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
00002438	FFFFFFFF FFFFFFFF						
				1585			
				1586	VRR_C	VNN	
00002440				1587+	DS	0FD	
00002440		00002440		1588+	USING	*,R5	base for test data and test routine
00002440	00002480			1589+T34	DC	A(X34)	address of test routine
00002444	0022			1590+	DC	H'34'	test number
00002446	00			1591+	DC	X'00'	
00002447	00			1592+	DC	HL1'00'	m field

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002448	E5D5D540 40404040			1593+	DC	CL8'VNN'	instruction name	
00002450	000024B8			1594+	DC	A(RE34+16)	address of v2 source	
00002454	000024C8			1595+	DC	A(RE34+32)	address of v3 source	
00002458	00000010			1596+	DC	A(16)	result length	
0000245C	000024A8			1597+REA34	DC	A(RE34)	result address	
00002460	00000000 00000000			1598+	DS	FD	gap	
00002468	00000000 00000000			1599+V1034	DS	XL16	V1 output	
00002470	00000000 00000000							
00002478	00000000 00000000			1600+	DS	FD	gap	
				1601+*				
00002480				1602+X34	DS	0F		
00002480	E310 5010 0014		00000010	1603+	LGF	R1,V2ADDR	load v2 source	
00002486	E761 0000 0806		00000000	1604+	VL	v22,0(R1)	use v22 to test decoder	
0000248C	E310 5014 0014		00000014	1605+	LGF	R1,V3ADDR	load v3 source	
00002492	E771 0000 0806		00000000	1606+	VL	v23,0(R1)	use v23 to test decoder	
00002498	E766 7000 0E6E			1607+	VNN	V22,V22,V23	test instruction (dest is a source)	
0000249E	E760 5028 080E		00002468	1608+	VST	V22,V1034	save v1 output	
000024A4	07FB			1609+	BR	R11	return	
000024A8				1610+RE34	DC	0F	xl16 expected result	
000024A8				1611+	DROP	R5		
000024A8	0F1F2F3F 4F5F6F7F			1612	DC	XL16'0F1F2F3F4F5F6F7F 8F9FAFBFCFDFEFFF'	result	
000024B0	8F9FAFBF CFDFEFFF							
000024B8	FFFFFFFF FFFFFFFF			1613	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2	
000024C0	FFFFFFFF FFFFFFFF							
000024C8	F0E0D0C0 B0A09080			1614	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3	
000024D0	70605040 30201000							
				1615				
				1616	VRR_C	VNN		
000024D8				1617+	DS	0FD		
000024D8		000024D8		1618+	USING	*,R5	base for test data and test routine	
000024D8	00002518			1619+T35	DC	A(X35)	address of test routine	
000024DC	0023			1620+	DC	H'35'	test number	
000024DE	00			1621+	DC	X'00'		
000024DF	00			1622+	DC	HL1'00'	m field	
000024E0	E5D5D540 40404040			1623+	DC	CL8'VNN'	instruction name	
000024E8	00002550			1624+	DC	A(RE35+16)	address of v2 source	
000024EC	00002560			1625+	DC	A(RE35+32)	address of v3 source	
000024F0	00000010			1626+	DC	A(16)	result length	
000024F4	00002540			1627+REA35	DC	A(RE35)	result address	
000024F8	00000000 00000000			1628+	DS	FD	gap	
00002500	00000000 00000000			1629+V1035	DS	XL16	V1 output	
00002508	00000000 00000000							
00002510	00000000 00000000			1630+	DS	FD	gap	
				1631+*				
00002518				1632+X35	DS	0F		
00002518	E310 5010 0014		00000010	1633+	LGF	R1,V2ADDR	load v2 source	
0000251E	E761 0000 0806		00000000	1634+	VL	v22,0(R1)	use v22 to test decoder	
00002524	E310 5014 0014		00000014	1635+	LGF	R1,V3ADDR	load v3 source	
0000252A	E771 0000 0806		00000000	1636+	VL	v23,0(R1)	use v23 to test decoder	
00002530	E766 7000 0E6E			1637+	VNN	V22,V22,V23	test instruction (dest is a source)	
00002536	E760 5028 080E		00002500	1638+	VST	V22,V1035	save v1 output	
0000253C	07FB			1639+	BR	R11	return	
00002540				1640+RE35	DC	0F	xl16 expected result	
00002540				1641+	DROP	R5		
00002540	0F1F2FFF 4F5F6FFF			1642	DC	XL16'0F1F2FFF4F5F6FFF 8F9FAFFFCFDFEFFF'	result	
00002548	8F9FAFFF CFDFEFFF							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002550	FFFFFF00 FFFFFF00			1643		DC	XL16'FFFFFF00FFFFFF00 FFFFFF00FFFFFFFF'	v2
00002558	FFFFFF00 FFFFFFFF							
00002560	F0E0D0C0 B0A09080			1644		DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3
00002568	70605040 30201000							
				1645				
				1646	*---			
				1647	*	VOC	- Vector OR with Complement	
				1648	*---			
				1649				
				1650		VRR_C	VOC	
00002570				1651+		DS	0FD	
00002570		00002570		1652+		USING	*,R5	base for test data and test routine
00002570	000025B0			1653+T36		DC	A(X36)	address of test routine
00002574	0024			1654+		DC	H'36'	test number
00002576	00			1655+		DC	X'00'	
00002577	00			1656+		DC	HL1'00'	m field
00002578	E5D6C340 40404040			1657+		DC	CL8'VOC'	instruction name
00002580	000025E8			1658+		DC	A(RE36+16)	address of v2 source
00002584	000025F8			1659+		DC	A(RE36+32)	address of v3 source
00002588	00000010			1660+		DC	A(16)	result length
0000258C	000025D8			1661+REA36		DC	A(RE36)	result address
00002590	00000000 00000000			1662+		DS	FD	gap
00002598	00000000 00000000			1663+V1036		DS	XL16	V1 output
000025A0	00000000 00000000							
000025A8	00000000 00000000			1664+		DS	FD	gap
				1665+*				
000025B0				1666+X36		DS	0F	
000025B0	E310 5010 0014		00000010	1667+		LGF	R1,V2ADDR	load v2 source
000025B6	E761 0000 0806		00000000	1668+		VL	v22,0(R1)	use v22 to test decoder
000025BC	E310 5014 0014		00000014	1669+		LGF	R1,V3ADDR	load v3 source
000025C2	E771 0000 0806		00000000	1670+		VL	v23,0(R1)	use v23 to test decoder
000025C8	E766 7000 0E6F			1671+		VOC	V22,V22,V23	test instruction (dest is a source)
000025CE	E760 5028 080E		00002598	1672+		VST	V22,V1036	save v1 output
000025D4	07FB			1673+		BR	R11	return
000025D8				1674+RE36		DC	0F	xl16 expected result
000025D8				1675+		DROP	R5	
000025D8	FFFFFFFF FFFFFFFF			1676		DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	result
000025E0	FFFFFFFF FFFFFFFF							
000025E8	00000000 00000000			1677		DC	XL16'0000000000000000 0000000000000000'	v2
000025F0	00000000 00000000							
000025F8	00000000 00000000			1678		DC	XL16'0000000000000000 0000000000000000'	v3
00002600	00000000 00000000							
				1679				
				1680		VRR_C	VOC	
00002608				1681+		DS	0FD	
00002608		00002608		1682+		USING	*,R5	base for test data and test routine
00002608	00002648			1683+T37		DC	A(X37)	address of test routine
0000260C	0025			1684+		DC	H'37'	test number
0000260E	00			1685+		DC	X'00'	
0000260F	00			1686+		DC	HL1'00'	m field
00002610	E5D6C340 40404040			1687+		DC	CL8'VOC'	instruction name
00002618	00002680			1688+		DC	A(RE37+16)	address of v2 source
0000261C	00002690			1689+		DC	A(RE37+32)	address of v3 source
00002620	00000010			1690+		DC	A(16)	result length
00002624	00002670			1691+REA37		DC	A(RE37)	result address
00002628	00000000 00000000			1692+		DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002630	00000000 00000000			1693+V1037	DS	XL16	V1 output
00002638	00000000 00000000						
00002640	00000000 00000000			1694+	DS	FD	gap
				1695+*			
00002648				1696+X37	DS	0F	
00002648	E310 5010 0014		00000010	1697+	LGF	R1,V2ADDR	load v2 source
0000264E	E761 0000 0806		00000000	1698+	VL	v22,0(R1)	use v22 to test decoder
00002654	E310 5014 0014		00000014	1699+	LGF	R1,V3ADDR	load v3 source
0000265A	E771 0000 0806		00000000	1700+	VL	v23,0(R1)	use v23 to test decoder
00002660	E766 7000 0E6F			1701+	VOC	V22,V22,V23	test instruction (dest is a source)
00002666	E760 5028 080E		00002630	1702+	VST	V22,V1037	save v1 output
0000266C	07FB			1703+	BR	R11	return
00002670				1704+RE37	DC	0F	xl16 expected result
00002670				1705+	DROP	R5	
00002670	FFFFFFFF FFFFFFFF			1706	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	result
00002678	FFFFFFFF FFFFFFFF						
00002680	FFFFFFFF FFFFFFFF			1707	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
00002688	FFFFFFFF FFFFFFFF						
00002690	FFFFFFFF FFFFFFFF			1708	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
00002698	FFFFFFFF FFFFFFFF						
				1709			
				1710	VRR_C	VOC	
000026A0				1711+	DS	0FD	
000026A0		000026A0		1712+	USING	*,R5	base for test data and test routine
000026A0	000026E0			1713+T38	DC	A(X38)	address of test routine
000026A4	0026			1714+	DC	H'38'	test number
000026A6	00			1715+	DC	X'00'	
000026A7	00			1716+	DC	HL1'00'	m field
000026A8	E5D6C340 40404040			1717+	DC	CL8'VOC'	instruction name
000026B0	00002718			1718+	DC	A(RE38+16)	address of v2 source
000026B4	00002728			1719+	DC	A(RE38+32)	address of v3 source
000026B8	00000010			1720+	DC	A(16)	result length
000026BC	00002708			1721+REA38	DC	A(RE38)	result address
000026C0	00000000 00000000			1722+	DS	FD	gap
000026C8	00000000 00000000			1723+V1038	DS	XL16	V1 output
000026D0	00000000 00000000						
000026D8	00000000 00000000			1724+	DS	FD	gap
				1725+*			
000026E0				1726+X38	DS	0F	
000026E0	E310 5010 0014		00000010	1727+	LGF	R1,V2ADDR	load v2 source
000026E6	E761 0000 0806		00000000	1728+	VL	v22,0(R1)	use v22 to test decoder
000026EC	E310 5014 0014		00000014	1729+	LGF	R1,V3ADDR	load v3 source
000026F2	E771 0000 0806		00000000	1730+	VL	v23,0(R1)	use v23 to test decoder
000026F8	E766 7000 0E6F			1731+	VOC	V22,V22,V23	test instruction (dest is a source)
000026FE	E760 5028 080E		000026C8	1732+	VST	V22,V1038	save v1 output
00002704	07FB			1733+	BR	R11	return
00002708				1734+RE38	DC	0F	xl16 expected result
00002708				1735+	DROP	R5	
00002708	00010203 04050607			1736	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	result
00002710	08090A0B 0C0D0E0F						
00002718	00010203 04050607			1737	DC	XL16'0001020304050607 08090A0B0C0D0E0F'	v2
00002720	08090A0B 0C0D0E0F						
00002728	FFFFFFFF FFFFFFFF			1738	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v3
00002730	FFFFFFFF FFFFFFFF						
				1739			
				1740	VRR_C	VOC	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002738				1741+	DS	0FD	
00002738		00002738		1742+	USING	*,R5	base for test data and test routine
00002738	00002778			1743+T39	DC	A(X39)	address of test routine
0000273C	0027			1744+	DC	H'39'	test number
0000273E	00			1745+	DC	X'00'	
0000273F	00			1746+	DC	HL1'00'	m field
00002740	E5D6C340 40404040			1747+	DC	CL8'VOC'	instruction name
00002748	000027B0			1748+	DC	A(RE39+16)	address of v2 source
0000274C	000027C0			1749+	DC	A(RE39+32)	address of v3 source
00002750	00000010			1750+	DC	A(16)	result length
00002754	000027A0			1751+REA39	DC	A(RE39)	result address
00002758	00000000 00000000			1752+	DS	FD	gap
00002760	00000000 00000000			1753+V1039	DS	XL16	V1 output
00002768	00000000 00000000						
00002770	00000000 00000000			1754+	DS	FD	gap
				1755+*			
00002778				1756+X39	DS	0F	
00002778	E310 5010 0014		00000010	1757+	LGF	R1,V2ADDR	load v2 source
0000277E	E761 0000 0806		00000000	1758+	VL	v22,0(R1)	use v22 to test decoder
00002784	E310 5014 0014		00000014	1759+	LGF	R1,V3ADDR	load v3 source
0000278A	E771 0000 0806		00000000	1760+	VL	v23,0(R1)	use v23 to test decoder
00002790	E766 7000 0E6F			1761+	VOC	V22,V22,V23	test instruction (dest is a source)
00002796	E760 5028 080E		00002760	1762+	VST	V22,V1039	save v1 output
0000279C	07FB			1763+	BR	R11	return
000027A0				1764+RE39	DC	0F	xl16 expected result
000027A0				1765+	DROP	R5	
000027A0	FFFFFFFF FFFFFFFF			1766	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	result
000027A8	FFFFFFFF FFFFFFFF						
000027B0	FFFFFFFF FFFFFFFF			1767	DC	XL16'FFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFF'	v2
000027B8	FFFFFFFF FFFFFFFF						
000027C0	F0E0D0C0 B0A09080			1768	DC	XL16'F0E0D0C0B0A09080 7060504030201000'	v3
000027C8	70605040 30201000						
				1769			
				1770	VRR_C	VOC	
000027D0				1771+	DS	0FD	
000027D0		000027D0		1772+	USING	*,R5	base for test data and test routine
000027D0	00002810			1773+T40	DC	A(X40)	address of test routine
000027D4	0028			1774+	DC	H'40'	test number
000027D6	00			1775+	DC	X'00'	
000027D7	00			1776+	DC	HL1'00'	m field
000027D8	E5D6C340 40404040			1777+	DC	CL8'VOC'	instruction name
000027E0	00002848			1778+	DC	A(RE40+16)	address of v2 source
000027E4	00002858			1779+	DC	A(RE40+32)	address of v3 source
000027E8	00000010			1780+	DC	A(16)	result length
000027EC	00002838			1781+REA40	DC	A(RE40)	result address
000027F0	00000000 00000000			1782+	DS	FD	gap
000027F8	00000000 00000000			1783+V1040	DS	XL16	V1 output
00002800	00000000 00000000						
00002808	00000000 00000000			1784+	DS	FD	gap
				1785+*			
00002810				1786+X40	DS	0F	
00002810	E310 5010 0014		00000010	1787+	LGF	R1,V2ADDR	load v2 source
00002816	E761 0000 0806		00000000	1788+	VL	v22,0(R1)	use v22 to test decoder
0000281C	E310 5014 0014		00000014	1789+	LGF	R1,V3ADDR	load v3 source
00002822	E771 0000 0806		00000000	1790+	VL	v23,0(R1)	use v23 to test decoder
00002828	E766 7000 0E6F			1791+	VOC	V22,V22,V23	test instruction (dest is a source)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000282E	E760 5028 080E		000027F8	1792+	VST	V22,V1040	save v1 output
00002834	07FB			1793+	BR	R11	return
00002838				1794+RE40	DC	0F	xl16 expected result
00002838				1795+	DROP	R5	
00002838	FFFFFF3F FFFFFF7F			1796	DC	XL16'FFFFFF3FFFFFFF7F FFFFFFBFFFFFFFFF'	result
00002840	FFFFFFBF FFFFFFFF						
00002848	FFFFFF00 FFFFFF00			1797	DC	XL16'FFFFFF00FFFFFF00 FFFFFF00FFFFFFFF'	v2
00002850	FFFFFF00 FFFFFFFF						
00002858	F0E0D0C0 B0A09080			1798	DC	XL16'F0E0D0C0B0A09080 70605040302010000'	v3
00002860	70605040 30201000						
				1799			
				1800			
00002868	00000000			1801	DC	F'0'	END OF TABLE
0000286C	00000000			1802	DC	F'0'	
				1803	*		
				1804	* table of pointers to individual load test		
				1805	*		
00002870				1806 E7TESTS	DS	0F	
				1807	PTTABLE		
00002870				1808+TTABLE	DS	0F	
00002870	000010A8			1809+	DC	A(T1)	
00002874	00001140			1810+	DC	A(T2)	
00002878	000011D8			1811+	DC	A(T3)	
0000287C	00001270			1812+	DC	A(T4)	
00002880	00001308			1813+	DC	A(T5)	
00002884	000013A0			1814+	DC	A(T6)	
00002888	00001438			1815+	DC	A(T7)	
0000288C	000014D0			1816+	DC	A(T8)	
00002890	00001568			1817+	DC	A(T9)	
00002894	00001600			1818+	DC	A(T10)	
00002898	00001698			1819+	DC	A(T11)	
0000289C	00001730			1820+	DC	A(T12)	
000028A0	000017C8			1821+	DC	A(T13)	
000028A4	00001860			1822+	DC	A(T14)	
000028A8	000018F8			1823+	DC	A(T15)	
000028AC	00001990			1824+	DC	A(T16)	
000028B0	00001A28			1825+	DC	A(T17)	
000028B4	00001AC0			1826+	DC	A(T18)	
000028B8	00001B58			1827+	DC	A(T19)	
000028BC	00001BF0			1828+	DC	A(T20)	
000028C0	00001C88			1829+	DC	A(T21)	
000028C4	00001D20			1830+	DC	A(T22)	
000028C8	00001DB8			1831+	DC	A(T23)	
000028CC	00001E50			1832+	DC	A(T24)	
000028D0	00001EE8			1833+	DC	A(T25)	
000028D4	00001F80			1834+	DC	A(T26)	
000028D8	00002018			1835+	DC	A(T27)	
000028DC	000020B0			1836+	DC	A(T28)	
000028E0	00002148			1837+	DC	A(T29)	
000028E4	000021E0			1838+	DC	A(T30)	
000028E8	00002278			1839+	DC	A(T31)	
000028EC	00002310			1840+	DC	A(T32)	
000028F0	000023A8			1841+	DC	A(T33)	
000028F4	00002440			1842+	DC	A(T34)	
000028F8	000024D8			1843+	DC	A(T35)	
000028FC	00002570			1844+	DC	A(T36)	

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 LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00002900   00002608                              1845+        DC      A(T37)
00002904   000026A0                              1846+        DC      A(T38)
00002908   00002738                              1847+        DC      A(T39)
0000290C   000027D0                              1848+        DC      A(T40)
                                                 1849+*
00002910   00000000                              1850+        DC      A(0)              END OF TABLE
00002914   00000000                              1851+        DC      A(0)
                                                 1852
00002918   00000000                              1853         DC      F'0'       END OF TABLE
0000291C   00000000                              1854         DC      F'0'
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				1856	**		
				1857	*	Register equates	
				1858	**		
		00000000	00000001	1860	R0	EQU	0
		00000001	00000001	1861	R1	EQU	1
		00000002	00000001	1862	R2	EQU	2
		00000003	00000001	1863	R3	EQU	3
		00000004	00000001	1864	R4	EQU	4
		00000005	00000001	1865	R5	EQU	5
		00000006	00000001	1866	R6	EQU	6
		00000007	00000001	1867	R7	EQU	7
		00000008	00000001	1868	R8	EQU	8
		00000009	00000001	1869	R9	EQU	9
		0000000A	00000001	1870	R10	EQU	10
		0000000B	00000001	1871	R11	EQU	11
		0000000C	00000001	1872	R12	EQU	12
		0000000D	00000001	1873	R13	EQU	13
		0000000E	00000001	1874	R14	EQU	14
		0000000F	00000001	1875	R15	EQU	15
				1877	**		
				1878	*	Register equates	
				1879	**		
		00000000	00000001	1881	V0	EQU	0
		00000001	00000001	1882	V1	EQU	1
		00000002	00000001	1883	V2	EQU	2
		00000003	00000001	1884	V3	EQU	3
		00000004	00000001	1885	V4	EQU	4
		00000005	00000001	1886	V5	EQU	5
		00000006	00000001	1887	V6	EQU	6
		00000007	00000001	1888	V7	EQU	7
		00000008	00000001	1889	V8	EQU	8
		00000009	00000001	1890	V9	EQU	9
		0000000A	00000001	1891	V10	EQU	10
		0000000B	00000001	1892	V11	EQU	11
		0000000C	00000001	1893	V12	EQU	12
		0000000D	00000001	1894	V13	EQU	13
		0000000E	00000001	1895	V14	EQU	14
		0000000F	00000001	1896	V15	EQU	15
		00000010	00000001	1897	V16	EQU	16
		00000011	00000001	1898	V17	EQU	17
		00000012	00000001	1899	V18	EQU	18
		00000013	00000001	1900	V19	EQU	19
		00000014	00000001	1901	V20	EQU	20
		00000015	00000001	1902	V21	EQU	21

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  LOC        OBJECT CODE     ADDR1     ADDR2    STMT

                          00000016  00000001  1903 V22      EQU   22
                          00000017  00000001  1904 V23      EQU   23
                          00000018  00000001  1905 V24      EQU   24
                          00000019  00000001  1906 V25      EQU   25
                          0000001A  00000001  1907 V26      EQU   26
                          0000001B  00000001  1908 V27      EQU   27
                          0000001C  00000001  1909 V28      EQU   28
                          0000001D  00000001  1910 V29      EQU   29
                          0000001E  00000001  1911 V30      EQU   30
                          0000001F  00000001  1912 V31      EQU   31
                                              1913
                                              1914          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES											
BEGIN	I	00000200	2	167	133	163	164	165								
CTLR0	F	00000524	4	392	177	178	179	180								
DECNUM	C	00001067	16	440	313	315										
E7TEST	4	00000000	64	454	262											
E7TESTS	F	00002870	4	1806	255											
EDIT	X	0000103B	18	435	314											
ENDTEST	U	000003CE	1	299	260											
EOJ	I	00000508	4	382	212	248	302									
EOJPSW	D	000004F8	8	380	382											
FAILCONT	U	000003BE	1	289												
FAILED	F	00001000	4	420	291	300										
FAILMSG	U	000003BA	1	283	273											
FAILPSW	D	00000510	8	384	386											
FAILTEST	I	00000520	4	386	303											
FB0001	F	00000280	8	196	200	201	203									
FB0002	F	00000330	8	232	236	237	239									
IMAGE	1	00000000	10528	0												
K	U	00000400	1	404	405	406	407									
K64	U	00010000	1	406												
MB	U	00100000	1	407												
MSG	I	00000440	4	342	211	247	325									
MSGCMD	C	0000048E	9	372	355	356										
MSGMSG	C	00000497	95	373	349	370	347									
MSGMVC	I	00000488	6	370	353											
MSGOK	I	00000456	2	351	348											
MSGRET	I	00000476	4	366	359	362										
MSGSAVE	F	0000047C	4	369	345	366										
NEXTE7	U	00000384	1	257	276	294										
OPNAME	C	00000008	8	460	318											
PAGE	U	00001000	1	405												
PRT3	C	00001051	18	438	314	315	316									
PRTLINE	C	00001008	16	426	430	324										
PRTLNG	U	00000033	1	430	323											
PRTNAME	C	00001033	8	429	318											
PRTNUM	C	00001018	3	427	316											
R0	U	00000000	1	1860	127	177	180	200	202	203	204	209	236	238	239	240	245
					264	265	290	291	322	323	326	342	345	347	349	351	366
R1	U	00000001	1	1861	210	246	271	272	300	301	324	356	370	589	590	591	592
					619	620	621	622	649	650	651	652	679	680	681	682	709
					710	711	712	743	744	745	746	773	774	775	776	803	804
					805	806	833	834	835	836	863	864	865	866	897	898	899
					900	927	928	929	930	957	958	959	960	987	988	989	990
					1017	1018	1019	1020	1051	1052	1053	1054	1081	1082	1083	1084	1111
					1112	1113	1114	1141	1142	1143	1144	1171	1172	1173	1174	1205	1206
					1207	1208	1235	1236	1237	1238	1265	1266	1267	1268	1295	1296	1297
					1298	1325	1326	1327	1328	1359	1360	1361	1362	1389	1390	1391	1392
					1419	1420	1421	1422	1449	1450	1451	1452	1479	1480	1481	1482	1513
					1514	1515	1516	1543	1544	1545	1546	1573	1574	1575	1576	1603	1604
					1605	1606	1633	1634	1635	1636	1667	1668	1669	1670	1697	1698	1699
					1700	1727	1728	1729	1730	1757	1758	1759	1760	1787	1788	1789	1790
R10	U	0000000A	1	1870	165	174	175										
R11	U	0000000B	1	1871	268	269	595	625	655	685	715	749	779	809	839	869	903
					933	963	993	1023	1057	1087	1117	1147	1177	1211	1241	1271	1301
					1331	1365	1395	1425	1455	1485	1519	1549	1579	1609	1639	1673	1703
					1733	1763	1793										
R12	U	0000000C	1	1872	255	258	275	293									

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
R13	U	0000000D	1	1873													
R14	U	0000000E	1	1874													
R15	U	0000000F	1	1875	284	309	329	330									
R2	U	00000002	1	1862	211	247	312	313	322	325	326	343	345	351	352	353	355
					361	366	367										
R3	U	00000003	1	1863													
R4	U	00000004	1	1864													
R5	U	00000005	1	1865	258	259	262	310	328	574	597	604	627	634	657	664	687
					694	717	728	751	758	781	788	811	818	841	848	871	882
					905	912	935	942	965	972	995	1002	1025	1036	1059	1066	1089
					1096	1119	1126	1149	1156	1179	1190	1213	1220	1243	1250	1273	1280
					1303	1310	1333	1344	1367	1374	1397	1404	1427	1434	1457	1464	1487
					1498	1521	1528	1551	1558	1581	1588	1611	1618	1641	1652	1675	1682
					1705	1712	1735	1742	1765	1772	1795						
R6	U	00000006	1	1866													
R7	U	00000007	1	1867													
R8	U	00000008	1	1868	163	167	168	169	171								
R9	U	00000009	1	1869	164	171	172	174									
RE1	F	00001110	4	596	580	581	583										
RE10	F	00001668	4	870	854	855	857										
RE11	F	00001700	4	904	888	889	891										
RE12	F	00001798	4	934	918	919	921										
RE13	F	00001830	4	964	948	949	951										
RE14	F	000018C8	4	994	978	979	981										
RE15	F	00001960	4	1024	1008	1009	1011										
RE16	F	000019F8	4	1058	1042	1043	1045										
RE17	F	00001A90	4	1088	1072	1073	1075										
RE18	F	00001B28	4	1118	1102	1103	1105										
RE19	F	00001BC0	4	1148	1132	1133	1135										
RE2	F	000011A8	4	626	610	611	613										
RE20	F	00001C58	4	1178	1162	1163	1165										
RE21	F	00001CF0	4	1212	1196	1197	1199										
RE22	F	00001D88	4	1242	1226	1227	1229										
RE23	F	00001E20	4	1272	1256	1257	1259										
RE24	F	00001EB8	4	1302	1286	1287	1289										
RE25	F	00001F50	4	1332	1316	1317	1319										
RE26	F	00001FE8	4	1366	1350	1351	1353										
RE27	F	00002080	4	1396	1380	1381	1383										
RE28	F	00002118	4	1426	1410	1411	1413										
RE29	F	000021B0	4	1456	1440	1441	1443										
RE3	F	00001240	4	656	640	641	643										
RE30	F	00002248	4	1486	1470	1471	1473										
RE31	F	000022E0	4	1520	1504	1505	1507										
RE32	F	00002378	4	1550	1534	1535	1537										
RE33	F	00002410	4	1580	1564	1565	1567										
RE34	F	000024A8	4	1610	1594	1595	1597										
RE35	F	00002540	4	1640	1624	1625	1627										
RE36	F	000025D8	4	1674	1658	1659	1661										
RE37	F	00002670	4	1704	1688	1689	1691										
RE38	F	00002708	4	1734	1718	1719	1721										
RE39	F	000027A0	4	1764	1748	1749	1751										
RE4	F	000012D8	4	686	670	671	673										
RE40	F	00002838	4	1794	1778	1779	1781										
RE5	F	00001370	4	716	700	701	703										
RE6	F	00001408	4	750	734	735	737										
RE7	F	000014A0	4	780	764	765	767										

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
RE8	F	00001538	4	810	794	795	797
RE9	F	000015D0	4	840	824	825	827
REA1	A	000010C4	4	583			
REA10	A	0000161C	4	857			
REA11	A	000016B4	4	891			
REA12	A	0000174C	4	921			
REA13	A	000017E4	4	951			
REA14	A	0000187C	4	981			
REA15	A	00001914	4	1011			
REA16	A	000019AC	4	1045			
REA17	A	00001A44	4	1075			
REA18	A	00001ADC	4	1105			
REA19	A	00001B74	4	1135			
REA2	A	0000115C	4	613			
REA20	A	00001C0C	4	1165			
REA21	A	00001CA4	4	1199			
REA22	A	00001D3C	4	1229			
REA23	A	00001DD4	4	1259			
REA24	A	00001E6C	4	1289			
REA25	A	00001F04	4	1319			
REA26	A	00001F9C	4	1353			
REA27	A	00002034	4	1383			
REA28	A	000020CC	4	1413			
REA29	A	00002164	4	1443			
REA3	A	000011F4	4	643			
REA30	A	000021FC	4	1473			
REA31	A	00002294	4	1507			
REA32	A	0000232C	4	1537			
REA33	A	000023C4	4	1567			
REA34	A	0000245C	4	1597			
REA35	A	000024F4	4	1627			
REA36	A	0000258C	4	1661			
REA37	A	00002624	4	1691			
REA38	A	000026BC	4	1721			
REA39	A	00002754	4	1751			
REA4	A	0000128C	4	673			
REA40	A	000027EC	4	1781			
REA5	A	00001324	4	703			
REA6	A	000013BC	4	737			
REA7	A	00001454	4	767			
REA8	A	000014EC	4	797			
REA9	A	00001584	4	827			
READDR	A	0000001C	4	464	271		
REG2LOW	U	000000DD	1	410			
REG2PATT	U	AABBCCDD	1	409			
RELEN	A	00000018	4	463			
RPTDWSAV	D	00000430	8	335	322	326	
RPTERROR	I	000003DC	4	309	284		
RPTSAVE	F	00000424	4	332	309	329	
RPTSVR5	F	00000428	4	333	310	328	
SKL0001	U	0000004E	1	193	209		
SKL0002	U	00000050	1	229	245		
SKT0001	C	0000022A	20	190	193	210	
SKT0002	C	000002D4	20	226	229	246	
SVOLDPSW	U	00000140	0	129			
T1	A	000010A8	4	575	1809		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
T10	A	00001600	4	849	1818	
T11	A	00001698	4	883	1819	
T12	A	00001730	4	913	1820	
T13	A	000017C8	4	943	1821	
T14	A	00001860	4	973	1822	
T15	A	000018F8	4	1003	1823	
T16	A	00001990	4	1037	1824	
T17	A	00001A28	4	1067	1825	
T18	A	00001AC0	4	1097	1826	
T19	A	00001B58	4	1127	1827	
T2	A	00001140	4	605	1810	
T20	A	00001BF0	4	1157	1828	
T21	A	00001C88	4	1191	1829	
T22	A	00001D20	4	1221	1830	
T23	A	00001DB8	4	1251	1831	
T24	A	00001E50	4	1281	1832	
T25	A	00001EE8	4	1311	1833	
T26	A	00001F80	4	1345	1834	
T27	A	00002018	4	1375	1835	
T28	A	000020B0	4	1405	1836	
T29	A	00002148	4	1435	1837	
T3	A	000011D8	4	635	1811	
T30	A	000021E0	4	1465	1838	
T31	A	00002278	4	1499	1839	
T32	A	00002310	4	1529	1840	
T33	A	000023A8	4	1559	1841	
T34	A	00002440	4	1589	1842	
T35	A	000024D8	4	1619	1843	
T36	A	00002570	4	1653	1844	
T37	A	00002608	4	1683	1845	
T38	A	000026A0	4	1713	1846	
T39	A	00002738	4	1743	1847	
T4	A	00001270	4	665	1812	
T40	A	000027D0	4	1773	1848	
T5	A	00001308	4	695	1813	
T6	A	000013A0	4	729	1814	
T7	A	00001438	4	759	1815	
T8	A	000014D0	4	789	1816	
T9	A	00001568	4	819	1817	
TESTING	F	00001004	4	421	265	
TNUM	H	00000004	2	456	264	312
TSUB	A	00000000	4	455	268	
TTABLE	F	00002870	4	1808		
V0	U	00000000	1	1881		
V1	U	00000001	1	1882	267	
V10	U	0000000A	1	1891		
V11	U	0000000B	1	1892		
V12	U	0000000C	1	1893		
V13	U	0000000D	1	1894		
V14	U	0000000E	1	1895		
V15	U	0000000F	1	1896		
V16	U	00000010	1	1897		
V17	U	00000011	1	1898		
V18	U	00000012	1	1899		
V19	U	00000013	1	1900		
V1FUDGE	X	00001088	16	447	267	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V101	X	000010D0	16	585	594												
V1010	X	00001628	16	859	868												
V1011	X	000016C0	16	893	902												
V1012	X	00001758	16	923	932												
V1013	X	000017F0	16	953	962												
V1014	X	00001888	16	983	992												
V1015	X	00001920	16	1013	1022												
V1016	X	000019B8	16	1047	1056												
V1017	X	00001A50	16	1077	1086												
V1018	X	00001AE8	16	1107	1116												
V1019	X	00001B80	16	1137	1146												
V102	X	00001168	16	615	624												
V1020	X	00001C18	16	1167	1176												
V1021	X	00001CB0	16	1201	1210												
V1022	X	00001D48	16	1231	1240												
V1023	X	00001DE0	16	1261	1270												
V1024	X	00001E78	16	1291	1300												
V1025	X	00001F10	16	1321	1330												
V1026	X	00001FA8	16	1355	1364												
V1027	X	00002040	16	1385	1394												
V1028	X	000020D8	16	1415	1424												
V1029	X	00002170	16	1445	1454												
V103	X	00001200	16	645	654												
V1030	X	00002208	16	1475	1484												
V1031	X	000022A0	16	1509	1518												
V1032	X	00002338	16	1539	1548												
V1033	X	000023D0	16	1569	1578												
V1034	X	00002468	16	1599	1608												
V1035	X	00002500	16	1629	1638												
V1036	X	00002598	16	1663	1672												
V1037	X	00002630	16	1693	1702												
V1038	X	000026C8	16	1723	1732												
V1039	X	00002760	16	1753	1762												
V104	X	00001298	16	675	684												
V1040	X	000027F8	16	1783	1792												
V105	X	00001330	16	705	714												
V106	X	000013C8	16	739	748												
V107	X	00001460	16	769	778												
V108	X	000014F8	16	799	808												
V109	X	00001590	16	829	838												
V10UTPUT	X	00000028	16	466	272												
V2	U	00000002	1	1883													
V20	U	00000014	1	1901													
V21	U	00000015	1	1902													
V22	U	00000016	1	1903	590	593	594	620	623	624	650	653	654	680	683	684	710
					713	714	744	747	748	774	777	778	804	807	808	834	837
					838	864	867	868	898	901	902	928	931	932	958	961	962
					988	991	992	1018	1021	1022	1052	1055	1056	1082	1085	1086	1112
					1115	1116	1142	1145	1146	1172	1175	1176	1206	1209	1210	1236	1239
					1240	1266	1269	1270	1296	1299	1300	1326	1329	1330	1360	1363	1364
					1390	1393	1394	1420	1423	1424	1450	1453	1454	1480	1483	1484	1514
					1517	1518	1544	1547	1548	1574	1577	1578	1604	1607	1608	1634	1637
					1638	1668	1671	1672	1698	1701	1702	1728	1731	1732	1758	1761	1762
					1788	1791	1792										
V23	U	00000017	1	1904	592	593	622	623	652	653	682	683	712	713	746	747	776
					777	806	807	836	837	866	867	900	901	930	931	960	961

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					990	991	1020	1021	1054	1055	1084	1085	1114	1115	1144	1145	1174
					1175	1208	1209	1238	1239	1268	1269	1298	1299	1328	1329	1362	1363
					1392	1393	1422	1423	1452	1453	1482	1483	1516	1517	1546	1547	1576
					1577	1606	1607	1636	1637	1670	1671	1700	1701	1730	1731	1760	1761
					1790	1791											
V24	U	00000018	1	1905													
V25	U	00000019	1	1906													
V26	U	0000001A	1	1907													
V27	U	0000001B	1	1908													
V28	U	0000001C	1	1909													
V29	U	0000001D	1	1910													
V2ADDR	A	00000010	4	461	589	619	649	679	709	743	773	803	833	863	897	927	957
					987	1017	1051	1081	1111	1141	1171	1205	1235	1265	1295	1325	1359
					1389	1419	1449	1479	1513	1543	1573	1603	1633	1667	1697	1727	1757
					1787												
V3	U	00000003	1	1884													
V30	U	0000001E	1	1911													
V31	U	0000001F	1	1912													
V3ADDR	A	00000014	4	462	591	621	651	681	711	745	775	805	835	865	899	929	959
					989	1019	1053	1083	1113	1143	1173	1207	1237	1267	1297	1327	1361
					1391	1421	1451	1481	1515	1545	1575	1605	1635	1669	1699	1729	1759
					1789												
V4	U	00000004	1	1885													
V5	U	00000005	1	1886													
V6	U	00000006	1	1887													
V7	U	00000007	1	1888													
V8	U	00000008	1	1889													
V9	U	00000009	1	1890													
X0001	U	000002A8	1	199	187	200											
X0002	U	00000358	1	235	223	236											
X1	F	000010E8	4	588	575												
X10	F	00001640	4	862	849												
X11	F	000016D8	4	896	883												
X12	F	00001770	4	926	913												
X13	F	00001808	4	956	943												
X14	F	000018A0	4	986	973												
X15	F	00001938	4	1016	1003												
X16	F	000019D0	4	1050	1037												
X17	F	00001A68	4	1080	1067												
X18	F	00001B00	4	1110	1097												
X19	F	00001B98	4	1140	1127												
X2	F	00001180	4	618	605												
X20	F	00001C30	4	1170	1157												
X21	F	00001CC8	4	1204	1191												
X22	F	00001D60	4	1234	1221												
X23	F	00001DF8	4	1264	1251												
X24	F	00001E90	4	1294	1281												
X25	F	00001F28	4	1324	1311												
X26	F	00001FC0	4	1358	1345												
X27	F	00002058	4	1388	1375												
X28	F	000020F0	4	1418	1405												
X29	F	00002188	4	1448	1435												
X3	F	00001218	4	648	635												
X30	F	00002220	4	1478	1465												
X31	F	000022B8	4	1512	1499												
X32	F	00002350	4	1542	1529												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X33	F	000023E8	4	1572	1559
X34	F	00002480	4	1602	1589
X35	F	00002518	4	1632	1619
X36	F	000025B0	4	1666	1653
X37	F	00002648	4	1696	1683
X38	F	000026E0	4	1726	1713
X39	F	00002778	4	1756	1743
X4	F	000012B0	4	678	665
X40	F	00002810	4	1786	1773
X5	F	00001348	4	708	695
X6	F	000013E0	4	742	729
X7	F	00001478	4	772	759
X8	F	00001510	4	802	789
X9	F	000015A8	4	832	819
XC0001	U	000002D0	1	213	205
XC0002	U	00000380	1	249	241
ZVE7TST	J	00000000	10528	126	129 131 135 139 419 127
=A(E7TESTS)	A	00000534	4	398	255
=AL2(L'MSGMSG)	R	0000053A	2	400	347
=F'1'	F	00000530	4	397	240 290
=F'64'	F	0000052C	4	396	204
=H'0'	H	00000538	2	399	342

MACRO	DEFN	REFERENCES																
FCHECK	79	186	222																
PTTABLE	530	1807																	
VRR_C	485	572	602	632	662	692	726	756	786	816	846	880	910	940	970	1000	1034	1064
		1094	1124	1154	1188	1218	1248	1278	1308	1342	1372	1402	1432	1462	1496	1526	1556	1586
		1616	1650	1680	1710	1740	1770											

DESC	SYMBOL	SIZE	POS	ADDR
Entry: 0				
Image	IMAGE	10528	0000-291F	0000-291F
Region		10528	0000-291F	0000-291F
CSECT	ZVE7TST	10528	0000-291F	0000-291F

STMT   FILE NAME

1   /home/tn529/sharedvfp/tests/zvector-e7-11-logical.asm

** NO ERRORS FOUND **