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LOC	OBJECT CODE	ADDR1	ADDR2	STM		
				52 *****	********	***********
				53 * 54 *	CHECK Macro - Is a Fa	acility Bit set?
				55 *	f the facility bit is	s NOT set, an message is issued and
				56 * 57 *	he test is skipped.	
				58 *	check uses RO, R1 and	d R2
				59 * 60 * eg. 61 *****	CHECK 134, 'vector-pag	cked-decimal'
				61 ****** 62	**************************************	************
				63	CHECK &BITNO, &NOTSETN	
				64 · * 65 · *	&BITM &NOTS	NO : facility bit number to check SETMSG : 'facility name'
				66	CLA &FBBYTE	Facility bit in Byte
				67 68	CLA &FBBIT	Facility bit within Byte
				69	CLA &L(8)	191 hit positions within buts
				70 &L(1) 71		1,2,1 bit positions within byte
				72 &FBBYT 73 &FBBIT	ETA &BITNO/8 ETA &L((&BITNO-(&FBI	RVTF*8))+1)
				74 .*	NOTE 0, 'checking Bit=	-&BITNO: FBBYTE-&FBBYTE, FBBIT-&FBBIT'
				75 76	X&SYSNDX	
				77 * 78 *		Fcheck data area
				79 SKT&SYS		skip messgae tests: '
				80 81	C C&NOTSETMSG C C' (bit &BITNO)	is not installed.'
				82 SKL&SYS	EQU *- SKT&SYSNDX	
				83 * 84	S FD	facility bits gap
				85 FB&SYS	DS 4FD	
				86 87 *	S FD	gap
				88 X&SYSNI 89	QU * A	R&SYSNDX) /8) - 1
				90	TFLE FB&SYSNDX	get facility bits
				91 92	GR RO, RO	
				93	C RO, FB&SYSNDX+&FI	BBYTE get fbit byte is bit set?
				94 95	RO, =F' &FBBIT' NZ XC&SYSNDX	is bit set!
				96 * 97 * facil	bit not set, issue i	message and exit
				98 *		
				99 100	A RO, SKL&SYSNDX A R1, SKT&SYSNDX	message length message address
				101 102	AL R2, MSG	
				103	ЕОЈ	
				104 XC&SYS	EQU * END	
				100		

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LOC	OBJECT CODE	ADDR1	ADDR2	STM				
				107 ******* 108 * 109 *****	Low co	**************************************	***********	
00000000		00000000 00000000	00001AB7	110 ZVE7TST 111	START		Low core addressability	
		00000140	00000000	112 113 SVOLDPSV	N EQU	ZVE7TST+X' 140'	z/Arch Supervisor call old PSW	
	00000001 80000000 00000000 00000200	00000000	000001A0	115 116 117	ORG DC DC	ZVE7TST+X' 1A0' X' 000000018000000 AD(BEGIN)	z/Architecure RESTART PSW 00'	
000001110	0000000			11,	DC	AD (DEGIN)		
	00020001 80000000 00000000 0000DEAD	000001B0	000001D0	119 120 121	ORG DC DC	ZVE7TST+X' 1D0' X' 000200018000000 AD(X' DEAD')	z/Architecure PROGRAM CHECK PSW 00'	
000001E0		000001E0	00000200	123	ORG	ZVE7TST+X' 200'	Start of actual test program	
				125 ******* 126 * 127 ******	*****	**************************************	**************************************	
				130 * Regis	tecture ster Us	e Mode: z/Arch age:		
				131 * 132 * R0 133 * R1-4		work) work)		
				134 * R5 135 * R6-R 136 * R8	R7 (1	esting control tal work) irst base registen	ole - current test base	
				137 * R9 138 * R10	So Tl	econd base registe hird base register	er	
				139 * R11 140 * R12 141 * R13	E'	7TEST call return 7TESTS register work)		
				142 * R14 143 * R15 144 *	Se	ubroutine call econdary Subroutin	ne call or work	
00000200		00000200		145 ******* 147			FIRST Base Register	
00000200 00000200		00001200 00002200		148 149	USI NG	BEGI N+4096, R9	SECOND Base Register THIRD Base Register	
00000202				151 BEGIN 152 153	BALR BCTR BCTR	R8, 0	Initalize FIRST base register Initalize FIRST base register Initalize FIRST base register	
	4190 8800 4190 9800		00000800 00000800	155 156 157	LA LA	R9, 2048(, R8) R9, 2048(, R9)	Initalize SECOND base register Initalize SECOND base register	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				225 ******* 226 * resul	****** t not a	as expected:	************	
				227 * 228 * 229 ******	*****	and instruction	est number, instruction under test n i2 **************	
00000304	45F0 8126	00000304	00000001 00000326	230 FAILMSG 231	EQU BAL	* R15, RPTERROR		
				234 * conti	nue aft	ter a failed tes		
00000308	5800 82B4	00000308	00000001 000004B4	235 ******* 236 FAILCON 237		**************************************	**************************************	
0000030C 00000310	5000 8E00 41C0 C004		00001000 00000004	238 239 240	ST LA	RO, FAILED R12, 4(0, R12)	next test address	
00000314			000002D4	241	В	NEXTE7	next test dudiess	
						**************************************	**************************************	
00000318 0000031C	5810 8E00 1211	00000318	00000001 00001000	246 ENDTEST 247 248	EQU L LTR	* R1, FAILED R1, R1	did a test fail?	
0000031E 00000322	4780 8288 47F0 82A0		00000488 000004A0	249 250	BZ B	EOJ FAI LTEST	No, exit Yes, exit with BAD PSW	

F' 0'

2D' 0'

R5 save area

RO-R2 save area for MSG call

292 RPTSVR5

294 RPTDWSAV DC

000003A8

000003B0

0000000

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LOC	OBJECT CODE	ADDR1	ADDR2	STM			
				296 ******** 297 * 298 * 299 ******		HERCULES MESSAGE poin R2 = return address	**************************************
000003C0 000003C4	4900 82B8 07D2		000004B8	301 MSG 302	CH BNHR	RO, =H' O' R2	Do we even HAVE a message? No, ignore
000003C6	9002 81FC		000003FC	304	STM	RO, R2, MSGSAVE	Save registers
000003CA 000003CE 000003D2	4900 82BA 47D0 81D6 4100 005F		000004BA 000003D6 000005F	306 307 308	CH BNH LA	RO, =AL2(L' MSGMSG) MSGOK RO, L' MSGMSG	Message length within limits? Yes, continue No, set to maximum
000003D6 000003D8 000003DA	1820 0620 4420 8208		00000408	310 MSGOK 311 312	LR BCTR EX	R2, R0 R2, 0 R2, MSGMVC	Copy length to work register Minus-1 for execute Copy message to O/P buffer
000003DE 000003E2	4120 200A 4110 820E		0000000A 0000040E	314 315	LA LA	R2, 1+L' MSGCMD(, R2) R1, MSGCMD	Calculate true command length Point to true command
000003E6 000003EA	83120008 4780 81F6		000003F6	317 318	DC BZ	X' 83' , X' 12' , X' 0008' MSGRET	Issue Hercules Diagnose X'008' Return if successful
000003EE 000003F0	1222 4780 81F6		000003F6	319 320 321	LTR BZ	R2, R2 MSGRET	Is Diag8 Ry (R2) 0? an error occurred but coninue
000003F4	0000			322 323	DC	Н' О'	CRASH for debugging purposes
000003F6 000003FA	9802 81FC 07F2		000003FC	325 MSGRET 326	LM BR	RO, R2, MSGSAVE R2	Restore registers Return to caller
000003FC	00000000 00000000			328 MSGSAVE		3F' 0'	Registers save area
00000408	D200 8217 1000	00000417	0000000	329 MSGMVC	MVC	MSGMSG(0), 0(R1)	Executed instruction
0000040E 00000417	D4E2C7D5 D6C8405C 40404040 40404040			331 MSGCMD 332 MSGMSG 333	DC DC	C' MSGNOH * ' CL95' '	*** HERCULES MESSAGE COMMAND *** The message text to be displayed

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				

00000478	00020001 80000000			339	EOJPSW	DC	OD' O' , X' 000200	018000000', AD(0)
00000488	B2B2 8278		00000478	341	E0J	LPSWE	E0JPSW	Normal completion
00000490	00020001 80000000			343	FAILPSW	DC	0D' 0' . X' 000200	018000000', AD(X'BAD')
	B2B2 8290		00000490		FAI LTEST			Abnormal termination
00000 1110			00000100	010				ADNOTHET COTHE MCCTON
				348	****** * *****		**************************************	***********
000004A4 000004A8	00000000 0000000			351 352	CTLRO	DS DS	F F	CRO
000004AC				354		LTORG		Literals pool
000004AC 000004B0 000004B4	00000040 00001A60 00000001			355 356 357		LIONG	=F' 64' =A(E7TESTS) =F' 1'	nicerary poor
000004B8 000004BA	0000 005F			358 359 360			=H' 0' =AL2(L' MSGMSG)	
				361 362		some o	constants	
		00000400 00001000 00010000 00100000	0000001	365 366	PAGE K64	EQU EQU EQU EQU	1024 (4*K) (64*K) (K*K)	One KB Size of one page 64 KB 1 MB
		AABBCCDD 000000DD	00000001 00000001		REG2PATT REG2LOW		X' AABBCCDD' X' DD'	Polluted Register pattern (last byte above)

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LOC	OBJECT CODE	ADDR1	ADDR2	STM			
				415 *	E7TES	T DSECT	**************************************
00000000 00000004	00000000 0000			418 E7TEST 419 TSUB 420 TNUM	DSECT DC DC	A(0) H' 00'	pointer to test Test Number
00000006 00000007	00			421 422 423 M4	DC DC	X' 00' HL1' 00'	m4 field
00000007	0000			424 I2 425	DC	HL2' 00'	i2 used
0000000A 00000014 00000018 0000001C	0000000 0000000 0000000			426 OPNAME 427 V2ADDR 428 V3ADDR 429 RELEN	DC DC DC DC	CL8' ' A(0) A(0) A(0)	E7 name address of v2 source address of v3 source RESULT LENGTH
00000020 00000028 00000030 00000040	00000000 00000000 00000000 00000000 000000			430 READDR 431 432 V10UTPUT 433	DC DS I DS DS	A(0) FD XL16 FD	result (expected) address gap V1 Output gap
				434 435 * 436 *	test	routine will be	e here (from VRI-c macro)
				437 * 438 *	follo	wed by EXPECTED RESUI	LT
000010C4		00000000	00001AB7	440 ZVE7TST 441	CSECT DS	OF	
				443 ******** 444 * M 445 ******	****** acros t *****	**************************************	**************************************
				449 *	•	nerate individ	ual test
				450 * Hexi do 451 * 452			
				453 454 .* 455 .*		&INST, &I2, &M4	&INST - VRI-c instruction under test &i2 - i2 index
				456 . * 457 458 459 &TNUM		&TNUM &TNUM+1	&m4 - m4 element size control
				460 461 462	DS USING	OFD *, R 5	base for test data and test routine
				463 464 T&TNUM	DC	A(X&TNUM)	address of test routine

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LOC	OBJECT CODE	ADDR1	ADDR2	STM				
				465 466			H' &TNUM' X' 00'	test number
				467		DC	HL1'&M4'	m3 field
				468 469		DC DC	HL2' &I 2' CL8' &I NST'	i2 used instruction name
				470		DC	A(RE&TNUM+16)	address of v2 source
				471 472		DC DC	A(RE&TNUM+32) A(16)	address of v3 source result length
					REA&TNUM		A(RE&TNUM)	result address
				474 475	V10&TNUM	DS DS	FD XL16	gap V1 output
				476		DS	FD	gap
				477 478	*			
				479	X&TNUM	DS	0F	
				480 481		VL	V22, V1FUDGE	
				482			R1, V2ADDR	load v2 source
				483 484		VL	v23, 0(R1)	use v23 to test decoder
				485 486		&I NST	V22, v23, &I 2, &M4	test instruction (dest is a source)
				487		VST	V22, V10&TNUM	save v1 output
				488 489		BR	R11	return
					RE&TNUM	DC	0F	xl16 expected result
				491		DDOD	De	•
				492 493		DROP MEND	KO	
				494	*			
				495 496	* macro t	o gene	erate table of po	inters to individual tests
				497		MACRO	r D	
				498 499		PTTABI GBLA	LE &TNUM	
				500		LCLA	&CUR	
				501 502	&CUR	SETA	1	
				503	TTABLE	DS	0F	
				504 505		ANOP		
				506		DC	A(T&CUR)	
				507 508		SFTA	&CUR+1	
				509		AIF	(&CUR LE &TNUM).	LOOP
				510 511		DC	A(0)	END OF TABLE
				512		DC DC	A(0) A(0)	END OF TABLE
				513 514	*	MEND		
				514		TATE TATA		

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LOC	OBJECT CODE	ADDR1	ADDR2	STM				
				517 ******	*****	******	************	
				518 *	E7 VR	I-c tests	***********	
				520	PRINT			
				521 *				
				522 * E74D 523 *	VREP	- Vector Repl	licate	
				524 *	VRI_C	instruction,	I2, M4	
				525 * 526 *		followed by	pected result (V1)	
				527 *		16 byte V3	source (referenced as V2)	
				528 *	Vac			
				529 * VREP 530 *	- vec	tor Replicate 		
				531 * Byte	UDI C	AMPER O O		
00010C8				532 533+	VRI_C DS	VREP, 0, 0 OFD		
00010C8		000010C8		534 +	USING	*, R 5	base for test data and test routine	
00010C8 00010CC	00001110 0001			535+T1 536+	DC DC	A(X1) H' 1'	address of test routine test number	
00010CE	0001			537+	DC	X' 00'		
00010CF	00			538+	DC DC	HL1'0'	m3 field	
00010D0 00010D2	0000 E5D9C5D7 40404040			539+ 540+	DC DC	HL2' 0' CL8' VREP'	i2 used instruction name	
00010DC	00001140			541 +	DC	A(RE1+16)	address of v2 source	
00010E0 00010E4	00001150 00000010			542+ 543+	DC DC	A(RE1+32) A(16)	address of v3 source result length	
00010E8	00001130			544+REA1	DC	A(RE1)	result address	
00010F0 00010F8	00000000 00000000 0000000 00000000			545+ 546+V101	DS DS	FD XL16	gap V1 output	
0001100	0000000 00000000						VI oucput	
0001108	00000000 00000000			547+ 548+*	DS	FD	gap	
0001110				549+X1	DS	OF		
0001110	E760 8EA4 0806		000010A4	550+	VL	V22, V1FUDGE	1 1 0	
00001116 0000111C	E310 5014 0014 E771 0000 0806		00000014 00000000	551+ 552+	LGF VL	R1, V2ADDR v23, O(R1)	load v2 source use v23 to test decoder	
0001122	E767 0000 0C4D		00001000	553 +	VREP	V22, v23, 0, 0	test instruction (dest is a source)	
0001128 000112E	E760 5030 080E 07FB		000010F8	554+ 555+	VST BR	V22, V101 R11	save v1 output return	
0001130	***			556+RE1	DC	0F	xl16 expected result	
0001130 0001130	0000000 00000000			557+ 558	DROP DC	R5 XL16' 00000000	00000000 00000000 00000000' result	
0001138	0000000 00000000							
0001140 0001148	00010101 01010101 01010101 01010101			559	DC	XL16' 00010101	01010101 01010101 01010101' v3	
0001140	OTOTOTOL OTOTOTOL			560				
0001150				561		VREP, 1, 0		
0001150 0001150		00001150		562+ 563+	DS USING	OFD *, R5	base for test data and test routine	
0001150	00001198	-		564+T2	DC	A(X2)	address of test routine	
0001154 0001156	0002 00			565+ 566+	DC DC	H' 2' X' 00'	test number	
0001157	00			567 +	DC	HL1' 0'	m3 field	
00001158 0000115A	0001 E5D9C5D7 40404040			568+ 569+	DC DC	HL2' 1' CL8' VREP'	i2 used instruction name	
OUDITUR	LUDUCUDI TUTUTUTU			0001	DC		I HOU WOU OH HAIR	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI			
00001164	000011C8			570 +	DC	A(RE2+16)	address of v2 source
00001168	000011D8			571+	DC	A(RE2+32)	address of v3 source
0000116C	00000010			572+	DC	A(16)	result length
00001170	000011B8			573+REA2	DC	A(RE2)	result address
00001178	00000000 00000000			574+	DS	FD	gap V1 output
00001180 00001188	00000000 00000000 0000000 00000000			575+V102	DS	XL16	vi output
00001100	0000000 0000000			576 +	DS	FD	gap
				577+*			
00001198	T700 0T14 0000		00004044	578+X2	DS	OF	
00001198	E760 8EA4 0806		000010A4	579+	VL	V22, V1FUDGE	1 1 0
0000119E	E310 5014 0014		00000014	580+	LGF	R1, V2ADDR	load v2 source
000011A4	E771 0000 0806		0000000	581+	VL	v23, 0(R1)	use v23 to test decoder
000011AA 000011B0	E767 0001 0C4D E760 5030 080E		00001180	582+ 583+	VREP VST	V22, v23, 1, 0	test instruction (dest is a source)
000011B0 000011B6	07FB		00001100	584+	BR	V22, V102 R11	save v1 output return
000011B0 000011B8	U/FB			585+RE2	DC DC	OF	xl16 expected result
000011B8				586+	DROP	R5	xi io expected resurt
000011B8	01010101 01010101			587	DC		01010101 01010101 01010101' result
000011B0	01010101 01010101			307	ьс	ALIO OIOIOIOI	olololol olololol olololol lesule
000011C8	00010101 01010101			588	DC	XL16' 00010101	01010101 01010101 01010101' v3
000011D0	01010101 01010101			000	20	ALIO OCCIOIOI	
				589			
				590	VRI C	VREP, 2, 0	
000011D8				591 +	DS _	OFD	
000011D8		000011D8		592 +	USING	*, R 5	base for test data and test routine
000011D8	00001220			593+T3	DC	A(X3)	address of test routine
000011DC	0003			594 +	DC	H' 3'	test number
000011DE	00			595 +	DC	X' 00'	
000011DF	00			596 +	DC	HL1' 0'	m3 field
000011E0	0002			597+	DC	HL2' 2'	i 2 used
000011E2	E5D9C5D7 40404040			598+	DC	CL8' VREP'	instruction name
000011EC	00001250			599+	DC	A(RE3+16)	address of v2 source
000011F0 000011F4	00001260			600+ 601+	DC DC	A(RE3+32)	address of v3 source
000011F4	00000010 00001240			602+REA3	DC DC	A(16) A(RE3)	result length result address
00001116	00001240			602+REAS	DS DS	FD	
00001200	0000000 0000000			604+V103	DS DS	XL16	gap V1 output
00001200	0000000 00000000			00411100	DS	ALIU	VI oucput
00001218	0000000 00000000			605 +	DS	FD	gap
				606+*	· 		O' I
00001220				607+X3	DS	0F	
00001220	E760 8EA4 0806		000010A4	608 +	VL	V22, V1FUDGE	
00001226	E310 5014 0014		0000014	609 +	LGF	R1, V2ADDR	load v2 source
0000122C	E771 0000 0806		0000000	610+	VL_	v23, 0(R1)	use v23 to test decoder
00001232	E767 0002 0C4D		00001555	611+		V22, v23, 2, 0	test instruction (dest is a source)
00001238	E760 9008 080E		00001208	612+	VST	V22, V103	save v1 output
0000123E	07FB			613+	BR	R11	return
00001240				614+RE3	DC	OF	xl16 expected result
00001240	09090909 09090909			615+ 616		R5	02020202 02020202 020202021 +
$00001240 \\ 00001248$	02020202 02020202 02020202 02020202			616	DC	ALIU UZUZUZUZ	02020202 02020202 02020202' result
00001248	01010201 01010101			617	DC	YI 16' 01010901	01010101 01010101 01010101' v3
00001250	01010201 01010101			UII	ъС	ALIU UIUIU&UI	OTOTOTOL OTOTOLOL OTOTOLOL VS
00001200	01010101 01010101			618			
				619	VRT C	VREP, 7, 0	
				010	, IVI _C		

R11

return

BR

671 +

0000134E

07FB

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00001350				672+RE5	DC	OF	xl16 expected result			
00001350 00001350	FOFOFOFO FOFOFOFO			673+ 674	DROP DC	R5	FOFOFO FOFOFOFO FOFOFOFO'	rocul t		
	FOFOFOFO FOFOFOFO			074	DC	ALIO FUFUFUFU FU	rororo rorororo rorororo	resurt		
00001360	01010201 01010102			675	DC	XL16' 01010201 01	010102 01010101 010101F0'	$\mathbf{v3}$		
00001368	01010101 010101F0			676						
				677 *Halfword	d					
00004070				678		VREP, 0, 1				
00001370 00001370		00001370		679+ 680+	DS USING	0FD * P5	base for test data and t	tost routi	nα	
00001370	000013B8	00001370		681+T6	DC	A(X6)	address of test routine	test Touti	iie	
00001374	0006			682+	DC	H' 6'	test number			
00001376 00001377	00 01			683+ 684+	DC DC	X' 00' HL1' 1'	m3 field			
00001377	0000			685+	DC DC	HL2' 0'	i 2 used			
0000137A	E5D9C5D7 40404040			686+	DC	CL8' VREP'	instruction name			
00001384 00001388	000013E8 000013F8			687+ 688+	DC DC	A(RE6+16) A(RE6+32)	address of v2 source address of v3 source			
0000138C	00000010			689+	DC	A(16)	result length			
00001390	000013D8			690+REA6	DC	A(RE6)	result address			
00001398 000013A0	00000000 00000000 0000000 00000000			691+ 692+V106	DS DS	FD XL16	gap V1 output			
000013A8	0000000 00000000			00211100			VI oucput			
000013B0	00000000 00000000			693+ 694+*	DS	FD	gap			
000013B8				695+X6	DS	0F				
000013B8	E760 8EA4 0806		000010A4	696 +	VL	V22, V1FUDGE				
000013BE 000013C4	E310 5014 0014 E771 0000 0806		00000014 00000000	697+ 698+	LGF VL	R1, V2ADDR v23, O(R1)	load v2 source use v23 to test decoder			
000013C4 000013CA	E767 0000 1C4D		0000000	699+	VE VREP	V23, U(R1) V22, v23, 0, 1	test instruction (dest	is a sour	ce)	
000013D0	E760 5030 080E		000013A0	700+	VST	V22, V106	save v1 output			
000013D6 000013D8	07FB			701+ 702+RE6	BR DC	R11 0F	return xl16 expected result			
000013D8 000013D8				702+RE0 703+		R5	Al lo expected l'esult			
000013D8	0000000 00000000			704	DC	XL16' 00000000 00	000000 00000000 00000000'	resul t		
000013E0 000013E8	00000000 00000000 00000101 01010101			705	DC	XI.16' 00000101 01	010101 01010101 01010101'	v3		
	01010101 01010101					ALIO OUUUUUU UI	010101 01010101 01010101	V O		
				706 707	VDT C	VDED 1 1				
000013F8				707 708+	DS DS	VREP, 1, 1 OFD				
000013F8		000013F8		709 +	USING	*, R 5	base for test data and t	test routi	ne	
000013F8	00001440			710+T7	DC	A(X7)	address of test routine			
000013FC 000013FE	0007 00			711+ 712+	DC DC	H' 7' X' 00'	test number			
000013FF	01			713+	DC	HL1' 1'	m3 field			
00001400 00001402	0001 E5D9C5D7 40404040			714+ 715+	DC DC	HL2' 1' CL8' VREP'	i2 used instruction name			
00001402 0000140C	00001470			715+ 716+	DC DC	A(RE7+16)	address of v2 source			
00001410	00001480			717+	DC	A(RE7+32)	address of v3 source			
00001414 00001418	00000010 00001460			718+ 719+REA7	DC DC	A(16) A(RE7)	result length result address			
00001418	0000000 00000000			719+KEA7 720+	DS	FD				
00001428 00001430	00000000 00000000 00000000 00000000			721+V107	DS	XL16	gap V1 output			

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI				
00001438	00000000 00000000			722+ 723+*	DS	FD	gap	
00001440 00001440	E760 8EA4 0806		000010A4	724+X7 725+	DS VL	OF V22, V1FUDGE		
00001446 0000144C	E310 5014 0014 E771 0000 0806		00000014 00000000	726+ 727+	LGF VL	R1, V2ADDR v23, O(R1)	load v2 source use v23 to test decoder	
0000144C 00001452 00001458	E767 0000 0806 E767 0001 1C4D E760 5030 080E		00001428	727+ 728+ 729+	VREP VST	V23, U(N1) V22, v23, 1, 1 V22, V107	test instruction (dest is a source) save v1 output	
0000145E	07FB		00001420	730 +	BR	R11	return	
00001460 00001460				731+RE7 732+	DC DROP	0F R5	xl16 expected result	
00001460	B109B109 B109B109			733	DC		9B109 B109B109 B109B109' result	
00001468 00001470	B109B109 B109B109 0001B109 01010101			734	DC	VI 16' 0001R100 010	10101 01010101 01010101' v3	
00001470	01010101 01010101			734	DC	ALIO UUUIBIU9 UIU	10101 01010101 01010101 V3	
				735 736	VDT C	VDED 9 1		
00001480				730 737+	DS DS	VREP, 2, 1 OFD		
00001480	00001460	00001480		738+	USING		base for test data and test routine	
00001480 00001484	000014C8 0008			739+T8 740+	DC DC	A(X8) H' 8'	address of test routine test number	
00001486	00			741 +	DC	X' 00'		
00001487 00001488	01 0002			742+ 743+	DC DC	HL1' 1' HL2' 2'	m3 field i2 used	
0000148A	E5D9C5D7 40404040			744 +	DC	CL8' VREP'	instruction name	
00001494 00001498	000014F8 00001508			745+ 746+	DC DC	A(RE8+16) A(RE8+32)	address of v2 source address of v3 source	
0000149C 000014A0	0000100 000014E8			747+ 748+REA8	DC DC	A(16) A(RE8)	result length result address	
000014A8	0000000 00000000			749+	DS	FD	gap	
000014B0 000014B8	00000000 00000000 0000000 00000000			750+V108	DS	XL16	V1 output	
000014C0	00000000 00000000			751+ 752+*	DS	FD	gap	
000014C8 000014C8	E760 8EA4 0806		000010A4	753+X8 754+	DS VL	OF V22, V1FUDGE		
000014C8 000014CE	E310 5014 0014		00001044	755+	LGF	R1, V2ADDR	load v2 source	
000014D4	E771 0000 0806		0000000	756+	VL	v23, 0(R1)	use v23 to test decoder	
000014DA 000014E0	E767 0002 1C4D E760 5030 080E		000014B0	757+ 75 8 +	VREP VST	V22, v23, 2, 1 V22, V108	test instruction (dest is a source) save v1 output	
000014E6	07FB			759 +	BR	R11	return	
000014E8 000014E8				760+RE8 761+	DC DROP	OF R5	xl16 expected result	
000014E8	07770777 07770777			762	DC		70777 07770777 07770777' result	
000014F0 000014F8 00001500	07770777 07770777 01010201 07770101 01010101 01010101			763	DC	XL16' 01010201 077	70101 01010101 01010101' v3	
00001508				764 765 766+	VRI_C DS	VREP, 4, 1 OFD		
00001508		00001508		767+	USING	*, R 5	base for test data and test routine	
00001508 0000150C	00001550 0009			768+T9 769+	DC DC	A(X9) H' 9'	address of test routine test number	
0000150E	00			770+	DC	X' 00'		
0000150F 00001510	01 0004			771+ 772+	DC DC	HL1' 1' HL2' 4'	m3 field i2 used	
00001310	UUU '1			1167	DC	IILA T	1& useu	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI			
00001512	E5D9C5D7 40404040			773+	DC	CL8' VREP'	instruction name
0000151C	00001580			774+	DC	A(RE9+16)	address of v2 source
00001520	00001590			775+	DC	A(RE9+32)	address of v3 source
00001524	00000010			776+	DC	A(16)	result length
00001528	00001570			777+REA9	DC	A(RE9)	result address
00001520	00000000 00000000			778+	DS	FD	
00001538	0000000 0000000			779+V109	DS DS	XL16	gap V1 output
00001538	0000000 0000000			773+7103	DЗ	ALIU	vi oucpuc
00001548	0000000 0000000			780+	DS	FD	dan
00001346	0000000 00000000			780+ 781+*	DЗ	ГU	gap
00001550				781+ ⁷ 782+X9	DC	0F	
00001550	E700 OEAA 0000		00001014		DS		
00001550	E760 8EA4 0806		000010A4	783+	VL	V22, V1FUDGE	1 1 0
00001556	E310 5014 0014		00000014	784+	LGF	R1, V2ADDR	load v2 source
0000155C	E771 0000 0806		00000000	785+	VL	v23, 0(R1)	use v23 to test decoder
00001562	E767 0004 1C4D		00004700	786 +	VREP	V22, v23, 4, 1	test instruction (dest is a source)
00001568	E760 5030 080E		00001538	787 +	VST	V22, V109	save v1 output
0000156E	O7FB			788+	BR	R11	return
00001570				789+RE9	DC	0F	xl16 expected result
00001570				790 +	DROP	R5	
00001570	FFA1FFA1 FFA1FFA1			791	DC	XL16' FFA1FFA1	FFA1FFA1 FFA1FFA1' result
00001578	FFA1FFA1 FFA1FFA1						
00001580	01010201 07770101			792	DC	XL16' 01010201	07770101 FFA10101 01010101' v3
00001588	FFA10101 01010101						
				793			
				794	VRI C	VREP, 7, 1	
00001590				795 +	DS _	OFD	
00001590		00001590		796 +	USING	*, R 5	base for test data and test routine
00001590	000015D8			797+T10	DC	A(X10)	address of test routine
00001594	000A			798 +	DC	H' 10'	test number
00001596	00			799+	DC	X' 00'	
00001597	01			800+	DC	HL1' 1'	m3 field
00001598	0007			801+	DC	HL2' 7'	i 2 used
0000159A	E5D9C5D7 40404040			802+	DC	CL8' VREP'	instruction name
000015A4	00001608			803+	DC	A(RE10+16)	address of v2 source
000015A8	00001618			804+	DC	A(RE10+32)	address of v3 source
000015AC	00000010			805+	DC	A(16)	result length
000015RC	000015F8			806+REA10	DC	A(RE10)	result address
000015B8	0000000 00000000			807+	DS	FD	
00015E0	0000000 00000000			808+V1010	DS	XL16	gap V1 output
00015C8	0000000 0000000			000+11010	DS	ALIU	VI output
00015C8	0000000 0000000			809+	DS	FD	dan
70001300				810+*	טע	ı·ν	gap
100015DO					DC	OF	
00015D8	EZCO OELA OOOC		00001014	811+X10	DS	OF	
000015D8	E760 8EA4 0806		000010A4	812+	VL	V22, V1FUDGE	land vo games
000015DE	E310 5014 0014		00000014	813+	LGF	R1, V2ADDR	load v2 source
000015E4	E771 0000 0806		0000000	814+	VL	v23, 0(R1)	use v23 to test decoder
000015EA	E767 0007 1C4D		00001700	815+	VREP	V22, v23, 7, 1	test instruction (dest is a source)
000015F0	E760 5030 080E		000015C0	816+	VST	V22, V1010	save v1 output
000015F6	07FB			817+	BR	R11	return
000015F8				818+RE10	DC	0F	xl16 expected result
000015F8				819+	DROP	R5	
000015F8	FOFOFOFO FOFOFOFO			820	DC	XL16' F0F0F0F0	FOFOFOFO FOFOFOFO' result
00001600	FOFOFOFO FOFOFOFO						
00001608	01010201 010101F0			821	DC	XL16' 01010201	010101F0 01010101 0101F0F0' v3
00001610	01010101 0101F0F0						
				822			

VREP

V22, v23, 1, 2

test instruction (dest is a source)

874 +

000016FA E767 0001 2C4D

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI			
00001700 00001706	E760 5030 080E 07FB		000016D0	875+ 876+	VST BR	V22, V1012 R11	save v1 output return
00001700	UTTD			877+RE12	DC	OF	xl16 expected result
00001708				878 +	DROP	R5	•
00001708 00001710	01077101 01077101 01077101			879	DC	XL16' 01077101	01077101 01077101 01077101' result
00001718	0001B109 01077101 01010101 01010101			880	DC	XL16' 0001B109	01077101 01010101 01010101' v3
00001728				881 882 883+	VRI_C DS	VREP, 2, 2 OFD	
00001728		00001728		884+	USING	*, R 5	base for test data and test routine
00001728	00001770			885+T13	DC	A(X13)	address of test routine
0000172C 0000172E	000D 00			886+ 887+	DC DC	H' 13' X' 00'	test number
0000172F	02			888+	DC	HL1' 2'	m3 field
00001730 00001732	0002 E5D9C5D7 40404040			889+ 890+	DC DC	HL2' 2' CL8' VREP'	i 2 used
00001732 0000173C	000017A0			891+	DC DC	A(RE13+16)	instruction name address of v2 source
00001740	000017B0			892+	DC	A(RE13+32)	address of v3 source
00001744 00001748	00000010 00001790			893+ 894+REA13	DC DC	A(16) A(RE13)	result length result address
00001748	00001790			895+	DS DS	FD	gap
00001758	00000000 00000000			896+V1013	DS	XL16	V1 output
00001760 00001768	00000000 00000000 0000000 00000000			897+	DS	FD	dan
00001708	0000000 0000000			898+*	DO	T.D	gap
00001770	T700 0T14 0000		00001014	899+X13	DS	OF	
00001770 00001776	E760 8EA4 0806 E310 5014 0014		000010A4 00000014	900+ 901+	VL LGF	V22, V1FUDGE R1, V2ADDR	load v2 source
0000177C	E771 0000 0806		00000000	902+	VL	v23, 0(R1)	use v23 to test decoder
00001782	E767 0002 2C4D		00001750	903+	VREP	V22, v23, 2, 2	test instruction (dest is a source)
0000178E	E760 5030 080E 07FB		00001758	904+ 905+	VST BR	V22, V1013 R11	save v1 output return
00001790	0.12			906+RE13	DC	0F	xl16 expected result
00001790 00001790	A010101A A010101A			907+ 908	DROP DC	R5	A010101A A010101A A010101A' result
00001790	A010101A A010101A A010101A A010101A			900	DC	ALIO AUIUIUIA	AUTOTOTA AUTOTOTA TESUTE
	01010201 07770101 A010101A 01010101			909	DC	XL16' 01010201	07770101 A010101A 01010101' v3
				910	UDI C	VDED 0 0	
000017B0				911 912+	VRI_C DS	VREP, 3, 2 OFD	
000017B0		000017B0		913+	USING		base for test data and test routine
000017B0	000017F8			914+T14	DC	A(X14)	address of test routine
000017B4 000017B6	000E 00			915+ 916+	DC DC	H' 14' X' 00'	test number
000017B7	02			917+	DC	HL1' 2'	m3 field
000017B8	0003 E5D0C5D7 40404040			918+	DC	HL2'3'	i 2 used
000017BA 000017C4	E5D9C5D7 40404040 00001828			919+ 920+	DC DC	CL8' VREP' A(RE14+16)	instruction name address of v2 source
000017C8	00001838			921+	DC	A(RE14+32)	address of v3 source
000017CC	0000010			922+	DC	A(16)	result length
000017D0 000017D8 000017E0	00001818 00000000 00000000 00000000 00000000			923+REA14 924+ 925+V1014	DC DS DS	A(RE14) FD XL16	result address gap V1 output
OUUITEU				080111017	DO	ALIU	11 Oucput

0001778	ASMA Ver.	0. 7. 0 zvector- e7- 2	22- VREP					03 Apr 2025 15: 40: 44 Page	22
10017F2	LOC	OBJECT CODE	ADDR1	ADDR2	STMI				
1927 1927 1927 1927 1927 1927 1928	000017E8								
0001178 0001178 0000104 929-4 VI. V22. VIFIDGE 00001778 00001778 00001778 00000000 00000000 00000000 000000	000017F0	00000000 00000000				DS	FD	gap	
10001781 2310 5014 0014 00000010 930+ CF R1, V2ADPR 1000 42 source 1000180 1771 0000 0806 000000000 931+ VIL V	000017F8				928+X14				
0001840 F771 0000 0806 00000000 931+ VL V23, 0(R1) use v23 to test decoder test instruction (dest is a source) 932+ VREP VZ2, v23, 3, v27 v22, v23, 0; use v23 to test decoder test instruction (dest is a source) 932+ VREP VZ2, v23, 0; use v2 output vertical variable variab								1 1 0	
1001810 1767 1003 2C4B 932-									
0001818 Feb 5030 808E 000017E0 933+ SE 1 1 1 1 1 1 1 1 1				0000000			V23, U(K1) V22 v23 3 2		
OOD 18 OOD 18 OF OF OF OF OF OF OF O				000017E0					
1001818 0001818 0001818 0001818 0001818 0001818 0001818 0001818 0001820 0001	00001816			00001120					
	00001818								
0001830 FA10101 B0B0A1A1 B0B0A1A1 S0B0A1A1 SOB0A1A1 SO	00001818					DROP			
ORDINS FAIOLO ORDINA O	00001818				937	DC	XL16' BOBOA1A1 B	OBOA1A1 BOBOA1A1 BOBOA1A1' result	
939 940 941	00001820					~~			
940 940 940 940 940 940 941					938	DC	XL16' 01010201 0	7770101 FFA10101 B0B0A1A1' v3	
940 *Word 941	00001830	FFAIUIUI BUBUAIAI			020				
941 VRI C VREP, 0.3									
0001838						VRT C	VREP 0 3		
0001838	00001838								
0001838 00001880 000F 945+ DC K15' address of test routine 000183E 00 946+ DC K10' test number 0001840 0000 947+ DC HIL1'3' n8 field 0001840 0000 948+ DC HIL2'0' i2 used 0001840 0000 949+ DC K18' RPP' instruction name 0001840 0001857 040404040 950+ DC A(REI5+16) address of v2 source 0001850 000018C0 951+ DC A(REI5+32) address of v3 source 0001850 000018A0 952+ DC A(REI5+32) address of v3 source 0001850 0000000 0000000 0001850 0000000 00000000 954+ DS FD gap 0001880 0000000 00000000 956+ DS FD gap 0001880 0000000 00000000 0001879 0000000 00000000 0001880 0000000 00000000 0001880 E760 8EA4 0806 00010A4 959+ VI. V22, V1FUDGE 0001886 E310 5014 0014 00000014 960+ LGF RI, V2ADDR load v2 source 0001886 E771 0000 0806 0000000 961+ VI. V22, V1FUDGE 0001886 E770 0000 0806 0000000 961+ VI. V22, V1FUDGE 0001886 E760 5030 080E 0000186 963+ VST V22, V23, 0, 3 test instruction (dest is a source) 0001889 F760 5030 080E 0000186 963+ VST V22, V23, 0, 3 test instruction (dest is a source) 0001880 0000010 01010101 0001880 0000010 01010101 0001880 0000010 01010101 0001880 0000010 01010101 0001880 0000010 01010101 0001880 0000010 01010101 0001880 0000010 01010101 0001880 0000010 01010101 0001880 0000000 0000000 00000000 0000000 000000	00001838		00001838					base for test data and test routine	
000183E 00 0001840 000 001840 0000 001840 0000 001840 0000 001840 0000 001840 0000 001840 0000 001840 0000 001840 0000 001840 0000 001840 0000 001840 0000 001840 0000 001850 00001860 0001850 00001860 0001850 00001860 0001850 0000000 0000000 00000000 0000000 000000	00001838	00001880				DC	A(X15)	address of test routine	
0001887 03 947+ DC HL1'3' m8 field 0001840 0000 948+ DC CL8'VREP' instruction name 0001842 E5D9C5D7 40404040 949+ DC CL8'VREP' instruction name 0001840 0001850 0001860 950+ DC A(RE15+16) address of v2 source 0001854 00001850 00001860 951+ DC A(RE15+32) address of v3 source 0001854 00001850 0000000 952+ DC A(RE15+32) address of v3 source 0001850 0000000 0000000 953+REA15 DC A(RE15) result 1 ength 0001860 0000000 00000000 954+ DS FD gap 0001860 0000000 00000000 955+V1015 DS TD gap 0001870 0000000 00000000 955+V1015 DS FD gap 0001870 0000000 00000000 955+V1015 DS FD gap 0001870 0000000 00000000 955+V1015 DS FD gap 0001880 P55+V1015 DS GD FD GAT DE	0000183C							test number	
0001840 0000 948+ DC HL2'0' i2 used 0001840 0001840 949+ DC CL8'VREP' instruction name oblighted by the property of the proper							X' 00'	0.01.1.1	
0001842 E5B9C5D7 40404040 949+ DC CL8'VREP' instruction name 000184C 0001850 000018C0 950+ DC A(RE15+16) address of v2 source 0001850 000018C0 951+ DC A(RE15+32) address of v3 source 0001850 000018C0 0000000 952+ DC A(RE15+32) address of v3 source 0001850 000018C0 0000000 00000000 953+REA15 DC A(RE15) result address 00018C0 00018C0 0000000 00000000 953+REA15 DC A(RE15) result address 00018C0 00018C0 0000000 00000000 955+V1015 DS XL16 VI output 00018C1 956+ DS FD gap 00018C1 957+* 958+X15 DS OF 00018C1 950+ VL V22, VIFUDGE 00018C1 962+ VREP V22, V23, 0, 3 test instruction (dest is a source) 00018C1 966+ DROP R5							HL1'3'		
000184C 000018B0 00018C0 951+ DC A(RE15+16) address of v2 source 0001850 00001850 00001800 952+ DC A(RE15+32) address of v3 source 0001850 0001800 953+REA15 DC A(RE15+32) result length 0001800 0000000 00000000 953+REA15 DC A(RE15+32) gap 0001800 0000000 00000000 00000000 955+V1015 DS XL16 V1 output 0001870 0000000 00000000 00000000 955+V1015 DS XL16 V1 output 0001870 0000000 000000000 956+ DS FD gap 0001800 0000000 00000000 957+* 958+X15 DS OF 0001880 E760 8EA4 0806 0001044 959+ VL V22, V1FUDGE 0001880 E761 0000 0806 0000000 961+ VL V23, 0(R1) use v23 to test decoder 0001882 E767 0000 3C4D 962+ VEEP V22, v23, 0, 3 test instruction (dest is a source) 0001888 E766 5030 080E 0000180 963+ VST V22, V1015 save v1 output 0001800 0001800 0001800 0001800 0001800 0000000 966+ DROP 864+ BR R11 return 0001800 0001800 0000101 01010101 9667 DC XL16' 00000101 01010101 01010101 v3 0001800 0000101 01010101 01010101 967 DC XL16' 00000101 01010101 01010101 v3 0001800 000									
0001850 000018C0 00018C0 00018C0 00018C0 00018C0 00018C0 00018C0 00018C0 000000 0000000 955+ DC A(16) result address 00018C0 0000000 00000000 955+V1015 DS XL16 V1 output 00018C0 0000000 00000000 00000000 955+V1015 DS XL16 V1 output 00018C0 0000000 00000000 00000000 955+V1015 DS XL16 V1 output 00018C0 00018C0 0000000 00000000 00000000 955+V1015 DS XL16 V1 output 00018C0 00018C0 0000000 00000000 955+V1015 DS XL16 V1 output 00018C0 00018C0 00000000 00000000 955+V1015 DS XL16 V1 output 00018C0 00018C0 00000000 00000000 955+V1015 DS XL16 V1 output 00018C0 00018C0 0000000 00000000 955+V1015 DS XL16 V1 output 00000000 955+V1015 DS V1 V22, V1FUDGE 00018C0 00018C0 00018C0 000018C0 0000000 955+V1015 DC A(RE15) DC OF XL16 00000101 01010101 01010101 V3 USE V23 to test decoder 00018C0 00018C0 000018C0 0000									
0001854 00000100 952+ DC A(16) result length 0001858 00001860 00000000 00000000 953+REA15 DC A(RE15) result address 0001860 00000000 00000000 954+ DS FD gap 0001868 00000000 00000000 00000000 00000000 0000									
0001858	00001854								
0001888	00001858	000018A0				DC	A(RE15)	result address	
0001870 0000000 00000000 956+ DS FD gap 0001880 0000000 00000000 957+* 0001880 E760 8EA4 0806 00001044 959+ VL V22, V1FUDGE 0001886 E310 5014 0014 00000014 960+ LGF R1, V2ADDR load v2 source 000188C E771 0000 0806 0000000 961+ VL V23, 0(R1) use v23 to test decoder 000189E E767 0000 3C4D 962+ VREP V22, V23, 0, 3 test instruction (dest is a source) 000189E 076B 963+ VST V22, V1015 save v1 output 000189E 076B 964+ BR R11 return 000180C 966+ DROP R5 000180C 0000101 01010101 000180C 0000101 01010101 000180C 0000180C 0000180C 972+ USING *, R5 base for test data and test routine 00018C0 00018C0 000018C0 973+T16 DC A(X16) address of test routine 00018C0 00018C0 000018C0 000018C0 973+T16 DC R16' test number								gap	
0001878	00001868				955+V1015	DS	XL16	V1 output	
957+* 958+X15 DS OF					050	DC	ED		
958+X15 DS OF OF OF OF OF OF OF O	00001878	0000000 00000000				DS	FD	gap	
0001880 E760 8EA4 0806	00001880					DC	0E		
0001886 E310 5014 0014 0014 00000014 960+ LGF R1, V2ADDR load v2 source 000188C E771 0000 0806 00000000 961+ VL v23, 0(R1) use v23 to test decoder 0001892 E767 0000 3C4D 962+ VREP V22, v23, 0, 3 test instruction (dest is a source) 000189E E760 5030 080E 00001868 963+ VST V22, V1015 save v1 output 000189E 07FB 964+ BR R11 return 00018A0 0000101 01010101 965+RE15 DC 0F xl 16 expected result 00018A0 00000101 01010101 967 DC XL16'00000101 0101010 10000101 0101010' result 00018A0 00000101 01010101 968 DC XL16'00000101 0101010 1010101 01010101 v3 00018B0 0000101 01010101 01010101 968 DC XL16'00000101 0101		F760 8F44 0806		00001044					
000188C E771 0000 0806	00001886							load v2 source	
0001892 E767 0000 3C4D 962+ VREP V22, v23, 0, 3 test instruction (dest is a source) 0001898 E760 5030 080E 00001868 963+ VST V22, V1015 save v1 output 0001840 965+RE15 DC 0F xl16 expected result 00018A0 0000101 01010101 967 DC XL16'00000101 0101010 00000101 0101010' result 00018A0 0000101 01010101 968 DC XL16'00000101 0101010 0101010' v3 00018B0 0000101 01010101 968 DC XL16'00000101 0101010 0101010' v3 00018B0 0101010 01010101 969 970 VRI_C VREP, 0, 3 00018C0 971+ DS 0FD 00018C0 00001908 972+ USING *, R5 base for test data and test routine 00018C0 000018C0 00001908 973+T16 DC A(X16) address of test routine 00018C4 0010 974+ DC H'16' test number	0000188C								
000189E 07FB 964+ BR R11 return 00018A0 965+RE15 DC 0F xl16 expected result 00018A0 966+ DROP R5 00018A8 00000101 0101010 967 DC XL16'00000101 010101 00000101 0101011' result 00018B0 00000101 0101010 968 DC XL16'00000101 0101010 01010101 01010101' v3 00018B8 01010101 0101010 969 970 VRI_C VREP, 0, 3 00018C0 971+ DS 0FD 00018C0 000018C0 972+ USING *, R5 base for test data and test routine 00018C0 00001908 973+T16 DC A(X16) address of test routine 00018C4 0010 974+ DC H'16' test number	00001892					VREP	V22, v23, 0, 3		
00018A0 965+RE15 DC 0F xl16 expected result 00018A0 966+ DROP R5 00018A0 00000101 01010101 967 DC XL16'00000101 01010101 00000101 01010101	00001898			00001868					
00018A0		07FB							
00018A0 00000101 01010101 967 DC XL16'00000101 01010101 00000101 ' result 00018B0 00000101 01010101 968 DC XL16'00000101 0101010 0101010 1 0101010 1 0101010 1 v3 00018B8 01010101 969 970 VRI_C VREP, 0, 3 00018C0 971+ DS 0FD 00018C0 972+ USING *, R5 base for test data and test routine 00018C0 00001908 973+T16 DC A(X16) address of test routine 00018C4 0010 974+ DC H'16' test number								x116 expected result	
00018A8 00000101 01010101 968 DC XL16' 00000101 01010101 01010101 ' v3 00018B8 01010101 01010101 969 970 VRI_C VREP, 0, 3 00018C0 971+ DS 0FD 00018C0 972+ USING *, R5 base for test data and test routine 00018C0 00001908 973+T16 DC A(X16) address of test routine 00018C4 0010 974+ DC H' 16' test number		00000101 01010101						1010101 00000101 01010101 magul+	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$					907	DC	ALIO UUUUUIUI U	1010101 00000101 01010101 Tesuit	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$					968	DC	XL16' 00000101 0	1010101 01010101 01010101' v3	
969 970 VRI_C VREP, 0, 3 00018C0 971+ DS 0FD 00018C0 00001908 973+T16 DC A(X16) address of test routine 00018C4 0010 974+ DC H' 16' test number	000018B8					_ •			
$\begin{array}{cccccccccccccccccccccccccccccccccccc$									
00018C0 000018C0 972+ USING *, R5 base for test data and test routine 00018C0 00001908 973+T16 DC A(X16) address of test routine 00018C4 0010 974+ DC H' 16' test number									
00018C0 00001908 973+T16 DC A(X16) address of test routine 00018C4 0010 974+ DC H'16' test number	000018C0		00001000						
00018C4 0010 974+ DC H'16' test number		00001000	000018C0						
OUTOCO OO A UU								test number	
	00001000				0701	ь	AUU		

DC

XL16' 01010201 07770101 A010101A 01010101' v3

1026

01010201 07770101

000019C0

1059

1060

DC

F' 0'

F' 0'

END OF TABLE

00001A58 00000000

00001A5C

SMA Ver.	0. 7. 0 zvector- e7	- 22- VREP			03 Apr 2025 15: 40: 44 Pag	e 26
LOC	OBJECT CODE	ADDR1	ADDR2	STMI		
Loc	ODOLOT CODE	ADDIVI	1100102			
				1093 ****** 1094 *		*
				1094 *******	Register equates ************************************	*
		0000000	00000001	1097 RO	EQU 0	
		0000000	00000001	1097 R0 1098 R1	EQU 1	
		0000002	0000001	1099 R2	EQU 2 EQU 3	
		0000003 0000004	$00000001 \\ 00000001$	1100 R3 1101 R4	EQU 2 EQU 3 EQU 4 EQU 5 EQU 6 EQU 7 EQU 8 EQU 9 EQU 10	
		00000004	00000001	1101 R4 1102 R5	EQU 5	
		00000006	00000001	1103 R6	EQU 6	
		0000007 0000008	00000001 00000001	1104 R7 1105 R8	EQU 7 EQU 8	
		00000009	00000001	1106 R9	EQU 9	
		000000A	00000001	1107 R10	EQU 10	
		0000000B 0000000C	00000001 00000001	1108 R11 1109 R12	EQU 11 EQU 12	
		000000D	0000001	1110 R13	EQU 13	
		000000E	00000001	1111 R14	EQU 14	
		000000F	0000001	1112 R15	EQU 15	
					***********************	*
				1115 *	Register equates ************************************	*
				1116 *****		
		0000000 0000001	00000001	1118 V0	EQU 0	
		0000001	00000001 00000001	1119 V1 1120 V2	EQU 1 EQU 2	
		0000003	0000001	1121 V3	EQU 3	
		0000004 0000005	$00000001 \\ 00000001$	1122 V4 1123 V5	EQU 4 EQU 5	
		00000003	00000001	1123 V3 1124 V6	EQU 6	
		0000007	0000001	1125 V7	EQU 7	
		00000008 00000009	00000001 00000001	1126 V8 1127 V9	EQU 8 EQU 9	
		0000009 0000000A	00000001	1127 V9 1128 V10	EQU 10	
		000000B	0000001	1129 V11	EQU 11	
		000000C 000000D	00000001 00000001	1130 V12 1131 V13	EQU 12 EQU 13	
		000000E	0000001	1132 V14	EQU 14	
		000000F	0000001	1133 V15	EQU 15	
		$00000010 \\ 00000011$	$00000001 \\ 00000001$	1134 V16 1135 V17	EQU 16 EQU 17	
		0000012	0000001	1136 V18	EQU 18	
		00000014	00000001	1137 V19	EQU 19	
		00000014 00000015	00000001 00000001	1138 V20 1139 V21	EQU 20 EQU 21	
		0000010	3000001	1100 121	240 ~1	

WA Ver.	0. 7. 0 zvector- e7	- 22- VREP						03 A ₁	or 2025 1	5: 40: 44	Page	27
LOC	OBJECT CODE	ADDR1	ADDR2	STMT								
		00000016	00000001	1140 V22	EQU	22						
		00000017 00000018	00000001 00000001	1141 V23 1142 V24	EQU EQU	23 24						
		00000019	00000001	1143 V25	EQU	25						
		0000001A 0000001B	00000001 00000001	1144 V26 1145 V27	EQU EQU EQU EQU EQU EQU EQU EQU EQU	22 23 24 25 26 27 28 29 30 31						
		0000001C 0000001D	00000001 00000001	1146 V28 1147 V29	EQU FOU	28 20						
		000001E	00000001	1148 V30	EQU	30						
		000001F	0000001	1149 V31 1150	EQU	31						
				1151	END							

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERE	MCEC											
	IIFE		LENGIH														
EGI N	I	00000200	2	151	117	147	148	149									
LRO	F	000004A4	4	351	161	162	163	164									
CNUM	C	00001081	16	404	260	262	268	270	274	276							
TEST	4	0000000	72	418	210												
TESTS	\mathbf{F}	00001A60	4	1065	203												
IT	X	00001055	18	399	261	269	275										
DTEST	U	00000318	1	246	208												
J	I	00000488	4	341	196	249											
JPSW	D	00000478	8	339	341												
ILCONT	U	00000308	1	236													
I LED	F	00001000	$\bar{4}$	379	238	247											
ILMSG	Ū	00000304	1	230	220												
ILPSW	Ď	00000490	8	343	345												
ILTEST	Ĩ	000004A0	4	345	250												
80001	F	00000480	8	180	184	185	187										
	Ī	00000280	2	424	267	100	101										
AGE	1	00000000	6840	0	~U1												
AUL	II	0000000	1	363	364	365	366										
34	II	00010000	1	365	304	303	300										
9 4	U	0001000	1	365 423	273												
	U		1		213												
	U	00100000	1	366	105	004											
G	1	000003C0	4	301	195	284											
GCMD	C	0000040E	9	331	314	315	000										
GMSG	Ç	00000417	95	332	308	329	306										
GMVC	Ĩ	00000408	6	329	312												
GOK	Ī	000003D6	2	310	307												
GRET	<u>I</u>	000003F6	4	325	318	321											
SGSAVE	F	000003FC	4	328	304	325											
EXTE7	U	000002D4	1	205	223	241											
PNAME	C	000000A	8	426	265												
GE	U	00001000	1	364													
T3	C	0000106B	18	402	261	262	263	269	270	271	275	276	277				
RTI 2	C	00001044	5	390	271												
ETLI NE	C	00001008	16	385	394	283											
RTLNG	U	000004D	1	394	282												
TM4	C	00001052	2	392	277												
TNAME	C	00001033	8	388	265												
TNUM	Č	00001018	3	386	263												
)	Ŭ	00000000	1	1097	111	161	164	184	186	187	188	193	212	213	237	238	281
	~	300000	•	_00,	282	285	301	304	306	308	310	325	~-~	~10		200	~~•
	U	0000001	1	1098	194	218	219	247	248	283	315	329	551	552	580	581	609
		3000001		1000	610	638	639	667	668	697	698	726	727	755	756	784	785
					813	814	843	844	872	873	901	902	930	931	960	961	989
						1018	1019	1047	1048	373	301	302	000	J J I	000	001	000
0	U	000000A	1	1107	149	158	159	1011	1010								
1	Ü	0000000A	1	1107	215	216	555	584	613	642	671	701	730	759	788	817	847
•	U	ооооооо	1	1100	876	905	934	964	993	1022	1051	,01	, 50	100	, 00	017	JT/
2	U	000000C	1	1109	203	206	222	240	<i>33</i> 3	1066	1001						
			1		203	200	222	240									
3	U	000000D	1	1110													
4	U	000000E	1	1111	001	050	000	000									
5	U	000000F	1	1112	231	256	288	289	000	0~0	c~ -	001	00.	00-	000	00.1	040
	U	00000002	1	1099	195	259	260	267	268	273	274	281	284	285	302	304	310
		0000000		440-	311	312	314	320	325	326							
	U	00000003	1	1100													
:	U	0000004	1	1101													
	U	00000005	1	1102	206	207	210	257	287	534	557	563	586	592	615	621	644

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERI	ENCES											
					650	673	680	703	709	732	738	761	767	790	796	819	826
					849	855	878	884	907	913	936	943	966	972	995	1001	1024
C	TI	0000006	1	1103	1030	1053											
6 7	U U	0000000	1	1103													
8	บั	00000007	1	1105	147	151	152	153	155								
9	U	00000009	1	1106	148	155	156	158									
E1	F	00001130	4	556	541	542	544										
RE10 RE11	F F	000015F8 00001680	4 4	818 848	803 833	804 834	806 836										
E12	F	00001080	4	877	862	863	865										
RE13	F	00001700	4	906	891	892	894										
RE14	F	00001818	4	935	920	921	923										
RE15	F	000018A0	4	965	950	951	953										
RE16	F	00001928	4	994	979 1008	980	982										
RE17 RE18	F F	000019B0 00001A38	4 4	1023 1052	1008	1009 1038	1011 1040										
RE2	F	00001A30	4	585	570	571	573										
RE3	F	00001240	4	614	599	600	602										
RE4	<u>F</u>	000012C8	4	643	628	629	631										
RE5	F	00001350	4	672	657	658	660										
EE6 EE7	F F	000013D8 00001460	4 4	702 731	687 716	688 717	690 719										
EE8	F	00001400 000014E8	4	760	745	746	748										
RE9	$ar{\mathbf{F}}$	00001570	4	789	774	775	777										
REA1	A	000010E8	4	544													
REA10	A	000015B0	4	806													
REA11 REA12	A A	00001638 000016C0	4 4	836 865													
REA13	A	00001000	4	894													
REA14	Ā	000017D0	$ar{4}$	923													
REA15	A	00001858	4	953													
REA16	A	000018E0	4	982													
REA17 REA18	A A	00001968 000019F0	4 1	1011 1040													
REA2	A	00001310	4	573													
REA3	Ā	000011F8	$ar{4}$	602													
REA4	A	00001280	4	631													
REA5	A	00001308	4	660													
REA6 REA7	A A	00001390 00001418	4	690 719													
REA8	A	00001418 000014A0	4	719													
REA9	Ā	00001528	$\stackrel{ a}{4}$	777													
READDR	A	00000020	4	430	218												
REG2LOW	U	000000DD	1	369													
REG2PATT RELEN	U A	AABBCCDD 000001C	1	368 429													
RPTDWSAV	D A	0000001C	8	294	281	285											
RPTERROR	Ĩ	00000326	4	256	231												
RPTSAVE	<u>F</u>	000003A4	4	291	256	288											
PTSVR5	F	000003A8	4	292	257	287											
SKL0001 SKT0001	U	0000004E 0000022A	1	177 174	193	194											
VOLDPSW	U II	0000022A 00000140	20	113	177	194											
11	Ä	0000140 000010C8	4	535	1068												
10	Ā	00001590	$\bar{4}$	797	1077												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERE	NCES											
1	A	00001618	4	827	1078												
2	A	000016A0	4	856	1079												
3	A	00001728	4	885	1080												
4	A	000017B0	4	914	1081												
5	A	00001838	4	944	1082												
6	A	00001800	4	973	1083												
7	A	00001948 000019D0	4	1002	1084												
8	A		4	1031	1085												
	A	00001150 000011D8	4	564 502	1069												
	A	00001108	4	593 622	1070												
	A.	00001260 000012E8	4 4	651	1071 1072												
	A	000012E8	4	681	1072												
	A A	00001370 000013F8	4	710	1073												
		00001318	4	739	1075												
•	A A	00001480	4	739 768	1073												
STING	F	00001308	4	380	213												
UM	H H	00001004	2	420	212	259											
UB	A	00000004	$\tilde{4}$	419	215	200											
ABLE	F	00001A60	4	1067	213												
TRUEL	Ū	00000000	1	1118													
	Ŭ	00000001	ī	1119													
0	Ŭ	0000000A	î	1128													
1	Ŭ	0000000H	î	1129													
2	Ŭ	0000000C	1	1130													
$\tilde{3}$	Ŭ	000000D	1	1131													
4	Ŭ	000000E	1	1132													
5	Ü	000000F	$\bar{1}$	1133													
6	Ū	00000010	$\bar{1}$	1134													
7	Ū	00000011	1	1135													
8	Ü	00000012	1	1136													
9	Ū	0000013	1	1137													
FUDGE	X	000010A4	16		550 929	579 959	608 988	637 1017	666 1046	696	725	754	783	812	842	871	900
01	X	000010F8	16	546	554												
010	X	000015C0	16	808	816												
011	X	00001648	16	838	846												
012	X	000016D0	16	867	875												
013	X	00001758	16	896	904												
014	X	000017E0	16	925	933												
015	X	00001868	16	955	963												
016	X	000018F0	16	984	992												
017	X	00001978	16	1013	1021												
018	X	00001A00	16	1042	1050												
02	X	00001180	16	575	583												
03	X	00001208	16	604	612												
04	X	00001290	16	633	641												
05	X	00001318	16	662	670												
06	X	000013A0	16	692	700												
07	X	00001428	16	721	729												
08	X	000014B0	16	750	758												
09	X	00001538	16	779	787												
OUTPUT	X	00000030	16	432	219												
0	U U	00000002	1	1120 1138													
		00000014	1	1100													

SYMB0L	TYPE	VALUE	LENGTH	DEFN	REFER	ENCES											
V22	U	0000016	1	1140	550 669 787	553 670 812	554 696 815	579 699 816	582 700 842	583 725 845	608 728 846	611 729 871	612 754 874	637 757 875	640 758 900	641 783 903	666 786 904
700	T T	00000017	1	1111	929 1049	932 1050	933	959	962	963	988	991	992	1017	1020	1021	1046
/23	U	0000017	1	1141	552 728 931	553 756 932	581 757 961	582 785 962	610 786 990	611 814 991	639 815 1019	640 844 1020	668 845 1048	669 873 1049	698 874	699 902	727 903
V24	U	00000018	1	1142													
V25	U	00000019	1	1143													
V26 V27	U U	0000001A 0000001B	1	1144 1145													
V 2 7 V 2 8	Ü	0000001B	1	1145													
V29	Ü	0000001C 0000001D	1	1140													
V2ADDR	A	0000001B 00000014	4	427	551	580	609	638	667	697	726	755	784	813	843	872	901
V ≈ ADDIK	А	0000014	7	T& 1	930	960	989	1018	1047	037	720	733	704	013	043	012	301
V3	U	00000003	1	1121	000	000	000	1010	1017								
V30	Ŭ	0000001E	1	1148													
V31	Ŭ	0000001F	1	1149													
V3ADDR	Ä	00000018	$\bar{4}$	428													
V4	Ū	00000004	1	1122													
V5	Ū	0000005	1	1123													
V 6	U	0000006	1	1124													
V7	U	0000007	1	1125													
V8	U	00000008	1	1126													
V9	U	0000009	1	1127													
X0001	U	000002A8	1	183	171	184											
X1	\mathbf{F}	00001110	4	549	535												
X10	<u>F</u>	000015D8	4	811	797												
X11	<u>F</u>	00001660	4	841	827												
X12	<u>F</u>	000016E8	4	870	856												
X13	F	00001770	4	899	885												
X14	F	000017F8	4	928	914												
X15	F	00001880	4	958	944												
X16	r F	00001908	4	987	973												
X17	r	00001990 00001A18	4	1016	1002												
X18 X2	r E	00001A18 00001198	4	1045 578	1031 564												
X3	r F	00001198	4	607	593												
X4	r F	00001220 000012A8	4	636	622												
X5	F	000012A0 00001330	4	665	651												
X6	F	00001330 000013B8	4	695	681												
X7	F	00001380	4	72 4	710												
X8	F	00001440 000014C8	4	753	739												
X9	F	00001460	4	782	768												
XC0001	Ū	00001000 000002D0	i	197	189												
ZVE7TST	$ar{f J}$	00000000	6840	110	113	115	119	123	378	111							
=A(E7TESTS)	Ä	000004B0	4	356	203				, . .	-							
=AL2(L'MSGMSG)	R	000004BA	$\overline{2}$	359	306												
=F' 1'	F	000004B4	4	357	237												
=F' 64'	F	000004AC	4	355	188												
=H' O'	H	000004B8	2	358	301												

		zvecto REFERENO		z-VREP										03 Apr	2025	15: 40: 44	Page	32
CHECK TABLE RI_C	63 498	170 1066 532 1028	EQ1	500	£10	640	670	707	796	765	704	004	059	009	011	041	070	000
11_C	453	1028	561	590	619	648	678	707	736	765	794	824	853	882	911	941	970	999

