```
 LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                     2 ************************************************************************
                                                     3 *
                                                     4 *   Zvector E7 instruction tests for VRR-d encoded:
                                                     5 *
                                                     6 *   E7A9 VMALH  - Vector Multiply and Add Logical High
                                                     7 *   E7AA VMAL   - Vector Multiply and Add Low
                                                     8 *   E7AB VMAH   - Vector Multiply and Add High
                                                     9 *   E7AC VMALE  - Vector Multiply and Add Logical Even
                                                    10 *   E7AD VMALO  - Vector Multiply and Add Logical Odd
                                                    11 *   E7AE VMAE   - Vector Multiply and Add Even
                                                    12 *   E7AF VMAO   - Vector Multiply and Add Odd
                                                    13 *
                                                    14 *        James Wekel March 2025
                                                    15 ************************************************************************


                                                    17 ************************************************************************
                                                    18 *
                                                    19 *        basic instruction tests
                                                    20 *
                                                    21 ************************************************************************
                                                    22 *  This program tests proper functioning of the z/arch E7 VRR-d vector
                                                    23 *  multiply and add (logical high, low, high, logical even,
                                                    24 *  logical odd, even, and odd) instructions.
                                                    25 *  Exceptions are not tested.
                                                    26 *
                                                    27 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                    28 *  obvious coding errors.  None of the tests are thorough.  They are
                                                    29 *  NOT designed to test all aspects of any of the instructions.
                                                    30 *
                                                    31 ************************************************************************
                                                    32 *
                                                    33 *   *Testcase zvector-e7-10-multiplyAdd
                                                    34 *   *
                                                    35 *   *   Zvector E7 instruction tests for VRR-d encoded:
                                                    36 *   *
                                                    37 *   *   E7A9 VMALH  - Vector Multiply and Add Logical High
                                                    38 *   *   E7AA VMAL   - Vector Multiply and Add Low
                                                    39 *   *   E7AB VMAH   - Vector Multiply and Add High
                                                    40 *   *   E7AC VMALE  - Vector Multiply and Add Logical Even
                                                    41 *   *   E7AD VMALO  - Vector Multiply and Add Logical Odd
                                                    42 *   *   E7AE VMAE   - Vector Multiply and Add Even
                                                    43 *   *   E7AF VMAO   - Vector Multiply and Add Odd
                                                    44 *   *
                                                    45 *   *   # ------------------------------------------------------------
                                                    46 *   *   #  This tests only the basic function of the instruction.
                                                    47 *   *   #  Exceptions are NOT tested.
                                                    48 *   *   # ------------------------------------------------------------
                                                    49 *   *
                                                    50 *   mainsize    2
                                                    51 *   numcpu      1
                                                    52 *   sysclear
                                                    53 *   archlvl     z/Arch
                                                    54 *
                                                    55 *   loadcore    "$(testpath)/zvector-e7-10-multiplyAdd.core" 0x0
                                                    56 *
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      57 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                      58 *   runtest     10        # (2 secs if intrinsic used, 10 otherwise!)
                                                      59 *   diag8cmd    disable   # (reset back to default)
                                                      60 *
                                                      61 *   *Done
                                                      62 *
                                                      63 ********************************************************************************
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                       65 ************************************************************************
                                                       66 *        FCHECK Macro - Is a Facility Bit set?
                                                       67 *
                                                       68 *        If the facility bit is NOT set, an message is issued and
                                                       69 *        the test is skipped.
                                                       70 *
                                                       71 *        Fcheck uses R0, R1 and R2
                                                       72 *
                                                       73 * eg.    FCHECK 134,'vector-packed-decimal'
                                                       74 ************************************************************************
                                                       75          MACRO
                                                       76          FCHECK &BITNO,&NOTSETMSG
                                                       77 .*                      &BITNO : facility bit number to check
                                                       78 .*                      &NOTSETMSG : 'facility name'
                                                       79          LCLA  &FBBYTE           Facility bit in Byte
                                                       80          LCLA  &FBBIT            Facility bit within Byte
                                                       81
                                                       82          LCLA  &L(8)
                                                       83 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                       84
                                                       85 &FBBYTE  SETA  &BITNO/8
                                                       86 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                       87 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                       88
                                                       89          B     X&SYSNDX
                                                       90 *                                       Fcheck data area
                                                       91 *                                       skip messgae
                                                       92 SKT&SYSNDX DC  C'    Skipping tests: '
                                                       93          DC    C&NOTSETMSG
                                                       94          DC    C' (bit &BITNO) is not installed.'
                                                       95 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                       96 *                                       facility bits
                                                       97          DS    FD                       gap
                                                       98 FB&SYSNDX DS   4FD
                                                       99          DS    FD                       gap
                                                      100 *
                                                      101 X&SYSNDX EQU *
                                                      102          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                      103          STFLE FB&SYSNDX               get facility bits
                                                      104
                                                      105          XGR   R0,R0
                                                      106          IC    R0,FB&SYSNDX+&FBBYTE    get fbit byte
                                                      107          N     R0,=F'&FBBIT'           is bit set?
                                                      108          BNZ   XC&SYSNDX
                                                      109 *
                                                      110 * facility bit not set, issue message and exit
                                                      111 *
                                                      112          LA    R0,SKL&SYSNDX           message length
                                                      113          LA    R1,SKT&SYSNDX           message address
                                                      114          BAL   R2,MSG
                                                      115
                                                      116          B     EOJ
                                                      117 XC&SYSNDX EQU *
                                                      118          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     120 ************************************************************************
                                                     121 *        Low core PSWs
                                                     122 ************************************************************************
                               00000000  00006137   123 ZVE7TST  START 0
00000000                       00000000             124          USING ZVE7TST,R0            Low core addressability
                                                    125
                               00000140  00000000   126 SVOLDPSW EQU   ZVE7TST+X'140'        z/Arch Supervisor call old PSW

00000000                       00000000  000001A0   128          ORG   ZVE7TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                         129          DC    X'0000000180000000'
000001A8  00000000 00000200                         130          DC    AD(BEGIN)

000001B0                       000001B0  000001D0   132          ORG   ZVE7TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                         133          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                         134          DC    AD(X'DEAD')

000001E0                       000001E0  00000200   136          ORG   ZVE7TST+X'200'        Start of actual test program...

                                                    138 ************************************************************************
                                                    139 *                The actual "ZVE7TST" program itself...
                                                    140 ************************************************************************
                                                    141 *
                                                    142 *  Architecture Mode: z/Arch
                                                    143 *  Register Usage:
                                                    144 *
                                                    145 *    R0       (work)
                                                    146 *    R1-4     (work)
                                                    147 *    R5       Testing control table - current test base
                                                    148 *    R6-R7    (work)
                                                    149 *    R8       First base register
                                                    150 *    R9       Second base register
                                                    151 *    R10      Third base register
                                                    152 *    R11      E7TEST call return
                                                    153 *    R12      E7TESTS register
                                                    154 *    R13      (work)
                                                    155 *    R14      Subroutine call
                                                    156 *    R15      Secondary Subroutine call or work
                                                    157 *
                                                    158 ************************************************************************

00000200                       00000200             160          USING  BEGIN,R8         FIRST Base Register
00000200                       00001200             161          USING  BEGIN+4096,R9    SECOND Base Register
00000200                       00002200             162          USING  BEGIN+8192,R10   THIRD Base Register

00000200  0580                                      164 BEGIN    BALR  R8,0              Initalize FIRST base register
00000202  0680                                      165          BCTR  R8,0              Initalize FIRST base register
00000204  0680                                      166          BCTR  R8,0              Initalize FIRST base register

00000206  4190 8800                    00000800     168          LA    R9,2048(,R8)      Initalize SECOND base register
0000020A  4190 9800                    00000800     169          LA    R9,2048(,R9)      Initalize SECOND base register
                                                    170
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000020E  41A0 9800                     00000800   171          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                     00000800   172          LA    R10,2048(,R10)   Initalize THIRD base register
                                                   173
00000216  B600 828C                     0000048C   174          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 828D                     0000048D   175          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 828D                     0000048D   176          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 828C                     0000048C   177          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                   178
                                                   179 ********************************************************************
                                                   180 * Is z/Architecture vector facility installed  (bit 129)
                                                   181 ********************************************************************
                                                   182
                                                   183          FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                     000002A8   184+         B     X0001
                                                   185+*                                  Fcheck data area
                                                   186+*                                  skip messgae
0000022A  40404040 E2928997                        187+SKT0001  DC    C'    Skipping tests: '
0000023E  A961C199 838889A3                        188+         DC    C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                        189+         DC    C' (bit 129) is not installed.'
                            0000004E  00000001     190+SKL0001  EQU   *-SKT0001
                                                   191+*                                  facility bits
00000278  00000000 00000000                        192+         DS    FD               gap
00000280  00000000 00000000                        193+FB0001   DS    4FD
000002A0  00000000 00000000                        194+         DS    FD               gap
                                                   195+*
                            000002A8  00000001     196+X0001    EQU   *
000002A8  4100 0004                     00000004   197+         LA    R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                     00000280   198+         STFLE FB0001           get facility bits
000002B0  B982 0000                                199+         XGR   R0,R0
000002B4  4300 8090                     00000290   200+         IC    R0,FB0001+16     get fbit byte
000002B8  5400 8294                     00000494   201+         N     R0,=F'64'        is bit set?
000002BC  4770 80D0                     000002D0   202+         BNZ   XC0001
                                                   203+*
                                                   204+* facility bit not set, issue message and exit
                                                   205+*
000002C0  4100 004E                     0000004E   206+         LA    R0,SKL0001       message length
000002C4  4110 802A                     0000022A   207+         LA    R1,SKT0001       message address
000002C8  4520 81A8                     000003A8   208+         BAL   R2,MSG
000002CC  47F0 8270                     00000470   209+         B     EOJ
                            000002D0  00000001     210+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    212 ************************************************************************
                                                    213 *               Do tests in the E7TESTS table
                                                    214 ************************************************************************
                                                    215
000002D0  58C0 8298                       00000498 216          L     R12,=A(E7TESTS)       get table of test addresses
                                                    217
                                 000002D4 00000001 218 NEXTE7   EQU   *
000002D4  5850 C000                       00000000 219          L     R5,0(0,R12)       get test address
000002D8  1255                                     220          LTR   R5,R5                have a test?
000002DA  4780 811E                       0000031E 221          BZ    ENDTEST                 done?
                                                    222
000002DE                          00000000         223          USING E7TEST,R5
                                                    224
000002DE  4800 5004                       00000004 225          LH    R0,TNUM           save current test number
000002E2  5000 8E04                       00001004 226          ST    R0,TESTING        for easy reference
                                                    227
000002E6  E710 8E94 0006                  00001094 228          VL    V1,V1FUDGE
000002EC  58B0 5000                       00000000 229          L     R11,TSUB          get address of test routine
000002F0  05BB                                     230          BALR  R11,R11           do test
                                                    231
000002F2  E310 5020 0014                  00000020 232          LGF   R1,READDR         get address of expected result
000002F8  D50F 5030 1000       00000030  00000000 233          CLC   V1OUTPUT,0(R1)    valid?
000002FE  4770 810A                       0000030A 234          BNE   FAILMSG              no, issue failed message
                                                    235
00000302  41C0 C004                       00000004 236          LA    R12,4(0,R12)      next test address
00000306  47F0 80D4                       000002D4 237          B     NEXTE7
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    239 ************************************************************************
                                                    240 * result not as expected:
                                                    241 *        issue message with test number, instruction under test
                                                    242 *              and instruction m4
                                                    243 ************************************************************************
                             0000030A  00000001     244 FAILMSG  EQU   *
0000030A  45F0 812C                    0000032C     245          BAL   R15,RPTERROR

                                                    247 ************************************************************************
                                                    248 * continue after a failed test
                                                    249 ************************************************************************
                             0000030E  00000001     250 FAILCONT EQU   *
0000030E  5800 829C                    0000049C     251          L     R0,=F'1'          set failed test indicator
00000312  5000 8E00                    00001000     252          ST    R0,FAILED
                                                    253
00000316  41C0 C004                    00000004     254          LA    R12,4(0,R12)      next test address
0000031A  47F0 80D4                    000002D4     255          B     NEXTE7


                                                    257 ************************************************************************
                                                    258 * end of testing; set ending psw
                                                    259 ************************************************************************
                             0000031E  00000001     260 ENDTEST  EQU   *
0000031E  5810 8E00                    00001000     261          L     R1,FAILED         did a test fail?
00000322  1211                                      262          LTR   R1,R1
00000324  4780 8270                    00000470     263          BZ    EOJ               No, exit
00000328  47F0 8288                    00000488     264          B     FAILTEST          Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    266 ********************************************************************************
                                                    267 *        RPTERROR                  Report instruction test in error
                                                    268 ********************************************************************************

0000032C  50F0 8190                        00000390   270 RPTERROR ST    R15,RPTSAVE          Save return address
00000330  5050 8194                        00000394   271          ST    R5,RPTSVR5           Save R5
                                                      272 *
00000334  4820 5004                        00000004   273          LH    R2,TNUM              get test number and convert
00000338  4E20 8E73                        00001073   274          CVD   R2,DECNUM
0000033C  D211 8E5D 8E47       0000105D    00001047   275          MVC   PRT3,EDIT
00000342  DE11 8E5D 8E73       0000105D    00001073   276          ED    PRT3,DECNUM
00000348  D202 8E18 8E6A       00001018    0000106A   277          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                      278
0000034E  D207 8E33 5008       00001033    00000008   279          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                      280 *
00000354  E320 5007 0076                   00000007   281          LB    R2,m5                get m5 and convert
0000035A  4E20 8E73                        00001073   282          CVD   R2,DECNUM
0000035E  D211 8E5D 8E47       0000105D    00001047   283          MVC   PRT3,EDIT
00000364  DE11 8E5D 8E73       0000105D    00001073   284          ED    PRT3,DECNUM
0000036A  D201 8E44 8E6B       00001044    0000106B   285          MVC   PRTM5(2),PRT3+14     fill in message with m4 field

                                                      287 *
                                                      288 *        Use Hercules Diagnose for Message to console
                                                      289 *
00000370  9002 8198                        00000398   290          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000374  4100 003F                        0000003F   291          LA    R0,PRTLNG            message length
00000378  4110 8E08                        00001008   292          LA    R1,PRTLINE             messagfe address
0000037C  4520 81A8                        000003A8   293          BAL   R2,MSG               call Hercules console MSG display
00000380  9802 8198                        00000398   294          LM    R0,R2,RPTDWSAV       restore regs


00000384  5850 8194                        00000394   296          L     R5,RPTSVR5           Restore R5
00000388  58F0 8190                        00000390   297          L     R15,RPTSAVE          Restore return address
0000038C  07FF                                        298          BR    R15                  Return to caller

00000390  00000000                                    300 RPTSAVE  DC    F'0'                 R15 save area
00000394  00000000                                    301 RPTSVR5  DC    F'0'                 R5 save area

00000398  00000000 00000000                           303 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    305 ************************************************************************
                                                    306 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    307 *              R2 = return address
                                                    308 ************************************************************************
000003A8  4900 82A0                       000004A0  310 MSG      CH    R0,=H'0'                Do we even HAVE a message?
000003AC  07D2                                      311           BNHR  R2                      No, ignore

000003AE  9002 81E4                       000003E4  313           STM   R0,R2,MSGSAVE           Save registers

000003B2  4900 82A2                       000004A2  315           CH    R0,=AL2(L'MSGMSG)       Message length within limits?
000003B6  47D0 81BE                       000003BE  316           BNH   MSGOK                   Yes, continue
000003BA  4100 005F                       0000005F  317           LA    R0,L'MSGMSG             No, set to maximum

000003BE  1820                                      319 MSGOK     LR    R2,R0                   Copy length to work register
000003C0  0620                                      320           BCTR  R2,0                    Minus-1 for execute
000003C2  4420 81F0                       000003F0  321           EX    R2,MSGMVC               Copy message to O/P buffer

000003C6  4120 200A                       0000000A  323           LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
000003CA  4110 81F6                       000003F6  324           LA    R1,MSGCMD               Point to true command

000003CE  83120008                                  326           DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
000003D2  4780 81DE                       000003DE  327           BZ    MSGRET                  Return if successful
                                                    328
000003D6  1222                                      329           LTR   R2,R2                   Is Diag8 Ry (R2) 0?
000003D8  4780 81DE                       000003DE  330           BZ    MSGRET                    an error occurred but coninue
                                                    331
000003DC  0000                                      332           DC    H'0'                    CRASH for debugging purposes

000003DE  9802 81E4                       000003E4  334 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
000003E2  07F2                                      335           BR    R2                      Return to caller

000003E4  00000000 00000000                         337 MSGSAVE  DC    3F'0'                   Registers save area
000003F0  D200 81FF 1000      000003FF  00000000    338 MSGMVC   MVC   MSGMSG(0),0(R1)          Executed instruction

000003F6  D4E2C7D5 D6C8405C                         340 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
000003FF  40404040 40404040                         341 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                    342
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    344 ************************************************************************
                                                    345 *        Normal completion or Abnormal termination PSWs
                                                    346 ************************************************************************


00000460  00020001 80000000                         348 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
00000470  B2B2 8260                   00000460      350 EOJ      LPSWE EOJPSW                Normal completion


00000478  00020001 80000000                         352 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
00000488  B2B2 8278                   00000478      354 FAILTEST LPSWE FAILPSW               Abnormal termination


                                                    356 ************************************************************************
                                                    357 *        Working Storage
                                                    358 ************************************************************************


0000048C  00000000                                  360 CTLR0    DS    F                    CR0
00000490  00000000                                  361          DS    F

00000494                                            363          LTORG ,                    Literals pool
00000494  00000040                                  364                =F'64'
00000498  00005F84                                  365                =A(E7TESTS)
0000049C  00000001                                  366                =F'1'
000004A0  0000                                      367                =H'0'
000004A2  005F                                      368                =AL2(L'MSGMSG)
                                                    369
                                                    370 *        some constants
                                                    371
                          00000400  00000001        372 K        EQU   1024                 One KB
                          00001000  00000001        373 PAGE     EQU   (4*K)                Size of one page
                          00010000  00000001        374 K64      EQU   (64*K)               64 KB
                          00100000  00000001        375 MB       EQU   (K*K)                 1 MB
                                                    376
                          AABBCCDD  00000001        377 REG2PATT EQU   X'AABBCCDD'     Polluted Register pattern
                          000000DD  00000001        378 REG2LOW  EQU         X'DD'     (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    380 *====================================================================
                                                    381 *
                                                    382 *  NOTE: start data on an address that is easy to display
                                                    383 *        within Hercules
                                                    384 *
                                                    385 *====================================================================
                                                    386
000004A4                      000004A4  00001000    387          ORG   ZVE7TST+X'1000'
00001000  00000000                                  388 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                  389 TESTING  DC    F'0'                    current test number


                                                    391 *
                                                    392 *        failed message and associated editting
                                                    393 *
00001008  40404040 40404040                         394 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                    395 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                         396          DC    c' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                         397 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 884094F5                         398          DC    C' with m5='
00001044  A7A7                                      399 PRTM5    DC    C'xx'
00001046  4B                                        400          DC    C'.'
                                0000003F  00000001  401 PRTLNG   EQU   *-PRTLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    403 ************************************************************************
                                                    404 *        TEST failed : message working storge
                                                    405 ************************************************************************
00001047  40212020 20202020                         406 EDIT     DC    XL18'40212020202020202020202020202020'
                                                    407
00001059  7E7E7E6E                                  408          DC    C'===>'
0000105D  40404040 40404040                         409 PRT3     DC    CL18' '
0000106F  4C7E7E7E                                  410          DC    C'<==='
00001073  00000000 00000000                         411 DECNUM   DS    CL16


                                                    413 ************************************************************************
                                                    414 *        Vector instruction results, pollution and input
                                                    415 ************************************************************************
00001084                                            416          DS    0F
00001084  00000000 00000000                         417          DS    XL16                                        gap
00001094  FFFFFFFF FFFFFFFF                         418 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010A4  00000000 00000000                         419          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     421 ********************************************************************************
                                                     422 *        E7TEST DSECT
                                                     423 ********************************************************************************


                                                     425 E7TEST   DSECT ,
00000000  00000000                                   426 TSUB     DC    A(0)           pointer  to test
00000004  0000                                       427 TNUM     DC    H'00'          Test Number
00000006  00                                         428          DC    X'00'
00000007  00                                         429 M5       DC    HL1'00'        m4 used
                                                     430
00000008  40404040 40404040                          431 OPNAME   DC    CL8' '         E7 name
00000010  00000000                                   432 V2ADDR   DC    A(0)           address of v2 source
00000014  00000000                                   433 V3ADDR   DC    A(0)           address of v3 source
00000018  00000000                                   434 V4ADDR   DC    A(0)           address of v4 source
0000001C  00000000                                   435 RELEN    DC    A(0)           RESULT LENGTH
00000020  00000000                                   436 READDR   DC    A(0)           result (expected) address
00000028  00000000 00000000                          437          DS    FD                gap
00000030  00000000 00000000                          438 V1OUTPUT DS    XL16           V1 Output
00000040  00000000 00000000                          439          DS    FD                gap
                                                     440
                                                     441 *        test routine will be here (from VRR-d macro)
                                                     442 *
                                                     443 *        followed by
                                                     444 *              EXPECTED RESULT


                          00000000  00006137   446 ZVE7TST  CSECT ,
000010B4                                             447          DS    0F


                                                     449 ********************************************************************************
                                                     450 *     Macros to help build test tables
                                                     451 ********************************************************************************


                                                     453 *
                                                     454 * macro to generate individual test
                                                     455 *
                                                     456          MACRO
                                                     457          VRR_D &INST,&M5
                                                     458 .*                              &INST   - VRR-d instruction under test
                                                     459 .*                              &m5     - m5 field
                                                     460
                                                     461          GBLA  &TNUM
                                                     462 &TNUM     SETA  &TNUM+1
                                                     463
                                                     464          DS    0FD
                                                     465          USING *,R5             base for test data and test routine
                                                     466
                                                     467 T&TNUM    DC    A(X&TNUM)        address of test routine
                                                     468          DC    H'&TNUM'         test number
                                                     469          DC    X'00'
                                                     470          DC    HL1'&M5'         m5
                                                     471          DC    CL8'&INST'       instruction name
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      472           DC    A(RE&TNUM+16)     address of v2 source
                                                      473           DC    A(RE&TNUM+32)     address of v3 source
                                                      474           DC    A(RE&TNUM+48)     address of v4 source
                                                      475           DC    A(16)             result length
                                                      476 REA&TNUM  DC    A(RE&TNUM)        result address
                                                      477           DS    FD                gap
                                                      478 V1O&TNUM  DS    XL16              V1 output
                                                      479           DS    FD                gap
                                                      480 .*
                                                      481 *
                                                      482 X&TNUM    DS    0F
                                                      483           LGF   R1,V2ADDR         load v2 source
                                                      484           VL    v22,0(R1)         use v22 to test decoder
                                                      485
                                                      486           LGF   R1,V3ADDR         load v3 source
                                                      487           VL    v23,0(R1)         use v23 to test decoder
                                                      488
                                                      489           LGF   R1,V4ADDR         load v4 source
                                                      490           VL    v24,0(R1)         use v24 to test decoder
                                                      491
                                                      492           &INST V22,V22,V23,V24,&M5  test instruction (dest is a source)
                                                      493           VST   V22,V1O&TNUM       save v1 output
                                                      494
                                                      495           BR    R11               return
                                                      496
                                                      497 RE&TNUM   DC    0F                xl16 expected result
                                                      498
                                                      499           DROP  R5
                                                      500           MEND




                                                      502 *
                                                      503 * macro to generate table of pointers to individual tests
                                                      504 *
                                                      505           MACRO
                                                      506           PTTABLE
                                                      507           GBLA  &TNUM
                                                      508           LCLA  &CUR
                                                      509 &CUR      SETA  1
                                                      510 .*
                                                      511 TTABLE    DS    0F
                                                      512 .LOOP     ANOP
                                                      513 .*
                                                      514           DC    A(T&CUR)
                                                      515 .*
                                                      516 &CUR      SETA  &CUR+1
                                                      517           AIF   (&CUR LE &TNUM).LOOP
                                                      518 *
                                                      519           DC    A(0)              END OF TABLE
                                                      520           DC    A(0)
                                                      521 .*
                                                      522           MEND
                                                      523
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     525 ************************************************************************
                                                     526 *        E7 VRR-d tests
                                                     527 ************************************************************************
                                                     528         PRINT DATA
000010B8  00000000 00000000                          529         DS    FD
                                                     530 *
                                                     531 *   E7A9 VMALH  - Vector Multiply and Add Logical High
                                                     532 *   E7AA VMAL   - Vector Multiply and Add Low
                                                     533 *   E7AB VMAH   - Vector Multiply and Add High
                                                     534 *   E7AC VMALE  - Vector Multiply and Add Logical Even
                                                     535 *   E7AD VMALO  - Vector Multiply and Add Logical Odd
                                                     536 *   E7AE VMAE   - Vector Multiply and Add Even
                                                     537 *   E7AF VMAO   - Vector Multiply and Add Odd
                                                     538 *
                                                     539 *        VRR-d instruction, m5
                                                     540 *              followed by
                                                     541 *                 16 byte expected result (V1)
                                                     542 *                 16 byte V2 source
                                                     543 *                 16 byte V3 source
                                                     544 *                 16 byte V4 source
                                                     545 *------------------------------------------------------------------
                                                     546 *  VMALH  - Vector Multiply and Add Logical High
                                                     547 *------------------------------------------------------------------
                                                     548 * Byte
                                                     549         VRR_D VMALH,0
000010C0                                             550+        DS    0FD
000010C0                          000010C0           551+        USING *,R5          base for test data and test routine
000010C0  00001108                                   552+T1      DC    A(X1)         address of test routine
000010C4  0001                                       553+        DC    H'1'          test number
000010C6  00                                         554+        DC    X'00'
000010C7  00                                         555+        DC    HL1'0'        m5
000010C8  E5D4C1D3 C8404040                          556+        DC    CL8'VMALH'    instruction name
000010D0  0000114C                                   557+        DC    A(RE1+16)     address of v2 source
000010D4  0000115C                                   558+        DC    A(RE1+32)     address of v3 source
000010D8  0000116C                                   559+        DC    A(RE1+48)     address of v4 source
000010DC  00000010                                   560+        DC    A(16)         result length
000010E0  0000113C                                   561+REA1    DC    A(RE1)        result address
000010E8  00000000 00000000                          562+        DS    FD            gap
000010F0  00000000 00000000                          563+V1O1    DS    XL16          V1 output
000010F8  00000000 00000000
00001100  00000000 00000000                          564+        DS    FD            gap
                                                     565+*
00001108                                             566+X1      DS    0F
00001108  E310 5010 0014                 00000010    567+        LGF   R1,V2ADDR     load v2 source
0000110E  E761 0000 0806                 00000000    568+        VL    v22,0(R1)     use v22 to test decoder
00001114  E310 5014 0014                 00000014    569+        LGF   R1,V3ADDR     load v3 source
0000111A  E771 0000 0806                 00000000    570+        VL    v23,0(R1)     use v23 to test decoder
00001120  E310 5018 0014                 00000018    571+        LGF   R1,V4ADDR     load v4 source
00001126  E781 0000 0806                 00000000    572+        VL    v24,0(R1)     use v24 to test decoder
0000112C  E766 7000 8FA9                             573+        VMALH V22,V22,V23,V24,0    test instruction (dest is a source)
00001132  E760 5030 080E                 000010F0    574+        VST   V22,V1O1       save v1 output
00001138  07FB                                       575+        BR    R11           return
0000113C                                             576+RE1     DC    0F            xl16 expected result
0000113C                                             577+        DROP  R5
0000113C  FE000000 00000002                          578         DC    XL16'FE00000000000002 0000000C000000F4'   result
00001144  0000000C 000000F4
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000114C  FF000000 00000019                          579          DC    XL16'FF00000000000019 00000038000000FA'   v2
00001154  00000038 000000FA
0000115C  FF000000 00000019                          580          DC    XL16'FF00000000000019 00000038000000FA'   v3
00001164  00000038 000000FA
0000116C  00000000 00000000                          581          DC    XL16'0000000000000000 0000000000000000'   v4
00001174  00000000 00000000
                                                     582
                                                     583          VRR_D VMALH,0
00001180                                             584+         DS    0FD
00001180                     00001180                585+         USING *,R5              base for test data and test routine
00001180  000011C8                                   586+T2       DC    A(X2)             address of test routine
00001184  0002                                       587+         DC    H'2'              test number
00001186  00                                         588+         DC    X'00'
00001187  00                                         589+         DC    HL1'0'            m5
00001188  E5D4C1D3 C8404040                         590+         DC    CL8'VMALH'        instruction name
00001190  0000120C                                   591+         DC    A(RE2+16)         address of v2 source
00001194  0000121C                                   592+         DC    A(RE2+32)         address of v3 source
00001198  0000122C                                   593+         DC    A(RE2+48)         address of v4 source
0000119C  00000010                                   594+         DC    A(16)             result length
000011A0  000011FC                                   595+REA2     DC    A(RE2)            result address
000011A8  00000000 00000000                          596+         DS    FD                gap
000011B0  00000000 00000000                          597+V1O2     DS    XL16              V1 output
000011B8  00000000 00000000
000011C0  00000000 00000000                          598+         DS    FD                gap
                                                     599+*
000011C8                                             600+X2       DS    0F
000011C8  E310 5010 0014                 00000010    601+         LGF   R1,V2ADDR         load v2 source
000011CE  E761 0000 0806                 00000000    602+         VL    v22,0(R1)         use v22 to test decoder
000011D4  E310 5014 0014                 00000014    603+         LGF   R1,V3ADDR         load v3 source
000011DA  E771 0000 0806                 00000000    604+         VL    v23,0(R1)         use v23 to test decoder
000011E0  E310 5018 0014                 00000018    605+         LGF   R1,V4ADDR         load v4 source
000011E6  E781 0000 0806                 00000000    606+         VL    v24,0(R1)         use v24 to test decoder
000011EC  E766 7000 8FA9                             607+         VMALH V22,V22,V23,V24,0    test instruction (dest is a source)
000011F2  E760 5030 080E                 000011B0    608+         VST   V22,V1O2           save v1 output
000011F8  07FB                                       609+         BR    R11               return
000011FC                                             610+RE2      DC    0F                xl16 expected result
000011FC                                             611+         DROP  R5
000011FC  FE000001 00000006                         612          DC    XL16'FE00000100000006 0000000C000000F4'   result
00001204  0000000C 000000F4
0000120C  FF0000FF 00000029                          613          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00001214  00000038 000000FA
0000121C  FF000001 00000029                          614          DC    XL16'FF00000100000029 00000038000000FA'   v3
00001224  00000038 000000FA
0000122C  00000001 0000002F                          615          DC    XL16'000000010000002F 0000000000000002'   v4
00001234  00000000 00000002
                                                     616
                                                     617          VRR_D VMALH,0
00001240                                             618+         DS    0FD
00001240                     00001240                619+         USING *,R5              base for test data and test routine
00001240  00001288                                   620+T3       DC    A(X3)             address of test routine
00001244  0003                                       621+         DC    H'3'              test number
00001246  00                                         622+         DC    X'00'
00001247  00                                         623+         DC    HL1'0'            m5
00001248  E5D4C1D3 C8404040                         624+         DC    CL8'VMALH'        instruction name
00001250  000012CC                                   625+         DC    A(RE3+16)         address of v2 source
00001254  000012DC                                   626+         DC    A(RE3+32)         address of v3 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001258  000012EC                          627+          DC    A(RE3+48)          address of v4 source
0000125C  00000010                          628+          DC    A(16)              result length
00001260  000012BC                          629+REA3      DC    A(RE3)             result address
00001268  00000000 00000000                 630+          DS    FD                 gap
00001270  00000000 00000000                 631+V1O3      DS    XL16               V1 output
00001278  00000000 00000000
00001280  00000000 00000000                 632+          DS    FD                 gap
                                            633+*
00001288                                    634+X3        DS    0F
00001288  E310 5010 0014          00000010  635+          LGF   R1,V2ADDR          load v2 source
0000128E  E761 0000 0806          00000000  636+          VL    v22,0(R1)          use v22 to test decoder
00001294  E310 5014 0014          00000014  637+          LGF   R1,V3ADDR          load v3 source
0000129A  E771 0000 0806          00000000  638+          VL    v23,0(R1)          use v23 to test decoder
000012A0  E310 5018 0014          00000018  639+          LGF   R1,V4ADDR          load v4 source
000012A6  E781 0000 0806          00000000  640+          VL    v24,0(R1)          use v24 to test decoder
000012AC  E766 7000 8FA9                    641+          VMALH V22,V22,V23,V24,0    test instruction (dest is a source)
000012B2  E760 5030 080E          00001270  642+          VST   V22,V1O3           save v1 output
000012B8  07FB                              643+          BR    R11                return
000012BC                                    644+RE3       DC    0F                 xl16 expected result
000012BC                                    645+          DROP  R5
000012BC  FF000000 00000000                 646           DC    XL16'FF00000000000000 0000000000000001'   result
000012C4  00000000 00000001
000012CC  FF020304 05060708                 647           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
000012D4  090A0B0C 0D0E0F10
000012DC  FF020304 05060708                 648           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
000012E4  090A0B0C 0D0E0F10
000012EC  FF020304 05060708                 649           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000012F4  090A0B0C 0D0E0F10
                                            650
                                            651           VRR_D VMALH,0
00001300                                    652+          DS    0FD
00001300                    00001300        653+          USING *,R5               base for test data and test routine
00001300  00001348                          654+T4        DC    A(X4)              address of test routine
00001304  0004                              655+          DC    H'4'               test number
00001306  00                                656+          DC    X'00'
00001307  00                                657+          DC    HL1'0'             m5
00001308  E5D4C1D3 C8404040                 658+          DC    CL8'VMALH'         instruction name
00001310  0000138C                          659+          DC    A(RE4+16)          address of v2 source
00001314  0000139C                          660+          DC    A(RE4+32)          address of v3 source
00001318  000013AC                          661+          DC    A(RE4+48)          address of v4 source
0000131C  00000010                          662+          DC    A(16)              result length
00001320  0000137C                          663+REA4      DC    A(RE4)             result address
00001328  00000000 00000000                 664+          DS    FD                 gap
00001330  00000000 00000000                 665+V1O4      DS    XL16               V1 output
00001338  00000000 00000000
00001340  00000000 00000000                 666+          DS    FD                 gap
                                            667+*
00001348                                    668+X4        DS    0F
00001348  E310 5010 0014          00000010  669+          LGF   R1,V2ADDR          load v2 source
0000134E  E761 0000 0806          00000000  670+          VL    v22,0(R1)          use v22 to test decoder
00001354  E310 5014 0014          00000014  671+          LGF   R1,V3ADDR          load v3 source
0000135A  E771 0000 0806          00000000  672+          VL    v23,0(R1)          use v23 to test decoder
00001360  E310 5018 0014          00000018  673+          LGF   R1,V4ADDR          load v4 source
00001366  E781 0000 0806          00000000  674+          VL    v24,0(R1)          use v24 to test decoder
0000136C  E766 7000 8FA9                    675+          VMALH V22,V22,V23,V24,0    test instruction (dest is a source)
00001372  E760 5030 080E          00001330  676+          VST   V22,V1O4           save v1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001378  07FB                                     677+         BR    R11               return
0000137C                                           678+RE4      DC    0F                xl16 expected result
0000137C                                           679+         DROP  R5
0000137C  FF000000 00000000                        680          DC    XL16'FF00000000000000 0000000000000000'   result
00001384  00000000 00000000
0000138C  FF020304 05060708                        681          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001394  090A0B0C 0D0E0F10
0000139C  FF010102 02030304                        682          DC    XL16'FF01010202030304 0405050606070708'   v3
000013A4  04050506 06070708
000013AC  FF020304 05060708                        683          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000013B4  090A0B0C 0D0E0F10
                                                   684
                                                   685          VRR_D VMALH,0
000013C0                                           686+         DS    0FD
000013C0                      000013C0             687+         USING *,R5              base for test data and test routine
000013C0  00001408                                 688+T5       DC    A(X5)             address of test routine
000013C4  0005                                     689+         DC    H'5'              test number
000013C6  00                                       690+         DC    X'00'
000013C7  00                                       691+         DC    HL1'0'            m5
000013C8  E5D4C1D3 C8404040                        692+         DC    CL8'VMALH'        instruction name
000013D0  0000144C                                 693+         DC    A(RE5+16)         address of v2 source
000013D4  0000145C                                 694+         DC    A(RE5+32)         address of v3 source
000013D8  0000146C                                 695+         DC    A(RE5+48)         address of v4 source
000013DC  00000010                                 696+         DC    A(16)             result length
000013E0  0000143C                                 697+REA5     DC    A(RE5)            result address
000013E8  00000000 00000000                        698+         DS    FD                gap
000013F0  00000000 00000000                        699+V1O5     DS    XL16              V1 output
000013F8  00000000 00000000
00001400  00000000 00000000                        700+         DS    FD                gap
                                                   701+*
00001408                                           702+X5       DS    0F
00001408  E310 5010 0014                 00000010  703+         LGF   R1,V2ADDR         load v2 source
0000140E  E761 0000 0806                 00000000  704+         VL    v22,0(R1)         use v22 to test decoder
00001414  E310 5014 0014                 00000014  705+         LGF   R1,V3ADDR         load v3 source
0000141A  E771 0000 0806                 00000000  706+         VL    v23,0(R1)         use v23 to test decoder
00001420  E310 5018 0014                 00000018  707+         LGF   R1,V4ADDR         load v4 source
00001426  E781 0000 0806                 00000000  708+         VL    v24,0(R1)         use v24 to test decoder
0000142C  E766 7000 8FA9                           709+         VMALH V22,V22,V23,V24,0    test instruction (dest is a source)
00001432  E760 5030 080E                 000013F0  710+         VST   V22,V1O5           save v1 output
00001438  07FB                           000013F0  711+         BR    R11               return
0000143C                                 000013F0  712+RE5      DC    0F                xl16 expected result
0000143C                                           713+         DROP  R5
0000143C  FF000000 00000000                        714          DC    XL16'FF00000000000000 0000000000000000'   result
00001444  00000000 00000000
0000144C  FF020304 05060708                        715          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001454  090A0B0C 0D0E0F10
0000145C  FF000000 00000001                        716          DC    XL16'FF00000000000001 0101010101010102'   v3
00001464  01010101 01010102
0000146C  FF020304 05060708                        717          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00001474  090A0B0C 0D0E0F10
                                                   718
                                                   719 * Halfword
                                                   720          VRR_D VMALH,1
00001480                                           721+         DS    0FD
00001480                      00001480             722+         USING *,R5              base for test data and test routine
00001480  000014C8                                 723+T6       DC    A(X6)             address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001484  0006                                     724+         DC    H'6'              test number
00001486  00                                       725+         DC    X'00'
00001487  01                                       726+         DC    HL1'1'            m5
00001488  E5D4C1D3 C8404040                        727+         DC    CL8'VMALH'        instruction name
00001490  0000150C                                 728+         DC    A(RE6+16)         address of v2 source
00001494  0000151C                                 729+         DC    A(RE6+32)         address of v3 source
00001498  0000152C                                 730+         DC    A(RE6+48)         address of v4 source
0000149C  00000010                                 731+         DC    A(16)             result length
000014A0  000014FC                                 732+REA6     DC    A(RE6)            result address
000014A8  00000000 00000000                        733+         DS    FD                gap
000014B0  00000000 00000000                        734+V1O6     DS    XL16              V1 output
000014B8  00000000 00000000
000014C0  00000000 00000000                        735+         DS    FD                gap
                                                   736+*
000014C8                                           737+X6       DS    0F
000014C8  E310 5010 0014                00000010   738+         LGF   R1,V2ADDR         load v2 source
000014CE  E761 0000 0806                00000000   739+         VL    v22,0(R1)         use v22 to test decoder
000014D4  E310 5014 0014                00000014   740+         LGF   R1,V3ADDR         load v3 source
000014DA  E771 0000 0806                00000000   741+         VL    v23,0(R1)         use v23 to test decoder
000014E0  E310 5018 0014                00000018   742+         LGF   R1,V4ADDR         load v4 source
000014E6  E781 0000 0806                00000000   743+         VL    v24,0(R1)         use v24 to test decoder
000014EC  E766 7100 8FA9                           744+         VMALH V22,V22,V23,V24,1    test instruction (dest is a source)
000014F2  E760 5030 080E                000014B0   745+         VST   V22,V1O6           save v1 output
000014F8  07FB                                     746+         BR    R11               return
000014FC                                           747+RE6      DC    0F                xl16 expected result
000014FC                                           748+         DROP  R5
000014FC  FE010000 00000000                        749          DC    XL16'FE01000000000000 0000000000000000'   result
00001504  00000000 00000000
0000150C  FF000000 00000019                        750          DC    XL16'FF00000000000019 00000038000000FA'   v2
00001514  00000038 000000FA
0000151C  FF000000 00000019                        751          DC    XL16'FF00000000000019 00000038000000FA'   v3
00001524  00000038 000000FA
0000152C  00000000 00000000                        752          DC    XL16'0000000000000000 0000000000000000'   v4
00001534  00000000 00000000
                                                   753
                                                   754          VRR_D VMALH,1
00001540                                           755+         DS    0FD
00001540                        00001540           756+         USING *,R5              base for test data and test routine
00001540  00001588                                 757+T7       DC    A(X7)             address of test routine
00001544  0007                                     758+         DC    H'7'              test number
00001546  00                                       759+         DC    X'00'
00001547  01                                       760+         DC    HL1'1'            m5
00001548  E5D4C1D3 C8404040                        761+         DC    CL8'VMALH'        instruction name
00001550  000015CC                                 762+         DC    A(RE7+16)         address of v2 source
00001554  000015DC                                 763+         DC    A(RE7+32)         address of v3 source
00001558  000015EC                                 764+         DC    A(RE7+48)         address of v4 source
0000155C  00000010                                 765+         DC    A(16)             result length
00001560  000015BC                                 766+REA7     DC    A(RE7)            result address
00001568  00000000 00000000                        767+         DS    FD                gap
00001570  00000000 00000000                        768+V1O7     DS    XL16              V1 output
00001578  00000000 00000000
00001580  00000000 00000000                        769+         DS    FD                gap
                                                   770+*
00001588                                           771+X7       DS    0F
00001588  E310 5010 0014                00000010   772+         LGF   R1,V2ADDR         load v2 source
0000158E  E761 0000 0806                00000000   773+         VL    v22,0(R1)         use v22 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001594  E310 5014 0014                 00000014   774+         LGF   R1,V3ADDR          load v3 source
0000159A  E771 0000 0806                 00000000   775+         VL    v23,0(R1)          use v23 to test decoder
000015A0  E310 5018 0014                 00000018   776+         LGF   R1,V4ADDR          load v4 source
000015A6  E781 0000 0806                 00000000   777+         VL    v24,0(R1)          use v24 to test decoder
000015AC  E766 7100 8FA9                            778+         VMALH V22,V22,V23,V24,1    test instruction (dest is a source)
000015B2  E760 5030 080E                 00001570   779+         VST   V22,V1O7            save v1 output
000015B8  07FB                                      780+         BR    R11                return
000015BC                                            781+RE7      DC    0F                 xl16 expected result
000015BC                                            782+         DROP  R5
000015BC  FE010000 00000000                         783          DC    XL16'FE01000000000000 0000000000000000'   result
000015C4  00000000 00000000
000015CC  FF0000FF 00000029                         784          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
000015D4  00000038 000000FA
000015DC  FF000001 00000029                         785          DC    XL16'FF00000100000029 00000038000000FA'   v3
000015E4  00000038 000000FA
000015EC  00000001 0000002F                         786          DC    XL16'000000010000002F 0000000000000002'   v4
000015F4  00000000 00000002
                                                    787
                                                    788          VRR_D VMALH,1
00001600                                            789+         DS    0FD
00001600                         00001600           790+         USING *,R5               base for test data and test routine
00001600  00001648                                  791+T8       DC    A(X8)              address of test routine
00001604  0008                                      792+         DC    H'8'               test number
00001606  00                                        793+         DC    X'00'
00001607  01                                        794+         DC    HL1'1'             m5
00001608  E5D4C1D3 C8404040                         795+         DC    CL8'VMALH'         instruction name
00001610  0000168C                                  796+         DC    A(RE8+16)          address of v2 source
00001614  0000169C                                  797+         DC    A(RE8+32)          address of v3 source
00001618  000016AC                                  798+         DC    A(RE8+48)          address of v4 source
0000161C  00000010                                  799+         DC    A(16)              result length
00001620  0000167C                                  800+REA8     DC    A(RE8)             result address
00001628  00000000 00000000                         801+         DS    FD                 gap
00001630  00000000 00000000                         802+V1O8     DS    XL16               V1 output
00001638  00000000 00000000
00001640  00000000 00000000                         803+         DS    FD                 gap
                                                    804+*
00001648                                            805+X8       DS    0F
00001648  E310 5010 0014                 00000010   806+         LGF   R1,V2ADDR          load v2 source
0000164E  E761 0000 0806                 00000000   807+         VL    v22,0(R1)          use v22 to test decoder
00001654  E310 5014 0014                 00000014   808+         LGF   R1,V3ADDR          load v3 source
0000165A  E771 0000 0806                 00000000   809+         VL    v23,0(R1)          use v23 to test decoder
00001660  E310 5018 0014                 00000018   810+         LGF   R1,V4ADDR          load v4 source
00001666  E781 0000 0806                 00000000   811+         VL    v24,0(R1)          use v24 to test decoder
0000166C  E766 7100 8FA9                            812+         VMALH V22,V22,V23,V24,1    test instruction (dest is a source)
00001672  E760 5030 080E                 00001630   813+         VST   V22,V1O8            save v1 output
00001678  07FB                                      814+         BR    R11                return
0000167C                                            815+RE8      DC    0F                 xl16 expected result
0000167C                                            816+         DROP  R5
0000167C  FE050009 00190031                         817          DC    XL16'FE05000900190031 0051007A00AA00E2'   result
00001684  0051007A 00AA00E2
0000168C  FF020304 05060708                         818          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001694  090A0B0C 0D0E0F10
0000169C  FF020304 05060708                         819          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
000016A4  090A0B0C 0D0E0F10
000016AC  FF020304 05060708                         820          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000016B4  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    821
                                                    822          VRR_D VMALH,1
000016C0                                            823+         DS    0FD
000016C0                      000016C0              824+         USING *,R5              base for test data and test routine
000016C0  00001708                                  825+T9       DC    A(X9)             address of test routine
000016C4  0009                                      826+         DC    H'9'              test number
000016C6  00                                        827+         DC    X'00'
000016C7  01                                        828+         DC    HL1'1'            m5
000016C8  E5D4C1D3 C8404040                         829+         DC    CL8'VMALH'        instruction name
000016D0  0000174C                                  830+         DC    A(RE9+16)         address of v2 source
000016D4  0000175C                                  831+         DC    A(RE9+32)         address of v3 source
000016D8  0000176C                                  832+         DC    A(RE9+48)         address of v4 source
000016DC  00000010                                  833+         DC    A(16)             result length
000016E0  0000173C                                  834+REA9     DC    A(RE9)            result address
000016E8  00000000 00000000                         835+         DS    FD                gap
000016F0  00000000 00000000                         836+V1O9     DS    XL16              V1 output
000016F8  00000000 00000000
00001700  00000000 00000000                         837+         DS    FD                gap
                                                    838+*
00001708                                            839+X9       DS    0F
00001708  E310 5010 0014                 00000010   840+         LGF   R1,V2ADDR         load v2 source
0000170E  E761 0000 0806                 00000000   841+         VL    v22,0(R1)         use v22 to test decoder
00001714  E310 5014 0014                 00000014   842+         LGF   R1,V3ADDR         load v3 source
0000171A  E771 0000 0806                 00000000   843+         VL    v23,0(R1)         use v23 to test decoder
00001720  E310 5018 0014                 00000018   844+         LGF   R1,V4ADDR         load v4 source
00001726  E781 0000 0806                 00000000   845+         VL    v24,0(R1)         use v24 to test decoder
0000172C  E766 7100 8FA9                            846+         VMALH V22,V22,V23,V24,1    test instruction (dest is a source)
00001732  E760 5030 080E                 000016F0   847+         VST   V22,V1O9           save v1 output
00001738  07FB                                      848+         BR    R11               return
0000173C                                            849+RE9      DC    0F                xl16 expected result
0000173C                                            850+         DROP  R5
0000173C  FE040003 000A0015                         851          DC    XL16'FE040003000A0015 00240037004E0069'   result
00001744  00240037 004E0069
0000174C  FF020304 05060708                         852          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001754  090A0B0C 0D0E0F10
0000175C  FF010102 02030304                         853          DC    XL16'FF01010202030304 0405050606070708'   v3
00001764  04050506 06070708
0000176C  FF020304 05060708                         854          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00001774  090A0B0C 0D0E0F10
                                                    855
                                                    856          VRR_D VMALH,1
00001780                                            857+         DS    0FD
00001780                      00001780              858+         USING *,R5              base for test data and test routine
00001780  000017C8                                  859+T10      DC    A(X10)            address of test routine
00001784  000A                                      860+         DC    H'10'             test number
00001786  00                                        861+         DC    X'00'
00001787  01                                        862+         DC    HL1'1'            m5
00001788  E5D4C1D3 C8404040                         863+         DC    CL8'VMALH'        instruction name
00001790  0000180C                                  864+         DC    A(RE10+16)        address of v2 source
00001794  0000181C                                  865+         DC    A(RE10+32)        address of v3 source
00001798  0000182C                                  866+         DC    A(RE10+48)        address of v4 source
0000179C  00000010                                  867+         DC    A(16)             result length
000017A0  000017FC                                  868+REA10    DC    A(RE10)           result address
000017A8  00000000 00000000                         869+         DS    FD                gap
000017B0  00000000 00000000                         870+V1O10    DS    XL16              V1 output
000017B8  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
000017C0  00000000 00000000                        871+         DS    FD                gap
                                                   872+*
000017C8                                           873+X10      DS    0F
000017C8  E310 5010 0014                 00000010  874+         LGF   R1,V2ADDR         load v2 source
000017CE  E761 0000 0806                 00000000  875+         VL    v22,0(R1)         use v22 to test decoder
000017D4  E310 5014 0014                 00000014  876+         LGF   R1,V3ADDR         load v3 source
000017DA  E771 0000 0806                 00000000  877+         VL    v23,0(R1)         use v23 to test decoder
000017E0  E310 5018 0014                 00000018  878+         LGF   R1,V4ADDR         load v4 source
000017E6  E781 0000 0806                 00000000  879+         VL    v24,0(R1)         use v24 to test decoder
000017EC  E766 7100 8FA9                           880+         VMALH V22,V22,V23,V24,1    test instruction (dest is a source)
000017F2  E760 5030 080E                 000017B0  881+         VST   V22,V1O10          save v1 output
000017F8  07FB                                     882+         BR    R11               return
000017FC                                           883+RE10     DC    0F                xl16 expected result
000017FC                                           884+         DROP  R5
000017FC  FE030000 00000000                        885          DC    XL16'FE03000000000000 0009000B000D000F'   result
00001804  0009000B 000D000F
0000180C  FF020304 05060708                        886          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001814  090A0B0C 0D0E0F10
0000181C  FF000000 00000001                        887          DC    XL16'FF00000000000001 0101010101010102'   v3
00001824  01010101 01010102
0000182C  FF020304 05060708                        888          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00001834  090A0B0C 0D0E0F10
                                                   889
                                                   890 * Word
                                                   891          VRR_D VMALH,2
00001840                                           892+         DS    0FD
00001840                 00001840                  893+         USING *,R5              base for test data and test routine
00001840  00001888                                 894+T11      DC    A(X11)            address of test routine
00001844  000B                                     895+         DC    H'11'             test number
00001846  00                                       896+         DC    X'00'
00001847  02                                       897+         DC    HL1'2'            m5
00001848  E5D4C1D3 C8404040                       898+         DC    CL8'VMALH'        instruction name
00001850  000018CC                                 899+         DC    A(RE11+16)        address of v2 source
00001854  000018DC                                 900+         DC    A(RE11+32)        address of v3 source
00001858  000018EC                                 901+         DC    A(RE11+48)        address of v4 source
0000185C  00000010                                 902+         DC    A(16)             result length
00001860  000018BC                                 903+REA11    DC    A(RE11)           result address
00001868  00000000 00000000                        904+         DS    FD                gap
00001870  00000000 00000000                        905+V1O11    DS    XL16              V1 output
00001878  00000000 00000000
00001880  00000000 00000000                        906+         DS    FD                gap
                                                   907+*
00001888                                           908+X11      DS    0F
00001888  E310 5010 0014                 00000010  909+         LGF   R1,V2ADDR         load v2 source
0000188E  E761 0000 0806                 00000000  910+         VL    v22,0(R1)         use v22 to test decoder
00001894  E310 5014 0014                 00000014  911+         LGF   R1,V3ADDR         load v3 source
0000189A  E771 0000 0806                 00000000  912+         VL    v23,0(R1)         use v23 to test decoder
000018A0  E310 5018 0014                 00000018  913+         LGF   R1,V4ADDR         load v4 source
000018A6  E781 0000 0806                 00000000  914+         VL    v24,0(R1)         use v24 to test decoder
000018AC  E766 7200 8FA9                           915+         VMALH V22,V22,V23,V24,2    test instruction (dest is a source)
000018B2  E760 5030 080E                 00001870  916+         VST   V22,V1O11          save v1 output
000018B8  07FB                                     917+         BR    R11               return
000018BC                                           918+RE11     DC    0F                xl16 expected result
000018BC                                           919+         DROP  R5
000018BC  FE010000 00000000                        920          DC    XL16'FE01000000000000 0000000000000000'   result
000018C4  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000018CC  FF000000 00000019                          921          DC    XL16'FF00000000000019 00000038000000FA'   v2
000018D4  00000038 000000FA
000018DC  FF000000 00000019                          922          DC    XL16'FF00000000000019 00000038000000FA'   v3
000018E4  00000038 000000FA
000018EC  00000000 00000000                          923          DC    XL16'0000000000000000 0000000000000000'   v4
000018F4  00000000 00000000
                                                     924
                                                     925          VRR_D VMALH,2
00001900                                             926+         DS    0FD
00001900                        00001900             927+         USING *,R5              base for test data and test routine
00001900  00001948                                   928+T12      DC    A(X12)            address of test routine
00001904  000C                                       929+         DC    H'12'             test number
00001906  00                                         930+         DC    X'00'
00001907  02                                         931+         DC    HL1'2'            m5
00001908  E5D4C1D3 C8404040                         932+         DC    CL8'VMALH'        instruction name
00001910  0000198C                                   933+         DC    A(RE12+16)        address of v2 source
00001914  0000199C                                   934+         DC    A(RE12+32)        address of v3 source
00001918  000019AC                                   935+         DC    A(RE12+48)        address of v4 source
0000191C  00000010                                   936+         DC    A(16)             result length
00001920  0000197C                                   937+REA12    DC    A(RE12)           result address
00001928  00000000 00000000                          938+         DS    FD                gap
00001930  00000000 00000000                          939+V1O12    DS    XL16              V1 output
00001938  00000000 00000000
00001940  00000000 00000000                          940+         DS    FD                gap
                                                     941+*
00001948                                             942+X12      DS    0F
00001948  E310 5010 0014                 00000010    943+         LGF   R1,V2ADDR         load v2 source
0000194E  E761 0000 0806                 00000000    944+         VL    v22,0(R1)         use v22 to test decoder
00001954  E310 5014 0014                 00000014    945+         LGF   R1,V3ADDR         load v3 source
0000195A  E771 0000 0806                 00000000    946+         VL    v23,0(R1)         use v23 to test decoder
00001960  E310 5018 0014                 00000018    947+         LGF   R1,V4ADDR         load v4 source
00001966  E781 0000 0806                 00000000    948+         VL    v24,0(R1)         use v24 to test decoder
0000196C  E766 7200 8FA9                             949+         VMALH V22,V22,V23,V24,2    test instruction (dest is a source)
00001972  E760 5030 080E                 00001930    950+         VST   V22,V1O12          save v1 output
00001978  07FB                                       951+         BR    R11               return
0000197C                                             952+RE12     DC    0F                xl16 expected result
0000197C                                             953+         DROP  R5
0000197C  FE0100FF 00000000                          954          DC    XL16'FE0100FF00000000 0000000000000000'   result
00001984  00000000 00000000
0000198C  FF0000FF 00000029                          955          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00001994  00000038 000000FA
0000199C  FF000001 00000029                          956          DC    XL16'FF00000100000029 00000038000000FA'   v3
000019A4  00000038 000000FA
000019AC  00000001 0000002F                          957          DC    XL16'000000010000002F 0000000000000002'   v4
000019B4  00000000 00000002
                                                     958
                                                     959          VRR_D VMALH,2
000019C0                                             960+         DS    0FD
000019C0                        000019C0             961+         USING *,R5              base for test data and test routine
000019C0  00001A08                                   962+T13      DC    A(X13)            address of test routine
000019C4  000D                                       963+         DC    H'13'             test number
000019C6  00                                         964+         DC    X'00'
000019C7  02                                         965+         DC    HL1'2'            m5
000019C8  E5D4C1D3 C8404040                         966+         DC    CL8'VMALH'        instruction name
000019D0  00001A4C                                   967+         DC    A(RE13+16)        address of v2 source
000019D4  00001A5C                                   968+         DC    A(RE13+32)        address of v3 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000019D8  00001A6C                            969+          DC    A(RE13+48)         address of v4 source
000019DC  00000010                            970+          DC    A(16)              result length
000019E0  00001A3C                            971+REA13     DC    A(RE13)            result address
000019E8  00000000 00000000                   972+          DS    FD                 gap
000019F0  00000000 00000000                   973+V1O13     DS    XL16               V1 output
000019F8  00000000 00000000
00001A00  00000000 00000000                   974+          DS    FD                 gap
                                              975+*
00001A08                                      976+X13       DS    0F
00001A08  E310 5010 0014              00000010 977+          LGF   R1,V2ADDR          load v2 source
00001A0E  E761 0000 0806              00000000 978+          VL    v22,0(R1)          use v22 to test decoder
00001A14  E310 5014 0014              00000014 979+          LGF   R1,V3ADDR          load v3 source
00001A1A  E771 0000 0806              00000000 980+          VL    v23,0(R1)          use v23 to test decoder
00001A20  E310 5018 0014              00000018 981+          LGF   R1,V4ADDR          load v4 source
00001A26  E781 0000 0806              00000000 982+          VL    v24,0(R1)          use v24 to test decoder
00001A2C  E766 7200 8FA9                       983+          VMALH V22,V22,V23,V24,2    test instruction (dest is a source)
00001A32  E760 5030 080E              000019F0 984+          VST   V22,V1O13           save v1 output
00001A38  07FB                                985+          BR    R11                return
00001A3C                                      986+RE13      DC    0F                 xl16 expected result
00001A3C                                      987+          DROP  R5
00001A3C  FE050207 00193C6A                   988           DC    XL16'FE05020700193C6A 0051B52B00AA6E4D'   result
00001A44  0051B52B 00AA6E4D
00001A4C  FF020304 05060708                   989           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001A54  090A0B0C 0D0E0F10
00001A5C  FF020304 05060708                   990           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00001A64  090A0B0C 0D0E0F10
00001A6C  FF020304 05060708                   991           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00001A74  090A0B0C 0D0E0F10
                                              992
                                              993           VRR_D VMALH,2
00001A80                                      994+          DS    0FD
00001A80                      00001A80        995+          USING *,R5               base for test data and test routine
00001A80  00001AC8                            996+T14       DC    A(X14)             address of test routine
00001A84  000E                                997+          DC    H'14'              test number
00001A86  00                                  998+          DC    X'00'
00001A87  02                                  999+          DC    HL1'2'             m5
00001A88  E5D4C1D3 C8404040                  1000+          DC    CL8'VMALH'         instruction name
00001A90  00001B0C                           1001+          DC    A(RE14+16)         address of v2 source
00001A94  00001B1C                           1002+          DC    A(RE14+32)         address of v3 source
00001A98  00001B2C                           1003+          DC    A(RE14+48)         address of v4 source
00001A9C  00000010                           1004+          DC    A(16)              result length
00001AA0  00001AFC                           1005+REA14     DC    A(RE14)            result address
00001AA8  00000000 00000000                  1006+          DS    FD                 gap
00001AB0  00000000 00000000                  1007+V1O14     DS    XL16               V1 output
00001AB8  00000000 00000000
00001AC0  00000000 00000000                  1008+          DS    FD                 gap
                                             1009+*
00001AC8                                     1010+X14       DS    0F
00001AC8  E310 5010 0014              00000010 1011+         LGF   R1,V2ADDR          load v2 source
00001ACE  E761 0000 0806              00000000 1012+         VL    v22,0(R1)          use v22 to test decoder
00001AD4  E310 5014 0014              00000014 1013+         LGF   R1,V3ADDR          load v3 source
00001ADA  E771 0000 0806              00000000 1014+         VL    v23,0(R1)          use v23 to test decoder
00001AE0  E310 5018 0014              00000018 1015+         LGF   R1,V4ADDR          load v4 source
00001AE6  E781 0000 0806              00000000 1016+         VL    v24,0(R1)          use v24 to test decoder
00001AEC  E766 7200 8FA9                       1017+         VMALH V22,V22,V23,V24,2    test instruction (dest is a source)
00001AF2  E760 5030 080E              00001AB0 1018+         VST   V22,V1O14           save v1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001AF8  07FB                           1019+          BR    R11               return
00001AFC                                 1020+RE14      DC    0F                xl16 expected result
00001AFC                                 1021+          DROP  R5
00001AFC  FE040104 000A1B2F              1022           DC    XL16'FE040104000A1B2F 0024558B004EB018'   result
00001B04  0024558B 004EB018
00001B0C  FF020304 05060708              1023           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001B14  090A0B0C 0D0E0F10
00001B1C  FF010102 02030304              1024           DC    XL16'FF01010202030304 0405050606070708'   v3
00001B24  04050506 06070708
00001B2C  FF020304 05060708              1025           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00001B34  090A0B0C 0D0E0F10
                                         1026
                                         1027           VRR_D VMALH,2
00001B40                                 1028+          DS    0FD
00001B40                      00001B40   1029+          USING *,R5              base for test data and test routine
00001B40  00001B88                       1030+T15       DC    A(X15)            address of test routine
00001B44  000F                           1031+          DC    H'15'             test number
00001B46  00                             1032+          DC    X'00'
00001B47  02                             1033+          DC    HL1'2'            m5
00001B48  E5D4C1D3 C8404040              1034+          DC    CL8'VMALH'        instruction name
00001B50  00001BCC                       1035+          DC    A(RE15+16)        address of v2 source
00001B54  00001BDC                       1036+          DC    A(RE15+32)        address of v3 source
00001B58  00001BEC                       1037+          DC    A(RE15+48)        address of v4 source
00001B5C  00000010                       1038+          DC    A(16)             result length
00001B60  00001BBC                       1039+REA15     DC    A(RE15)           result address
00001B68  00000000 00000000              1040+          DS    FD                gap
00001B70  00000000 00000000              1041+V1O15     DS    XL16              V1 output
00001B78  00000000 00000000
00001B80  00000000 00000000              1042+          DS    FD                gap
                                         1043+*
00001B88                                 1044+X15       DS    0F
00001B88  E310 5010 0014       00000010  1045+          LGF   R1,V2ADDR         load v2 source
00001B8E  E761 0000 0806       00000000  1046+          VL    v22,0(R1)         use v22 to test decoder
00001B94  E310 5014 0014       00000014  1047+          LGF   R1,V3ADDR         load v3 source
00001B9A  E771 0000 0806       00000000  1048+          VL    v23,0(R1)         use v23 to test decoder
00001BA0  E310 5018 0014       00000018  1049+          LGF   R1,V4ADDR         load v4 source
00001BA6  E781 0000 0806       00000000  1050+          VL    v24,0(R1)         use v24 to test decoder
00001BAC  E766 7200 8FA9                 1051+          VMALH V22,V22,V23,V24,2    test instruction (dest is a source)
00001BB2  E760 5030 080E       00001B70  1052+          VST   V22,V1O15          save v1 output
00001BB8  07FB                           1053+          BR    R11               return
00001BBC                                 1054+RE15      DC    0F                xl16 expected result
00001BBC                                 1055+          DROP  R5
00001BBC  FE030101 00000000              1056           DC    XL16'FE03010100000000 0009131E000D1B2A'   result
00001BC4  0009131E 000D1B2A
00001BCC  FF020304 05060708              1057           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001BD4  090A0B0C 0D0E0F10
00001BDC  FF000000 00000001              1058           DC    XL16'FF00000000000001 0101010101010102'   v3
00001BE4  01010101 01010102
00001BEC  FF020304 05060708              1059           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00001BF4  090A0B0C 0D0E0F10
                                         1060
                                         1061 *-------------------------------------------------------------------
                                         1062 *  VMAL   - Vector Multiply and Add Low
                                         1063 *-------------------------------------------------------------------
                                         1064 * Byte
                                         1065           VRR_D VMAL,0
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001C00                                          1066+          DS    0FD
00001C00                     00001C00             1067+          USING *,R5              base for test data and test routine
00001C00  00001C48                                1068+T16       DC    A(X16)            address of test routine
00001C04  0010                                    1069+          DC    H'16'             test number
00001C06  00                                      1070+          DC    X'00'
00001C07  00                                      1071+          DC    HL1'0'            m5
00001C08  E5D4C1D3 40404040                       1072+          DC    CL8'VMAL'         instruction name
00001C10  00001C8C                                1073+          DC    A(RE16+16)        address of v2 source
00001C14  00001C9C                                1074+          DC    A(RE16+32)        address of v3 source
00001C18  00001CAC                                1075+          DC    A(RE16+48)        address of v4 source
00001C1C  00000010                                1076+          DC    A(16)             result length
00001C20  00001C7C                                1077+REA16     DC    A(RE16)           result address
00001C28  00000000 00000000                       1078+          DS    FD                gap
00001C30  00000000 00000000                       1079+V1O16     DS    XL16              V1 output
00001C38  00000000 00000000
00001C40  00000000 00000000                       1080+          DS    FD                gap
                                                  1081+*
00001C48                                          1082+X16       DS    0F
00001C48  E310 5010 0014                 00000010 1083+          LGF   R1,V2ADDR         load v2 source
00001C4E  E761 0000 0806                 00000000 1084+          VL    v22,0(R1)         use v22 to test decoder
00001C54  E310 5014 0014                 00000014 1085+          LGF   R1,V3ADDR         load v3 source
00001C5A  E771 0000 0806                 00000000 1086+          VL    v23,0(R1)         use v23 to test decoder
00001C60  E310 5018 0014                 00000018 1087+          LGF   R1,V4ADDR         load v4 source
00001C66  E781 0000 0806                 00000000 1088+          VL    v24,0(R1)         use v24 to test decoder
00001C6C  E766 7000 8FAA                          1089+          VMAL  V22,V22,V23,V24,0    test instruction (dest is a source)
00001C72  E760 5030 080E                 00001C30 1090+          VST   V22,V1O16          save v1 output
00001C78  07FB                                    1091+          BR    R11               return
00001C7C                                          1092+RE16      DC    0F                xl16 expected result
00001C7C                                          1093+          DROP  R5
00001C7C  01000000 00000071                       1094           DC    XL16'0100000000000071 0000004000000024'   result
00001C84  00000040 00000024
00001C8C  FF000000 00000019                       1095           DC    XL16'FF00000000000019 00000038000000FA'   v2
00001C94  00000038 000000FA
00001C9C  FF000000 00000019                       1096           DC    XL16'FF00000000000019 00000038000000FA'   v3
00001CA4  00000038 000000FA
00001CAC  00000000 00000000                       1097           DC    XL16'0000000000000000 0000000000000000'   v4
00001CB4  00000000 00000000
                                                  1098
                                                  1099           VRR_D VMAL,0
00001CC0                                          1100+          DS    0FD
00001CC0                     00001CC0             1101+          USING *,R5              base for test data and test routine
00001CC0  00001D08                                1102+T17       DC    A(X17)            address of test routine
00001CC4  0011                                    1103+          DC    H'17'             test number
00001CC6  00                                      1104+          DC    X'00'
00001CC7  00                                      1105+          DC    HL1'0'            m5
00001CC8  E5D4C1D3 40404040                       1106+          DC    CL8'VMAL'         instruction name
00001CD0  00001D4C                                1107+          DC    A(RE17+16)        address of v2 source
00001CD4  00001D5C                                1108+          DC    A(RE17+32)        address of v3 source
00001CD8  00001D6C                                1109+          DC    A(RE17+48)        address of v4 source
00001CDC  00000010                                1110+          DC    A(16)             result length
00001CE0  00001D3C                                1111+REA17     DC    A(RE17)           result address
00001CE8  00000000 00000000                       1112+          DS    FD                gap
00001CF0  00000000 00000000                       1113+V1O17     DS    XL16              V1 output
00001CF8  00000000 00000000
00001D00  00000000 00000000                       1114+          DS    FD                gap
                                                  1115+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001D08                                           1116+X17      DS    0F
00001D08  E310 5010 0014                 00000010  1117+         LGF   R1,V2ADDR         load v2 source
00001D0E  E761 0000 0806                 00000000  1118+         VL    v22,0(R1)         use v22 to test decoder
00001D14  E310 5014 0014                 00000014  1119+         LGF   R1,V3ADDR         load v3 source
00001D1A  E771 0000 0806                 00000000  1120+         VL    v23,0(R1)         use v23 to test decoder
00001D20  E310 5018 0014                 00000018  1121+         LGF   R1,V4ADDR         load v4 source
00001D26  E781 0000 0806                 00000000  1122+         VL    v24,0(R1)         use v24 to test decoder
00001D2C  E766 7000 8FAA                           1123+         VMAL  V22,V22,V23,V24,0    test instruction (dest is a source)
00001D32  E760 5030 080E                 00001CF0  1124+         VST   V22,V1O17          save v1 output
00001D38  07FB                                     1125+         BR    R11               return
00001D3C                                           1126+RE17     DC    0F                xl16 expected result
00001D3C                                           1127+         DROP  R5
00001D3C  01000000 000000C0                        1128          DC    XL16'0100000000000C0 0000004300000026'   result
00001D44  00000043 00000026
00001D4C  FF0000FF 00000029                        1129          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00001D54  00000038 000000FA
00001D5C  FF000001 00000029                        1130          DC    XL16'FF00000100000029 00000038000000FA'   v3
00001D64  00000038 000000FA
00001D6C  00000001 0000002F                        1131          DC    XL16'000000010000002F 0000000300000002'   v4
00001D74  00000003 00000002
                                                   1132
                                                   1133          VRR_D VMAL,0
00001D80                                           1134+         DS    0FD
00001D80                 00001D80                  1135+         USING *,R5              base for test data and test routine
00001D80  00001DC8                                 1136+T18      DC    A(X18)            address of test routine
00001D84  0012                                     1137+         DC    H'18'             test number
00001D86  00                                       1138+         DC    X'00'
00001D87  00                                       1139+         DC    HL1'0'                m5
00001D88  E5D4C1D3 40404040                        1140+         DC    CL8'VMAL'             instruction name
00001D90  00001E0C                                 1141+         DC    A(RE18+16)        address of v2 source
00001D94  00001E1C                                 1142+         DC    A(RE18+32)        address of v3 source
00001D98  00001E2C                                 1143+         DC    A(RE18+48)        address of v4 source
00001D9C  00000010                                 1144+         DC    A(16)             result length
00001DA0  00001DFC                                 1145+REA18    DC    A(RE18)           result address
00001DA8  00000000 00000000                        1146+         DS    FD                gap
00001DB0  00000000 00000000                        1147+V1O18    DS    XL16              V1 output
00001DB8  00000000 00000000
00001DC0  00000000 00000000                        1148+         DS    FD                gap
                                                   1149+*
00001DC8                                           1150+X18      DS    0F
00001DC8  E310 5010 0014                 00000010  1151+         LGF   R1,V2ADDR         load v2 source
00001DCE  E761 0000 0806                 00000000  1152+         VL    v22,0(R1)         use v22 to test decoder
00001DD4  E310 5014 0014                 00000014  1153+         LGF   R1,V3ADDR         load v3 source
00001DDA  E771 0000 0806                 00000000  1154+         VL    v23,0(R1)         use v23 to test decoder
00001DE0  E310 5018 0014                 00000018  1155+         LGF   R1,V4ADDR         load v4 source
00001DE6  E781 0000 0806                 00000000  1156+         VL    v24,0(R1)         use v24 to test decoder
00001DEC  E766 7000 8FAA                           1157+         VMAL  V22,V22,V23,V24,0    test instruction (dest is a source)
00001DF2  E760 5030 080E                 00001DB0  1158+         VST   V22,V1O18          save v1 output
00001DF8  07FB                                     1159+         BR    R11               return
00001DFC                                           1160+RE18     DC    0F                xl16 expected result
00001DFC                                           1161+         DROP  R5
00001DFC  00060C14 1E2A3848                        1162          DC    XL16'00060C141E2A3848 5A6E849CB6D2F010'   result
00001E04  5A6E849C B6D2F010
00001E0C  FF020304 05060708                        1163          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001E14  090A0B0C 0D0E0F10
00001E1C  FF020304 05060708                        1164          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001E24  090A0B0C 0D0E0F10
00001E2C  FF020304 05060708                        1165          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00001E34  090A0B0C 0D0E0F10
                                                   1166
                                                   1167          VRR_D VMAL,0
00001E40                                           1168+         DS    0FD
00001E40                    00001E40               1169+         USING *,R5              base for test data and test routine
00001E40  00001E88                                 1170+T19      DC    A(X19)            address of test routine
00001E44  0013                                     1171+         DC    H'19'             test number
00001E46  00                                       1172+         DC    X'00'
00001E47  00                                       1173+         DC    HL1'0'            m5
00001E48  E5D4C1D3 40404040                        1174+         DC    CL8'VMAL'         instruction name
00001E50  00001ECC                                 1175+         DC    A(RE19+16)        address of v2 source
00001E54  00001EDC                                 1176+         DC    A(RE19+32)        address of v3 source
00001E58  00001EEC                                 1177+         DC    A(RE19+48)        address of v4 source
00001E5C  00000010                                 1178+         DC    A(16)             result length
00001E60  00001EBC                                 1179+REA19    DC    A(RE19)           result address
00001E68  00000000 00000000                        1180+         DS    FD                gap
00001E70  00000000 00000000                        1181+V1O19    DS    XL16              V1 output
00001E78  00000000 00000000
00001E80  00000000 00000000                        1182+         DS    FD                gap
                                                   1183+*
00001E88                                           1184+X19      DS    0F
00001E88  E310 5010 0014                00000010   1185+         LGF   R1,V2ADDR         load v2 source
00001E8E  E761 0000 0806                00000000   1186+         VL    v22,0(R1)         use v22 to test decoder
00001E94  E310 5014 0014                00000014   1187+         LGF   R1,V3ADDR         load v3 source
00001E9A  E771 0000 0806                00000000   1188+         VL    v23,0(R1)         use v23 to test decoder
00001EA0  E310 5018 0014                00000018   1189+         LGF   R1,V4ADDR         load v4 source
00001EA6  E781 0000 0806                00000000   1190+         VL    v24,0(R1)         use v24 to test decoder
00001EAC  E766 7000 8FAA                           1191+         VMAL  V22,V22,V23,V24,0    test instruction (dest is a source)
00001EB2  E760 5030 080E                00001E70   1192+         VST   V22,V1O19          save v1 output
00001EB8  07FB                                     1193+         BR    R11               return
00001EBC                                           1194+RE19     DC    0F                xl16 expected result
00001EBC                                           1195+         DROP  R5
00001EBC  0004060C 0F181C28                        1196          DC    XL16'0004060C0F181C28 2D3C42545B707890'   result
00001EC4  2D3C4254 5B707890
00001ECC  FF020304 05060708                        1197          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001ED4  090A0B0C 0D0E0F10
00001EDC  FF010102 02030304                        1198          DC    XL16'FF01010202030304 0405050606070708'   v3
00001EE4  04050506 06070708
00001EEC  FF020304 05060708                        1199          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00001EF4  090A0B0C 0D0E0F10
                                                   1200
                                                   1201          VRR_D VMAL,0
00001F00                                           1202+         DS    0FD
00001F00                    00001F00               1203+         USING *,R5              base for test data and test routine
00001F00  00001F48                                 1204+T20      DC    A(X20)            address of test routine
00001F04  0014                                     1205+         DC    H'20'             test number
00001F06  00                                       1206+         DC    X'00'
00001F07  00                                       1207+         DC    HL1'0'            m5
00001F08  E5D4C1D3 40404040                        1208+         DC    CL8'VMAL'         instruction name
00001F10  00001F8C                                 1209+         DC    A(RE20+16)        address of v2 source
00001F14  00001F9C                                 1210+         DC    A(RE20+32)        address of v3 source
00001F18  00001FAC                                 1211+         DC    A(RE20+48)        address of v4 source
00001F1C  00000010                                 1212+         DC    A(16)             result length
00001F20  00001F7C                                 1213+REA20    DC    A(RE20)           result address
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001F28  00000000 00000000                        1214+          DS    FD                gap
00001F30  00000000 00000000                        1215+V1O20     DS    XL16              V1 output
00001F38  00000000 00000000
00001F40  00000000 00000000                        1216+          DS    FD                gap
                                                   1217+*
00001F48                                           1218+X20       DS    0F
00001F48  E310 5010 0014                 00000010  1219+          LGF   R1,V2ADDR         load v2 source
00001F4E  E761 0000 0806                 00000000  1220+          VL    v22,0(R1)         use v22 to test decoder
00001F54  E310 5014 0014                 00000014  1221+          LGF   R1,V3ADDR         load v3 source
00001F5A  E771 0000 0806                 00000000  1222+          VL    v23,0(R1)         use v23 to test decoder
00001F60  E310 5018 0014                 00000018  1223+          LGF   R1,V4ADDR         load v4 source
00001F66  E781 0000 0806                 00000000  1224+          VL    v24,0(R1)         use v24 to test decoder
00001F6C  E766 7000 8FAA                           1225+          VMAL  V22,V22,V23,V24,0    test instruction (dest is a source)
00001F72  E760 5030 080E                 00001F30  1226+          VST   V22,V1O20          save v1 output
00001F78  07FB                                     1227+          BR    R11               return
00001F7C                                           1228+RE20      DC    0F                xl16 expected result
00001F7C                                           1229+          DROP  R5
00001F7C  00020304 05060710                        1230           DC    XL16'0002030405060710 121416181A1C1E30'   result
00001F84  12141618 1A1C1E30
00001F8C  FF020304 05060708                        1231           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00001F94  090A0B0C 0D0E0F10
00001F9C  FF000000 00000001                        1232           DC    XL16'FF00000000000001 0101010101010102'   v3
00001FA4  01010101 01010102
00001FAC  FF020304 05060708                        1233           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00001FB4  090A0B0C 0D0E0F10
                                                   1234
                                                   1235 * Halfword
                                                   1236           VRR_D VMAL,1
00001FC0                                           1237+          DS    0FD
00001FC0                         00001FC0          1238+          USING *,R5              base for test data and test routine
00001FC0  00002008                                 1239+T21       DC    A(X21)            address of test routine
00001FC4  0015                                     1240+          DC    H'21'             test number
00001FC6  00                                       1241+          DC    X'00'
00001FC7  01                                       1242+          DC    HL1'1'            m5
00001FC8  E5D4C1D3 40404040                        1243+          DC    CL8'VMAL'         instruction name
00001FD0  0000204C                                 1244+          DC    A(RE21+16)        address of v2 source
00001FD4  0000205C                                 1245+          DC    A(RE21+32)        address of v3 source
00001FD8  0000206C                                 1246+          DC    A(RE21+48)        address of v4 source
00001FDC  00000010                                 1247+          DC    A(16)             result length
00001FE0  0000203C                                 1248+REA21     DC    A(RE21)           result address
00001FE8  00000000 00000000                        1249+          DS    FD                gap
00001FF0  00000000 00000000                        1250+V1O21     DS    XL16              V1 output
00001FF8  00000000 00000000
00002000  00000000 00000000                        1251+          DS    FD                gap
                                                   1252+*
00002008                                           1253+X21       DS    0F
00002008  E310 5010 0014                 00000010  1254+          LGF   R1,V2ADDR         load v2 source
0000200E  E761 0000 0806                 00000000  1255+          VL    v22,0(R1)         use v22 to test decoder
00002014  E310 5014 0014                 00000014  1256+          LGF   R1,V3ADDR         load v3 source
0000201A  E771 0000 0806                 00000000  1257+          VL    v23,0(R1)         use v23 to test decoder
00002020  E310 5018 0014                 00000018  1258+          LGF   R1,V4ADDR         load v4 source
00002026  E781 0000 0806                 00000000  1259+          VL    v24,0(R1)         use v24 to test decoder
0000202C  E766 7100 8FAA                           1260+          VMAL  V22,V22,V23,V24,1    test instruction (dest is a source)
00002032  E760 5030 080E                 00001FF0  1261+          VST   V22,V1O21          save v1 output
00002038  07FB                                     1262+          BR    R11               return
0000203C                                           1263+RE21      DC    0F                xl16 expected result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000203C                                          1264+          DROP  R5
0000203C  00000000 00000271                       1265           DC    XL16'0000000000000271 00000C400000F424'   result
00002044  00000C40 0000F424
0000204C  FF000000 00000019                       1266           DC    XL16'FF00000000000019 00000038000000FA'   v2
00002054  00000038 000000FA
0000205C  FF000000 00000019                       1267           DC    XL16'FF00000000000019 00000038000000FA'   v3
00002064  00000038 000000FA
0000206C  00000000 00000000                       1268           DC    XL16'0000000000000000 0000000000000000'   v4
00002074  00000000 00000000
                                                  1269
                                                  1270           VRR_D VMAL,1
00002080                                          1271+          DS    0FD
00002080                     00002080             1272+          USING *,R5              base for test data and test routine
00002080  000020C8                                1273+T22       DC    A(X22)            address of test routine
00002084  0016                                    1274+          DC    H'22'             test number
00002086  00                                      1275+          DC    X'00'
00002087  01                                      1276+          DC    HL1'1'            m5
00002088  E5D4C1D3 40404040                       1277+          DC    CL8'VMAL'         instruction name
00002090  0000210C                                1278+          DC    A(RE22+16)        address of v2 source
00002094  0000211C                                1279+          DC    A(RE22+32)        address of v3 source
00002098  0000212C                                1280+          DC    A(RE22+48)        address of v4 source
0000209C  00000010                                1281+          DC    A(16)             result length
000020A0  000020FC                                1282+REA22     DC    A(RE22)           result address
000020A8  00000000 00000000                       1283+          DS    FD                gap
000020B0  00000000 00000000                       1284+V1O22     DS    XL16              V1 output
000020B8  00000000 00000000
000020C0  00000000 00000000                       1285+          DS    FD                gap
                                                  1286+*
000020C8                                          1287+X22       DS    0F
000020C8  E310 5010 0014                 00000010 1288+          LGF   R1,V2ADDR         load v2 source
000020CE  E761 0000 0806                 00000000 1289+          VL    v22,0(R1)         use v22 to test decoder
000020D4  E310 5014 0014                 00000014 1290+          LGF   R1,V3ADDR         load v3 source
000020DA  E771 0000 0806                 00000000 1291+          VL    v23,0(R1)         use v23 to test decoder
000020E0  E310 5018 0014                 00000018 1292+          LGF   R1,V4ADDR         load v4 source
000020E6  E781 0000 0806                 00000000 1293+          VL    v24,0(R1)         use v24 to test decoder
000020EC  E766 7100 8FAA                          1294+          VMAL  V22,V22,V23,V24,1    test instruction (dest is a source)
000020F2  E760 5030 080E                 000020B0 1295+          VST   V22,V1O22          save v1 output
000020F8  07FB                                    1296+          BR    R11               return
000020FC                                          1297+RE22      DC    0F                xl16 expected result
000020FC                                          1298+          DROP  R5
000020FC  00000100 000006C0                       1299           DC    XL16'0000010000006C0 00000C430000F426'   result
00002104  00000C43 0000F426
0000210C  FF0000FF 00000029                       1300           DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00002114  00000038 000000FA
0000211C  FF000001 00000029                       1301           DC    XL16'FF00000100000029 00000038000000FA'   v3
00002124  00000038 000000FA
0000212C  00000001 0000002F                       1302           DC    XL16'000000010000002F 0000000300000002'   v4
00002134  00000003 00000002
                                                  1303
                                                  1304           VRR_D VMAL,1
00002140                                          1305+          DS    0FD
00002140                     00002140             1306+          USING *,R5              base for test data and test routine
00002140  00002188                                1307+T23       DC    A(X23)            address of test routine
00002144  0017                                    1308+          DC    H'23'             test number
00002146  00                                      1309+          DC    X'00'
00002147  01                                      1310+          DC    HL1'1'            m5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002148  E5D4C1D3 40404040                        1311+          DC    CL8'VMAL'          instruction name
00002150  000021CC                                 1312+          DC    A(RE23+16)         address of v2 source
00002154  000021DC                                 1313+          DC    A(RE23+32)         address of v3 source
00002158  000021EC                                 1314+          DC    A(RE23+48)         address of v4 source
0000215C  00000010                                 1315+          DC    A(16)              result length
00002160  000021BC                                 1316+REA23     DC    A(RE23)            result address
00002168  00000000 00000000                        1317+          DS    FD                 gap
00002170  00000000 00000000                        1318+V1O23     DS    XL16               V1 output
00002178  00000000 00000000
00002180  00000000 00000000                        1319+          DS    FD                 gap
                                                   1320+*
00002188                                           1321+X23       DS    0F
00002188  E310 5010 0014                 00000010  1322+          LGF   R1,V2ADDR          load v2 source
0000218E  E761 0000 0806                 00000000  1323+          VL    v22,0(R1)          use v22 to test decoder
00002194  E310 5014 0014                 00000014  1324+          LGF   R1,V3ADDR          load v3 source
0000219A  E771 0000 0806                 00000000  1325+          VL    v23,0(R1)          use v23 to test decoder
000021A0  E310 5018 0014                 00000018  1326+          LGF   R1,V4ADDR          load v4 source
000021A6  E781 0000 0806                 00000000  1327+          VL    v24,0(R1)          use v24 to test decoder
000021AC  E766 7100 8FAA                           1328+          VMAL  V22,V22,V23,V24,1    test instruction (dest is a source)
000021B2  E760 5030 080E                 00002170  1329+          VST   V22,V1O23           save v1 output
000021B8  07FB                                     1330+          BR    R11                return
000021BC                                           1331+RE23      DC    0F                 xl16 expected result
000021BC                                           1332+          DROP  R5
000021BC  FB061B14 412A7748                        1333           DC    XL16'FB061B14412A7748 BD6E139C79D2F010'   result
000021C4  BD6E139C 79D2F010
000021CC  FF020304 05060708                        1334           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
000021D4  090A0B0C 0D0E0F10
000021DC  FF020304 05060708                        1335           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
000021E4  090A0B0C 0D0E0F10
000021EC  FF020304 05060708                        1336           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000021F4  090A0B0C 0D0E0F10
                                                   1337
                                                   1338           VRR_D VMAL,1
00002200                                           1339+          DS    0FD
00002200                          00002200         1340+          USING *,R5               base for test data and test routine
00002200  00002248                                 1341+T24       DC    A(X24)             address of test routine
00002204  0018                                     1342+          DC    H'24'              test number
00002206  00                                       1343+          DC    X'00'
00002207  01                                       1344+          DC    HL1'1'             m5
00002208  E5D4C1D3 40404040                        1345+          DC    CL8'VMAL'          instruction name
00002210  0000228C                                 1346+          DC    A(RE24+16)         address of v2 source
00002214  0000229C                                 1347+          DC    A(RE24+32)         address of v3 source
00002218  000022AC                                 1348+          DC    A(RE24+48)         address of v4 source
0000221C  00000010                                 1349+          DC    A(16)              result length
00002220  0000227C                                 1350+REA24     DC    A(RE24)            result address
00002228  00000000 00000000                        1351+          DS    FD                 gap
00002230  00000000 00000000                        1352+V1O24     DS    XL16               V1 output
00002238  00000000 00000000
00002240  00000000 00000000                        1353+          DS    FD                 gap
                                                   1354+*
00002248                                           1355+X24       DS    0F
00002248  E310 5010 0014                 00000010  1356+          LGF   R1,V2ADDR          load v2 source
0000224E  E761 0000 0806                 00000000  1357+          VL    v22,0(R1)          use v22 to test decoder
00002254  E310 5014 0014                 00000014  1358+          LGF   R1,V3ADDR          load v3 source
0000225A  E771 0000 0806                 00000000  1359+          VL    v23,0(R1)          use v23 to test decoder
00002260  E310 5018 0014                 00000018  1360+          LGF   R1,V4ADDR          load v4 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002266  E781 0000 0806                 00000000  1361+         VL    v24,0(R1)          use v24 to test decoder
0000226C  E766 7100 8FAA                           1362+         VMAL  V22,V22,V23,V24,1    test instruction (dest is a source)
00002272  E760 A030 080E                 00002230  1363+         VST   V22,V1O24           save v1 output
00002278  07FB                                     1364+         BR    R11                return
0000227C                                           1365+RE24     DC    0F                 xl16 expected result
0000227C                                           1366+         DROP  R5
0000227C  FC040D0C 20183B28                        1367          DC    XL16'FC040D0C20183B28 5E3C8954BC70F790'   result
00002284  5E3C8954 BC70F790
0000228C  FF020304 05060708                        1368          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002294  090A0B0C 0D0E0F10
0000229C  FF010102 02030304                        1369          DC    XL16'FF01010202030304 0405050606070708'   v3
000022A4  04050506 06070708
000022AC  FF020304 05060708                        1370          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000022B4  090A0B0C 0D0E0F10
                                                   1371
                                                   1372          VRR_D VMAL,1
000022C0                                           1373+         DS    0FD
000022C0                           000022C0        1374+         USING *,R5               base for test data and test routine
000022C0  00002308                                 1375+T25      DC    A(X25)             address of test routine
000022C4  0019                                     1376+         DC    H'25'              test number
000022C6  00                                       1377+         DC    X'00'
000022C7  01                                       1378+         DC    HL1'1'             m5
000022C8  E5D4C1D3 40404040                        1379+         DC    CL8'VMAL'          instruction name
000022D0  0000234C                                 1380+         DC    A(RE25+16)         address of v2 source
000022D4  0000235C                                 1381+         DC    A(RE25+32)         address of v3 source
000022D8  0000236C                                 1382+         DC    A(RE25+48)         address of v4 source
000022DC  00000010                                 1383+         DC    A(16)              result length
000022E0  0000233C                                 1384+REA25    DC    A(RE25)            result address
000022E8  00000000 00000000                        1385+         DS    FD                 gap
000022F0  00000000 00000000                        1386+V1O25    DS    XL16               V1 output
000022F8  00000000 00000000
00002300  00000000 00000000                        1387+         DS    FD                 gap
                                                   1388+*
00002308                                           1389+X25      DS    0F
00002308  E310 5010 0014                 00000010  1390+         LGF   R1,V2ADDR          load v2 source
0000230E  E761 0000 0806                 00000000  1391+         VL    v22,0(R1)          use v22 to test decoder
00002314  E310 5014 0014                 00000014  1392+         LGF   R1,V3ADDR          load v3 source
0000231A  E771 0000 0806                 00000000  1393+         VL    v23,0(R1)          use v23 to test decoder
00002320  E310 5018 0014                 00000018  1394+         LGF   R1,V4ADDR          load v4 source
00002326  E781 0000 0806                 00000000  1395+         VL    v24,0(R1)          use v24 to test decoder
0000232C  E766 7100 8FAA                           1396+         VMAL  V22,V22,V23,V24,1    test instruction (dest is a source)
00002332  E760 5030 080E                 000022F0  1397+         VST   V22,V1O25           save v1 output
00002338  07FB                                     1398+         BR    R11                return
0000233C                                           1399+RE25     DC    0F                 xl16 expected result
0000233C                                           1400+         DROP  R5
0000233C  FD020304 05060E10                        1401          DC    XL16'FD02030405060E10 1C142218281C3D30'   result
00002344  1C142218 281C3D30
0000234C  FF020304 05060708                        1402          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002354  090A0B0C 0D0E0F10
0000235C  FF000000 00000001                        1403          DC    XL16'FF00000000000001 0101010101010102'   v3
00002364  01010101 01010102
0000236C  FF020304 05060708                        1404          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00002374  090A0B0C 0D0E0F10
                                                   1405
                                                   1406 * Word
                                                   1407          VRR_D VMAL,2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002380                                          1408+          DS    0FD
00002380                      00002380            1409+          USING *,R5              base for test data and test routine
00002380  000023C8                                1410+T26       DC    A(X26)            address of test routine
00002384  001A                                    1411+          DC    H'26'             test number
00002386  00                                      1412+          DC    X'00'
00002387  02                                      1413+          DC    HL1'2'            m5
00002388  E5D4C1D3 40404040                       1414+          DC    CL8'VMAL'         instruction name
00002390  0000240C                                1415+          DC    A(RE26+16)        address of v2 source
00002394  0000241C                                1416+          DC    A(RE26+32)        address of v3 source
00002398  0000242C                                1417+          DC    A(RE26+48)        address of v4 source
0000239C  00000010                                1418+          DC    A(16)             result length
000023A0  000023FC                                1419+REA26     DC    A(RE26)           result address
000023A8  00000000 00000000                       1420+          DS    FD                gap
000023B0  00000000 00000000                       1421+V1O26     DS    XL16              V1 output
000023B8  00000000 00000000
000023C0  00000000 00000000                       1422+          DS    FD                gap
                                                  1423+*
000023C8                                          1424+X26       DS    0F
000023C8  E310 5010 0014                00000010  1425+          LGF   R1,V2ADDR         load v2 source
000023CE  E761 0000 0806                00000000  1426+          VL    v22,0(R1)         use v22 to test decoder
000023D4  E310 5014 0014                00000014  1427+          LGF   R1,V3ADDR         load v3 source
000023DA  E771 0000 0806                00000000  1428+          VL    v23,0(R1)         use v23 to test decoder
000023E0  E310 5018 0014                00000018  1429+          LGF   R1,V4ADDR         load v4 source
000023E6  E781 0000 0806                00000000  1430+          VL    v24,0(R1)         use v24 to test decoder
000023EC  E766 7200 8FAA                          1431+          VMAL  V22,V22,V23,V24,2    test instruction (dest is a source)
000023F2  E760 5030 080E                000023B0  1432+          VST   V22,V1O26          save v1 output
000023F8  07FB                                    1433+          BR    R11               return
000023FC                                          1434+RE26      DC    0F                xl16 expected result
000023FC                                          1435+          DROP  R5
000023FC  00000000 00000271                       1436           DC    XL16'0000000000000271 00000C400000F424'   result
00002404  00000C40 0000F424
0000240C  FF000000 00000019                       1437           DC    XL16'FF00000000000019 00000038000000FA'   v2
00002414  00000038 000000FA
0000241C  FF000000 00000019                       1438           DC    XL16'FF00000000000019 00000038000000FA'   v3
00002424  00000038 000000FA
0000242C  00000000 00000000                       1439           DC    XL16'0000000000000000 0000000000000000'   v4
00002434  00000000 00000000
                                                  1440
                                                  1441           VRR_D VMAL,2
00002440                                          1442+          DS    0FD
00002440                      00002440            1443+          USING *,R5              base for test data and test routine
00002440  00002488                                1444+T27       DC    A(X27)            address of test routine
00002444  001B                                    1445+          DC    H'27'             test number
00002446  00                                      1446+          DC    X'00'
00002447  02                                      1447+          DC    HL1'2'            m5
00002448  E5D4C1D3 40404040                       1448+          DC    CL8'VMAL'         instruction name
00002450  000024CC                                1449+          DC    A(RE27+16)        address of v2 source
00002454  000024DC                                1450+          DC    A(RE27+32)        address of v3 source
00002458  000024EC                                1451+          DC    A(RE27+48)        address of v4 source
0000245C  00000010                                1452+          DC    A(16)             result length
00002460  000024BC                                1453+REA27     DC    A(RE27)           result address
00002468  00000000 00000000                       1454+          DS    FD                gap
00002470  00000000 00000000                       1455+V1O27     DS    XL16              V1 output
00002478  00000000 00000000
00002480  00000000 00000000                       1456+          DS    FD                gap
                                                  1457+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002488                                           1458+X27      DS    0F
00002488  E310 5010 0014                 00000010  1459+         LGF   R1,V2ADDR         load v2 source
0000248E  E761 0000 0806                 00000000  1460+         VL    v22,0(R1)         use v22 to test decoder
00002494  E310 5014 0014                 00000014  1461+         LGF   R1,V3ADDR         load v3 source
0000249A  E771 0000 0806                 00000000  1462+         VL    v23,0(R1)         use v23 to test decoder
000024A0  E310 5018 0014                 00000018  1463+         LGF   R1,V4ADDR         load v4 source
000024A6  E781 0000 0806                 00000000  1464+         VL    v24,0(R1)         use v24 to test decoder
000024AC  E766 7200 8FAA                           1465+         VMAL  V22,V22,V23,V24,2    test instruction (dest is a source)
000024B2  E760 5030 080E                 00002470  1466+         VST   V22,V1O27          save v1 output
000024B8  07FB                                     1467+         BR    R11               return
000024BC                                           1468+RE27     DC    0F                xl16 expected result
000024BC                                           1469+         DROP  R5
000024BC  00000100 000006C0                        1470          DC    XL16'0000010000006C0 00000C430000F426'   result
000024C4  00000C43 0000F426
000024CC  FF0000FF 00000029                        1471          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
000024D4  00000038 000000FA
000024DC  FF000001 00000029                        1472          DC    XL16'FF00000100000029 00000038000000FA'   v3
000024E4  00000038 000000FA
000024EC  00000001 0000002F                        1473          DC    XL16'000000010000002F 0000000300000002'   v4
000024F4  00000003 00000002
                                                   1474
                                                   1475          VRR_D VMAL,2
00002500                                           1476+         DS    0FD
00002500                   00002500                1477+         USING *,R5              base for test data and test routine
00002500  00002548                                 1478+T28      DC    A(X28)            address of test routine
00002504  001C                                     1479+         DC    H'28'             test number
00002506  00                                       1480+         DC    X'00'
00002507  02                                       1481+         DC    HL1'2'            m5
00002508  E5D4C1D3 40404040                       1482+         DC    CL8'VMAL'         instruction name
00002510  0000258C                                 1483+         DC    A(RE28+16)        address of v2 source
00002514  0000259C                                 1484+         DC    A(RE28+32)        address of v3 source
00002518  000025AC                                 1485+         DC    A(RE28+48)        address of v4 source
0000251C  00000010                                 1486+         DC    A(16)             result length
00002520  0000257C                                 1487+REA28    DC    A(RE28)           result address
00002528  00000000 00000000                        1488+         DS    FD                gap
00002530  00000000 00000000                        1489+V1O28    DS    XL16              V1 output
00002538  00000000 00000000
00002540  00000000 00000000                        1490+         DS    FD                gap
                                                   1491+*
00002548                                           1492+X28      DS    0F
00002548  E310 5010 0014                 00000010  1493+         LGF   R1,V2ADDR         load v2 source
0000254E  E761 0000 0806                 00000000  1494+         VL    v22,0(R1)         use v22 to test decoder
00002554  E310 5014 0014                 00000014  1495+         LGF   R1,V3ADDR         load v3 source
0000255A  E771 0000 0806                 00000000  1496+         VL    v23,0(R1)         use v23 to test decoder
00002560  E310 5018 0014                 00000018  1497+         LGF   R1,V4ADDR         load v4 source
00002566  E781 0000 0806                 00000000  1498+         VL    v24,0(R1)         use v24 to test decoder
0000256C  E766 7200 8FAA                           1499+         VMAL  V22,V22,V23,V24,2    test instruction (dest is a source)
00002572  E760 5030 080E                 00002530  1500+         VST   V22,V1O28          save v1 output
00002578  07FB                                     1501+         BR    R11               return
0000257C                                           1502+RE28     DC    0F                xl16 expected result
0000257C                                           1503+         DROP  R5
0000257C  031B1B14 A9977748                        1504          DC    XL16'031B1B14A9977748 BE74139C53B0F010'   result
00002584  BE74139C 53B0F010
0000258C  FF020304 05060708                        1505          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002594  090A0B0C 0D0E0F10
0000259C  FF020304 05060708                        1506          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000025A4  090A0B0C 0D0E0F10
000025AC  FF020304 05060708                        1507          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000025B4  090A0B0C 0D0E0F10
                                                   1508
                                                   1509          VRR_D VMAL,2
000025C0                                           1510+         DS    0FD
000025C0                    000025C0               1511+         USING *,R5              base for test data and test routine
000025C0  00002608                                 1512+T29      DC    A(X29)            address of test routine
000025C4  001D                                     1513+         DC    H'29'             test number
000025C6  00                                       1514+         DC    X'00'
000025C7  02                                       1515+         DC    HL1'2'            m5
000025C8  E5D4C1D3 40404040                        1516+         DC    CL8'VMAL'         instruction name
000025D0  0000264C                                 1517+         DC    A(RE29+16)        address of v2 source
000025D4  0000265C                                 1518+         DC    A(RE29+32)        address of v3 source
000025D8  0000266C                                 1519+         DC    A(RE29+48)        address of v4 source
000025DC  00000010                                 1520+         DC    A(16)             result length
000025E0  0000263C                                 1521+REA29    DC    A(RE29)           result address
000025E8  00000000 00000000                        1522+         DS    FD                gap
000025F0  00000000 00000000                        1523+V1O29    DS    XL16              V1 output
000025F8  00000000 00000000
00002600  00000000 00000000                        1524+         DS    FD                gap
                                                   1525+*
00002608                                           1526+X29      DS    0F
00002608  E310 5010 0014                00000010   1527+         LGF   R1,V2ADDR         load v2 source
0000260E  E761 0000 0806                00000000   1528+         VL    v22,0(R1)         use v22 to test decoder
00002614  E310 5014 0014                00000014   1529+         LGF   R1,V3ADDR         load v3 source
0000261A  E771 0000 0806                00000000   1530+         VL    v23,0(R1)         use v23 to test decoder
00002620  E310 5018 0014                00000018   1531+         LGF   R1,V4ADDR         load v4 source
00002626  E781 0000 0806                00000000   1532+         VL    v24,0(R1)         use v24 to test decoder
0000262C  E766 7200 8FAA                           1533+         VMAL  V22,V22,V23,V24,2    test instruction (dest is a source)
00002632  E760 5030 080E                000025F0   1534+         VST   V22,V1O29          save v1 output
00002638  07FB                                     1535+         BR    R11               return
0000263C                                           1536+RE29     DC    0F                xl16 expected result
0000263C                                           1537+         DROP  R5
0000263C  FE0D0D0C 504B3B28                        1538          DC    XL16'FE0D0D0C504B3B28 D8B98954A157F790'   result
00002644  D8B98954 A157F790
0000264C  FF020304 05060708                        1539          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002654  090A0B0C 0D0E0F10
0000265C  FF010102 02030304                        1540          DC    XL16'FF01010202030304 0405050606070708'   v3
00002664  04050506 06070708
0000266C  FF020304 05060708                        1541          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00002674  090A0B0C 0D0E0F10
                                                   1542
                                                   1543          VRR_D VMAL,2
00002680                                           1544+         DS    0FD
00002680                    00002680               1545+         USING *,R5              base for test data and test routine
00002680  000026C8                                 1546+T30      DC    A(X30)            address of test routine
00002684  001E                                     1547+         DC    H'30'             test number
00002686  00                                       1548+         DC    X'00'
00002687  02                                       1549+         DC    HL1'2'            m5
00002688  E5D4C1D3 40404040                        1550+         DC    CL8'VMAL'         instruction name
00002690  0000270C                                 1551+         DC    A(RE30+16)        address of v2 source
00002694  0000271C                                 1552+         DC    A(RE30+32)        address of v3 source
00002698  0000272C                                 1553+         DC    A(RE30+48)        address of v4 source
0000269C  00000010                                 1554+         DC    A(16)             result length
000026A0  000026FC                                 1555+REA30    DC    A(RE30)           result address
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000026A8  00000000 00000000                        1556+          DS    FD                gap
000026B0  00000000 00000000                        1557+V1O30     DS    XL16              V1 output
000026B8  00000000 00000000
000026C0  00000000 00000000                        1558+          DS    FD                gap
                                                   1559+*
000026C8                                           1560+X30       DS    0F
000026C8  E310 5010 0014                 00000010  1561+           LGF   R1,V2ADDR         load v2 source
000026CE  E761 0000 0806                 00000000  1562+           VL    v22,0(R1)         use v22 to test decoder
000026D4  E310 5014 0014                 00000014  1563+           LGF   R1,V3ADDR         load v3 source
000026DA  E771 0000 0806                 00000000  1564+           VL    v23,0(R1)         use v23 to test decoder
000026E0  E310 5018 0014                 00000018  1565+           LGF   R1,V4ADDR         load v4 source
000026E6  E781 0000 0806                 00000000  1566+           VL    v24,0(R1)         use v24 to test decoder
000026EC  E766 7200 8FAA                           1567+           VMAL  V22,V22,V23,V24,2    test instruction (dest is a source)
000026F2  E760 5030 080E                 000026B0  1568+           VST   V22,V1O30          save v1 output
000026F8  07FB                                     1569+           BR    R11               return
000026FC                                           1570+RE30      DC    0F                xl16 expected result
000026FC                                           1571+          DROP  R5
000026FC  FB020304 0A0C0E10                        1572           DC    XL16'FB0203040A0C0E10 332B221854493D30'   result
00002704  332B2218 54493D30
0000270C  FF020304 05060708                        1573           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002714  090A0B0C 0D0E0F10
0000271C  FF000000 00000001                        1574           DC    XL16'FF00000000000001 0101010101010102'   v3
00002724  01010101 01010102
0000272C  FF020304 05060708                        1575           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00002734  090A0B0C 0D0E0F10
                                                   1576
                                                   1577 *-------------------------------------------------------------------
                                                   1578 *  VMAH   - Vector Multiply and Add High
                                                   1579 *-------------------------------------------------------------------
                                                   1580 * Byte
                                                   1581           VRR_D VMAH,0
00002740                                           1582+          DS    0FD
00002740                      00002740             1583+          USING *,R5              base for test data and test routine
00002740  00002788                                 1584+T31       DC    A(X31)            address of test routine
00002744  001F                                     1585+          DC    H'31'             test number
00002746  00                                       1586+          DC    X'00'
00002747  00                                       1587+          DC    HL1'0'            m5
00002748  E5D4C1C8 40404040                       1588+          DC    CL8'VMAH'         instruction name
00002750  000027CC                                 1589+          DC    A(RE31+16)        address of v2 source
00002754  000027DC                                 1590+          DC    A(RE31+32)        address of v3 source
00002758  000027EC                                 1591+          DC    A(RE31+48)        address of v4 source
0000275C  00000010                                 1592+          DC    A(16)             result length
00002760  000027BC                                 1593+REA31     DC    A(RE31)           result address
00002768  00000000 00000000                        1594+          DS    FD                gap
00002770  00000000 00000000                        1595+V1O31     DS    XL16              V1 output
00002778  00000000 00000000
00002780  00000000 00000000                        1596+          DS    FD                gap
                                                   1597+*
00002788                                           1598+X31       DS    0F
00002788  E310 5010 0014                 00000010  1599+           LGF   R1,V2ADDR         load v2 source
0000278E  E761 0000 0806                 00000000  1600+           VL    v22,0(R1)         use v22 to test decoder
00002794  E310 5014 0014                 00000014  1601+           LGF   R1,V3ADDR         load v3 source
0000279A  E771 0000 0806                 00000000  1602+           VL    v23,0(R1)         use v23 to test decoder
000027A0  E310 5018 0014                 00000018  1603+           LGF   R1,V4ADDR         load v4 source
000027A6  E781 0000 0806                 00000000  1604+           VL    v24,0(R1)         use v24 to test decoder
000027AC  E766 7000 8FAB                           1605+           VMAH  V22,V22,V23,V24,0    test instruction (dest is a source)
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000027B2  E760 5030 080E                 00002770  1606+          VST   V22,V1O31          save v1 output
000027B8  07FB                                     1607+          BR    R11               return
000027BC                                           1608+RE31      DC    0F                xl16 expected result
000027BC                                           1609+          DROP  R5
000027BC  00000000 00000002                        1610           DC    XL16'0000000000000002 0000000C00000000'   result
000027C4  0000000C 00000000
000027CC  FF000000 00000019                        1611           DC    XL16'FF00000000000019 00000038000000FA'   v2
000027D4  00000038 000000FA
000027DC  FF000000 00000019                        1612           DC    XL16'FF00000000000019 00000038000000FA'   v3
000027E4  00000038 000000FA
000027EC  00000000 00000000                        1613           DC    XL16'0000000000000000 0000000000000000'   v4
000027F4  00000000 00000000
                                                   1614
                                                   1615           VRR_D VMAH,0
00002800                                           1616+          DS    0FD
00002800                  00002800                 1617+          USING *,R5              base for test data and test routine
00002800  00002848                                 1618+T32       DC    A(X32)            address of test routine
00002804  0020                                     1619+          DC    H'32'             test number
00002806  00                                       1620+          DC    X'00'
00002807  00                                       1621+          DC    HL1'0'            m5
00002808  E5D4C1C8 40404040                       1622+          DC    CL8'VMAH'         instruction name
00002810  0000288C                                 1623+          DC    A(RE32+16)        address of v2 source
00002814  0000289C                                 1624+          DC    A(RE32+32)        address of v3 source
00002818  000028AC                                 1625+          DC    A(RE32+48)        address of v4 source
0000281C  00000010                                 1626+          DC    A(16)             result length
00002820  0000287C                                 1627+REA32     DC    A(RE32)           result address
00002828  00000000 00000000                        1628+          DS    FD                gap
00002830  00000000 00000000                        1629+V1O32     DS    XL16              V1 output
00002838  00000000 00000000
00002840  00000000 00000000                        1630+          DS    FD                gap
                                                   1631+*
00002848                                           1632+X32       DS    0F
00002848  E310 5010 0014                 00000010  1633+          LGF   R1,V2ADDR         load v2 source
0000284E  E761 0000 0806                 00000000  1634+          VL    v22,0(R1)         use v22 to test decoder
00002854  E310 5014 0014                 00000014  1635+          LGF   R1,V3ADDR         load v3 source
0000285A  E771 0000 0806                 00000000  1636+          VL    v23,0(R1)         use v23 to test decoder
00002860  E310 5018 0014                 00000018  1637+          LGF   R1,V4ADDR         load v4 source
00002866  E781 0000 0806                 00000000  1638+          VL    v24,0(R1)         use v24 to test decoder
0000286C  E766 7000 8FAB                           1639+          VMAH  V22,V22,V23,V24,0    test instruction (dest is a source)
00002872  E760 5030 080E                 00002830  1640+          VST   V22,V1O32          save v1 output
00002878  07FB                                     1641+          BR    R11               return
0000287C                                           1642+RE32      DC    0F                xl16 expected result
0000287C                                           1643+          DROP  R5
0000287C  00000000 00000006                        1644           DC    XL16'0000000000000006 0000000C00000000'   result
00002884  0000000C 00000000
0000288C  FF0000FF 00000029                        1645           DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00002894  00000038 000000FA
0000289C  FF000001 00000029                        1646           DC    XL16'FF00000100000029 00000038000000FA'   v3
000028A4  00000038 000000FA
000028AC  00000001 0000002F                        1647           DC    XL16'000000010000002F 0000000300000002'   v4
000028B4  00000003 00000002
                                                   1648
                                                   1649           VRR_D VMAH,0
000028C0                                           1650+          DS    0FD
000028C0                  000028C0                 1651+          USING *,R5              base for test data and test routine
000028C0  00002908                                 1652+T33       DC    A(X33)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000028C4  0021                                    1653+          DC    H'33'              test number
000028C6  00                                      1654+          DC    X'00'
000028C7  00                                      1655+          DC    HL1'0'             m5
000028C8  E5D4C1C8 40404040                       1656+          DC    CL8'VMAH'          instruction name
000028D0  0000294C                                1657+          DC    A(RE33+16)         address of v2 source
000028D4  0000295C                                1658+          DC    A(RE33+32)         address of v3 source
000028D8  0000296C                                1659+          DC    A(RE33+48)         address of v4 source
000028DC  00000010                                1660+          DC    A(16)              result length
000028E0  0000293C                                1661+REA33     DC    A(RE33)            result address
000028E8  00000000 00000000                       1662+          DS    FD                 gap
000028F0  00000000 00000000                       1663+V1033     DS    XL16               V1 output
000028F8  00000000 00000000
00002900  00000000 00000000                       1664+          DS    FD                 gap
                                                  1665+*
00002908                                          1666+X33       DS    0F
00002908  E310 5010 0014                 00000010 1667+          LGF   R1,V2ADDR          load v2 source
0000290E  E761 0000 0806                 00000000 1668+          VL    v22,0(R1)          use v22 to test decoder
00002914  E310 5014 0014                 00000014 1669+          LGF   R1,V3ADDR          load v3 source
0000291A  E771 0000 0806                 00000000 1670+          VL    v23,0(R1)          use v23 to test decoder
00002920  E310 5018 0014                 00000018 1671+          LGF   R1,V4ADDR          load v4 source
00002926  E781 0000 0806                 00000000 1672+          VL    v24,0(R1)          use v24 to test decoder
0000292C  E766 7000 8FAB                          1673+          VMAH  V22,V22,V23,V24,0    test instruction (dest is a source)
00002932  E760 5030 080E                 000028F0 1674+          VST   V22,V1033           save v1 output
00002938  07FB                                    1675+          BR    R11                return
0000293C                                          1676+RE33      DC    0F                 xl16 expected result
0000293C                                          1677+          DROP  R5
0000293C  FF000000 00000000                       1678           DC    XL16'FF00000000000000 00000000000000FF'   result
00002944  00000000 000000FF
0000294C  FF020304 05060708                       1679           DC    XL16'FF02030405060708 090A0B0C0D0E0FF0'   v2
00002954  090A0B0C 0D0E0FF0
0000295C  01020304 05060708                       1680           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002964  090A0B0C 0D0E0F10
0000296C  FF020304 05060708                       1681           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00002974  090A0B0C 0D0E0F10
                                                  1682
                                                  1683           VRR_D VMAH,0
00002980                                          1684+          DS    0FD
00002980                          00002980        1685+          USING *,R5               base for test data and test routine
00002980  000029C8                                1686+T34       DC    A(X34)             address of test routine
00002984  0022                                    1687+          DC    H'34'              test number
00002986  00                                      1688+          DC    X'00'
00002987  00                                      1689+          DC    HL1'0'             m5
00002988  E5D4C1C8 40404040                       1690+          DC    CL8'VMAH'          instruction name
00002990  00002A0C                                1691+          DC    A(RE34+16)         address of v2 source
00002994  00002A1C                                1692+          DC    A(RE34+32)         address of v3 source
00002998  00002A2C                                1693+          DC    A(RE34+48)         address of v4 source
0000299C  00000010                                1694+          DC    A(16)              result length
000029A0  000029FC                                1695+REA34     DC    A(RE34)            result address
000029A8  00000000 00000000                       1696+          DS    FD                 gap
000029B0  00000000 00000000                       1697+V1034     DS    XL16               V1 output
000029B8  00000000 00000000
000029C0  00000000 00000000                       1698+          DS    FD                 gap
                                                  1699+*
000029C8                                          1700+X34       DS    0F
000029C8  E310 5010 0014                 00000010 1701+          LGF   R1,V2ADDR          load v2 source
000029CE  E761 0000 0806                 00000000 1702+          VL    v22,0(R1)          use v22 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000029D4  E310 5014 0014                 00000014  1703+          LGF   R1,V3ADDR          load v3 source
000029DA  E771 0000 0806                 00000000  1704+          VL    v23,0(R1)          use v23 to test decoder
000029E0  E310 5018 0014                 00000018  1705+          LGF   R1,V4ADDR          load v4 source
000029E6  E781 0000 0806                 00000000  1706+          VL    v24,0(R1)          use v24 to test decoder
000029EC  E766 7000 8FAB                           1707+          VMAH  V22,V22,V23,V24,0    test instruction (dest is a source)
000029F2  E760 5030 080E                 000029B0  1708+          VST   V22,V1O34           save v1 output
000029F8  07FB                                     1709+          BR    R11                return
000029FC                                           1710+RE34      DC    0F                 xl16 expected result
000029FC                                           1711+          DROP  R5
000029FC  FF000000 00000000                        1712           DC    XL16'FF00000000000000 00000000000000FF'   result
00002A04  00000000 000000FF
00002A0C  FF020304 05060708                        1713           DC    XL16'FF02030405060708 090A0B0C0D0E0FF0'   v2
00002A14  090A0B0C 0D0E0FF0
00002A1C  00010102 02030304                        1714           DC    XL16'0001010202030304 0405050606070708'   v3
00002A24  04050506 06070708
00002A2C  FF020304 05060708                        1715           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00002A34  090A0B0C 0D0E0F10
                                                   1716
                                                   1717           VRR_D VMAH,0
00002A40                                           1718+          DS    0FD
00002A40                         00002A40          1719+          USING *,R5               base for test data and test routine
00002A40  00002A88                                 1720+T35       DC    A(X35)             address of test routine
00002A44  0023                                     1721+          DC    H'35'              test number
00002A46  00                                       1722+          DC    X'00'
00002A47  00                                       1723+          DC    HL1'0'             m5
00002A48  E5D4C1C8 40404040                        1724+          DC    CL8'VMAH'          instruction name
00002A50  00002ACC                                 1725+          DC    A(RE35+16)         address of v2 source
00002A54  00002ADC                                 1726+          DC    A(RE35+32)         address of v3 source
00002A58  00002AEC                                 1727+          DC    A(RE35+48)         address of v4 source
00002A5C  00000010                                 1728+          DC    A(16)              result length
00002A60  00002ABC                                 1729+REA35     DC    A(RE35)            result address
00002A68  00000000 00000000                        1730+          DS    FD                 gap
00002A70  00000000 00000000                        1731+V1O35     DS    XL16               V1 output
00002A78  00000000 00000000
00002A80  00000000 00000000                        1732+          DS    FD                 gap
                                                   1733+*
00002A88                                           1734+X35       DS    0F
00002A88  E310 5010 0014                 00000010  1735+          LGF   R1,V2ADDR          load v2 source
00002A8E  E761 0000 0806                 00000000  1736+          VL    v22,0(R1)          use v22 to test decoder
00002A94  E310 5014 0014                 00000014  1737+          LGF   R1,V3ADDR          load v3 source
00002A9A  E771 0000 0806                 00000000  1738+          VL    v23,0(R1)          use v23 to test decoder
00002AA0  E310 5018 0014                 00000018  1739+          LGF   R1,V4ADDR          load v4 source
00002AA6  E781 0000 0806                 00000000  1740+          VL    v24,0(R1)          use v24 to test decoder
00002AAC  E766 7000 8FAB                           1741+          VMAH  V22,V22,V23,V24,0    test instruction (dest is a source)
00002AB2  E760 5030 080E                 00002A70  1742+          VST   V22,V1O35           save v1 output
00002AB8  07FB                                     1743+          BR    R11                return
00002ABC                                           1744+RE35      DC    0F                 xl16 expected result
00002ABC                                           1745+          DROP  R5
00002ABC  FF000000 00000000                        1746           DC    XL16'FF00000000000000 00000000000000FF'   result
00002AC4  00000000 000000FF
00002ACC  FF020304 05060708                        1747           DC    XL16'FF02030405060708 090A0B0C0D0E0FF0'   v2
00002AD4  090A0B0C 0D0E0FF0
00002ADC  00000000 00000001                        1748           DC    XL16'0000000000000001 0101010101010102'   v3
00002AE4  01010101 01010102
00002AEC  FF020304 05060708                        1749           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00002AF4  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1750
                                                    1751 * Halfword
                                                    1752          VRR_D VMAH,1
00002B00                                            1753+         DS    0FD
00002B00                      00002B00              1754+         USING *,R5              base for test data and test routine
00002B00  00002B48                                  1755+T36      DC    A(X36)            address of test routine
00002B04  0024                                      1756+         DC    H'36'             test number
00002B06  00                                        1757+         DC    X'00'
00002B07  01                                        1758+         DC    HL1'1'            m5
00002B08  E5D4C1C8 40404040                         1759+         DC    CL8'VMAH'         instruction name
00002B10  00002B8C                                  1760+         DC    A(RE36+16)        address of v2 source
00002B14  00002B9C                                  1761+         DC    A(RE36+32)        address of v3 source
00002B18  00002BAC                                  1762+         DC    A(RE36+48)        address of v4 source
00002B1C  00000010                                  1763+         DC    A(16)             result length
00002B20  00002B7C                                  1764+REA36    DC    A(RE36)           result address
00002B28  00000000 00000000                         1765+         DS    FD                gap
00002B30  00000000 00000000                         1766+V1O36    DS    XL16              V1 output
00002B38  00000000 00000000
00002B40  00000000 00000000                         1767+         DS    FD                gap
                                                    1768+*
00002B48                                            1769+X36      DS    0F
00002B48  E310 5010 0014                 00000010   1770+         LGF   R1,V2ADDR         load v2 source
00002B4E  E761 0000 0806                 00000000   1771+         VL    v22,0(R1)         use v22 to test decoder
00002B54  E310 5014 0014                 00000014   1772+         LGF   R1,V3ADDR         load v3 source
00002B5A  E771 0000 0806                 00000000   1773+         VL    v23,0(R1)         use v23 to test decoder
00002B60  E310 5018 0014                 00000018   1774+         LGF   R1,V4ADDR         load v4 source
00002B66  E781 0000 0806                 00000000   1775+         VL    v24,0(R1)         use v24 to test decoder
00002B6C  E766 7100 8FAB                            1776+         VMAH  V22,V22,V23,V24,1    test instruction (dest is a source)
00002B72  E760 5030 080E                 00002B30   1777+         VST   V22,V1O36          save v1 output
00002B78  07FB                                      1778+         BR    R11               return
00002B7C                                            1779+RE36     DC    0F                xl16 expected result
00002B7C                                            1780+         DROP  R5
00002B7C  00010000 00000000                         1781          DC    XL16'0001000000000000 0000000000000000'   result
00002B84  00000000 00000000
00002B8C  FF000000 00000019                         1782          DC    XL16'FF00000000000019 00000038000000FA'   v2
00002B94  00000038 000000FA
00002B9C  FF000000 00000019                         1783          DC    XL16'FF00000000000019 00000038000000FA'   v3
00002BA4  00000038 000000FA
00002BAC  00000000 00000000                         1784          DC    XL16'0000000000000000 0000000000000000'   v4
00002BB4  00000000 00000000
                                                    1785
                                                    1786          VRR_D VMAH,1
00002BC0                                            1787+         DS    0FD
00002BC0                      00002BC0              1788+         USING *,R5              base for test data and test routine
00002BC0  00002C08                                  1789+T37      DC    A(X37)            address of test routine
00002BC4  0025                                      1790+         DC    H'37'             test number
00002BC6  00                                        1791+         DC    X'00'
00002BC7  01                                        1792+         DC    HL1'1'            m5
00002BC8  E5D4C1C8 40404040                         1793+         DC    CL8'VMAH'         instruction name
00002BD0  00002C4C                                  1794+         DC    A(RE37+16)        address of v2 source
00002BD4  00002C5C                                  1795+         DC    A(RE37+32)        address of v3 source
00002BD8  00002C6C                                  1796+         DC    A(RE37+48)        address of v4 source
00002BDC  00000010                                  1797+         DC    A(16)             result length
00002BE0  00002C3C                                  1798+REA37    DC    A(RE37)           result address
00002BE8  00000000 00000000                         1799+         DS    FD                gap
00002BF0  00000000 00000000                         1800+V1O37    DS    XL16              V1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002BF8  00000000 00000000
00002C00  00000000 00000000                        1801+         DS    FD                gap
                                                   1802+*
00002C08                                           1803+X37      DS    0F
00002C08  E310 5010 0014                 00000010  1804+         LGF   R1,V2ADDR         load v2 source
00002C0E  E761 0000 0806                 00000000  1805+         VL    v22,0(R1)         use v22 to test decoder
00002C14  E310 5014 0014                 00000014  1806+         LGF   R1,V3ADDR         load v3 source
00002C1A  E771 0000 0806                 00000000  1807+         VL    v23,0(R1)         use v23 to test decoder
00002C20  E310 5018 0014                 00000018  1808+         LGF   R1,V4ADDR         load v4 source
00002C26  E781 0000 0806                 00000000  1809+         VL    v24,0(R1)         use v24 to test decoder
00002C2C  E766 7100 8FAB                           1810+         VMAH  V22,V22,V23,V24,1    test instruction (dest is a source)
00002C32  E760 5030 080E                 00002BF0  1811+         VST   V22,V1O37          save v1 output
00002C38  07FB                                     1812+         BR    R11               return
00002C3C                                           1813+RE37     DC    0F                xl16 expected result
00002C3C                                           1814+         DROP  R5
00002C3C  00010000 00000000                        1815          DC    XL16'0001000000000000 0000000000000000'   result
00002C44  00000000 00000000
00002C4C  FF0000FF 00000029                        1816          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00002C54  00000038 000000FA
00002C5C  FF000001 00000029                        1817          DC    XL16'FF00000100000029 00000038000000FA'   v3
00002C64  00000038 000000FA
00002C6C  00000001 0000002F                        1818          DC    XL16'000000010000002F 0000000300000002'   v4
00002C74  00000003 00000002
                                                   1819
                                                   1820          VRR_D VMAH,1
00002C80                                           1821+         DS    0FD
00002C80                 00002C80                  1822+         USING *,R5              base for test data and test routine
00002C80  00002CC8                                 1823+T38      DC    A(X38)            address of test routine
00002C84  0026                                     1824+         DC    H'38'             test number
00002C86  00                                       1825+         DC    X'00'
00002C87  01                                       1826+         DC    HL1'1'            m5
00002C88  E5D4C1C8 40404040                        1827+         DC    CL8'VMAH'         instruction name
00002C90  00002D0C                                 1828+         DC    A(RE38+16)        address of v2 source
00002C94  00002D1C                                 1829+         DC    A(RE38+32)        address of v3 source
00002C98  00002D2C                                 1830+         DC    A(RE38+48)        address of v4 source
00002C9C  00000010                                 1831+         DC    A(16)             result length
00002CA0  00002CFC                                 1832+REA38    DC    A(RE38)           result address
00002CA8  00000000 00000000                        1833+         DS    FD                gap
00002CB0  00000000 00000000                        1834+V1O38    DS    XL16              V1 output
00002CB8  00000000 00000000
00002CC0  00000000 00000000                        1835+         DS    FD                gap
                                                   1836+*
00002CC8                                           1837+X38      DS    0F
00002CC8  E310 5010 0014                 00000010  1838+         LGF   R1,V2ADDR         load v2 source
00002CCE  E761 0000 0806                 00000000  1839+         VL    v22,0(R1)         use v22 to test decoder
00002CD4  E310 5014 0014                 00000014  1840+         LGF   R1,V3ADDR         load v3 source
00002CDA  E771 0000 0806                 00000000  1841+         VL    v23,0(R1)         use v23 to test decoder
00002CE0  E310 5018 0014                 00000018  1842+         LGF   R1,V4ADDR         load v4 source
00002CE6  E781 0000 0806                 00000000  1843+         VL    v24,0(R1)         use v24 to test decoder
00002CEC  E766 7100 8FAB                           1844+         VMAH  V22,V22,V23,V24,1    test instruction (dest is a source)
00002CF2  E760 5030 080E                 00002CB0  1845+         VST   V22,V1O38          save v1 output
00002CF8  07FB                                     1846+         BR    R11               return
00002CFC                                           1847+RE38     DC    0F                xl16 expected result
00002CFC                                           1848+         DROP  R5
00002CFC  FFFE0009 00190031                        1849          DC    XL16'FFFE000900190031 0051007AFF57FF1F'   result
00002D04  0051007A FF57FF1F
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002D0C  FF020304 05060708                        1850           DC    XL16'FF02030405060708 090A0B0CF30EF110'   v2
00002D14  090A0B0C F30EF110
00002D1C  01020304 05060708                        1851           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
00002D24  090A0B0C 0D0E0F10
00002D2C  FF020304 05060708                        1852           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00002D34  090A0B0C 0D0E0F10
                                                   1853
                                                   1854           VRR_D VMAH,1
00002D40                                           1855+          DS    0FD
00002D40                    00002D40               1856+          USING *,R5              base for test data and test routine
00002D40  00002D88                                 1857+T39       DC    A(X39)            address of test routine
00002D44  0027                                     1858+          DC    H'39'             test number
00002D46  00                                       1859+          DC    X'00'
00002D47  01                                       1860+          DC    HL1'1'            m5
00002D48  E5D4C1C8 40404040                        1861+          DC    CL8'VMAH'         instruction name
00002D50  00002DCC                                 1862+          DC    A(RE39+16)        address of v2 source
00002D54  00002DDC                                 1863+          DC    A(RE39+32)        address of v3 source
00002D58  00002DEC                                 1864+          DC    A(RE39+48)        address of v4 source
00002D5C  00000010                                 1865+          DC    A(16)             result length
00002D60  00002DBC                                 1866+REA39     DC    A(RE39)           result address
00002D68  00000000 00000000                        1867+          DS    FD                gap
00002D70  00000000 00000000                        1868+V1O39     DS    XL16              V1 output
00002D78  00000000 00000000
00002D80  00000000 00000000                        1869+          DS    FD                gap
                                                   1870+*
00002D88                                           1871+X39       DS    0F
00002D88  E310 5010 0014                  00000010 1872+          LGF   R1,V2ADDR         load v2 source
00002D8E  E761 0000 0806                  00000000 1873+          VL    v22,0(R1)         use v22 to test decoder
00002D94  E310 5014 0014                  00000014 1874+          LGF   R1,V3ADDR         load v3 source
00002D9A  E771 0000 0806                  00000000 1875+          VL    v23,0(R1)         use v23 to test decoder
00002DA0  E310 5018 0014                  00000018 1876+          LGF   R1,V4ADDR         load v4 source
00002DA6  E781 0000 0806                  00000000 1877+          VL    v24,0(R1)         use v24 to test decoder
00002DAC  E766 7100 8FAB                           1878+          VMAH  V22,V22,V23,V24,1    test instruction (dest is a source)
00002DB2  E760 5030 080E                  00002D70 1879+          VST   V22,V1O39          save v1 output
00002DB8  07FB                                     1880+          BR    R11               return
00002DBC                                           1881+RE39      DC    0F                xl16 expected result
00002DBC                                           1882+          DROP  R5
00002DBC  FFFF0003 000A0015                        1883           DC    XL16'FFFF0003000A0015 00240037FFB2FF97'   result
00002DC4  00240037 FFB2FF97
00002DCC  FF020304 05060708                        1884           DC    XL16'FF02030405060708 090A0B0CF30EF110'   v2
00002DD4  090A0B0C F30EF110
00002DDC  00010102 02030304                        1885           DC    XL16'0001010202030304 0405050606070708'   v3
00002DE4  04050506 06070708
00002DEC  FF020304 05060708                        1886           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00002DF4  090A0B0C 0D0E0F10
                                                   1887
                                                   1888           VRR_D VMAH,1
00002E00                                           1889+          DS    0FD
00002E00                    00002E00               1890+          USING *,R5              base for test data and test routine
00002E00  00002E48                                 1891+T40       DC    A(X40)            address of test routine
00002E04  0028                                     1892+          DC    H'40'             test number
00002E06  00                                       1893+          DC    X'00'
00002E07  01                                       1894+          DC    HL1'1'            m5
00002E08  E5D4C1C8 40404040                        1895+          DC    CL8'VMAH'         instruction name
00002E10  00002E8C                                 1896+          DC    A(RE40+16)        address of v2 source
00002E14  00002E9C                                 1897+          DC    A(RE40+32)        address of v3 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002E18  00002EAC                          1898+          DC    A(RE40+48)          address of v4 source
00002E1C  00000010                          1899+          DC    A(16)               result length
00002E20  00002E7C                          1900+REA40     DC    A(RE40)             result address
00002E28  00000000 00000000                 1901+          DS    FD                  gap
00002E30  00000000 00000000                 1902+V1O40     DS    XL16                V1 output
00002E38  00000000 00000000
00002E40  00000000 00000000                 1903+          DS    FD                  gap
                                            1904+*
00002E48                                    1905+X40       DS    0F
00002E48  E310 5010 0014          00000010  1906+          LGF   R1,V2ADDR           load v2 source
00002E4E  E761 0000 0806          00000000  1907+          VL    v22,0(R1)           use v22 to test decoder
00002E54  E310 5014 0014          00000014  1908+          LGF   R1,V3ADDR           load v3 source
00002E5A  E771 0000 0806          00000000  1909+          VL    v23,0(R1)           use v23 to test decoder
00002E60  E310 5018 0014          00000018  1910+          LGF   R1,V4ADDR           load v4 source
00002E66  E781 0000 0806          00000000  1911+          VL    v24,0(R1)           use v24 to test decoder
00002E6C  E766 7100 8FAB                    1912+          VMAH  V22,V22,V23,V24,1    test instruction (dest is a source)
00002E72  E760 5030 080E          00002E30  1913+          VST   V22,V1O40            save v1 output
00002E78  07FB                              1914+          BR    R11                 return
00002E7C                                    1915+RE40      DC    0F                  xl16 expected result
00002E7C                                    1916+          DROP  R5
00002E7C  FFFF0000 00000000                 1917           DC    XL16'FFFF000000000000 0009000BFFF3FFF1'   result
00002E84  0009000B FFF3FFF1
00002E8C  FF020304 05060708                 1918           DC    XL16'FF02030405060708 090A0B0CF30EF110'   v2
00002E94  090A0B0C F30EF110
00002E9C  00000000 00000001                 1919           DC    XL16'0000000000000001 0101010101010102'   v3
00002EA4  01010101 01010102
00002EAC  FF020304 05060708                 1920           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00002EB4  090A0B0C 0D0E0F10
                                            1921
                                            1922 * Word
                                            1923           VRR_D VMAH,2
00002EC0                                    1924+          DS    0FD
00002EC0                    00002EC0        1925+          USING *,R5                base for test data and test routine
00002EC0  00002F08                          1926+T41       DC    A(X41)              address of test routine
00002EC4  0029                              1927+          DC    H'41'               test number
00002EC6  00                                1928+          DC    X'00'
00002EC7  02                                1929+          DC    HL1'2'              m5
00002EC8  E5D4C1C8 40404040                 1930+          DC    CL8'VMAH'           instruction name
00002ED0  00002F4C                          1931+          DC    A(RE41+16)          address of v2 source
00002ED4  00002F5C                          1932+          DC    A(RE41+32)          address of v3 source
00002ED8  00002F6C                          1933+          DC    A(RE41+48)          address of v4 source
00002EDC  00000010                          1934+          DC    A(16)               result length
00002EE0  00002F3C                          1935+REA41     DC    A(RE41)             result address
00002EE8  00000000 00000000                 1936+          DS    FD                  gap
00002EF0  00000000 00000000                 1937+V1O41     DS    XL16                V1 output
00002EF8  00000000 00000000
00002F00  00000000 00000000                 1938+          DS    FD                  gap
                                            1939+*
00002F08                                    1940+X41       DS    0F
00002F08  E310 5010 0014          00000010  1941+          LGF   R1,V2ADDR           load v2 source
00002F0E  E761 0000 0806          00000000  1942+          VL    v22,0(R1)           use v22 to test decoder
00002F14  E310 5014 0014          00000014  1943+          LGF   R1,V3ADDR           load v3 source
00002F1A  E771 0000 0806          00000000  1944+          VL    v23,0(R1)           use v23 to test decoder
00002F20  E310 5018 0014          00000018  1945+          LGF   R1,V4ADDR           load v4 source
00002F26  E781 0000 0806          00000000  1946+          VL    v24,0(R1)           use v24 to test decoder
00002F2C  E766 7200 8FAB                    1947+          VMAH  V22,V22,V23,V24,2    test instruction (dest is a source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00002F32  E760 5030 080E                 00002EF0  1948+          VST   V22,V1O41          save v1 output
00002F38  07FB                                     1949+          BR    R11               return
00002F3C                                           1950+RE41      DC    0F                xl16 expected result
00002F3C                                           1951+          DROP  R5
00002F3C  00010000 00000000                        1952           DC    XL16'0001000000000000 0000000000000000'   result
00002F44  00000000 00000000
00002F4C  FF000000 00000019                        1953           DC    XL16'FF00000000000019 00000038000000FA'   v2
00002F54  00000038 000000FA
00002F5C  FF000000 00000019                        1954           DC    XL16'FF00000000000019 00000038000000FA'   v3
00002F64  00000038 000000FA
00002F6C  00000000 00000000                        1955           DC    XL16'0000000000000000 0000000000000000'   v4
00002F74  00000000 00000000
                                                   1956
                                                   1957           VRR_D VMAH,2
00002F80                                           1958+          DS    0FD
00002F80                       00002F80            1959+          USING *,R5              base for test data and test routine
00002F80  00002FC8                                 1960+T42       DC    A(X42)            address of test routine
00002F84  002A                                     1961+          DC    H'42'             test number
00002F86  00                                       1962+          DC    X'00'
00002F87  02                                       1963+          DC    HL1'2'            m5
00002F88  E5D4C1C8 40404040                        1964+          DC    CL8'VMAH'         instruction name
00002F90  0000300C                                 1965+          DC    A(RE42+16)        address of v2 source
00002F94  0000301C                                 1966+          DC    A(RE42+32)        address of v3 source
00002F98  0000302C                                 1967+          DC    A(RE42+48)        address of v4 source
00002F9C  00000010                                 1968+          DC    A(16)             result length
00002FA0  00002FFC                                 1969+REA42     DC    A(RE42)           result address
00002FA8  00000000 00000000                        1970+          DS    FD                gap
00002FB0  00000000 00000000                        1971+V1O42     DS    XL16              V1 output
00002FB8  00000000 00000000
00002FC0  00000000 00000000                        1972+          DS    FD                gap
                                                   1973+*
00002FC8                                           1974+X42       DS    0F
00002FC8  E310 5010 0014                 00000010  1975+          LGF   R1,V2ADDR         load v2 source
00002FCE  E761 0000 0806                 00000000  1976+          VL    v22,0(R1)         use v22 to test decoder
00002FD4  E310 5014 0014                 00000014  1977+          LGF   R1,V3ADDR         load v3 source
00002FDA  E771 0000 0806                 00000000  1978+          VL    v23,0(R1)         use v23 to test decoder
00002FE0  E310 5018 0014                 00000018  1979+          LGF   R1,V4ADDR         load v4 source
00002FE6  E781 0000 0806                 00000000  1980+          VL    v24,0(R1)         use v24 to test decoder
00002FEC  E766 7200 8FAB                           1981+          VMAH  V22,V22,V23,V24,2    test instruction (dest is a source)
00002FF2  E760 5030 080E                 00002FB0  1982+          VST   V22,V1O42          save v1 output
00002FF8  07FB                                     1983+          BR    R11               return
00002FFC                                           1984+RE42      DC    0F                xl16 expected result
00002FFC                                           1985+          DROP  R5
00002FFC  0000FFFF 00000000                        1986           DC    XL16'0000FFFF00000000 0000000000000000'   result
00003004  00000000 00000000
0000300C  FF0000FF 00000029                        1987           DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00003014  00000038 000000FA
0000301C  FF000001 00000029                        1988           DC    XL16'FF00000100000029 00000038000000FA'   v3
00003024  00000038 000000FA
0000302C  00000001 0000002F                        1989           DC    XL16'000000010000002F 0000000300000002'   v4
00003034  00000003 00000002
                                                   1990
                                                   1991           VRR_D VMAH,2
00003040                                           1992+          DS    0FD
00003040                       00003040            1993+          USING *,R5              base for test data and test routine
00003040  00003088                                 1994+T43       DC    A(X43)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003044  002B                                    1995+          DC    H'43'              test number
00003046  00                                      1996+          DC    X'00'
00003047  02                                      1997+          DC    HL1'2'             m5
00003048  E5D4C1C8 40404040                       1998+          DC    CL8'VMAH'          instruction name
00003050  000030CC                                1999+          DC    A(RE43+16)         address of v2 source
00003054  000030DC                                2000+          DC    A(RE43+32)         address of v3 source
00003058  000030EC                                2001+          DC    A(RE43+48)         address of v4 source
0000305C  00000010                                2002+          DC    A(16)              result length
00003060  000030BC                                2003+REA43     DC    A(RE43)            result address
00003068  00000000 00000000                       2004+          DS    FD                 gap
00003070  00000000 00000000                       2005+V1O43     DS    XL16               V1 output
00003078  00000000 00000000
00003080  00000000 00000000                       2006+          DS    FD                 gap
                                                  2007+*
00003088                                          2008+X43       DS    0F
00003088  E310 5010 0014                00000010  2009+          LGF   R1,V2ADDR          load v2 source
0000308E  E761 0000 0806                00000000  2010+          VL    v22,0(R1)          use v22 to test decoder
00003094  E310 5014 0014                00000014  2011+          LGF   R1,V3ADDR          load v3 source
0000309A  E771 0000 0806                00000000  2012+          VL    v23,0(R1)          use v23 to test decoder
000030A0  E310 5018 0014                00000018  2013+          LGF   R1,V4ADDR          load v4 source
000030A6  E781 0000 0806                00000000  2014+          VL    v24,0(R1)          use v24 to test decoder
000030AC  E766 7200 8FAB                          2015+          VMAH  V22,V22,V23,V24,2    test instruction (dest is a source)
000030B2  E760 5030 080E                00003070  2016+          VST   V22,V1O43           save v1 output
000030B8  07FB                                    2017+          BR    R11                return
000030BC                                          2018+RE43      DC    0F                 xl16 expected result
000030BC                                          2019+          DROP  R5
000030BC  FFFF0004 00193C6A                       2020           DC    XL16'FFFF000400193C6A 0051B52BFF5700C5'   result
000030C4  0051B52B FF5700C5
000030CC  FF020304 05060708                       2021           DC    XL16'FF02030405060708 090A0B0CF30E0F10'   v2
000030D4  090A0B0C F30E0F10
000030DC  01020304 05060708                       2022           DC    XL16'0102030405060708 090A0B0C0D0E0F10'   v3
000030E4  090A0B0C 0D0E0F10
000030EC  FF020304 05060708                       2023           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000030F4  090A0B0C 0D0E0F10
                                                  2024
                                                  2025           VRR_D VMAH,2
00003100                                          2026+          DS    0FD
00003100                        00003100          2027+          USING *,R5               base for test data and test routine
00003100  00003148                                2028+T44       DC    A(X44)             address of test routine
00003104  002C                                    2029+          DC    H'44'              test number
00003106  00                                      2030+          DC    X'00'
00003107  02                                      2031+          DC    HL1'2'             m5
00003108  E5D4C1C8 40404040                       2032+          DC    CL8'VMAH'          instruction name
00003110  0000318C                                2033+          DC    A(RE44+16)         address of v2 source
00003114  0000319C                                2034+          DC    A(RE44+32)         address of v3 source
00003118  000031AC                                2035+          DC    A(RE44+48)         address of v4 source
0000311C  00000010                                2036+          DC    A(16)              result length
00003120  0000317C                                2037+REA44     DC    A(RE44)            result address
00003128  00000000 00000000                       2038+          DS    FD                 gap
00003130  00000000 00000000                       2039+V1O44     DS    XL16               V1 output
00003138  00000000 00000000
00003140  00000000 00000000                       2040+          DS    FD                 gap
                                                  2041+*
00003148                                          2042+X44       DS    0F
00003148  E310 5010 0014                00000010  2043+          LGF   R1,V2ADDR          load v2 source
0000314E  E761 0000 0806                00000000  2044+          VL    v22,0(R1)          use v22 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003154  E310 5014 0014                 00000014  2045+          LGF   R1,V3ADDR          load v3 source
0000315A  E771 0000 0806                 00000000  2046+          VL    v23,0(R1)          use v23 to test decoder
00003160  E310 5018 0014                 00000018  2047+          LGF   R1,V4ADDR          load v4 source
00003166  E781 0000 0806                 00000000  2048+          VL    v24,0(R1)          use v24 to test decoder
0000316C  E766 7200 8FAB                           2049+          VMAH  V22,V22,V23,V24,2    test instruction (dest is a source)
00003172  E760 5030 080E                 00003130  2050+          VST   V22,V1O44           save v1 output
00003178  07FB                                     2051+          BR    R11                return
0000317C                                           2052+RE44      DC    0F                 xl16 expected result
0000317C                                           2053+          DROP  R5
0000317C  FFFFFF01 000A1B2F                        2054           DC    XL16'FFFFFF01000A1B2F 0024558BFFB1F961'   result
00003184  0024558B FFB1F961
0000318C  FF020304 05060708                        2055           DC    XL16'FF02030405060708 090A0B0CF30E0F10'   v2
00003194  090A0B0C F30E0F10
0000319C  00010102 02030304                        2056           DC    XL16'0001010202030304 0405050606070708'   v3
000031A4  04050506 06070708
000031AC  FF020304 05060708                        2057           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000031B4  090A0B0C 0D0E0F10
                                                   2058
                                                   2059           VRR_D VMAH,2
000031C0                                           2060+          DS    0FD
000031C0                         000031C0          2061+          USING *,R5               base for test data and test routine
000031C0  00003208                                 2062+T45       DC    A(X45)             address of test routine
000031C4  002D                                     2063+          DC    H'45'              test number
000031C6  00                                       2064+          DC    X'00'
000031C7  02                                       2065+          DC    HL1'2'             m5
000031C8  E5D4C1C8 40404040                        2066+          DC    CL8'VMAH'          instruction name
000031D0  0000324C                                 2067+          DC    A(RE45+16)         address of v2 source
000031D4  0000325C                                 2068+          DC    A(RE45+32)         address of v3 source
000031D8  0000326C                                 2069+          DC    A(RE45+48)         address of v4 source
000031DC  00000010                                 2070+          DC    A(16)              result length
000031E0  0000323C                                 2071+REA45     DC    A(RE45)            result address
000031E8  00000000 00000000                        2072+          DS    FD                 gap
000031F0  00000000 00000000                        2073+V1O45     DS    XL16               V1 output
000031F8  00000000 00000000
00003200  00000000 00000000                        2074+          DS    FD                 gap
                                                   2075+*
00003208                                           2076+X45       DS    0F
00003208  E310 5010 0014                 00000010  2077+          LGF   R1,V2ADDR          load v2 source
0000320E  E761 0000 0806                 00000000  2078+          VL    v22,0(R1)          use v22 to test decoder
00003214  E310 5014 0014                 00000014  2079+          LGF   R1,V3ADDR          load v3 source
0000321A  E771 0000 0806                 00000000  2080+          VL    v23,0(R1)          use v23 to test decoder
00003220  E310 5018 0014                 00000018  2081+          LGF   R1,V4ADDR          load v4 source
00003226  E781 0000 0806                 00000000  2082+          VL    v24,0(R1)          use v24 to test decoder
0000322C  E766 7200 8FAB                           2083+          VMAH  V22,V22,V23,V24,2    test instruction (dest is a source)
00003232  E760 5030 080E                 000031F0  2084+          VST   V22,V1O45           save v1 output
00003238  07FB                                     2085+          BR    R11                return
0000323C                                           2086+RE45      DC    0F                 xl16 expected result
0000323C                                           2087+          DROP  R5
0000323C  FFFFFFFF 00000000                        2088           DC    XL16'FFFFFFFF00000000 0009131EFFF30110'   result
00003244  0009131E FFF30110
0000324C  FF020304 05060708                        2089           DC    XL16'FF02030405060708 090A0B0CF30E0F10'   v2
00003254  090A0B0C F30E0F10
0000325C  00000000 00000001                        2090           DC    XL16'0000000000000001 0101010101010102'   v3
00003264  01010101 01010102
0000326C  FF020304 05060708                        2091           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00003274  090A0B0C 0D0E0F10
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   2092
                                                   2093 *-------------------------------------------------------------------
                                                   2094 *  VMALE  - Vector Multiply and Add Logical Even
                                                   2095 *-------------------------------------------------------------------
                                                   2096 * Byte
                                                   2097          VRR_D VMALE,0
00003280                                           2098+         DS    0FD
00003280                          00003280         2099+         USING *,R5              base for test data and test routine
00003280  000032C8                                 2100+T46      DC    A(X46)            address of test routine
00003284  002E                                     2101+         DC    H'46'             test number
00003286  00                                       2102+         DC    X'00'
00003287  00                                       2103+         DC    HL1'0'            m5
00003288  E5D4C1D3 C5404040                       2104+         DC    CL8'VMALE'        instruction name
00003290  0000330C                                 2105+         DC    A(RE46+16)        address of v2 source
00003294  0000331C                                 2106+         DC    A(RE46+32)        address of v3 source
00003298  0000332C                                 2107+         DC    A(RE46+48)        address of v4 source
0000329C  00000010                                 2108+         DC    A(16)             result length
000032A0  000032FC                                 2109+REA46    DC    A(RE46)           result address
000032A8  00000000 00000000                        2110+         DS    FD                gap
000032B0  00000000 00000000                        2111+V1O46    DS    XL16              V1 output
000032B8  00000000 00000000
000032C0  00000000 00000000                        2112+         DS    FD                gap
                                                   2113+*
000032C8                                           2114+X46      DS    0F
000032C8  E310 5010 0014                 00000010  2115+         LGF   R1,V2ADDR         load v2 source
000032CE  E761 0000 0806                 00000000  2116+         VL    v22,0(R1)         use v22 to test decoder
000032D4  E310 5014 0014                 00000014  2117+         LGF   R1,V3ADDR         load v3 source
000032DA  E771 0000 0806                 00000000  2118+         VL    v23,0(R1)         use v23 to test decoder
000032E0  E310 5018 0014                 00000018  2119+         LGF   R1,V4ADDR         load v4 source
000032E6  E781 0000 0806                 00000000  2120+         VL    v24,0(R1)         use v24 to test decoder
000032EC  E766 7000 8FAC                           2121+         VMALE V22,V22,V23,V24,0    test instruction (dest is a source)
000032F2  E760 5030 080E                 000032B0  2122+         VST   V22,V1O46          save v1 output
000032F8  07FB                                     2123+         BR    R11               return
000032FC                                           2124+RE46     DC    0F                xl16 expected result
000032FC                                           2125+         DROP  R5
000032FC  FE010000 00000000                        2126          DC    XL16'FE01000000000000 0000000000000000'   result
00003304  00000000 00000000
0000330C  FF000000 00000019                        2127          DC    XL16'FF00000000000019 00000038000000FA'   v2
00003314  00000038 000000FA
0000331C  FF000000 00000019                        2128          DC    XL16'FF00000000000019 00000038000000FA'   v3
00003324  00000038 000000FA
0000332C  00000000 00000000                        2129          DC    XL16'0000000000000000 0000000000000000'   v4
00003334  00000000 00000000
                                                   2130
                                                   2131          VRR_D VMALE,0
00003340                                           2132+         DS    0FD
00003340                          00003340         2133+         USING *,R5              base for test data and test routine
00003340  00003388                                 2134+T47      DC    A(X47)            address of test routine
00003344  002F                                     2135+         DC    H'47'             test number
00003346  00                                       2136+         DC    X'00'
00003347  00                                       2137+         DC    HL1'0'            m5
00003348  E5D4C1D3 C5404040                       2138+         DC    CL8'VMALE'        instruction name
00003350  000033CC                                 2139+         DC    A(RE47+16)        address of v2 source
00003354  000033DC                                 2140+         DC    A(RE47+32)        address of v3 source
00003358  000033EC                                 2141+         DC    A(RE47+48)        address of v4 source
0000335C  00000010                                 2142+         DC    A(16)             result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003360  000033BC                          2143+REA47    DC    A(RE47)           result address
00003368  00000000 00000000                 2144+         DS    FD                gap
00003370  00000000 00000000                 2145+V1O47    DS    XL16              V1 output
00003378  00000000 00000000
00003380  00000000 00000000                 2146+         DS    FD                gap
                                            2147+*
00003388                                    2148+X47      DS    0F
00003388  E310 5010 0014          00000010  2149+         LGF   R1,V2ADDR         load v2 source
0000338E  E761 0000 0806          00000000  2150+         VL    v22,0(R1)         use v22 to test decoder
00003394  E310 5014 0014          00000014  2151+         LGF   R1,V3ADDR         load v3 source
0000339A  E771 0000 0806          00000000  2152+         VL    v23,0(R1)         use v23 to test decoder
000033A0  E310 5018 0014          00000018  2153+         LGF   R1,V4ADDR         load v4 source
000033A6  E781 0000 0806          00000000  2154+         VL    v24,0(R1)         use v24 to test decoder
000033AC  E766 7000 8FAC                    2155+         VMALE V22,V22,V23,V24,0    test instruction (dest is a source)
000033B2  E760 5030 080E          00003370  2156+         VST   V22,V1O47          save v1 output
000033B8  07FB                              2157+         BR    R11               return
000033BC                                    2158+RE47     DC    0F                xl16 expected result
000033BC                                    2159+         DROP  R5
000033BC  FE030001 0000002F                 2160          DC    XL16'FE0300010000002F 0000000300000002'   result
000033C4  00000003 00000002
000033CC  FF0000FF 00000029                 2161          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
000033D4  00000038 000000FA
000033DC  FF000001 00000029                 2162          DC    XL16'FF00000100000029 00000038000000FA'   v3
000033E4  00000038 000000FA
000033EC  00020001 0000002F                 2163          DC    XL16'00200010000002F 0000000300000002'   v4
000033F4  00000003 00000002
                                            2164
                                            2165          VRR_D VMALE,0
00003400                                    2166+         DS    0FD
00003400                        00003400    2167+         USING *,R5              base for test data and test routine
00003400  00003448                          2168+T48      DC    A(X48)            address of test routine
00003404  0030                              2169+         DC    H'48'             test number
00003406  00                                2170+         DC    X'00'
00003407  00                                2171+         DC    HL1'0'            m5
00003408  E5D4C1D3 C5404040                 2172+         DC    CL8'VMALE'        instruction name
00003410  0000348C                          2173+         DC    A(RE48+16)        address of v2 source
00003414  0000349C                          2174+         DC    A(RE48+32)        address of v3 source
00003418  000034AC                          2175+         DC    A(RE48+48)        address of v4 source
0000341C  00000010                          2176+         DC    A(16)             result length
00003420  0000347C                          2177+REA48    DC    A(RE48)           result address
00003428  00000000 00000000                 2178+         DS    FD                gap
00003430  00000000 00000000                 2179+V1O48    DS    XL16              V1 output
00003438  00000000 00000000
00003440  00000000 00000000                 2180+         DS    FD                gap
                                            2181+*
00003448                                    2182+X48      DS    0F
00003448  E310 5010 0014          00000010  2183+         LGF   R1,V2ADDR         load v2 source
0000344E  E761 0000 0806          00000000  2184+         VL    v22,0(R1)         use v22 to test decoder
00003454  E310 5014 0014          00000014  2185+         LGF   R1,V3ADDR         load v3 source
0000345A  E771 0000 0806          00000000  2186+         VL    v23,0(R1)         use v23 to test decoder
00003460  E310 5018 0014          00000018  2187+         LGF   R1,V4ADDR         load v4 source
00003466  E781 0000 0806          00000000  2188+         VL    v24,0(R1)         use v24 to test decoder
0000346C  E766 7000 8FAC                    2189+         VMALE V22,V22,V23,V24,0    test instruction (dest is a source)
00003472  E760 5030 080E          00003430  2190+         VST   V22,V1O48          save v1 output
00003478  07FB                              2191+         BR    R11               return
0000347C                                    2192+RE48     DC    0F                xl16 expected result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000347C                                          2193+          DROP  R5
0000347C  FD03030D 051F0739                       2194           DC    XL16'FD03030D051F0739 095B0B850DB70FF1'   result
00003484  095B0B85 0DB70FF1
0000348C  FF020304 05060708                       2195           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00003494  090A0B0C 0D0E0F10
0000349C  FF020304 05060708                       2196           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
000034A4  090A0B0C 0D0E0F10
000034AC  FF020304 05060708                       2197           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000034B4  090A0B0C 0D0E0F10
                                                  2198
                                                  2199           VRR_D VMALE,0
000034C0                                          2200+          DS    0FD
000034C0                      000034C0            2201+          USING *,R5              base for test data and test routine
000034C0  00003508                                2202+T49       DC    A(X49)            address of test routine
000034C4  0031                                    2203+          DC    H'49'             test number
000034C6  00                                      2204+          DC    X'00'
000034C7  00                                      2205+          DC    HL1'0'            m5
000034C8  E5D4C1D3 C5404040                       2206+          DC    CL8'VMALE'        instruction name
000034D0  0000354C                                2207+          DC    A(RE49+16)        address of v2 source
000034D4  0000355C                                2208+          DC    A(RE49+32)        address of v3 source
000034D8  0000356C                                2209+          DC    A(RE49+48)        address of v4 source
000034DC  00000010                                2210+          DC    A(16)             result length
000034E0  0000353C                                2211+REA49     DC    A(RE49)           result address
000034E8  00000000 00000000                       2212+          DS    FD                gap
000034F0  00000000 00000000                       2213+V1O49     DS    XL16              V1 output
000034F8  00000000 00000000
00003500  00000000 00000000                       2214+          DS    FD                gap
                                                  2215+*
00003508                                          2216+X49       DS    0F
00003508  E310 5010 0014                00000010  2217+          LGF   R1,V2ADDR         load v2 source
0000350E  E761 0000 0806                00000000  2218+          VL    v22,0(R1)         use v22 to test decoder
00003514  E310 5014 0014                00000014  2219+          LGF   R1,V3ADDR         load v3 source
0000351A  E771 0000 0806                00000000  2220+          VL    v23,0(R1)         use v23 to test decoder
00003520  E310 5018 0014                00000018  2221+          LGF   R1,V4ADDR         load v4 source
00003526  E781 0000 0806                00000000  2222+          VL    v24,0(R1)         use v24 to test decoder
0000352C  E766 7000 8FAC                          2223+          VMALE V22,V22,V23,V24,0    test instruction (dest is a source)
00003532  E760 5030 080E                000034F0  2224+          VST   V22,V1O49          save v1 output
00003538  07FB                                    2225+          BR    R11               return
0000353C                                          2226+RE49      DC    0F                xl16 expected result
0000353C                                          2227+          DROP  R5
0000353C  FD030307 0510071D                       2228           DC    XL16'FD0303070510071D 092E0B430D5C0F79'   result
00003544  092E0B43 0D5C0F79
0000354C  FF020304 05060708                       2229           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00003554  090A0B0C 0D0E0F10
0000355C  FF010102 02030304                       2230           DC    XL16'FF01010202030304 0405050606070708'   v3
00003564  04050506 06070708
0000356C  FF020304 05060708                       2231           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00003574  090A0B0C 0D0E0F10
                                                  2232
                                                  2233           VRR_D VMALE,0
00003580                                          2234+          DS    0FD
00003580                      00003580            2235+          USING *,R5              base for test data and test routine
00003580  000035C8                                2236+T50       DC    A(X50)            address of test routine
00003584  0032                                    2237+          DC    H'50'             test number
00003586  00                                      2238+          DC    X'00'
00003587  00                                      2239+          DC    HL1'0'            m5
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003588  E5D4C1D3 C5404040                        2240+          DC    CL8'VMALE'         instruction name
00003590  0000360C                                 2241+          DC    A(RE50+16)         address of v2 source
00003594  0000361C                                 2242+          DC    A(RE50+32)         address of v3 source
00003598  0000362C                                 2243+          DC    A(RE50+48)         address of v4 source
0000359C  00000010                                 2244+          DC    A(16)              result length
000035A0  000035FC                                 2245+REA50     DC    A(RE50)            result address
000035A8  00000000 00000000                        2246+          DS    FD                 gap
000035B0  00000000 00000000                        2247+V1O50     DS    XL16               V1 output
000035B8  00000000 00000000
000035C0  00000000 00000000                        2248+          DS    FD                 gap
                                                   2249+*
000035C8                                           2250+X50       DS    0F
000035C8  E310 5010 0014                00000010   2251+          LGF   R1,V2ADDR          load v2 source
000035CE  E761 0000 0806                00000000   2252+          VL    v22,0(R1)          use v22 to test decoder
000035D4  E310 5014 0014                00000014   2253+          LGF   R1,V3ADDR          load v3 source
000035DA  E771 0000 0806                00000000   2254+          VL    v23,0(R1)          use v23 to test decoder
000035E0  E310 5018 0014                00000018   2255+          LGF   R1,V4ADDR          load v4 source
000035E6  E781 0000 0806                00000000   2256+          VL    v24,0(R1)          use v24 to test decoder
000035EC  E766 7000 8FAC                           2257+          VMALE V22,V22,V23,V24,0    test instruction (dest is a source)
000035F2  E760 5030 080E                000035B0   2258+          VST   V22,V1O50           save v1 output
000035F8  07FB                                     2259+          BR    R11                return
000035FC                                           2260+RE50      DC    0F                 xl16 expected result
000035FC                                           2261+          DROP  R5
000035FC  FD030304 05060708                        2262           DC    XL16'FD03030405060708 09130B170D1B0F1F'   result
00003604  09130B17 0D1B0F1F
0000360C  FF020304 05060708                        2263           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00003614  090A0B0C 0D0E0F10
0000361C  FF000000 00000001                        2264           DC    XL16'FF00000000000001 0101010101010102'   v3
00003624  01010101 01010102
0000362C  FF020304 05060708                        2265           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00003634  090A0B0C 0D0E0F10
                                                   2266
                                                   2267 * Halfword
                                                   2268           VRR_D VMALE,1
00003640                                           2269+          DS    0FD
00003640                        00003640           2270+          USING *,R5               base for test data and test routine
00003640  00003688                                 2271+T51       DC    A(X51)             address of test routine
00003644  0033                                     2272+          DC    H'51'              test number
00003646  00                                       2273+          DC    X'00'
00003647  01                                       2274+          DC    HL1'1'             m5
00003648  E5D4C1D3 C5404040                        2275+          DC    CL8'VMALE'         instruction name
00003650  000036CC                                 2276+          DC    A(RE51+16)         address of v2 source
00003654  000036DC                                 2277+          DC    A(RE51+32)         address of v3 source
00003658  000036EC                                 2278+          DC    A(RE51+48)         address of v4 source
0000365C  00000010                                 2279+          DC    A(16)              result length
00003660  000036BC                                 2280+REA51     DC    A(RE51)            result address
00003668  00000000 00000000                        2281+          DS    FD                 gap
00003670  00000000 00000000                        2282+V1O51     DS    XL16               V1 output
00003678  00000000 00000000
00003680  00000000 00000000                        2283+          DS    FD                 gap
                                                   2284+*
00003688                                           2285+X51       DS    0F
00003688  E310 5010 0014                00000010   2286+          LGF   R1,V2ADDR          load v2 source
0000368E  E761 0000 0806                00000000   2287+          VL    v22,0(R1)          use v22 to test decoder
00003694  E310 5014 0014                00000014   2288+          LGF   R1,V3ADDR          load v3 source
0000369A  E771 0000 0806                00000000   2289+          VL    v23,0(R1)          use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000036A0  E310 5018 0014                 00000018  2290+          LGF    R1,V4ADDR          load v4 source
000036A6  E781 0000 0806                 00000000  2291+          VL     v24,0(R1)          use v24 to test decoder
000036AC  E766 7100 8FAC                           2292+          VMALE  V22,V22,V23,V24,1    test instruction (dest is a source)
000036B2  E760 5030 080E                 00003670  2293+          VST    V22,V1O51           save v1 output
000036B8  07FB                                     2294+          BR     R11                return
000036BC                                           2295+RE51      DC     0F                 xl16 expected result
000036BC                                           2296+          DROP   R5
000036BC  FE010000 00000000                        2297           DC     XL16'FE01000000000000 0000000000000000'   result
000036C4  00000000 00000000
000036CC  FF000000 00000019                        2298           DC     XL16'FF00000000000019 00000038000000FA'   v2
000036D4  00000038 000000FA
000036DC  FF000000 00000019                        2299           DC     XL16'FF00000000000019 00000038000000FA'   v3
000036E4  00000038 000000FA
000036EC  00000000 00000000                        2300           DC     XL16'0000000000000000 0000000000000000'   v4
000036F4  00000000 00000000
                                                   2301
                                                   2302           VRR_D  VMALE,1
00003700                                           2303+          DS     0FD
00003700                  00003700                 2304+          USING  *,R5               base for test data and test routine
00003700  00003748                                 2305+T52       DC     A(X52)             address of test routine
00003704  0034                                     2306+          DC     H'52'              test number
00003706  00                                       2307+          DC     X'00'
00003707  01                                       2308+          DC     HL1'1'             m5
00003708  E5D4C1D3 C5404040                       2309+          DC     CL8'VMALE'         instruction name
00003710  0000378C                                 2310+          DC     A(RE52+16)         address of v2 source
00003714  0000379C                                 2311+          DC     A(RE52+32)         address of v3 source
00003718  000037AC                                 2312+          DC     A(RE52+48)         address of v4 source
0000371C  00000010                                 2313+          DC     A(16)              result length
00003720  0000377C                                 2314+REA52     DC     A(RE52)            result address
00003728  00000000 00000000                        2315+          DS     FD                 gap
00003730  00000000 00000000                        2316+V1O52     DS     XL16               V1 output
00003738  00000000 00000000
00003740  00000000 00000000                        2317+          DS     FD                 gap
                                                   2318+*
00003748                                           2319+X52       DS     0F
00003748  E310 5010 0014                 00000010  2320+          LGF    R1,V2ADDR          load v2 source
0000374E  E761 0000 0806                 00000000  2321+          VL     v22,0(R1)          use v22 to test decoder
00003754  E310 5014 0014                 00000014  2322+          LGF    R1,V3ADDR          load v3 source
0000375A  E771 0000 0806                 00000000  2323+          VL     v23,0(R1)          use v23 to test decoder
00003760  E310 5018 0014                 00000018  2324+          LGF    R1,V4ADDR          load v4 source
00003766  E781 0000 0806                 00000000  2325+          VL     v24,0(R1)          use v24 to test decoder
0000376C  E766 7100 8FAC                           2326+          VMALE  V22,V22,V23,V24,1    test instruction (dest is a source)
00003772  E760 5030 080E                 00003730  2327+          VST    V22,V1O52           save v1 output
00003778  07FB                                     2328+          BR     R11                return
0000377C                                           2329+RE52      DC     0F                 xl16 expected result
0000377C                                           2330+          DROP   R5
0000377C  FE030001 0000002F                        2331           DC     XL16'FE0300010000002F 0000000300000002'   result
00003784  00000003 00000002
0000378C  FF0000FF 00000029                        2332           DC     XL16'FF0000FF00000029 00000038000000FA'   v2
00003794  00000038 000000FA
0000379C  FF000001 00000029                        2333           DC     XL16'FF00000100000029 00000038000000FA'   v3
000037A4  00000038 000000FA
000037AC  00020001 0000002F                        2334           DC     XL16'000200010000002F 0000000300000002'   v4
000037B4  00000003 00000002
                                                   2335
                                                   2336           VRR_D  VMALE,1
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000037C0                                          2337+          DS    0FD
000037C0                     000037C0             2338+          USING *,R5              base for test data and test routine
000037C0  00003808                                2339+T53       DC    A(X53)            address of test routine
000037C4  0035                                    2340+          DC    H'53'             test number
000037C6  00                                      2341+          DC    X'00'
000037C7  01                                      2342+          DC    HL1'1'            m5
000037C8  E5D4C1D3 C5404040                       2343+          DC    CL8'VMALE'        instruction name
000037D0  0000384C                                2344+          DC    A(RE53+16)        address of v2 source
000037D4  0000385C                                2345+          DC    A(RE53+32)        address of v3 source
000037D8  0000386C                                2346+          DC    A(RE53+48)        address of v4 source
000037DC  00000010                                2347+          DC    A(16)             result length
000037E0  0000383C                                2348+REA53     DC    A(RE53)           result address
000037E8  00000000 00000000                       2349+          DS    FD                gap
000037F0  00000000 00000000                       2350+V1O53     DS    XL16              V1 output
000037F8  00000000 00000000
00003800  00000000 00000000                       2351+          DS    FD                gap
                                                  2352+*
00003808                                          2353+X53       DS    0F
00003808  E310 5010 0014                 00000010 2354+          LGF   R1,V2ADDR         load v2 source
0000380E  E761 0000 0806                 00000000 2355+          VL    v22,0(R1)         use v22 to test decoder
00003814  E310 5014 0014                 00000014 2356+          LGF   R1,V3ADDR         load v3 source
0000381A  E771 0000 0806                 00000000 2357+          VL    v23,0(R1)         use v23 to test decoder
00003820  E310 5018 0014                 00000018 2358+          LGF   R1,V4ADDR         load v4 source
00003826  E781 0000 0806                 00000000 2359+          VL    v24,0(R1)         use v24 to test decoder
0000382C  E766 7100 8FAC                          2360+          VMALE V22,V22,V23,V24,1    test instruction (dest is a source)
00003832  E760 5030 080E                 000037F0 2361+          VST   V22,V1O53          save v1 output
00003838  07FB                                    2362+          BR    R11               return
0000383C                                          2363+RE53      DC    0F                xl16 expected result
0000383C                                          2364+          DROP  R5
0000383C  FD06FF08 051F432C                       2365           DC    XL16'FD06FF08051F432C 095BBF700DB87BD4'   result
00003844  095BBF70 0DB87BD4
0000384C  FF020304 05060708                       2366           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00003854  090A0B0C 0D0E0F10
0000385C  FF020304 05060708                       2367           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00003864  090A0B0C 0D0E0F10
0000386C  FF020304 05060708                       2368           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00003874  090A0B0C 0D0E0F10
                                                  2369
                                                  2370           VRR_D VMALE,1
00003880                                          2371+          DS    0FD
00003880                     00003880             2372+          USING *,R5              base for test data and test routine
00003880  000038C8                                2373+T54       DC    A(X54)            address of test routine
00003884  0036                                    2374+          DC    H'54'             test number
00003886  00                                      2375+          DC    X'00'
00003887  01                                      2376+          DC    HL1'1'            m5
00003888  E5D4C1D3 C5404040                       2377+          DC    CL8'VMALE'        instruction name
00003890  0000390C                                2378+          DC    A(RE54+16)        address of v2 source
00003894  0000391C                                2379+          DC    A(RE54+32)        address of v3 source
00003898  0000392C                                2380+          DC    A(RE54+48)        address of v4 source
0000389C  00000010                                2381+          DC    A(16)             result length
000038A0  000038FC                                2382+REA54     DC    A(RE54)           result address
000038A8  00000000 00000000                       2383+          DS    FD                gap
000038B0  00000000 00000000                       2384+V1O54     DS    XL16              V1 output
000038B8  00000000 00000000
000038C0  00000000 00000000                       2385+          DS    FD                gap
                                                  2386+*
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000038C8                                           2387+X54      DS    0F
000038C8  E310 5010 0014                 00000010  2388+         LGF   R1,V2ADDR         load v2 source
000038CE  E761 0000 0806                 00000000  2389+         VL    v22,0(R1)         use v22 to test decoder
000038D4  E310 5014 0014                 00000014  2390+         LGF   R1,V3ADDR         load v3 source
000038DA  E771 0000 0806                 00000000  2391+         VL    v23,0(R1)         use v23 to test decoder
000038E0  E310 5018 0014                 00000018  2392+         LGF   R1,V4ADDR         load v4 source
000038E6  E781 0000 0806                 00000000  2393+         VL    v24,0(R1)         use v24 to test decoder
000038EC  E766 7100 8FAC                           2394+         VMALE V22,V22,V23,V24,1    test instruction (dest is a source)
000038F2  E760 5030 080E                 000038B0  2395+         VST   V22,V1O54          save v1 output
000038F8  07FB                                     2396+         BR    R11               return
000038FC                                           2397+RE54     DC    0F                xl16 expected result
000038FC                                           2398+         DROP  R5
000038FC  FD060006 0510221A                        2399          DC    XL16'FD0600060510221A 092E603E0D5CBE72'   result
00003904  092E603E 0D5CBE72
0000390C  FF020304 05060708                        2400          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00003914  090A0B0C 0D0E0F10
0000391C  FF010102 02030304                        2401          DC    XL16'FF01010202030304 0405050606070708'   v3
00003924  04050506 06070708
0000392C  FF020304 05060708                        2402          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00003934  090A0B0C 0D0E0F10
                                                   2403
                                                   2404          VRR_D VMALE,1
00003940                                           2405+         DS    0FD
00003940                      00003940             2406+         USING *,R5              base for test data and test routine
00003940  00003988                                 2407+T55      DC    A(X55)            address of test routine
00003944  0037                                     2408+         DC    H'55'             test number
00003946  00                                       2409+         DC    X'00'
00003947  01                                       2410+         DC    HL1'1'            m5
00003948  E5D4C1D3 C5404040                       2411+         DC    CL8'VMALE'        instruction name
00003950  000039CC                                 2412+         DC    A(RE55+16)        address of v2 source
00003954  000039DC                                 2413+         DC    A(RE55+32)        address of v3 source
00003958  000039EC                                 2414+         DC    A(RE55+48)        address of v4 source
0000395C  00000010                                 2415+         DC    A(16)             result length
00003960  000039BC                                 2416+REA55    DC    A(RE55)           result address
00003968  00000000 00000000                        2417+         DS    FD                gap
00003970  00000000 00000000                        2418+V1O55    DS    XL16              V1 output
00003978  00000000 00000000
00003980  00000000 00000000                        2419+         DS    FD                gap
                                                   2420+*
00003988                                           2421+X55      DS    0F
00003988  E310 5010 0014                 00000010  2422+         LGF   R1,V2ADDR         load v2 source
0000398E  E761 0000 0806                 00000000  2423+         VL    v22,0(R1)         use v22 to test decoder
00003994  E310 5014 0014                 00000014  2424+         LGF   R1,V3ADDR         load v3 source
0000399A  E771 0000 0806                 00000000  2425+         VL    v23,0(R1)         use v23 to test decoder
000039A0  E310 5018 0014                 00000018  2426+         LGF   R1,V4ADDR         load v4 source
000039A6  E781 0000 0806                 00000000  2427+         VL    v24,0(R1)         use v24 to test decoder
000039AC  E766 7100 8FAC                           2428+         VMALE V22,V22,V23,V24,1    test instruction (dest is a source)
000039B2  E760 5030 080E                 00003970  2429+         VST   V22,V1O55          save v1 output
000039B8  07FB                                     2430+         BR    R11               return
000039BC                                           2431+RE55     DC    0F                xl16 expected result
000039BC                                           2432+         DROP  R5
000039BC  FD050104 05060708                        2433          DC    XL16'FD05010405060708 09131E160D1B2A1E'   result
000039C4  09131E16 0D1B2A1E
000039CC  FF020304 05060708                        2434          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
000039D4  090A0B0C 0D0E0F10
000039DC  FF000000 00000001                        2435          DC    XL16'FF00000000000001 0101010101010102'   v3
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000039E4  01010101 01010102
000039EC  FF020304 05060708                        2436           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000039F4  090A0B0C 0D0E0F10
                                                   2437
                                                   2438 * Word
                                                   2439           VRR_D VMALE,2
00003A00                                           2440+          DS    0FD
00003A00                     00003A00              2441+          USING *,R5               base for test data and test routine
00003A00  00003A48                                 2442+T56       DC    A(X56)             address of test routine
00003A04  0038                                     2443+          DC    H'56'              test number
00003A06  00                                       2444+          DC    X'00'
00003A07  02                                       2445+          DC    HL1'2'             m5
00003A08  E5D4C1D3 C5404040                        2446+          DC    CL8'VMALE'         instruction name
00003A10  00003A8C                                 2447+          DC    A(RE56+16)         address of v2 source
00003A14  00003A9C                                 2448+          DC    A(RE56+32)         address of v3 source
00003A18  00003AAC                                 2449+          DC    A(RE56+48)         address of v4 source
00003A1C  00000010                                 2450+          DC    A(16)              result length
00003A20  00003A7C                                 2451+REA56     DC    A(RE56)            result address
00003A28  00000000 00000000                        2452+          DS    FD                 gap
00003A30  00000000 00000000                        2453+V1O56     DS    XL16               V1 output
00003A38  00000000 00000000
00003A40  00000000 00000000                        2454+          DS    FD                 gap
                                                   2455+*
00003A48                                           2456+X56       DS    0F
00003A48  E310 5010 0014                 00000010  2457+          LGF   R1,V2ADDR          load v2 source
00003A4E  E761 0000 0806                 00000000  2458+          VL    v22,0(R1)          use v22 to test decoder
00003A54  E310 5014 0014                 00000014  2459+          LGF   R1,V3ADDR          load v3 source
00003A5A  E771 0000 0806                 00000000  2460+          VL    v23,0(R1)          use v23 to test decoder
00003A60  E310 5018 0014                 00000018  2461+          LGF   R1,V4ADDR          load v4 source
00003A66  E781 0000 0806                 00000000  2462+          VL    v24,0(R1)          use v24 to test decoder
00003A6C  E766 7200 8FAC                           2463+          VMALE V22,V22,V23,V24,2    test instruction (dest is a source)
00003A72  E760 5030 080E                 00003A30  2464+          VST   V22,V1O56           save v1 output
00003A78  07FB                                     2465+          BR    R11                return
00003A7C                                           2466+RE56      DC    0F                 xl16 expected result
00003A7C                                           2467+          DROP  R5
00003A7C  FE010000 00000000                        2468           DC    XL16'FE01000000000000 0000000000000C40'   result
00003A84  00000000 00000C40
00003A8C  FF000000 00000019                        2469           DC    XL16'FF00000000000019 00000038000000FA'   v2
00003A94  00000038 000000FA
00003A9C  FF000000 00000019                        2470           DC    XL16'FF00000000000019 00000038000000FA'   v3
00003AA4  00000038 000000FA
00003AAC  00000000 00000000                        2471           DC    XL16'0000000000000000 0000000000000000'   v4
00003AB4  00000000 00000000
                                                   2472
                                                   2473           VRR_D VMALE,2
00003AC0                                           2474+          DS    0FD
00003AC0                     00003AC0              2475+          USING *,R5               base for test data and test routine
00003AC0  00003B08                                 2476+T57       DC    A(X57)             address of test routine
00003AC4  0039                                     2477+          DC    H'57'              test number
00003AC6  00                                       2478+          DC    X'00'
00003AC7  02                                       2479+          DC    HL1'2'             m5
00003AC8  E5D4C1D3 C5404040                        2480+          DC    CL8'VMALE'         instruction name
00003AD0  00003B4C                                 2481+          DC    A(RE57+16)         address of v2 source
00003AD4  00003B5C                                 2482+          DC    A(RE57+32)         address of v3 source
00003AD8  00003B6C                                 2483+          DC    A(RE57+48)         address of v4 source
00003ADC  00000010                                 2484+          DC    A(16)              result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003AE0  00003B3C                        2485+REA57    DC    A(RE57)           result address
00003AE8  00000000 00000000               2486+         DS    FD                gap
00003AF0  00000000 00000000               2487+V1O57    DS    XL16              V1 output
00003AF8  00000000 00000000
00003B00  00000000 00000000               2488+         DS    FD                gap
                                          2489+*
00003B08                                  2490+X57      DS    0F
00003B08  E310 5010 0014          00000010 2491+         LGF   R1,V2ADDR         load v2 source
00003B0E  E761 0000 0806          00000000 2492+         VL    v22,0(R1)         use v22 to test decoder
00003B14  E310 5014 0014          00000014 2493+         LGF   R1,V3ADDR         load v3 source
00003B1A  E771 0000 0806          00000000 2494+         VL    v23,0(R1)         use v23 to test decoder
00003B20  E310 5018 0014          00000018 2495+         LGF   R1,V4ADDR         load v4 source
00003B26  E781 0000 0806          00000000 2496+         VL    v24,0(R1)         use v24 to test decoder
00003B2C  E766 7200 8FAC                   2497+         VMALE V22,V22,V23,V24,2    test instruction (dest is a source)
00003B32  E760 5030 080E          00003AF0 2498+         VST   V22,V1O57          save v1 output
00003B38  07FB                             2499+         BR    R11               return
00003B3C                                   2500+RE57     DC    0F                xl16 expected result
00003B3C                                   2501+         DROP  R5
00003B3C  FE030100 0000012E                2502          DC    XL16'FE0301000000012E 0000000300000C42'   result
00003B44  00000003 00000C42
00003B4C  FF0000FF 00000029                2503          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00003B54  00000038 000000FA
00003B5C  FF000001 00000029                2504          DC    XL16'FF00000100000029 00000038000000FA'   v3
00003B64  00000038 000000FA
00003B6C  00020001 0000002F                2505          DC    XL16'00020001000002F 0000000300000002'   v4
00003B74  00000003 00000002
                                           2506
                                           2507          VRR_D VMALE,2
00003B80                                   2508+         DS    0FD
00003B80                        00003B80   2509+         USING *,R5              base for test data and test routine
00003B80  00003BC8                         2510+T58      DC    A(X58)            address of test routine
00003B84  003A                             2511+         DC    H'58'             test number
00003B86  00                               2512+         DC    X'00'
00003B87  02                               2513+         DC    HL1'2'            m5
00003B88  E5D4C1D3 C5404040                2514+         DC    CL8'VMALE'        instruction name
00003B90  00003C0C                         2515+         DC    A(RE58+16)        address of v2 source
00003B94  00003C1C                         2516+         DC    A(RE58+32)        address of v3 source
00003B98  00003C2C                         2517+         DC    A(RE58+48)        address of v4 source
00003B9C  00000010                         2518+         DC    A(16)             result length
00003BA0  00003BFC                         2519+REA58    DC    A(RE58)           result address
00003BA8  00000000 00000000                2520+         DS    FD                gap
00003BB0  00000000 00000000                2521+V1O58    DS    XL16              V1 output
00003BB8  00000000 00000000
00003BC0  00000000 00000000                2522+         DS    FD                gap
                                           2523+*
00003BC8                                   2524+X58      DS    0F
00003BC8  E310 5010 0014          00000010 2525+         LGF   R1,V2ADDR         load v2 source
00003BCE  E761 0000 0806          00000000 2526+         VL    v22,0(R1)         use v22 to test decoder
00003BD4  E310 5014 0014          00000014 2527+         LGF   R1,V3ADDR         load v3 source
00003BDA  E771 0000 0806          00000000 2528+         VL    v23,0(R1)         use v23 to test decoder
00003BE0  E310 5018 0014          00000018 2529+         LGF   R1,V4ADDR         load v4 source
00003BE6  E781 0000 0806          00000000 2530+         VL    v24,0(R1)         use v24 to test decoder
00003BEC  E766 7200 8FAC                   2531+         VMALE V22,V22,V23,V24,2    test instruction (dest is a source)
00003BF2  E760 5030 080E          00003BB0 2532+         VST   V22,V1O58          save v1 output
00003BF8  07FB                             2533+         BR    R11               return
00003BFC                                   2534+RE58     DC    0F                xl16 expected result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003BFC                                           2535+          DROP  R5
00003BFC  FD07050A 091F1F18                        2536           DC    XL16'FD07050A091F1F18 095BC037C27817A0'   result
00003C04  095BC037 C27817A0
00003C0C  FF020304 05060708                        2537           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00003C14  090A0B0C 0D0E0F10
00003C1C  FF020304 05060708                        2538           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00003C24  090A0B0C 0D0E0F10
00003C2C  FF020304 05060708                        2539           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00003C34  090A0B0C 0D0E0F10
                                                   2540
                                                   2541           VRR_D VMALE,2
00003C40                                           2542+          DS    0FD
00003C40                      00003C40             2543+          USING *,R5              base for test data and test routine
00003C40  00003C88                                 2544+T59       DC    A(X59)            address of test routine
00003C44  003B                                     2545+          DC    H'59'             test number
00003C46  00                                       2546+          DC    X'00'
00003C47  02                                       2547+          DC    HL1'2'            m5
00003C48  E5D4C1D3 C5404040                        2548+          DC    CL8'VMALE'        instruction name
00003C50  00003CCC                                 2549+          DC    A(RE59+16)        address of v2 source
00003C54  00003CDC                                 2550+          DC    A(RE59+32)        address of v3 source
00003C58  00003CEC                                 2551+          DC    A(RE59+48)        address of v4 source
00003C5C  00000010                                 2552+          DC    A(16)             result length
00003C60  00003CBC                                 2553+REA59     DC    A(RE59)           result address
00003C68  00000000 00000000                        2554+          DS    FD                gap
00003C70  00000000 00000000                        2555+V1O59     DS    XL16              V1 output
00003C78  00000000 00000000
00003C80  00000000 00000000                        2556+          DS    FD                gap
                                                   2557+*
00003C88                                           2558+X59       DS    0F
00003C88  E310 5010 0014                 00000010  2559+          LGF   R1,V2ADDR         load v2 source
00003C8E  E761 0000 0806                 00000000  2560+          VL    v22,0(R1)         use v22 to test decoder
00003C94  E310 5014 0014                 00000014  2561+          LGF   R1,V3ADDR         load v3 source
00003C9A  E771 0000 0806                 00000000  2562+          VL    v23,0(R1)         use v23 to test decoder
00003CA0  E310 5018 0014                 00000018  2563+          LGF   R1,V4ADDR         load v4 source
00003CA6  E781 0000 0806                 00000000  2564+          VL    v24,0(R1)         use v24 to test decoder
00003CAC  E766 7200 8FAC                           2565+          VMALE V22,V22,V23,V24,2    test instruction (dest is a source)
00003CB2  E760 5030 080E                 00003C70  2566+          VST   V22,V1O59          save v1 output
00003CB8  07FB                                     2567+          BR    R11               return
00003CBC                                           2568+RE59      DC    0F                xl16 expected result
00003CBC                                           2569+          DROP  R5
00003CBC  FD060408 04111110                        2570           DC    XL16'FD06040804111110 092E6097DCBD8D58'   result
00003CC4  092E6097 DCBD8D58
00003CCC  FF020304 05060708                        2571           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00003CD4  090A0B0C 0D0E0F10
00003CDC  FF010102 02030304                        2572           DC    XL16'FF01010202030304 0405050606070708'   v3
00003CE4  04050506 06070708
00003CEC  FF020304 05060708                        2573           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00003CF4  090A0B0C 0D0E0F10
                                                   2574
                                                   2575           VRR_D VMALE,2
00003D00                                           2576+          DS    0FD
00003D00                      00003D00             2577+          USING *,R5              base for test data and test routine
00003D00  00003D48                                 2578+T60       DC    A(X60)            address of test routine
00003D04  003C                                     2579+          DC    H'60'             test number
00003D06  00                                       2580+          DC    X'00'
00003D07  02                                       2581+          DC    HL1'2'            m5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003D08  E5D4C1D3 C5404040                        2582+         DC    CL8'VMALE'         instruction name
00003D10  00003D8C                                 2583+         DC    A(RE60+16)         address of v2 source
00003D14  00003D9C                                 2584+         DC    A(RE60+32)         address of v3 source
00003D18  00003DAC                                 2585+         DC    A(RE60+48)         address of v4 source
00003D1C  00000010                                 2586+         DC    A(16)              result length
00003D20  00003D7C                                 2587+REA60    DC    A(RE60)            result address
00003D28  00000000 00000000                        2588+         DS    FD                 gap
00003D30  00000000 00000000                        2589+V1O60    DS    XL16               V1 output
00003D38  00000000 00000000
00003D40  00000000 00000000                        2590+         DS    FD                 gap
                                                   2591+*
00003D48                                           2592+X60      DS    0F
00003D48  E310 5010 0014                 00000010  2593+         LGF   R1,V2ADDR          load v2 source
00003D4E  E761 0000 0806                 00000000  2594+         VL    v22,0(R1)          use v22 to test decoder
00003D54  E310 5014 0014                 00000014  2595+         LGF   R1,V3ADDR          load v3 source
00003D5A  E771 0000 0806                 00000000  2596+         VL    v23,0(R1)          use v23 to test decoder
00003D60  E310 5018 0014                 00000018  2597+         LGF   R1,V4ADDR          load v4 source
00003D66  E781 0000 0806                 00000000  2598+         VL    v24,0(R1)          use v24 to test decoder
00003D6C  E766 7200 8FAC                           2599+         VMALE V22,V22,V23,V24,2    test instruction (dest is a source)
00003D72  E760 5030 080E                 00003D30  2600+         VST   V22,V1O60           save v1 output
00003D78  07FB                                     2601+         BR    R11                return
00003D7C                                           2602+RE60     DC    0F                 xl16 expected result
00003D7C                                           2603+         DROP  R5
00003D7C  FD050405 01060708                        2604          DC    XL16'FD05040501060708 09131E2A372F261C'   result
00003D84  09131E2A 372F261C
00003D8C  FF020304 05060708                        2605          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00003D94  090A0B0C 0D0E0F10
00003D9C  FF000000 00000001                        2606          DC    XL16'FF00000000000001 0101010101010102'   v3
00003DA4  01010101 01010102
00003DAC  FF020304 05060708                        2607          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00003DB4  090A0B0C 0D0E0F10
                                                   2608
                                                   2609 *-------------------------------------------------------------------
                                                   2610 *  VMALO  - Vector Multiply and Add Logical Odd
                                                   2611 *-------------------------------------------------------------------
                                                   2612 * Byte
                                                   2613          VRR_D VMALO,0
00003DC0                                           2614+         DS    0FD
00003DC0                         00003DC0          2615+         USING *,R5               base for test data and test routine
00003DC0  00003E08                                 2616+T61      DC    A(X61)             address of test routine
00003DC4  003D                                     2617+         DC    H'61'              test number
00003DC6  00                                       2618+         DC    X'00'
00003DC7  00                                       2619+         DC    HL1'0'             m5
00003DC8  E5D4C1D3 D6404040                        2620+         DC    CL8'VMALO'         instruction name
00003DD0  00003E4C                                 2621+         DC    A(RE61+16)         address of v2 source
00003DD4  00003E5C                                 2622+         DC    A(RE61+32)         address of v3 source
00003DD8  00003E6C                                 2623+         DC    A(RE61+48)         address of v4 source
00003DDC  00000010                                 2624+         DC    A(16)              result length
00003DE0  00003E3C                                 2625+REA61    DC    A(RE61)            result address
00003DE8  00000000 00000000                        2626+         DS    FD                 gap
00003DF0  00000000 00000000                        2627+V1O61    DS    XL16               V1 output
00003DF8  00000000 00000000
00003E00  00000000 00000000                        2628+         DS    FD                 gap
                                                   2629+*
00003E08                                           2630+X61      DS    0F
00003E08  E310 5010 0014                 00000010  2631+         LGF   R1,V2ADDR          load v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003E0E  E761 0000 0806                 00000000  2632+         VL    v22,0(R1)          use v22 to test decoder
00003E14  E310 5014 0014                 00000014  2633+         LGF   R1,V3ADDR         load v3 source
00003E1A  E771 0000 0806                 00000000  2634+         VL    v23,0(R1)          use v23 to test decoder
00003E20  E310 5018 0014                 00000018  2635+         LGF   R1,V4ADDR         load v4 source
00003E26  E781 0000 0806                 00000000  2636+         VL    v24,0(R1)          use v24 to test decoder
00003E2C  E766 7000 8FAD                           2637+         VMALO V22,V22,V23,V24,0    test instruction (dest is a source)
00003E32  E760 5030 080E                 00003DF0  2638+         VST   V22,V1O61           save v1 output
00003E38  07FB                                     2639+         BR    R11                return
00003E3C                                           2640+RE61     DC    0F                 xl16 expected result
00003E3C                                           2641+         DROP  R5
00003E3C  00000000 00000271                        2642          DC    XL16'0000000000000271 00000C400000F424'   result
00003E44  00000C40 0000F424
00003E4C  FF000000 00000019                        2643          DC    XL16'FF00000000000019 00000038000000FA'   v2
00003E54  00000038 000000FA
00003E5C  FF000000 00000019                        2644          DC    XL16'FF00000000000019 00000038000000FA'   v3
00003E64  00000038 000000FA
00003E6C  00000000 00000000                        2645          DC    XL16'0000000000000000 0000000000000000'   v4
00003E74  00000000 00000000
                                                   2646
                                                   2647          VRR_D VMALO,0
00003E80                                           2648+         DS    0FD
00003E80                           00003E80        2649+         USING *,R5               base for test data and test routine
00003E80  00003EC8                                 2650+T62      DC    A(X62)             address of test routine
00003E84  003E                                     2651+         DC    H'62'              test number
00003E86  00                                       2652+         DC    X'00'
00003E87  00                                       2653+         DC    HL1'0'             m5
00003E88  E5D4C1D3 D6404040                        2654+         DC    CL8'VMALO'         instruction name
00003E90  00003F0C                                 2655+         DC    A(RE62+16)         address of v2 source
00003E94  00003F1C                                 2656+         DC    A(RE62+32)         address of v3 source
00003E98  00003F2C                                 2657+         DC    A(RE62+48)         address of v4 source
00003E9C  00000010                                 2658+         DC    A(16)              result length
00003EA0  00003EFC                                 2659+REA62    DC    A(RE62)            result address
00003EA8  00000000 00000000                        2660+         DS    FD                 gap
00003EB0  00000000 00000000                        2661+V1O62    DS    XL16               V1 output
00003EB8  00000000 00000000
00003EC0  00000000 00000000                        2662+         DS    FD                 gap
                                                   2663+*
00003EC8                                           2664+X62      DS    0F
00003EC8  E310 5010 0014                 00000010  2665+         LGF   R1,V2ADDR          load v2 source
00003ECE  E761 0000 0806                 00000000  2666+         VL    v22,0(R1)          use v22 to test decoder
00003ED4  E310 5014 0014                 00000014  2667+         LGF   R1,V3ADDR          load v3 source
00003EDA  E771 0000 0806                 00000000  2668+         VL    v23,0(R1)          use v23 to test decoder
00003EE0  E310 5018 0014                 00000018  2669+         LGF   R1,V4ADDR          load v4 source
00003EE6  E781 0000 0806                 00000000  2670+         VL    v24,0(R1)          use v24 to test decoder
00003EEC  E766 7000 8FAD                           2671+         VMALO V22,V22,V23,V24,0    test instruction (dest is a source)
00003EF2  E760 5030 080E                 00003EB0  2672+         VST   V22,V1O62           save v1 output
00003EF8  07FB                                     2673+         BR    R11                return
00003EFC                                           2674+RE62     DC    0F                 xl16 expected result
00003EFC                                           2675+         DROP  R5
00003EFC  00020100 000006C0                        2676          DC    XL16'00020100000006C0 00000C430000F426'   result
00003F04  00000C43 0000F426
00003F0C  FF0000FF 00000029                        2677          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00003F14  00000038 000000FA
00003F1C  FF000001 00000029                        2678          DC    XL16'FF00000100000029 00000038000000FA'   v3
00003F24  00000038 000000FA
00003F2C  00020001 0000002F                        2679          DC    XL16'00020001000002F 0000000300000002'   v4
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00003F34  00000003 00000002                        2680
                                                   2681          VRR_D VMALO,0
00003F40                                           2682+         DS    0FD
00003F40                          00003F40         2683+         USING *,R5              base for test data and test routine
00003F40  00003F88                                 2684+T63      DC    A(X63)            address of test routine
00003F44  003F                                     2685+         DC    H'63'             test number
00003F46  00                                       2686+         DC    X'00'
00003F47  00                                       2687+         DC    HL1'0'            m5
00003F48  E5D4C1D3 D6404040                        2688+         DC    CL8'VMALO'        instruction name
00003F50  00003FCC                                 2689+         DC    A(RE63+16)        address of v2 source
00003F54  00003FDC                                 2690+         DC    A(RE63+32)        address of v3 source
00003F58  00003FEC                                 2691+         DC    A(RE63+48)        address of v4 source
00003F5C  00000010                                 2692+         DC    A(16)             result length
00003F60  00003FBC                                 2693+REA63    DC    A(RE63)           result address
00003F68  00000000 00000000                        2694+         DS    FD                gap
00003F70  00000000 00000000                        2695+V1O63    DS    XL16              V1 output
00003F78  00000000 00000000
00003F80  00000000 00000000                        2696+         DS    FD                gap
                                                   2697+*
00003F88                                           2698+X63      DS    0F
00003F88  E310 5010 0014                00000010   2699+         LGF   R1,V2ADDR         load v2 source
00003F8E  E761 0000 0806                00000000   2700+         VL    v22,0(R1)         use v22 to test decoder
00003F94  E310 5014 0014                00000014   2701+         LGF   R1,V3ADDR         load v3 source
00003F9A  E771 0000 0806                00000000   2702+         VL    v23,0(R1)         use v23 to test decoder
00003FA0  E310 5018 0014                00000018   2703+         LGF   R1,V4ADDR         load v4 source
00003FA6  E781 0000 0806                00000000   2704+         VL    v24,0(R1)         use v24 to test decoder
00003FAC  E766 7000 8FAD                           2705+         VMALO V22,V22,V23,V24,0    test instruction (dest is a source)
00003FB2  E760 5030 080E                00003F70   2706+         VST   V22,V1O63          save v1 output
00003FB8  07FB                                     2707+         BR    R11               return
00003FBC                                           2708+RE63     DC    0F                xl16 expected result
00003FBC                                           2709+         DROP  R5
00003FBC  FF060314 052A0748                        2710          DC    XL16'FF060314052A0748 096E0B9C0DD21010'   result
00003FC4  096E0B9C 0DD21010
00003FCC  FF020304 05060708                        2711          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00003FD4  090A0B0C 0D0E0F10
00003FDC  FF020304 05060708                        2712          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00003FE4  090A0B0C 0D0E0F10
00003FEC  FF020304 05060708                        2713          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00003FF4  090A0B0C 0D0E0F10
                                                   2714
                                                   2715          VRR_D VMALO,0
00004000                                           2716+         DS    0FD
00004000                          00004000         2717+         USING *,R5              base for test data and test routine
00004000  00004048                                 2718+T64      DC    A(X64)            address of test routine
00004004  0040                                     2719+         DC    H'64'             test number
00004006  00                                       2720+         DC    X'00'
00004007  00                                       2721+         DC    HL1'0'            m5
00004008  E5D4C1D3 D6404040                        2722+         DC    CL8'VMALO'        instruction name
00004010  0000408C                                 2723+         DC    A(RE64+16)        address of v2 source
00004014  0000409C                                 2724+         DC    A(RE64+32)        address of v3 source
00004018  000040AC                                 2725+         DC    A(RE64+48)        address of v4 source
0000401C  00000010                                 2726+         DC    A(16)             result length
00004020  0000407C                                 2727+REA64    DC    A(RE64)           result address
00004028  00000000 00000000                        2728+         DS    FD                gap
00004030  00000000 00000000                        2729+V1O64    DS    XL16              V1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004038  00000000 00000000
00004040  00000000 00000000                        2730+          DS    FD                gap
                                                   2731+*
00004048                                           2732+X64       DS    0F
00004048  E310 5010 0014                 00000010  2733+          LGF   R1,V2ADDR          load v2 source
0000404E  E761 0000 0806                 00000000  2734+          VL    v22,0(R1)         use v22 to test decoder
00004054  E310 5014 0014                 00000014  2735+          LGF   R1,V3ADDR          load v3 source
0000405A  E771 0000 0806                 00000000  2736+          VL    v23,0(R1)         use v23 to test decoder
00004060  E310 5018 0014                 00000018  2737+          LGF   R1,V4ADDR          load v4 source
00004066  E781 0000 0806                 00000000  2738+          VL    v24,0(R1)         use v24 to test decoder
0000406C  E766 7000 8FAD                           2739+          VMALO V22,V22,V23,V24,0    test instruction (dest is a source)
00004072  E760 5030 080E                 00004030  2740+          VST   V22,V1O64          save v1 output
00004078  07FB                                     2741+          BR    R11               return
0000407C                                           2742+RE64      DC    0F                xl16 expected result
0000407C                                           2743+          DROP  R5
0000407C  FF04030C 05180728                        2744           DC    XL16'FF04030C05180728 093C0B540D700F90'   result
00004084  093C0B54 0D700F90
0000408C  FF020304 05060708                        2745           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004094  090A0B0C 0D0E0F10
0000409C  FF010102 02030304                        2746           DC    XL16'FF01010202030304 0405050606070708'   v3
000040A4  04050506 06070708
000040AC  FF020304 05060708                        2747           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000040B4  090A0B0C 0D0E0F10
                                                   2748
                                                   2749           VRR_D VMALO,0
000040C0                                           2750+          DS    0FD
000040C0                  000040C0                 2751+          USING *,R5              base for test data and test routine
000040C0  00004108                                 2752+T65       DC    A(X65)            address of test routine
000040C4  0041                                     2753+          DC    H'65'             test number
000040C6  00                                       2754+          DC    X'00'
000040C7  00                                       2755+          DC    HL1'0'            m5
000040C8  E5D4C1D3 D6404040                        2756+          DC    CL8'VMALO'        instruction name
000040D0  0000414C                                 2757+          DC    A(RE65+16)        address of v2 source
000040D4  0000415C                                 2758+          DC    A(RE65+32)        address of v3 source
000040D8  0000416C                                 2759+          DC    A(RE65+48)        address of v4 source
000040DC  00000010                                 2760+          DC    A(16)             result length
000040E0  0000413C                                 2761+REA65     DC    A(RE65)           result address
000040E8  00000000 00000000                        2762+          DS    FD                gap
000040F0  00000000 00000000                        2763+V1O65     DS    XL16              V1 output
000040F8  00000000 00000000
00004100  00000000 00000000                        2764+          DS    FD                gap
                                                   2765+*
00004108                                           2766+X65       DS    0F
00004108  E310 5010 0014                 00000010  2767+          LGF   R1,V2ADDR          load v2 source
0000410E  E761 0000 0806                 00000000  2768+          VL    v22,0(R1)         use v22 to test decoder
00004114  E310 5014 0014                 00000014  2769+          LGF   R1,V3ADDR          load v3 source
0000411A  E771 0000 0806                 00000000  2770+          VL    v23,0(R1)         use v23 to test decoder
00004120  E310 5018 0014                 00000018  2771+          LGF   R1,V4ADDR          load v4 source
00004126  E781 0000 0806                 00000000  2772+          VL    v24,0(R1)         use v24 to test decoder
0000412C  E766 7000 8FAD                           2773+          VMALO V22,V22,V23,V24,0    test instruction (dest is a source)
00004132  E760 5030 080E                 000040F0  2774+          VST   V22,V1O65          save v1 output
00004138  07FB                                     2775+          BR    R11               return
0000413C                                           2776+RE65      DC    0F                xl16 expected result
0000413C                                           2777+          DROP  R5
0000413C  FF020304 05060710                        2778           DC    XL16'FF02030405060710 09140B180D1C0F30'   result
00004144  09140B18 0D1C0F30
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
0000414C  FF020304 05060708                        2779          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004154  090A0B0C 0D0E0F10
0000415C  FF000000 00000001                        2780          DC    XL16'FF00000000000001 0101010101010102'   v3
00004164  01010101 01010102
0000416C  FF020304 05060708                        2781          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004174  090A0B0C 0D0E0F10
                                                   2782
                                                   2783 * Halfword
                                                   2784          VRR_D VMALO,1
00004180                                           2785+         DS    0FD
00004180                          00004180         2786+         USING *,R5              base for test data and test routine
00004180  000041C8                                 2787+T66      DC    A(X66)            address of test routine
00004184  0042                                     2788+         DC    H'66'             test number
00004186  00                                       2789+         DC    X'00'
00004187  01                                       2790+         DC    HL1'1'            m5
00004188  E5D4C1D3 D6404040                        2791+         DC    CL8'VMALO'        instruction name
00004190  0000420C                                 2792+         DC    A(RE66+16)        address of v2 source
00004194  0000421C                                 2793+         DC    A(RE66+32)        address of v3 source
00004198  0000422C                                 2794+         DC    A(RE66+48)        address of v4 source
0000419C  00000010                                 2795+         DC    A(16)             result length
000041A0  000041FC                                 2796+REA66    DC    A(RE66)           result address
000041A8  00000000 00000000                        2797+         DS    FD                gap
000041B0  00000000 00000000                        2798+V1O66    DS    XL16              V1 output
000041B8  00000000 00000000
000041C0  00000000 00000000                        2799+         DS    FD                gap
                                                   2800+*
000041C8                                           2801+X66      DS    0F
000041C8  E310 5010 0014                 00000010  2802+         LGF   R1,V2ADDR         load v2 source
000041CE  E761 0000 0806                 00000000  2803+         VL    v22,0(R1)         use v22 to test decoder
000041D4  E310 5014 0014                 00000014  2804+         LGF   R1,V3ADDR         load v3 source
000041DA  E771 0000 0806                 00000000  2805+         VL    v23,0(R1)         use v23 to test decoder
000041E0  E310 5018 0014                 00000018  2806+         LGF   R1,V4ADDR         load v4 source
000041E6  E781 0000 0806                 00000000  2807+         VL    v24,0(R1)         use v24 to test decoder
000041EC  E766 7100 8FAD                           2808+         VMALO V22,V22,V23,V24,1    test instruction (dest is a source)
000041F2  E760 5030 080E                 000041B0  2809+         VST   V22,V1O66          save v1 output
000041F8  07FB                                     2810+         BR    R11               return
000041FC                                           2811+RE66     DC    0F                xl16 expected result
000041FC                                           2812+         DROP  R5
000041FC  00000000 00000271                        2813          DC    XL16'0000000000000271 00000C400000F424'   result
00004204  00000C40 0000F424
0000420C  FF000000 00000019                        2814          DC    XL16'FF00000000000019 00000038000000FA'   v2
00004214  00000038 000000FA
0000421C  FF000000 00000019                        2815          DC    XL16'FF00000000000019 00000038000000FA'   v3
00004224  00000038 000000FA
0000422C  00000000 00000000                        2816          DC    XL16'0000000000000000 0000000000000000'   v4
00004234  00000000 00000000
                                                   2817
                                                   2818          VRR_D VMALO,1
00004240                                           2819+         DS    0FD
00004240                          00004240         2820+         USING *,R5              base for test data and test routine
00004240  00004288                                 2821+T67      DC    A(X67)            address of test routine
00004244  0043                                     2822+         DC    H'67'             test number
00004246  00                                       2823+         DC    X'00'
00004247  01                                       2824+         DC    HL1'1'            m5
00004248  E5D4C1D3 D6404040                        2825+         DC    CL8'VMALO'        instruction name
00004250  000042CC                                 2826+         DC    A(RE67+16)        address of v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004254  000042DC                          2827+          DC    A(RE67+32)          address of v3 source
00004258  000042EC                          2828+          DC    A(RE67+48)          address of v4 source
0000425C  00000010                          2829+          DC    A(16)               result length
00004260  000042BC                          2830+REA67     DC    A(RE67)             result address
00004268  00000000 00000000                 2831+          DS    FD                  gap
00004270  00000000 00000000                 2832+V1O67     DS    XL16                V1 output
00004278  00000000 00000000
00004280  00000000 00000000                 2833+          DS    FD                  gap
                                            2834+*
00004288                                    2835+X67       DS    0F
00004288  E310 5010 0014              00000010  2836+          LGF   R1,V2ADDR           load v2 source
0000428E  E761 0000 0806              00000000  2837+          VL    v22,0(R1)           use v22 to test decoder
00004294  E310 5014 0014              00000014  2838+          LGF   R1,V3ADDR           load v3 source
0000429A  E771 0000 0806              00000000  2839+          VL    v23,0(R1)           use v23 to test decoder
000042A0  E310 5018 0014              00000018  2840+          LGF   R1,V4ADDR           load v4 source
000042A6  E781 0000 0806              00000000  2841+          VL    v24,0(R1)           use v24 to test decoder
000042AC  E766 7100 8FAD                        2842+          VMALO V22,V22,V23,V24,1    test instruction (dest is a source)
000042B2  E760 5030 080E              00004270  2843+          VST   V22,V1O67            save v1 output
000042B8  07FB                                  2844+          BR    R11                 return
000042BC                                    2845+RE67      DC    0F                  xl16 expected result
000042BC                                    2846+          DROP  R5
000042BC  00020100 000006C0                 2847           DC    XL16'00020100000006C0 00000C430000F426'   result
000042C4  00000C43 0000F426
000042CC  FF0000FF 00000029                 2848           DC    XL16'FF0000FF00000029 00000038000000FA'   v2
000042D4  00000038 000000FA
000042DC  FF000001 00000029                 2849           DC    XL16'FF00000100000029 00000038000000FA'   v3
000042E4  00000038 000000FA
000042EC  00020001 0000002F                 2850           DC    XL16'00020010000002F 0000000300000002'   v4
000042F4  00000003 00000002
                                            2851
                                            2852           VRR_D VMALO,1
00004300                                    2853+          DS    0FD
00004300                    00004300        2854+          USING *,R5                base for test data and test routine
00004300  00004348                          2855+T68       DC    A(X68)              address of test routine
00004304  0044                              2856+          DC    H'68'               test number
00004306  00                                2857+          DC    X'00'
00004307  01                                2858+          DC    HL1'1'              m5
00004308  E5D4C1D3 D6404040                 2859+          DC    CL8'VMALO'          instruction name
00004310  0000438C                          2860+          DC    A(RE68+16)          address of v2 source
00004314  0000439C                          2861+          DC    A(RE68+32)          address of v3 source
00004318  000043AC                          2862+          DC    A(RE68+48)          address of v4 source
0000431C  00000010                          2863+          DC    A(16)               result length
00004320  0000437C                          2864+REA68     DC    A(RE68)             result address
00004328  00000000 00000000                 2865+          DS    FD                  gap
00004330  00000000 00000000                 2866+V1O68     DS    XL16                V1 output
00004338  00000000 00000000
00004340  00000000 00000000                 2867+          DS    FD                  gap
                                            2868+*
00004348                                    2869+X68       DS    0F
00004348  E310 5010 0014              00000010  2870+          LGF   R1,V2ADDR           load v2 source
0000434E  E761 0000 0806              00000000  2871+          VL    v22,0(R1)           use v22 to test decoder
00004354  E310 5014 0014              00000014  2872+          LGF   R1,V3ADDR           load v3 source
0000435A  E771 0000 0806              00000000  2873+          VL    v23,0(R1)           use v23 to test decoder
00004360  E310 5018 0014              00000018  2874+          LGF   R1,V4ADDR           load v4 source
00004366  E781 0000 0806              00000000  2875+          VL    v24,0(R1)           use v24 to test decoder
0000436C  E766 7100 8FAD                        2876+          VMALO V22,V22,V23,V24,1    test instruction (dest is a source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004372  E760 5030 080E                 00004330  2877+          VST   V22,V1O68          save v1 output
00004378  07FB                                      2878+          BR    R11               return
0000437C                                            2879+RE68      DC    0F                xl16 expected result
0000437C                                            2880+          DROP  R5
0000437C  FF0B1B14 05377748                         2881           DC    XL16'FF0B1B1405377748 0984139C0DF0F010'   result
00004384  0984139C 0DF0F010
0000438C  FF020304 05060708                         2882           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004394  090A0B0C 0D0E0F10
0000439C  FF020304 05060708                         2883           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
000043A4  090A0B0C 0D0E0F10
000043AC  FF020304 05060708                         2884           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000043B4  090A0B0C 0D0E0F10
                                                    2885
                                                    2886           VRR_D VMALO,1
000043C0                                            2887+          DS    0FD
000043C0                    000043C0                2888+          USING *,R5              base for test data and test routine
000043C0  00004408                                  2889+T69       DC    A(X69)            address of test routine
000043C4  0045                                      2890+          DC    H'69'             test number
000043C6  00                                        2891+          DC    X'00'
000043C7  01                                        2892+          DC    HL1'1'            m5
000043C8  E5D4C1D3 D6404040                         2893+          DC    CL8'VMALO'        instruction name
000043D0  0000444C                                  2894+          DC    A(RE69+16)        address of v2 source
000043D4  0000445C                                  2895+          DC    A(RE69+32)        address of v3 source
000043D8  0000446C                                  2896+          DC    A(RE69+48)        address of v4 source
000043DC  00000010                                  2897+          DC    A(16)             result length
000043E0  0000443C                                  2898+REA69     DC    A(RE69)           result address
000043E8  00000000 00000000                         2899+          DS    FD                gap
000043F0  00000000 00000000                         2900+V1O69     DS    XL16              V1 output
000043F8  00000000 00000000
00004400  00000000 00000000                         2901+          DS    FD                gap
                                                    2902+*
00004408                                            2903+X69       DS    0F
00004408  E310 5010 0014                 00000010   2904+          LGF   R1,V2ADDR         load v2 source
0000440E  E761 0000 0806                 00000000   2905+          VL    v22,0(R1)         use v22 to test decoder
00004414  E310 5014 0014                 00000014   2906+          LGF   R1,V3ADDR         load v3 source
0000441A  E771 0000 0806                 00000000   2907+          VL    v23,0(R1)         use v23 to test decoder
00004420  E310 5018 0014                 00000018   2908+          LGF   R1,V4ADDR         load v4 source
00004426  E781 0000 0806                 00000000   2909+          VL    v24,0(R1)         use v24 to test decoder
0000442C  E766 7100 8FAD                            2910+          VMALO V22,V22,V23,V24,1    test instruction (dest is a source)
00004432  E760 5030 080E                 000043F0   2911+          VST   V22,V1O69          save v1 output
00004438  07FB                                      2912+          BR    R11               return
0000443C                                            2913+RE69      DC    0F                xl16 expected result
0000443C                                            2914+          DROP  R5
0000443C  FF050D0C 051B3B28                         2915           DC    XL16'FF050D0C051B3B28 094189540D77F790'   result
00004444  09418954 0D77F790
0000444C  FF020304 05060708                         2916           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004454  090A0B0C 0D0E0F10
0000445C  FF010102 02030304                         2917           DC    XL16'FF01010202030304 0405050606070708'   v3
00004464  04050506 06070708
0000446C  FF020304 05060708                         2918           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004474  090A0B0C 0D0E0F10
                                                    2919
                                                    2920           VRR_D VMALO,1
00004480                                            2921+          DS    0FD
00004480                    00004480                2922+          USING *,R5              base for test data and test routine
00004480  000044C8                                  2923+T70       DC    A(X70)            address of test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004484  0046                                    2924+          DC    H'70'              test number
00004486  00                                      2925+          DC    X'00'
00004487  01                                      2926+          DC    HL1'1'             m5
00004488  E5D4C1D3 D6404040                       2927+          DC    CL8'VMALO'         instruction name
00004490  0000450C                                2928+          DC    A(RE70+16)         address of v2 source
00004494  0000451C                                2929+          DC    A(RE70+32)         address of v3 source
00004498  0000452C                                2930+          DC    A(RE70+48)         address of v4 source
0000449C  00000010                                2931+          DC    A(16)              result length
000044A0  000044FC                                2932+REA70     DC    A(RE70)            result address
000044A8  00000000 00000000                       2933+          DS    FD                 gap
000044B0  00000000 00000000                       2934+V1O70     DS    XL16               V1 output
000044B8  00000000 00000000
000044C0  00000000 00000000                       2935+          DS    FD                 gap
                                                  2936+*
000044C8                                          2937+X70       DS    0F
000044C8  E310 5010 0014                 00000010 2938+          LGF   R1,V2ADDR          load v2 source
000044CE  E761 0000 0806                 00000000 2939+          VL    v22,0(R1)          use v22 to test decoder
000044D4  E310 5014 0014                 00000014 2940+          LGF   R1,V3ADDR          load v3 source
000044DA  E771 0000 0806                 00000000 2941+          VL    v23,0(R1)          use v23 to test decoder
000044E0  E310 5018 0014                 00000018 2942+          LGF   R1,V4ADDR          load v4 source
000044E6  E781 0000 0806                 00000000 2943+          VL    v24,0(R1)          use v24 to test decoder
000044EC  E766 7100 8FAD                          2944+          VMALO V22,V22,V23,V24,1    test instruction (dest is a source)
000044F2  E760 5030 080E                 000044B0 2945+          VST   V22,V1O70           save v1 output
000044F8  07FB                                    2946+          BR    R11                return
000044FC                                          2947+RE70      DC    0F                 xl16 expected result
000044FC                                          2948+          DROP  R5
000044FC  FF020304 05060E10                       2949           DC    XL16'FF02030405060E10 091522180D1D3D30'   result
00004504  09152218 0D1D3D30
0000450C  FF020304 05060708                       2950           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004514  090A0B0C 0D0E0F10
0000451C  FF000000 00000001                       2951           DC    XL16'FF00000000000001 0101010101010102'   v3
00004524  01010101 01010102
0000452C  FF020304 05060708                       2952           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004534  090A0B0C 0D0E0F10
                                                  2953
                                                  2954 * Word
                                                  2955           VRR_D VMALO,2
00004540                                          2956+          DS    0FD
00004540                         00004540         2957+          USING *,R5               base for test data and test routine
00004540  00004588                                2958+T71       DC    A(X71)             address of test routine
00004544  0047                                    2959+          DC    H'71'              test number
00004546  00                                      2960+          DC    X'00'
00004547  02                                      2961+          DC    HL1'2'             m5
00004548  E5D4C1D3 D6404040                       2962+          DC    CL8'VMALO'         instruction name
00004550  000045CC                                2963+          DC    A(RE71+16)         address of v2 source
00004554  000045DC                                2964+          DC    A(RE71+32)         address of v3 source
00004558  000045EC                                2965+          DC    A(RE71+48)         address of v4 source
0000455C  00000010                                2966+          DC    A(16)              result length
00004560  000045BC                                2967+REA71     DC    A(RE71)            result address
00004568  00000000 00000000                       2968+          DS    FD                 gap
00004570  00000000 00000000                       2969+V1O71     DS    XL16               V1 output
00004578  00000000 00000000
00004580  00000000 00000000                       2970+          DS    FD                 gap
                                                  2971+*
00004588                                          2972+X71       DS    0F
00004588  E310 5010 0014                 00000010 2973+          LGF   R1,V2ADDR          load v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000458E  E761 0000 0806                 00000000  2974+         VL    v22,0(R1)          use v22 to test decoder
00004594  E310 5014 0014                 00000014  2975+         LGF   R1,V3ADDR          load v3 source
0000459A  E771 0000 0806                 00000000  2976+         VL    v23,0(R1)          use v23 to test decoder
000045A0  E310 5018 0014                 00000018  2977+         LGF   R1,V4ADDR          load v4 source
000045A6  E781 0000 0806                 00000000  2978+         VL    v24,0(R1)          use v24 to test decoder
000045AC  E766 7200 8FAD                           2979+         VMALO V22,V22,V23,V24,2    test instruction (dest is a source)
000045B2  E760 5030 080E                 00004570  2980+         VST   V22,V1O71           save v1 output
000045B8  07FB                                     2981+         BR    R11                return
000045BC                                           2982+RE71     DC    0F                 xl16 expected result
000045BC                                           2983+         DROP  R5
000045BC  00000000 00000271                        2984          DC    XL16'0000000000000271 000000000000F424'   result
000045C4  00000000 0000F424
000045CC  FF000000 00000019                        2985          DC    XL16'FF00000000000019 00000038000000FA'   v2
000045D4  00000038 000000FA
000045DC  FF000000 00000019                        2986          DC    XL16'FF00000000000019 00000038000000FA'   v3
000045E4  00000038 000000FA
000045EC  00000000 00000000                        2987          DC    XL16'0000000000000000 0000000000000000'   v4
000045F4  00000000 00000000
                                                   2988
                                                   2989          VRR_D VMALO,2
00004600                                           2990+         DS    0FD
00004600                   00004600                2991+         USING *,R5               base for test data and test routine
00004600  00004648                                 2992+T72      DC    A(X72)             address of test routine
00004604  0048                                     2993+         DC    H'72'              test number
00004606  00                                       2994+         DC    X'00'
00004607  02                                       2995+         DC    HL1'2'             m5
00004608  E5D4C1D3 D6404040                       2996+         DC    CL8'VMALO'         instruction name
00004610  0000468C                                 2997+         DC    A(RE72+16)         address of v2 source
00004614  0000469C                                 2998+         DC    A(RE72+32)         address of v3 source
00004618  000046AC                                 2999+         DC    A(RE72+48)         address of v4 source
0000461C  00000010                                 3000+         DC    A(16)              result length
00004620  0000467C                                 3001+REA72    DC    A(RE72)            result address
00004628  00000000 00000000                        3002+         DS    FD                 gap
00004630  00000000 00000000                        3003+V1O72    DS    XL16               V1 output
00004638  00000000 00000000
00004640  00000000 00000000                        3004+         DS    FD                 gap
                                                   3005+*
00004648                                           3006+X72      DS    0F
00004648  E310 5010 0014                 00000010  3007+         LGF   R1,V2ADDR          load v2 source
0000464E  E761 0000 0806                 00000000  3008+         VL    v22,0(R1)          use v22 to test decoder
00004654  E310 5014 0014                 00000014  3009+         LGF   R1,V3ADDR          load v3 source
0000465A  E771 0000 0806                 00000000  3010+         VL    v23,0(R1)          use v23 to test decoder
00004660  E310 5018 0014                 00000018  3011+         LGF   R1,V4ADDR          load v4 source
00004666  E781 0000 0806                 00000000  3012+         VL    v24,0(R1)          use v24 to test decoder
0000466C  E766 7200 8FAD                           3013+         VMALO V22,V22,V23,V24,2    test instruction (dest is a source)
00004672  E760 5030 080E                 00004630  3014+         VST   V22,V1O72           save v1 output
00004678  07FB                                     3015+         BR    R11                return
0000467C                                           3016+RE72     DC    0F                 xl16 expected result
0000467C                                           3017+         DROP  R5
0000467C  00020001 000006C0                        3018          DC    XL16'00020001000006C0 000000030000F426'   result
00004684  00000003 0000F426
0000468C  FF0000FF 00000029                        3019          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00004694  00000038 000000FA
0000469C  FF000001 00000029                        3020          DC    XL16'FF00000100000029 00000038000000FA'   v3
000046A4  00000038 000000FA
000046AC  00020001 0000002F                        3021          DC    XL16'00020001000002F 0000000300000002'   v4
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000046B4  00000003 00000002                        3022
                                                   3023          VRR_D VMALO,2
000046C0                                           3024+         DS    0FD
000046C0                          000046C0         3025+         USING *,R5              base for test data and test routine
000046C0  00004708                                 3026+T73      DC    A(X73)            address of test routine
000046C4  0049                                     3027+         DC    H'73'             test number
000046C6  00                                       3028+         DC    X'00'
000046C7  02                                       3029+         DC    HL1'2'            m5
000046C8  E5D4C1D3 D6404040                        3030+         DC    CL8'VMALO'        instruction name
000046D0  0000474C                                 3031+         DC    A(RE73+16)        address of v2 source
000046D4  0000475C                                 3032+         DC    A(RE73+32)        address of v3 source
000046D8  0000476C                                 3033+         DC    A(RE73+48)        address of v4 source
000046DC  00000010                                 3034+         DC    A(16)             result length
000046E0  0000473C                                 3035+REA73    DC    A(RE73)           result address
000046E8  00000000 00000000                        3036+         DS    FD                gap
000046F0  00000000 00000000                        3037+V1O73    DS    XL16              V1 output
000046F8  00000000 00000000
00004700  00000000 00000000                        3038+         DS    FD                gap
                                                   3039+*
00004708                                           3040+X73      DS    0F
00004708  E310 5010 0014                 00000010  3041+         LGF   R1,V2ADDR         load v2 source
0000470E  E761 0000 0806                 00000000  3042+         VL    v22,0(R1)         use v22 to test decoder
00004714  E310 5014 0014                 00000014  3043+         LGF   R1,V3ADDR         load v3 source
0000471A  E771 0000 0806                 00000000  3044+         VL    v23,0(R1)         use v23 to test decoder
00004720  E310 5018 0014                 00000018  3045+         LGF   R1,V4ADDR         load v4 source
00004726  E781 0000 0806                 00000000  3046+         VL    v24,0(R1)         use v24 to test decoder
0000472C  E766 7200 8FAD                           3047+         VMALO V22,V22,V23,V24,2    test instruction (dest is a source)
00004732  E760 5030 080E                 000046F0  3048+         VST   V22,V1O73          save v1 output
00004738  07FB                                     3049+         BR    R11               return
0000473C                                           3050+RE73     DC    0F                xl16 expected result
0000473C                                           3051+         DROP  R5
0000473C  FF1B3F6E A9977748                        3052          DC    XL16'FF1B3F6EA9977748 09B4795953B0F010'   result
00004744  09B47959 53B0F010
0000474C  FF020304 05060708                        3053          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004754  090A0B0C 0D0E0F10
0000475C  FF020304 05060708                        3054          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00004764  090A0B0C 0D0E0F10
0000476C  FF020304 05060708                        3055          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004774  090A0B0C 0D0E0F10
                                                   3056
                                                   3057          VRR_D VMALO,2
00004780                                           3058+         DS    0FD
00004780                          00004780         3059+         USING *,R5              base for test data and test routine
00004780  000047C8                                 3060+T74      DC    A(X74)            address of test routine
00004784  004A                                     3061+         DC    H'74'             test number
00004786  00                                       3062+         DC    X'00'
00004787  02                                       3063+         DC    HL1'2'            m5
00004788  E5D4C1D3 D6404040                        3064+         DC    CL8'VMALO'        instruction name
00004790  0000480C                                 3065+         DC    A(RE74+16)        address of v2 source
00004794  0000481C                                 3066+         DC    A(RE74+32)        address of v3 source
00004798  0000482C                                 3067+         DC    A(RE74+48)        address of v4 source
0000479C  00000010                                 3068+         DC    A(16)             result length
000047A0  000047FC                                 3069+REA74    DC    A(RE74)           result address
000047A8  00000000 00000000                        3070+         DS    FD                gap
000047B0  00000000 00000000                        3071+V1O74    DS    XL16              V1 output
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000047B8  00000000 00000000
000047C0  00000000 00000000                        3072+         DS    FD                gap
                                                   3073+*
000047C8                                           3074+X74      DS    0F
000047C8  E310 5010 0014                 00000010  3075+          LGF   R1,V2ADDR         load v2 source
000047CE  E761 0000 0806                 00000000  3076+          VL    v22,0(R1)         use v22 to test decoder
000047D4  E310 5014 0014                 00000014  3077+          LGF   R1,V3ADDR         load v3 source
000047DA  E771 0000 0806                 00000000  3078+          VL    v23,0(R1)         use v23 to test decoder
000047E0  E310 5018 0014                 00000018  3079+          LGF   R1,V4ADDR         load v4 source
000047E6  E781 0000 0806                 00000000  3080+          VL    v24,0(R1)         use v24 to test decoder
000047EC  E766 7200 8FAD                           3081+          VMALO V22,V22,V23,V24,2    test instruction (dest is a source)
000047F2  E760 5030 080E                 000047B0  3082+          VST   V22,V1O74          save v1 output
000047F8  07FB                                     3083+          BR    R11               return
000047FC                                           3084+RE74      DC    0F                xl16 expected result
000047FC                                           3085+          DROP  R5
000047FC  FF0C1E33 504B3B28                        3086           DC    XL16'FF0C1E33504B3B28 0958BB24A157F790'   result
00004804  0958BB24 A157F790
0000480C  FF020304 05060708                        3087           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004814  090A0B0C 0D0E0F10
0000481C  FF010102 02030304                        3088           DC    XL16'FF01010202030304 0405050606070708'   v3
00004824  04050506 06070708
0000482C  FF020304 05060708                        3089           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004834  090A0B0C 0D0E0F10
                                                   3090
                                                   3091           VRR_D VMALO,2
00004840                                           3092+          DS    0FD
00004840                 00004840                  3093+          USING *,R5              base for test data and test routine
00004840  00004888                                 3094+T75       DC    A(X75)            address of test routine
00004844  004B                                     3095+          DC    H'75'             test number
00004846  00                                       3096+          DC    X'00'
00004847  02                                       3097+          DC    HL1'2'            m5
00004848  E5D4C1D3 D6404040                       3098+          DC    CL8'VMALO'        instruction name
00004850  000048CC                                 3099+          DC    A(RE75+16)        address of v2 source
00004854  000048DC                                 3100+          DC    A(RE75+32)        address of v3 source
00004858  000048EC                                 3101+          DC    A(RE75+48)        address of v4 source
0000485C  00000010                                 3102+          DC    A(16)             result length
00004860  000048BC                                 3103+REA75     DC    A(RE75)           result address
00004868  00000000 00000000                        3104+          DS    FD                gap
00004870  00000000 00000000                        3105+V1O75     DS    XL16              V1 output
00004878  00000000 00000000
00004880  00000000 00000000                        3106+          DS    FD                gap
                                                   3107+*
00004888                                           3108+X75       DS    0F
00004888  E310 5010 0014                 00000010  3109+          LGF   R1,V2ADDR         load v2 source
0000488E  E761 0000 0806                 00000000  3110+          VL    v22,0(R1)         use v22 to test decoder
00004894  E310 5014 0014                 00000014  3111+          LGF   R1,V3ADDR         load v3 source
0000489A  E771 0000 0806                 00000000  3112+          VL    v23,0(R1)         use v23 to test decoder
000048A0  E310 5018 0014                 00000018  3113+          LGF   R1,V4ADDR         load v4 source
000048A6  E781 0000 0806                 00000000  3114+          VL    v24,0(R1)         use v24 to test decoder
000048AC  E766 7200 8FAD                           3115+          VMALO V22,V22,V23,V24,2    test instruction (dest is a source)
000048B2  E760 5030 080E                 00004870  3116+          VST   V22,V1O75          save v1 output
000048B8  07FB                                     3117+          BR    R11               return
000048BC                                           3118+RE75      DC    0F                xl16 expected result
000048BC                                           3119+          DROP  R5
000048BC  FF020304 0A0C0E10                        3120           DC    XL16'FF0203040A0C0E10 0917263654493D30'   result
000048C4  09172636 54493D30
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000048CC  FF020304 05060708                      3121          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
000048D4  090A0B0C 0D0E0F10
000048DC  FF000000 00000001                      3122          DC    XL16'FF00000000000001 0101010101010102'   v3
000048E4  01010101 01010102
000048EC  FF020304 05060708                      3123          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000048F4  090A0B0C 0D0E0F10
                                                 3124
                                                 3125 *-------------------------------------------------------------------
                                                 3126 * VMAE   - Vector Multiply and Add Even
                                                 3127 *-------------------------------------------------------------------
                                                 3128 * Byte
                                                 3129          VRR_D VMAE,0
00004900                                         3130+         DS    0FD
00004900                          00004900       3131+         USING *,R5              base for test data and test routine
00004900  00004948                               3132+T76      DC    A(X76)            address of test routine
00004904  004C                                   3133+         DC    H'76'             test number
00004906  00                                     3134+         DC    X'00'
00004907  00                                     3135+         DC    HL1'0'            m5
00004908  E5D4C1C5 40404040                      3136+         DC    CL8'VMAE'         instruction name
00004910  0000498C                               3137+         DC    A(RE76+16)        address of v2 source
00004914  0000499C                               3138+         DC    A(RE76+32)        address of v3 source
00004918  000049AC                               3139+         DC    A(RE76+48)        address of v4 source
0000491C  00000010                               3140+         DC    A(16)             result length
00004920  0000497C                               3141+REA76    DC    A(RE76)           result address
00004928  00000000 00000000                      3142+         DS    FD                gap
00004930  00000000 00000000                      3143+V1O76    DS    XL16              V1 output
00004938  00000000 00000000
00004940  00000000 00000000                      3144+         DS    FD                gap
                                                 3145+*
00004948                                         3146+X76      DS    0F
00004948  E310 5010 0014                00000010 3147+         LGF   R1,V2ADDR         load v2 source
0000494E  E761 0000 0806                00000000 3148+         VL    v22,0(R1)         use v22 to test decoder
00004954  E310 5014 0014                00000014 3149+         LGF   R1,V3ADDR         load v3 source
0000495A  E771 0000 0806                00000000 3150+         VL    v23,0(R1)         use v23 to test decoder
00004960  E310 5018 0014                00000018 3151+         LGF   R1,V4ADDR         load v4 source
00004966  E781 0000 0806                00000000 3152+         VL    v24,0(R1)         use v24 to test decoder
0000496C  E766 7000 8FAE                         3153+         VMAE  V22,V22,V23,V24,0    test instruction (dest is a source)
00004972  E760 5030 080E                00004930 3154+         VST   V22,V1O76          save v1 output
00004978  07FB                                   3155+         BR    R11               return
0000497C                                         3156+RE76     DC    0F                xl16 expected result
0000497C                                         3157+         DROP  R5
0000497C  00010000 00000000                      3158          DC    XL16'0001000000000000 0000000000000000'   result
00004984  00000000 00000000
0000498C  FF000000 00000019                      3159          DC    XL16'FF00000000000019 00000038000000FA'   v2
00004994  00000038 000000FA
0000499C  FF000000 00000019                      3160          DC    XL16'FF00000000000019 00000038000000FA'   v3
000049A4  00000038 000000FA
000049AC  00000000 00000000                      3161          DC    XL16'0000000000000000 0000000000000000'   v4
000049B4  00000000 00000000
                                                 3162
                                                 3163          VRR_D VMAE,0
000049C0                                         3164+         DS    0FD
000049C0                          000049C0       3165+         USING *,R5              base for test data and test routine
000049C0  00004A08                               3166+T77      DC    A(X77)            address of test routine
000049C4  004D                                   3167+         DC    H'77'             test number
000049C6  00                                     3168+         DC    X'00'
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000049C7  00                                       3169+          DC    HL1'0'              m5
000049C8  E5D4C1C5 40404040                        3170+          DC    CL8'VMAE'           instruction name
000049D0  00004A4C                                 3171+          DC    A(RE77+16)          address of v2 source
000049D4  00004A5C                                 3172+          DC    A(RE77+32)          address of v3 source
000049D8  00004A6C                                 3173+          DC    A(RE77+48)          address of v4 source
000049DC  00000010                                 3174+          DC    A(16)               result length
000049E0  00004A3C                                 3175+REA77     DC    A(RE77)             result address
000049E8  00000000 00000000                        3176+          DS    FD                  gap
000049F0  00000000 00000000                        3177+V1O77     DS    XL16                V1 output
000049F8  00000000 00000000
00004A00  00000000 00000000                        3178+          DS    FD                  gap
                                                   3179+*
00004A08                                           3180+X77       DS    0F
00004A08  E310 5010 0014                 00000010  3181+          LGF   R1,V2ADDR           load v2 source
00004A0E  E761 0000 0806                 00000000  3182+          VL    v22,0(R1)           use v22 to test decoder
00004A14  E310 5014 0014                 00000014  3183+          LGF   R1,V3ADDR           load v3 source
00004A1A  E771 0000 0806                 00000000  3184+          VL    v23,0(R1)           use v23 to test decoder
00004A20  E310 5018 0014                 00000018  3185+          LGF   R1,V4ADDR           load v4 source
00004A26  E781 0000 0806                 00000000  3186+          VL    v24,0(R1)           use v24 to test decoder
00004A2C  E766 7000 8FAE                           3187+          VMAE  V22,V22,V23,V24,0    test instruction (dest is a source)
00004A32  E760 5030 080E                 000049F0  3188+          VST   V22,V1O77           save v1 output
00004A38  07FB                                     3189+          BR    R11               return
00004A3C                                           3190+RE77      DC    0F                xl16 expected result
00004A3C                                           3191+          DROP  R5
00004A3C  00030001 0000002F                        3192           DC    XL16'000300010000002F 0000000300000002'   result
00004A44  00000003 00000002
00004A4C  FF0000FF 00000029                        3193           DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00004A54  00000038 000000FA
00004A5C  FF000001 00000029                        3194           DC    XL16'FF00000100000029 00000038000000FA'   v3
00004A64  00000038 000000FA
00004A6C  00020001 0000002F                        3195           DC    XL16'000200010000002F 0000000300000002'   v4
00004A74  00000003 00000002
                                                   3196
                                                   3197           VRR_D VMAE,0
00004A80                                           3198+          DS    0FD
00004A80                      00004A80             3199+          USING *,R5                base for test data and test routine
00004A80  00004AC8                                 3200+T78       DC    A(X78)              address of test routine
00004A84  004E                                     3201+          DC    H'78'               test number
00004A86  00                                       3202+          DC    X'00'
00004A87  00                                       3203+          DC    HL1'0'              m5
00004A88  E5D4C1C5 40404040                        3204+          DC    CL8'VMAE'           instruction name
00004A90  00004B0C                                 3205+          DC    A(RE78+16)          address of v2 source
00004A94  00004B1C                                 3206+          DC    A(RE78+32)          address of v3 source
00004A98  00004B2C                                 3207+          DC    A(RE78+48)          address of v4 source
00004A9C  00000010                                 3208+          DC    A(16)               result length
00004AA0  00004AFC                                 3209+REA78     DC    A(RE78)             result address
00004AA8  00000000 00000000                        3210+          DS    FD                  gap
00004AB0  00000000 00000000                        3211+V1O78     DS    XL16                V1 output
00004AB8  00000000 00000000
00004AC0  00000000 00000000                        3212+          DS    FD                  gap
                                                   3213+*
00004AC8                                           3214+X78       DS    0F
00004AC8  E310 5010 0014                 00000010  3215+          LGF   R1,V2ADDR           load v2 source
00004ACE  E761 0000 0806                 00000000  3216+          VL    v22,0(R1)           use v22 to test decoder
00004AD4  E310 5014 0014                 00000014  3217+          LGF   R1,V3ADDR           load v3 source
00004ADA  E771 0000 0806                 00000000  3218+          VL    v23,0(R1)           use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004AE0  E310 5018 0014                 00000018  3219+          LGF   R1,V4ADDR          load v4 source
00004AE6  E781 0000 0806                 00000000  3220+          VL    v24,0(R1)          use v24 to test decoder
00004AEC  E766 7000 8FAE                           3221+          VMAE  V22,V22,V23,V24,0    test instruction (dest is a source)
00004AF2  E760 5030 080E                 00004AB0  3222+          VST   V22,V1O78           save v1 output
00004AF8  07FB                                     3223+          BR    R11                return
00004AFC                                           3224+RE78      DC    0F                 xl16 expected result
00004AFC                                           3225+          DROP  R5
00004AFC  FF03030D 051F0739                        3226           DC    XL16'FF03030D051F0739 095B0B850DB70FF1'   result
00004B04  095B0B85 0DB70FF1
00004B0C  FF020304 05060708                        3227           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004B14  090A0B0C 0D0E0F10
00004B1C  FF020304 05060708                        3228           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00004B24  090A0B0C 0D0E0F10
00004B2C  FF020304 05060708                        3229           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004B34  090A0B0C 0D0E0F10
                                                   3230
                                                   3231           VRR_D VMAE,0
00004B40                                           3232+          DS    0FD
00004B40                           00004B40        3233+          USING *,R5               base for test data and test routine
00004B40  00004B88                                 3234+T79       DC    A(X79)             address of test routine
00004B44  004F                                     3235+          DC    H'79'              test number
00004B46  00                                       3236+          DC    X'00'
00004B47  00                                       3237+          DC    HL1'0'             m5
00004B48  E5D4C1C5 40404040                        3238+          DC    CL8'VMAE'          instruction name
00004B50  00004BCC                                 3239+          DC    A(RE79+16)         address of v2 source
00004B54  00004BDC                                 3240+          DC    A(RE79+32)         address of v3 source
00004B58  00004BEC                                 3241+          DC    A(RE79+48)         address of v4 source
00004B5C  00000010                                 3242+          DC    A(16)              result length
00004B60  00004BBC                                 3243+REA79     DC    A(RE79)            result address
00004B68  00000000 00000000                        3244+          DS    FD                 gap
00004B70  00000000 00000000                        3245+V1O79     DS    XL16               V1 output
00004B78  00000000 00000000
00004B80  00000000 00000000                        3246+          DS    FD                 gap
                                                   3247+*
00004B88                                           3248+X79       DS    0F
00004B88  E310 5010 0014                 00000010  3249+          LGF   R1,V2ADDR          load v2 source
00004B8E  E761 0000 0806                 00000000  3250+          VL    v22,0(R1)          use v22 to test decoder
00004B94  E310 5014 0014                 00000014  3251+          LGF   R1,V3ADDR          load v3 source
00004B9A  E771 0000 0806                 00000000  3252+          VL    v23,0(R1)          use v23 to test decoder
00004BA0  E310 5018 0014                 00000018  3253+          LGF   R1,V4ADDR          load v4 source
00004BA6  E781 0000 0806                 00000000  3254+          VL    v24,0(R1)          use v24 to test decoder
00004BAC  E766 7000 8FAE                           3255+          VMAE  V22,V22,V23,V24,0    test instruction (dest is a source)
00004BB2  E760 5030 080E                 00004B70  3256+          VST   V22,V1O79           save v1 output
00004BB8  07FB                                     3257+          BR    R11                return
00004BBC                                           3258+RE79      DC    0F                 xl16 expected result
00004BBC                                           3259+          DROP  R5
00004BBC  FF030307 0510071D                        3260           DC    XL16'FF0303070510071D 092E0B430D5C0F79'   result
00004BC4  092E0B43 0D5C0F79
00004BCC  FF020304 05060708                        3261           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004BD4  090A0B0C 0D0E0F10
00004BDC  FF010102 02030304                        3262           DC    XL16'FF01010202030304 0405050606070708'   v3
00004BE4  04050506 06070708
00004BEC  FF020304 05060708                        3263           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004BF4  090A0B0C 0D0E0F10
                                                   3264
                                                   3265           VRR_D VMAE,0
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004C00                                          3266+          DS    0FD
00004C00                      00004C00            3267+          USING *,R5              base for test data and test routine
00004C00  00004C48                                3268+T80       DC    A(X80)            address of test routine
00004C04  0050                                    3269+          DC    H'80'             test number
00004C06  00                                      3270+          DC    X'00'
00004C07  00                                      3271+          DC    HL1'0'            m5
00004C08  E5D4C1C5 40404040                       3272+          DC    CL8'VMAE'         instruction name
00004C10  00004C8C                                3273+          DC    A(RE80+16)        address of v2 source
00004C14  00004C9C                                3274+          DC    A(RE80+32)        address of v3 source
00004C18  00004CAC                                3275+          DC    A(RE80+48)        address of v4 source
00004C1C  00000010                                3276+          DC    A(16)             result length
00004C20  00004C7C                                3277+REA80     DC    A(RE80)           result address
00004C28  00000000 00000000                       3278+          DS    FD                gap
00004C30  00000000 00000000                       3279+V1O80     DS    XL16              V1 output
00004C38  00000000 00000000
00004C40  00000000 00000000                       3280+          DS    FD                gap
                                                  3281+*
00004C48                                          3282+X80       DS    0F
00004C48  E310 5010 0014                00000010  3283+          LGF   R1,V2ADDR         load v2 source
00004C4E  E761 0000 0806                00000000  3284+          VL    v22,0(R1)         use v22 to test decoder
00004C54  E310 5014 0014                00000014  3285+          LGF   R1,V3ADDR         load v3 source
00004C5A  E771 0000 0806                00000000  3286+          VL    v23,0(R1)         use v23 to test decoder
00004C60  E310 5018 0014                00000018  3287+          LGF   R1,V4ADDR         load v4 source
00004C66  E781 0000 0806                00000000  3288+          VL    v24,0(R1)         use v24 to test decoder
00004C6C  E766 7000 8FAE                          3289+          VMAE  V22,V22,V23,V24,0    test instruction (dest is a source)
00004C72  E760 5030 080E                00004C30  3290+          VST   V22,V1O80          save v1 output
00004C78  07FB                                    3291+          BR    R11               return
00004C7C                                          3292+RE80      DC    0F                xl16 expected result
00004C7C                                          3293+          DROP  R5
00004C7C  FF030304 05060708                       3294           DC    XL16'FF03030405060708 09130B170D1B0F1F'   result
00004C84  09130B17 0D1B0F1F
00004C8C  FF020304 05060708                       3295           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004C94  090A0B0C 0D0E0F10
00004C9C  FF000000 00000001                       3296           DC    XL16'FF00000000000001 0101010101010102'   v3
00004CA4  01010101 01010102
00004CAC  FF020304 05060708                       3297           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004CB4  090A0B0C 0D0E0F10
                                                  3298
                                                  3299 * Halfword
                                                  3300           VRR_D VMAE,1
00004CC0                                          3301+          DS    0FD
00004CC0                      00004CC0            3302+          USING *,R5              base for test data and test routine
00004CC0  00004D08                                3303+T81       DC    A(X81)            address of test routine
00004CC4  0051                                    3304+          DC    H'81'             test number
00004CC6  00                                      3305+          DC    X'00'
00004CC7  01                                      3306+          DC    HL1'1'            m5
00004CC8  E5D4C1C5 40404040                       3307+          DC    CL8'VMAE'         instruction name
00004CD0  00004D4C                                3308+          DC    A(RE81+16)        address of v2 source
00004CD4  00004D5C                                3309+          DC    A(RE81+32)        address of v3 source
00004CD8  00004D6C                                3310+          DC    A(RE81+48)        address of v4 source
00004CDC  00000010                                3311+          DC    A(16)             result length
00004CE0  00004D3C                                3312+REA81     DC    A(RE81)           result address
00004CE8  00000000 00000000                       3313+          DS    FD                gap
00004CF0  00000000 00000000                       3314+V1O81     DS    XL16              V1 output
00004CF8  00000000 00000000
00004D00  00000000 00000000                       3315+          DS    FD                gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   3316+*
00004D08                                           3317+X81      DS    0F
00004D08  E310 5010 0014                 00000010  3318+         LGF   R1,V2ADDR         load v2 source
00004D0E  E761 0000 0806                 00000000  3319+         VL    v22,0(R1)         use v22 to test decoder
00004D14  E310 5014 0014                 00000014  3320+         LGF   R1,V3ADDR         load v3 source
00004D1A  E771 0000 0806                 00000000  3321+         VL    v23,0(R1)         use v23 to test decoder
00004D20  E310 5018 0014                 00000018  3322+         LGF   R1,V4ADDR         load v4 source
00004D26  E781 0000 0806                 00000000  3323+         VL    v24,0(R1)         use v24 to test decoder
00004D2C  E766 7100 8FAE                           3324+         VMAE  V22,V22,V23,V24,1    test instruction (dest is a source)
00004D32  E760 5030 080E                 00004CF0  3325+         VST   V22,V1O81          save v1 output
00004D38  07FB                                     3326+         BR    R11               return
00004D3C                                           3327+RE81     DC    0F                xl16 expected result
00004D3C                                           3328+         DROP  R5
00004D3C  00010000 00000000                        3329          DC    XL16'0001000000000000 0000000000000000'   result
00004D44  00000000 00000000
00004D4C  FF000000 00000019                        3330          DC    XL16'FF00000000000019 00000038000000FA'   v2
00004D54  00000038 000000FA
00004D5C  FF000000 00000019                        3331          DC    XL16'FF00000000000019 00000038000000FA'   v3
00004D64  00000038 000000FA
00004D6C  00000000 00000000                        3332          DC    XL16'0000000000000000 0000000000000000'   v4
00004D74  00000000 00000000
                                                   3333
                                                   3334          VRR_D VMAE,1
00004D80                                           3335+         DS    0FD
00004D80                 00004D80                  3336+         USING *,R5              base for test data and test routine
00004D80  00004DC8                                 3337+T82      DC    A(X82)            address of test routine
00004D84  0052                                     3338+         DC    H'82'             test number
00004D86  00                                       3339+         DC    X'00'
00004D87  01                                       3340+         DC    HL1'1'            m5
00004D88  E5D4C1C5 40404040                        3341+         DC    CL8'VMAE'         instruction name
00004D90  00004E0C                                 3342+         DC    A(RE82+16)        address of v2 source
00004D94  00004E1C                                 3343+         DC    A(RE82+32)        address of v3 source
00004D98  00004E2C                                 3344+         DC    A(RE82+48)        address of v4 source
00004D9C  00000010                                 3345+         DC    A(16)             result length
00004DA0  00004DFC                                 3346+REA82    DC    A(RE82)           result address
00004DA8  00000000 00000000                        3347+         DS    FD                gap
00004DB0  00000000 00000000                        3348+V1O82    DS    XL16              V1 output
00004DB8  00000000 00000000
00004DC0  00000000 00000000                        3349+         DS    FD                gap
                                                   3350+*
00004DC8                                           3351+X82      DS    0F
00004DC8  E310 5010 0014                 00000010  3352+         LGF   R1,V2ADDR         load v2 source
00004DCE  E761 0000 0806                 00000000  3353+         VL    v22,0(R1)         use v22 to test decoder
00004DD4  E310 5014 0014                 00000014  3354+         LGF   R1,V3ADDR         load v3 source
00004DDA  E771 0000 0806                 00000000  3355+         VL    v23,0(R1)         use v23 to test decoder
00004DE0  E310 5018 0014                 00000018  3356+         LGF   R1,V4ADDR         load v4 source
00004DE6  E781 0000 0806                 00000000  3357+         VL    v24,0(R1)         use v24 to test decoder
00004DEC  E766 7100 8FAE                           3358+         VMAE  V22,V22,V23,V24,1    test instruction (dest is a source)
00004DF2  E760 5030 080E                 00004DB0  3359+         VST   V22,V1O82          save v1 output
00004DF8  07FB                                     3360+         BR    R11               return
00004DFC                                           3361+RE82     DC    0F                xl16 expected result
00004DFC                                           3362+         DROP  R5
00004DFC  00030001 0000002F                        3363          DC    XL16'000300010000002F 0000000300000002'   result
00004E04  00000003 00000002
00004E0C  FF0000FF 00000029                        3364          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00004E14  00000038 000000FA
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004E1C  FF000001 00000029                        3365          DC    XL16'FF00000100000029 00000038000000FA'   v3
00004E24  00000038 000000FA
00004E2C  00020001 0000002F                        3366          DC    XL16'00020001000002F 0000000300000002'   v4
00004E34  00000003 00000002
                                                   3367
                                                   3368          VRR_D VMAE,1
00004E40                                           3369+         DS    0FD
00004E40                     00004E40              3370+         USING *,R5              base for test data and test routine
00004E40  00004E88                                 3371+T83      DC    A(X83)            address of test routine
00004E44  0053                                     3372+         DC    H'83'             test number
00004E46  00                                       3373+         DC    X'00'
00004E47  01                                       3374+         DC    HL1'1'            m5
00004E48  E5D4C1C5 40404040                        3375+         DC    CL8'VMAE'         instruction name
00004E50  00004ECC                                 3376+         DC    A(RE83+16)        address of v2 source
00004E54  00004EDC                                 3377+         DC    A(RE83+32)        address of v3 source
00004E58  00004EEC                                 3378+         DC    A(RE83+48)        address of v4 source
00004E5C  00000010                                 3379+         DC    A(16)             result length
00004E60  00004EBC                                 3380+REA83    DC    A(RE83)           result address
00004E68  00000000 00000000                        3381+         DS    FD                gap
00004E70  00000000 00000000                        3382+V1O83    DS    XL16              V1 output
00004E78  00000000 00000000
00004E80  00000000 00000000                        3383+         DS    FD                gap
                                                   3384+*
00004E88                                           3385+X83      DS    0F
00004E88  E310 5010 0014                 00000010  3386+         LGF   R1,V2ADDR         load v2 source
00004E8E  E761 0000 0806                 00000000  3387+         VL    v22,0(R1)         use v22 to test decoder
00004E94  E310 5014 0014                 00000014  3388+         LGF   R1,V3ADDR         load v3 source
00004E9A  E771 0000 0806                 00000000  3389+         VL    v23,0(R1)         use v23 to test decoder
00004EA0  E310 5018 0014                 00000018  3390+         LGF   R1,V4ADDR         load v4 source
00004EA6  E781 0000 0806                 00000000  3391+         VL    v24,0(R1)         use v24 to test decoder
00004EAC  E766 7100 8FAE                           3392+         VMAE  V22,V22,V23,V24,1    test instruction (dest is a source)
00004EB2  E760 5030 080E                 00004E70  3393+         VST   V22,V1O83          save v1 output
00004EB8  07FB                                     3394+         BR    R11               return
00004EBC                                           3395+RE83     DC    0F                xl16 expected result
00004EBC                                           3396+         DROP  R5
00004EBC  FF02FF08 051F432C                        3397          DC    XL16'FF02FF08051F432C 095BBF700DB87BD4'   result
00004EC4  095BBF70 0DB87BD4
00004ECC  FF020304 05060708                        3398          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004ED4  090A0B0C 0D0E0F10
00004EDC  FF020304 05060708                        3399          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00004EE4  090A0B0C 0D0E0F10
00004EEC  FF020304 05060708                        3400          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004EF4  090A0B0C 0D0E0F10
                                                   3401
                                                   3402          VRR_D VMAE,1
00004F00                                           3403+         DS    0FD
00004F00                     00004F00              3404+         USING *,R5              base for test data and test routine
00004F00  00004F48                                 3405+T84      DC    A(X84)            address of test routine
00004F04  0054                                     3406+         DC    H'84'             test number
00004F06  00                                       3407+         DC    X'00'
00004F07  01                                       3408+         DC    HL1'1'            m5
00004F08  E5D4C1C5 40404040                        3409+         DC    CL8'VMAE'         instruction name
00004F10  00004F8C                                 3410+         DC    A(RE84+16)        address of v2 source
00004F14  00004F9C                                 3411+         DC    A(RE84+32)        address of v3 source
00004F18  00004FAC                                 3412+         DC    A(RE84+48)        address of v4 source
00004F1C  00000010                                 3413+         DC    A(16)             result length
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00004F20  00004F7C                        3414+REA84    DC    A(RE84)           result address
00004F28  00000000 00000000               3415+         DS    FD                gap
00004F30  00000000 00000000               3416+V1O84    DS    XL16              V1 output
00004F38  00000000 00000000
00004F40  00000000 00000000               3417+         DS    FD                gap
                                          3418+*
00004F48                                  3419+X84      DS    0F
00004F48  E310 5010 0014          00000010 3420+         LGF   R1,V2ADDR         load v2 source
00004F4E  E761 0000 0806          00000000 3421+         VL    v22,0(R1)         use v22 to test decoder
00004F54  E310 5014 0014          00000014 3422+         LGF   R1,V3ADDR         load v3 source
00004F5A  E771 0000 0806          00000000 3423+         VL    v23,0(R1)         use v23 to test decoder
00004F60  E310 5018 0014          00000018 3424+         LGF   R1,V4ADDR         load v4 source
00004F66  E781 0000 0806          00000000 3425+         VL    v24,0(R1)         use v24 to test decoder
00004F6C  E766 7100 8FAE                   3426+         VMAE  V22,V22,V23,V24,1    test instruction (dest is a source)
00004F72  E760 5030 080E          00004F30 3427+         VST   V22,V1O84          save v1 output
00004F78  07FB                             3428+         BR    R11               return
00004F7C                                   3429+RE84     DC    0F                xl16 expected result
00004F7C                                   3430+         DROP  R5
00004F7C  FF030006 0510221A                3431          DC    XL16'FF0300060510221A 092E603E0D5CBE72'   result
00004F84  092E603E 0D5CBE72
00004F8C  FF020304 05060708                3432          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00004F94  090A0B0C 0D0E0F10
00004F9C  FF010102 02030304                3433          DC    XL16'FF01010202030304 0405050606070708'   v3
00004FA4  04050506 06070708
00004FAC  FF020304 05060708                3434          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00004FB4  090A0B0C 0D0E0F10
                                           3435
                                           3436          VRR_D VMAE,1
00004FC0                                   3437+         DS    0FD
00004FC0                       00004FC0    3438+         USING *,R5              base for test data and test routine
00004FC0  00005008                         3439+T85      DC    A(X85)            address of test routine
00004FC4  0055                             3440+         DC    H'85'             test number
00004FC6  00                               3441+         DC    X'00'
00004FC7  01                               3442+         DC    HL1'1'            m5
00004FC8  E5D4C1C5 40404040                3443+         DC    CL8'VMAE'         instruction name
00004FD0  0000504C                         3444+         DC    A(RE85+16)        address of v2 source
00004FD4  0000505C                         3445+         DC    A(RE85+32)        address of v3 source
00004FD8  0000506C                         3446+         DC    A(RE85+48)        address of v4 source
00004FDC  00000010                         3447+         DC    A(16)             result length
00004FE0  0000503C                         3448+REA85    DC    A(RE85)           result address
00004FE8  00000000 00000000                3449+         DS    FD                gap
00004FF0  00000000 00000000                3450+V1O85    DS    XL16              V1 output
00004FF8  00000000 00000000
00005000  00000000 00000000                3451+         DS    FD                gap
                                           3452+*
00005008                                   3453+X85      DS    0F
00005008  E310 5010 0014          00000010 3454+         LGF   R1,V2ADDR         load v2 source
0000500E  E761 0000 0806          00000000 3455+         VL    v22,0(R1)         use v22 to test decoder
00005014  E310 5014 0014          00000014 3456+         LGF   R1,V3ADDR         load v3 source
0000501A  E771 0000 0806          00000000 3457+         VL    v23,0(R1)         use v23 to test decoder
00005020  E310 5018 0014          00000018 3458+         LGF   R1,V4ADDR         load v4 source
00005026  E781 0000 0806          00000000 3459+         VL    v24,0(R1)         use v24 to test decoder
0000502C  E766 7100 8FAE                   3460+         VMAE  V22,V22,V23,V24,1    test instruction (dest is a source)
00005032  E760 5030 080E          00004FF0 3461+         VST   V22,V1O85          save v1 output
00005038  07FB                             3462+         BR    R11               return
0000503C                                   3463+RE85     DC    0F                xl16 expected result
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000503C                                          3464+          DROP  R5
0000503C  FF030104 05060708                       3465           DC    XL16'FF03010405060708 09131E160D1B2A1E'   result
00005044  09131E16 0D1B2A1E
0000504C  FF020304 05060708                       3466           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005054  090A0B0C 0D0E0F10
0000505C  FF000000 00000001                       3467           DC    XL16'FF00000000000001 0101010101010102'   v3
00005064  01010101 01010102
0000506C  FF020304 05060708                       3468           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005074  090A0B0C 0D0E0F10
                                                  3469
                                                  3470 * Word
                                                  3471           VRR_D VMAE,2
00005080                                          3472+          DS    0FD
00005080                          00005080        3473+          USING *,R5              base for test data and test routine
00005080  000050C8                                3474+T86       DC    A(X86)            address of test routine
00005084  0056                                    3475+          DC    H'86'             test number
00005086  00                                      3476+          DC    X'00'
00005087  02                                      3477+          DC    HL1'2'            m5
00005088  E5D4C1C5 40404040                       3478+          DC    CL8'VMAE'         instruction name
00005090  0000510C                                3479+          DC    A(RE86+16)        address of v2 source
00005094  0000511C                                3480+          DC    A(RE86+32)        address of v3 source
00005098  0000512C                                3481+          DC    A(RE86+48)        address of v4 source
0000509C  00000010                                3482+          DC    A(16)             result length
000050A0  000050FC                                3483+REA86     DC    A(RE86)           result address
000050A8  00000000 00000000                       3484+          DS    FD                gap
000050B0  00000000 00000000                       3485+V1O86     DS    XL16              V1 output
000050B8  00000000 00000000
000050C0  00000000 00000000                       3486+          DS    FD                gap
                                                  3487+*
000050C8                                          3488+X86       DS    0F
000050C8  E310 5010 0014                 00000010 3489+          LGF   R1,V2ADDR         load v2 source
000050CE  E761 0000 0806                 00000000 3490+          VL    v22,0(R1)         use v22 to test decoder
000050D4  E310 5014 0014                 00000014 3491+          LGF   R1,V3ADDR         load v3 source
000050DA  E771 0000 0806                 00000000 3492+          VL    v23,0(R1)         use v23 to test decoder
000050E0  E310 5018 0014                 00000018 3493+          LGF   R1,V4ADDR         load v4 source
000050E6  E781 0000 0806                 00000000 3494+          VL    v24,0(R1)         use v24 to test decoder
000050EC  E766 7200 8FAE                          3495+          VMAE  V22,V22,V23,V24,2    test instruction (dest is a source)
000050F2  E760 5030 080E                 000050B0 3496+          VST   V22,V1O86          save v1 output
000050F8  07FB                                    3497+          BR    R11               return
000050FC                                          3498+RE86      DC    0F                xl16 expected result
000050FC                                          3499+          DROP  R5
000050FC  00010000 00000000                       3500           DC    XL16'0001000000000000 0000000000000C40'   result
00005104  00000000 00000C40
0000510C  FF000000 00000019                       3501           DC    XL16'FF00000000000019 00000038000000FA'   v2
00005114  00000038 000000FA
0000511C  FF000000 00000019                       3502           DC    XL16'FF00000000000019 00000038000000FA'   v3
00005124  00000038 000000FA
0000512C  00000000 00000000                       3503           DC    XL16'0000000000000000 0000000000000000'   v4
00005134  00000000 00000000
                                                  3504
                                                  3505           VRR_D VMAE,2
00005140                                          3506+          DS    0FD
00005140                          00005140        3507+          USING *,R5              base for test data and test routine
00005140  00005188                                3508+T87       DC    A(X87)            address of test routine
00005144  0057                                    3509+          DC    H'87'             test number
00005146  00                                      3510+          DC    X'00'
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005147  02                                      3511+          DC    HL1'2'              m5
00005148  E5D4C1C5 40404040                       3512+          DC    CL8'VMAE'           instruction name
00005150  000051CC                                3513+          DC    A(RE87+16)          address of v2 source
00005154  000051DC                                3514+          DC    A(RE87+32)          address of v3 source
00005158  000051EC                                3515+          DC    A(RE87+48)          address of v4 source
0000515C  00000010                                3516+          DC    A(16)               result length
00005160  000051BC                                3517+REA87     DC    A(RE87)             result address
00005168  00000000 00000000                       3518+          DS    FD                  gap
00005170  00000000 00000000                       3519+V1O87     DS    XL16                V1 output
00005178  00000000 00000000
00005180  00000000 00000000                       3520+          DS    FD                  gap
                                                  3521+*
00005188                                          3522+X87       DS    0F
00005188  E310 5010 0014                 00000010 3523+          LGF   R1,V2ADDR           load v2 source
0000518E  E761 0000 0806                 00000000 3524+          VL    v22,0(R1)           use v22 to test decoder
00005194  E310 5014 0014                 00000014 3525+          LGF   R1,V3ADDR           load v3 source
0000519A  E771 0000 0806                 00000000 3526+          VL    v23,0(R1)           use v23 to test decoder
000051A0  E310 5018 0014                 00000018 3527+          LGF   R1,V4ADDR           load v4 source
000051A6  E781 0000 0806                 00000000 3528+          VL    v24,0(R1)           use v24 to test decoder
000051AC  E766 7200 8FAE                          3529+          VMAE  V22,V22,V23,V24,2    test instruction (dest is a source)
000051B2  E760 5030 080E                 00005170 3530+          VST   V22,V1O87            save v1 output
000051B8  07FB                                    3531+          BR    R11                 return
000051BC                                          3532+RE87      DC    0F                  xl16 expected result
000051BC                                          3533+          DROP  R5
000051BC  00030000 0000012E                       3534           DC    XL16'000300000000012E 0000000300000C42'   result
000051C4  00000003 00000C42
000051CC  FF0000FF 00000029                       3535           DC    XL16'FF0000FF00000029 00000038000000FA'   v2
000051D4  00000038 000000FA
000051DC  FF000001 00000029                       3536           DC    XL16'FF00000100000029 00000038000000FA'   v3
000051E4  00000038 000000FA
000051EC  00020001 0000002F                       3537           DC    XL16'000200010000002F 0000000300000002'   v4
000051F4  00000003 00000002
                                                  3538
                                                  3539           VRR_D VMAE,2
00005200                                          3540+          DS    0FD
00005200                         00005200         3541+          USING *,R5                base for test data and test routine
00005200  00005248                                3542+T88       DC    A(X88)              address of test routine
00005204  0058                                    3543+          DC    H'88'               test number
00005206  00                                      3544+          DC    X'00'
00005207  02                                      3545+          DC    HL1'2'              m5
00005208  E5D4C1C5 40404040                       3546+          DC    CL8'VMAE'           instruction name
00005210  0000528C                                3547+          DC    A(RE88+16)          address of v2 source
00005214  0000529C                                3548+          DC    A(RE88+32)          address of v3 source
00005218  000052AC                                3549+          DC    A(RE88+48)          address of v4 source
0000521C  00000010                                3550+          DC    A(16)               result length
00005220  0000527C                                3551+REA88     DC    A(RE88)             result address
00005228  00000000 00000000                       3552+          DS    FD                  gap
00005230  00000000 00000000                       3553+V1O88     DS    XL16                V1 output
00005238  00000000 00000000
00005240  00000000 00000000                       3554+          DS    FD                  gap
                                                  3555+*
00005248                                          3556+X88       DS    0F
00005248  E310 5010 0014                 00000010 3557+          LGF   R1,V2ADDR           load v2 source
0000524E  E761 0000 0806                 00000000 3558+          VL    v22,0(R1)           use v22 to test decoder
00005254  E310 5014 0014                 00000014 3559+          LGF   R1,V3ADDR           load v3 source
0000525A  E771 0000 0806                 00000000 3560+          VL    v23,0(R1)           use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005260  E310 5018 0014                 00000018  3561+          LGF   R1,V4ADDR          load v4 source
00005266  E781 0000 0806                 00000000  3562+          VL    v24,0(R1)          use v24 to test decoder
0000526C  E766 7200 8FAE                           3563+          VMAE  V22,V22,V23,V24,2    test instruction (dest is a source)
00005272  E760 5030 080E                 00005230  3564+          VST   V22,V1O88           save v1 output
00005278  07FB                                     3565+          BR    R11                return
0000527C                                           3566+RE88      DC    0F                 xl16 expected result
0000527C                                           3567+          DROP  R5
0000527C  FF02FF02 091F1F18                        3568           DC    XL16'FF02FF02091F1F18 095BC037C27817A0'   result
00005284  095BC037 C27817A0
0000528C  FF020304 05060708                        3569           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005294  090A0B0C 0D0E0F10
0000529C  FF020304 05060708                        3570           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
000052A4  090A0B0C 0D0E0F10
000052AC  FF020304 05060708                        3571           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000052B4  090A0B0C 0D0E0F10
                                                   3572
                                                   3573           VRR_D VMAE,2
000052C0                                           3574+          DS    0FD
000052C0                         000052C0          3575+          USING *,R5               base for test data and test routine
000052C0  00005308                                 3576+T89       DC    A(X89)             address of test routine
000052C4  0059                                     3577+          DC    H'89'              test number
000052C6  00                                       3578+          DC    X'00'
000052C7  02                                       3579+          DC    HL1'2'             m5
000052C8  E5D4C1C5 40404040                        3580+          DC    CL8'VMAE'          instruction name
000052D0  0000534C                                 3581+          DC    A(RE89+16)         address of v2 source
000052D4  0000535C                                 3582+          DC    A(RE89+32)         address of v3 source
000052D8  0000536C                                 3583+          DC    A(RE89+48)         address of v4 source
000052DC  00000010                                 3584+          DC    A(16)              result length
000052E0  0000533C                                 3585+REA89     DC    A(RE89)            result address
000052E8  00000000 00000000                        3586+          DS    FD                 gap
000052F0  00000000 00000000                        3587+V1O89     DS    XL16               V1 output
000052F8  00000000 00000000
00005300  00000000 00000000                        3588+          DS    FD                 gap
                                                   3589+*
00005308                                           3590+X89       DS    0F
00005308  E310 5010 0014                 00000010  3591+          LGF   R1,V2ADDR          load v2 source
0000530E  E761 0000 0806                 00000000  3592+          VL    v22,0(R1)          use v22 to test decoder
00005314  E310 5014 0014                 00000014  3593+          LGF   R1,V3ADDR          load v3 source
0000531A  E771 0000 0806                 00000000  3594+          VL    v23,0(R1)          use v23 to test decoder
00005320  E310 5018 0014                 00000018  3595+          LGF   R1,V4ADDR          load v4 source
00005326  E781 0000 0806                 00000000  3596+          VL    v24,0(R1)          use v24 to test decoder
0000532C  E766 7200 8FAE                           3597+          VMAE  V22,V22,V23,V24,2    test instruction (dest is a source)
00005332  E760 5030 080E                 000052F0  3598+          VST   V22,V1O89           save v1 output
00005338  07FB                                     3599+          BR    R11                return
0000533C                                           3600+RE89      DC    0F                 xl16 expected result
0000533C                                           3601+          DROP  R5
0000533C  FF030002 04111110                        3602           DC    XL16'FF03000204111110 092E6097DCBD8D58'   result
00005344  092E6097 DCBD8D58
0000534C  FF020304 05060708                        3603           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005354  090A0B0C 0D0E0F10
0000535C  FF010102 02030304                        3604           DC    XL16'FF01010202030304 0405050606070708'   v3
00005364  04050506 06070708
0000536C  FF020304 05060708                        3605           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005374  090A0B0C 0D0E0F10
                                                   3606
                                                   3607           VRR_D VMAE,2
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005380                                          3608+         DS    0FD
00005380                     00005380             3609+         USING *,R5              base for test data and test routine
00005380  000053C8                                3610+T90      DC    A(X90)            address of test routine
00005384  005A                                    3611+         DC    H'90'             test number
00005386  00                                      3612+         DC    X'00'
00005387  02                                      3613+         DC    HL1'2'            m5
00005388  E5D4C1C5 40404040                       3614+         DC    CL8'VMAE'         instruction name
00005390  0000540C                                3615+         DC    A(RE90+16)        address of v2 source
00005394  0000541C                                3616+         DC    A(RE90+32)        address of v3 source
00005398  0000542C                                3617+         DC    A(RE90+48)        address of v4 source
0000539C  00000010                                3618+         DC    A(16)             result length
000053A0  000053FC                                3619+REA90    DC    A(RE90)           result address
000053A8  00000000 00000000                       3620+         DS    FD                gap
000053B0  00000000 00000000                       3621+V1O90    DS    XL16              V1 output
000053B8  00000000 00000000
000053C0  00000000 00000000                       3622+         DS    FD                gap
                                                  3623+*
000053C8                                          3624+X90      DS    0F
000053C8  E310 5010 0014                00000010  3625+         LGF   R1,V2ADDR         load v2 source
000053CE  E761 0000 0806                00000000  3626+         VL    v22,0(R1)         use v22 to test decoder
000053D4  E310 5014 0014                00000014  3627+         LGF   R1,V3ADDR         load v3 source
000053DA  E771 0000 0806                00000000  3628+         VL    v23,0(R1)         use v23 to test decoder
000053E0  E310 5018 0014                00000018  3629+         LGF   R1,V4ADDR         load v4 source
000053E6  E781 0000 0806                00000000  3630+         VL    v24,0(R1)         use v24 to test decoder
000053EC  E766 7200 8FAE                          3631+         VMAE  V22,V22,V23,V24,2    test instruction (dest is a source)
000053F2  E760 5030 080E                000053B0  3632+         VST   V22,V1O90          save v1 output
000053F8  07FB                                    3633+         BR    R11               return
000053FC                                          3634+RE90     DC    0F                xl16 expected result
000053FC                                          3635+         DROP  R5
000053FC  FF030101 01060708                       3636          DC    XL16'FF03010101060708 09131E2A372F261C'   result
00005404  09131E2A 372F261C
0000540C  FF020304 05060708                       3637          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005414  090A0B0C 0D0E0F10
0000541C  FF000000 00000001                       3638          DC    XL16'FF00000000000001 0101010101010102'   v3
00005424  01010101 01010102
0000542C  FF020304 05060708                       3639          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005434  090A0B0C 0D0E0F10
                                                  3640
                                                  3641 *-------------------------------------------------------------------
                                                  3642 * VMAO   - Vector Multiply and Add Odd
                                                  3643 *-------------------------------------------------------------------
                                                  3644 * Byte
                                                  3645          VRR_D VMAO,0
00005440                                          3646+         DS    0FD
00005440                     00005440             3647+         USING *,R5              base for test data and test routine
00005440  00005488                                3648+T91      DC    A(X91)            address of test routine
00005444  005B                                    3649+         DC    H'91'             test number
00005446  00                                      3650+         DC    X'00'
00005447  00                                      3651+         DC    HL1'0'            m5
00005448  E5D4C1D6 40404040                       3652+         DC    CL8'VMAO'         instruction name
00005450  000054CC                                3653+         DC    A(RE91+16)        address of v2 source
00005454  000054DC                                3654+         DC    A(RE91+32)        address of v3 source
00005458  000054EC                                3655+         DC    A(RE91+48)        address of v4 source
0000545C  00000010                                3656+         DC    A(16)             result length
00005460  000054BC                                3657+REA91    DC    A(RE91)           result address
00005468  00000000 00000000                       3658+         DS    FD                gap
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005470  00000000 00000000                       3659+V1O91    DS    XL16              V1 output
00005478  00000000 00000000
00005480  00000000 00000000                       3660+         DS    FD                gap
                                                  3661+*
00005488                                          3662+X91      DS    0F
00005488  E310 5010 0014                 00000010 3663+         LGF   R1,V2ADDR         load v2 source
0000548E  E761 0000 0806                 00000000 3664+         VL    v22,0(R1)         use v22 to test decoder
00005494  E310 5014 0014                 00000014 3665+         LGF   R1,V3ADDR         load v3 source
0000549A  E771 0000 0806                 00000000 3666+         VL    v23,0(R1)         use v23 to test decoder
000054A0  E310 5018 0014                 00000018 3667+         LGF   R1,V4ADDR         load v4 source
000054A6  E781 0000 0806                 00000000 3668+         VL    v24,0(R1)         use v24 to test decoder
000054AC  E766 7000 8FAF                          3669+         VMAO  V22,V22,V23,V24,0    test instruction (dest is a source)
000054B2  E760 5030 080E                 00005470 3670+         VST   V22,V1O91          save v1 output
000054B8  07FB                                    3671+         BR    R11               return
000054BC                                          3672+RE91     DC    0F                xl16 expected result
000054BC                                          3673+         DROP  R5
000054BC  00000000 00000271                       3674          DC    XL16'0000000000000271 00000C4000000024'   result
000054C4  00000C40 00000024
000054CC  FF000000 00000019                       3675          DC    XL16'FF00000000000019 00000038000000FA'   v2
000054D4  00000038 000000FA
000054DC  FF000000 00000019                       3676          DC    XL16'FF00000000000019 00000038000000FA'   v3
000054E4  00000038 000000FA
000054EC  00000000 00000000                       3677          DC    XL16'0000000000000000 0000000000000000'   v4
000054F4  00000000 00000000
                                                  3678
                                                  3679          VRR_D VMAO,0
00005500                                          3680+         DS    0FD
00005500                  00005500                3681+         USING *,R5              base for test data and test routine
00005500  00005548                                3682+T92      DC    A(X92)            address of test routine
00005504  005C                                    3683+         DC    H'92'             test number
00005506  00                                      3684+         DC    X'00'
00005507  00                                      3685+         DC    HL1'0'            m5
00005508  E5D4C1D6 40404040                       3686+         DC    CL8'VMAO'         instruction name
00005510  0000558C                                3687+         DC    A(RE92+16)        address of v2 source
00005514  0000559C                                3688+         DC    A(RE92+32)        address of v3 source
00005518  000055AC                                3689+         DC    A(RE92+48)        address of v4 source
0000551C  00000010                                3690+         DC    A(16)             result length
00005520  0000557C                                3691+REA92    DC    A(RE92)           result address
00005528  00000000 00000000                       3692+         DS    FD                gap
00005530  00000000 00000000                       3693+V1O92    DS    XL16              V1 output
00005538  00000000 00000000
00005540  00000000 00000000                       3694+         DS    FD                gap
                                                  3695+*
00005548                                          3696+X92      DS    0F
00005548  E310 5010 0014                 00000010 3697+         LGF   R1,V2ADDR         load v2 source
0000554E  E761 0000 0806                 00000000 3698+         VL    v22,0(R1)         use v22 to test decoder
00005554  E310 5014 0014                 00000014 3699+         LGF   R1,V3ADDR         load v3 source
0000555A  E771 0000 0806                 00000000 3700+         VL    v23,0(R1)         use v23 to test decoder
00005560  E310 5018 0014                 00000018 3701+         LGF   R1,V4ADDR         load v4 source
00005566  E781 0000 0806                 00000000 3702+         VL    v24,0(R1)         use v24 to test decoder
0000556C  E766 7000 8FAF                          3703+         VMAO  V22,V22,V23,V24,0    test instruction (dest is a source)
00005572  E760 5030 080E                 00005530 3704+         VST   V22,V1O92          save v1 output
00005578  07FB                                    3705+         BR    R11               return
0000557C                                          3706+RE92     DC    0F                xl16 expected result
0000557C                                          3707+         DROP  R5
0000557C  00020000 000006C0                       3708          DC    XL16'00020000000006C0 00000C4300000026'   result
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005584  00000C43 00000026
0000558C  FF0000FF 00000029                        3709          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00005594  00000038 000000FA
0000559C  FF000001 00000029                        3710          DC    XL16'FF00000100000029 00000038000000FA'   v3
000055A4  00000038 000000FA
000055AC  00020001 0000002F                        3711          DC    XL16'00020001000002F 0000000300000002'   v4
000055B4  00000003 00000002
                                                   3712
                                                   3713          VRR_D VMAO,0
000055C0                                           3714+         DS    0FD
000055C0                     000055C0              3715+         USING *,R5              base for test data and test routine
000055C0  00005608                                 3716+T93      DC    A(X93)            address of test routine
000055C4  005D                                     3717+         DC    H'93'             test number
000055C6  00                                       3718+         DC    X'00'
000055C7  00                                       3719+         DC    HL1'0'            m5
000055C8  E5D4C1D6 40404040                        3720+         DC    CL8'VMAO'         instruction name
000055D0  0000564C                                 3721+         DC    A(RE93+16)        address of v2 source
000055D4  0000565C                                 3722+         DC    A(RE93+32)        address of v3 source
000055D8  0000566C                                 3723+         DC    A(RE93+48)        address of v4 source
000055DC  00000010                                 3724+         DC    A(16)             result length
000055E0  0000563C                                 3725+REA93    DC    A(RE93)           result address
000055E8  00000000 00000000                        3726+         DS    FD                gap
000055F0  00000000 00000000                        3727+V1O93    DS    XL16              V1 output
000055F8  00000000 00000000
00005600  00000000 00000000                        3728+         DS    FD                gap
                                                   3729+*
00005608                                           3730+X93      DS    0F
00005608  E310 5010 0014                 00000010  3731+         LGF   R1,V2ADDR         load v2 source
0000560E  E761 0000 0806                 00000000  3732+         VL    v22,0(R1)         use v22 to test decoder
00005614  E310 5014 0014                 00000014  3733+         LGF   R1,V3ADDR         load v3 source
0000561A  E771 0000 0806                 00000000  3734+         VL    v23,0(R1)         use v23 to test decoder
00005620  E310 5018 0014                 00000018  3735+         LGF   R1,V4ADDR         load v4 source
00005626  E781 0000 0806                 00000000  3736+         VL    v24,0(R1)         use v24 to test decoder
0000562C  E766 7000 8FAF                           3737+         VMAO  V22,V22,V23,V24,0    test instruction (dest is a source)
00005632  E760 5030 080E                 000055F0  3738+         VST   V22,V1O93          save v1 output
00005638  07FB                                     3739+         BR    R11               return
0000563C                                           3740+RE93     DC    0F                xl16 expected result
0000563C                                           3741+         DROP  R5
0000563C  FF060314 052A0748                        3742          DC    XL16'FF060314052A0748 096E0B9C0DD21010'   result
00005644  096E0B9C 0DD21010
0000564C  FF020304 05060708                        3743          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005654  090A0B0C 0D0E0F10
0000565C  FF020304 05060708                        3744          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00005664  090A0B0C 0D0E0F10
0000566C  FF020304 05060708                        3745          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005674  090A0B0C 0D0E0F10
                                                   3746
                                                   3747          VRR_D VMAO,0
00005680                                           3748+         DS    0FD
00005680                     00005680              3749+         USING *,R5              base for test data and test routine
00005680  000056C8                                 3750+T94      DC    A(X94)            address of test routine
00005684  005E                                     3751+         DC    H'94'             test number
00005686  00                                       3752+         DC    X'00'
00005687  00                                       3753+         DC    HL1'0'            m5
00005688  E5D4C1D6 40404040                        3754+         DC    CL8'VMAO'         instruction name
00005690  0000570C                                 3755+         DC    A(RE94+16)        address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005694  0000571C                          3756+          DC    A(RE94+32)          address of v3 source
00005698  0000572C                          3757+          DC    A(RE94+48)          address of v4 source
0000569C  00000010                          3758+          DC    A(16)               result length
000056A0  000056FC                          3759+REA94     DC    A(RE94)             result address
000056A8  00000000 00000000                 3760+          DS    FD                  gap
000056B0  00000000 00000000                 3761+V1O94     DS    XL16                V1 output
000056B8  00000000 00000000
000056C0  00000000 00000000                 3762+          DS    FD                  gap
                                            3763+*
000056C8                                    3764+X94       DS    0F
000056C8  E310 5010 0014              00000010  3765+      LGF   R1,V2ADDR           load v2 source
000056CE  E761 0000 0806              00000000  3766+      VL    v22,0(R1)           use v22 to test decoder
000056D4  E310 5014 0014              00000014  3767+      LGF   R1,V3ADDR           load v3 source
000056DA  E771 0000 0806              00000000  3768+      VL    v23,0(R1)           use v23 to test decoder
000056E0  E310 5018 0014              00000018  3769+      LGF   R1,V4ADDR           load v4 source
000056E6  E781 0000 0806              00000000  3770+      VL    v24,0(R1)           use v24 to test decoder
000056EC  E766 7000 8FAF                        3771+      VMAO  V22,V22,V23,V24,0     test instruction (dest is a source)
000056F2  E760 5030 080E              000056B0  3772+      VST   V22,V1O94           save v1 output
000056F8  07FB                              3773+          BR    R11                 return
000056FC                                    3774+RE94      DC    0F                  xl16 expected result
000056FC                                    3775+          DROP  R5
000056FC  FF04030C 05180728                 3776           DC    XL16'FF04030C05180728 093C0B540D700F90'   result
00005704  093C0B54 0D700F90
0000570C  FF020304 05060708                 3777           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005714  090A0B0C 0D0E0F10
0000571C  FF010102 02030304                 3778           DC    XL16'FF01010202030304 0405050606070708'   v3
00005724  04050506 06070708
0000572C  FF020304 05060708                 3779           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005734  090A0B0C 0D0E0F10
                                            3780
                                            3781           VRR_D VMAO,0
00005740                                    3782+          DS    0FD
00005740                        00005740    3783+          USING *,R5                base for test data and test routine
00005740  00005788                          3784+T95       DC    A(X95)              address of test routine
00005744  005F                              3785+          DC    H'95'               test number
00005746  00                                3786+          DC    X'00'
00005747  00                                3787+          DC    HL1'0'              m5
00005748  E5D4C1D6 40404040                 3788+          DC    CL8'VMAO'           instruction name
00005750  000057CC                          3789+          DC    A(RE95+16)          address of v2 source
00005754  000057DC                          3790+          DC    A(RE95+32)          address of v3 source
00005758  000057EC                          3791+          DC    A(RE95+48)          address of v4 source
0000575C  00000010                          3792+          DC    A(16)               result length
00005760  000057BC                          3793+REA95     DC    A(RE95)             result address
00005768  00000000 00000000                 3794+          DS    FD                  gap
00005770  00000000 00000000                 3795+V1O95     DS    XL16                V1 output
00005778  00000000 00000000
00005780  00000000 00000000                 3796+          DS    FD                  gap
                                            3797+*
00005788                                    3798+X95       DS    0F
00005788  E310 5010 0014              00000010  3799+      LGF   R1,V2ADDR           load v2 source
0000578E  E761 0000 0806              00000000  3800+      VL    v22,0(R1)           use v22 to test decoder
00005794  E310 5014 0014              00000014  3801+      LGF   R1,V3ADDR           load v3 source
0000579A  E771 0000 0806              00000000  3802+      VL    v23,0(R1)           use v23 to test decoder
000057A0  E310 5018 0014              00000018  3803+      LGF   R1,V4ADDR           load v4 source
000057A6  E781 0000 0806              00000000  3804+      VL    v24,0(R1)           use v24 to test decoder
000057AC  E766 7000 8FAF                        3805+      VMAO  V22,V22,V23,V24,0     test instruction (dest is a source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000057B2  E760 5030 080E                 00005770  3806+          VST   V22,V1O95          save v1 output
000057B8  07FB                                     3807+          BR    R11               return
000057BC                                           3808+RE95      DC    0F                xl16 expected result
000057BC                                           3809+          DROP  R5
000057BC  FF020304 05060710                        3810           DC    XL16'FF02030405060710 09140B180D1C0F30'   result
000057C4  09140B18 0D1C0F30
000057CC  FF020304 05060708                        3811           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
000057D4  090A0B0C 0D0E0F10
000057DC  FF000000 00000001                        3812           DC    XL16'FF00000000000001 0101010101010102'   v3
000057E4  01010101 01010102
000057EC  FF020304 05060708                        3813           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
000057F4  090A0B0C 0D0E0F10
                                                   3814
                                                   3815 * Halfword
                                                   3816           VRR_D VMAO,1
00005800                                           3817+          DS    0FD
00005800                           00005800        3818+          USING *,R5              base for test data and test routine
00005800  00005848                                 3819+T96       DC    A(X96)            address of test routine
00005804  0060                                     3820+          DC    H'96'             test number
00005806  00                                       3821+          DC    X'00'
00005807  01                                       3822+          DC    HL1'1'            m5
00005808  E5D4C1D6 40404040                       3823+          DC    CL8'VMAO'         instruction name
00005810  0000588C                                 3824+          DC    A(RE96+16)        address of v2 source
00005814  0000589C                                 3825+          DC    A(RE96+32)        address of v3 source
00005818  000058AC                                 3826+          DC    A(RE96+48)        address of v4 source
0000581C  00000010                                 3827+          DC    A(16)             result length
00005820  0000587C                                 3828+REA96     DC    A(RE96)           result address
00005828  00000000 00000000                        3829+          DS    FD                gap
00005830  00000000 00000000                        3830+V1O96     DS    XL16              V1 output
00005838  00000000 00000000
00005840  00000000 00000000                        3831+          DS    FD                gap
                                                   3832+*
00005848                                           3833+X96       DS    0F
00005848  E310 5010 0014                 00000010  3834+          LGF   R1,V2ADDR         load v2 source
0000584E  E761 0000 0806                 00000000  3835+          VL    v22,0(R1)         use v22 to test decoder
00005854  E310 5014 0014                 00000014  3836+          LGF   R1,V3ADDR         load v3 source
0000585A  E771 0000 0806                 00000000  3837+          VL    v23,0(R1)         use v23 to test decoder
00005860  E310 5018 0014                 00000018  3838+          LGF   R1,V4ADDR         load v4 source
00005866  E781 0000 0806                 00000000  3839+          VL    v24,0(R1)         use v24 to test decoder
0000586C  E766 7100 8FAF                           3840+          VMAO  V22,V22,V23,V24,1    test instruction (dest is a source)
00005872  E760 5030 080E                 00005830  3841+          VST   V22,V1O96          save v1 output
00005878  07FB                                     3842+          BR    R11               return
0000587C                                           3843+RE96      DC    0F                xl16 expected result
0000587C                                           3844+          DROP  R5
0000587C  00000000 00000271                        3845           DC    XL16'0000000000000271 00000C400000F424'   result
00005884  00000C40 0000F424
0000588C  FF000000 00000019                        3846           DC    XL16'FF00000000000019 00000038000000FA'   v2
00005894  00000038 000000FA
0000589C  FF000000 00000019                        3847           DC    XL16'FF00000000000019 00000038000000FA'   v3
000058A4  00000038 000000FA
000058AC  00000000 00000000                        3848           DC    XL16'0000000000000000 0000000000000000'   v4
000058B4  00000000 00000000
                                                   3849
                                                   3850           VRR_D VMAO,1
000058C0                                           3851+          DS    0FD
000058C0                           000058C0        3852+          USING *,R5              base for test data and test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000058C0  00005908                             3853+T97      DC    A(X97)            address of test routine
000058C4  0061                                 3854+         DC    H'97'             test number
000058C6  00                                   3855+         DC    X'00'
000058C7  01                                   3856+         DC    HL1'1'            m5
000058C8  E5D4C1D6 40404040                    3857+         DC    CL8'VMAO'         instruction name
000058D0  0000594C                             3858+         DC    A(RE97+16)        address of v2 source
000058D4  0000595C                             3859+         DC    A(RE97+32)        address of v3 source
000058D8  0000596C                             3860+         DC    A(RE97+48)        address of v4 source
000058DC  00000010                             3861+         DC    A(16)             result length
000058E0  0000593C                             3862+REA97    DC    A(RE97)           result address
000058E8  00000000 00000000                    3863+         DS    FD                gap
000058F0  00000000 00000000                    3864+V1O97    DS    XL16              V1 output
000058F8  00000000 00000000
00005900  00000000 00000000                    3865+         DS    FD                gap
                                               3866+*
00005908                                       3867+X97      DS    0F
00005908  E310 5010 0014              00000010 3868+         LGF   R1,V2ADDR         load v2 source
0000590E  E761 0000 0806              00000000 3869+         VL    v22,0(R1)         use v22 to test decoder
00005914  E310 5014 0014              00000014 3870+         LGF   R1,V3ADDR         load v3 source
0000591A  E771 0000 0806              00000000 3871+         VL    v23,0(R1)         use v23 to test decoder
00005920  E310 5018 0014              00000018 3872+         LGF   R1,V4ADDR         load v4 source
00005926  E781 0000 0806              00000000 3873+         VL    v24,0(R1)         use v24 to test decoder
0000592C  E766 7100 8FAF                       3874+         VMAO  V22,V22,V23,V24,1    test instruction (dest is a source)
00005932  E760 5030 080E              000058F0 3875+         VST   V22,V1O97          save v1 output
00005938  07FB                                 3876+         BR    R11               return
0000593C                                       3877+RE97     DC    0F                xl16 expected result
0000593C                                       3878+         DROP  R5
0000593C  00020100 000006C0                    3879          DC    XL16'00020100000006C0 00000C430000F426'   result
00005944  00000C43 0000F426
0000594C  FF0000FF 00000029                    3880          DC    XL16'FF0000FF00000029 0000003800000FA'    v2
00005954  00000038 000000FA
0000595C  FF000001 00000029                    3881          DC    XL16'FF00000100000029 0000003800000FA'    v3
00005964  00000038 000000FA
0000596C  00020001 0000002F                    3882          DC    XL16'000200010000002F 0000000300000002'   v4
00005974  00000003 00000002
                                               3883
                                               3884          VRR_D VMAO,1
00005980                                       3885+         DS    0FD
00005980                       00005980        3886+         USING *,R5              base for test data and test routine
00005980  000059C8                             3887+T98      DC    A(X98)            address of test routine
00005984  0062                                 3888+         DC    H'98'             test number
00005986  00                                   3889+         DC    X'00'
00005987  01                                   3890+         DC    HL1'1'            m5
00005988  E5D4C1D6 40404040                    3891+         DC    CL8'VMAO'         instruction name
00005990  00005A0C                             3892+         DC    A(RE98+16)        address of v2 source
00005994  00005A1C                             3893+         DC    A(RE98+32)        address of v3 source
00005998  00005A2C                             3894+         DC    A(RE98+48)        address of v4 source
0000599C  00000010                             3895+         DC    A(16)             result length
000059A0  000059FC                             3896+REA98    DC    A(RE98)           result address
000059A8  00000000 00000000                    3897+         DS    FD                gap
000059B0  00000000 00000000                    3898+V1O98    DS    XL16              V1 output
000059B8  00000000 00000000
000059C0  00000000 00000000                    3899+         DS    FD                gap
                                               3900+*
000059C8                                       3901+X98      DS    0F
000059C8  E310 5010 0014              00000010 3902+         LGF   R1,V2ADDR         load v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000059CE  E761 0000 0806                 00000000  3903+         VL    v22,0(R1)          use v22 to test decoder
000059D4  E310 5014 0014                 00000014  3904+         LGF   R1,V3ADDR          load v3 source
000059DA  E771 0000 0806                 00000000  3905+         VL    v23,0(R1)          use v23 to test decoder
000059E0  E310 5018 0014                 00000018  3906+         LGF   R1,V4ADDR          load v4 source
000059E6  E781 0000 0806                 00000000  3907+         VL    v24,0(R1)          use v24 to test decoder
000059EC  E766 7100 8FAF                           3908+         VMAO  V22,V22,V23,V24,1    test instruction (dest is a source)
000059F2  E760 5030 080E                 000059B0  3909+         VST   V22,V1O98           save v1 output
000059F8  07FB                                     3910+         BR    R11                return
000059FC                                           3911+RE98     DC    0F                 xl16 expected result
000059FC                                           3912+         DROP  R5
000059FC  FF0B1B14 05377748                        3913          DC    XL16'FF0B1B1405377748 0984139C0DF0F010'   result
00005A04  0984139C 0DF0F010
00005A0C  FF020304 05060708                        3914          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005A14  090A0B0C 0D0E0F10
00005A1C  FF020304 05060708                        3915          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00005A24  090A0B0C 0D0E0F10
00005A2C  FF020304 05060708                        3916          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005A34  090A0B0C 0D0E0F10
                                                   3917
                                                   3918          VRR_D VMAO,1
00005A40                                           3919+         DS    0FD
00005A40                 00005A40                  3920+         USING *,R5               base for test data and test routine
00005A40  00005A88                                 3921+T99      DC    A(X99)             address of test routine
00005A44  0063                                     3922+         DC    H'99'              test number
00005A46  00                                       3923+         DC    X'00'
00005A47  01                                       3924+         DC    HL1'1'             m5
00005A48  E5D4C1D6 40404040                        3925+         DC    CL8'VMAO'          instruction name
00005A50  00005ACC                                 3926+         DC    A(RE99+16)         address of v2 source
00005A54  00005ADC                                 3927+         DC    A(RE99+32)         address of v3 source
00005A58  00005AEC                                 3928+         DC    A(RE99+48)         address of v4 source
00005A5C  00000010                                 3929+         DC    A(16)              result length
00005A60  00005ABC                                 3930+REA99    DC    A(RE99)            result address
00005A68  00000000 00000000                        3931+         DS    FD                 gap
00005A70  00000000 00000000                        3932+V1O99    DS    XL16               V1 output
00005A78  00000000 00000000
00005A80  00000000 00000000                        3933+         DS    FD                 gap
                                                   3934+*
00005A88                                           3935+X99      DS    0F
00005A88  E310 5010 0014                 00000010  3936+         LGF   R1,V2ADDR          load v2 source
00005A8E  E761 0000 0806                 00000000  3937+         VL    v22,0(R1)          use v22 to test decoder
00005A94  E310 5014 0014                 00000014  3938+         LGF   R1,V3ADDR          load v3 source
00005A9A  E771 0000 0806                 00000000  3939+         VL    v23,0(R1)          use v23 to test decoder
00005AA0  E310 5018 0014                 00000018  3940+         LGF   R1,V4ADDR          load v4 source
00005AA6  E781 0000 0806                 00000000  3941+         VL    v24,0(R1)          use v24 to test decoder
00005AAC  E766 7100 8FAF                           3942+         VMAO  V22,V22,V23,V24,1    test instruction (dest is a source)
00005AB2  E760 5030 080E                 00005A70  3943+         VST   V22,V1O99           save v1 output
00005AB8  07FB                                     3944+         BR    R11                return
00005ABC                                           3945+RE99     DC    0F                 xl16 expected result
00005ABC                                           3946+         DROP  R5
00005ABC  FF050D0C 051B3B28                        3947          DC    XL16'FF050D0C051B3B28 094189540D77F790'   result
00005AC4  09418954 0D77F790
00005ACC  FF020304 05060708                        3948          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005AD4  090A0B0C 0D0E0F10
00005ADC  FF010102 02030304                        3949          DC    XL16'FF01010202030304 0405050606070708'   v3
00005AE4  04050506 06070708
00005AEC  FF020304 05060708                        3950          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00005AF4  090A0B0C 0D0E0F10                          3951
                                                     3952          VRR_D VMAO,1
00005B00                                             3953+         DS    0FD
00005B00                       00005B00              3954+         USING *,R5              base for test data and test routine
00005B00  00005B48                                   3955+T100     DC    A(X100)           address of test routine
00005B04  0064                                       3956+         DC    H'100'            test number
00005B06  00                                         3957+         DC    X'00'
00005B07  01                                         3958+         DC    HL1'1'            m5
00005B08  E5D4C1D6 40404040                          3959+         DC    CL8'VMAO'         instruction name
00005B10  00005B8C                                   3960+         DC    A(RE100+16)       address of v2 source
00005B14  00005B9C                                   3961+         DC    A(RE100+32)       address of v3 source
00005B18  00005BAC                                   3962+         DC    A(RE100+48)       address of v4 source
00005B1C  00000010                                   3963+         DC    A(16)             result length
00005B20  00005B7C                                   3964+REA100   DC    A(RE100)          result address
00005B28  00000000 00000000                          3965+         DS    FD                gap
00005B30  00000000 00000000                          3966+V1O100   DS    XL16              V1 output
00005B38  00000000 00000000
00005B40  00000000 00000000                          3967+         DS    FD                gap
                                                     3968+*
00005B48                                             3969+X100     DS    0F
00005B48  E310 5010 0014                 00000010    3970+         LGF   R1,V2ADDR         load v2 source
00005B4E  E761 0000 0806                 00000000    3971+         VL    v22,0(R1)         use v22 to test decoder
00005B54  E310 5014 0014                 00000014    3972+         LGF   R1,V3ADDR         load v3 source
00005B5A  E771 0000 0806                 00000000    3973+         VL    v23,0(R1)         use v23 to test decoder
00005B60  E310 5018 0014                 00000018    3974+         LGF   R1,V4ADDR         load v4 source
00005B66  E781 0000 0806                 00000000    3975+         VL    v24,0(R1)         use v24 to test decoder
00005B6C  E766 7100 8FAF                             3976+         VMAO  V22,V22,V23,V24,1    test instruction (dest is a source)
00005B72  E760 5030 080E                 00005B30    3977+         VST   V22,V1O100         save v1 output
00005B78  07FB                                       3978+         BR    R11               return
00005B7C                                             3979+RE100    DC    0F                xl16 expected result
00005B7C                                             3980+         DROP  R5
00005B7C  FF020304 05060E10                          3981          DC    XL16'FF02030405060E10 091522180D1D3D30'   result
00005B84  09152218 0D1D3D30
00005B8C  FF020304 05060708                          3982          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005B94  090A0B0C 0D0E0F10
00005B9C  FF000000 00000001                          3983          DC    XL16'FF00000000000001 0101010101010102'   v3
00005BA4  01010101 01010102
00005BAC  FF020304 05060708                          3984          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005BB4  090A0B0C 0D0E0F10
                                                     3985
                                                     3986 * Word
                                                     3987          VRR_D VMAO,2
00005BC0                                             3988+         DS    0FD
00005BC0                       00005BC0              3989+         USING *,R5              base for test data and test routine
00005BC0  00005C08                                   3990+T101     DC    A(X101)           address of test routine
00005BC4  0065                                       3991+         DC    H'101'            test number
00005BC6  00                                         3992+         DC    X'00'
00005BC7  02                                         3993+         DC    HL1'2'            m5
00005BC8  E5D4C1D6 40404040                          3994+         DC    CL8'VMAO'         instruction name
00005BD0  00005C4C                                   3995+         DC    A(RE101+16)       address of v2 source
00005BD4  00005C5C                                   3996+         DC    A(RE101+32)       address of v3 source
00005BD8  00005C6C                                   3997+         DC    A(RE101+48)       address of v4 source
00005BDC  00000010                                   3998+         DC    A(16)             result length
00005BE0  00005C3C                                   3999+REA101   DC    A(RE101)          result address
00005BE8  00000000 00000000                          4000+         DS    FD                gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00005BF0  00000000 00000000                      4001+V1O101   DS    XL16              V1 output
00005BF8  00000000 00000000
00005C00  00000000 00000000                      4002+         DS    FD                gap
                                                 4003+*
00005C08                                         4004+X101     DS    0F
00005C08  E310 5010 0014                00000010 4005+         LGF   R1,V2ADDR         load v2 source
00005C0E  E761 0000 0806                00000000 4006+         VL    v22,0(R1)         use v22 to test decoder
00005C14  E310 5014 0014                00000014 4007+         LGF   R1,V3ADDR         load v3 source
00005C1A  E771 0000 0806                00000000 4008+         VL    v23,0(R1)         use v23 to test decoder
00005C20  E310 5018 0014                00000018 4009+         LGF   R1,V4ADDR         load v4 source
00005C26  E781 0000 0806                00000000 4010+         VL    v24,0(R1)         use v24 to test decoder
00005C2C  E766 7200 8FAF                         4011+         VMAO  V22,V22,V23,V24,2    test instruction (dest is a source)
00005C32  E760 5030 080E                00005BF0 4012+         VST   V22,V1O101         save v1 output
00005C38  07FB                                   4013+         BR    R11               return
00005C3C                                         4014+RE101    DC    0F                xl16 expected result
00005C3C                                         4015+         DROP  R5
00005C3C  00000000 00000271                      4016          DC    XL16'0000000000000271 000000000000F424'   result
00005C44  00000000 0000F424
00005C4C  FF000000 00000019                      4017          DC    XL16'FF00000000000019 00000038000000FA'   v2
00005C54  00000038 000000FA
00005C5C  FF000000 00000019                      4018          DC    XL16'FF00000000000019 00000038000000FA'   v3
00005C64  00000038 000000FA
00005C6C  00000000 00000000                      4019          DC    XL16'0000000000000000 0000000000000000'   v4
00005C74  00000000 00000000
                                                 4020
                                                 4021          VRR_D VMAO,2
00005C80                                         4022+         DS    0FD
00005C80                        00005C80         4023+         USING *,R5              base for test data and test routine
00005C80  00005CC8                               4024+T102     DC    A(X102)           address of test routine
00005C84  0066                                   4025+         DC    H'102'            test number
00005C86  00                                     4026+         DC    X'00'
00005C87  02                                     4027+         DC    HL1'2'            m5
00005C88  E5D4C1D6 40404040                      4028+         DC    CL8'VMAO'         instruction name
00005C90  00005D0C                               4029+         DC    A(RE102+16)       address of v2 source
00005C94  00005D1C                               4030+         DC    A(RE102+32)       address of v3 source
00005C98  00005D2C                               4031+         DC    A(RE102+48)       address of v4 source
00005C9C  00000010                               4032+         DC    A(16)             result length
00005CA0  00005CFC                               4033+REA102   DC    A(RE102)          result address
00005CA8  00000000 00000000                      4034+         DS    FD                gap
00005CB0  00000000 00000000                      4035+V1O102   DS    XL16              V1 output
00005CB8  00000000 00000000
00005CC0  00000000 00000000                      4036+         DS    FD                gap
                                                 4037+*
00005CC8                                         4038+X102     DS    0F
00005CC8  E310 5010 0014                00000010 4039+         LGF   R1,V2ADDR         load v2 source
00005CCE  E761 0000 0806                00000000 4040+         VL    v22,0(R1)         use v22 to test decoder
00005CD4  E310 5014 0014                00000014 4041+         LGF   R1,V3ADDR         load v3 source
00005CDA  E771 0000 0806                00000000 4042+         VL    v23,0(R1)         use v23 to test decoder
00005CE0  E310 5018 0014                00000018 4043+         LGF   R1,V4ADDR         load v4 source
00005CE6  E781 0000 0806                00000000 4044+         VL    v24,0(R1)         use v24 to test decoder
00005CEC  E766 7200 8FAF                         4045+         VMAO  V22,V22,V23,V24,2    test instruction (dest is a source)
00005CF2  E760 5030 080E                00005CB0 4046+         VST   V22,V1O102         save v1 output
00005CF8  07FB                                   4047+         BR    R11               return
00005CFC                                         4048+RE102    DC    0F                xl16 expected result
00005CFC                                         4049+         DROP  R5
00005CFC  00020001 000006C0                      4050          DC    XL16'00020001000006C0 000000030000F426'   result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00005D04  00000003 0000F426
00005D0C  FF0000FF 00000029                        4051          DC    XL16'FF0000FF00000029 00000038000000FA'   v2
00005D14  00000038 000000FA
00005D1C  FF000001 00000029                        4052          DC    XL16'FF00000100000029 00000038000000FA'   v3
00005D24  00000038 000000FA
00005D2C  00020001 0000002F                        4053          DC    XL16'00020001000002F 0000000300000002'   v4
00005D34  00000003 00000002
                                                   4054
                                                   4055          VRR_D VMAO,2
00005D40                                           4056+         DS    0FD
00005D40                     00005D40              4057+         USING *,R5              base for test data and test routine
00005D40  00005D88                                 4058+T103     DC    A(X103)           address of test routine
00005D44  0067                                     4059+         DC    H'103'            test number
00005D46  00                                       4060+         DC    X'00'
00005D47  02                                       4061+         DC    HL1'2'            m5
00005D48  E5D4C1D6 40404040                        4062+         DC    CL8'VMAO'         instruction name
00005D50  00005DCC                                 4063+         DC    A(RE103+16)       address of v2 source
00005D54  00005DDC                                 4064+         DC    A(RE103+32)       address of v3 source
00005D58  00005DEC                                 4065+         DC    A(RE103+48)       address of v4 source
00005D5C  00000010                                 4066+         DC    A(16)             result length
00005D60  00005DBC                                 4067+REA103   DC    A(RE103)          result address
00005D68  00000000 00000000                        4068+         DS    FD                gap
00005D70  00000000 00000000                        4069+V1O103   DS    XL16              V1 output
00005D78  00000000 00000000
00005D80  00000000 00000000                        4070+         DS    FD                gap
                                                   4071+*
00005D88                                           4072+X103     DS    0F
00005D88  E310 5010 0014                 00000010  4073+         LGF   R1,V2ADDR         load v2 source
00005D8E  E761 0000 0806                 00000000  4074+         VL    v22,0(R1)         use v22 to test decoder
00005D94  E310 5014 0014                 00000014  4075+         LGF   R1,V3ADDR         load v3 source
00005D9A  E771 0000 0806                 00000000  4076+         VL    v23,0(R1)         use v23 to test decoder
00005DA0  E310 5018 0014                 00000018  4077+         LGF   R1,V4ADDR         load v4 source
00005DA6  E781 0000 0806                 00000000  4078+         VL    v24,0(R1)         use v24 to test decoder
00005DAC  E766 7200 8FAF                           4079+         VMAO  V22,V22,V23,V24,2    test instruction (dest is a source)
00005DB2  E760 5030 080E                 00005D70  4080+         VST   V22,V1O103         save v1 output
00005DB8  07FB                                     4081+         BR    R11               return
00005DBC                                           4082+RE103    DC    0F                xl16 expected result
00005DBC                                           4083+         DROP  R5
00005DBC  FF1B3F6E A9977748                        4084          DC    XL16'FF1B3F6EA9977748 09B4795953B0F010'   result
00005DC4  09B47959 53B0F010
00005DCC  FF020304 05060708                        4085          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005DD4  090A0B0C 0D0E0F10
00005DDC  FF020304 05060708                        4086          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00005DE4  090A0B0C 0D0E0F10
00005DEC  FF020304 05060708                        4087          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005DF4  090A0B0C 0D0E0F10
                                                   4088
                                                   4089          VRR_D VMAO,2
00005E00                                           4090+         DS    0FD
00005E00                     00005E00              4091+         USING *,R5              base for test data and test routine
00005E00  00005E48                                 4092+T104     DC    A(X104)           address of test routine
00005E04  0068                                     4093+         DC    H'104'            test number
00005E06  00                                       4094+         DC    X'00'
00005E07  02                                       4095+         DC    HL1'2'            m5
00005E08  E5D4C1D6 40404040                        4096+         DC    CL8'VMAO'         instruction name
00005E10  00005E8C                                 4097+         DC    A(RE104+16)       address of v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00005E14  00005E9C                        4098+          DC    A(RE104+32)       address of v3 source
00005E18  00005EAC                        4099+          DC    A(RE104+48)       address of v4 source
00005E1C  00000010                        4100+          DC    A(16)             result length
00005E20  00005E7C                        4101+REA104    DC    A(RE104)          result address
00005E28  00000000 00000000               4102+          DS    FD                gap
00005E30  00000000 00000000               4103+V1O104    DS    XL16              V1 output
00005E38  00000000 00000000
00005E40  00000000 00000000               4104+          DS    FD                gap
                                          4105+*
00005E48                                  4106+X104      DS    0F
00005E48  E310 5010 0014          00000010 4107+          LGF   R1,V2ADDR         load v2 source
00005E4E  E761 0000 0806          00000000 4108+          VL    v22,0(R1)         use v22 to test decoder
00005E54  E310 5014 0014          00000014 4109+          LGF   R1,V3ADDR         load v3 source
00005E5A  E771 0000 0806          00000000 4110+          VL    v23,0(R1)         use v23 to test decoder
00005E60  E310 5018 0014          00000018 4111+          LGF   R1,V4ADDR         load v4 source
00005E66  E781 0000 0806          00000000 4112+          VL    v24,0(R1)         use v24 to test decoder
00005E6C  E766 7200 8FAF                   4113+          VMAO  V22,V22,V23,V24,2    test instruction (dest is a source)
00005E72  E760 5030 080E          00005E30 4114+          VST   V22,V1O104         save v1 output
00005E78  07FB                             4115+          BR    R11               return
00005E7C                                   4116+RE104     DC    0F                xl16 expected result
00005E7C                                   4117+          DROP  R5
00005E7C  FF0C1E33 504B3B28                4118           DC    XL16'FF0C1E33504B3B28 0958BB24A157F790'   result
00005E84  0958BB24 A157F790
00005E8C  FF020304 05060708                4119           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005E94  090A0B0C 0D0E0F10
00005E9C  FF010102 02030304                4120           DC    XL16'FF01010202030304 0405050606070708'   v3
00005EA4  04050506 06070708
00005EAC  FF020304 05060708                4121           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005EB4  090A0B0C 0D0E0F10
                                           4122
                                           4123           VRR_D VMAO,2
00005EC0                                   4124+          DS    0FD
00005EC0                        00005EC0   4125+          USING *,R5              base for test data and test routine
00005EC0  00005F08                         4126+T105      DC    A(X105)           address of test routine
00005EC4  0069                             4127+          DC    H'105'            test number
00005EC6  00                               4128+          DC    X'00'
00005EC7  02                               4129+          DC    HL1'2'            m5
00005EC8  E5D4C1D6 40404040                4130+          DC    CL8'VMAO'         instruction name
00005ED0  00005F4C                         4131+          DC    A(RE105+16)       address of v2 source
00005ED4  00005F5C                         4132+          DC    A(RE105+32)       address of v3 source
00005ED8  00005F6C                         4133+          DC    A(RE105+48)       address of v4 source
00005EDC  00000010                         4134+          DC    A(16)             result length
00005EE0  00005F3C                         4135+REA105    DC    A(RE105)          result address
00005EE8  00000000 00000000                4136+          DS    FD                gap
00005EF0  00000000 00000000                4137+V1O105    DS    XL16              V1 output
00005EF8  00000000 00000000
00005F00  00000000 00000000                4138+          DS    FD                gap
                                           4139+*
00005F08                                   4140+X105      DS    0F
00005F08  E310 5010 0014          00000010 4141+          LGF   R1,V2ADDR         load v2 source
00005F0E  E761 0000 0806          00000000 4142+          VL    v22,0(R1)         use v22 to test decoder
00005F14  E310 5014 0014          00000014 4143+          LGF   R1,V3ADDR         load v3 source
00005F1A  E771 0000 0806          00000000 4144+          VL    v23,0(R1)         use v23 to test decoder
00005F20  E310 5018 0014          00000018 4145+          LGF   R1,V4ADDR         load v4 source
00005F26  E781 0000 0806          00000000 4146+          VL    v24,0(R1)         use v24 to test decoder
00005F2C  E766 7200 8FAF                   4147+          VMAO  V22,V22,V23,V24,2    test instruction (dest is a source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
00005F32  E760 5030 080E                 00005EF0  4148+          VST   V22,V1O105         save v1 output
00005F38  07FB                                     4149+          BR    R11               return
00005F3C                                           4150+RE105     DC    0F                xl16 expected result
00005F3C                                           4151+          DROP  R5
00005F3C  FF020304 0A0C0E10                        4152           DC    XL16'FF0203040A0C0E10 0917263654493D30'   result
00005F44  09172636 54493D30
00005F4C  FF020304 05060708                        4153           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00005F54  090A0B0C 0D0E0F10
00005F5C  FF000000 00000001                        4154           DC    XL16'FF00000000000001 0101010101010102'   v3
00005F64  01010101 01010102
00005F6C  FF020304 05060708                        4155           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v4
00005F74  090A0B0C 0D0E0F10
                                                   4156
                                                   4157
00005F7C  00000000                                 4158           DC    F'0'     END OF TABLE
00005F80  00000000                                 4159           DC    F'0'
                                                   4160 *
                                                   4161 * table of pointers to individual load test
                                                   4162 *
00005F84                                           4163 E7TESTS   DS    0F
                                                   4164           PTTABLE
00005F84                                           4165+TTABLE    DS    0F
00005F84  000010C0                                 4166+          DC    A(T1)
00005F88  00001180                                 4167+          DC    A(T2)
00005F8C  00001240                                 4168+          DC    A(T3)
00005F90  00001300                                 4169+          DC    A(T4)
00005F94  000013C0                                 4170+          DC    A(T5)
00005F98  00001480                                 4171+          DC    A(T6)
00005F9C  00001540                                 4172+          DC    A(T7)
00005FA0  00001600                                 4173+          DC    A(T8)
00005FA4  000016C0                                 4174+          DC    A(T9)
00005FA8  00001780                                 4175+          DC    A(T10)
00005FAC  00001840                                 4176+          DC    A(T11)
00005FB0  00001900                                 4177+          DC    A(T12)
00005FB4  000019C0                                 4178+          DC    A(T13)
00005FB8  00001A80                                 4179+          DC    A(T14)
00005FBC  00001B40                                 4180+          DC    A(T15)
00005FC0  00001C00                                 4181+          DC    A(T16)
00005FC4  00001CC0                                 4182+          DC    A(T17)
00005FC8  00001D80                                 4183+          DC    A(T18)
00005FCC  00001E40                                 4184+          DC    A(T19)
00005FD0  00001F00                                 4185+          DC    A(T20)
00005FD4  00001FC0                                 4186+          DC    A(T21)
00005FD8  00002080                                 4187+          DC    A(T22)
00005FDC  00002140                                 4188+          DC    A(T23)
00005FE0  00002200                                 4189+          DC    A(T24)
00005FE4  000022C0                                 4190+          DC    A(T25)
00005FE8  00002380                                 4191+          DC    A(T26)
00005FEC  00002440                                 4192+          DC    A(T27)
00005FF0  00002500                                 4193+          DC    A(T28)
00005FF4  000025C0                                 4194+          DC    A(T29)
00005FF8  00002680                                 4195+          DC    A(T30)
00005FFC  00002740                                 4196+          DC    A(T31)
00006000  00002800                                 4197+          DC    A(T32)
00006004  000028C0                                 4198+          DC    A(T33)
00006008  00002980                                 4199+          DC    A(T34)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000600C  00002A40                             4200+          DC    A(T35)
00006010  00002B00                             4201+          DC    A(T36)
00006014  00002BC0                             4202+          DC    A(T37)
00006018  00002C80                             4203+          DC    A(T38)
0000601C  00002D40                             4204+          DC    A(T39)
00006020  00002E00                             4205+          DC    A(T40)
00006024  00002EC0                             4206+          DC    A(T41)
00006028  00002F80                             4207+          DC    A(T42)
0000602C  00003040                             4208+          DC    A(T43)
00006030  00003100                             4209+          DC    A(T44)
00006034  000031C0                             4210+          DC    A(T45)
00006038  00003280                             4211+          DC    A(T46)
0000603C  00003340                             4212+          DC    A(T47)
00006040  00003400                             4213+          DC    A(T48)
00006044  000034C0                             4214+          DC    A(T49)
00006048  00003580                             4215+          DC    A(T50)
0000604C  00003640                             4216+          DC    A(T51)
00006050  00003700                             4217+          DC    A(T52)
00006054  000037C0                             4218+          DC    A(T53)
00006058  00003880                             4219+          DC    A(T54)
0000605C  00003940                             4220+          DC    A(T55)
00006060  00003A00                             4221+          DC    A(T56)
00006064  00003AC0                             4222+          DC    A(T57)
00006068  00003B80                             4223+          DC    A(T58)
0000606C  00003C40                             4224+          DC    A(T59)
00006070  00003D00                             4225+          DC    A(T60)
00006074  00003DC0                             4226+          DC    A(T61)
00006078  00003E80                             4227+          DC    A(T62)
0000607C  00003F40                             4228+          DC    A(T63)
00006080  00004000                             4229+          DC    A(T64)
00006084  000040C0                             4230+          DC    A(T65)
00006088  00004180                             4231+          DC    A(T66)
0000608C  00004240                             4232+          DC    A(T67)
00006090  00004300                             4233+          DC    A(T68)
00006094  000043C0                             4234+          DC    A(T69)
00006098  00004480                             4235+          DC    A(T70)
0000609C  00004540                             4236+          DC    A(T71)
000060A0  00004600                             4237+          DC    A(T72)
000060A4  000046C0                             4238+          DC    A(T73)
000060A8  00004780                             4239+          DC    A(T74)
000060AC  00004840                             4240+          DC    A(T75)
000060B0  00004900                             4241+          DC    A(T76)
000060B4  000049C0                             4242+          DC    A(T77)
000060B8  00004A80                             4243+          DC    A(T78)
000060BC  00004B40                             4244+          DC    A(T79)
000060C0  00004C00                             4245+          DC    A(T80)
000060C4  00004CC0                             4246+          DC    A(T81)
000060C8  00004D80                             4247+          DC    A(T82)
000060CC  00004E40                             4248+          DC    A(T83)
000060D0  00004F00                             4249+          DC    A(T84)
000060D4  00004FC0                             4250+          DC    A(T85)
000060D8  00005080                             4251+          DC    A(T86)
000060DC  00005140                             4252+          DC    A(T87)
000060E0  00005200                             4253+          DC    A(T88)
000060E4  000052C0                             4254+          DC    A(T89)
000060E8  00005380                             4255+          DC    A(T90)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000060EC  00005440                             4256+          DC    A(T91)
000060F0  00005500                             4257+          DC    A(T92)
000060F4  000055C0                             4258+          DC    A(T93)
000060F8  00005680                             4259+          DC    A(T94)
000060FC  00005740                             4260+          DC    A(T95)
00006100  00005800                             4261+          DC    A(T96)
00006104  000058C0                             4262+          DC    A(T97)
00006108  00005980                             4263+          DC    A(T98)
0000610C  00005A40                             4264+          DC    A(T99)
00006110  00005B00                             4265+          DC    A(T100)
00006114  00005BC0                             4266+          DC    A(T101)
00006118  00005C80                             4267+          DC    A(T102)
0000611C  00005D40                             4268+          DC    A(T103)
00006120  00005E00                             4269+          DC    A(T104)
00006124  00005EC0                             4270+          DC    A(T105)
                                               4271+*
00006128  00000000                             4272+          DC    A(0)              END OF TABLE
0000612C  00000000                             4273+          DC    A(0)
                                               4274
00006130  00000000                             4275           DC    F'0'     END OF TABLE
00006134  00000000                             4276           DC    F'0'
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                    4278 ********************************************************************************
                                                    4279 *        Register equates
                                                    4280 ********************************************************************************


                                00000000  00000001  4282 R0       EQU   0
                                00000001  00000001  4283 R1       EQU   1
                                00000002  00000001  4284 R2       EQU   2
                                00000003  00000001  4285 R3       EQU   3
                                00000004  00000001  4286 R4       EQU   4
                                00000005  00000001  4287 R5       EQU   5
                                00000006  00000001  4288 R6       EQU   6
                                00000007  00000001  4289 R7       EQU   7
                                00000008  00000001  4290 R8       EQU   8
                                00000009  00000001  4291 R9       EQU   9
                                0000000A  00000001  4292 R10      EQU   10
                                0000000B  00000001  4293 R11      EQU   11
                                0000000C  00000001  4294 R12      EQU   12
                                0000000D  00000001  4295 R13      EQU   13
                                0000000E  00000001  4296 R14      EQU   14
                                0000000F  00000001  4297 R15      EQU   15


                                                    4299 ********************************************************************************
                                                    4300 *        Register equates
                                                    4301 ********************************************************************************


                              00000000  00000001  4303 V0       EQU   0
                              00000001  00000001  4304 V1       EQU   1
                              00000002  00000001  4305 V2       EQU   2
                              00000003  00000001  4306 V3       EQU   3
                              00000004  00000001  4307 V4       EQU   4
                              00000005  00000001  4308 V5       EQU   5
                              00000006  00000001  4309 V6       EQU   6
                              00000007  00000001  4310 V7       EQU   7
                              00000008  00000001  4311 V8       EQU   8
                              00000009  00000001  4312 V9       EQU   9
                              0000000A  00000001  4313 V10      EQU   10
                              0000000B  00000001  4314 V11      EQU   11
                              0000000C  00000001  4315 V12      EQU   12
                              0000000D  00000001  4316 V13      EQU   13
                              0000000E  00000001  4317 V14      EQU   14
                              0000000F  00000001  4318 V15      EQU   15
                              00000010  00000001  4319 V16      EQU   16
                              00000011  00000001  4320 V17      EQU   17
                              00000012  00000001  4321 V18      EQU   18
                              00000013  00000001  4322 V19      EQU   19
                              00000014  00000001  4323 V20      EQU   20
                              00000015  00000001  4324 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001  4325 V22       EQU   22
                                00000017  00000001  4326 V23       EQU   23
                                00000018  00000001  4327 V24       EQU   24
                                00000019  00000001  4328 V25       EQU   25
                                0000001A  00000001  4329 V26       EQU   26
                                0000001B  00000001  4330 V27       EQU   27
                                0000001C  00000001  4331 V28       EQU   28
                                0000001D  00000001  4332 V29       EQU   29
                                0000001E  00000001  4333 V30       EQU   30
                                0000001F  00000001  4334 V31       EQU   31
                                                    4335
                                                    4336           END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	164	130 160 161 162
CTLR0	F	0000048C	4	360	174 175 176 177
DECNUM	C	00001073	16	411	274 276 282 284
E7TEST	4	00000000	72	425	223
E7TESTS	F	00005F84	4	4163	216
EDIT	X	00001047	18	406	275 283
ENDTEST	U	0000031E	1	260	221
EOJ	I	00000470	4	350	209 263
EOJPSW	D	00000460	8	348	350
FAILCONT	U	0000030E	1	250	
FAILED	F	00001000	4	388	252 261
FAILMSG	U	0000030A	1	244	234
FAILPSW	D	00000478	8	352	354
FAILTEST	I	00000488	4	354	264
FB0001	F	00000280	8	193	197 198 200
IMAGE	1	00000000	24888	0	
K	U	00000400	1	372	373 374 375
K64	U	00010000	1	374	
M5	U	00000007	1	429	281
MB	U	00100000	1	375	
MSG	I	000003A8	4	310	208 293
MSGCMD	C	000003F6	9	340	323 324
MSGMSG	C	000003FF	95	341	317 338 315
MSGMVC	I	000003F0	6	338	321
MSGOK	I	000003BE	2	319	316
MSGRET	I	000003DE	4	334	327 330
MSGSAVE	F	000003E4	4	337	313 334
NEXTE7	U	000002D4	1	218	237 255
OPNAME	C	00000008	8	431	279
PAGE	U	00001000	1	373	
PRT3	C	0000105D	18	409	275 276 277 283 284 285
PRTLINE	C	00001008	16	394	401 292
PRTLNG	U	0000003F	1	401	291
PRTM5	C	00001044	2	399	285
PRTNAME	C	00001033	8	397	279
PRTNUM	C	00001018	3	395	277
R0	U	00000000	1	4282	124 174 177 197 199 200 201 206 225 226 251 252 290
					291 294 310 313 315 317 319 334
R1	U	00000001	1	4283	207 232 233 261 262 292 324 338 567 568 569 570 571
					572 601 602 603 604 605 606 635 636 637 638 639 640
					669 670 671 672 673 674 703 704 705 706 707 708 738
					739 740 741 742 743 772 773 774 775 776 777 806 807
					808 809 810 811 840 841 842 843 844 845 874 875 876
					877 878 879 909 910 911 912 913 914 943 944 945 946
					947 948 977 978 979 980 981 982 1011 1012 1013 1014 1015
					1016 1045 1046 1047 1048 1049 1050 1083 1084 1085 1086 1087 1088
					1117 1118 1119 1120 1121 1122 1151 1152 1153 1154 1155 1156 1185
					1186 1187 1188 1189 1190 1219 1220 1221 1222 1223 1224 1254 1255
					1256 1257 1258 1259 1288 1289 1290 1291 1292 1293 1322 1323 1324
					1325 1326 1327 1356 1357 1358 1359 1360 1361 1390 1391 1392 1393
					1394 1395 1425 1426 1427 1428 1429 1430 1459 1460 1461 1462 1463
					1464 1493 1494 1495 1496 1497 1498 1527 1528 1529 1530 1531 1532
					1561 1562 1563 1564 1565 1566 1599 1600 1601 1602 1603 1604 1633
					1634 1635 1636 1637 1638 1667 1668 1669 1670 1671 1672 1701 1702
					1703 1704 1705 1706 1735 1736 1737 1738 1739 1740 1770 1771 1772
					1773 1774 1775 1804 1805 1806 1807 1808 1809 1838 1839 1840 1841

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					1842	1843	1872	1873	1874	1875	1876	1877	1906	1907	1908	1909	1910
					1911	1941	1942	1943	1944	1945	1946	1975	1976	1977	1978	1979	1980
					2009	2010	2011	2012	2013	2014	2043	2044	2045	2046	2047	2048	2077
					2078	2079	2080	2081	2082	2115	2116	2117	2118	2119	2120	2149	2150
					2151	2152	2153	2154	2183	2184	2185	2186	2187	2188	2217	2218	2219
					2220	2221	2222	2251	2252	2253	2254	2255	2256	2286	2287	2288	2289
					2290	2291	2320	2321	2322	2323	2324	2325	2354	2355	2356	2357	2358
					2359	2388	2389	2390	2391	2392	2393	2422	2423	2424	2425	2426	2427
					2457	2458	2459	2460	2461	2462	2491	2492	2493	2494	2495	2496	2525
					2526	2527	2528	2529	2530	2559	2560	2561	2562	2563	2564	2593	2594
					2595	2596	2597	2598	2631	2632	2633	2634	2635	2636	2665	2666	2667
					2668	2669	2670	2699	2700	2701	2702	2703	2704	2733	2734	2735	2736
					2737	2738	2767	2768	2769	2770	2771	2772	2802	2803	2804	2805	2806
					2807	2836	2837	2838	2839	2840	2841	2870	2871	2872	2873	2874	2875
					2904	2905	2906	2907	2908	2909	2938	2939	2940	2941	2942	2943	2973
					2974	2975	2976	2977	2978	3007	3008	3009	3010	3011	3012	3041	3042
					3043	3044	3045	3046	3075	3076	3077	3078	3079	3080	3109	3110	3111
					3112	3113	3114	3147	3148	3149	3150	3151	3152	3181	3182	3183	3184
					3185	3186	3215	3216	3217	3218	3219	3220	3249	3250	3251	3252	3253
					3254	3283	3284	3285	3286	3287	3288	3318	3319	3320	3321	3322	3323
					3352	3353	3354	3355	3356	3357	3386	3387	3388	3389	3390	3391	3420
					3421	3422	3423	3424	3425	3454	3455	3456	3457	3458	3459	3489	3490
					3491	3492	3493	3494	3523	3524	3525	3526	3527	3528	3557	3558	3559
					3560	3561	3562	3591	3592	3593	3594	3595	3596	3625	3626	3627	3628
					3629	3630	3663	3664	3665	3666	3667	3668	3697	3698	3699	3700	3701
					3702	3731	3732	3733	3734	3735	3736	3765	3766	3767	3768	3769	3770
					3799	3800	3801	3802	3803	3804	3834	3835	3836	3837	3838	3839	3868
					3869	3870	3871	3872	3873	3902	3903	3904	3905	3906	3907	3936	3937
					3938	3939	3940	3941	3970	3971	3972	3973	3974	3975	4005	4006	4007
					4008	4009	4010	4039	4040	4041	4042	4043	4044	4073	4074	4075	4076
					4077	4078	4107	4108	4109	4110	4111	4112	4141	4142	4143	4144	4145
					4146												
R10	U	0000000A	1	4292	162	171	172										
R11	U	0000000B	1	4293	229	230	575	609	643	677	711	746	780	814	848	882	917
					951	985	1019	1053	1091	1125	1159	1193	1227	1262	1296	1330	1364
					1398	1433	1467	1501	1535	1569	1607	1641	1675	1709	1743	1778	1812
					1846	1880	1914	1949	1983	2017	2051	2085	2123	2157	2191	2225	2259
					2294	2328	2362	2396	2430	2465	2499	2533	2567	2601	2639	2673	2707
					2741	2775	2810	2844	2878	2912	2946	2981	3015	3049	3083	3117	3155
					3189	3223	3257	3291	3326	3360	3394	3428	3462	3497	3531	3565	3599
					3633	3671	3705	3739	3773	3807	3842	3876	3910	3944	3978	4013	4047
					4081	4115	4149										
R12	U	0000000C	1	4294	216	219	236	254									
R13	U	0000000D	1	4295													
R14	U	0000000E	1	4296													
R15	U	0000000F	1	4297	245	270	297	298									
R2	U	00000002	1	4284	208	273	274	281	282	290	293	294	311	313	319	320	321
					323	329	334	335									
R3	U	00000003	1	4285													
R4	U	00000004	1	4286													
R5	U	00000005	1	4287	219	220	223	271	296	551	577	585	611	619	645	653	679
					687	713	722	748	756	782	790	816	824	850	858	884	893
					919	927	953	961	987	995	1021	1029	1055	1067	1093	1101	1127
					1135	1161	1169	1195	1203	1229	1238	1264	1272	1298	1306	1332	1340
					1366	1374	1400	1409	1435	1443	1469	1477	1503	1511	1537	1545	1571
					1583	1609	1617	1643	1651	1677	1685	1711	1719	1745	1754	1780	1788

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					1814	1822	1848	1856	1882	1890	1916	1925	1951	1959	1985	1993	2019
					2027	2053	2061	2087	2099	2125	2133	2159	2167	2193	2201	2227	2235
					2261	2270	2296	2304	2330	2338	2364	2372	2398	2406	2432	2441	2467
					2475	2501	2509	2535	2543	2569	2577	2603	2615	2641	2649	2675	2683
					2709	2717	2743	2751	2777	2786	2812	2820	2846	2854	2880	2888	2914
					2922	2948	2957	2983	2991	3017	3025	3051	3059	3085	3093	3119	3131
					3157	3165	3191	3199	3225	3233	3259	3267	3293	3302	3328	3336	3362
					3370	3396	3404	3430	3438	3464	3473	3499	3507	3533	3541	3567	3575
					3601	3609	3635	3647	3673	3681	3707	3715	3741	3749	3775	3783	3809
					3818	3844	3852	3878	3886	3912	3920	3946	3954	3980	3989	4015	4023
					4049	4057	4083	4091	4117	4125	4151						
R6	U	00000006	1	4288													
R7	U	00000007	1	4289													
R8	U	00000008	1	4290	160	164	165	166	168								
R9	U	00000009	1	4291	161	168	169	171									
RE1	F	0000113C	4	576	557	558	559	561									
RE10	F	000017FC	4	883	864	865	866	868									
RE100	F	00005B7C	4	3979	3960	3961	3962	3964									
RE101	F	00005C3C	4	4014	3995	3996	3997	3999									
RE102	F	00005CFC	4	4048	4029	4030	4031	4033									
RE103	F	00005DBC	4	4082	4063	4064	4065	4067									
RE104	F	00005E7C	4	4116	4097	4098	4099	4101									
RE105	F	00005F3C	4	4150	4131	4132	4133	4135									
RE11	F	000018BC	4	918	899	900	901	903									
RE12	F	0000197C	4	952	933	934	935	937									
RE13	F	00001A3C	4	986	967	968	969	971									
RE14	F	00001AFC	4	1020	1001	1002	1003	1005									
RE15	F	00001BBC	4	1054	1035	1036	1037	1039									
RE16	F	00001C7C	4	1092	1073	1074	1075	1077									
RE17	F	00001D3C	4	1126	1107	1108	1109	1111									
RE18	F	00001DFC	4	1160	1141	1142	1143	1145									
RE19	F	00001EBC	4	1194	1175	1176	1177	1179									
RE2	F	000011FC	4	610	591	592	593	595									
RE20	F	00001F7C	4	1228	1209	1210	1211	1213									
RE21	F	0000203C	4	1263	1244	1245	1246	1248									
RE22	F	000020FC	4	1297	1278	1279	1280	1282									
RE23	F	000021BC	4	1331	1312	1313	1314	1316									
RE24	F	0000227C	4	1365	1346	1347	1348	1350									
RE25	F	0000233C	4	1399	1380	1381	1382	1384									
RE26	F	000023FC	4	1434	1415	1416	1417	1419									
RE27	F	000024BC	4	1468	1449	1450	1451	1453									
RE28	F	0000257C	4	1502	1483	1484	1485	1487									
RE29	F	0000263C	4	1536	1517	1518	1519	1521									
RE3	F	000012BC	4	644	625	626	627	629									
RE30	F	000026FC	4	1570	1551	1552	1553	1555									
RE31	F	000027BC	4	1608	1589	1590	1591	1593									
RE32	F	0000287C	4	1642	1623	1624	1625	1627									
RE33	F	0000293C	4	1676	1657	1658	1659	1661									
RE34	F	000029FC	4	1710	1691	1692	1693	1695									
RE35	F	00002ABC	4	1744	1725	1726	1727	1729									
RE36	F	00002B7C	4	1779	1760	1761	1762	1764									
RE37	F	00002C3C	4	1813	1794	1795	1796	1798									
RE38	F	00002CFC	4	1847	1828	1829	1830	1832									
RE39	F	00002DBC	4	1881	1862	1863	1864	1866									
RE4	F	0000137C	4	678	659	660	661	663									
RE40	F	00002E7C	4	1915	1896	1897	1898	1900									

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE41	F	00002F3C	4	1950	1931	1932	1933	1935
RE42	F	00002FFC	4	1984	1965	1966	1967	1969
RE43	F	000030BC	4	2018	1999	2000	2001	2003
RE44	F	0000317C	4	2052	2033	2034	2035	2037
RE45	F	0000323C	4	2086	2067	2068	2069	2071
RE46	F	000032FC	4	2124	2105	2106	2107	2109
RE47	F	000033BC	4	2158	2139	2140	2141	2143
RE48	F	0000347C	4	2192	2173	2174	2175	2177
RE49	F	0000353C	4	2226	2207	2208	2209	2211
RE5	F	0000143C	4	712	693	694	695	697
RE50	F	000035FC	4	2260	2241	2242	2243	2245
RE51	F	000036BC	4	2295	2276	2277	2278	2280
RE52	F	0000377C	4	2329	2310	2311	2312	2314
RE53	F	0000383C	4	2363	2344	2345	2346	2348
RE54	F	000038FC	4	2397	2378	2379	2380	2382
RE55	F	000039BC	4	2431	2412	2413	2414	2416
RE56	F	00003A7C	4	2466	2447	2448	2449	2451
RE57	F	00003B3C	4	2500	2481	2482	2483	2485
RE58	F	00003BFC	4	2534	2515	2516	2517	2519
RE59	F	00003CBC	4	2568	2549	2550	2551	2553
RE6	F	000014FC	4	747	728	729	730	732
RE60	F	00003D7C	4	2602	2583	2584	2585	2587
RE61	F	00003E3C	4	2640	2621	2622	2623	2625
RE62	F	00003EFC	4	2674	2655	2656	2657	2659
RE63	F	00003FBC	4	2708	2689	2690	2691	2693
RE64	F	0000407C	4	2742	2723	2724	2725	2727
RE65	F	0000413C	4	2776	2757	2758	2759	2761
RE66	F	000041FC	4	2811	2792	2793	2794	2796
RE67	F	000042BC	4	2845	2826	2827	2828	2830
RE68	F	0000437C	4	2879	2860	2861	2862	2864
RE69	F	0000443C	4	2913	2894	2895	2896	2898
RE7	F	000015BC	4	781	762	763	764	766
RE70	F	000044FC	4	2947	2928	2929	2930	2932
RE71	F	000045BC	4	2982	2963	2964	2965	2967
RE72	F	0000467C	4	3016	2997	2998	2999	3001
RE73	F	0000473C	4	3050	3031	3032	3033	3035
RE74	F	000047FC	4	3084	3065	3066	3067	3069
RE75	F	000048BC	4	3118	3099	3100	3101	3103
RE76	F	0000497C	4	3156	3137	3138	3139	3141
RE77	F	00004A3C	4	3190	3171	3172	3173	3175
RE78	F	00004AFC	4	3224	3205	3206	3207	3209
RE79	F	00004BBC	4	3258	3239	3240	3241	3243
RE8	F	0000167C	4	815	796	797	798	800
RE80	F	00004C7C	4	3292	3273	3274	3275	3277
RE81	F	00004D3C	4	3327	3308	3309	3310	3312
RE82	F	00004DFC	4	3361	3342	3343	3344	3346
RE83	F	00004EBC	4	3395	3376	3377	3378	3380
RE84	F	00004F7C	4	3429	3410	3411	3412	3414
RE85	F	0000503C	4	3463	3444	3445	3446	3448
RE86	F	000050FC	4	3498	3479	3480	3481	3483
RE87	F	000051BC	4	3532	3513	3514	3515	3517
RE88	F	0000527C	4	3566	3547	3548	3549	3551
RE89	F	0000533C	4	3600	3581	3582	3583	3585
RE9	F	0000173C	4	849	830	831	832	834
RE90	F	000053FC	4	3634	3615	3616	3617	3619
RE91	F	000054BC	4	3672	3653	3654	3655	3657

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE92	F	0000557C	4	3706	3687 3688 3689 3691
RE93	F	0000563C	4	3740	3721 3722 3723 3725
RE94	F	000056FC	4	3774	3755 3756 3757 3759
RE95	F	000057BC	4	3808	3789 3790 3791 3793
RE96	F	0000587C	4	3843	3824 3825 3826 3828
RE97	F	0000593C	4	3877	3858 3859 3860 3862
RE98	F	000059FC	4	3911	3892 3893 3894 3896
RE99	F	00005ABC	4	3945	3926 3927 3928 3930
REA1	A	000010E0	4	561	
REA10	A	000017A0	4	868	
REA100	A	00005B20	4	3964	
REA101	A	00005BE0	4	3999	
REA102	A	00005CA0	4	4033	
REA103	A	00005D60	4	4067	
REA104	A	00005E20	4	4101	
REA105	A	00005EE0	4	4135	
REA11	A	00001860	4	903	
REA12	A	00001920	4	937	
REA13	A	000019E0	4	971	
REA14	A	00001AA0	4	1005	
REA15	A	00001B60	4	1039	
REA16	A	00001C20	4	1077	
REA17	A	00001CE0	4	1111	
REA18	A	00001DA0	4	1145	
REA19	A	00001E60	4	1179	
REA2	A	000011A0	4	595	
REA20	A	00001F20	4	1213	
REA21	A	00001FE0	4	1248	
REA22	A	000020A0	4	1282	
REA23	A	00002160	4	1316	
REA24	A	00002220	4	1350	
REA25	A	000022E0	4	1384	
REA26	A	000023A0	4	1419	
REA27	A	00002460	4	1453	
REA28	A	00002520	4	1487	
REA29	A	000025E0	4	1521	
REA3	A	00001260	4	629	
REA30	A	000026A0	4	1555	
REA31	A	00002760	4	1593	
REA32	A	00002820	4	1627	
REA33	A	000028E0	4	1661	
REA34	A	000029A0	4	1695	
REA35	A	00002A60	4	1729	
REA36	A	00002B20	4	1764	
REA37	A	00002BE0	4	1798	
REA38	A	00002CA0	4	1832	
REA39	A	00002D60	4	1866	
REA4	A	00001320	4	663	
REA40	A	00002E20	4	1900	
REA41	A	00002EE0	4	1935	
REA42	A	00002FA0	4	1969	
REA43	A	00003060	4	2003	
REA44	A	00003120	4	2037	
REA45	A	000031E0	4	2071	
REA46	A	000032A0	4	2109	
REA47	A	00003360	4	2143	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA48	A	00003420	4	2177	
REA49	A	000034E0	4	2211	
REA5	A	000013E0	4	697	
REA50	A	000035A0	4	2245	
REA51	A	00003660	4	2280	
REA52	A	00003720	4	2314	
REA53	A	000037E0	4	2348	
REA54	A	000038A0	4	2382	
REA55	A	00003960	4	2416	
REA56	A	00003A20	4	2451	
REA57	A	00003AE0	4	2485	
REA58	A	00003BA0	4	2519	
REA59	A	00003C60	4	2553	
REA6	A	000014A0	4	732	
REA60	A	00003D20	4	2587	
REA61	A	00003DE0	4	2625	
REA62	A	00003EA0	4	2659	
REA63	A	00003F60	4	2693	
REA64	A	00004020	4	2727	
REA65	A	000040E0	4	2761	
REA66	A	000041A0	4	2796	
REA67	A	00004260	4	2830	
REA68	A	00004320	4	2864	
REA69	A	000043E0	4	2898	
REA7	A	00001560	4	766	
REA70	A	000044A0	4	2932	
REA71	A	00004560	4	2967	
REA72	A	00004620	4	3001	
REA73	A	000046E0	4	3035	
REA74	A	000047A0	4	3069	
REA75	A	00004860	4	3103	
REA76	A	00004920	4	3141	
REA77	A	000049E0	4	3175	
REA78	A	00004AA0	4	3209	
REA79	A	00004B60	4	3243	
REA8	A	00001620	4	800	
REA80	A	00004C20	4	3277	
REA81	A	00004CE0	4	3312	
REA82	A	00004DA0	4	3346	
REA83	A	00004E60	4	3380	
REA84	A	00004F20	4	3414	
REA85	A	00004FE0	4	3448	
REA86	A	000050A0	4	3483	
REA87	A	00005160	4	3517	
REA88	A	00005220	4	3551	
REA89	A	000052E0	4	3585	
REA9	A	000016E0	4	834	
REA90	A	000053A0	4	3619	
REA91	A	00005460	4	3657	
REA92	A	00005520	4	3691	
REA93	A	000055E0	4	3725	
REA94	A	000056A0	4	3759	
REA95	A	00005760	4	3793	
REA96	A	00005820	4	3828	
REA97	A	000058E0	4	3862	
REA98	A	000059A0	4	3896	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA99	A	00005A60	4	3930	
READDR	A	00000020	4	436	232
REG2LOW	U	000000DD	1	378	
REG2PATT	U	AABBCCDD	1	377	
RELEN	A	0000001C	4	435	
RPTDWSAV	D	00000398	8	303	290 294
RPTERROR	I	0000032C	4	270	245
RPTSAVE	F	00000390	4	300	270 297
RPTSVR5	F	00000394	4	301	271 296
SKL0001	U	0000004E	1	190	206
SKT0001	C	0000022A	20	187	190 207
SVOLDPSW	U	00000140	0	126	
T1	A	000010C0	4	552	4166
T10	A	00001780	4	859	4175
T100	A	00005B00	4	3955	4265
T101	A	00005BC0	4	3990	4266
T102	A	00005C80	4	4024	4267
T103	A	00005D40	4	4058	4268
T104	A	00005E00	4	4092	4269
T105	A	00005EC0	4	4126	4270
T11	A	00001840	4	894	4176
T12	A	00001900	4	928	4177
T13	A	000019C0	4	962	4178
T14	A	00001A80	4	996	4179
T15	A	00001B40	4	1030	4180
T16	A	00001C00	4	1068	4181
T17	A	00001CC0	4	1102	4182
T18	A	00001D80	4	1136	4183
T19	A	00001E40	4	1170	4184
T2	A	00001180	4	586	4167
T20	A	00001F00	4	1204	4185
T21	A	00001FC0	4	1239	4186
T22	A	00002080	4	1273	4187
T23	A	00002140	4	1307	4188
T24	A	00002200	4	1341	4189
T25	A	000022C0	4	1375	4190
T26	A	00002380	4	1410	4191
T27	A	00002440	4	1444	4192
T28	A	00002500	4	1478	4193
T29	A	000025C0	4	1512	4194
T3	A	00001240	4	620	4168
T30	A	00002680	4	1546	4195
T31	A	00002740	4	1584	4196
T32	A	00002800	4	1618	4197
T33	A	000028C0	4	1652	4198
T34	A	00002980	4	1686	4199
T35	A	00002A40	4	1720	4200
T36	A	00002B00	4	1755	4201
T37	A	00002BC0	4	1789	4202
T38	A	00002C80	4	1823	4203
T39	A	00002D40	4	1857	4204
T4	A	00001300	4	654	4169
T40	A	00002E00	4	1891	4205
T41	A	00002EC0	4	1926	4206
T42	A	00002F80	4	1960	4207
T43	A	00003040	4	1994	4208

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T44	A	00003100	4	2028	4209
T45	A	000031C0	4	2062	4210
T46	A	00003280	4	2100	4211
T47	A	00003340	4	2134	4212
T48	A	00003400	4	2168	4213
T49	A	000034C0	4	2202	4214
T5	A	000013C0	4	688	4170
T50	A	00003580	4	2236	4215
T51	A	00003640	4	2271	4216
T52	A	00003700	4	2305	4217
T53	A	000037C0	4	2339	4218
T54	A	00003880	4	2373	4219
T55	A	00003940	4	2407	4220
T56	A	00003A00	4	2442	4221
T57	A	00003AC0	4	2476	4222
T58	A	00003B80	4	2510	4223
T59	A	00003C40	4	2544	4224
T6	A	00001480	4	723	4171
T60	A	00003D00	4	2578	4225
T61	A	00003DC0	4	2616	4226
T62	A	00003E80	4	2650	4227
T63	A	00003F40	4	2684	4228
T64	A	00004000	4	2718	4229
T65	A	000040C0	4	2752	4230
T66	A	00004180	4	2787	4231
T67	A	00004240	4	2821	4232
T68	A	00004300	4	2855	4233
T69	A	000043C0	4	2889	4234
T7	A	00001540	4	757	4172
T70	A	00004480	4	2923	4235
T71	A	00004540	4	2958	4236
T72	A	00004600	4	2992	4237
T73	A	000046C0	4	3026	4238
T74	A	00004780	4	3060	4239
T75	A	00004840	4	3094	4240
T76	A	00004900	4	3132	4241
T77	A	000049C0	4	3166	4242
T78	A	00004A80	4	3200	4243
T79	A	00004B40	4	3234	4244
T8	A	00001600	4	791	4173
T80	A	00004C00	4	3268	4245
T81	A	00004CC0	4	3303	4246
T82	A	00004D80	4	3337	4247
T83	A	00004E40	4	3371	4248
T84	A	00004F00	4	3405	4249
T85	A	00004FC0	4	3439	4250
T86	A	00005080	4	3474	4251
T87	A	00005140	4	3508	4252
T88	A	00005200	4	3542	4253
T89	A	000052C0	4	3576	4254
T9	A	000016C0	4	825	4174
T90	A	00005380	4	3610	4255
T91	A	00005440	4	3648	4256
T92	A	00005500	4	3682	4257
T93	A	000055C0	4	3716	4258
T94	A	00005680	4	3750	4259

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
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T96	A	00005800	4	3819	4261
T97	A	000058C0	4	3853	4262
T98	A	00005980	4	3887	4263
T99	A	00005A40	4	3921	4264
TESTING	F	00001004	4	389	226
TNUM	H	00000004	2	427	225 273
TSUB	A	00000000	4	426	229
TTABLE	F	00005F84	4	4165	
V0	U	00000000	1	4303	
V1	U	00000001	1	4304	228
V10	U	0000000A	1	4313	
V11	U	0000000B	1	4314	
V12	U	0000000C	1	4315	
V13	U	0000000D	1	4316	
V14	U	0000000E	1	4317	
V15	U	0000000F	1	4318	
V16	U	00000010	1	4319	
V17	U	00000011	1	4320	
V18	U	00000012	1	4321	
V19	U	00000013	1	4322	
V1FUDGE	X	00001094	16	418	228
V1O1	X	000010F0	16	563	574
V1O10	X	000017B0	16	870	881
V1O100	X	00005B30	16	3966	3977
V1O101	X	00005BF0	16	4001	4012
V1O102	X	00005CB0	16	4035	4046
V1O103	X	00005D70	16	4069	4080
V1O104	X	00005E30	16	4103	4114
V1O105	X	00005EF0	16	4137	4148
V1O11	X	00001870	16	905	916
V1O12	X	00001930	16	939	950
V1O13	X	000019F0	16	973	984
V1O14	X	00001AB0	16	1007	1018
V1O15	X	00001B70	16	1041	1052
V1O16	X	00001C30	16	1079	1090
V1O17	X	00001CF0	16	1113	1124
V1O18	X	00001DB0	16	1147	1158
V1O19	X	00001E70	16	1181	1192
V1O2	X	000011B0	16	597	608
V1O20	X	00001F30	16	1215	1226
V1O21	X	00001FF0	16	1250	1261
V1O22	X	000020B0	16	1284	1295
V1O23	X	00002170	16	1318	1329
V1O24	X	00002230	16	1352	1363
V1O25	X	000022F0	16	1386	1397
V1O26	X	000023B0	16	1421	1432
V1O27	X	00002470	16	1455	1466
V1O28	X	00002530	16	1489	1500
V1O29	X	000025F0	16	1523	1534
V1O3	X	00001270	16	631	642
V1O30	X	000026B0	16	1557	1568
V1O31	X	00002770	16	1595	1606
V1O32	X	00002830	16	1629	1640
V1O33	X	000028F0	16	1663	1674
V1O34	X	000029B0	16	1697	1708

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1035	X	00002A70	16	1731	1742
V1036	X	00002B30	16	1766	1777
V1037	X	00002BF0	16	1800	1811
V1038	X	00002CB0	16	1834	1845
V1039	X	00002D70	16	1868	1879
V104	X	00001330	16	665	676
V1040	X	00002E30	16	1902	1913
V1041	X	00002EF0	16	1937	1948
V1042	X	00002FB0	16	1971	1982
V1043	X	00003070	16	2005	2016
V1044	X	00003130	16	2039	2050
V1045	X	000031F0	16	2073	2084
V1046	X	000032B0	16	2111	2122
V1047	X	00003370	16	2145	2156
V1048	X	00003430	16	2179	2190
V1049	X	000034F0	16	2213	2224
V105	X	000013F0	16	699	710
V1050	X	000035B0	16	2247	2258
V1051	X	00003670	16	2282	2293
V1052	X	00003730	16	2316	2327
V1053	X	000037F0	16	2350	2361
V1054	X	000038B0	16	2384	2395
V1055	X	00003970	16	2418	2429
V1056	X	00003A30	16	2453	2464
V1057	X	00003AF0	16	2487	2498
V1058	X	00003BB0	16	2521	2532
V1059	X	00003C70	16	2555	2566
V106	X	000014B0	16	734	745
V1060	X	00003D30	16	2589	2600
V1061	X	00003DF0	16	2627	2638
V1062	X	00003EB0	16	2661	2672
V1063	X	00003F70	16	2695	2706
V1064	X	00004030	16	2729	2740
V1065	X	000040F0	16	2763	2774
V1066	X	000041B0	16	2798	2809
V1067	X	00004270	16	2832	2843
V1068	X	00004330	16	2866	2877
V1069	X	000043F0	16	2900	2911
V107	X	00001570	16	768	779
V1070	X	000044B0	16	2934	2945
V1071	X	00004570	16	2969	2980
V1072	X	00004630	16	3003	3014
V1073	X	000046F0	16	3037	3048
V1074	X	000047B0	16	3071	3082
V1075	X	00004870	16	3105	3116
V1076	X	00004930	16	3143	3154
V1077	X	000049F0	16	3177	3188
V1078	X	00004AB0	16	3211	3222
V1079	X	00004B70	16	3245	3256
V108	X	00001630	16	802	813
V1080	X	00004C30	16	3279	3290
V1081	X	00004CF0	16	3314	3325
V1082	X	00004DB0	16	3348	3359
V1083	X	00004E70	16	3382	3393
V1084	X	00004F30	16	3416	3427
V1085	X	00004FF0	16	3450	3461

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1O86	X	000050B0	16	3485	3496
V1O87	X	00005170	16	3519	3530
V1O88	X	00005230	16	3553	3564
V1O89	X	000052F0	16	3587	3598
V1O9	X	000016F0	16	836	847
V1O90	X	000053B0	16	3621	3632
V1O91	X	00005470	16	3659	3670
V1O92	X	00005530	16	3693	3704
V1O93	X	000055F0	16	3727	3738
V1O94	X	000056B0	16	3761	3772
V1O95	X	00005770	16	3795	3806
V1O96	X	00005830	16	3830	3841
V1O97	X	000058F0	16	3864	3875
V1O98	X	000059B0	16	3898	3909
V1O99	X	00005A70	16	3932	3943
V1OUTPUT	X	00000030	16	438	233
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V20	U	00000014	1	4323	
V21	U	00000015	1	4324	
V22	U	00000016	1	4325	568 573 574 602 607 608 636 641 642 670 675 676 704 709 710 739 744 745 773 778 779 807 812 813 841 846 847 875 880 881 910 915 916 944 949 950 978 983 984 1012 1017 1018 1046 1051 1052 1084 1089 1090 1118 1123 1124 1152 1157 1158 1186 1191 1192 1220 1225 1226 1255 1260 1261 1289 1294 1295 1323 1328 1329 1357 1362 1363 1391 1396 1397 1426 1431 1432 1460 1465 1466 1494 1499 1500 1528 1533 1534 1562 1567 1568 1600 1605 1606 1634 1639 1640 1668 1673 1674 1702 1707 1708 1736 1741 1742 1771 1776 1777 1805 1810 1811 1839 1844 1845 1873 1878 1879 1907 1912 1913 1942 1947 1948 1976 1981 1982 2010 2015 2016 2044 2049 2050 2078 2083 2084 2116 2121 2122 2150 2155 2156 2184 2189 2190 2218 2223 2224 2252 2257 2258 2287 2292 2293 2321 2326 2327 2355 2360 2361 2389 2394 2395 2423 2428 2429 2458 2463 2464 2492 2497 2498 2526 2531 2532 2560 2565 2566 2594 2599 2600 2632 2637 2638 2666 2671 2672 2700 2705 2706 2734 2739 2740 2768 2773 2774 2803 2808 2809 2837 2842 2843 2871 2876 2877 2905 2910 2911 2939 2944 2945 2974 2979 2980 3008 3013 3014 3042 3047 3048 3076 3081 3082 3110 3115 3116 3148 3153 3154 3182 3187 3188 3216 3221 3222 3250 3255 3256 3284 3289 3290 3319 3324 3325 3353 3358 3359 3387 3392 3393 3421 3426 3427 3455 3460 3461 3490 3495 3496 3524 3529 3530 3558 3563 3564 3592 3597 3598 3626 3631 3632 3664 3669 3670 3698 3703 3704 3732 3737 3738 3766 3771 3772 3800 3805 3806 3835 3840 3841 3869 3874 3875 3903 3908 3909 3937 3942 3943 3971 3976 3977 4006 4011 4012 4040 4045 4046 4074 4079 4080 4108 4113 4114 4142 4147 4148
V23	U	00000017	1	4326	570 573 604 607 638 641 672 675 706 709 741 744 775 778 809 812 843 846 877 880 912 915 946 949 980 983 1014 1017 1048 1051 1086 1089 1120 1123 1154 1157 1188 1191 1222 1225 1257 1260 1291 1294 1325 1328 1359 1362 1393 1396 1428 1431 1462 1465 1496 1499 1530 1533 1564 1567 1602 1605 1636 1639 1670 1673 1704 1707 1738 1741 1773 1776 1807 1810 1841 1844 1875 1878 1909 1912 1944 1947 1978 1981 2012 2015 2046 2049 2080 2083 2118 2121 2152 2155 2186 2189 2220 2223 2254 2257 2289 2292 2323 2326 2357 2360 2391 2394 2425 2428 2460 2463 2494 2497 2528 2531 2562 2565 2596 2599 2634 2637 2668 2671 2702 2705 2736 2739 2770 2773 2805 2808 2839 2842 2873 2876 2907 2910 2941 2944 2976 2979 3010 3013 3044 3047 3078 3081 3112 3115 3150 3153 3184 3187 3218 3221

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
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					3700 3703 3734 3737 3768 3771 3802 3805 3837 3840 3871 3874 3905
					3908 3939 3942 3973 3976 4008 4011 4042 4045 4076 4079 4110 4113
					4144 4147
V24	U	00000018	1	4327	572 573 606 607 640 641 674 675 708 709 743 744 777
					778 811 812 845 846 879 880 914 915 948 949 982 983
					1016 1017 1050 1051 1088 1089 1122 1123 1156 1157 1190 1191 1224
					1225 1259 1260 1293 1294 1327 1328 1361 1362 1395 1396 1430 1431
					1464 1465 1498 1499 1532 1533 1566 1567 1604 1605 1638 1639 1672
					1673 1706 1707 1740 1741 1775 1776 1809 1810 1843 1844 1877 1878
					1911 1912 1946 1947 1980 1981 2014 2015 2048 2049 2082 2083 2120
					2121 2154 2155 2188 2189 2222 2223 2256 2257 2291 2292 2325 2326
					2359 2360 2393 2394 2427 2428 2462 2463 2496 2497 2530 2531 2564
					2565 2598 2599 2636 2637 2670 2671 2704 2705 2738 2739 2772 2773
					2807 2808 2841 2842 2875 2876 2909 2910 2943 2944 2978 2979 3012
					3013 3046 3047 3080 3081 3114 3115 3152 3153 3186 3187 3220 3221
					3254 3255 3288 3289 3323 3324 3357 3358 3391 3392 3425 3426 3459
					3460 3494 3495 3528 3529 3562 3563 3596 3597 3630 3631 3668 3669
					3702 3703 3736 3737 3770 3771 3804 3805 3839 3840 3873 3874 3907
					3908 3941 3942 3975 3976 4010 4011 4044 4045 4078 4079 4112 4113
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V26	U	0000001A	1	4329	
V27	U	0000001B	1	4330	
V28	U	0000001C	1	4331	
V29	U	0000001D	1	4332	
V2ADDR	A	00000010	4	432	567 601 635 669 703 738 772 806 840 874 909 943 977
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					1459 1493 1527 1561 1599 1633 1667 1701 1735 1770 1804 1838 1872
					1906 1941 1975 2009 2043 2077 2115 2149 2183 2217 2251 2286 2320
					2354 2388 2422 2457 2491 2525 2559 2593 2631 2665 2699 2733 2767
					2802 2836 2870 2904 2938 2973 3007 3041 3075 3109 3147 3181 3215
					3249 3283 3318 3352 3386 3420 3454 3489 3523 3557 3591 3625 3663
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					4141
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V30	U	0000001E	1	4333	
V31	U	0000001F	1	4334	
V3ADDR	A	00000014	4	433	569 603 637 671 705 740 774 808 842 876 911 945 979
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					1908 1943 1977 2011 2045 2079 2117 2151 2185 2219 2253 2288 2322
					2356 2390 2424 2459 2493 2527 2561 2595 2633 2667 2701 2735 2769
					2804 2838 2872 2906 2940 2975 3009 3043 3077 3111 3149 3183 3217
					3251 3285 3320 3354 3388 3422 3456 3491 3525 3559 3593 3627 3665
					3699 3733 3767 3801 3836 3870 3904 3938 3972 4007 4041 4075 4109
					4143
V4	U	00000004	1	4307	
V4ADDR	A	00000018	4	434	571 605 639 673 707 742 776 810 844 878 913 947 981
					1015 1049 1087 1121 1155 1189 1223 1258 1292 1326 1360 1394 1429
					1463 1497 1531 1565 1603 1637 1671 1705 1739 1774 1808 1842 1876
					1910 1945 1979 2013 2047 2081 2119 2153 2187 2221 2255 2290 2324
					2358 2392 2426 2461 2495 2529 2563 2597 2635 2669 2703 2737 2771
					2806 2840 2874 2908 2942 2977 3011 3045 3079 3113 3151 3185 3219
					3253 3287 3322 3356 3390 3424 3458 3493 3527 3561 3595 3629 3667

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
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V6	U	00000006	1	4309	
V7	U	00000007	1	4310	
V8	U	00000008	1	4311	
V9	U	00000009	1	4312	
X0001	U	000002A8	1	196	184 197
X1	F	00001108	4	566	552
X10	F	000017C8	4	873	859
X100	F	00005B48	4	3969	3955
X101	F	00005C08	4	4004	3990
X102	F	00005CC8	4	4038	4024
X103	F	00005D88	4	4072	4058
X104	F	00005E48	4	4106	4092
X105	F	00005F08	4	4140	4126
X11	F	00001888	4	908	894
X12	F	00001948	4	942	928
X13	F	00001A08	4	976	962
X14	F	00001AC8	4	1010	996
X15	F	00001B88	4	1044	1030
X16	F	00001C48	4	1082	1068
X17	F	00001D08	4	1116	1102
X18	F	00001DC8	4	1150	1136
X19	F	00001E88	4	1184	1170
X2	F	000011C8	4	600	586
X20	F	00001F48	4	1218	1204
X21	F	00002008	4	1253	1239
X22	F	000020C8	4	1287	1273
X23	F	00002188	4	1321	1307
X24	F	00002248	4	1355	1341
X25	F	00002308	4	1389	1375
X26	F	000023C8	4	1424	1410
X27	F	00002488	4	1458	1444
X28	F	00002548	4	1492	1478
X29	F	00002608	4	1526	1512
X3	F	00001288	4	634	620
X30	F	000026C8	4	1560	1546
X31	F	00002788	4	1598	1584
X32	F	00002848	4	1632	1618
X33	F	00002908	4	1666	1652
X34	F	000029C8	4	1700	1686
X35	F	00002A88	4	1734	1720
X36	F	00002B48	4	1769	1755
X37	F	00002C08	4	1803	1789
X38	F	00002CC8	4	1837	1823
X39	F	00002D88	4	1871	1857
X4	F	00001348	4	668	654
X40	F	00002E48	4	1905	1891
X41	F	00002F08	4	1940	1926
X42	F	00002FC8	4	1974	1960
X43	F	00003088	4	2008	1994
X44	F	00003148	4	2042	2028
X45	F	00003208	4	2076	2062
X46	F	000032C8	4	2114	2100
X47	F	00003388	4	2148	2134

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X48	F	00003448	4	2182	2168
X49	F	00003508	4	2216	2202
X5	F	00001408	4	702	688
X50	F	000035C8	4	2250	2236
X51	F	00003688	4	2285	2271
X52	F	00003748	4	2319	2305
X53	F	00003808	4	2353	2339
X54	F	000038C8	4	2387	2373
X55	F	00003988	4	2421	2407
X56	F	00003A48	4	2456	2442
X57	F	00003B08	4	2490	2476
X58	F	00003BC8	4	2524	2510
X59	F	00003C88	4	2558	2544
X6	F	000014C8	4	737	723
X60	F	00003D48	4	2592	2578
X61	F	00003E08	4	2630	2616
X62	F	00003EC8	4	2664	2650
X63	F	00003F88	4	2698	2684
X64	F	00004048	4	2732	2718
X65	F	00004108	4	2766	2752
X66	F	000041C8	4	2801	2787
X67	F	00004288	4	2835	2821
X68	F	00004348	4	2869	2855
X69	F	00004408	4	2903	2889
X7	F	00001588	4	771	757
X70	F	000044C8	4	2937	2923
X71	F	00004588	4	2972	2958
X72	F	00004648	4	3006	2992
X73	F	00004708	4	3040	3026
X74	F	000047C8	4	3074	3060
X75	F	00004888	4	3108	3094
X76	F	00004948	4	3146	3132
X77	F	00004A08	4	3180	3166
X78	F	00004AC8	4	3214	3200
X79	F	00004B88	4	3248	3234
X8	F	00001648	4	805	791
X80	F	00004C48	4	3282	3268
X81	F	00004D08	4	3317	3303
X82	F	00004DC8	4	3351	3337
X83	F	00004E88	4	3385	3371
X84	F	00004F48	4	3419	3405
X85	F	00005008	4	3453	3439
X86	F	000050C8	4	3488	3474
X87	F	00005188	4	3522	3508
X88	F	00005248	4	3556	3542
X89	F	00005308	4	3590	3576
X9	F	00001708	4	839	825
X90	F	000053C8	4	3624	3610
X91	F	00005488	4	3662	3648
X92	F	00005548	4	3696	3682
X93	F	00005608	4	3730	3716
X94	F	000056C8	4	3764	3750
X95	F	00005788	4	3798	3784
X96	F	00005848	4	3833	3819
X97	F	00005908	4	3867	3853
X98	F	000059C8	4	3901	3887

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X99	F	00005A88	4	3935	3921
XC0001	U	000002D0	1	210	202
ZVE7TST	J	00000000	24888	123	126 128 132 136 387 124
=A(E7TESTS)	A	00000498	4	365	216
=AL2(L'MSGMSG)	R	000004A2	2	368	315
=F'1'	F	0000049C	4	366	251
=F'64'	F	00000494	4	364	201
=H'0'	H	000004A0	2	367	310

```
 MACRO    DEFN   REFERENCES

FCHECK     76    183
PTTABLE   506   4164
VRR_D     457    549    583    617    651    685    720    754    788    822    856    891    925    959    993   1027   1065   1099
                1133   1167   1201   1236   1270   1304   1338   1372   1407   1441   1475   1509   1543   1581   1615   1649   1683
                1717   1752   1786   1820   1854   1888   1923   1957   1991   2025   2059   2097   2131   2165   2199   2233   2268
                2302   2336   2370   2404   2439   2473   2507   2541   2575   2613   2647   2681   2715   2749   2784   2818   2852
                2886   2920   2955   2989   3023   3057   3091   3129   3163   3197   3231   3265   3300   3334   3368   3402   3436
                3471   3505   3539   3573   3607   3645   3679   3713   3747   3781   3816   3850   3884   3918   3952   3987   4021
                4055   4089   4123
```

```
   DESC      SYMBOL    SIZE      POS         ADDR

Entry: 0

Image       IMAGE     24888   0000-6137   0000-6137
  Region                24888   0000-6137   0000-6137
    CSECT   ZVE7TST   24888   0000-6137   0000-6137
```

```
   STMT                          FILE NAME
1     /home/tn529/sharedvfp/tests/zvector-e7-10-multiplyAdd.asm

** NO ERRORS FOUND **
```