```
   LOC        OBJECT CODE      ADDR1      ADDR2     STMT

                                                      2  *****************************************************************************
                                                      3  *
                                                      4  *     Zvector E7 instruction tests for VRR-a encoded:
                                                      5  *
                                                      6  *     E7D4 VUPLL  - Vector Unpack Logical Low
                                                      7  *     E7D5 VUPLH  - Vector Unpack Logical High
                                                      8  *     E7D6 VUPL   - Vector Unpack Low
                                                      9  *     E7D7 VUPH   - Vector Unpack High
                                                     10  *
                                                     11  *     and
                                                     12  *
                                                     13  *     E75F VSEG   - Vector Sign Extend To Doubleword
                                                     14  *     E7DE VLC    - Vector Load Complement
                                                     15  *     E7DF VLP    - Vector Load Positive
                                                     16  *
                                                     17  *          James Wekel January 2025
                                                     18  *****************************************************************************


                                                     20  *****************************************************************************
                                                     21  *
                                                     22  *        basic instruction tests
                                                     23  *
                                                     24  *****************************************************************************
                                                     25  *  This program tests proper functioning of the z/arch E7 VRR-a
                                                     26  *  unpack instructions (Logical Low, Logical High, Low and High) and
                                                     27  *  miscellaneous instructions (Sign Extend To Doubleword,
                                                     28  *  Load Complement, and Load Positive).
                                                     29  *  Exceptions are not tested.
                                                     30  *
                                                     31  *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                     32  *  obvious coding errors.   None of the tests are thorough.   They are
                                                     33  *  NOT designed to test all aspects of any of the instructions.
                                                     34  *
                                                     35  *****************************************************************************
                                                     36  *
                                                     37  *     *Testcase zvector-e7-13-UnpackMisc
                                                     38  *     *
                                                     39  *     *    Zvector E7 instruction tests for VRR-a encoded:
                                                     40  *     *
                                                     41  *     *    E7D4 VUPLL  - Vector Unpack Logical Low
                                                     42  *     *    E7D5 VUPLH  - Vector Unpack Logical High
                                                     43  *     *    E7D6 VUPL   - Vector Unpack Low
                                                     44  *     *    E7D7 VUPH   - Vector Unpack High
                                                     45  *     *
                                                     46  *     *    E75F VSEG   - Vector Sign Extend To Doubleword
                                                     47  *     *    E7DE VLC    - Vector Load Complement
                                                     48  *     *    E7DF VLP    - Vector Load Positive
                                                     49  *     *
                                                     50  *     *    # -----------------------------------------------------------
                                                     51  *     *    #  This tests only the basic function of the instruction.
                                                     52  *     *    #  Exceptions are NOT tested.
                                                     53  *     *    # -----------------------------------------------------------
                                                     54  *     *
                                                     55  *     mainsize    2
                                                     56  *     numcpu      1
```

```
  LOC        OBJECT CODE        ADDR1      ADDR2     STMT

                                                     57 *    sysclear
                                                     58 *    archlvl     z/Arch
                                                     59 *
                                                     60 *    loadcore    "$(testpath)/zvector-e7-13-UnpackMisc.core" 0x0
                                                     61 *
                                                     62 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                     63 *    runtest     5         #
                                                     64 *    diag8cmd    disable   # (reset back to default)
                                                     65 *
                                                     66 *    *Done
                                                     67 *
                                                     68 *******************************************************************************
```

```
  LOC           OBJECT CODE      ADDR1     ADDR2     STMT

             70 ******************************************************************************
             71 *          FCHECK Macro - Is a Facility Bit set?
             72 *
             73 *          If the facility bit is NOT set, an message is issued and
             74 *          the test is skipped.
             75 *
             76 *          Fcheck uses R0, R1 and R2
             77 *
             78 * eg.      FCHECK 134,'vector-packed-decimal'
             79 ******************************************************************************
             80           MACRO
             81           FCHECK &BITNO,&NOTSETMSG
             82 .*                          &BITNO : facility bit number to check
             83 .*                          &NOTSETMSG : 'facility name'
             84           LCLA   &FBBYTE          Facility bit in Byte
             85           LCLA   &FBBIT           Facility bit within Byte
             86
             87           LCLA   &L(8)
             88 &L(1)     SetA   128,64,32,16,8,4,2,1  bit positions within byte
             89
             90 &FBBYTE   SETA   &BITNO/8
             91 &FBBIT    SETA   &L((&BITNO-(&FBBYTE*8))+1)
             92 .*        MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
             93
             94           B      X&SYSNDX
             95 *                                           Fcheck data area
             96 *                                           skip messgae
             97 SKT&SYSNDX DC   C'     Skipping tests: '
             98           DC     C&NOTSETMSG
             99           DC     C' (bit &BITNO) is not installed.'
            100 SKL&SYSNDX EQU *-SKT&SYSNDX
            101 *                                           facility bits
            102           DS     FD                gap
            103 FB&SYSNDX DS   4FD
            104           DS     FD                gap
            105 *
            106 X&SYSNDX EQU *
            107           LA     R0,((X&SYSNDX-FB&SYSNDX)/8)-1
            108           STFLE FB&SYSNDX           get facility bits
            109
            110           XGR    R0,R0
            111           IC     R0,FB&SYSNDX+&FBBYTE   get fbit byte
            112           N      R0,=F'&FBBIT'         is bit set?
            113           BNZ    XC&SYSNDX
            114 *
            115 * facility bit not set, issue message and exit
            116 *
            117           LA     R0,SKL&SYSNDX          message length
            118           LA     R1,SKT&SYSNDX          message address
            119           BAL    R2,MSG
            120
            121           B      EOJ
            122 XC&SYSNDX EQU *
            123           MEND
```

```
  LOC          OBJECT CODE        ADDR1       ADDR2       STMT

                                                          125 ****************************************************************************
                                                          126 *        Low core PSWs
                                                          127 ****************************************************************************
                                  00000000    000035EB    128 ZVE7TST   START 0
00000000                          00000000                129           USING ZVE7TST,R0              Low core addressability
                                                          130
                                  00000140    00000000    131 SVOLDPSW  EQU   ZVE7TST+X'140'           z/Arch Supervisor call old PSW


00000000                          00000000    000001A0    133           ORG   ZVE7TST+X'1A0'           z/Architecure RESTART PSW
000001A0    00000001 80000000                             134           DC    X'0000000180000000'
000001A8    00000000 00000200                             135           DC    AD(BEGIN)


000001B0                          000001B0    000001D0    137           ORG   ZVE7TST+X'1D0'           z/Architecure PROGRAM CHECK PSW
000001D0    00020001 80000000                             138           DC    X'0002000180000000'
000001D8    00000000 0000DEAD                             139           DC    AD(X'DEAD')



000001E0                          000001E0    00000200    141           ORG   ZVE7TST+X'200'           Start of actual test program..


                                                          143 ****************************************************************************
                                                          144 *                   The actual "ZVE7TST" program itself...
                                                          145 ****************************************************************************
                                                          146 *
                                                          147 *   Architecture Mode: z/Arch
                                                          148 *   Register Usage:
                                                          149 *
                                                          150 *    R0         (work)
                                                          151 *    R1-4       (work)
                                                          152 *    R5         Testing control table - current test base
                                                          153 *    R6-R7      (work)
                                                          154 *    R8         First base register
                                                          155 *    R9         Second base register
                                                          156 *    R10        Third base register
                                                          157 *    R11        E7TEST call return
                                                          158 *    R12        E7TESTS register
                                                          159 *    R13        (work)
                                                          160 *    R14        Subroutine call
                                                          161 *    R15        Secondary Subroutine call or work
                                                          162 *
                                                          163 ****************************************************************************

00000200                          00000200                165           USING BEGIN,R8                FIRST Base Register
00000200                          00001200                166           USING BEGIN+4096,R9           SECOND Base Register
00000200                          00002200                167           USING BEGIN+8192,R10          THIRD Base Register

00000200    0580                                          169 BEGIN     BALR  R8,0                     Initialize FIRST base register
00000202    0680                                          170           BCTR  R8,0                     Initialize FIRST base register
00000204    0680                                          171           BCTR  R8,0                     Initialize FIRST base register

00000206    4190 8800                         00000800    173           LA    R9,2048(,R8)             Initialize SECOND base register
0000020A    4190 9800                         00000800    174           LA    R9,2048(,R9)             Initialize SECOND base register
                                                          175
```

```
  LOC        OBJECT CODE      ADDR1      ADDR2     STMT

0000020E  41A0 9800                    00000800   176           LA     R10,2048(,R9)     Initalize THIRD base register
00000212  41A0 A800                    00000800   177           LA     R10,2048(,R10)    Initalize THIRD base register
                                                  178
00000216  B600 828C                    0000048C   179           STCTL  R0,R0,CTLR0       Store CR0 to enable AFP
0000021A  9604 828D                    0000048D   180           OI     CTLR0+1,X'04'     Turn on AFP bit
0000021E  9602 828D                    0000048D   181           OI     CTLR0+1,X'02'     Turn on Vector bit
00000222  B700 828C                    0000048C   182           LCTL   R0,R0,CTLR0       Reload updated CR0
                                                  183
                                                  184  ************************************************************************
                                                  185  * Is z/Architecture vector facility installed  (bit 129)
                                                  186  ************************************************************************
                                                  187
                                                  188           FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                    000002A8   189+          B      X0001
                                                  190+*                                   Fcheck data area
                                                  191+*                                   skip messgae
0000022A  40404040 E2928997                       192+SKT0001   DC     C'     Skipping tests: '
0000023E  A961C199 838889A3                       193+          DC     C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                       194+          DC     C' (bit 129) is not installed.'
                             0000004E  00000001   195+SKL0001   EQU    *-SKT0001
                                                  196+*                                   facility bits
00000278  00000000 00000000                       197+          DS     FD                gap
00000280  00000000 00000000                       198+FB0001    DS     4FD
000002A0  00000000 00000000                       199+          DS     FD                gap
                                                  200+*
                             000002A8  00000001   201+X0001     EQU    *
000002A8  4100 0004                    00000004   202+          LA     R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                    00000280   203+          STFLE  FB0001            get facility bits
000002B0  B982 0000                               204+          XGR    R0,R0
000002B4  4300 8090                    00000290   205+          IC     R0,FB0001+16      get fbit byte
000002B8  5400 8294                    00000494   206+          N      R0,=F'64'         is bit set?
000002BC  4770 80D0                    000002D0   207+          BNZ    XC0001
                                                  208+*
                                                  209+* facility bit not set, issue message and exit
                                                  210+*
000002C0  4100 004E                    0000004E   211+          LA     R0,SKL0001        message length
000002C4  4110 802A                    0000022A   212+          LA     R1,SKT0001        message address
000002C8  4520 81A8                    000003A8   213+          BAL    R2,MSG
000002CC  47F0 8270                    00000470   214+          B      EOJ
                             000002D0  00000001   215+XC0001    EQU    *
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  217 ************************************************************************
                                                  218 *              Do tests in the E7TESTS table
                                                  219 ************************************************************************
                                                  220
000002D0  58C0 8298                      00000498  221          L     R12,=A(E7TESTS)            get table of test addresses
                                                  222
          000002D4  00000001                      223 NEXTE7   EQU   *
000002D4  5850 C000                      00000000  224          L     R5,0(0,R12)               get test address
000002D8  1255                                     225          LTR   R5,R5                       have a test?
000002DA  4780 811E                      0000031E  226          BZ    ENDTEST                       done?
                                                  227
000002DE            00000000                       228          USING E7TEST,R5
                                                  229
000002DE  4800 5004                      00000004  230          LH    R0,TNUM                   save current test number
000002E2  5000 8E04                      00001004  231          ST    R0,TESTING                for easy reference
                                                  232
000002E6  E710 8E94 0006                 00001094  233          VL    V1,V1FUDGE
000002EC  58B0 5000                      00000000  234          L     R11,TSUB                  get address of test routine
000002F0  05BB                                     235          BALR  R11,R11                   do test
                                                  236
000002F2  E310 5018 0014                 00000018  237          LGF   R1,READDR                 get address of expected result
000002F8  D50F 5028 1000   00000028      00000000  238          CLC   V10UTPUT,0(R1)            valid?
000002FE  4770 810A                      0000030A  239          BNE   FAILMSG                      no, issue failed message
                                                  240
00000302  41C0 C004                      00000004  241          LA    R12,4(0,R12)              next test address
00000306  47F0 80D4                      000002D4  242          B     NEXTE7
```

```
 LOC        OBJECT CODE     ADDR1     ADDR2     STMT

                                                244 ******************************************************************************
                                                245 * result not as expected:
                                                246 *       issue message with test number, instruction under test
                                                247 *               and instruction m4
                                                248 ******************************************************************************
                            0000030A  00000001  249 FAILMSG  EQU    *
0000030A   45F0 812C                   0000032C  250          BAL    R15,RPTERROR


                                                252 ******************************************************************************
                                                253 * continue after a failed test
                                                254 ******************************************************************************
                            0000030E  00000001  255 FAILCONT EQU    *
0000030E   5800 829C                   0000049C  256          L      R0,=F'1'                   set failed test indicator
00000312   5000 8E00                   00001000  257          ST     R0,FAILED
                                                258
00000316   41C0 C004                   00000004  259          LA     R12,4(0,R12)               next test address
0000031A   47F0 80D4                   000002D4  260          B      NEXTE7


                                                262 ******************************************************************************
                                                263 * end of testing; set ending psw
                                                264 ******************************************************************************
                            0000031E  00000001  265 ENDTEST  EQU    *
0000031E   5810 8E00                   00001000  266          L      R1,FAILED                  did a test fail?
00000322   1211                                  267          LTR    R1,R1
00000324   4780 8270                   00000470  268          BZ     EOJ                        No, exit
00000328   47F0 8288                   00000488  269          B      FAILTEST                   Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  271 *********************************************************************
                                                  272 *          RPTERROR                    Report instruction test in error
                                                  273 *********************************************************************

0000032C  50F0 8190                     00000390  275 RPTERROR ST   R15,RPTSAVE             Save return address
00000330  5050 8194                     00000394  276          ST   R5,RPTSVR5              Save R5
                                                  277 *
00000334  4820 5004                     00000004  278          LH   R2,TNUM                 get test number and convert
00000338  4E20 8E73                     00001073  279          CVD  R2,DECNUM
0000033C  D211 8E5D 8E47      0000105D  00001047  280          MVC  PRT3,EDIT
00000342  DE11 8E5D 8E73      0000105D  00001073  281          ED   PRT3,DECNUM
00000348  D202 8E18 8E6A      00001018  0000106A  282          MVC  PRTNUM(3),PRT3+13       fill in message with test #
                                                  283
0000034E  D207 8E33 5008      00001033  00000008  284          MVC  PRTNAME,OPNAME          fill in message with instruction
                                                  285 *
00000354  E320 5007 0076                00000007  286          LB   R2,M3                   get M3 and convert
0000035A  4E20 8E73                     00001073  287          CVD  R2,DECNUM
0000035E  D211 8E5D 8E47      0000105D  00001047  288          MVC  PRT3,EDIT
00000364  DE11 8E5D 8E73      0000105D  00001073  289          ED   PRT3,DECNUM
0000036A  D201 8E44 8E6B      00001044  0000106B  290          MVC  PRTM3(2),PRT3+14        fill in message with m3 field

                                                  292 *
                                                  293 *          Use Hercules Diagnose for Message to console
                                                  294 *
00000370  9002 8198                     00000398  295          STM  R0,R2,RPTDWSAV          save regs used by MSG
00000374  4100 003F                     0000003F  296          LA   R0,PRTLNG               message length
00000378  4110 8E08                     00001008  297          LA   R1,PRTLINE              messagfe address
0000037C  4520 81A8                     000003A8  298          BAL  R2,MSG                  call Hercules to display MSG
00000380  9802 8198                     00000398  299          LM   R0,R2,RPTDWSAV          restore regs


00000384  5850 8194                     00000394  301          L    R5,RPTSVR5              Restore R5
00000388  58F0 8190                     00000390  302          L    R15,RPTSAVE             Restore return address
0000038C  07FF                                    303          BR   R15                     Return to caller

00000390  00000000                                305 RPTSAVE  DC   F'0'                    R15 save area
00000394  00000000                                306 RPTSVR5  DC   F'0'                    R5 save area

00000398  00000000 00000000                       308 RPTDWSAV DC   2D'0'                   R0-R2 save area for MSG call
```

```
  LOC         OBJECT CODE      ADDR1    ADDR2    STMT

                                                 310 ****************************************************************************
                                                 311 *          Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                 312 *                 R2 = return address
                                                 313 ****************************************************************************
000003A8  4900 82A0                     000004A0 315 MSG      CH     R0,=H'0'                 Do we even HAVE a message?
000003AC  07D2                                   316          BNHR   R2                       No, ignore

000003AE  9002 81E4                     000003E4 318          STM    R0,R2,MSGSAVE            Save registers

000003B2  4900 82A2                     000004A2 320          CH     R0,=AL2(L'MSGMSG)        Message length within limits?
000003B6  47D0 81BE                     000003BE 321          BNH    MSGOK                    Yes, continue
000003BA  4100 005F                     0000005F 322          LA     R0,L'MSGMSG             No, set to maximum

000003BE  1820                                   324 MSGOK    LR     R2,R0                    Copy length to work register
000003C0  0620                                   325          BCTR   R2,0                     Minus-1 for execute
000003C2  4420 81F0                     000003F0 326          EX     R2,MSGMVC                Copy message to O/P buffer

000003C6  4120 200A                     0000000A 328          LA     R2,1+L'MSGCMD(,R2)       Calculate true command length
000003CA  4110 81F6                     000003F6 329          LA     R1,MSGCMD                Point to true command

000003CE  83120008                               331          DC     X'83',X'12',X'0008'      Issue Hercules Diagnose X'008'
000003D2  4780 81DE                     000003DE 332          BZ     MSGRET                   Return if successful
                                                 333
000003D6  1222                                   334          LTR    R2,R2                    Is Diag8 Ry (R2) 0?
000003D8  4780 81DE                     000003DE 335          BZ     MSGRET                    an error occurred but coninue
                                                 336
000003DC  0000                                   337          DC     H'0'                     CRASH for debugging purposes

000003DE  9802 81E4                     000003E4 339 MSGRET   LM     R0,R2,MSGSAVE           Restore registers
000003E2  07F2                                   340          BR     R2                       Return to caller



000003E4  00000000 00000000             342 MSGSAVE  DC     3F'0'                    Registers save area
000003F0  D200 81FF 1000       000003FF 00000000 343 MSGMVC   MVC    MSGMSG(0),0(R1)          Executed instruction

000003F6  D4E2C7D5 D6C8405C             345 MSGCMD   DC     C'MSGNOH * '             *** HERCULES MESSAGE COMMAND ***
000003FF  40404040 40404040            346 MSGMSG   DC     CL95' '                  The message text to be displayed
                                                 347
```

```
 LOC          OBJECT CODE       ADDR1     ADDR2     STMT

                                                    349 *****************************************************************************
                                                    350 *          Normal completion or Abnormal termination PSWs
                                                    351 *****************************************************************************



00000460    00020001 80000000                       353 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000470    B2B2 8260                     00000460   355 EOJ      LPSWE EOJPSW                        Normal completion



00000478    00020001 80000000                       357 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

00000488    B2B2 8278                     00000478   359 FAILTEST LPSWE FAILPSW                       Abnormal termination




                                                    361 *****************************************************************************
                                                    362 *          Working Storage
                                                    363 *****************************************************************************


0000048C    00000000                                365 CTLR0    DS    F                             CR0
00000490    00000000                                366          DS    F

00000494                                            368          LTORG ,                             Literals pool
00000494    00000040                                369                =F'64'
00000498    000034BC                                370                =A(E7TESTS)
0000049C    00000001                                371                =F'1'
000004A0    0000                                    372                =H'0'
000004A2    005F                                    373                =AL2(L'MSGMSG)
                                                    374
                                                    375 *        some constants
                                                    376
                            00000400   00000001     377 K        EQU   1024                          One KB
                            00001000   00000001     378 PAGE     EQU   (4*K)                         Size of one page
                            00010000   00000001     379 K64      EQU   (64*K)                        64 KB
                            00100000   00000001     380 MB       EQU   (K*K)                          1 MB
                                                    381
                            AABBCCDD   00000001     382 REG2PATT EQU   X'AABBCCDD'                   Polluted Register pattern
                            000000DD   00000001     383 REG2LOW  EQU         X'DD'                   (last byte above)
```

```
   LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  385 *===============================================================================
                                                  386 *
                                                  387 *   NOTE: start data on an address that is easy to display
                                                  388 *         within Hercules
                                                  389 *
                                                  390 *===============================================================================
                                                  391
000004A4                      000004A4  00001000  392           ORG     ZVE7TST+X'1000'
00001000  00000000                                393 FAILED    DC      F'0'                      some test failed?
00001004  00000000                                394 TESTING   DC      F'0'                      current test number

                                                  396 *
                                                  397 *           failed message and associated editting
                                                  398 *
00001008  40404040 40404040                       399 PRTLINE   DC      C'         Test # '
00001018  A7A7A7                                  400 PRTNUM    DC      C'xxx'
0000101B  40868189 93858440                       401           DC      c' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                       402 PRTNAME   DC      CL8'xxxxxxxx'
0000103B  40A689A3 8840D4F3                       403           DC      C' with M3='
00001044  A7A7                                    404 PRTM3     DC      C'xx'
00001046  4B                                      405           DC      C'.'
                              0000003F  00000001  406 PRTLNG    EQU     *-PRTLINE
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  408 *****************************************************************************
                                                  409 *          TEST failed : message working storge
                                                  410 *****************************************************************************
00001047  40212020 20202020                       411 EDIT     DC     XL18'402120202020202020202020202020202020'
                                                  412
00001059  7E7E7E6E                                413          DC     C'===>'
0000105D  40404040 40404040                       414 PRT3     DC     CL18' '
0000106F  4C7E7E7E                                415          DC     C'<==='
00001073  00000000 00000000                       416 DECNUM   DS     CL16


                                                  418 *****************************************************************************
                                                  419 *          Vector instruction results, pollution and input
                                                  420 *****************************************************************************
00001084                                          421          DS     0F
00001084  00000000 00000000                       422          DS     XL16                                              gap
00001094  FFFFFFFF FFFFFFFF                        423 V1FUDGE  DC     XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'       V1 FUDGE
000010A4  00000000 00000000                       424          DS     XL16
```

```
 LOC          OBJECT CODE       ADDR1      ADDR2      STMT

                                                      426 *****************************************************************************
                                                      427 *          E7TEST DSECT
                                                      428 *****************************************************************************


                                                      430 E7TEST    DSECT ,
00000000    00000000                                  431 TSUB      DC      A(0)                      pointer  to test
00000004    0000                                      432 TNUM      DC      H'00'                     Test Number
00000006    00                                        433           DC      X'00'
00000007    00                                        434 M3        DC      HL1'00'                   m4 used
                                                      435
00000008    40404040 40404040                         436 OPNAME    DC      CL8' '                    E6 name
00000010    00000000                                  437 V2ADDR    DC      A(0)                      address of v2 source
00000014    00000000                                  438 RELEN     DC      A(0)                      RESULT LENGTH
00000018    00000000                                  439 READDR    DC      A(0)                      result (expected) address
00000020    00000000 00000000                         440           DS      FD                        gap
00000028    00000000 00000000                         441 V1OUTPUT  DS      XL16                      V1 Output
00000038    00000000 00000000                         442           DS      FD                        gap
                                                      443
                                                      444 *          test routine will be here (from VRR-a macro)
                                                      445 *
                                                      446 *          followed by
                                                      447 *              EXPECTED RESULT


                             00000000  000035EB        449 ZVE7TST   CSECT ,
000010B4                                               450           DS      0F


                                                      452 *****************************************************************************
                                                      453 *      Macros to help build test tables
                                                      454 *****************************************************************************


                                                      456 *
                                                      457 * macro to generate individual test
                                                      458 *
                                                      459           MACRO
                                                      460           VRR_A &INST,&M3
                                                      461 .*                                    &INST   - VRR-a instruction under test
                                                      462 .*                                    &M3     - m3 field
                                                      463
                                                      464           GBLA    &TNUM
                                                      465 &TNUM     SETA    &TNUM+1
                                                      466
                                                      467           DS      0FD
                                                      468           USING *,R5                   base for test data and test routine
                                                      469
                                                      470 T&TNUM    DC      A(X&TNUM)             address of test routine
                                                      471           DC      H'&TNUM'             test number
                                                      472           DC      X'00'
                                                      473           DC      HL1'&M3'             M3
                                                      474           DC      CL8'&INST'           instruction name
                                                      475           DC      A(RE&TNUM+16)        address of v2 source
                                                      476           DC      A(16)                result length
```

```
  LOC          OBJECT CODE        ADDR1     ADDR2     STMT

                                                      477 REA&TNUM DC      A(RE&TNUM)           result address
                                                      478          DS      FD                  gap
                                                      479 V10&TNUM DS      XL16                V1 output
                                                      480          DS      FD                  gap
                                                      481 .*
                                                      482 *
                                                      483 X&TNUM   DS      0F
                                                      484          LGF     R1,V2ADDR           load v2 source
                                                      485          VL      v22,0(R1)           use v22 to test decoder
                                                      486
                                                      487          &INST V22,V22,&M3           test instruction (dest is a source)
                                                      488          VST     V22,V10&TNUM        save v1 output
                                                      489
                                                      490          BR      R11                 return
                                                      491
                                                      492 RE&TNUM  DC      0F                  xl16 expected result
                                                      493
                                                      494          DROP R5
                                                      495          MEND


                                                      497 *
                                                      498 * macro to generate table of pointers to individual tests
                                                      499 *
                                                      500          MACRO
                                                      501          PTTABLE
                                                      502          GBLA    &TNUM
                                                      503          LCLA    &CUR
                                                      504 &CUR     SETA    1
                                                      505 .*
                                                      506 TTABLE   DS      0F
                                                      507 .LOOP    ANOP
                                                      508 .*
                                                      509          DC      A(T&CUR)
                                                      510 .*
                                                      511 &CUR     SETA    &CUR+1
                                                      512          AIF     (&CUR LE &TNUM).LOOP
                                                      513 *
                                                      514          DC      A(0)                         END OF TABLE
                                                      515          DC      A(0)                         END OF TABLE
                                                      516 .*
                                                      517          MEND
                                                      518
```

```
   LOC          OBJECT CODE      ADDR1      ADDR2      STMT

                                                       520 *******************************************************************
                                                       521 *        E7 VRR-a tests
                                                       522 *******************************************************************
                                                       523        PRINT DATA
                                                       524 *
                                                       525 *   E7D4 VUPLL  - Vector Unpack Logical Low
                                                       526 *   E7D5 VUPLH  - Vector Unpack Logical High
                                                       527 *   E7D6 VUPL   - Vector Unpack Low
                                                       528 *   E7D7 VUPH   - Vector Unpack High
                                                       529 *
                                                       530 *   and
                                                       531 *
                                                       532 *   E75F VSEG   - Vector Sign Extend To Doubleword
                                                       533 *   E7DE VLC    - Vector Load Complement
                                                       534 *   E7DF VLP    - Vector Load Positive
                                                       535 *
                                                       536 *        VRR-a instruction, M3
                                                       537 *             followed by
                                                       538 *                16 byte expected result (V1)
                                                       539 *                16 byte V2 source
                                                       540 *-------------------------------------------------------------------
                                                       541 * VUPLL  - Vector Unpack Logical Low
                                                       542 *-------------------------------------------------------------------
                                                       543 * Byte
                                                       544        VRR_A VUPLL, 0
000010B8                                               545+       DS    0FD
000010B8                       000010B8                546+       USING *, R5                    base for test data and test routine
000010B8   000010F8                                    547+T1     DC    A(X1)                     address of test routine
000010BC   0001                                        548+       DC    H'1'                      test number
000010BE   00                                          549+       DC    X'00'
000010BF   00                                          550+       DC    HL1'0'                    M3
000010C0   E5E4D7D3 D3404040                            551+       DC    CL8'VUPLL'                instruction name
000010C8   00001124                                    552+       DC    A(RE1+16)                 address of v2 source
000010CC   00000010                                    553+       DC    A(16)                     result length
000010D0   00001114                                    554+REA1   DC    A(RE1)                    result address
000010D8   00000000 00000000                            555+       DS    FD                        gap
000010E0   00000000 00000000                            556+V101   DS    XL16                      V1 output
000010E8   00000000 00000000
000010F0   00000000 00000000                            557+       DS    FD                        gap
                                                       558+*
000010F8                                               559+X1     DS    0F
000010F8   E310 5010 0014                   00000010    560+       LGF   R1, V2ADDR               load v2 source
000010FE   E761 0000 0806                   00000000    561+       VL    v22, 0(R1)               use v22 to test decoder
00001104   E766 0000 0CD4                               562+       VUPLL V22, V22, 0              test instruction (dest is a source)
0000110A   E760 5028 080E                   000010E0    563+       VST   V22, V101                save v1 output
00001110   07FB                                         564+       BR    R11                      return
00001114                                               565+RE1    DC    0F                        xl16 expected result
00001114                                               566+       DROP  R5
00001114   00110022 00330044                            567        DC    XL16'0011002200330044 0055006600770088'    result
0000111C   00550066 00770088
00001124   ABABABAB ABABABAB                            568        DC    XL16'ABABABABABABABAB 1122334455667788'    v2
0000112C   11223344 55667788
                                                       569
                                                       570        VRR_A VUPLL, 0
00001138                                               571+       DS    0FD
00001138                       00001138                572+       USING *, R5                    base for test data and test routine
```

```
   LOC         OBJECT CODE      ADDR1     ADDR2     STMT

00001138   00001178                                573+T2     DC      A(X2)              address of test routine
0000113C   0002                                    574+       DC      H'2'               test number
0000113E   00                                      575+       DC      X'00'
0000113F   00                                      576+       DC      HL1'0'             M3
00001140   E5E4D7D3 D3404040                        577+       DC      CL8'VUPLL'         instruction name
00001148   000011A4                                578+       DC      A(RE2+16)          address of v2 source
0000114C   00000010                                579+       DC      A(16)              result length
00001150   00001194                                580+REA2   DC      A(RE2)             result address
00001158   00000000 00000000                        581+       DS      FD                 gap
00001160   00000000 00000000                        582+V102   DS      XL16               V1 output
00001168   00000000 00000000
00001170   00000000 00000000                        583+       DS      FD                 gap
                                                    584+*
00001178                                            585+X2     DS      0F
00001178   E310 5010 0014                00000010   586+       LGF     R1,V2ADDR          load v2 source
0000117E   E761 0000 0806                00000000   587+       VL      v22,0(R1)          use v22 to test decoder
00001184   E766 0000 0CD4                           588+       VUPLL   V22,V22,0          test instruction (dest is a source)
0000118A   E760 5028 080E                00001160   589+       VST     V22,V102           save v1 output
00001190   07FB                                     590+       BR      R11                return
00001194                                            591+RE2    DC      0F                 xl16 expected result
00001194                                            592+       DROP    R5
00001194   00F10002 00C30004                        593        DC      XL16'00F1000200C30004 0005000600D700F8'    result
0000119C   00050006 00D700F8
000011A4   ABABABAB ABABABAB                        594        DC      XL16'ABABABABABABABAB F102C3040506D7F8'    v2
000011AC   F102C304 0506D7F8
                                                    595
                                                    596        VRR_A   VUPLL,0
000011B8                                            597+       DS      0FD
000011B8                              000011B8       598+       USING   *,R5               base for test data and test routine
000011B8   000011F8                                599+T3     DC      A(X3)              address of test routine
000011BC   0003                                     600+       DC      H'3'               test number
000011BE   00                                       601+       DC      X'00'
000011BF   00                                       602+       DC      HL1'0'             M3
000011C0   E5E4D7D3 D3404040                        603+       DC      CL8'VUPLL'         instruction name
000011C8   00001224                                604+       DC      A(RE3+16)          address of v2 source
000011CC   00000010                                605+       DC      A(16)              result length
000011D0   00001214                                606+REA3   DC      A(RE3)             result address
000011D8   00000000 00000000                        607+       DS      FD                 gap
000011E0   00000000 00000000                        608+V103   DS      XL16               V1 output
000011E8   00000000 00000000
000011F0   00000000 00000000                        609+       DS      FD                 gap
                                                    610+*
000011F8                                            611+X3     DS      0F
000011F8   E310 5010 0014                00000010   612+       LGF     R1,V2ADDR          load v2 source
000011FE   E761 0000 0806                00000000   613+       VL      v22,0(R1)          use v22 to test decoder
00001204   E766 0000 0CD4                           614+       VUPLL   V22,V22,0          test instruction (dest is a source)
0000120A   E760 5028 080E                000011E0   615+       VST     V22,V103           save v1 output
00001210   07FB                                     616+       BR      R11                return
00001214                                            617+RE3    DC      0F                 xl16 expected result
00001214                                            618+       DROP    R5
00001214   00F100D2 00C300F4                        619        DC      XL16'00F100D200C300F4 00F500C600D700F8'    result
0000121C   00F500C6 00D700F8
00001224   ABABABAB ABABABAB                        620        DC      XL16'ABABABABABABABAB F1D2C3F4F5C6D7F8'    v2
0000122C   F1D2C3F4 F5C6D7F8
                                                    621
                                                    622 * Halfword
```

```
  LOC           OBJECT CODE       ADDR1     ADDR2     STMT


                                                      623              VRR_A VUPLL, 1
00001238                                              624+             DS    0FD
00001238                          00001238            625+             USING *, R5                  base for test data and test routine
00001238  00001278                                    626+T4           DC    A(X4)                   address of test routine
0000123C  0004                                        627+             DC    H'4'                    test number
0000123E  00                                          628+             DC    X'00'
0000123F  01                                          629+             DC    HL1'1'                  M3
00001240  E5E4D7D3 D3404040                            630+             DC    CL8'VUPLL'              instruction name
00001248  000012A4                                    631+             DC    A(RE4+16)               address of v2 source
0000124C  00000010                                    632+             DC    A(16)                   result length
00001250  00001294                                    633+REA4         DC    A(RE4)                  result address
00001258  00000000 00000000                            634+             DS    FD                      gap
00001260  00000000 00000000                            635+V104         DS    XL16                    V1 output
00001268  00000000 00000000
00001270  00000000 00000000                            636+             DS    FD                      gap
                                                      637+*
00001278                                              638+X4           DS    0F
00001278  E310 5010 0014                    00000010  639+             LGF   R1, V2ADDR              load v2 source
0000127E  E761 0000 0806                    00000000  640+             VL    v22, 0(R1)              use v22 to test decoder
00001284  E766 0000 1CD4                              641+             VUPLL V22, V22, 1             test instruction (dest is a source)
0000128A  E760 5028 080E                    00001260  642+             VST   V22, V104               save v1 output
00001290  07FB                                        643+             BR    R11                     return
00001294                                              644+RE4          DC    0F                      xl16 expected result
00001294                                              645+             DROP  R5
00001294  00001122 00003344                            646              DC    XL16'0000112200003344 0000556600007788'    result
0000129C  00005566 00007788
000012A4  ABABABAB ABABABAB                            647              DC    XL16'ABABABABABABABAB 1122334455667788'    v2
000012AC  11223344 55667788

                                                      648
                                                      649              VRR_A VUPLL, 1
000012B8                                              650+             DS    0FD
000012B8                          000012B8            651+             USING *, R5                  base for test data and test routine
000012B8  000012F8                                    652+T5           DC    A(X5)                   address of test routine
000012BC  0005                                        653+             DC    H'5'                    test number
000012BE  00                                          654+             DC    X'00'
000012BF  01                                          655+             DC    HL1'1'                  M3
000012C0  E5E4D7D3 D3404040                            656+             DC    CL8'VUPLL'              instruction name
000012C8  00001324                                    657+             DC    A(RE5+16)               address of v2 source
000012CC  00000010                                    658+             DC    A(16)                   result length
000012D0  00001314                                    659+REA5         DC    A(RE5)                  result address
000012D8  00000000 00000000                            660+             DS    FD                      gap
000012E0  00000000 00000000                            661+V105         DS    XL16                    V1 output
000012E8  00000000 00000000
000012F0  00000000 00000000                            662+             DS    FD                      gap
                                                      663+*
000012F8                                              664+X5           DS    0F
000012F8  E310 5010 0014                    00000010  665+             LGF   R1, V2ADDR              load v2 source
000012FE  E761 0000 0806                    00000000  666+             VL    v22, 0(R1)              use v22 to test decoder
00001304  E766 0000 1CD4                              667+             VUPLL V22, V22, 1             test instruction (dest is a source)
0000130A  E760 5028 080E                    000012E0  668+             VST   V22, V105               save v1 output
00001310  07FB                                        669+             BR    R11                     return
00001314                                              670+RE5          DC    0F                      xl16 expected result
00001314                                              671+             DROP  R5
00001314  0000F102 0000C304                            672              DC    XL16'0000F1020000C304 000005060000D7F8'    result
0000131C  00000506 0000D7F8
00001324  ABABABAB ABABABAB                            673              DC    XL16'ABABABABABABABAB F102C3040506D7F8'    v2
```

```
  LOC          OBJECT CODE     ADDR1     ADDR2     STMT

0000132C  F102C304 0506D7F8
                                                   674
                                                   675        VRR_A VUPLL, 1
00001338                                           676+       DS    0FD
00001338                              00001338     677+       USING *, R5                    base for test data and test routine
00001338  00001378                                 678+T6     DC    A(X6)                     address of test routine
0000133C  0006                                     679+       DC    H'6'                      test number
0000133E  00                                       680+       DC    X'00'
0000133F  01                                       681+       DC    HL1'1'                    M3
00001340  E5E4D7D3 D3404040                         682+       DC    CL8'VUPLL'                instruction name
00001348  000013A4                                 683+       DC    A(RE6+16)                 address of v2 source
0000134C  00000010                                 684+       DC    A(16)                     result length
00001350  00001394                                 685+REA6   DC    A(RE6)                    result address
00001358  00000000 00000000                         686+       DS    FD                        gap
00001360  00000000 00000000                         687+V106   DS    XL16                      V1 output
00001368  00000000 00000000
00001370  00000000 00000000                         688+       DS    FD                        gap
                                                   689+*
00001378                                           690+X6     DS    0F
00001378  E310 5010 0014                00000010   691+       LGF   R1, V2ADDR                load v2 source
0000137E  E761 0000 0806                00000000   692+       VL    v22, 0(R1)                use v22 to test decoder
00001384  E766 0000 1CD4                           693+       VUPLL V22, V22, 1               test instruction (dest is a source)
0000138A  E760 5028 080E                00001360   694+       VST   V22, V106                 save v1 output
00001390  07FB                                     695+       BR    R11                       return
00001394                                           696+RE6    DC    0F                        xl16 expected result
00001394                                           697+       DROP  R5
00001394  0000F1D2 0000C3F4                         698        DC    XL16'0000F1D20000C3F4 0000F5C60000D7F8'     result
0000139C  0000F5C6 0000D7F8
000013A4  ABABABAB ABABABAB                          699        DC    XL16'ABABABABABABABAB F1D2C3F4F5C6D7F8'     v2
000013AC  F1D2C3F4 F5C6D7F8
                                                   700
                                                   701 * Word
                                                   702        VRR_A VUPLL, 2
000013B8                                           703+       DS    0FD
000013B8                              000013B8     704+       USING *, R5                    base for test data and test routine
000013B8  000013F8                                 705+T7     DC    A(X7)                     address of test routine
000013BC  0007                                     706+       DC    H'7'                      test number
000013BE  00                                       707+       DC    X'00'
000013BF  02                                       708+       DC    HL1'2'                    M3
000013C0  E5E4D7D3 D3404040                         709+       DC    CL8'VUPLL'                instruction name
000013C8  00001424                                 710+       DC    A(RE7+16)                 address of v2 source
000013CC  00000010                                 711+       DC    A(16)                     result length
000013D0  00001414                                 712+REA7   DC    A(RE7)                    result address
000013D8  00000000 00000000                         713+       DS    FD                        gap
000013E0  00000000 00000000                         714+V107   DS    XL16                      V1 output
000013E8  00000000 00000000
000013F0  00000000 00000000                         715+       DS    FD                        gap
                                                   716+*
000013F8                                           717+X7     DS    0F
000013F8  E310 5010 0014                00000010   718+       LGF   R1, V2ADDR                load v2 source
000013FE  E761 0000 0806                00000000   719+       VL    v22, 0(R1)                use v22 to test decoder
00001404  E766 0000 2CD4                           720+       VUPLL V22, V22, 2               test instruction (dest is a source)
0000140A  E760 5028 080E                000013E0   721+       VST   V22, V107                 save v1 output
00001410  07FB                                     722+       BR    R11                       return
00001414                                           723+RE7    DC    0F                        xl16 expected result
00001414                                           724+       DROP  R5
```

```
  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

00001414   00000000 11223344                        725         DC      XL16'0000000011223344 0000000055667788'      result
0000141C   00000000 55667788
00001424   ABABABAB ABABABAB                        726         DC      XL16'ABABABABABABABAB 1122334455667788'      v2
0000142C   11223344 55667788
                                                    727
                                                    728         VRR_A VUPLL,2
00001438                                            729+        DS      0FD
00001438                        00001438            730+        USING   *,R5                        base for test data and test routine
00001438   00001478                                731+T8       DC      A(X8)                       address of test routine
0000143C   0008                                     732+        DC      H'8'                        test number
0000143E   00                                       733+        DC      X'00'
0000143F   02                                       734+        DC      HL1'2'                      M3
00001440   E5E4D7D3 D3404040                        735+        DC      CL8'VUPLL'                  instruction name
00001448   000014A4                                 736+        DC      A(RE8+16)                   address of v2 source
0000144C   00000010                                 737+        DC      A(16)                       result length
00001450   00001494                                 738+REA8    DC      A(RE8)                      result address
00001458   00000000 00000000                        739+        DS      FD                          gap
00001460   00000000 00000000                        740+V108    DS      XL16                        V1 output
00001468   00000000 00000000
00001470   00000000 00000000                        741+        DS      FD                          gap
                                                    742+*
00001478                                            743+X8       DS      0F
00001478   E310 5010 0014                 00000010  744+        LGF     R1,V2ADDR                   load v2 source
0000147E   E761 0000 0806                 00000000  745+        VL      v22,0(R1)                   use v22 to test decoder
00001484   E766 0000 2CD4                           746+        VUPLL   V22,V22,2                   test instruction (dest is a source)
0000148A   E760 5028 080E                 00001460  747+        VST     V22,V108                    save v1 output
00001490   07FB                                     748+        BR      R11                         return
00001494                                            749+RE8     DC      0F                          xl16 expected result
00001494                                            750+        DROP    R5
00001494   00000000 F102C304                        751         DC      XL16'00000000F102C304 000000000506D7F8'      result
0000149C   00000000 0506D7F8
000014A4   ABABABAB ABABABAB                        752         DC      XL16'ABABABABABABABAB F102C3040506D7F8'      v2
000014AC   F102C304 0506D7F8
                                                    753
                                                    754         VRR_A VUPLL,2
000014B8                                            755+        DS      0FD
000014B8                        000014B8            756+        USING   *,R5                        base for test data and test routine
000014B8   000014F8                                757+T9       DC      A(X9)                       address of test routine
000014BC   0009                                     758+        DC      H'9'                        test number
000014BE   00                                       759+        DC      X'00'
000014BF   02                                       760+        DC      HL1'2'                      M3
000014C0   E5E4D7D3 D3404040                        761+        DC      CL8'VUPLL'                  instruction name
000014C8   00001524                                 762+        DC      A(RE9+16)                   address of v2 source
000014CC   00000010                                 763+        DC      A(16)                       result length
000014D0   00001514                                 764+REA9    DC      A(RE9)                      result address
000014D8   00000000 00000000                        765+        DS      FD                          gap
000014E0   00000000 00000000                        766+V109    DS      XL16                        V1 output
000014E8   00000000 00000000
000014F0   00000000 00000000                        767+        DS      FD                          gap
                                                    768+*
000014F8                                            769+X9       DS      0F
000014F8   E310 5010 0014                 00000010  770+        LGF     R1,V2ADDR                   load v2 source
000014FE   E761 0000 0806                 00000000  771+        VL      v22,0(R1)                   use v22 to test decoder
00001504   E766 0000 2CD4                           772+        VUPLL   V22,V22,2                   test instruction (dest is a source)
0000150A   E760 5028 080E                 000014E0  773+        VST     V22,V109                    save v1 output
00001510   07FB                                     774+        BR      R11                         return
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00001514                                          775+RE9      DC    0F                      xl16 expected result
00001514                                          776+         DROP  R5
00001514   00000000 F1D2C3F4                      777          DC    XL16'00000000F1D2C3F4 00000000F5C6D7F8'     result
0000151C   00000000 F5C6D7F8
00001524   ABABABAB ABABABAB                      778          DC    XL16'ABABABABABABABAB F1D2C3F4F5C6D7F8'     v2
0000152C   F1D2C3F4 F5C6D7F8
                                                  779
                                                  780 *-------------------------------------------------------------
                                                  781 * VUPLH  - Vector Unpack Logical High
                                                  782 *-------------------------------------------------------------
                                                  783 * Byte
                                                  784          VRR_A VUPLH,0
00001538                                          785+         DS    0FD
00001538                       00001538           786+         USING *,R5                    base for test data and test routine
00001538   00001578                               787+T10      DC    A(X10)                   address of test routine
0000153C   000A                                   788+         DC    H'10'                    test number
0000153E   00                                     789+         DC    X'00'
0000153F   00                                     790+         DC    HL1'0'                   M3
00001540   E5E4D7D3 C8404040                      791+         DC    CL8'VUPLH'               instruction name
00001548   000015A4                               792+         DC    A(RE10+16)               address of v2 source
0000154C   00000010                               793+         DC    A(16)                    result length
00001550   00001594                               794+REA10    DC    A(RE10)                  result address
00001558   00000000 00000000                      795+         DS    FD                       gap
00001560   00000000 00000000                      796+V1010    DS    XL16                     V1 output
00001568   00000000 00000000
00001570   00000000 00000000                      797+         DS    FD                       gap
                                                  798+*
00001578                                          799+X10      DS    0F
00001578   E310 5010 0014            00000010     800+         LGF   R1,V2ADDR                load v2 source
0000157E   E761 0000 0806            00000000     801+         VL    v22,0(R1)                use v22 to test decoder
00001584   E766 0000 0CD5                         802+         VUPLH V22,V22,0                test instruction (dest is a source)
0000158A   E760 5028 080E            00001560     803+         VST   V22,V1010                save v1 output
00001590   07FB                                   804+         BR    R11                      return
00001594                                          805+RE10     DC    0F                       xl16 expected result
00001594                                          806+         DROP  R5
00001594   00110022 00330044                      807          DC    XL16'0011002200330044 0055006600770088'     result
0000159C   00550066 00770088
000015A4   11223344 55667788                      808          DC    XL16'1122334455667788 ABABABABABABABAB'     v2
000015AC   ABABABAB ABABABAB
                                                  809
                                                  810          VRR_A VUPLH,0
000015B8                                          811+         DS    0FD
000015B8                       000015B8           812+         USING *,R5                    base for test data and test routine
000015B8   000015F8                               813+T11      DC    A(X11)                   address of test routine
000015BC   000B                                   814+         DC    H'11'                    test number
000015BE   00                                     815+         DC    X'00'
000015BF   00                                     816+         DC    HL1'0'                   M3
000015C0   E5E4D7D3 C8404040                      817+         DC    CL8'VUPLH'               instruction name
000015C8   00001624                               818+         DC    A(RE11+16)               address of v2 source
000015CC   00000010                               819+         DC    A(16)                    result length
000015D0   00001614                               820+REA11    DC    A(RE11)                  result address
000015D8   00000000 00000000                      821+         DS    FD                       gap
000015E0   00000000 00000000                      822+V1011    DS    XL16                     V1 output
000015E8   00000000 00000000
000015F0   00000000 00000000                      823+         DS    FD                       gap
                                                  824+*
```

```
  LOC         OBJECT CODE     ADDR1     ADDR2    STMT

000015F8                                        825+X11      DS    0F
000015F8   E310 5010 0014              00000010  826+         LGF   R1,V2ADDR            load v2 source
000015FE   E761 0000 0806              00000000  827+         VL    v22,0(R1)           use v22 to test decoder
00001604   E766 0000 0CD5                        828+         VUPLH V22,V22,0            test instruction (dest is a source)
0000160A   E760 5028 080E              000015E0  829+         VST   V22,V1011           save v1 output
00001610   07FB                                  830+         BR    R11                 return
00001614                                         831+RE11     DC    0F                  xl16 expected result
00001614                                         832+         DROP  R5
00001614   00F10002 00C30004                     833          DC    XL16'00F1000200C30004 0005000600D700F8'     result
0000161C   00050006 00D700F8
00001624   F102C304 0506D7F8                     834          DC    XL16'F102C3040506D7F8 ABABABABABABABAB'      v2
0000162C   ABABABAB ABABABAB
                                                 835
                                                 836          VRR_A VUPLH, 0
00001638                                         837+         DS    0FD
00001638                         00001638        838+         USING *,R5                base for test data and test routine
00001638   00001678                              839+T12      DC    A(X12)              address of test routine
0000163C   000C                                  840+         DC    H'12'               test number
0000163E   00                                    841+         DC    X'00'
0000163F   00                                    842+         DC    HL1'0'              M3
00001640   E5E4D7D3 C8404040                     843+         DC    CL8'VUPLH'          instruction name
00001648   000016A4                              844+         DC    A(RE12+16)          address of v2 source
0000164C   00000010                              845+         DC    A(16)               result length
00001650   00001694                              846+REA12    DC    A(RE12)             result address
00001658   00000000 00000000                     847+         DS    FD                  gap
00001660   00000000 00000000                     848+V1012    DS    XL16               V1 output
00001668   00000000 00000000
00001670   00000000 00000000                     849+         DS    FD                  gap
                                                 850+*
00001678                                         851+X12      DS    0F
00001678   E310 5010 0014              00000010  852+         LGF   R1,V2ADDR           load v2 source
0000167E   E761 0000 0806              00000000  853+         VL    v22,0(R1)           use v22 to test decoder
00001684   E766 0000 0CD5                        854+         VUPLH V22,V22,0            test instruction (dest is a source)
0000168A   E760 5028 080E              00001660  855+         VST   V22,V1012           save v1 output
00001690   07FB                                  856+         BR    R11                 return
00001694                                         857+RE12     DC    0F                  xl16 expected result
00001694                                         858+         DROP  R5
00001694   00F100D2 00C300F4                     859          DC    XL16'00F100D200C300F4 00F500C600D700F8'     result
0000169C   00F500C6 00D700F8
000016A4   F1D2C3F4 F5C6D7F8                     860          DC    XL16'F1D2C3F4F5C6D7F8 ABABABABABABABAB'      v2
000016AC   ABABABAB ABABABAB
                                                 861
                                                 862  * Halfword
                                                 863          VRR_A VUPLH, 1
000016B8                                         864+         DS    0FD
000016B8                         000016B8        865+         USING *,R5                base for test data and test routine
000016B8   000016F8                              866+T13      DC    A(X13)              address of test routine
000016BC   000D                                  867+         DC    H'13'               test number
000016BE   00                                    868+         DC    X'00'
000016BF   01                                    869+         DC    HL1'1'              M3
000016C0   E5E4D7D3 C8404040                     870+         DC    CL8'VUPLH'          instruction name
000016C8   00001724                              871+         DC    A(RE13+16)          address of v2 source
000016CC   00000010                              872+         DC    A(16)               result length
000016D0   00001714                              873+REA13    DC    A(RE13)             result address
000016D8   00000000 00000000                     874+         DS    FD                  gap
000016E0   00000000 00000000                     875+V1013    DS    XL16               V1 output
```

```
   LOC          OBJECT CODE      ADDR1     ADDR2     STMT

000016E8  00000000 00000000
000016F0  00000000 00000000            876+          DS     FD                  gap
                                       877+*
000016F8                               878+X13        DS     OF
000016F8  E310 5010 0014                 00000010     879+          LGF    R1,V2ADDR           load v2 source
000016FE  E761 0000 0806                 00000000     880+          VL     v22,0(R1)           use v22 to test decoder
00001704  E766 0000 1CD5                              881+          VUPLH  V22,V22,1           test instruction (dest is a source)
0000170A  E760 5028 080E                 000016E0     882+          VST    V22,V1013           save v1 output
00001710  07FB                                        883+          BR     R11                 return
00001714                                              884+RE13      DC     0F                  xl16 expected result
00001714                                              885+          DROP   R5
00001714  00001122 00003344                           886           DC     XL16'0000112200003344 0000556600007788'   result
0000171C  00005566 00007788
00001724  11223344 55667788                           887           DC     XL16'1122334455667788 ABABABABABABABAB'   v2
0000172C  ABABABAB ABABABAB
                                                      888
                                                      889           VRR_A  VUPLH,1
00001738                                              890+          DS     0FD
00001738                          00001738            891+          USING  *,R5                base for test data and test routine
00001738  00001778                                    892+T14       DC     A(X14)              address of test routine
0000173C  000E                                        893+          DC     H'14'               test number
0000173E  00                                          894+          DC     X'00'
0000173F  01                                          895+          DC     HL1'1'              M3
00001740  E5E4D7D3 C8404040                           896+          DC     CL8'VUPLH'          instruction name
00001748  000017A4                                    897+          DC     A(RE14+16)          address of v2 source
0000174C  00000010                                    898+          DC     A(16)               result length
00001750  00001794                                    899+REA14     DC     A(RE14)             result address
00001758  00000000 00000000                           900+          DS     FD                  gap
00001760  00000000 00000000                           901+V1014     DS     XL16                V1 output
00001768  00000000 00000000
00001770  00000000 00000000                           902+          DS     FD                  gap
                                                      903+*
00001778                                              904+X14        DS     OF
00001778  E310 5010 0014                 00000010     905+          LGF    R1,V2ADDR           load v2 source
0000177E  E761 0000 0806                 00000000     906+          VL     v22,0(R1)           use v22 to test decoder
00001784  E766 0000 1CD5                              907+          VUPLH  V22,V22,1           test instruction (dest is a source)
0000178A  E760 5028 080E                 00001760     908+          VST    V22,V1014           save v1 output
00001790  07FB                                        909+          BR     R11                 return
00001794                                              910+RE14      DC     0F                  xl16 expected result
00001794                                              911+          DROP   R5
00001794  0000F102 0000C304                           912           DC     XL16'0000F1020000C304 000005060000D7F8'   result
0000179C  00000506 0000D7F8
000017A4  F102C304 0506D7F8                           913           DC     XL16'F102C3040506D7F8 ABABABABABABABAB'   v2
000017AC  ABABABAB ABABABAB
                                                      914
                                                      915           VRR_A  VUPLH,1
000017B8                                              916+          DS     0FD
000017B8                          000017B8            917+          USING  *,R5                base for test data and test routine
000017B8  000017F8                                    918+T15       DC     A(X15)              address of test routine
000017BC  000F                                        919+          DC     H'15'               test number
000017BE  00                                          920+          DC     X'00'
000017BF  01                                          921+          DC     HL1'1'              M3
000017C0  E5E4D7D3 C8404040                           922+          DC     CL8'VUPLH'          instruction name
000017C8  00001824                                    923+          DC     A(RE15+16)          address of v2 source
000017CC  00000010                                    924+          DC     A(16)               result length
000017D0  00001814                                    925+REA15     DC     A(RE15)             result address
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000017D8	00000000 00000000			926+	DS	FD	gap
000017E0	00000000 00000000			927+V1015	DS	XL16	V1 output
000017E8	00000000 00000000						
000017F0	00000000 00000000			928+	DS	FD	gap
				929+*			
000017F8				930+X15	DS	0F	
000017F8	E310 5010 0014		00000010	931+	LGF	R1,V2ADDR	load v2 source
000017FE	E761 0000 0806		00000000	932+	VL	v22,0(R1)	use v22 to test decoder
00001804	E766 0000 1CD5			933+	VUPLH	V22,V22,1	test instruction (dest is a source)
0000180A	E760 5028 080E		000017E0	934+	VST	V22,V1015	save v1 output
00001810	07FB			935+	BR	R11	return
00001814				936+RE15	DC	0F	xl16 expected result
00001814				937+	DROP	R5	
00001814	0000F1D2 0000C3F4			938	DC	XL16'0000F1D20000C3F4 0000F5C60000D7F8' result
0000181C	0000F5C6 0000D7F8						
00001824	F1D2C3F4 F5C6D7F8			939	DC	XL16'F1D2C3F4F5C6D7F8 ABABABABABABABAB' v2
0000182C	ABABABAB ABABABAB						
				940			
				941 * Word			
				942	VRR_A	VUPLH,2	
00001838				943+	DS	0FD	
00001838		00001838		944+	USING	*,R5	base for test data and test routine
00001838	00001878			945+T16	DC	A(X16)	address of test routine
0000183C	0010			946+	DC	H'16'	test number
0000183E	00			947+	DC	X'00'	
0000183F	02			948+	DC	HL1'2'	M3
00001840	E5E4D7D3 C8404040			949+	DC	CL8'VUPLH'	instruction name
00001848	000018A4			950+	DC	A(RE16+16)	address of v2 source
0000184C	00000010			951+	DC	A(16)	result length
00001850	00001894			952+REA16	DC	A(RE16)	result address
00001858	00000000 00000000			953+	DS	FD	gap
00001860	00000000 00000000			954+V1016	DS	XL16	V1 output
00001868	00000000 00000000						
00001870	00000000 00000000			955+	DS	FD	gap
				956+*			
00001878				957+X16	DS	0F	
00001878	E310 5010 0014		00000010	958+	LGF	R1,V2ADDR	load v2 source
0000187E	E761 0000 0806		00000000	959+	VL	v22,0(R1)	use v22 to test decoder
00001884	E766 0000 2CD5			960+	VUPLH	V22,V22,2	test instruction (dest is a source)
0000188A	E760 5028 080E		00001860	961+	VST	V22,V1016	save v1 output
00001890	07FB			962+	BR	R11	return
00001894				963+RE16	DC	0F	xl16 expected result
00001894				964+	DROP	R5	
00001894	00000000 11223344			965	DC	XL16'0000000011223344 0000000055667788' result
0000189C	00000000 55667788						
000018A4	11223344 55667788			966	DC	XL16'1122334455667788 ABABABABABABABAB' v2
000018AC	ABABABAB ABABABAB						
				967			
				968	VRR_A	VUPLH,2	
000018B8				969+	DS	0FD	
000018B8		000018B8		970+	USING	*,R5	base for test data and test routine
000018B8	000018F8			971+T17	DC	A(X17)	address of test routine
000018BC	0011			972+	DC	H'17'	test number
000018BE	00			973+	DC	X'00'	
000018BF	02			974+	DC	HL1'2'	M3
000018C0	E5E4D7D3 C8404040			975+	DC	CL8'VUPLH'	instruction name

```
  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

000018C8  00001924                                 976+          DC    A(RE17+16)         address of v2 source
000018CC  00000010                                 977+          DC    A(16)              result length
000018D0  00001914                                 978+REA17     DC    A(RE17)            result address
000018D8  00000000 00000000                        979+          DS    FD                 gap
000018E0  00000000 00000000                        980+V1017     DS    XL16               V1 output
000018E8  00000000 00000000
000018F0  00000000 00000000                        981+          DS    FD                 gap
                                                   982+*
000018F8                                           983+X17       DS    0F
000018F8  E310 5010 0014             00000010       984+          LGF   R1,V2ADDR          load v2 source
000018FE  E761 0000 0806             00000000       985+          VL    v22,0(R1)          use v22 to test decoder
00001904  E766 0000 2CD5                            986+          VUPLH V22,V22,2          test instruction (dest is a source)
0000190A  E760 5028 080E             000018E0       987+          VST   V22,V1017          save v1 output
00001910  07FB                                      988+          BR    R11                return
00001914                                            989+RE17      DC    0F                 xl16 expected result
00001914                                            990+          DROP  R5
00001914  00000000 F102C304                         991           DC    XL16'00000000F102C304 000000000506D7F8'     result
0000191C  00000000 0506D7F8
00001924  F102C304 0506D7F8                         992           DC    XL16'F102C3040506D7F8 ABABABABABABABAB'     v2
0000192C  ABABABAB ABABABAB

                                                   993
                                                   994           VRR_A VUPLH,2
00001938                                            995+          DS    0FD
00001938                          00001938          996+          USING *,R5              base for test data and test routine
00001938  00001978                                 997+T18       DC    A(X18)             address of test routine
0000193C  0012                                      998+          DC    H'18'              test number
0000193E  00                                        999+          DC    X'00'
0000193F  02                                       1000+          DC    HL1'2'             M3
00001940  E5E4D7D3 C8404040                        1001+          DC    CL8'VUPLH'         instruction name
00001948  000019A4                                 1002+          DC    A(RE18+16)         address of v2 source
0000194C  00000010                                 1003+          DC    A(16)              result length
00001950  00001994                                 1004+REA18     DC    A(RE18)            result address
00001958  00000000 00000000                        1005+          DS    FD                 gap
00001960  00000000 00000000                        1006+V1018     DS    XL16               V1 output
00001968  00000000 00000000
00001970  00000000 00000000                        1007+          DS    FD                 gap
                                                  1008+*
00001978                                          1009+X18       DS    0F
00001978  E310 5010 0014             00000010      1010+          LGF   R1,V2ADDR          load v2 source
0000197E  E761 0000 0806             00000000      1011+          VL    v22,0(R1)          use v22 to test decoder
00001984  E766 0000 2CD5                           1012+          VUPLH V22,V22,2          test instruction (dest is a source)
0000198A  E760 5028 080E             00001960      1013+          VST   V22,V1018          save v1 output
00001990  07FB                                     1014+          BR    R11                return
00001994                                           1015+RE18      DC    0F                 xl16 expected result
00001994                                           1016+          DROP  R5
00001994  00000000 F1D2C3F4                        1017           DC    XL16'00000000F1D2C3F4 00000000F5C6D7F8'     result
0000199C  00000000 F5C6D7F8
000019A4  F1D2C3F4 F5C6D7F8                         1018           DC    XL16'F1D2C3F4F5C6D7F8 ABABABABABABABAB'     v2
000019AC  ABABABAB ABABABAB

                                                  1019
                                                  1020 *-------------------------------------------------------------------
                                                  1021 * VUPL   - Vector Unpack Low
                                                  1022 *-------------------------------------------------------------------
                                                  1023 * Byte
                                                  1024           VRR_A VUPL,0
000019B8                                          1025+          DS    0FD
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000019B8		000019B8		1026+	USING	*,R5	base for test data and test routine
000019B8	000019F8			1027+T19	DC	A(X19)	address of test routine
000019BC	0013			1028+	DC	H'19'	test number
000019BE	00			1029+	DC	X'00'	
000019BF	00			1030+	DC	HL1'0'	M3
000019C0	E5E4D7D3 40404040			1031+	DC	CL8'VUPL'	instruction name
000019C8	00001A24			1032+	DC	A(RE19+16)	address of v2 source
000019CC	00000010			1033+	DC	A(16)	result length
000019D0	00001A14			1034+REA19	DC	A(RE19)	result address
000019D8	00000000 00000000			1035+	DS	FD	gap
000019E0	00000000 00000000			1036+V1019	DS	XL16	V1 output
000019E8	00000000 00000000						
000019F0	00000000 00000000			1037+	DS	FD	gap
				1038+*			
000019F8				1039+X19	DS	0F	
000019F8	E310 5010 0014		00000010	1040+	LGF	R1,V2ADDR	load v2 source
000019FE	E761 0000 0806		00000000	1041+	VL	v22,0(R1)	use v22 to test decoder
00001A04	E766 0000 0CD6			1042+	VUPL	V22,V22,0	test instruction (dest is a source)
00001A0A	E760 5028 080E		000019E0	1043+	VST	V22,V1019	save v1 output
00001A10	07FB			1044+	BR	R11	return
00001A14				1045+RE19	DC	0F	xl16 expected result
00001A14				1046+	DROP	R5	
00001A14	00110022 00330044			1047	DC	XL16'0011002200330044 005500660077FF88'	result
00001A1C	00550066 0077FF88						
00001A24	ABABABAB ABABABAB			1048	DC	XL16'ABABABABABABABAB 1122334455667788'	v2
00001A2C	11223344 55667788						
				1049			
				1050	VRR_A	VUPL,0	
00001A38				1051+	DS	0FD	
00001A38		00001A38		1052+	USING	*,R5	base for test data and test routine
00001A38	00001A78			1053+T20	DC	A(X20)	address of test routine
00001A3C	0014			1054+	DC	H'20'	test number
00001A3E	00			1055+	DC	X'00'	
00001A3F	00			1056+	DC	HL1'0'	M3
00001A40	E5E4D7D3 40404040			1057+	DC	CL8'VUPL'	instruction name
00001A48	00001AA4			1058+	DC	A(RE20+16)	address of v2 source
00001A4C	00000010			1059+	DC	A(16)	result length
00001A50	00001A94			1060+REA20	DC	A(RE20)	result address
00001A58	00000000 00000000			1061+	DS	FD	gap
00001A60	00000000 00000000			1062+V1020	DS	XL16	V1 output
00001A68	00000000 00000000						
00001A70	00000000 00000000			1063+	DS	FD	gap
				1064+*			
00001A78				1065+X20	DS	0F	
00001A78	E310 5010 0014		00000010	1066+	LGF	R1,V2ADDR	load v2 source
00001A7E	E761 0000 0806		00000000	1067+	VL	v22,0(R1)	use v22 to test decoder
00001A84	E766 0000 0CD6			1068+	VUPL	V22,V22,0	test instruction (dest is a source)
00001A8A	E760 5028 080E		00001A60	1069+	VST	V22,V1020	save v1 output
00001A90	07FB			1070+	BR	R11	return
00001A94				1071+RE20	DC	0F	xl16 expected result
00001A94				1072+	DROP	R5	
00001A94	FFF10002 FFC30004			1073	DC	XL16'FFF10002FFC30004 00050006FFD7FFF8'	result
00001A9C	00050006 FFD7FFF8						
00001AA4	ABABABAB ABABABAB			1074	DC	XL16'ABABABABABABABAB F102C3040506D7F8'	v2
00001AAC	F102C304 0506D7F8						
				1075			

```
  LOC         OBJECT CODE      ADDR1     ADDR2     STMT


                                                   1076          VRR_A VUPL,0
00001AB8                                           1077+         DS    0FD
00001AB8                       00001AB8            1078+         USING *,R5              base for test data and test routine
00001AB8   00001AF8                                1079+T21      DC    A(X21)            address of test routine
00001ABC   0015                                    1080+         DC    H'21'             test number
00001ABE   00                                      1081+         DC    X'00'
00001ABF   00                                      1082+         DC    HL1'0'            M3
00001AC0   E5E4D7D3 40404040                       1083+         DC    CL8'VUPL'         instruction name
00001AC8   00001B24                                1084+         DC    A(RE21+16)        address of v2 source
00001ACC   00000010                                1085+         DC    A(16)             result length
00001AD0   00001B14                                1086+REA21    DC    A(RE21)           result address
00001AD8   00000000 00000000                       1087+         DS    FD                gap
00001AE0   00000000 00000000                       1088+V1021    DS    XL16              V1 output
00001AE8   00000000 00000000
00001AF0   00000000 00000000                       1089+         DS    FD                gap
                                                   1090+*
00001AF8                                           1091+X21      DS    0F
00001AF8   E310 5010 0014              00000010    1092+         LGF   R1,V2ADDR         load v2 source
00001AFE   E761 0000 0806              00000000    1093+         VL    v22,0(R1)         use v22 to test decoder
00001B04   E766 0000 0CD6                          1094+         VUPL  V22,V22,0         test instruction (dest is a source)
00001B0A   E760 5028 080E              00001AE0    1095+         VST   V22,V1021         save v1 output
00001B10   07FB                                    1096+         BR    R11               return
00001B14                                           1097+RE21     DC    0F                xl16 expected result
00001B14                                           1098+         DROP  R5
00001B14   FFF1FFD2 FFC3FFF4                        1099         DC    XL16'FFF1FFD2FFC3FFF4 FFF5FFC6FFD7FFF8'     result
00001B1C   FFF5FFC6 FFD7FFF8
00001B24   ABABABAB ABABABAB                        1100         DC    XL16'ABABABABABABABAB F1D2C3F4F5C6D7F8'     v2
00001B2C   F1D2C3F4 F5C6D7F8

                                                   1101
                                                   1102 * Halfword
                                                   1103          VRR_A VUPL,1
00001B38                                           1104+         DS    0FD
00001B38                       00001B38            1105+         USING *,R5              base for test data and test routine
00001B38   00001B78                                1106+T22      DC    A(X22)            address of test routine
00001B3C   0016                                    1107+         DC    H'22'             test number
00001B3E   00                                      1108+         DC    X'00'
00001B3F   01                                      1109+         DC    HL1'1'            M3
00001B40   E5E4D7D3 40404040                       1110+         DC    CL8'VUPL'         instruction name
00001B48   00001BA4                                1111+         DC    A(RE22+16)        address of v2 source
00001B4C   00000010                                1112+         DC    A(16)             result length
00001B50   00001B94                                1113+REA22    DC    A(RE22)           result address
00001B58   00000000 00000000                       1114+         DS    FD                gap
00001B60   00000000 00000000                       1115+V1022    DS    XL16              V1 output
00001B68   00000000 00000000
00001B70   00000000 00000000                       1116+         DS    FD                gap
                                                   1117+*
00001B78                                           1118+X22      DS    0F
00001B78   E310 5010 0014              00000010    1119+         LGF   R1,V2ADDR         load v2 source
00001B7E   E761 0000 0806              00000000    1120+         VL    v22,0(R1)         use v22 to test decoder
00001B84   E766 0000 1CD6                          1121+         VUPL  V22,V22,1         test instruction (dest is a source)
00001B8A   E760 5028 080E              00001B60    1122+         VST   V22,V1022         save v1 output
00001B90   07FB                                    1123+         BR    R11               return
00001B94                                           1124+RE22     DC    0F                xl16 expected result
00001B94                                           1125+         DROP  R5
00001B94   00001122 00003344                        1126         DC    XL16'0000112200003344 0000556600007788'     result
00001B9C   00005566 00007788
```

```
  LOC          OBJECT CODE        ADDR1      ADDR2      STMT

00001BA4   ABABABAB  ABABABAB                           1127          DC     XL16'ABABABABABABABAB 1122334455667788'     v2
00001BAC   11223344  55667788

                                                        1128
                                                        1129          VRR_A  VUPL, 1
00001BB8                                                1130+         DS     0FD
00001BB8                         00001BB8               1131+         USING  *,R5                     base for test data and test routine
00001BB8   00001BF8                                     1132+T23      DC     A(X23)                   address of test routine
00001BBC   0017                                         1133+         DC     H'23'                    test number
00001BBE   00                                           1134+         DC     X'00'
00001BBF   01                                           1135+         DC     HL1'1'                   M3
00001BC0   E5E4D7D3  40404040                           1136+         DC     CL8'VUPL'                instruction name
00001BC8   00001C24                                     1137+         DC     A(RE23+16)               address of v2 source
00001BCC   00000010                                     1138+         DC     A(16)                    result length
00001BD0   00001C14                                     1139+REA23    DC     A(RE23)                  result address
00001BD8   00000000  00000000                           1140+         DS     FD                       gap
00001BE0   00000000  00000000                           1141+V1023    DS     XL16                     V1 output
00001BE8   00000000  00000000
00001BF0   00000000  00000000                           1142+         DS     FD                       gap
                                                        1143+*
00001BF8                                                1144+X23      DS     0F
00001BF8   E310 5010 0014                    00000010   1145+         LGF    R1,V2ADDR                load v2 source
00001BFE   E761 0000 0806                    00000000   1146+         VL     v22,0(R1)                use v22 to test decoder
00001C04   E766 0000 1CD6                               1147+         VUPL   V22,V22,1                test instruction (dest is a source)
00001C0A   E760 5028 080E                    00001BE0   1148+         VST    V22,V1023                save v1 output
00001C10   07FB                                         1149+         BR     R11                      return
00001C14                                                1150+RE23     DC     0F                       xl16 expected result
00001C14                                                1151+         DROP   R5
00001C14   FFFFF102  FFFFC304                            1152          DC     XL16'FFFFF102FFFFC304 00000506FFFFD7F8'     result
00001C1C   00000506  FFFFD7F8
00001C24   ABABABAB  ABABABAB                            1153          DC     XL16'ABABABABABABABAB F102C3040506D7F8'     v2
00001C2C   F102C304  0506D7F8
                                                        1154
                                                        1155          VRR_A  VUPL, 1
00001C38                                                1156+         DS     0FD
00001C38                         00001C38               1157+         USING  *,R5                     base for test data and test routine
00001C38   00001C78                                     1158+T24      DC     A(X24)                   address of test routine
00001C3C   0018                                         1159+         DC     H'24'                    test number
00001C3E   00                                           1160+         DC     X'00'
00001C3F   01                                           1161+         DC     HL1'1'                   M3
00001C40   E5E4D7D3  40404040                           1162+         DC     CL8'VUPL'                instruction name
00001C48   00001CA4                                     1163+         DC     A(RE24+16)               address of v2 source
00001C4C   00000010                                     1164+         DC     A(16)                    result length
00001C50   00001C94                                     1165+REA24    DC     A(RE24)                  result address
00001C58   00000000  00000000                           1166+         DS     FD                       gap
00001C60   00000000  00000000                           1167+V1024    DS     XL16                     V1 output
00001C68   00000000  00000000
00001C70   00000000  00000000                           1168+         DS     FD                       gap
                                                        1169+*
00001C78                                                1170+X24      DS     0F
00001C78   E310 5010 0014                    00000010   1171+         LGF    R1,V2ADDR                load v2 source
00001C7E   E761 0000 0806                    00000000   1172+         VL     v22,0(R1)                use v22 to test decoder
00001C84   E766 0000 1CD6                               1173+         VUPL   V22,V22,1                test instruction (dest is a source)
00001C8A   E760 5028 080E                    00001C60   1174+         VST    V22,V1024                save v1 output
00001C90   07FB                                         1175+         BR     R11                      return
00001C94                                                1176+RE24     DC     0F                       xl16 expected result
00001C94                                                1177+         DROP   R5
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001C94	FFFFF1D2 FFFFC3F4			1178	DC	XL16'FFFFF1D2FFFFC3F4 FFFFF5C6FFFFD7F8'	result	
00001C9C	FFFFF5C6 FFFFD7F8							
00001CA4	ABABABAB ABABABAB			1179	DC	XL16'ABABABABABABABAB F1D2C3F4F5C6D7F8'	v2	
00001CAC	F1D2C3F4 F5C6D7F8							
				1180				
				1181	* Word			
				1182	VRR_A	VUPL, 2		
00001CB8				1183+	DS	0FD		
00001CB8		00001CB8		1184+	USING	*, R5	base for test data and test routine	
00001CB8	00001CF8			1185+T25	DC	A(X25)	address of test routine	
00001CBC	0019			1186+	DC	H'25'	test number	
00001CBE	00			1187+	DC	X'00'		
00001CBF	02			1188+	DC	HL1'2'	M3	
00001CC0	E5E4D7D3 40404040			1189+	DC	CL8'VUPL'	instruction name	
00001CC8	00001D24			1190+	DC	A(RE25+16)	address of v2 source	
00001CCC	00000010			1191+	DC	A(16)	result length	
00001CD0	00001D14			1192+REA25	DC	A(RE25)	result address	
00001CD8	00000000 00000000			1193+	DS	FD	gap	
00001CE0	00000000 00000000			1194+V1025	DS	XL16	V1 output	
00001CE8	00000000 00000000							
00001CF0	00000000 00000000			1195+	DS	FD	gap	
				1196+*				
00001CF8				1197+X25	DS	0F		
00001CF8	E310 5010 0014		00000010	1198+	LGF	R1, V2ADDR	load v2 source	
00001CFE	E761 0000 0806		00000000	1199+	VL	v22, 0(R1)	use v22 to test decoder	
00001D04	E766 0000 2CD6			1200+	VUPL	V22, V22, 2	test instruction (dest is a source)	
00001D0A	E760 5028 080E		00001CE0	1201+	VST	V22, V1025	save v1 output	
00001D10	07FB			1202+	BR	R11	return	
00001D14				1203+RE25	DC	0F	xl16 expected result	
00001D14				1204+	DROP	R5		
00001D14	00000000 11223344			1205	DC	XL16'0000000011223344 0000000055667788'	result	
00001D1C	00000000 55667788							
00001D24	ABABABAB ABABABAB			1206	DC	XL16'ABABABABABABABAB 1122334455667788'	v2	
00001D2C	11223344 55667788							
				1207				
				1208	VRR_A	VUPL, 2		
00001D38				1209+	DS	0FD		
00001D38		00001D38		1210+	USING	*, R5	base for test data and test routine	
00001D38	00001D78			1211+T26	DC	A(X26)	address of test routine	
00001D3C	001A			1212+	DC	H'26'	test number	
00001D3E	00			1213+	DC	X'00'		
00001D3F	02			1214+	DC	HL1'2'	M3	
00001D40	E5E4D7D3 40404040			1215+	DC	CL8'VUPL'	instruction name	
00001D48	00001DA4			1216+	DC	A(RE26+16)	address of v2 source	
00001D4C	00000010			1217+	DC	A(16)	result length	
00001D50	00001D94			1218+REA26	DC	A(RE26)	result address	
00001D58	00000000 00000000			1219+	DS	FD	gap	
00001D60	00000000 00000000			1220+V1026	DS	XL16	V1 output	
00001D68	00000000 00000000							
00001D70	00000000 00000000			1221+	DS	FD	gap	
				1222+*				
00001D78				1223+X26	DS	0F		
00001D78	E310 5010 0014		00000010	1224+	LGF	R1, V2ADDR	load v2 source	
00001D7E	E761 0000 0806		00000000	1225+	VL	v22, 0(R1)	use v22 to test decoder	
00001D84	E766 0000 2CD6			1226+	VUPL	V22, V22, 2	test instruction (dest is a source)	
00001D8A	E760 5028 080E		00001D60	1227+	VST	V22, V1026	save v1 output	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001D90	07FB			1228+	BR	R11	return
00001D94				1229+RE26	DC	0F	xl16 expected result
00001D94				1230+	DROP	R5	
00001D94	FFFFFFFF F102C304			1231	DC	XL16'FFFFFFFFF102C304 000000000506D7F8'	result
00001D9C	00000000 0506D7F8						
00001DA4	ABABABAB ABABABAB			1232	DC	XL16'ABABABABABABABAB F102C3040506D7F8'	v2
00001DAC	F102C304 0506D7F8						
				1233			
00001DB8				1234	VRR_A	VUPL, 2	
00001DB8				1235+	DS	0FD	
00001DB8		00001DB8		1236+	USING	*, R5	base for test data and test routine
00001DB8	00001DF8			1237+T27	DC	A(X27)	address of test routine
00001DBC	001B			1238+	DC	H'27'	test number
00001DBE	00			1239+	DC	X'00'	
00001DBF	02			1240+	DC	HL1'2'	M3
00001DC0	E5E4D7D3 40404040			1241+	DC	CL8'VUPL'	instruction name
00001DC8	00001E24			1242+	DC	A(RE27+16)	address of v2 source
00001DCC	00000010			1243+	DC	A(16)	result length
00001DD0	00001E14			1244+REA27	DC	A(RE27)	result address
00001DD8	00000000 00000000			1245+	DS	FD	gap
00001DE0	00000000 00000000			1246+V1027	DS	XL16	V1 output
00001DE8	00000000 00000000						
00001DF0	00000000 00000000			1247+	DS	FD	gap
				1248+*			
00001DF8				1249+X27	DS	0F	
00001DF8	E310 5010 0014		00000010	1250+	LGF	R1, V2ADDR	load v2 source
00001DFE	E761 0000 0806		00000000	1251+	VL	v22, 0(R1)	use v22 to test decoder
00001E04	E766 0000 2CD6			1252+	VUPL	V22, V22, 2	test instruction (dest is a source)
00001E0A	E760 5028 080E		00001DE0	1253+	VST	V22, V1027	save v1 output
00001E10	07FB			1254+	BR	R11	return
00001E14				1255+RE27	DC	0F	xl16 expected result
00001E14				1256+	DROP	R5	
00001E14	FFFFFFFF F1D2C3F4			1257	DC	XL16'FFFFFFFFF1D2C3F4 FFFFFFFFF5C6D7F8'	result
00001E1C	FFFFFFFF F5C6D7F8						
00001E24	ABABABAB ABABABAB			1258	DC	XL16'ABABABABABABABAB F1D2C3F4F5C6D7F8'	v2
00001E2C	F1D2C3F4 F5C6D7F8						
				1259			
				1260	*---		
				1261	* VUPH - Vector Unpack High		
				1262	*---		
				1263	* Byte		
00001E38				1264	VRR_A	VUPH, 0	
00001E38				1265+	DS	0FD	
00001E38		00001E38		1266+	USING	*, R5	base for test data and test routine
00001E38	00001E78			1267+T28	DC	A(X28)	address of test routine
00001E3C	001C			1268+	DC	H'28'	test number
00001E3E	00			1269+	DC	X'00'	
00001E3F	00			1270+	DC	HL1'0'	M3
00001E40	E5E4D7C8 40404040			1271+	DC	CL8'VUPH'	instruction name
00001E48	00001EA4			1272+	DC	A(RE28+16)	address of v2 source
00001E4C	00000010			1273+	DC	A(16)	result length
00001E50	00001E94			1274+REA28	DC	A(RE28)	result address
00001E58	00000000 00000000			1275+	DS	FD	gap
00001E60	00000000 00000000			1276+V1028	DS	XL16	V1 output
00001E68	00000000 00000000						
00001E70	00000000 00000000			1277+	DS	FD	gap

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  LOC          OBJECT CODE       ADDR1      ADDR2      STMT

                                                       1278+*
00001E78                                               1279+X28       DS      0F
00001E78   E310 5010 0014                  00000010    1280+          LGF     R1,V2ADDR            load v2 source
00001E7E   E761 0000 0806                  00000000    1281+          VL      v22,0(R1)            use v22 to test decoder
00001E84   E766 0000 0CD7                               1282+          VUPH    V22,V22,0           test instruction (dest is a source)
00001E8A   E760 5028 080E                  00001E60    1283+          VST     V22,V1028           save v1 output
00001E90   07FB                                         1284+          BR      R11                 return
00001E94                                               1285+RE28      DC      0F                  xl16 expected result
00001E94                                               1286+          DROP    R5
00001E94   00110022 00330044                            1287           DC      XL16'0011002200330044 005500660077FF88'    result
00001E9C   00550066 0077FF88
00001EA4   11223344 55667788                            1288           DC      XL16'1122334455667788 ABABABABABABABAB'     v2
00001EAC   ABABABAB ABABABAB
                                                       1289
                                                       1290           VRR_A   VUPH,0
00001EB8                                               1291+          DS      0FD
00001EB8                                  00001EB8     1292+          USING   *,R5                base for test data and test routine
00001EB8   00001EF8                                   1293+T29        DC      A(X29)              address of test routine
00001EBC   001D                                       1294+          DC      H'29'               test number
00001EBE   00                                         1295+          DC      X'00'
00001EBF   00                                         1296+          DC      HL1'0'              M3
00001EC0   E5E4D7C8 40404040                            1297+          DC      CL8'VUPH'           instruction name
00001EC8   00001F24                                   1298+          DC      A(RE29+16)          address of v2 source
00001ECC   00000010                                   1299+          DC      A(16)               result length
00001ED0   00001F14                                   1300+REA29     DC      A(RE29)             result address
00001ED8   00000000 00000000                            1301+          DS      FD                  gap
00001EE0   00000000 00000000                            1302+V1029    DS      XL16                V1 output
00001EE8   00000000 00000000
00001EF0   00000000 00000000                            1303+          DS      FD                  gap
                                                       1304+*
00001EF8                                               1305+X29       DS      0F
00001EF8   E310 5010 0014                  00000010    1306+          LGF     R1,V2ADDR            load v2 source
00001EFE   E761 0000 0806                  00000000    1307+          VL      v22,0(R1)            use v22 to test decoder
00001F04   E766 0000 0CD7                               1308+          VUPH    V22,V22,0           test instruction (dest is a source)
00001F0A   E760 5028 080E                  00001EE0    1309+          VST     V22,V1029           save v1 output
00001F10   07FB                                         1310+          BR      R11                 return
00001F14                                               1311+RE29      DC      0F                  xl16 expected result
00001F14                                               1312+          DROP    R5
00001F14   FFF10002 FFC30004                            1313           DC      XL16'FFF10002FFC30004 00050006FFD7FFF8'    result
00001F1C   00050006 FFD7FFF8
00001F24   F102C304 0506D7F8                            1314           DC      XL16'F102C3040506D7F8 ABABABABABABABAB'     v2
00001F2C   ABABABAB ABABABAB
                                                       1315
                                                       1316           VRR_A   VUPH,0
00001F38                                               1317+          DS      0FD
00001F38                                  00001F38     1318+          USING   *,R5                base for test data and test routine
00001F38   00001F78                                   1319+T30        DC      A(X30)              address of test routine
00001F3C   001E                                       1320+          DC      H'30'               test number
00001F3E   00                                         1321+          DC      X'00'
00001F3F   00                                         1322+          DC      HL1'0'              M3
00001F40   E5E4D7C8 40404040                            1323+          DC      CL8'VUPH'           instruction name
00001F48   00001FA4                                   1324+          DC      A(RE30+16)          address of v2 source
00001F4C   00000010                                   1325+          DC      A(16)               result length
00001F50   00001F94                                   1326+REA30     DC      A(RE30)             result address
00001F58   00000000 00000000                            1327+          DS      FD                  gap
00001F60   00000000 00000000                            1328+V1030    DS      XL16                V1 output
```

```
  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

00001F68   00000000 00000000
00001F70   00000000 00000000            1329+            DS     FD              gap
                                        1330+*
00001F78                                1331+X30         DS     0F
00001F78   E310 5010 0014              00000010  1332+   LGF    R1,V2ADDR        load v2 source
00001F7E   E761 0000 0806              00000000  1333+   VL     v22,0(R1)        use v22 to test decoder
00001F84   E766 0000 0CD7                        1334+   VUPH   V22,V22,0        test instruction (dest is a source)
00001F8A   E760 5028 080E              00001F60  1335+   VST    V22,V1030        save v1 output
00001F90   07FB                                  1336+   BR     R11             return
00001F94                                1337+RE30         DC     0F              xl16 expected result
00001F94                                1338+            DROP   R5
00001F94   FFF1FFD2 FFC3FFF4            1339             DC     XL16'FFF1FFD2FFC3FFF4 FFF5FFC6FFD7FFF8'    result
00001F9C   FFF5FFC6 FFD7FFF8
00001FA4   F1D2C3F4 F5C6D7F8            1340             DC     XL16'F1D2C3F4F5C6D7F8 ABABABABABABABAB'    v2
00001FAC   ABABABAB ABABABAB
                                        1341
                                        1342 * Halfword
                                        1343             VRR_A  VUPH,1
00001FB8                                1344+            DS     0FD
00001FB8                      00001FB8  1345+            USING  *,R5            base for test data and test routine
00001FB8   00001FF8                     1346+T31         DC     A(X31)          address of test routine
00001FBC   001F                         1347+            DC     H'31'           test number
00001FBE   00                           1348+            DC     X'00'
00001FBF   01                           1349+            DC     HL1'1'          M3
00001FC0   E5E4D7C8 40404040            1350+            DC     CL8'VUPH'       instruction name
00001FC8   00002024                     1351+            DC     A(RE31+16)      address of v2 source
00001FCC   00000010                     1352+            DC     A(16)           result length
00001FD0   00002014                     1353+REA31       DC     A(RE31)         result address
00001FD8   00000000 00000000            1354+            DS     FD              gap
00001FE0   00000000 00000000            1355+V1031       DS     XL16            V1 output
00001FE8   00000000 00000000
00001FF0   00000000 00000000            1356+            DS     FD              gap
                                        1357+*
00001FF8                                1358+X31         DS     0F
00001FF8   E310 5010 0014              00000010  1359+   LGF    R1,V2ADDR       load v2 source
00001FFE   E761 0000 0806              00000000  1360+   VL     v22,0(R1)       use v22 to test decoder
00002004   E766 0000 1CD7                        1361+   VUPH   V22,V22,1       test instruction (dest is a source)
0000200A   E760 5028 080E              00001FE0  1362+   VST    V22,V1031       save v1 output
00002010   07FB                                  1363+   BR     R11             return
00002014                                1364+RE31         DC     0F              xl16 expected result
00002014                                1365+            DROP   R5
00002014   00001122 00003344            1366             DC     XL16'0000112200003344 0000556600007788'   result
0000201C   00005566 00007788
00002024   11223344 55667788            1367             DC     XL16'1122334455667788 ABABABABABABABAB'   v2
0000202C   ABABABAB ABABABAB
                                        1368
                                        1369             VRR_A  VUPH,1
00002038                                1370+            DS     0FD
00002038                      00002038  1371+            USING  *,R5            base for test data and test routine
00002038   00002078                     1372+T32         DC     A(X32)          address of test routine
0000203C   0020                         1373+            DC     H'32'           test number
0000203E   00                           1374+            DC     X'00'
0000203F   01                           1375+            DC     HL1'1'          M3
00002040   E5E4D7C8 40404040            1376+            DC     CL8'VUPH'       instruction name
00002048   000020A4                     1377+            DC     A(RE32+16)      address of v2 source
0000204C   00000010                     1378+            DC     A(16)           result length
```

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  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

00002050   00002094                             1379+REA32   DC    A(RE32)              result address
00002058   00000000 00000000                    1380+        DS    FD                   gap
00002060   00000000 00000000                    1381+V1032   DS    XL16                 V1 output
00002068   00000000 00000000
00002070   00000000 00000000                    1382+        DS    FD                   gap
                                                 1383+*
00002078                                         1384+X32     DS    0F
00002078   E310 5010 0014              00000010  1385+        LGF   R1,V2ADDR            load v2 source
0000207E   E761 0000 0806              00000000  1386+        VL    v22,0(R1)            use v22 to test decoder
00002084   E766 0000 1CD7                        1387+        VUPH  V22,V22,1            test instruction (dest is a source)
0000208A   E760 5028 080E              00002060  1388+        VST   V22,V1032            save v1 output
00002090   07FB                                  1389+        BR    R11                  return
00002094                                         1390+RE32    DC    0F                   xl16 expected result
00002094                                         1391+        DROP  R5
00002094   FFFFF102 FFFFC304                      1392         DC    XL16'FFFFF102FFFFC304 00000506FFFFD7F8'    result
0000209C   00000506 FFFFD7F8
000020A4   F102C304 0506D7F8                      1393         DC    XL16'F102C3040506D7F8 ABABABABABABABAB'    v2
000020AC   ABABABAB ABABABAB
                                                  1394
                                                  1395         VRR_A VUPH,1
000020B8                                          1396+        DS    0FD
000020B8                    000020B8              1397+        USING *,R5               base for test data and test routine
000020B8   000020F8                               1398+T33     DC    A(X33)               address of test routine
000020BC   0021                                   1399+        DC    H'33'                test number
000020BE   00                                     1400+        DC    X'00'
000020BF   01                                     1401+        DC    HL1'1'               M3
000020C0   E5E4D7C8 40404040                      1402+        DC    CL8'VUPH'            instruction name
000020C8   00002124                               1403+        DC    A(RE33+16)           address of v2 source
000020CC   00000010                               1404+        DC    A(16)                result length
000020D0   00002114                               1405+REA33   DC    A(RE33)              result address
000020D8   00000000 00000000                      1406+        DS    FD                   gap
000020E0   00000000 00000000                      1407+V1033   DS    XL16                 V1 output
000020E8   00000000 00000000
000020F0   00000000 00000000                      1408+        DS    FD                   gap
                                                  1409+*
000020F8                                          1410+X33     DS    0F
000020F8   E310 5010 0014              00000010   1411+        LGF   R1,V2ADDR            load v2 source
000020FE   E761 0000 0806              00000000   1412+        VL    v22,0(R1)            use v22 to test decoder
00002104   E766 0000 1CD7                         1413+        VUPH  V22,V22,1            test instruction (dest is a source)
0000210A   E760 5028 080E              000020E0   1414+        VST   V22,V1033            save v1 output
00002110   07FB                                   1415+        BR    R11                  return
00002114                                          1416+RE33    DC    0F                   xl16 expected result
00002114                                          1417+        DROP  R5
00002114   FFFFF1D2 FFFFC3F4                       1418         DC    XL16'FFFFF1D2FFFFC3F4 FFFFF5C6FFFFD7F8'    result
0000211C   FFFFF5C6 FFFFD7F8
00002124   F1D2C3F4 F5C6D7F8                       1419         DC    XL16'F1D2C3F4F5C6D7F8 ABABABABABABABAB'    v2
0000212C   ABABABAB ABABABAB
                                                   1420
                                                   1421 * Word
                                                   1422         VRR_A VUPH,2
00002138                                           1423+        DS    0FD
00002138                    00002138               1424+        USING *,R5               base for test data and test routine
00002138   00002178                                1425+T34     DC    A(X34)               address of test routine
0000213C   0022                                    1426+        DC    H'34'                test number
0000213E   00                                      1427+        DC    X'00'
0000213F   02                                      1428+        DC    HL1'2'               M3
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002140	E5E4D7C8 40404040			1429+	DC	CL8'VUPH'	instruction name
00002148	000021A4			1430+	DC	A(RE34+16)	address of v2 source
0000214C	00000010			1431+	DC	A(16)	result length
00002150	00002194			1432+REA34	DC	A(RE34)	result address
00002158	00000000 00000000			1433+	DS	FD	gap
00002160	00000000 00000000			1434+V1034	DS	XL16	V1 output
00002168	00000000 00000000						
00002170	00000000 00000000			1435+	DS	FD	gap
				1436+*			
00002178				1437+X34	DS	0F	
00002178	E310 5010 0014		00000010	1438+	LGF	R1,V2ADDR	load v2 source
0000217E	E761 0000 0806		00000000	1439+	VL	v22,0(R1)	use v22 to test decoder
00002184	E766 0000 2CD7			1440+	VUPH	V22,V22,2	test instruction (dest is a source)
0000218A	E760 5028 080E		00002160	1441+	VST	V22,V1034	save v1 output
00002190	07FB			1442+	BR	R11	return
00002194				1443+RE34	DC	0F	xl16 expected result
00002194				1444+	DROP	R5	
00002194	00000000 11223344			1445	DC	XL16'0000000011223344 0000000055667788'	result
0000219C	00000000 55667788						
000021A4	11223344 55667788			1446	DC	XL16'1122334455667788 ABABABABABABABAB'	v2
000021AC	ABABABAB ABABABAB						
				1447			
				1448	VRR_A	VUPH,2	
000021B8				1449+	DS	0FD	
000021B8		000021B8		1450+	USING	*,R5	base for test data and test routine
000021B8	000021F8			1451+T35	DC	A(X35)	address of test routine
000021BC	0023			1452+	DC	H'35'	test number
000021BE	00			1453+	DC	X'00'	
000021BF	02			1454+	DC	HL1'2'	M3
000021C0	E5E4D7C8 40404040			1455+	DC	CL8'VUPH'	instruction name
000021C8	00002224			1456+	DC	A(RE35+16)	address of v2 source
000021CC	00000010			1457+	DC	A(16)	result length
000021D0	00002214			1458+REA35	DC	A(RE35)	result address
000021D8	00000000 00000000			1459+	DS	FD	gap
000021E0	00000000 00000000			1460+V1035	DS	XL16	V1 output
000021E8	00000000 00000000						
000021F0	00000000 00000000			1461+	DS	FD	gap
				1462+*			
000021F8				1463+X35	DS	0F	
000021F8	E310 5010 0014		00000010	1464+	LGF	R1,V2ADDR	load v2 source
000021FE	E761 0000 0806		00000000	1465+	VL	v22,0(R1)	use v22 to test decoder
00002204	E766 0000 2CD7			1466+	VUPH	V22,V22,2	test instruction (dest is a source)
0000220A	E760 5028 080E		000021E0	1467+	VST	V22,V1035	save v1 output
00002210	07FB			1468+	BR	R11	return
00002214				1469+RE35	DC	0F	xl16 expected result
00002214				1470+	DROP	R5	
00002214	FFFFFFFF F102C304			1471	DC	XL16'FFFFFFFFF102C304 000000000506D7F8'	result
0000221C	00000000 0506D7F8						
00002224	F102C304 0506D7F8			1472	DC	XL16'F102C3040506D7F8 ABABABABABABABAB'	v2
0000222C	ABABABAB ABABABAB						
				1473			
				1474	VRR_A	VUPH,2	
00002238				1475+	DS	0FD	
00002238		00002238		1476+	USING	*,R5	base for test data and test routine
00002238	00002278			1477+T36	DC	A(X36)	address of test routine
0000223C	0024			1478+	DC	H'36'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000223E	00			1479+	DC	X'00'	
0000223F	02			1480+	DC	HL1'2'	M3
00002240	E5E4D7C8 40404040			1481+	DC	CL8'VUPH'	instruction name
00002248	000022A4			1482+	DC	A(RE36+16)	address of v2 source
0000224C	00000010			1483+	DC	A(16)	result length
00002250	00002294			1484+REA36	DC	A(RE36)	result address
00002258	00000000 00000000			1485+	DS	FD	gap
00002260	00000000 00000000			1486+V1036	DS	XL16	V1 output
00002268	00000000 00000000						
00002270	00000000 00000000			1487+	DS	FD	gap
				1488+*			
00002278				1489+X36	DS	0F	
00002278	E310 5010 0014		00000010	1490+	LGF	R1,V2ADDR	load v2 source
0000227E	E761 0000 0806		00000000	1491+	VL	v22,0(R1)	use v22 to test decoder
00002284	E766 0000 2CD7			1492+	VUPH	V22,V22,2	test instruction (dest is a source)
0000228A	E760 5028 080E		00002260	1493+	VST	V22,V1036	save v1 output
00002290	07FB			1494+	BR	R11	return
00002294				1495+RE36	DC	0F	xl16 expected result
00002294				1496+	DROP	R5	
00002294	FFFFFFFF F1D2C3F4			1497	DC	XL16'FFFFFFFFF1D2C3F4 FFFFFFFFF5C6D7F8' result	
0000229C	FFFFFFFF F5C6D7F8						
000022A4	F1D2C3F4 F5C6D7F8			1498	DC	XL16'F1D2C3F4F5C6D7F8 ABABABABABABABAB' v2	
000022AC	ABABABAB ABABABAB						
				1499			
				1500	*---		
				1501	* VSEG - Vector Sign Extend To Doubleword		
				1502	*---		
				1503	* Byte		
				1504		VRR_A	VSEG,0
000022B8				1505+	DS	0FD	
000022B8		000022B8		1506+	USING	*,R5	base for test data and test routine
000022B8	000022F8			1507+T37	DC	A(X37)	address of test routine
000022BC	0025			1508+	DC	H'37'	test number
000022BE	00			1509+	DC	X'00'	
000022BF	00			1510+	DC	HL1'0'	M3
000022C0	E5E2C5C7 40404040			1511+	DC	CL8'VSEG'	instruction name
000022C8	00002324			1512+	DC	A(RE37+16)	address of v2 source
000022CC	00000010			1513+	DC	A(16)	result length
000022D0	00002314			1514+REA37	DC	A(RE37)	result address
000022D8	00000000 00000000			1515+	DS	FD	gap
000022E0	00000000 00000000			1516+V1037	DS	XL16	V1 output
000022E8	00000000 00000000						
000022F0	00000000 00000000			1517+	DS	FD	gap
				1518+*			
000022F8				1519+X37	DS	0F	
000022F8	E310 5010 0014		00000010	1520+	LGF	R1,V2ADDR	load v2 source
000022FE	E761 0000 0806		00000000	1521+	VL	v22,0(R1)	use v22 to test decoder
00002304	E766 0000 0C5F			1522+	VSEG	V22,V22,0	test instruction (dest is a source)
0000230A	E760 5028 080E		000022E0	1523+	VST	V22,V1037	save v1 output
00002310	07FB			1524+	BR	R11	return
00002314				1525+RE37	DC	0F	xl16 expected result
00002314				1526+	DROP	R5	
00002314	00000000 0000000B			1527	DC	XL16'000000000000000B 0000000000000018' result	
0000231C	00000000 00000018						
00002324	ABABABAB ABABAB0B			1528	DC	XL16'ABABABABABABAB0B 1122334455667718' v2	
0000232C	11223344 55667718						

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  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

                                                1529
                                                1530          VRR_A VSEG, 0
00002338                                        1531+         DS    0FD
00002338                      00002338          1532+         USING *, R5              base for test data and test routine
00002338   00002378                             1533+T38      DC    A(X38)             address of test routine
0000233C   0026                                 1534+         DC    H'38'              test number
0000233E   00                                   1535+         DC    X'00'
0000233F   00                                   1536+         DC    HL1'0'             M3
00002340   E5E2C5C7 40404040                    1537+         DC    CL8'VSEG'          instruction name
00002348   000023A4                             1538+         DC    A(RE38+16)         address of v2 source
0000234C   00000010                             1539+         DC    A(16)              result length
00002350   00002394                             1540+REA38    DC    A(RE38)            result address
00002358   00000000 00000000                    1541+         DS    FD                 gap
00002360   00000000 00000000                    1542+V1038    DS    XL16               V1 output
00002368   00000000 00000000
00002370   00000000 00000000                    1543+         DS    FD                 gap
                                                1544+*
00002378                                        1545+X38      DS    0F
00002378   E310 5010 0014           00000010    1546+         LGF   R1, V2ADDR         load v2 source
0000237E   E761 0000 0806           00000000    1547+         VL    v22, 0(R1)         use v22 to test decoder
00002384   E766 0000 0C5F                        1548+         VSEG  V22, V22, 0        test instruction (dest is a source)
0000238A   E760 5028 080E           00002360    1549+         VST   V22, V1038         save v1 output
00002390   07FB                                 1550+         BR    R11                return
00002394                                        1551+RE38     DC    0F                 xl16 expected result
00002394                                        1552+         DROP  R5
00002394   00000000 0000000B                    1553          DC    XL16'000000000000000B FFFFFFFFFFFFFF88'     result
0000239C   FFFFFFFF FFFFFF88
000023A4   ABABABAB ABABAB0B                    1554          DC    XL16'ABABABABABABAB0B 1122334455667788'     v2
000023AC   11223344 55667788
                                                1555
                                                1556          VRR_A VSEG, 0
000023B8                                        1557+         DS    0FD
000023B8                      000023B8          1558+         USING *, R5              base for test data and test routine
000023B8   000023F8                             1559+T39      DC    A(X39)             address of test routine
000023BC   0027                                 1560+         DC    H'39'              test number
000023BE   00                                   1561+         DC    X'00'
000023BF   00                                   1562+         DC    HL1'0'             M3
000023C0   E5E2C5C7 40404040                    1563+         DC    CL8'VSEG'          instruction name
000023C8   00002424                             1564+         DC    A(RE39+16)         address of v2 source
000023CC   00000010                             1565+         DC    A(16)              result length
000023D0   00002414                             1566+REA39    DC    A(RE39)            result address
000023D8   00000000 00000000                    1567+         DS    FD                 gap
000023E0   00000000 00000000                    1568+V1039    DS    XL16               V1 output
000023E8   00000000 00000000
000023F0   00000000 00000000                    1569+         DS    FD                 gap
                                                1570+*
000023F8                                        1571+X39      DS    0F
000023F8   E310 5010 0014           00000010    1572+         LGF   R1, V2ADDR         load v2 source
000023FE   E761 0000 0806           00000000    1573+         VL    v22, 0(R1)         use v22 to test decoder
00002404   E766 0000 0C5F                        1574+         VSEG  V22, V22, 0        test instruction (dest is a source)
0000240A   E760 5028 080E           000023E0    1575+         VST   V22, V1039         save v1 output
00002410   07FB                                 1576+         BR    R11                return
00002414                                        1577+RE39     DC    0F                 xl16 expected result
00002414                                        1578+         DROP  R5
00002414   FFFFFFFF FFFFFFAB                    1579          DC    XL16'FFFFFFFFFFFFFFAB 0000000000000048'     result
0000241C   00000000 00000048
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002424	ABABABAB ABABABAB			1580	DC	XL16'ABABABABABABABAB 1122334455667748'	v2
0000242C	11223344 55667748						
				1581			
				1582	VRR_A	VSEG, 0	
00002438				1583+	DS	0FD	
00002438		00002438		1584+	USING	*, R5	base for test data and test routine
00002438	00002478			1585+T40	DC	A(X40)	address of test routine
0000243C	0028			1586+	DC	H'40'	test number
0000243E	00			1587+	DC	X'00'	
0000243F	00			1588+	DC	HL1'0'	M3
00002440	E5E2C5C7 40404040			1589+	DC	CL8'VSEG'	instruction name
00002448	000024A4			1590+	DC	A(RE40+16)	address of v2 source
0000244C	00000010			1591+	DC	A(16)	result length
00002450	00002494			1592+REA40	DC	A(RE40)	result address
00002458	00000000 00000000			1593+	DS	FD	gap
00002460	00000000 00000000			1594+V1040	DS	XL16	V1 output
00002468	00000000 00000000						
00002470	00000000 00000000			1595+	DS	FD	gap
				1596+*			
00002478				1597+X40	DS	0F	
00002478	E310 5010 0014		00000010	1598+	LGF	R1, V2ADDR	load v2 source
0000247E	E761 0000 0806		00000000	1599+	VL	v22, 0(R1)	use v22 to test decoder
00002484	E766 0000 0C5F			1600+	VSEG	V22, V22, 0	test instruction (dest is a source)
0000248A	E760 5028 080E		00002460	1601+	VST	V22, V1040	save v1 output
00002490	07FB			1602+	BR	R11	return
00002494				1603+RE40	DC	0F	xl16 expected result
00002494				1604+	DROP	R5	
00002494	FFFFFFFF FFFFFFAB			1605	DC	XL16'FFFFFFFFFFFFFFAB FFFFFFFFFFFFFFF8'	result
0000249C	FFFFFFFF FFFFFFF8						
000024A4	ABABABAB ABABABAB			1606	DC	XL16'ABABABABABABABAB F102C3040506D7F8'	v2
000024AC	F102C304 0506D7F8						
				1607			
				1608	* Halfword		
				1609	VRR_A	VSEG, 1	
000024B8				1610+	DS	0FD	
000024B8		000024B8		1611+	USING	*, R5	base for test data and test routine
000024B8	000024F8			1612+T41	DC	A(X41)	address of test routine
000024BC	0029			1613+	DC	H'41'	test number
000024BE	00			1614+	DC	X'00'	
000024BF	01			1615+	DC	HL1'1'	M3
000024C0	E5E2C5C7 40404040			1616+	DC	CL8'VSEG'	instruction name
000024C8	00002524			1617+	DC	A(RE41+16)	address of v2 source
000024CC	00000010			1618+	DC	A(16)	result length
000024D0	00002514			1619+REA41	DC	A(RE41)	result address
000024D8	00000000 00000000			1620+	DS	FD	gap
000024E0	00000000 00000000			1621+V1041	DS	XL16	V1 output
000024E8	00000000 00000000						
000024F0	00000000 00000000			1622+	DS	FD	gap
				1623+*			
000024F8				1624+X41	DS	0F	
000024F8	E310 5010 0014		00000010	1625+	LGF	R1, V2ADDR	load v2 source
000024FE	E761 0000 0806		00000000	1626+	VL	v22, 0(R1)	use v22 to test decoder
00002504	E766 0000 1C5F			1627+	VSEG	V22, V22, 1	test instruction (dest is a source)
0000250A	E760 5028 080E		000024E0	1628+	VST	V22, V1041	save v1 output
00002510	07FB			1629+	BR	R11	return
00002514				1630+RE41	DC	0F	xl16 expected result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002514				1631+	DROP	R5	
00002514	00000000 00000B0B			1632	DC	XL16'0000000000000B0B 0000000000007718'	result
0000251C	00000000 00007718						
00002524	ABABABAB ABAB0B0B			1633	DC	XL16'ABABABABABAB0B0B 1122334455667718'	v2
0000252C	11223344 55667718						
				1634			
				1635	VRR_A	VSEG, 1	
00002538				1636+	DS	0FD	
00002538		00002538		1637+	USING	*, R5	base for test data and test routine
00002538	00002578			1638+T42	DC	A(X42)	address of test routine
0000253C	002A			1639+	DC	H'42'	test number
0000253E	00			1640+	DC	X'00'	
0000253F	01			1641+	DC	HL1'1'	M3
00002540	E5E2C5C7 40404040			1642+	DC	CL8'VSEG'	instruction name
00002548	000025A4			1643+	DC	A(RE42+16)	address of v2 source
0000254C	00000010			1644+	DC	A(16)	result length
00002550	00002594			1645+REA42	DC	A(RE42)	result address
00002558	00000000 00000000			1646+	DS	FD	gap
00002560	00000000 00000000			1647+V1042	DS	XL16	V1 output
00002568	00000000 00000000						
00002570	00000000 00000000			1648+	DS	FD	gap
				1649+*			
00002578				1650+X42	DS	0F	
00002578	E310 5010 0014		00000010	1651+	LGF	R1, V2ADDR	load v2 source
0000257E	E761 0000 0806		00000000	1652+	VL	v22, 0(R1)	use v22 to test decoder
00002584	E766 0000 1C5F			1653+	VSEG	V22, V22, 1	test instruction (dest is a source)
0000258A	E760 5028 080E		00002560	1654+	VST	V22, V1042	save v1 output
00002590	07FB			1655+	BR	R11	return
00002594				1656+RE42	DC	0F	xl16 expected result
00002594				1657+	DROP	R5	
00002594	00000000 00001B0B			1658	DC	XL16'0000000000001B0B FFFFFFFFFFFFD788'	result
0000259C	FFFFFFFF FFFFD788						
000025A4	ABABABAB ABAB1B0B			1659	DC	XL16'ABABABABABAB1B0B 112233445566D788'	v2
000025AC	11223344 5566D788						
				1660			
				1661	VRR_A	VSEG, 1	
000025B8				1662+	DS	0FD	
000025B8		000025B8		1663+	USING	*, R5	base for test data and test routine
000025B8	000025F8			1664+T43	DC	A(X43)	address of test routine
000025BC	002B			1665+	DC	H'43'	test number
000025BE	00			1666+	DC	X'00'	
000025BF	01			1667+	DC	HL1'1'	M3
000025C0	E5E2C5C7 40404040			1668+	DC	CL8'VSEG'	instruction name
000025C8	00002624			1669+	DC	A(RE43+16)	address of v2 source
000025CC	00000010			1670+	DC	A(16)	result length
000025D0	00002614			1671+REA43	DC	A(RE43)	result address
000025D8	00000000 00000000			1672+	DS	FD	gap
000025E0	00000000 00000000			1673+V1043	DS	XL16	V1 output
000025E8	00000000 00000000						
000025F0	00000000 00000000			1674+	DS	FD	gap
				1675+*			
000025F8				1676+X43	DS	0F	
000025F8	E310 5010 0014		00000010	1677+	LGF	R1, V2ADDR	load v2 source
000025FE	E761 0000 0806		00000000	1678+	VL	v22, 0(R1)	use v22 to test decoder
00002604	E766 0000 1C5F			1679+	VSEG	V22, V22, 1	test instruction (dest is a source)
0000260A	E760 5028 080E		000025E0	1680+	VST	V22, V1043	save v1 output

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  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

00002610   07FB                                    1681+         BR    R11             return
00002614                                           1682+RE43     DC    0F              xl16 expected result
00002614                                           1683+         DROP  R5
00002614   FFFFFFFF FFFFABAB                        1684          DC    XL16'FFFFFFFFFFFFABAB 0000000000007748'    result
0000261C   00000000 00007748
00002624   ABABABAB ABABABAB                        1685          DC    XL16'ABABABABABABABAB 1122334455667748'    v2
0000262C   11223344 55667748
                                                    1686
                                                    1687         VRR_A VSEG, 1
00002638                                            1688+         DS    0FD
00002638                        00002638           1689+         USING *,R5           base for test data and test routine
00002638   00002678                                 1690+T44      DC    A(X44)          address of test routine
0000263C   002C                                     1691+         DC    H'44'           test number
0000263E   00                                       1692+         DC    X'00'
0000263F   01                                       1693+         DC    HL1'1'          M3
00002640   E5E2C5C7 40404040                        1694+         DC    CL8'VSEG'       instruction name
00002648   000026A4                                 1695+         DC    A(RE44+16)      address of v2 source
0000264C   00000010                                 1696+         DC    A(16)           result length
00002650   00002694                                 1697+REA44    DC    A(RE44)         result address
00002658   00000000 00000000                        1698+         DS    FD              gap
00002660   00000000 00000000                        1699+V1044    DS    XL16            V1 output
00002668   00000000 00000000
00002670   00000000 00000000                        1700+         DS    FD              gap
                                                    1701+*
00002678                                            1702+X44      DS    0F
00002678   E310 5010 0014               00000010    1703+         LGF   R1,V2ADDR       load v2 source
0000267E   E761 0000 0806               00000000    1704+         VL    v22,0(R1)       use v22 to test decoder
00002684   E766 0000 1C5F                           1705+         VSEG  V22,V22,1       test instruction (dest is a source)
0000268A   E760 5028 080E               00002660    1706+         VST   V22,V1044       save v1 output
00002690   07FB                                     1707+         BR    R11             return
00002694                                            1708+RE44     DC    0F              xl16 expected result
00002694                                            1709+         DROP  R5
00002694   FFFFFFFF FFFFABAB                        1710          DC    XL16'FFFFFFFFFFFFABAB FFFFFFFFFFFFC7F8'    result
0000269C   FFFFFFFF FFFFC7F8
000026A4   ABABABAB ABABABAB                        1711          DC    XL16'ABABABABABABABAB F102C3040506C7F8'    v2
000026AC   F102C304 0506C7F8
                                                    1712
                                                    1713 * Word
                                                    1714         VRR_A VSEG, 2
000026B8                                            1715+         DS    0FD
000026B8                        000026B8           1716+         USING *,R5           base for test data and test routine
000026B8   000026F8                                 1717+T45      DC    A(X45)          address of test routine
000026BC   002D                                     1718+         DC    H'45'           test number
000026BE   00                                       1719+         DC    X'00'
000026BF   02                                       1720+         DC    HL1'2'          M3
000026C0   E5E2C5C7 40404040                        1721+         DC    CL8'VSEG'       instruction name
000026C8   00002724                                 1722+         DC    A(RE45+16)      address of v2 source
000026CC   00000010                                 1723+         DC    A(16)           result length
000026D0   00002714                                 1724+REA45    DC    A(RE45)         result address
000026D8   00000000 00000000                        1725+         DS    FD              gap
000026E0   00000000 00000000                        1726+V1045    DS    XL16            V1 output
000026E8   00000000 00000000
000026F0   00000000 00000000                        1727+         DS    FD              gap
                                                    1728+*
000026F8                                            1729+X45      DS    0F
000026F8   E310 5010 0014               00000010    1730+         LGF   R1,V2ADDR       load v2 source
```

```
  LOC         OBJECT CODE      ADDR1     ADDR2      STMT

000026FE  E761 0000 0806              00000000  1731+          VL     v22,0(R1)        use v22 to test decoder
00002704  E766 0000 2C5F                        1732+          VSEG   V22,V22,2        test instruction (dest is a source)
0000270A  E760 5028 080E              000026E0  1733+          VST    V22,V1045        save v1 output
00002710  07FB                                  1734+          BR     R11              return
00002714                                        1735+RE45      DC     0F               xl16 expected result
00002714                                        1736+          DROP   R5
00002714  00000000 0B0B0B0B                     1737           DC     XL16'000000000B0B0B0B 0000000055667718'    result
0000271C  00000000 55667718
00002724  ABABABAB 0B0B0B0B                     1738           DC     XL16'ABABABAB0B0B0B0B 1122334455667718'    v2
0000272C  11223344 55667718
                                                1739
                                                1740           VRR_A  VSEG,2
00002738                                        1741+          DS     0FD
00002738                              00002738  1742+          USING  *,R5             base for test data and test routine
00002738  00002778                              1743+T46       DC     A(X46)           address of test routine
0000273C  002E                                  1744+          DC     H'46'            test number
0000273E  00                                    1745+          DC     X'00'
0000273F  02                                    1746+          DC     HL1'2'           M3
00002740  E5E2C5C7 40404040                     1747+          DC     CL8'VSEG'        instruction name
00002748  000027A4                              1748+          DC     A(RE46+16)       address of v2 source
0000274C  00000010                              1749+          DC     A(16)            result length
00002750  00002794                              1750+REA46     DC     A(RE46)          result address
00002758  00000000 00000000                     1751+          DS     FD               gap
00002760  00000000 00000000                     1752+V1046     DS     XL16             V1 output
00002768  00000000 00000000
00002770  00000000 00000000                     1753+          DS     FD               gap
                                                1754+*
00002778                                        1755+X46       DS     0F
00002778  E310 5010 0014              00000010  1756+          LGF    R1,V2ADDR        load v2 source
0000277E  E761 0000 0806              00000000  1757+          VL     v22,0(R1)        use v22 to test decoder
00002784  E766 0000 2C5F                        1758+          VSEG   V22,V22,2        test instruction (dest is a source)
0000278A  E760 5028 080E              00002760  1759+          VST    V22,V1046        save v1 output
00002790  07FB                                  1760+          BR     R11              return
00002794                                        1761+RE46      DC     0F               xl16 expected result
00002794                                        1762+          DROP   R5
00002794  00000000 1B0B1B0B                     1763           DC     XL16'000000001B0B1B0B FFFFFFFFC566D788'    result
0000279C  FFFFFFFF C566D788
000027A4  ABABABAB 1B0B1B0B                     1764           DC     XL16'ABABABAB1B0B1B0B 11223344C566D788'    v2
000027AC  11223344 C566D788
                                                1765
                                                1766           VRR_A  VSEG,2
000027B8                                        1767+          DS     0FD
000027B8                              000027B8  1768+          USING  *,R5             base for test data and test routine
000027B8  000027F8                              1769+T47       DC     A(X47)           address of test routine
000027BC  002F                                  1770+          DC     H'47'            test number
000027BE  00                                    1771+          DC     X'00'
000027BF  02                                    1772+          DC     HL1'2'           M3
000027C0  E5E2C5C7 40404040                     1773+          DC     CL8'VSEG'        instruction name
000027C8  00002824                              1774+          DC     A(RE47+16)       address of v2 source
000027CC  00000010                              1775+          DC     A(16)            result length
000027D0  00002814                              1776+REA47     DC     A(RE47)          result address
000027D8  00000000 00000000                     1777+          DS     FD               gap
000027E0  00000000 00000000                     1778+V1047     DS     XL16             V1 output
000027E8  00000000 00000000
000027F0  00000000 00000000                     1779+          DS     FD               gap
                                                1780+*
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000027F8				1781+X47	DS	0F	
000027F8	E310 5010 0014		00000010	1782+	LGF	R1,V2ADDR	load v2 source
000027FE	E761 0000 0806		00000000	1783+	VL	v22,0(R1)	use v22 to test decoder
00002804	E766 0000 2C5F			1784+	VSEG	V22,V22,2	test instruction (dest is a source)
0000280A	E760 5028 080E		000027E0	1785+	VST	V22,V1047	save v1 output
00002810	07FB			1786+	BR	R11	return
00002814				1787+RE47	DC	0F	xl16 expected result
00002814				1788+	DROP	R5	
00002814	FFFFFFFF ABABABAB			1789	DC	XL16'FFFFFFFFABABABAB 0000000055667748'	result
0000281C	00000000 55667748						
00002824	ABABABAB ABABABAB			1790	DC	XL16'ABABABABABABABAB 1122334455667748'	v2
0000282C	11223344 55667748						
				1791			
				1792	VRR_A	VSEG,2	
00002838				1793+	DS	0FD	
00002838		00002838		1794+	USING	*,R5	base for test data and test routine
00002838	00002878			1795+T48	DC	A(X48)	address of test routine
0000283C	0030			1796+	DC	H'48'	test number
0000283E	00			1797+	DC	X'00'	
0000283F	02			1798+	DC	HL1'2'	M3
00002840	E5E2C5C7 40404040			1799+	DC	CL8'VSEG'	instruction name
00002848	000028A4			1800+	DC	A(RE48+16)	address of v2 source
0000284C	00000010			1801+	DC	A(16)	result length
00002850	00002894			1802+REA48	DC	A(RE48)	result address
00002858	00000000 00000000			1803+	DS	FD	gap
00002860	00000000 00000000			1804+V1048	DS	XL16	V1 output
00002868	00000000 00000000						
00002870	00000000 00000000			1805+	DS	FD	gap
				1806+*			
00002878				1807+X48	DS	0F	
00002878	E310 5010 0014		00000010	1808+	LGF	R1,V2ADDR	load v2 source
0000287E	E761 0000 0806		00000000	1809+	VL	v22,0(R1)	use v22 to test decoder
00002884	E766 0000 2C5F			1810+	VSEG	V22,V22,2	test instruction (dest is a source)
0000288A	E760 5028 080E		00002860	1811+	VST	V22,V1048	save v1 output
00002890	07FB			1812+	BR	R11	return
00002894				1813+RE48	DC	0F	xl16 expected result
00002894				1814+	DROP	R5	
00002894	FFFFFFFF ABABABAB			1815	DC	XL16'FFFFFFFFABABABAB FFFFFFFFB506C7F8'	result
0000289C	FFFFFFFF B506C7F8						
000028A4	ABABABAB ABABABAB			1816	DC	XL16'ABABABABABABABAB F102C304B506C7F8'	v2
000028AC	F102C304 B506C7F8						
				1817			
				1818	*--		
				1819	* VLC - Vector Load Complement		
				1820	*--		
				1821	* Byte		
				1822	VRR_A	VLC,0	
000028B8				1823+	DS	0FD	
000028B8		000028B8		1824+	USING	*,R5	base for test data and test routine
000028B8	000028F8			1825+T49	DC	A(X49)	address of test routine
000028BC	0031			1826+	DC	H'49'	test number
000028BE	00			1827+	DC	X'00'	
000028BF	00			1828+	DC	HL1'0'	M3
000028C0	E5D3C340 40404040			1829+	DC	CL8'VLC'	instruction name
000028C8	00002924			1830+	DC	A(RE49+16)	address of v2 source
000028CC	00000010			1831+	DC	A(16)	result length

```
  LOC          OBJECT CODE       ADDR1     ADDR2     STMT

000028D0   00002914                                 1832+REA49   DC     A(RE49)              result address
000028D8   00000000 00000000                        1833+        DS     FD                   gap
000028E0   00000000 00000000                        1834+V1049   DS     XL16                 V1 output
000028E8   00000000 00000000
000028F0   00000000 00000000                        1835+        DS     FD                   gap
                                                    1836+*
000028F8                                            1837+X49     DS     0F
000028F8   E310 5010 0014              00000010     1838+        LGF    R1,V2ADDR            load v2 source
000028FE   E761 0000 0806              00000000     1839+        VL     v22,0(R1)            use v22 to test decoder
00002904   E766 0000 0CDE                           1840+        VLC    V22,V22,0            test instruction (dest is a source)
0000290A   E760 5028 080E              000028E0     1841+        VST    V22,V1049            save v1 output
00002910   07FB                                     1842+        BR     R11                  return
00002914                                            1843+RE49    DC     0F                   xl16 expected result
00002914                                            1844+        DROP   R5
00002914   00000000 00000000                        1845         DC     XL16'0000000000000000 0101010101010101'    result
0000291C   01010101 01010101
00002924   00000000 00000000                        1846         DC     XL16'0000000000000000 FFFFFFFFFFFFFFFF'    v2
0000292C   FFFFFFFF FFFFFFFF
                                                    1847
                                                    1848         VRR_A  VLC,0
00002938                                            1849+        DS     0FD
00002938                    00002938                1850+        USING  *,R5                 base for test data and test routine
00002938   00002978                                 1851+T50     DC     A(X50)               address of test routine
0000293C   0032                                     1852+        DC     H'50'                test number
0000293E   00                                       1853+        DC     X'00'
0000293F   00                                       1854+        DC     HL1'0'               M3
00002940   E5D3C340 40404040                        1855+        DC     CL8'VLC'             instruction name
00002948   000029A4                                 1856+        DC     A(RE50+16)           address of v2 source
0000294C   00000010                                 1857+        DC     A(16)                result length
00002950   00002994                                 1858+REA50   DC     A(RE50)              result address
00002958   00000000 00000000                        1859+        DS     FD                   gap
00002960   00000000 00000000                        1860+V1050   DS     XL16                 V1 output
00002968   00000000 00000000
00002970   00000000 00000000                        1861+        DS     FD                   gap
                                                    1862+*
00002978                                            1863+X50     DS     0F
00002978   E310 5010 0014              00000010     1864+        LGF    R1,V2ADDR            load v2 source
0000297E   E761 0000 0806              00000000     1865+        VL     v22,0(R1)            use v22 to test decoder
00002984   E766 0000 0CDE                           1866+        VLC    V22,V22,0            test instruction (dest is a source)
0000298A   E760 5028 080E              00002960     1867+        VST    V22,V1050            save v1 output
00002990   07FB                                     1868+        BR     R11                  return
00002994                                            1869+RE50    DC     0F                   xl16 expected result
00002994                                            1870+        DROP   R5
00002994   55555555 555555F5                        1871         DC     XL16'55555555555555F5 EFDECDBCAB9A89E8'    result
0000299C   EFDECDBC AB9A89E8
000029A4   ABABABAB ABABAB0B                        1872         DC     XL16'ABABABABABABAB0B 1122334455667718'    v2
000029AC   11223344 55667718
                                                    1873
                                                    1874         VRR_A  VLC,0
000029B8                                            1875+        DS     0FD
000029B8                    000029B8                1876+        USING  *,R5                 base for test data and test routine
000029B8   000029F8                                 1877+T51     DC     A(X51)               address of test routine
000029BC   0033                                     1878+        DC     H'51'                test number
000029BE   00                                       1879+        DC     X'00'
000029BF   00                                       1880+        DC     HL1'0'               M3
000029C0   E5D3C340 40404040                        1881+        DC     CL8'VLC'             instruction name
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000029C8	00002A24			1882+	DC	A(RE51+16)	address of v2 source	
000029CC	00000010			1883+	DC	A(16)	result length	
000029D0	00002A14			1884+REA51	DC	A(RE51)	result address	
000029D8	00000000 00000000			1885+	DS	FD	gap	
000029E0	00000000 00000000			1886+V1051	DS	XL16	V1 output	
000029E8	00000000 00000000							
000029F0	00000000 00000000			1887+	DS	FD	gap	
				1888+*				
000029F8				1889+X51	DS	0F		
000029F8	E310 5010 0014		00000010	1890+	LGF	R1,V2ADDR	load v2 source	
000029FE	E761 0000 0806		00000000	1891+	VL	v22,0(R1)	use v22 to test decoder	
00002A04	E766 0000 0CDE			1892+	VLC	V22,V22,0	test instruction (dest is a source)	
00002A0A	E760 5028 080E		000029E0	1893+	VST	V22,V1051	save v1 output	
00002A10	07FB			1894+	BR	R11	return	
00002A14				1895+RE51	DC	0F	xl16 expected result	
00002A14				1896+	DROP	R5		
00002A14	00FFFEFD FCFBFAF9			1897	DC	XL16'00FFFEFDFCFBFAF9 100F0E0D0C0B0A09'		result
00002A1C	100F0E0D 0C0B0A09							
00002A24	00010203 04050607			1898	DC	XL16'0001020304050607 F0F1F2F3F4F5F6F7'		v2
00002A2C	F0F1F2F3 F4F5F6F7							
				1899				
				1900	* Halfword			
				1901		VRR_A VLC,1		
00002A38				1902+	DS	0FD		
00002A38		00002A38		1903+	USING	*,R5	base for test data and test routine	
00002A38	00002A78			1904+T52	DC	A(X52)	address of test routine	
00002A3C	0034			1905+	DC	H'52'	test number	
00002A3E	00			1906+	DC	X'00'		
00002A3F	01			1907+	DC	HL1'1'	M3	
00002A40	E5D3C340 40404040			1908+	DC	CL8'VLC'	instruction name	
00002A48	00002AA4			1909+	DC	A(RE52+16)	address of v2 source	
00002A4C	00000010			1910+	DC	A(16)	result length	
00002A50	00002A94			1911+REA52	DC	A(RE52)	result address	
00002A58	00000000 00000000			1912+	DS	FD	gap	
00002A60	00000000 00000000			1913+V1052	DS	XL16	V1 output	
00002A68	00000000 00000000							
00002A70	00000000 00000000			1914+	DS	FD	gap	
				1915+*				
00002A78				1916+X52	DS	0F		
00002A78	E310 5010 0014		00000010	1917+	LGF	R1,V2ADDR	load v2 source	
00002A7E	E761 0000 0806		00000000	1918+	VL	v22,0(R1)	use v22 to test decoder	
00002A84	E766 0000 1CDE			1919+	VLC	V22,V22,1	test instruction (dest is a source)	
00002A8A	E760 5028 080E		00002A60	1920+	VST	V22,V1052	save v1 output	
00002A90	07FB			1921+	BR	R11	return	
00002A94				1922+RE52	DC	0F	xl16 expected result	
00002A94				1923+	DROP	R5		
00002A94	00000000 00000000			1924	DC	XL16'0000000000000000 0001000100010001'		result
00002A9C	00010001 00010001							
00002AA4	00000000 00000000			1925	DC	XL16'0000000000000000 FFFFFFFFFFFFFFFF'		v2
00002AAC	FFFFFFFF FFFFFFFF							
				1926				
				1927		VRR_A VLC,1		
00002AB8				1928+	DS	0FD		
00002AB8		00002AB8		1929+	USING	*,R5	base for test data and test routine	
00002AB8	00002AF8			1930+T53	DC	A(X53)	address of test routine	
00002ABC	0035			1931+	DC	H'53'	test number	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002ABE	00			1932+	DC	X'00'	
00002ABF	01			1933+	DC	HL1'1'	M3
00002AC0	E5D3C340 40404040			1934+	DC	CL8'VLC'	instruction name
00002AC8	00002B24			1935+	DC	A(RE53+16)	address of v2 source
00002ACC	00000010			1936+	DC	A(16)	result length
00002AD0	00002B14			1937+REA53	DC	A(RE53)	result address
00002AD8	00000000 00000000			1938+	DS	FD	gap
00002AE0	00000000 00000000			1939+V1053	DS	XL16	V1 output
00002AE8	00000000 00000000						
00002AF0	00000000 00000000			1940+	DS	FD	gap
				1941+*			
00002AF8				1942+X53	DS	0F	
00002AF8	E310 5010 0014		00000010	1943+	LGF	R1,V2ADDR	load v2 source
00002AFE	E761 0000 0806		00000000	1944+	VL	v22,0(R1)	use v22 to test decoder
00002B04	E766 0000 1CDE			1945+	VLC	V22,V22,1	test instruction (dest is a source)
00002B0A	E760 5028 080E		00002AE0	1946+	VST	V22,V1053	save v1 output
00002B10	07FB			1947+	BR	R11	return
00002B14				1948+RE53	DC	0F	xl16 expected result
00002B14				1949+	DROP	R5	
00002B14	54555455 545554F5			1950	DC	XL16'54555455545554F5 EEDECCBCAA9A88E8'	result
00002B1C	EEDECCBC AA9A88E8						
00002B24	ABABABAB ABABAB0B			1951	DC	XL16'ABABABABABABAB0B 1122334455667718'	v2
00002B2C	11223344 55667718						
				1952			
				1953	VRR_A	VLC,1	
00002B38				1954+	DS	0FD	
00002B38		00002B38		1955+	USING	*,R5	base for test data and test routine
00002B38	00002B78			1956+T54	DC	A(X54)	address of test routine
00002B3C	0036			1957+	DC	H'54'	test number
00002B3E	00			1958+	DC	X'00'	
00002B3F	01			1959+	DC	HL1'1'	M3
00002B40	E5D3C340 40404040			1960+	DC	CL8'VLC'	instruction name
00002B48	00002BA4			1961+	DC	A(RE54+16)	address of v2 source
00002B4C	00000010			1962+	DC	A(16)	result length
00002B50	00002B94			1963+REA54	DC	A(RE54)	result address
00002B58	00000000 00000000			1964+	DS	FD	gap
00002B60	00000000 00000000			1965+V1054	DS	XL16	V1 output
00002B68	00000000 00000000						
00002B70	00000000 00000000			1966+	DS	FD	gap
				1967+*			
00002B78				1968+X54	DS	0F	
00002B78	E310 5010 0014		00000010	1969+	LGF	R1,V2ADDR	load v2 source
00002B7E	E761 0000 0806		00000000	1970+	VL	v22,0(R1)	use v22 to test decoder
00002B84	E766 0000 1CDE			1971+	VLC	V22,V22,1	test instruction (dest is a source)
00002B8A	E760 5028 080E		00002B60	1972+	VST	V22,V1054	save v1 output
00002B90	07FB			1973+	BR	R11	return
00002B94				1974+RE54	DC	0F	xl16 expected result
00002B94				1975+	DROP	R5	
00002B94	FFFFFDFD FBFBF9F9			1976	DC	XL16'FFFFFDFDFBFBF9F9 0F0F0D0D0B0B0909'	result
00002B9C	0F0F0D0D 0B0B0909						
00002BA4	00010203 04050607			1977	DC	XL16'0001020304050607 F0F1F2F3F4F5F6F7'	v2
00002BAC	F0F1F2F3 F4F5F6F7						
				1978			
				1979 * Word			
				1980	VRR_A	VLC,2	
00002BB8				1981+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002BB8		00002BB8		1982+	USING	*,R5	base for test data and test routine
00002BB8	00002BF8			1983+T55	DC	A(X55)	address of test routine
00002BBC	0037			1984+	DC	H'55'	test number
00002BBE	00			1985+	DC	X'00'	
00002BBF	02			1986+	DC	HL1'2'	M3
00002BC0	E5D3C340 40404040			1987+	DC	CL8'VLC'	instruction name
00002BC8	00002C24			1988+	DC	A(RE55+16)	address of v2 source
00002BCC	00000010			1989+	DC	A(16)	result length
00002BD0	00002C14			1990+REA55	DC	A(RE55)	result address
00002BD8	00000000 00000000			1991+	DS	FD	gap
00002BE0	00000000 00000000			1992+V1055	DS	XL16	V1 output
00002BE8	00000000 00000000						
00002BF0	00000000 00000000			1993+	DS	FD	gap
				1994+*			
00002BF8				1995+X55	DS	0F	
00002BF8	E310 5010 0014		00000010	1996+	LGF	R1,V2ADDR	load v2 source
00002BFE	E761 0000 0806		00000000	1997+	VL	v22,0(R1)	use v22 to test decoder
00002C04	E766 0000 2CDE			1998+	VLC	V22,V22,2	test instruction (dest is a source)
00002C0A	E760 5028 080E		00002BE0	1999+	VST	V22,V1055	save v1 output
00002C10	07FB			2000+	BR	R11	return
00002C14				2001+RE55	DC	0F	xl16 expected result
00002C14				2002+	DROP	R5	
00002C14	00000000 00000000			2003	DC	XL16'0000000000000000 0000000100000001'	result
00002C1C	00000001 00000001						
00002C24	00000000 00000000			2004	DC	XL16'0000000000000000 FFFFFFFFFFFFFFFF'	v2
00002C2C	FFFFFFFF FFFFFFFF						
				2005			
				2006	VRR_A	VLC,2	
00002C38				2007+	DS	0FD	
00002C38		00002C38		2008+	USING	*,R5	base for test data and test routine
00002C38	00002C78			2009+T56	DC	A(X56)	address of test routine
00002C3C	0038			2010+	DC	H'56'	test number
00002C3E	00			2011+	DC	X'00'	
00002C3F	02			2012+	DC	HL1'2'	M3
00002C40	E5D3C340 40404040			2013+	DC	CL8'VLC'	instruction name
00002C48	00002CA4			2014+	DC	A(RE56+16)	address of v2 source
00002C4C	00000010			2015+	DC	A(16)	result length
00002C50	00002C94			2016+REA56	DC	A(RE56)	result address
00002C58	00000000 00000000			2017+	DS	FD	gap
00002C60	00000000 00000000			2018+V1056	DS	XL16	V1 output
00002C68	00000000 00000000						
00002C70	00000000 00000000			2019+	DS	FD	gap
				2020+*			
00002C78				2021+X56	DS	0F	
00002C78	E310 5010 0014		00000010	2022+	LGF	R1,V2ADDR	load v2 source
00002C7E	E761 0000 0806		00000000	2023+	VL	v22,0(R1)	use v22 to test decoder
00002C84	E766 0000 2CDE			2024+	VLC	V22,V22,2	test instruction (dest is a source)
00002C8A	E760 5028 080E		00002C60	2025+	VST	V22,V1056	save v1 output
00002C90	07FB			2026+	BR	R11	return
00002C94				2027+RE56	DC	0F	xl16 expected result
00002C94				2028+	DROP	R5	
00002C94	54545455 545454F5			2029	DC	XL16'54545455545454F5 EEDDCCBCAA9988E8'	result
00002C9C	EEDDCCBC AA9988E8						
00002CA4	ABABABAB ABABAB0B			2030	DC	XL16'ABABABABABABAB0B 1122334455667718'	v2
00002CAC	11223344 55667718						
				2031			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				2032		VRR_A VLC, 2	
00002CB8				2033+	DS	0FD	
00002CB8		00002CB8		2034+	USING	*, R5	base for test data and test routine
00002CB8	00002CF8			2035+T57	DC	A(X57)	address of test routine
00002CBC	0039			2036+	DC	H'57'	test number
00002CBE	00			2037+	DC	X'00'	
00002CBF	02			2038+	DC	HL1'2'	M3
00002CC0	E5D3C340 40404040			2039+	DC	CL8'VLC'	instruction name
00002CC8	00002D24			2040+	DC	A(RE57+16)	address of v2 source
00002CCC	00000010			2041+	DC	A(16)	result length
00002CD0	00002D14			2042+REA57	DC	A(RE57)	result address
00002CD8	00000000 00000000			2043+	DS	FD	gap
00002CE0	00000000 00000000			2044+V1057	DS	XL16	V1 output
00002CE8	00000000 00000000						
00002CF0	00000000 00000000			2045+	DS	FD	gap
				2046+*			
00002CF8				2047+X57	DS	0F	
00002CF8	E310 5010 0014		00000010	2048+	LGF	R1, V2ADDR	load v2 source
00002CFE	E761 0000 0806		00000000	2049+	VL	v22, 0(R1)	use v22 to test decoder
00002D04	E766 0000 2CDE			2050+	VLC	V22, V22, 2	test instruction (dest is a source)
00002D0A	E760 5028 080E		00002CE0	2051+	VST	V22, V1057	save v1 output
00002D10	07FB			2052+	BR	R11	return
00002D14				2053+RE57	DC	0F	xl16 expected result
00002D14				2054+	DROP	R5	
00002D14	FFFEFDFD FBFAF9F9			2055	DC	XL16'FFFEFDFDFBFAF9F9 0F0E0D0D0B0A0909' result	
00002D1C	0F0E0D0D 0B0A0909						
00002D24	00010203 04050607			2056	DC	XL16'0001020304050607 F0F1F2F3F4F5F6F7' v2	
00002D2C	F0F1F2F3 F4F5F6F7						
				2057			
				2058	* Doubleword		
				2059		VRR_A VLC, 3	
00002D38				2060+	DS	0FD	
00002D38		00002D38		2061+	USING	*, R5	base for test data and test routine
00002D38	00002D78			2062+T58	DC	A(X58)	address of test routine
00002D3C	003A			2063+	DC	H'58'	test number
00002D3E	00			2064+	DC	X'00'	
00002D3F	03			2065+	DC	HL1'3'	M3
00002D40	E5D3C340 40404040			2066+	DC	CL8'VLC'	instruction name
00002D48	00002DA4			2067+	DC	A(RE58+16)	address of v2 source
00002D4C	00000010			2068+	DC	A(16)	result length
00002D50	00002D94			2069+REA58	DC	A(RE58)	result address
00002D58	00000000 00000000			2070+	DS	FD	gap
00002D60	00000000 00000000			2071+V1058	DS	XL16	V1 output
00002D68	00000000 00000000						
00002D70	00000000 00000000			2072+	DS	FD	gap
				2073+*			
00002D78				2074+X58	DS	0F	
00002D78	E310 5010 0014		00000010	2075+	LGF	R1, V2ADDR	load v2 source
00002D7E	E761 0000 0806		00000000	2076+	VL	v22, 0(R1)	use v22 to test decoder
00002D84	E766 0000 3CDE			2077+	VLC	V22, V22, 3	test instruction (dest is a source)
00002D8A	E760 5028 080E		00002D60	2078+	VST	V22, V1058	save v1 output
00002D90	07FB			2079+	BR	R11	return
00002D94				2080+RE58	DC	0F	xl16 expected result
00002D94				2081+	DROP	R5	
00002D94	00000000 00000000			2082	DC	XL16'0000000000000000 0000000000000001' result	
00002D9C	00000000 00000001						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002DA4	00000000 00000000			2083	DC	XL16'000000000000000 FFFFFFFFFFFFFFFF'	v2
00002DAC	FFFFFFFF FFFFFFFF						
				2084			
				2085	VRR_A	VLC,3	
00002DB8				2086+	DS	0FD	
00002DB8		00002DB8		2087+	USING	*,R5	base for test data and test routine
00002DB8	00002DF8			2088+T59	DC	A(X59)	address of test routine
00002DBC	003B			2089+	DC	H'59'	test number
00002DBE	00			2090+	DC	X'00'	
00002DBF	03			2091+	DC	HL1'3'	M3
00002DC0	E5D3C340 40404040			2092+	DC	CL8'VLC'	instruction name
00002DC8	00002E24			2093+	DC	A(RE59+16)	address of v2 source
00002DCC	00000010			2094+	DC	A(16)	result length
00002DD0	00002E14			2095+REA59	DC	A(RE59)	result address
00002DD8	00000000 00000000			2096+	DS	FD	gap
00002DE0	00000000 00000000			2097+V1059	DS	XL16	V1 output
00002DE8	00000000 00000000						
00002DF0	00000000 00000000			2098+	DS	FD	gap
				2099+*			
00002DF8				2100+X59	DS	0F	
00002DF8	E310 5010 0014		00000010	2101+	LGF	R1,V2ADDR	load v2 source
00002DFE	E761 0000 0806		00000000	2102+	VL	v22,0(R1)	use v22 to test decoder
00002E04	E766 0000 3CDE			2103+	VLC	V22,V22,3	test instruction (dest is a source)
00002E0A	E760 5028 080E		00002DE0	2104+	VST	V22,V1059	save v1 output
00002E10	07FB			2105+	BR	R11	return
00002E14				2106+RE59	DC	0F	xl16 expected result
00002E14				2107+	DROP	R5	
00002E14	54545454 545454F5			2108	DC	XL16'54545454545454F5 EEDDCCBBAA9988E8'	result
00002E1C	EEDDCCBB AA9988E8						
00002E24	ABABABAB ABABAB0B			2109	DC	XL16'ABABABABABABAB0B 1122334455667718'	v2
00002E2C	11223344 55667718						
				2110			
				2111	VRR_A	VLC,3	
00002E38				2112+	DS	0FD	
00002E38		00002E38		2113+	USING	*,R5	base for test data and test routine
00002E38	00002E78			2114+T60	DC	A(X60)	address of test routine
00002E3C	003C			2115+	DC	H'60'	test number
00002E3E	00			2116+	DC	X'00'	
00002E3F	03			2117+	DC	HL1'3'	M3
00002E40	E5D3C340 40404040			2118+	DC	CL8'VLC'	instruction name
00002E48	00002EA4			2119+	DC	A(RE60+16)	address of v2 source
00002E4C	00000010			2120+	DC	A(16)	result length
00002E50	00002E94			2121+REA60	DC	A(RE60)	result address
00002E58	00000000 00000000			2122+	DS	FD	gap
00002E60	00000000 00000000			2123+V1060	DS	XL16	V1 output
00002E68	00000000 00000000						
00002E70	00000000 00000000			2124+	DS	FD	gap
				2125+*			
00002E78				2126+X60	DS	0F	
00002E78	E310 5010 0014		00000010	2127+	LGF	R1,V2ADDR	load v2 source
00002E7E	E761 0000 0806		00000000	2128+	VL	v22,0(R1)	use v22 to test decoder
00002E84	E766 0000 3CDE			2129+	VLC	V22,V22,3	test instruction (dest is a source)
00002E8A	E760 5028 080E		00002E60	2130+	VST	V22,V1060	save v1 output
00002E90	07FB			2131+	BR	R11	return
00002E94				2132+RE60	DC	0F	xl16 expected result
00002E94				2133+	DROP	R5	

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  LOC          OBJECT CODE        ADDR1      ADDR2      STMT

00002E94  FFFEFDFC FBFAF9F9                            2134         DC      XL16'FFFEFDFCFBFAF9F9 0F0E0D0C0B0A0909'      result
00002E9C  0F0E0D0C 0B0A0909
00002EA4  00010203 04050607                            2135         DC      XL16'0001020304050607 F0F1F2F3F4F5F6F7'      v2
00002EAC  F0F1F2F3 F4F5F6F7
                                                       2136
                                                       2137 *-----------------------------------------------------------------
                                                       2138 * VLP     - Vector Load Positive
                                                       2139 *-----------------------------------------------------------------
                                                       2140 * Byte
                                                       2141         VRR_A VLP,0
00002EB8                                               2142+        DS      0FD
00002EB8                          00002EB8             2143+        USING  *,R5                  base for test data and test routine
00002EB8  00002EF8                                     2144+T61     DC      A(X61)               address of test routine
00002EBC  003D                                         2145+        DC      H'61'                test number
00002EBE  00                                           2146+        DC      X'00'
00002EBF  00                                           2147+        DC      HL1'0'               M3
00002EC0  E5D3D740 40404040                            2148+        DC      CL8'VLP'             instruction name
00002EC8  00002F24                                     2149+        DC      A(RE61+16)           address of v2 source
00002ECC  00000010                                     2150+        DC      A(16)                result length
00002ED0  00002F14                                     2151+REA61   DC      A(RE61)              result address
00002ED8  00000000 00000000                            2152+        DS      FD                   gap
00002EE0  00000000 00000000                            2153+V1061   DS      XL16                 V1 output
00002EE8  00000000 00000000
00002EF0  00000000 00000000                            2154+        DS      FD                   gap
                                                       2155+*
00002EF8                                               2156+X61     DS      0F
00002EF8  E310 5010 0014                    00000010   2157+        LGF     R1,V2ADDR            load v2 source
00002EFE  E761 0000 0806                    00000000   2158+        VL      v22,0(R1)            use v22 to test decoder
00002F04  E766 0000 0CDF                               2159+        VLP     V22,V22,0           test instruction (dest is a source)
00002F0A  E760 5028 080E                    00002EE0   2160+        VST     V22,V1061           save v1 output
00002F10  07FB                                         2161+        BR      R11                  return
00002F14                                               2162+RE61    DC      0F                   xl16 expected result
00002F14                                               2163+        DROP   R5
00002F14  00000000 00000000                            2164         DC      XL16'0000000000000000 0101010101010101'      result
00002F1C  01010101 01010101
00002F24  00000000 00000000                            2165         DC      XL16'0000000000000000 FFFFFFFFFFFFFFFF'      v2
00002F2C  FFFFFFFF FFFFFFFF
                                                       2166
                                                       2167         VRR_A VLP,0
00002F38                                               2168+        DS      0FD
00002F38                          00002F38             2169+        USING  *,R5                  base for test data and test routine
00002F38  00002F78                                     2170+T62     DC      A(X62)               address of test routine
00002F3C  003E                                         2171+        DC      H'62'                test number
00002F3E  00                                           2172+        DC      X'00'
00002F3F  00                                           2173+        DC      HL1'0'               M3
00002F40  E5D3D740 40404040                            2174+        DC      CL8'VLP'             instruction name
00002F48  00002FA4                                     2175+        DC      A(RE62+16)           address of v2 source
00002F4C  00000010                                     2176+        DC      A(16)                result length
00002F50  00002F94                                     2177+REA62   DC      A(RE62)              result address
00002F58  00000000 00000000                            2178+        DS      FD                   gap
00002F60  00000000 00000000                            2179+V1062   DS      XL16                 V1 output
00002F68  00000000 00000000
00002F70  00000000 00000000                            2180+        DS      FD                   gap
                                                       2181+*
00002F78                                               2182+X62     DS      0F
00002F78  E310 5010 0014                    00000010   2183+        LGF     R1,V2ADDR            load v2 source
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  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

00002F7E  E761 0000 0806                 00000000  2184+          VL     v22,0(R1)              use v22 to test decoder
00002F84  E766 0000 0CDF                           2185+          VLP    V22,V22,0              test instruction (dest is a source)
00002F8A  E760 5028 080E                 00002F60  2186+          VST    V22,V1062              save v1 output
00002F90  07FB                                     2187+          BR     R11                    return
00002F94                                           2188+RE62      DC     0F                     xl16 expected result
00002F94                                           2189+          DROP   R5
00002F94  55555555 5555550B                        2190           DC     XL16'555555555555550B 1122334455667718'    result
00002F9C  11223344 55667718
00002FA4  ABABABAB ABABAB0B                        2191           DC     XL16'ABABABABABABAB0B 1122334455667718'    v2
00002FAC  11223344 55667718
                                                   2192
00002FB8                                           2193           VRR_A VLP,0
00002FB8                                           2194+          DS     0FD
00002FB8                       00002FB8            2195+          USING  *,R5                   base for test data and test routine
00002FB8  00002FF8                                 2196+T63       DC     A(X63)                 address of test routine
00002FBC  003F                                     2197+          DC     H'63'                  test number
00002FBE  00                                       2198+          DC     X'00'
00002FBF  00                                       2199+          DC     HL1'0'                 M3
00002FC0  E5D3D740 40404040                        2200+          DC     CL8'VLP'               instruction name
00002FC8  00003024                                 2201+          DC     A(RE63+16)             address of v2 source
00002FCC  00000010                                 2202+          DC     A(16)                  result length
00002FD0  00003014                                 2203+REA63     DC     A(RE63)                result address
00002FD8  00000000 00000000                        2204+          DS     FD                     gap
00002FE0  00000000 00000000                        2205+V1063     DS     XL16                   V1 output
00002FE8  00000000 00000000
00002FF0  00000000 00000000                        2206+          DS     FD                     gap
                                                   2207+*
00002FF8                                           2208+X63       DS     0F
00002FF8  E310 5010 0014                 00000010  2209+          LGF    R1,V2ADDR              load v2 source
00002FFE  E761 0000 0806                 00000000  2210+          VL     v22,0(R1)              use v22 to test decoder
00003004  E766 0000 0CDF                           2211+          VLP    V22,V22,0              test instruction (dest is a source)
0000300A  E760 5028 080E                 00002FE0  2212+          VST    V22,V1063              save v1 output
00003010  07FB                                     2213+          BR     R11                    return
00003014                                           2214+RE63      DC     0F                     xl16 expected result
00003014                                           2215+          DROP   R5
00003014  00010203 04050607                        2216           DC     XL16'0001020304050607 100F0E0D0C0B0A09'    result
0000301C  100F0E0D 0C0B0A09
00003024  00010203 04050607                        2217           DC     XL16'0001020304050607 F0F1F2F3F4F5F6F7'    v2
0000302C  F0F1F2F3 F4F5F6F7
                                                   2218
                                                   2219 * Halfword
                                                   2220           VRR_A VLP,1
00003038                                           2221+          DS     0FD
00003038                       00003038            2222+          USING  *,R5                   base for test data and test routine
00003038  00003078                                 2223+T64       DC     A(X64)                 address of test routine
0000303C  0040                                     2224+          DC     H'64'                  test number
0000303E  00                                       2225+          DC     X'00'
0000303F  01                                       2226+          DC     HL1'1'                 M3
00003040  E5D3D740 40404040                        2227+          DC     CL8'VLP'               instruction name
00003048  000030A4                                 2228+          DC     A(RE64+16)             address of v2 source
0000304C  00000010                                 2229+          DC     A(16)                  result length
00003050  00003094                                 2230+REA64     DC     A(RE64)                result address
00003058  00000000 00000000                        2231+          DS     FD                     gap
00003060  00000000 00000000                        2232+V1064     DS     XL16                   V1 output
00003068  00000000 00000000
00003070  00000000 00000000                        2233+          DS     FD                     gap
```

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  LOC          OBJECT CODE      ADDR1     ADDR2     STMT


                                                    2234+*
00003078                                            2235+X64         DS      0F
00003078   E310 5010 0014              00000010     2236+            LGF     R1,V2ADDR       load v2 source
0000307E   E761 0000 0806              00000000     2237+            VL      v22,0(R1)       use v22 to test decoder
00003084   E766 0000 1CDF                           2238+            VLP     V22,V22,1       test instruction (dest is a source)
0000308A   E760 5028 080E              00003060     2239+            VST     V22,V1064       save v1 output
00003090   07FB                                     2240+            BR      R11             return
00003094                                            2241+RE64        DC      0F              xl16 expected result
00003094                                            2242+            DROP    R5
00003094   00000000 00000000                        2243             DC      XL16'0000000000000000 0001000100010001'    result
0000309C   00010001 00010001
000030A4   00000000 00000000                        2244             DC      XL16'0000000000000000 FFFFFFFFFFFFFFFF'    v2
000030AC   FFFFFFFF FFFFFFFF

                                                    2245
                                                    2246             VRR_A VLP,1
000030B8                                            2247+            DS      0FD
000030B8                          000030B8          2248+            USING *,R5              base for test data and test routine
000030B8   000030F8                                 2249+T65         DC      A(X65)          address of test routine
000030BC   0041                                     2250+            DC      H'65'           test number
000030BE   00                                       2251+            DC      X'00'
000030BF   01                                       2252+            DC      HL1'1'          M3
000030C0   E5D3D740 40404040                        2253+            DC      CL8'VLP'        instruction name
000030C8   00003124                                 2254+            DC      A(RE65+16)      address of v2 source
000030CC   00000010                                 2255+            DC      A(16)           result length
000030D0   00003114                                 2256+REA65       DC      A(RE65)         result address
000030D8   00000000 00000000                        2257+            DS      FD              gap
000030E0   00000000 00000000                        2258+V1065       DS      XL16            V1 output
000030E8   00000000 00000000
000030F0   00000000 00000000                        2259+            DS      FD              gap
                                                    2260+*
000030F8                                            2261+X65         DS      0F
000030F8   E310 5010 0014              00000010     2262+            LGF     R1,V2ADDR       load v2 source
000030FE   E761 0000 0806              00000000     2263+            VL      v22,0(R1)       use v22 to test decoder
00003104   E766 0000 1CDF                           2264+            VLP     V22,V22,1       test instruction (dest is a source)
0000310A   E760 5028 080E              000030E0     2265+            VST     V22,V1065       save v1 output
00003110   07FB                                     2266+            BR      R11             return
00003114                                            2267+RE65        DC      0F              xl16 expected result
00003114                                            2268+            DROP    R5
00003114   54555455 545554F5                        2269             DC      XL16'54555455545554F5 1122334455667718'    result
0000311C   11223344 55667718
00003124   ABABABAB ABABAB0B                        2270             DC      XL16'ABABABABABABAB0B 1122334455667718'    v2
0000312C   11223344 55667718
                                                    2271
                                                    2272             VRR_A VLP,1
00003138                                            2273+            DS      0FD
00003138                          00003138          2274+            USING *,R5              base for test data and test routine
00003138   00003178                                 2275+T66         DC      A(X66)          address of test routine
0000313C   0042                                     2276+            DC      H'66'           test number
0000313E   00                                       2277+            DC      X'00'
0000313F   01                                       2278+            DC      HL1'1'          M3
00003140   E5D3D740 40404040                        2279+            DC      CL8'VLP'        instruction name
00003148   000031A4                                 2280+            DC      A(RE66+16)      address of v2 source
0000314C   00000010                                 2281+            DC      A(16)           result length
00003150   00003194                                 2282+REA66       DC      A(RE66)         result address
00003158   00000000 00000000                        2283+            DS      FD              gap
00003160   00000000 00000000                        2284+V1066       DS      XL16            V1 output
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  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

00003168   00000000 00000000
00003170   00000000 00000000          2285+         DS    FD            gap
                                       2286+*
00003178                               2287+X66      DS    0F
00003178   E310 5010 0014            00000010  2288+         LGF   R1,V2ADDR     load v2 source
0000317E   E761 0000 0806            00000000  2289+         VL    v22,0(R1)     use v22 to test decoder
00003184   E766 0000 1CDF                       2290+         VLP   V22,V22,1     test instruction (dest is a source)
0000318A   E760 5028 080E            00003160  2291+         VST   V22,V1066     save v1 output
00003190   07FB                                 2292+         BR    R11           return
00003194                               2293+RE66     DC    0F            xl16 expected result
00003194                               2294+         DROP  R5
00003194   00010203 04050607          2295          DC    XL16'0001020304050607 0F0F0D0D0B0B0909'    result
0000319C   0F0F0D0D 0B0B0909
000031A4   00010203 04050607          2296          DC    XL16'0001020304050607 F0F1F2F3F4F5F6F7'    v2
000031AC   F0F1F2F3 F4F5F6F7
                                       2297
                                       2298 * Word
                                       2299          VRR_A VLP,2
000031B8                               2300+         DS    0FD
000031B8                     000031B8  2301+         USING *,R5            base for test data and test routine
000031B8   000031F8                    2302+T67      DC    A(X67)         address of test routine
000031BC   0043                        2303+         DC    H'67'          test number
000031BE   00                          2304+         DC    X'00'
000031BF   02                          2305+         DC    HL1'2'         M3
000031C0   E5D3D740 40404040           2306+         DC    CL8'VLP'       instruction name
000031C8   00003224                    2307+         DC    A(RE67+16)     address of v2 source
000031CC   00000010                    2308+         DC    A(16)          result length
000031D0   00003214                    2309+REA67    DC    A(RE67)        result address
000031D8   00000000 00000000           2310+         DS    FD            gap
000031E0   00000000 00000000           2311+V1067    DS    XL16          V1 output
000031E8   00000000 00000000
000031F0   00000000 00000000           2312+         DS    FD            gap
                                       2313+*
000031F8                               2314+X67      DS    0F
000031F8   E310 5010 0014            00000010  2315+         LGF   R1,V2ADDR     load v2 source
000031FE   E761 0000 0806            00000000  2316+         VL    v22,0(R1)     use v22 to test decoder
00003204   E766 0000 2CDF                       2317+         VLP   V22,V22,2     test instruction (dest is a source)
0000320A   E760 5028 080E            000031E0  2318+         VST   V22,V1067     save v1 output
00003210   07FB                                 2319+         BR    R11           return
00003214                               2320+RE67     DC    0F            xl16 expected result
00003214                               2321+         DROP  R5
00003214   00000000 00000000           2322          DC    XL16'0000000000000000 0000000100000001'    result
0000321C   00000001 00000001
00003224   00000000 00000000           2323          DC    XL16'0000000000000000 FFFFFFFFFFFFFFFF'    v2
0000322C   FFFFFFFF FFFFFFFF
                                       2324
                                       2325          VRR_A VLP,2
00003238                               2326+         DS    0FD
00003238                     00003238  2327+         USING *,R5            base for test data and test routine
00003238   00003278                    2328+T68      DC    A(X68)         address of test routine
0000323C   0044                        2329+         DC    H'68'          test number
0000323E   00                          2330+         DC    X'00'
0000323F   02                          2331+         DC    HL1'2'         M3
00003240   E5D3D740 40404040           2332+         DC    CL8'VLP'       instruction name
00003248   000032A4                    2333+         DC    A(RE68+16)     address of v2 source
0000324C   00000010                    2334+         DC    A(16)          result length
```

```
   LOC        OBJECT CODE        ADDR1     ADDR2     STMT

00003250   00003294                                 2335+REA68   DC     A(RE68)           result address
00003258   00000000 00000000                        2336+        DS     FD                gap
00003260   00000000 00000000                        2337+V1068   DS     XL16              V1 output
00003268   00000000 00000000
00003270   00000000 00000000                        2338+        DS     FD                gap
                                                     2339+*
00003278                                             2340+X68     DS     0F
00003278   E310 5010 0014            00000010        2341+        LGF    R1,V2ADDR         load v2 source
0000327E   E761 0000 0806            00000000        2342+        VL     v22,0(R1)         use v22 to test decoder
00003284   E766 0000 2CDF                            2343+        VLP    V22,V22,2         test instruction (dest is a source)
0000328A   E760 5028 080E            00003260        2344+        VST    V22,V1068         save v1 output
00003290   07FB                                      2345+        BR     R11               return
00003294                                             2346+RE68    DC     0F                xl16 expected result
00003294                                             2347+        DROP   R5
00003294   54545455 545454F5                         2348         DC     XL16'54545455545454F5 1122334455667718'    result
0000329C   11223344 55667718
000032A4   ABABABAB ABABAB0B                         2349         DC     XL16'ABABABABABABAB0B 1122334455667718'    v2
000032AC   11223344 55667718
                                                     2350
                                                     2351         VRR_A  VLP,2
000032B8                                             2352+        DS     0FD
000032B8                      000032B8               2353+        USING  *,R5              base for test data and test routine
000032B8   000032F8                                  2354+T69     DC     A(X69)            address of test routine
000032BC   0045                                      2355+        DC     H'69'             test number
000032BE   00                                        2356+        DC     X'00'
000032BF   02                                        2357+        DC     HL1'2'            M3
000032C0   E5D3D740 40404040                         2358+        DC     CL8'VLP'          instruction name
000032C8   00003324                                  2359+        DC     A(RE69+16)        address of v2 source
000032CC   00000010                                  2360+        DC     A(16)             result length
000032D0   00003314                                  2361+REA69   DC     A(RE69)           result address
000032D8   00000000 00000000                         2362+        DS     FD                gap
000032E0   00000000 00000000                         2363+V1069   DS     XL16              V1 output
000032E8   00000000 00000000
000032F0   00000000 00000000                         2364+        DS     FD                gap
                                                     2365+*
000032F8                                             2366+X69     DS     0F
000032F8   E310 5010 0014            00000010        2367+        LGF    R1,V2ADDR         load v2 source
000032FE   E761 0000 0806            00000000        2368+        VL     v22,0(R1)         use v22 to test decoder
00003304   E766 0000 2CDF                            2369+        VLP    V22,V22,2         test instruction (dest is a source)
0000330A   E760 5028 080E            000032E0        2370+        VST    V22,V1069         save v1 output
00003310   07FB                                      2371+        BR     R11               return
00003314                                             2372+RE69    DC     0F                xl16 expected result
00003314                                             2373+        DROP   R5
00003314   00010203 04050607                         2374         DC     XL16'0001020304050607 0F0E0D0D0B0A0909'    result
0000331C   0F0E0D0D 0B0A0909
00003324   00010203 04050607                         2375         DC     XL16'0001020304050607 F0F1F2F3F4F5F6F7'    v2
0000332C   F0F1F2F3 F4F5F6F7
                                                     2376
                                                     2377 * Doubleword
                                                     2378         VRR_A  VLP,3
00003338                                             2379+        DS     0FD
00003338                      00003338               2380+        USING  *,R5              base for test data and test routine
00003338   00003378                                  2381+T70     DC     A(X70)            address of test routine
0000333C   0046                                      2382+        DC     H'70'             test number
0000333E   00                                        2383+        DC     X'00'
0000333F   03                                        2384+        DC     HL1'3'            M3
```

```
   LOC          OBJECT CODE      ADDR1      ADDR2      STMT

00003340   E5D3D740 40404040                          2385+          DC      CL8'VLP'              instruction name
00003348   000033A4                                   2386+          DC      A(RE70+16)            address of v2 source
0000334C   00000010                                   2387+          DC      A(16)                 result length
00003350   00003394                                   2388+REA70     DC      A(RE70)               result address
00003358   00000000 00000000                          2389+          DS      FD                    gap
00003360   00000000 00000000                          2390+V1070     DS      XL16                  V1 output
00003368   00000000 00000000
00003370   00000000 00000000                          2391+          DS      FD                    gap
                                                      2392+*
00003378                                              2393+X70       DS      0F
00003378   E310 5010 0014                  00000010   2394+          LGF     R1,V2ADDR             load v2 source
0000337E   E761 0000 0806                  00000000   2395+          VL      v22,0(R1)             use v22 to test decoder
00003384   E766 0000 3CDF                             2396+          VLP     V22,V22,3             test instruction (dest is a source)
0000338A   E760 5028 080E                  00003360   2397+          VST     V22,V1070             save v1 output
00003390   07FB                                       2398+          BR      R11                   return
00003394                                              2399+RE70      DC      0F                    xl16 expected result
00003394                                              2400+          DROP    R5
00003394   00000000 00000000                          2401           DC      XL16'0000000000000000 0000000000000001'    result
0000339C   00000000 00000001
000033A4   00000000 00000000                          2402           DC      XL16'0000000000000000 FFFFFFFFFFFFFFFF'     v2
000033AC   FFFFFFFF FFFFFFFF
                                                      2403
                                                      2404           VRR_A VLP,3
000033B8                                              2405+          DS      0FD
000033B8                            000033B8           2406+          USING   *,R5                  base for test data and test routine
000033B8   000033F8                                   2407+T71       DC      A(X71)                address of test routine
000033BC   0047                                       2408+          DC      H'71'                 test number
000033BE   00                                         2409+          DC      X'00'
000033BF   03                                         2410+          DC      HL1'3'                M3
000033C0   E5D3D740 40404040                          2411+          DC      CL8'VLP'              instruction name
000033C8   00003424                                   2412+          DC      A(RE71+16)            address of v2 source
000033CC   00000010                                   2413+          DC      A(16)                 result length
000033D0   00003414                                   2414+REA71     DC      A(RE71)               result address
000033D8   00000000 00000000                          2415+          DS      FD                    gap
000033E0   00000000 00000000                          2416+V1071     DS      XL16                  V1 output
000033E8   00000000 00000000
000033F0   00000000 00000000                          2417+          DS      FD                    gap
                                                      2418+*
000033F8                                              2419+X71       DS      0F
000033F8   E310 5010 0014                  00000010   2420+          LGF     R1,V2ADDR             load v2 source
000033FE   E761 0000 0806                  00000000   2421+          VL      v22,0(R1)             use v22 to test decoder
00003404   E766 0000 3CDF                             2422+          VLP     V22,V22,3             test instruction (dest is a source)
0000340A   E760 5028 080E                  000033E0   2423+          VST     V22,V1071             save v1 output
00003410   07FB                                       2424+          BR      R11                   return
00003414                                              2425+RE71      DC      0F                    xl16 expected result
00003414                                              2426+          DROP    R5
00003414   54545454 545454F5                          2427           DC      XL16'54545454545454F5 1122334455667718'    result
0000341C   11223344 55667718
00003424   ABABABAB ABABAB0B                          2428           DC      XL16'ABABABABABABAB0B 1122334455667718'     v2
0000342C   11223344 55667718
                                                      2429
                                                      2430           VRR_A VLP,3
00003438                                              2431+          DS      0FD
00003438                            00003438           2432+          USING   *,R5                  base for test data and test routine
00003438   00003478                                   2433+T72       DC      A(X72)                address of test routine
0000343C   0048                                       2434+          DC      H'72'                 test number
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000343E	00			2435+	DC	X'00'	
0000343F	03			2436+	DC	HL1'3'	M3
00003440	E5D3D740 40404040			2437+	DC	CL8'VLP'	instruction name
00003448	000034A4			2438+	DC	A(RE72+16)	address of v2 source
0000344C	00000010			2439+	DC	A(16)	result length
00003450	00003494			2440+REA72	DC	A(RE72)	result address
00003458	00000000 00000000			2441+	DS	FD	gap
00003460	00000000 00000000			2442+V1072	DS	XL16	V1 output
00003468	00000000 00000000						
00003470	00000000 00000000			2443+	DS	FD	gap
				2444+*			
00003478				2445+X72	DS	0F	
00003478	E310 5010 0014		00000010	2446+	LGF	R1,V2ADDR	load v2 source
0000347E	E761 0000 0806		00000000	2447+	VL	v22,0(R1)	use v22 to test decoder
00003484	E766 0000 3CDF			2448+	VLP	V22,V22,3	test instruction (dest is a source)
0000348A	E760 5028 080E		00003460	2449+	VST	V22,V1072	save v1 output
00003490	07FB			2450+	BR	R11	return
00003494				2451+RE72	DC	0F	xl16 expected result
00003494				2452+	DROP	R5	
00003494	00010203 04050607			2453	DC	XL16'0001020304050607 0F0E0D0C0B0A0909' result	
0000349C	0F0E0D0C 0B0A0909						
000034A4	00010203 04050607			2454	DC	XL16'0001020304050607 F0F1F2F3F4F5F6F7' v2	
000034AC	F0F1F2F3 F4F5F6F7						
				2455			
				2456			
				2457			
000034B4	00000000			2458	DC	F'0' END OF TABLE	
000034B8	00000000			2459	DC	F'0'	
				2460 *			
				2461 * table of pointers to individual load test			
				2462 *			
000034BC				2463 E7TESTS	DS	0F	
				2464	PTTABLE		
000034BC				2465+TTABLE	DS	0F	
000034BC	000010B8			2466+	DC	A(T1)	
000034C0	00001138			2467+	DC	A(T2)	
000034C4	000011B8			2468+	DC	A(T3)	
000034C8	00001238			2469+	DC	A(T4)	
000034CC	000012B8			2470+	DC	A(T5)	
000034D0	00001338			2471+	DC	A(T6)	
000034D4	000013B8			2472+	DC	A(T7)	
000034D8	00001438			2473+	DC	A(T8)	
000034DC	000014B8			2474+	DC	A(T9)	
000034E0	00001538			2475+	DC	A(T10)	
000034E4	000015B8			2476+	DC	A(T11)	
000034E8	00001638			2477+	DC	A(T12)	
000034EC	000016B8			2478+	DC	A(T13)	
000034F0	00001738			2479+	DC	A(T14)	
000034F4	000017B8			2480+	DC	A(T15)	
000034F8	00001838			2481+	DC	A(T16)	
000034FC	000018B8			2482+	DC	A(T17)	
00003500	00001938			2483+	DC	A(T18)	
00003504	000019B8			2484+	DC	A(T19)	
00003508	00001A38			2485+	DC	A(T20)	
0000350C	00001AB8			2486+	DC	A(T21)	
00003510	00001B38			2487+	DC	A(T22)	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00003514	00001BB8			2488+	DC	A(T23)
00003518	00001C38			2489+	DC	A(T24)
0000351C	00001CB8			2490+	DC	A(T25)
00003520	00001D38			2491+	DC	A(T26)
00003524	00001DB8			2492+	DC	A(T27)
00003528	00001E38			2493+	DC	A(T28)
0000352C	00001EB8			2494+	DC	A(T29)
00003530	00001F38			2495+	DC	A(T30)
00003534	00001FB8			2496+	DC	A(T31)
00003538	00002038			2497+	DC	A(T32)
0000353C	000020B8			2498+	DC	A(T33)
00003540	00002138			2499+	DC	A(T34)
00003544	000021B8			2500+	DC	A(T35)
00003548	00002238			2501+	DC	A(T36)
0000354C	000022B8			2502+	DC	A(T37)
00003550	00002338			2503+	DC	A(T38)
00003554	000023B8			2504+	DC	A(T39)
00003558	00002438			2505+	DC	A(T40)
0000355C	000024B8			2506+	DC	A(T41)
00003560	00002538			2507+	DC	A(T42)
00003564	000025B8			2508+	DC	A(T43)
00003568	00002638			2509+	DC	A(T44)
0000356C	000026B8			2510+	DC	A(T45)
00003570	00002738			2511+	DC	A(T46)
00003574	000027B8			2512+	DC	A(T47)
00003578	00002838			2513+	DC	A(T48)
0000357C	000028B8			2514+	DC	A(T49)
00003580	00002938			2515+	DC	A(T50)
00003584	000029B8			2516+	DC	A(T51)
00003588	00002A38			2517+	DC	A(T52)
0000358C	00002AB8			2518+	DC	A(T53)
00003590	00002B38			2519+	DC	A(T54)
00003594	00002BB8			2520+	DC	A(T55)
00003598	00002C38			2521+	DC	A(T56)
0000359C	00002CB8			2522+	DC	A(T57)
000035A0	00002D38			2523+	DC	A(T58)
000035A4	00002DB8			2524+	DC	A(T59)
000035A8	00002E38			2525+	DC	A(T60)
000035AC	00002EB8			2526+	DC	A(T61)
000035B0	00002F38			2527+	DC	A(T62)
000035B4	00002FB8			2528+	DC	A(T63)
000035B8	00003038			2529+	DC	A(T64)
000035BC	000030B8			2530+	DC	A(T65)
000035C0	00003138			2531+	DC	A(T66)
000035C4	000031B8			2532+	DC	A(T67)
000035C8	00003238			2533+	DC	A(T68)
000035CC	000032B8			2534+	DC	A(T69)
000035D0	00003338			2535+	DC	A(T70)
000035D4	000033B8			2536+	DC	A(T71)
000035D8	00003438			2537+	DC	A(T72)
				2538+*		
000035DC	00000000			2539+	DC	A(0) END OF TABLE
000035E0	00000000			2540+	DC	A(0) END OF TABLE
				2541		
000035E4	00000000			2542	DC	F'0' END OF TABLE
000035E8	00000000			2543	DC	F'0'

```
LOC          OBJECT CODE      ADDR1      ADDR2      STMT

                                                    2545 ****************************************************************************
                                                    2546 *          Register equates
                                                    2547 ****************************************************************************

                              00000000   00000001   2549 R0        EQU    0
                              00000001   00000001   2550 R1        EQU    1
                              00000002   00000001   2551 R2        EQU    2
                              00000003   00000001   2552 R3        EQU    3
                              00000004   00000001   2553 R4        EQU    4
                              00000005   00000001   2554 R5        EQU    5
                              00000006   00000001   2555 R6        EQU    6
                              00000007   00000001   2556 R7        EQU    7
                              00000008   00000001   2557 R8        EQU    8
                              00000009   00000001   2558 R9        EQU    9
                              0000000A   00000001   2559 R10       EQU    10
                              0000000B   00000001   2560 R11       EQU    11
                              0000000C   00000001   2561 R12       EQU    12
                              0000000D   00000001   2562 R13       EQU    13
                              0000000E   00000001   2563 R14       EQU    14
                              0000000F   00000001   2564 R15       EQU    15




                                                    2566 ****************************************************************************
                                                    2567 *          Register equates
                                                    2568 ****************************************************************************

                              00000000   00000001   2570 V0        EQU    0
                              00000001   00000001   2571 V1        EQU    1
                              00000002   00000001   2572 V2        EQU    2
                              00000003   00000001   2573 V3        EQU    3
                              00000004   00000001   2574 V4        EQU    4
                              00000005   00000001   2575 V5        EQU    5
                              00000006   00000001   2576 V6        EQU    6
                              00000007   00000001   2577 V7        EQU    7
                              00000008   00000001   2578 V8        EQU    8
                              00000009   00000001   2579 V9        EQU    9
                              0000000A   00000001   2580 V10       EQU    10
                              0000000B   00000001   2581 V11       EQU    11
                              0000000C   00000001   2582 V12       EQU    12
                              0000000D   00000001   2583 V13       EQU    13
                              0000000E   00000001   2584 V14       EQU    14
                              0000000F   00000001   2585 V15       EQU    15
                              00000010   00000001   2586 V16       EQU    16
                              00000011   00000001   2587 V17       EQU    17
                              00000012   00000001   2588 V18       EQU    18
                              00000013   00000001   2589 V19       EQU    19
                              00000014   00000001   2590 V20       EQU    20
                              00000015   00000001   2591 V21       EQU    21
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
		00000016	00000001	2592	V22	EQU	22
		00000017	00000001	2593	V23	EQU	23
		00000018	00000001	2594	V24	EQU	24
		00000019	00000001	2595	V25	EQU	25
		0000001A	00000001	2596	V26	EQU	26
		0000001B	00000001	2597	V27	EQU	27
		0000001C	00000001	2598	V28	EQU	28
		0000001D	00000001	2599	V29	EQU	29
		0000001E	00000001	2600	V30	EQU	30
		0000001F	00000001	2601	V31	EQU	31
				2602			
				2603		END	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES											
BEGIN	I	00000200	2	169	135	165	166	167								
CTLR0	F	0000048C	4	365	179	180	181	182								
DECNUM	C	00001073	16	416	279	281	287	289								
E7TEST	4	00000000	64	430	228											
E7TESTS	F	000034BC	4	2463	221											
EDIT	X	00001047	18	411	280	288										
ENDTEST	U	0000031E	1	265	226											
EOJ	I	00000470	4	355	214	268										
EOJPSW	D	00000460	8	353	355											
FAILCONT	U	0000030E	1	255												
FAILED	F	00001000	4	393	257	266										
FAILMSG	U	0000030A	1	249	239											
FAILPSW	D	00000478	8	357	359											
FAILTEST	I	00000488	4	359	269											
FB0001	F	00000280	8	198	202	203	205									
IMAGE	1	00000000	13804	0												
K	U	00000400	1	377	378	379	380									
K64	U	00010000	1	379												
M3	U	00000007	1	434	286											
MB	U	00100000	1	380												
MSG	I	000003A8	4	315	213	298										
MSGCMD	C	000003F6	9	345	328	329										
MSGMSG	C	000003FF	95	346	322	343	320									
MSGMVC	I	000003F0	6	343	326											
MSGOK	I	000003BE	2	324	321											
MSGRET	I	000003DE	4	339	332	335										
MSGSAVE	F	000003E4	4	342	318	339										
NEXTE7	U	000002D4	1	223	242	260										
OPNAME	C	00000008	8	436	284											
PAGE	U	00001000	1	378												
PRT3	C	0000105D	18	414	280	281	282	288	289	290						
PRTLINE	C	00001008	16	399	406	297										
PRTLNG	U	0000003F	1	406	296											
PRTM3	C	00001044	2	404	290											
PRTNAME	C	00001033	8	402	284											
PRTNUM	C	00001018	3	400	282											
R0	U	00000000	1	2549	129	179	182	202	204	205	206	211	230	231	256	257	295
					296	299	315	318	320	322	324	339				
R1	U	00000001	1	2550	212	237	238	266	267	297	329	343	560	561	586	587	612
					613	639	640	665	666	691	692	718	719	744	745	770	771
					800	801	826	827	852	853	879	880	905	906	931	932	958
					959	984	985	1010	1011	1040	1041	1066	1067	1092	1093	1119	1120
					1145	1146	1171	1172	1198	1199	1224	1225	1250	1251	1280	1281	1306
					1307	1332	1333	1359	1360	1385	1386	1411	1412	1438	1439	1464	1465
					1490	1491	1520	1521	1546	1547	1572	1573	1598	1599	1625	1626	1651
					1652	1677	1678	1703	1704	1730	1731	1756	1757	1782	1783	1808	1809
					1838	1839	1864	1865	1890	1891	1917	1918	1943	1944	1969	1970	1996
					1997	2022	2023	2048	2049	2075	2076	2101	2102	2127	2128	2157	2158
					2183	2184	2209	2210	2236	2237	2262	2263	2288	2289	2315	2316	2341
					2342	2367	2368	2394	2395	2420	2421	2446	2447				
R10	U	0000000A	1	2559	167	176	177										
R11	U	0000000B	1	2560	234	235	564	590	616	643	669	695	722	748	774	804	830
					856	883	909	935	962	988	1014	1044	1070	1096	1123	1149	1175
					1202	1228	1254	1284	1310	1336	1363	1389	1415	1442	1468	1494	1524
					1550	1576	1602	1629	1655	1681	1707	1734	1760	1786	1812	1842	1868
					1894	1921	1947	1973	2000	2026	2052	2079	2105	2131	2161	2187	2213

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					2240 2266 2292 2319 2345 2371 2398 2424 2450
R12	U	0000000C	1	2561	221 224 241 259
R13	U	0000000D	1	2562	
R14	U	0000000E	1	2563	
R15	U	0000000F	1	2564	250 275 302 303
R2	U	00000002	1	2551	213 278 279 286 287 295 298 299 316 318 324 325 326 328 334 339 340
R3	U	00000003	1	2552	
R4	U	00000004	1	2553	
R5	U	00000005	1	2554	224 225 228 276 301 546 566 572 592 598 618 625 645 651 671 677 697 704 724 730 750 756 776 786 806 812 832 838 858 865 885 891 911 917 937 944 964 970 990 996 1016 1026 1046 1052 1072 1078 1098 1105 1125 1131 1151 1157 1177 1184 1204 1210 1230 1236 1256 1266 1286 1292 1312 1318 1338 1345 1365 1371 1391 1397 1417 1424 1444 1450 1470 1476 1496 1506 1526 1532 1552 1558 1578 1584 1604 1611 1631 1637 1657 1663 1683 1689 1709 1716 1736 1742 1762 1768 1788 1794 1814 1824 1844 1850 1870 1876 1896 1903 1923 1929 1949 1955 1975 1982 2002 2008 2028 2034 2054 2061 2081 2087 2107 2113 2133 2143 2163 2169 2189 2195 2215 2222 2242 2248 2268 2274 2294 2301 2321 2327 2347 2353 2373 2380 2400 2406 2426 2432 2452
R6	U	00000006	1	2555	
R7	U	00000007	1	2556	
R8	U	00000008	1	2557	165 169 170 171 173
R9	U	00000009	1	2558	166 173 174 176
RE1	F	00001114	4	565	552 554
RE10	F	00001594	4	805	792 794
RE11	F	00001614	4	831	818 820
RE12	F	00001694	4	857	844 846
RE13	F	00001714	4	884	871 873
RE14	F	00001794	4	910	897 899
RE15	F	00001814	4	936	923 925
RE16	F	00001894	4	963	950 952
RE17	F	00001914	4	989	976 978
RE18	F	00001994	4	1015	1002 1004
RE19	F	00001A14	4	1045	1032 1034
RE2	F	00001194	4	591	578 580
RE20	F	00001A94	4	1071	1058 1060
RE21	F	00001B14	4	1097	1084 1086
RE22	F	00001B94	4	1124	1111 1113
RE23	F	00001C14	4	1150	1137 1139
RE24	F	00001C94	4	1176	1163 1165
RE25	F	00001D14	4	1203	1190 1192
RE26	F	00001D94	4	1229	1216 1218
RE27	F	00001E14	4	1255	1242 1244
RE28	F	00001E94	4	1285	1272 1274
RE29	F	00001F14	4	1311	1298 1300
RE3	F	00001214	4	617	604 606
RE30	F	00001F94	4	1337	1324 1326
RE31	F	00002014	4	1364	1351 1353
RE32	F	00002094	4	1390	1377 1379
RE33	F	00002114	4	1416	1403 1405
RE34	F	00002194	4	1443	1430 1432
RE35	F	00002214	4	1469	1456 1458
RE36	F	00002294	4	1495	1482 1484
RE37	F	00002314	4	1525	1512 1514

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
RE38	F	00002394	4	1551	1538	1540
RE39	F	00002414	4	1577	1564	1566
RE4	F	00001294	4	644	631	633
RE40	F	00002494	4	1603	1590	1592
RE41	F	00002514	4	1630	1617	1619
RE42	F	00002594	4	1656	1643	1645
RE43	F	00002614	4	1682	1669	1671
RE44	F	00002694	4	1708	1695	1697
RE45	F	00002714	4	1735	1722	1724
RE46	F	00002794	4	1761	1748	1750
RE47	F	00002814	4	1787	1774	1776
RE48	F	00002894	4	1813	1800	1802
RE49	F	00002914	4	1843	1830	1832
RE5	F	00001314	4	670	657	659
RE50	F	00002994	4	1869	1856	1858
RE51	F	00002A14	4	1895	1882	1884
RE52	F	00002A94	4	1922	1909	1911
RE53	F	00002B14	4	1948	1935	1937
RE54	F	00002B94	4	1974	1961	1963
RE55	F	00002C14	4	2001	1988	1990
RE56	F	00002C94	4	2027	2014	2016
RE57	F	00002D14	4	2053	2040	2042
RE58	F	00002D94	4	2080	2067	2069
RE59	F	00002E14	4	2106	2093	2095
RE6	F	00001394	4	696	683	685
RE60	F	00002E94	4	2132	2119	2121
RE61	F	00002F14	4	2162	2149	2151
RE62	F	00002F94	4	2188	2175	2177
RE63	F	00003014	4	2214	2201	2203
RE64	F	00003094	4	2241	2228	2230
RE65	F	00003114	4	2267	2254	2256
RE66	F	00003194	4	2293	2280	2282
RE67	F	00003214	4	2320	2307	2309
RE68	F	00003294	4	2346	2333	2335
RE69	F	00003314	4	2372	2359	2361
RE7	F	00001414	4	723	710	712
RE70	F	00003394	4	2399	2386	2388
RE71	F	00003414	4	2425	2412	2414
RE72	F	00003494	4	2451	2438	2440
RE8	F	00001494	4	749	736	738
RE9	F	00001514	4	775	762	764
REA1	A	000010D0	4	554		
REA10	A	00001550	4	794		
REA11	A	000015D0	4	820		
REA12	A	00001650	4	846		
REA13	A	000016D0	4	873		
REA14	A	00001750	4	899		
REA15	A	000017D0	4	925		
REA16	A	00001850	4	952		
REA17	A	000018D0	4	978		
REA18	A	00001950	4	1004		
REA19	A	000019D0	4	1034		
REA2	A	00001150	4	580		
REA20	A	00001A50	4	1060		
REA21	A	00001AD0	4	1086		
REA22	A	00001B50	4	1113		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA23	A	00001BD0	4	1139	
REA24	A	00001C50	4	1165	
REA25	A	00001CD0	4	1192	
REA26	A	00001D50	4	1218	
REA27	A	00001DD0	4	1244	
REA28	A	00001E50	4	1274	
REA29	A	00001ED0	4	1300	
REA3	A	000011D0	4	606	
REA30	A	00001F50	4	1326	
REA31	A	00001FD0	4	1353	
REA32	A	00002050	4	1379	
REA33	A	000020D0	4	1405	
REA34	A	00002150	4	1432	
REA35	A	000021D0	4	1458	
REA36	A	00002250	4	1484	
REA37	A	000022D0	4	1514	
REA38	A	00002350	4	1540	
REA39	A	000023D0	4	1566	
REA4	A	00001250	4	633	
REA40	A	00002450	4	1592	
REA41	A	000024D0	4	1619	
REA42	A	00002550	4	1645	
REA43	A	000025D0	4	1671	
REA44	A	00002650	4	1697	
REA45	A	000026D0	4	1724	
REA46	A	00002750	4	1750	
REA47	A	000027D0	4	1776	
REA48	A	00002850	4	1802	
REA49	A	000028D0	4	1832	
REA5	A	000012D0	4	659	
REA50	A	00002950	4	1858	
REA51	A	000029D0	4	1884	
REA52	A	00002A50	4	1911	
REA53	A	00002AD0	4	1937	
REA54	A	00002B50	4	1963	
REA55	A	00002BD0	4	1990	
REA56	A	00002C50	4	2016	
REA57	A	00002CD0	4	2042	
REA58	A	00002D50	4	2069	
REA59	A	00002DD0	4	2095	
REA6	A	00001350	4	685	
REA60	A	00002E50	4	2121	
REA61	A	00002ED0	4	2151	
REA62	A	00002F50	4	2177	
REA63	A	00002FD0	4	2203	
REA64	A	00003050	4	2230	
REA65	A	000030D0	4	2256	
REA66	A	00003150	4	2282	
REA67	A	000031D0	4	2309	
REA68	A	00003250	4	2335	
REA69	A	000032D0	4	2361	
REA7	A	000013D0	4	712	
REA70	A	00003350	4	2388	
REA71	A	000033D0	4	2414	
REA72	A	00003450	4	2440	
REA8	A	00001450	4	738	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA9	A	000014D0	4	764		
READDR	A	00000018	4	439	237	
REG2LOW	U	000000DD	1	383		
REG2PATT	U	AABBCCDD	1	382		
RELEN	A	00000014	4	438		
RPTDWSAV	D	00000398	8	308	295	299
RPTERROR	I	0000032C	4	275	250	
RPTSAVE	F	00000390	4	305	275	302
RPTSVR5	F	00000394	4	306	276	301
SKL0001	U	0000004E	1	195	211	
SKT0001	C	0000022A	20	192	195	212
SVOLDPSW	U	00000140	0	131		
T1	A	000010B8	4	547	2466	
T10	A	00001538	4	787	2475	
T11	A	000015B8	4	813	2476	
T12	A	00001638	4	839	2477	
T13	A	000016B8	4	866	2478	
T14	A	00001738	4	892	2479	
T15	A	000017B8	4	918	2480	
T16	A	00001838	4	945	2481	
T17	A	000018B8	4	971	2482	
T18	A	00001938	4	997	2483	
T19	A	000019B8	4	1027	2484	
T2	A	00001138	4	573	2467	
T20	A	00001A38	4	1053	2485	
T21	A	00001AB8	4	1079	2486	
T22	A	00001B38	4	1106	2487	
T23	A	00001BB8	4	1132	2488	
T24	A	00001C38	4	1158	2489	
T25	A	00001CB8	4	1185	2490	
T26	A	00001D38	4	1211	2491	
T27	A	00001DB8	4	1237	2492	
T28	A	00001E38	4	1267	2493	
T29	A	00001EB8	4	1293	2494	
T3	A	000011B8	4	599	2468	
T30	A	00001F38	4	1319	2495	
T31	A	00001FB8	4	1346	2496	
T32	A	00002038	4	1372	2497	
T33	A	000020B8	4	1398	2498	
T34	A	00002138	4	1425	2499	
T35	A	000021B8	4	1451	2500	
T36	A	00002238	4	1477	2501	
T37	A	000022B8	4	1507	2502	
T38	A	00002338	4	1533	2503	
T39	A	000023B8	4	1559	2504	
T4	A	00001238	4	626	2469	
T40	A	00002438	4	1585	2505	
T41	A	000024B8	4	1612	2506	
T42	A	00002538	4	1638	2507	
T43	A	000025B8	4	1664	2508	
T44	A	00002638	4	1690	2509	
T45	A	000026B8	4	1717	2510	
T46	A	00002738	4	1743	2511	
T47	A	000027B8	4	1769	2512	
T48	A	00002838	4	1795	2513	
T49	A	000028B8	4	1825	2514	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
T5	A	000012B8	4	652	2470	
T50	A	00002938	4	1851	2515	
T51	A	000029B8	4	1877	2516	
T52	A	00002A38	4	1904	2517	
T53	A	00002AB8	4	1930	2518	
T54	A	00002B38	4	1956	2519	
T55	A	00002BB8	4	1983	2520	
T56	A	00002C38	4	2009	2521	
T57	A	00002CB8	4	2035	2522	
T58	A	00002D38	4	2062	2523	
T59	A	00002DB8	4	2088	2524	
T6	A	00001338	4	678	2471	
T60	A	00002E38	4	2114	2525	
T61	A	00002EB8	4	2144	2526	
T62	A	00002F38	4	2170	2527	
T63	A	00002FB8	4	2196	2528	
T64	A	00003038	4	2223	2529	
T65	A	000030B8	4	2249	2530	
T66	A	00003138	4	2275	2531	
T67	A	000031B8	4	2302	2532	
T68	A	00003238	4	2328	2533	
T69	A	000032B8	4	2354	2534	
T7	A	000013B8	4	705	2472	
T70	A	00003338	4	2381	2535	
T71	A	000033B8	4	2407	2536	
T72	A	00003438	4	2433	2537	
T8	A	00001438	4	731	2473	
T9	A	000014B8	4	757	2474	
TESTING	F	00001004	4	394	231	
TNUM	H	00000004	2	432	230	278
TSUB	A	00000000	4	431	234	
TTABLE	F	000034BC	4	2465		
V0	U	00000000	1	2570		
V1	U	00000001	1	2571	233	
V10	U	0000000A	1	2580		
V11	U	0000000B	1	2581		
V12	U	0000000C	1	2582		
V13	U	0000000D	1	2583		
V14	U	0000000E	1	2584		
V15	U	0000000F	1	2585		
V16	U	00000010	1	2586		
V17	U	00000011	1	2587		
V18	U	00000012	1	2588		
V19	U	00000013	1	2589		
V1FUDGE	X	00001094	16	423	233	
V101	X	000010E0	16	556	563	
V1010	X	00001560	16	796	803	
V1011	X	000015E0	16	822	829	
V1012	X	00001660	16	848	855	
V1013	X	000016E0	16	875	882	
V1014	X	00001760	16	901	908	
V1015	X	000017E0	16	927	934	
V1016	X	00001860	16	954	961	
V1017	X	000018E0	16	980	987	
V1018	X	00001960	16	1006	1013	
V1019	X	000019E0	16	1036	1043	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V102	X	00001160	16	582	589
V1020	X	00001A60	16	1062	1069
V1021	X	00001AE0	16	1088	1095
V1022	X	00001B60	16	1115	1122
V1023	X	00001BE0	16	1141	1148
V1024	X	00001C60	16	1167	1174
V1025	X	00001CE0	16	1194	1201
V1026	X	00001D60	16	1220	1227
V1027	X	00001DE0	16	1246	1253
V1028	X	00001E60	16	1276	1283
V1029	X	00001EE0	16	1302	1309
V103	X	000011E0	16	608	615
V1030	X	00001F60	16	1328	1335
V1031	X	00001FE0	16	1355	1362
V1032	X	00002060	16	1381	1388
V1033	X	000020E0	16	1407	1414
V1034	X	00002160	16	1434	1441
V1035	X	000021E0	16	1460	1467
V1036	X	00002260	16	1486	1493
V1037	X	000022E0	16	1516	1523
V1038	X	00002360	16	1542	1549
V1039	X	000023E0	16	1568	1575
V104	X	00001260	16	635	642
V1040	X	00002460	16	1594	1601
V1041	X	000024E0	16	1621	1628
V1042	X	00002560	16	1647	1654
V1043	X	000025E0	16	1673	1680
V1044	X	00002660	16	1699	1706
V1045	X	000026E0	16	1726	1733
V1046	X	00002760	16	1752	1759
V1047	X	000027E0	16	1778	1785
V1048	X	00002860	16	1804	1811
V1049	X	000028E0	16	1834	1841
V105	X	000012E0	16	661	668
V1050	X	00002960	16	1860	1867
V1051	X	000029E0	16	1886	1893
V1052	X	00002A60	16	1913	1920
V1053	X	00002AE0	16	1939	1946
V1054	X	00002B60	16	1965	1972
V1055	X	00002BE0	16	1992	1999
V1056	X	00002C60	16	2018	2025
V1057	X	00002CE0	16	2044	2051
V1058	X	00002D60	16	2071	2078
V1059	X	00002DE0	16	2097	2104
V106	X	00001360	16	687	694
V1060	X	00002E60	16	2123	2130
V1061	X	00002EE0	16	2153	2160
V1062	X	00002F60	16	2179	2186
V1063	X	00002FE0	16	2205	2212
V1064	X	00003060	16	2232	2239
V1065	X	000030E0	16	2258	2265
V1066	X	00003160	16	2284	2291
V1067	X	000031E0	16	2311	2318
V1068	X	00003260	16	2337	2344
V1069	X	000032E0	16	2363	2370
V107	X	000013E0	16	714	721

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V1070	X	00003360	16	2390	2397												
V1071	X	000033E0	16	2416	2423												
V1072	X	00003460	16	2442	2449												
V108	X	00001460	16	740	747												
V109	X	000014E0	16	766	773												
V10UTPUT	X	00000028	16	441	238												
V2	U	00000002	1	2572													
V20	U	00000014	1	2590													
V21	U	00000015	1	2591													
V22	U	00000016	1	2592	561	562	563	587	588	589	613	614	615	640	641	642	666
					667	668	692	693	694	719	720	721	745	746	747	771	772
					773	801	802	803	827	828	829	853	854	855	880	881	882
					906	907	908	932	933	934	959	960	961	985	986	987	1011
					1012	1013	1041	1042	1043	1067	1068	1069	1093	1094	1095	1120	1121
					1122	1146	1147	1148	1172	1173	1174	1199	1200	1201	1225	1226	1227
					1251	1252	1253	1281	1282	1283	1307	1308	1309	1333	1334	1335	1360
					1361	1362	1386	1387	1388	1412	1413	1414	1439	1440	1441	1465	1466
					1467	1491	1492	1493	1521	1522	1523	1547	1548	1549	1573	1574	1575
					1599	1600	1601	1626	1627	1628	1652	1653	1654	1678	1679	1680	1704
					1705	1706	1731	1732	1733	1757	1758	1759	1783	1784	1785	1809	1810
					1811	1839	1840	1841	1865	1866	1867	1891	1892	1893	1918	1919	1920
					1944	1945	1946	1970	1971	1972	1997	1998	1999	2023	2024	2025	2049
					2050	2051	2076	2077	2078	2102	2103	2104	2128	2129	2130	2158	2159
					2160	2184	2185	2186	2210	2211	2212	2237	2238	2239	2263	2264	2265
					2289	2290	2291	2316	2317	2318	2342	2343	2344	2368	2369	2370	2395
					2396	2397	2421	2422	2423	2447	2448	2449					
V23	U	00000017	1	2593													
V24	U	00000018	1	2594													
V25	U	00000019	1	2595													
V26	U	0000001A	1	2596													
V27	U	0000001B	1	2597													
V28	U	0000001C	1	2598													
V29	U	0000001D	1	2599													
V2ADDR	A	00000010	4	437	560	586	612	639	665	691	718	744	770	800	826	852	879
					905	931	958	984	1010	1040	1066	1092	1119	1145	1171	1198	1224
					1250	1280	1306	1332	1359	1385	1411	1438	1464	1490	1520	1546	1572
					1598	1625	1651	1677	1703	1730	1756	1782	1808	1838	1864	1890	1917
					1943	1969	1996	2022	2048	2075	2101	2127	2157	2183	2209	2236	2262
					2288	2315	2341	2367	2394	2420	2446						
V3	U	00000003	1	2573													
V30	U	0000001E	1	2600													
V31	U	0000001F	1	2601													
V4	U	00000004	1	2574													
V5	U	00000005	1	2575													
V6	U	00000006	1	2576													
V7	U	00000007	1	2577													
V8	U	00000008	1	2578													
V9	U	00000009	1	2579													
X0001	U	000002A8	1	201	189	202											
X1	F	000010F8	4	559	547												
X10	F	00001578	4	799	787												
X11	F	000015F8	4	825	813												
X12	F	00001678	4	851	839												
X13	F	000016F8	4	878	866												
X14	F	00001778	4	904	892												
X15	F	000017F8	4	930	918												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X16	F	00001878	4	957	945
X17	F	000018F8	4	983	971
X18	F	00001978	4	1009	997
X19	F	000019F8	4	1039	1027
X2	F	00001178	4	585	573
X20	F	00001A78	4	1065	1053
X21	F	00001AF8	4	1091	1079
X22	F	00001B78	4	1118	1106
X23	F	00001BF8	4	1144	1132
X24	F	00001C78	4	1170	1158
X25	F	00001CF8	4	1197	1185
X26	F	00001D78	4	1223	1211
X27	F	00001DF8	4	1249	1237
X28	F	00001E78	4	1279	1267
X29	F	00001EF8	4	1305	1293
X3	F	000011F8	4	611	599
X30	F	00001F78	4	1331	1319
X31	F	00001FF8	4	1358	1346
X32	F	00002078	4	1384	1372
X33	F	000020F8	4	1410	1398
X34	F	00002178	4	1437	1425
X35	F	000021F8	4	1463	1451
X36	F	00002278	4	1489	1477
X37	F	000022F8	4	1519	1507
X38	F	00002378	4	1545	1533
X39	F	000023F8	4	1571	1559
X4	F	00001278	4	638	626
X40	F	00002478	4	1597	1585
X41	F	000024F8	4	1624	1612
X42	F	00002578	4	1650	1638
X43	F	000025F8	4	1676	1664
X44	F	00002678	4	1702	1690
X45	F	000026F8	4	1729	1717
X46	F	00002778	4	1755	1743
X47	F	000027F8	4	1781	1769
X48	F	00002878	4	1807	1795
X49	F	000028F8	4	1837	1825
X5	F	000012F8	4	664	652
X50	F	00002978	4	1863	1851
X51	F	000029F8	4	1889	1877
X52	F	00002A78	4	1916	1904
X53	F	00002AF8	4	1942	1930
X54	F	00002B78	4	1968	1956
X55	F	00002BF8	4	1995	1983
X56	F	00002C78	4	2021	2009
X57	F	00002CF8	4	2047	2035
X58	F	00002D78	4	2074	2062
X59	F	00002DF8	4	2100	2088
X6	F	00001378	4	690	678
X60	F	00002E78	4	2126	2114
X61	F	00002EF8	4	2156	2144
X62	F	00002F78	4	2182	2170
X63	F	00002FF8	4	2208	2196
X64	F	00003078	4	2235	2223
X65	F	000030F8	4	2261	2249
X66	F	00003178	4	2287	2275

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
X67	F	000031F8	4	2314	2302				
X68	F	00003278	4	2340	2328				
X69	F	000032F8	4	2366	2354				
X7	F	000013F8	4	717	705				
X70	F	00003378	4	2393	2381				
X71	F	000033F8	4	2419	2407				
X72	F	00003478	4	2445	2433				
X8	F	00001478	4	743	731				
X9	F	000014F8	4	769	757				
XC0001	U	000002D0	1	215	207				
ZVE7TST	J	00000000	13804	128	131	133	137	141	392	129
=A(E7TESTS)	A	00000498	4	370	221				
=AL2(L'MSGMSG)	R	000004A2	2	373	320				
=F'1'	F	0000049C	4	371	256				
=F'64'	F	00000494	4	369	206				
=H'0'	H	000004A0	2	372	315				

MACRO	DEFN	REFERENCES															
FCHECK	81	188															
PTTABLE	501	2464															
VRR_A	460	544	570	596	623	649	675	702	728	754	784	810	836	863	889	915	942	968
		994	1024	1050	1076	1103	1129	1155	1182	1208	1234	1264	1290	1316	1343	1369	1395	1422
		1448	1474	1504	1530	1556	1582	1609	1635	1661	1687	1714	1740	1766	1792	1822	1848	1874
		1901	1927	1953	1980	2006	2032	2059	2085	2111	2141	2167	2193	2220	2246	2272	2299	2325
		2351	2378	2404	2430												

```
     DESC      SYMBOL   SIZE      POS          ADDR

Entry: 0

Image        IMAGE    13804   0000-35EB    0000-35EB
   Region             13804   0000-35EB    0000-35EB
     CSECT   ZVE7TST  13804   0000-35EB    0000-35EB
```

STMT   FILE NAME

1   /home/tn529/sharedvfp/tests/zvector-e7-13-UnpackMisc.asm

** NO ERRORS FOUND **