va ver.	0. 7. 0 zvector- e7-	- 20- ASTDD		03 Apr 2025 15: 40: 04 Page
LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 ************************************
				4 * Zvector E7 instruction tests for VRI-d encoded:
				5 * 6 * E777 VSLDB - Vector Shift Left Double By Byte
				7 * 8 * James Wekel March 2025 9 ************************************
				11 ***********************************
				13 * basic instruction tests 14 *
				15 *********************
				16 * This program tests proper functioning of the z/arch E7 VRI-d 17 * Vector Shift Left Double By Byt instruction.
				18 * 19 * Exceptions are not tested. 20 *
				21 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch 22 * obvious coding errors. None of the tests are thorough. They are 23 * NOT designed to test all aspects of any of the instructions.
				24 * 25 **********************************
				27 * *Testcase zvector-e7-20-VSLDB
				28 * * Zvector E7 instruction tests for VRI-d encoded:
				30 * * 31 * * E777 VSLDB - Vector Shift Left Double By Byte
				32 * * 33 * * #
				34 * * # This tests only the basic function of the instructions. $35 * * #$ Exceptions are NOT tested.
				36 * * #
				38 * mainsize 2
				39 * numcpu 1 40 * sysclear
				41 * archl vl z/Arch
				42 * 43 * loadcore "\$(testpath)/zvector-e7-20-VSLDB.core" 0x0 44 *
				45 * diag8cmd enable # (needed for messages to Hercules console)
				46 * runtest 2 47 * diag8cmd disable # (reset back to default)
				48 * 49 * *Done
				50 * 51 **********************************

***************  i ssued and  ********  to check  te  in byte  FBBIT=&FBBIT'
issued and  *******  to check  te  in byte
*********  to check  te  in byte
*********  to check  te  in byte
te in byte
te in byte
te in byte
te in byte
te in byte
te in byte
in byte
in byte
, and the second
, and the second
FBBIT=&FBBIT'
FBBIT=&FBBIT'
S

ASMA Ver.	0.7.0 zvector-e7-2	20- VSLDB					03 Apr 2025 15: 40: 04 Page 3
LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				108 **** 109 * 110 ***	Low co	**************************************	************ *********
00000000		0000000 0000000	000013DB	111 ZVE7 112	7TST START		Low core addressability
		00000140	00000000	113 114 SV0I	LDPSW EQU	ZVE7TST+X' 140'	z/Arch Supervisor call old PSW
0000000 00001A0	00000001 80000000	00000000	000001A0	116 117	DC	ZVE7TST+X' 1A0' X' 000000018000000	z/Architecure RESTART PSW
000001A8	00000000 00000200			118	DC	AD(BEGIN)	
000001B0 000001D0 000001D8	00020001 80000000 0000000 0000DEAD	000001B0	000001D0	120 121 122	DC	ZVE7TST+X' 1D0' X' 000200018000000 AD(X' DEAD' )	z/Architecure PROGRAM CHECK PSW 00'
000001E0		000001E0	00000200	124	ORG	ZVE7TST+X' 200'	Start of actual test program
				129 *		**************************************	**************************************
				131 * I 132 *	Register Usa		
				133 * 134 *	R1-4 (w	vork) vork)	
				135 * 136 * 137 *	R6-R7 (w	esting control tal work) rst base registel	ble - current test base r
				138 * 139 * 140 *	R9 Se R10 Th	econd base registe nird base registen TEST call return	er
				141 * 142 * 143 *	R12 E7 R13 (w R14 Su	TESTS register work) ubroutine call	
				144 * 145 * 146 ****	R15 Se	econdary Subrouti	ne call or work  ***********************************
00000200 00000200 00000200		00000200 00001200 00002200		148 149 150		BEGIN, R8 BEGIN+4096, R9 BEGIN+8192, R10	FIRST Base Register SECOND Base Register THIRD Base Register
00000200 00000200 00000202 00000204	0580 0680 0680	00002200		152 BEGI 153 154		R8, 0 R8, 0	Initalize FIRST base register Initalize FIRST base register Initalize FIRST base register
00000206 0000020A	4190 8800 4190 9800		00000800 00000800	156 157 158		R9, 2048(, R8) R9, 2048(, R9)	Initalize SECOND base register Initalize SECOND base register

ASMA Ver.	0. 7. 0 zvector- e7- 2	20- VSLDB					03 Apr 2025 15: 40: 04 Page	6
LOC	OBJECT CODE	ADDR1	ADDR2	STM				
				227 ******* 228 * result 229 *	not a	s expected:	**************************************	
				230 * 231 ******		and instructio	n m4  ***********************************	
0000030A	45F0 812C	0000030A	00000001 0000032C	232 FAILMSG 233	EQU BAL	* R15, RPTERROR		
					ue aft	er a failed tes	**************************************	
0000030E	5800 829C	0000030E	00000001 0000049C	238 FAILCONT 239	EQU L	* RO, =F' 1'	set failed test indicator	
00000312 00000316	5000 8E00 41C0 C004		00001000 0000004	240 241 242	ST LA	RO, FAILED R12, 4(0, R12)	next test address	
00000310 0000031A	47F0 80D4		0000004 000002D4	243	В	NEXTE7	next test audi ess	
				246 * end of 247 ******	testi	**************************************	**************************************	
0000031E 00000322	5810 8E00 1211	0000031E	00000001 00001000	248 ENDTEST 249 250	EQU L LTR	* R1, FAILED R1, R1	did a test fail?	
00000324 00000328	4780 8270 47F0 8288		00000470 00000488	251 252	BZ B	EOJ FAI LTEST	No, exit Yes, exit with BAD PSW	

2D' 0'

RO-R2 save area for MSG call

290 RPTDWSAV DC

00000398

ASMA Ver.	0. 7. 0 zvector- e7- 2	O- VSLDB					03 Apr 2025 15: 40: 04 Page 8
LOC	OBJECT CODE	ADDR1	ADDR2	STM			
				292 ******** 293 * 294 * 295 ******		HERCULES MESSAGE poin R2 = return address	**************************************
000003A8 000003AC	4900 82A0 07D2		000004A0	297 MSG 298	CH BNHR	RO, =H' O' R2	Do we even HAVE a message? No, ignore
000003AE	9002 81E4		000003E4	300	STM	RO, R2, MSGSAVE	Save registers
000003B2 000003B6 000003BA	4900 82A2 47D0 81BE 4100 005F		000004A2 000003BE 0000005F	302 303 304	CH BNH LA	RO, =AL2(L' MSGMSG) MSGOK RO, L' MSGMSG	Message length within limits? Yes, continue No, set to maximum
000003BE 000003C0 000003C2	1820 0620 4420 81F0		000003F0	306 MSGOK 307 308	LR BCTR EX	R2, R0 R2, 0 R2, MSGMVC	Copy length to work register Minus-1 for execute Copy message to 0/P buffer
000003C6 000003CA	4120 200A 4110 81F6		0000000A 000003F6	310 311	LA LA	R2, 1+L' MSGCMD(, R2) R1, MSGCMD	Calculate true command length Point to true command
000003CE 000003D2	83120008 4780 81DE		000003DE	313 314	DC BZ	X' 83', X' 12', X' 0008' MSGRET	Issue Hercules Diagnose X'008' Return if successful
000003D6 000003D8	1222 4780 81DE		000003DE	315 316 317	LTR BZ	R2, R2 MSGRET	Is Diag8 Ry (R2) 0? an error occurred but coninue
000003DC	0000			318 319	DC	Н' О'	CRASH for debugging purposes
000003DE 000003E2	9802 81E4 07F2		000003E4	321 MSGRET 322	LM BR	RO, R2, MSGSAVE R2	Restore registers Return to caller
000003E4	00000000 00000000 00000000 00000000	00000000	0000000	324 MSGSAVE	_	3F' 0'	Registers save area
000003F0	D200 81FF 1000	000003FF	0000000	325 MSGMVC	MVC	MSGMSG(0), 0(R1)	Executed instruction
000003F6 000003FF	D4E2C7D5 D6C8405C 40404040 40404040			327 MSGCMD 328 MSGMSG 329	DC DC	C' MSGNOH * ' CL95' '	*** HERCULES MESSAGE COMMAND *** The message text to be displayed

ASMA Ver.	0. 7. 0 zvector- e7- 2	O- VSLDB						03 Apr 2025 15: 40: 04 Page
LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
								**************************************
00000460	00020001 80000000			335	EOJPSW	DC	0D' 0' , X' 000200	0180000000', AD(0)
00000470	B2B2 8260		00000460	337	<b>EOJ</b>	LPSWE	<b>E0JPSW</b>	Normal completion
00000478	00020001 80000000			339	<b>FAI LPSW</b>	DC	OD' O' , X' 000200	018000000', AD(X'BAD')
00000488	B2B2 8278		00000478	341	FAI LTEST	LPSWE	FAILPSW	Abnormal termination
				343 344 345	***** * *****	****** <b>Worki</b> : *****	**************************************	************
00000400	0000000			0.47	CITI DO	Th C	<b>.</b>	ano.
	00000000 0000000			347 348	CTLRO	DS DS	F F	CRO
00000494				350		LTORG		Literals pool
00000494 00000498 0000049C	00000040 000013B8 00000001			351 352 353		21010	=F' 64' =A(E7TESTS) =F' 1'	22 ccruz s pocr
000004A0 000004A2	0000 005F			354 355 356	,		=H' 0' =AL2(L' MSGMSG)	
		00000105	0000000	357 358			constants	
		00000400 00001000 00010000 00100000	00000001 00000001 00000001 00000001	361 362	PAGE K64	EQU EQU EQU EQU	1024 (4*K) (64*K) (K*K)	One KB Size of one page 64 KB 1 MB
		AABBCCDD 000000DD	00000001 00000001	363 364	REG2PATT REG2LOW	EQU	X' AABBCCDD' X' DD'	Polluted Register pattern (last byte above)

ASMA Ver.	0. 7. 0 zvector- e7- 2	20- VSLDB				03 Apr 2025 15: 40: 04 Page	12
LOC	OBJECT CODE	ADDR1	ADDR2	STM			
				409 *	E7TEST DSECT	**************	
00000000 00000004 00000006 00000007 00000008 00000010 00000014 00000018 0000001C 00000020 00000028 00000038	00000000 000 00 00 40404040 40404040 00000000			412 E7TEST 413 TSUB 414 TNUM 415 416 I4 417 418 OPNAME 419 V2ADDR 420 V3ADDR 421 RELEN 422 READDR 423 424 V10UTPUT 425 426 427 * 428 *	DS FD	pointer to test Test Number  i 4 field  E7 name address of v2 source address of v3 source RESULT LENGTH result (expected) address gap V1 Output gap  be here (from VRI-d macro)	
		00000000	000013DB	428 * 429 * 430 * 432 ZVE7TST	followed by EXPECTED RES	SULT	
000010B4				436 * Ma	cros to help build	**************************************	
				441 * 442 443	to generate individ MACRO VRI_D &INST, &I4		
				444 . * 445 . * 446 447 448 &TNUM 449 450	GBLA &TNUM SETA &TNUM+1 DS OFD	&INST - VRI-d instruction under test &I4 - shift	
				450 451 452 453 T&TNUM 454 455 456	DS OFD USING *, R5  DC A(X&TNUM) DC H' &TNUM' DC X' 00' DC HL1' &I 4'	base for test data and test routine address of test routine test number i4 field	
				457 458	DC CL8' &I NST' DC A(RE&TNUM+16	instruction name	

LOC	0. 7. 0 zvector-e7- 0BJECT CODE	ADDR1	ADDR2	STMI			03 Apr 2025 15: 40: 04 Page
LUC	OBJECT CODE	ADDRI	ADDRZ		DC.	A (DESTNIM, 22)	addragg of v2 source
				459 460	DC DC	A(RE&TNUM+32) A(16)	address of v3 source result length
				461 REA&TN		A (RE&TNUM)	result address
				462 463 V10&TN	DS UM DS	FD XL16	gap V1 output
				464	DS	FD	gap
				465 . * 466 *			
				467 X&TNUM		OF	1 1 0
				468 469	LGF VL	R1, V2ADDR v22, O(R1)	load v2 source use v22 to test decoder
				470			
				471 472	LGF VL	R1, V3ADDR v23, O(R1)	load v3 source use v23 to test decoder
				473			
				474 475	&I NST VST	V22, V22, V23, &I 4 V22, V10&TNUM	test instruction (dest is a source) save v1 output
				476			
				477 478	BR	R11	return
				479 RE&TNU	M DC	0F	xl16 expected result
				480 481	DROP	R5	
				482	MEND		
				484 *			
				485 * macr	o to gen	erate table of poi	inters to individual tests
				486 * 487	MACRO	_	
				488	PTTAB		
				489	GBLA LCLA	&TNUM	
				490 491 &CUR	SETA	acur 1	
				492 . * 493 TTABLE			
				493 TTABLE 494 . LOOP	DS ANOP	0F	
				495 . *		A (TIO CLID)	
				496 497 . *	DC	A(T&CUR)	
				498 &CUR	SETA	&CUR+1	LOOP
				499 500 *	AIF	(&CUR LE &TNUM). 1	LUUP
				501	DC	A(0)	END OF TABLE
				502 503 . *	DC	A(0)	
				504 505	MEND		

ASMA Ver.	0. 7. 0 zvector- e7- 2	20- VSLDB					03 Apr 2025 15: 40: 04 Page 1
LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				507 ******	*****	*******	**********
				508 *	E7 VR	I-d tests	**********
				510	PRINT		
				511			
				512 * E77° 513	7 VSLDB	- Vector Shift I	Left Double By Byte
				514 *	VRI - d	instruction, i4	
				515 *		followed by	. 1 1. (8/4)
				516 * 517 *		16 byte expect 16 byte V2 sou	ted result (V1) urce
				518 *		16 byte V3 sou	urce
				519 * 520 * VSL	W	ector Shift Left l	Nouble Dy Dyte
				521 *	 		
				522	T/DT P	VCI DD O	
00010B8				523 524+	VR1_D DS	VSLDB, O OFD	
00010B8		000010B8		<b>525</b> +	USING		base for test data and test routine
00010B8	000010F8			526+T1	DC	A(X1)	address of test routine
00010BC 00010BE	0001 00			527+ 528+	DC DC	H' 1' X' 00'	test number
0010BF	00			<b>529</b> +	DC	HL1' 0'	i4 field
00010C0 00010C8	E5E2D3C4 C2404040 00001130			530+ 531+	DC DC	CL8' VSLDB' A(RE1+16)	instruction name address of v2 source
0010C8	00001130			532+	DC	A(RE1+10) A(RE1+32)	address of v2 source
00010D0	00000010			533+	DC	A(16)	result length
00010D4 00010D8	00001120 00000000 00000000			534+REA1 535+	DC DS	A(RE1) FD	result address
00010E0	0000000 00000000			536+V101	DS	XL16	gap V1 output
00010E8 00010F0	00000000 00000000 0000000 00000000			537+	DS	FD	dan
	0000000 0000000			538+*	DЗ	T'D	gap
00010F8	E010 7010 0014		00000010	539+X1	DS	OF	1 - 1 - 9
00010F8 00010FE	E310 5010 0014 E761 0000 0806		00000010 00000000	540+ 541+	LGF VL	R1, V2ADDR v22, O(R1)	load v2 source use v22 to test decoder
0001104	E310 5014 0014		0000014	<b>542</b> +	LGF	R1, V3ADDR	load v3 source
000110A 0001110	E771 0000 0806 E766 7000 0E77		0000000	543+ 544+	VL VSI DR	v23, 0(R1) V22, V22, V23, 0	use v23 to test decoder test instruction (dest is a source)
0001116	E760 7000 0E77 E760 5028 080E		000010E0	545+	VST	V22, V101	save v1 output
000111C	07FB			546+	BR	R11	return
0001120 0001120				547+RE1 548+	DC DROP	OF R5	xl16 expected result
0001120	FFFFFFF FFFFFFF			549	DC		FFFFF FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
0001128 0001130	FFFFFFFF FFFFFFFFFFFFFFFFFFFFFFFFFFFFF			550	DC	YI 16' FFFFFFFFFFF	FFFFF FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
001130	FFFFFFFF FFFFFFF			JJU	ъС	ALIU TETTETETET	THE THEFFEFFFFFF V&
0001140	0000000 00000000			551	DC	XL16' 000000000000	00000 00000000000000000000' v3
0001148	00000000 00000000			552			
				553		VSLDB, 3	
0001150		00001150		554+	DS	0FD * D5	hase for test data and test mouting
0001150 0001150	00001190	00001150		555+ 556+T2	USI NG DC	*, K5 A(X2)	base for test data and test routine address of test routine
0001154	0002			<b>557</b> +	DC	H' 2'	test number
0001156	00			<b>558</b> +	DC	X' 00'	

DOI:	ASMA Ver.	0.7.0 zvector-e7-2	20- VSLDB					03 Apr 2025	15: 40: 04	Page	15
00001118   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   0000128   0000128   00000000   00000000   00000000   000000	LOC	OBJECT CODE	ADDR1	ADDR2	STMT						
00001118   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   00001128   0000128   0000128   00000000   00000000   00000000   000000	00001157	03			559+	DC	HL1' 3'	i4 field			
00001168   00001108   561											
00001164   00000108											
00001168 0000010											
0000116C 0000118B   564+REA2   DC   A(RE2)   Figure   Septimizer   Se											
00001179   00000000 000000000						DC					
00001178   00000000 00000000   564-102   58   XL16   \$\frac{7}{1}\$ \text{ output} \\ 00001188 \\ 000000000 00000000 00000000 \\ 000000											
00001180   00000000 000000000000000000								V1 output			
00001188   00000000   0000000   0000000   568+x   568+x   569+x   568+x   569+x   568+x   569+x   56					00011102	20	1210	VI odepac			
00001190   00001190   0000190   0000190   0000190   0000190   0000190   0000190   0000190   0000190   0000190   0000190   0000000   00000000   0000190   0000000   00000000   00000000   000000						DS	FD	gap			
00001190 E310 5010 0014	00001190				569+X2	DS	<b>OF</b>				
00001196   8761 0000 0806		E310 5010 0014		00000010				load v2 source			
0000119C   E310 5014 0014   00000014 572+   LGF   R1, \( \text{S1DB} \)   10ad \( \text{s1 source} \)   0000118   1760 5008 080   0000178 573+   V.   V.   V.   V.   V.   V.   V.   V				00000000			v22, 0(R1)	use v22 to test decoder			
00001142   E771   0000 0806   00000000   573+   V.L   v.23.0 (R1)   use v.23 to test decoder test instruction (dest is a source)   0000114E   F766 7030 8077   574+   V.SLDB V.22. V.22, v.23.3   test instruction (dest is a source)   00001180   00001180   00001180   00001180   00001180   00001180   00001180   00001180   00001180   00001180   00001180   00000000   00000000   00000000   000000											
00001148   E766 7003 0E77   574+ VSLDB V22, V23, V23, V23											
O00011AE   C765 5028 080E   O0001178   575+   VST				<del>-</del>			V22, V22, V23, 3		is a sour	ce)	
000011B4				00001178							
000011B8											
00001188											
000011B8					<b>578</b> +			<u> </u>			
000011C0 FFFFFFF FF000000		FFFFFFFF FFFFFFFF			579	DC	XL16' FFFFFFFFFFF	'FFFF FFFFFFFFF000000'	resul t		
000011C8 PFFFFFF FFFFFFFF FFFFFFFF 000011D8 00000000 00000000 FFFFFFFF FFFFFFFF											
000011B0 0000000 00000000 00000000 00000000					580	DC	XL16' FFFFFFFFFFF	'FFFF FFFFFFFFFFFFF'	v2		
000011D8         00000000         00000000         581         DC         XL16' 000000000000000000000000000000000000											
S82   VRI_D VSLDB, 7	000011D8				581	DC	XL16' 0000000000000	0000 0000000000000000'	$\mathbf{v3}$		
000011E8	000011E0	00000000 00000000				VRI D	VSLDB. 7				
000011E8         0000128         585+         USING *.R5         base for test data and test routine           000011EC         0003         587+         DC         H'3'         test number           000011EF         00         588+         DC         X'00'           000011EF         07         589+         DC         HL1'7'         i 4 field           000011F0         05223C4         C2404040         590+         DC         CL8'VSLDB'         instruction name           000011F0         00001270         592+         DC         A(RE3+16)         address of v2 source           00001200         000001270         594+         DC         A(RE3+32)         address of v3 source           00001201         00001200         594+REA3         DC         A(RE3)         result address           00001204         00001250         594+REA3         DC         A(RE3)         result address           00001210         00000000         595+         DS         FD         gap           00001210         00000000         596+V103         DS         XL16         V1 output           00001210         00000000         596+V103         DS         FD         gap           00001228	000011E8										
000011E8         00001228         586+T3         DC         A(X3)         address of test routine           000011EF         00003         587+         DC         H'3'         test number           000011EF         07         589+         DC         HL1'7'         i 4 field           00001FF         0589+         DC         HL1'7'         i 4 field           00001F8         00001260         591+         DC         A(RE3+16)         address of v2 source           0000120         0000120         592+         DC         A(RE3+32)         address of v3 source           0000120         0000000         593+         DC         A(RE3)         result length           0000120         0000000         594+REA3         DC         A(RE3)         result address           0000121         00000000         594+REA3         DC         A(RE3)         result address           00001220         00000000         595+         DS         FD         gap           00001210         00000000         596+V103         DS         XL16         V1 output           00001228         00000000         599+X         DS         FD         gap           00001228         E310         50			000011E8					base for test data and	test routi	ne	
000011EC   00003		00001228									
000011EF         00         588+         DC         X' 00'           000011F0         E5E2D3C4         C2404040         590+         DC         CL8' VSLDB'         instruction name           000011F0         00001260         591+         DC         A(RE3+16)         address of v2 source           000011F0         00001270         592+         DC         A(RE3+32)         address of v3 source           00001200         000001201         593+         DC         A(16)         result length           00001220         00000020         594*REA3         DC         A(RE3)         result address           00001220         00000000         595+         DS         FD         gap           00001210         00000000         596*V103         DS         XL16         V1 output           00001220         00000000         596*V103         DS         FD         gap           00001221         00000000         00000000         598+*         DS         FD         gap           00001228         E310 5010 0014         00000124         600+         LGF         R1, V2ADDR         load v2 source           00001234         E310 5014 0014         00004         000*C         LGF         R1,								_			
000011EF         07         589+         DC         HL1'7'         i4 field           000011F0         E5E2D3C4 C2404040         590+         DC         CL8' VSLDB'         instruction name           000011F0         00001260         591+         DC         A(RE3+16)         address of v2 source           00001270         592+         DC         A(RE3+32)         address of v3 source           00001204         00001250         593+         DC         A(RE3)         result length           00001204         00001250         594+REA3         DC         A(RE3)         result address           00001210         0000000         0000000         595+         DS         FD         gap           00001218         00000000         00000000         596+V103         DS         XL16         V1 output           00001228         00000000         00000000         597+         DS         FD         gap           00001228         599+X3         DS         FD         gap           00001228         599+X3         DS         FD         source           00001234         E310 5010 0014         0000000         600+         LGF         R1, V2ADDR         load v2 source							X' 00'				
000011F8         00001260         591+ DC A(RE3+16) A(RE3+32)         address of v2 source address of v3 source           00001200         00001270         592+ DC A(RE3+32)         address of v3 source           00001201         0000010         593+ DC A(RE3)         result length           00001202         00000000         594+REA3 DC A(RE3)         result address           00001210         00000000         595+ DS FD gap         gap           00001218         0000000         596+V103 DS XL16         V1 output           00001220         00000000 00000000         597+ DS FD gap         gap           00001228         598+*         599+X3 DS FD gap         gap           00001228 E310 5010 0014         0000010 600+ LGF R1, V2ADDR load v2 source         load v2 source           00001228 E761 0000 0806 00000000 601+ VL v22, Q(R1) use v22 to test decoder         0001234 E310 5014 0014 0014 00000014 602+ LGF R1, V3ADDR load v3 source           00001234 E771 0000 0806 0000000 603+ VL v23, Q(R1) use v23 to test decoder         0001240 E766 7007 0E77  test instruction (dest is a source)           00001240 E766 7007 0E77	000011EF	07			<b>589</b> +	DC	HL1' 7'	i4 field			
000011FC         00001270         592+         DC         A(RE3+32)         address of v3 source           00001200         000001201         593+         DC         A(16)         result length           00001204         000001208         00000000         594+REA3         DC         A(RE3)         result address           00001210         00000000         595+         DS         FD         gap           00001218         00000000         00000000         596+V103         DS         XL16         V1 output           00001228         00000000         00000000         598+*         DS         FD         gap           00001228         E310         5010         0014         0000010         600+         LGF         R1, V2ADDR         load v2 source           00001228         E761         0000         0806         00000000         601+         VL         v22, 0(R1)         use v22 to test decoder           00001234         E310         5014         0014         00000124         602+         LGF         R1, V3ADDR         load v3 source           00001246         E766         7007         0000124         604+         VSL         VSL         V22, V22, V23, 7         test instruction (dest is a so	000011F0	E5E2D3C4 C2404040			<b>590</b> +	DC	CL8' VSLDB'	instruction name			
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	000011F8	00001260			<b>591</b> +	DC	A(RE3+16)	address of v2 source			
00001200         0000010         593+ DC A(16)         result length           00001204         00001250         594+REA3 DC A(RE3)         result address           00001210         00000000         00000000         595+ DS FD         gap           00001210         00000000         00000000         596+V103 DS XL16         V1 output           00001220         00000000         00000000         597+ DS FD         gap           00001228         598+*         599+X3 DS OF         FD         gap           00001228 E761 0000 0806         00000000 601+ VL V22, O(R1)         use v22 to test decoder           00001234 E310 5014 0014 0014 00000014 602+ LGF R1, V3ADDR load v3 source         load v3 source           00001235 E771 0000 0806 0000000 603+ VL v23, O(R1)         use v23 to test decoder           00001246 E760 9010 080E 00001210 605+ VST V22, V103         save v1 output           00001240 07FB         604+ VSLDB V22, V22, V23, 7         test instruction (dest is a source)           00001250 608+ DR0P R5         800+ R5	000011FC	00001270					A(RE3+32)	address of v3 source			
00001208         00000000         00000000         595+         DS         FD         gap           00001210         00000000         00000000         596+V103         DS         XL16         V1 output           00001218         00000000         00000000         597+         DS         FD         gap           00001228         599+X3         DS         FF         FF         FF         FF           00001228         599+X3         DS         FF         FF         FF         FF           00001228         599+X3         DS         FF         FF         FF         FF           00001228         E761         0000         806         00000000         600+         LGF         R1, V2ADDR         Load v2 source           00001234         E310         5014         0014         0000014         602+         LGF         R1, V3ADDR         Load v3 source           00001234         E771         0000         806         00000000         603+         VL         v23, 0(R1)         use v23 to test decoder           00001240         E766         7007         0E77         604+         VSLDB         V22, V22, V23, 7         test instruction (dest is a source)											
00001208         00000000         00000000         595+         DS         FD         gap           00001210         00000000         00000000         596+V103         DS         XL16         V1 output           00001218         00000000         00000000         597+         DS         FD         gap           00001228         599+X3         DS         FD         gap           00001228         599+X3         DS         OF           00001228         599+X3         DS         OF           00001224         E761         0000         0806         00000000           00001234         E310         5014         0014         00000014         602+         LGF         R1, V3ADDR         load v2 source           00001234         E771         0000         806         00000000         603+         VL         v23, 0(R1)         use v22 to test decoder           00001240         E766         7007         0E77         604+         VSLDB         V22, V22, V23, 7         test instruction (dest is a source)           00001240         07FB         606+         BR         R11         return           00001250         607+RE3         DC         OF         xl16 expect											
00001210       00000000       00000000       596+V103       DS       XL16       V1 output         00001220       00000000       00000000       597+       DS       FD       gap         598+*         00001228       5310       5010       0014       00000000       600+       LGF       R1, V2ADDR       load v2 source         0000122E       E761       0000       00000000       601+       VL       v22, 0(R1)       use v22 to test decoder         00001234       E310       5014       0014       00000000       603+       VL       v23, 0(R1)       use v23 to test decoder         00001240       E766       7007       0E77       604+       VSLDB       V22, V22, V23, 7       test instruction (dest is a source)         00001240       07FB       606+       BR       R11       return         00001250       607+RE3       DC       0F       xl16 expected result         00001250       608+       DROP       R5							FD	gap			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$					596+V103	DS	XL16	V1 output			
00001228       607+RE3       00001228       00001228       E310 5010 0014       00000010       600+       LGF R1, V2ADDR       load v2 source         0000122E       E761 0000 0806       00000000       601+       VL v22, 0(R1)       use v22 to test decoder         00001234       E310 5014 0014       00000000       602+       LGF R1, V3ADDR       load v3 source         0000123A       E771 0000 0806       00000000       603+       VL v23, 0(R1)       use v23 to test decoder         00001240       E766 7007 0E77       604+       VSLDB V22, V22, V23, 7       test instruction (dest is a source)         00001246       E760 9010 080E       00001210       605+       VST V22, V103       save v1 output         00001250       607+RE3       DC 0F       xl 16 expected result         00001250       608+       DROP R5											
598+*   599+X3   DS   OF   O0001228   E310   5010   0014   O0000010   600+   LGF   R1, V2ADDR   load   v2   source   O000122E   E761   0000   0806   O0000000   601+   VL   v22, O(R1)   use   v22   to   test   decoder   O0001234   E310   5014   0014   O0044   O0000014   602+   LGF   R1, V3ADDR   load   v3   source   O000123A   E771   0000   0806   O0000000   603+   VL   v23, O(R1)   use   v23   to   test   decoder   O0001240   E766   7007   0E77   O0001240   E766   7007   0E77   O0001246   E760   9010   080E   O0001210   605+   VST   V22, V23, V23, V23, V23, V24, V25, V25, V25, V25, V25, V25, V25, V25	00001220	00000000 00000000				DS	FD	gap			
00001228       E310       5010       0014       00000010       600+       LGF       R1, V2ADDR       load v2 source         0000122E       E761       0000       0806       00000000       601+       VL       v22, 0(R1)       use v22 to test decoder         00001234       E310       5014       0014       00000014       602+       LGF       R1, V3ADDR       load v3 source         0000123A       E771       0000       603+       VL       v23, 0(R1)       use v23 to test decoder         00001240       E766       7007       0E77       604+       VSLDB       V22, V22, V23, 7       test instruction (dest is a source)         00001246       E760       9010       080E       00001210       605+       VST       V22, V103       save v1 output         00001250       607+RE3       DC       0F       xl16 expected result         00001250       608+       DROP       R5											
$\begin{array}{cccccccccccccccccccccccccccccccccccc$											
00001234       E310       5014       0014       00000014       602+       LGF       R1, V3ADDR       load v3 source         0000123A       E771       0000       0000000       603+       VL       v23, 0(R1)       use v23 to test decoder         00001240       E766       7007       0E77       604+       VSLDB       V22, V22, V23, 7       test instruction (dest is a source)         00001246       E760       9010       080E       606+       BR       R11       return         00001250       607+RE3       DC       0F       xl 16 expected result         00001250       608+       DROP       R5											
$\begin{array}{cccccccccccccccccccccccccccccccccccc$											
$\begin{array}{cccccccccccccccccccccccccccccccccccc$											
$\begin{array}{cccccccccccccccccccccccccccccccccccc$				00000000			v23, 0(R1)				
0000124C 07FB       606+       BR R11       return         00001250       607+RE3 DC 0F xl16 expected result         00001250       608+       DR0P R5				000015:5					is a sour	ce)	
00001250 607+RE3 DC 0F xl 16 expected result 00001250 608+ DR0P R5				00001210							
00001250 608+ DROP R5		O7FB									
								x116 expected result			
00001250 FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF									7.		
	00001250	PEFFFFF FFFFFFFF			609	DC	XL16' FFFFFFFFFFF	FFFF FF0000000000000000000000000000000	result		

	0. 7. 0 zvector- e7- 2						03 Apr 2025	15: 40: 04	Page	16
LOC	OBJECT CODE	ADDR1	ADDR2	STM						
	FF000000 00000000			010	D.C.	VI 401 DDDDDDDDDDDD		0		
	FFFFFFF FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF			610	DC	XL16' FFFFFFFFFFF	'FFF FFFFFFFFFFFF'	v2		
00001270	00000000 00000000			611	DC	XL16' 00000000000000	0000 0000000000000000000000000000000000	v3		
				612 613	VPT D	VSLDB, 8				
00001280				614+	DS	OFD				
0001280	00001000	00001280		615+	USING		base for test data and	test routin	e	
	000012C0 0004			616+T4 617+	DC DC	A(X4) H' 4'	address of test routine test number			
	00			618+	DC	X' 00'				
	08 EFFORCA COAOAOAO			619+	DC		i4 field			
	E5E2D3C4 C2404040 000012F8			620+ 621+	DC DC	CL8' VSLDB' A(RE4+16)	instruction name address of v2 source			
00001294	00001308			622+	DC	A(RE4+32)	address of v3 source			
	0000010			623+	DC		result length			
	000012E8 00000000 00000000			624+REA4 625+	DC DS	A(RE4) FD	result address			
000012A8	0000000 00000000			626+V104	DS	XL16	V1 output			
	00000000 00000000			007.	DC	ED	-			
000012B8	00000000 00000000			627+ 628+*	DS	FD	gap			
000012C0				629+X4	DS	0F				
	E310 5010 0014		00000010	630+	LGF	R1, V2ADDR	load v2 source			
	E761 0000 0806 E310 5014 0014		00000000 0000014	631+ 632+	VL LGF	v22, O(R1) R1, V3ADDR	use v22 to test decoder load v3 source			
000012D2	E771 0000 0806		00000000	633+	VL	v23, 0(R1)	use v23 to test decoder			
	E766 7008 0E77 E760 5028 080E		000012A8	634+ 635+	VSLDB VST	V22, V22, V23, 8	test instruction (dest	is a sourc	<b>e</b> )	
	07FB		000012A6	636+	BR	V22, V104 R11	save v1 output return			
000012E8				637+RE4	DC	<b>OF</b>	xl16 expected result			
000012E8 000012E8	FFFFFFF FFFFFFF			638+ 639	DROP DC	R5	FFF FFFFFFFFFFF08'	resul t		
	FFFFFFF FFFFF08			039	DC	ALIO FFFFFFFFFFF	THE THEFFITTETTETOS	resurt		
000012F8	FFFFFFF FFFFFFF			640	DC	XL16' FFFFFFFFFFFF	'FFF FFFFFFFFFFFF'	<b>v2</b>		
	FFFFFFFF FFFFFFFFFFFFFFFFFFFFFFFFFFFFF			641	DC	VI 16' FFFFFFFFFFFF	FO8 FFFFFFFFFFFFFF	v3		
	FFFFFFF FFFFFFF				DC	ALIO ITTTTTTTTTTT	100 IIIIIFFFFFFFFF	<b>40</b>		
				642	MDT P	UCIND 45				
00001318				643 644+	VRI_D DS	VSLDB, 15 OFD				
00001318		00001318		645+	<b>USING</b>	*, <b>R5</b>	base for test data and	test routin	e	
	00001358			646+T5	DC	A(X5)	address of test routine			
	0005 00			647+ 648+	DC DC	H' 5' X' 00'	test number			
0000131F	<b>0F</b>			649+	DC	HL1' 15'	i4 field			
	E5E2D3C4 C2404040			650+	DC		instruction name			
	00001390 000013A0			651+ 652+	DC DC	A(RE5+16) A(RE5+32)	address of v2 source address of v3 source			
00001330	0000010			653+	DC	A(16)	result length			
	00001380			654+REA5 655+	DC DS	A(RE5) FD	result address			
	00000000 00000000 0000000 00000000			656+V105	DS DS	XL16	gap V1 output			
00001348	0000000 00000000						- 3 <b>43</b> F43			
00001350	0000000 00000000			<b>657</b> +	DS	FD	gap			

ASMA Ver.	0.7.0 zvector-e7-20	- VSLDB					03 Apr 2025	15: 40: 04	Page	17
LOC	OBJECT CODE	ADDR1	ADDR2	STMI						
00001358				658+* 659+X5	DS	<b>0F</b>				
00001358 0000135E	E310 5010 0014 E761 0000 0806	0	00000010	660+ 661+	LGF VL	R1, V2ADDR v22, O(R1)	load v2 source use v22 to test decoder			
0000136A	E310 5014 0014 E771 0000 0806 E766 700F 0E77		00000014	662+ 663+ 664+	VL	,	load v3 source use v23 to test decoder test instruction (dest	is a sourc	e)	
00001376 0000137C	E760 5028 080E 07FB	0	00001340	665+ 666+	VST BR	V22, V105 R11	save v1 output return		-,	
00001380 00001380 00001380				668+		<b>R5</b>	xl16 expected result TFFF 08FFFFFFFFFFFFF	magul +		
00001380 00001388 00001390	0FFFFFF FFFFFFF 08FFFFFF FFFFFFF 00010203 04050607						607 08090A0B0C0D0E0F'	result v2		
00001398 000013A0							FO8 FFFFFFFFFFFFF	<b>v</b> 3		
000013A8	FFFFFFF FFFFFFF			672 673 * Ignore:	Bits	0-3 of the fourth	operand should contain			
				674 * 675 *			sults are unpredictable.			
				676 * 677 *		VSLDB, 16 XL16' FFFFFFFFFFFF	'FFF FFFFFFFFFFFF'	resul t		
				678 *	DC	XL16' FFFFFFFFFFFF	FFF FFFFFFFFFFFFFF 010 7060504030201000'	v2 v3		
					DC		FFF FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	result v2		
				684 * 685 *	DC	XL16' FOEODOCOBOA09	010 7060504030201000'	v3		
				<b>688</b> *	DC DC	XL16' FOEODOCOBOA09	080 7060504030201000' 080 7060504030201000' 030 0000000000000000'	result v2 v3		
000013B0	00000000			690 691 692	DC	F'O' END OF TA	RI F			
000013B4	00000000			693 694 *	DC	F'0' nters to individual				
000013B8				696 * 697 E7TESTS	•	<b>OF</b>	Todu test			
000013B8 000013B8	000010B8			699+TTABLE 700+	DS DC	0F A(T1)				
000013BC 000013C0 000013C4	00001150 000011E8 00001280			702+ 703+	DC DC	A(T2) A(T3) A(T4)				
000013C8 000013CC	00001318 00000000			705+* 706+	DC	` /	END OF TABLE			
000013D0 000013D4	00000000			708		A(0) F' O' END OF TA	BLE			
000013D8	00000000					F' 0'				

ASMA Ver.	0. 7. 0 zvector- e7- 2	20- VSLDB				03 Apr 2025 15: 40: 04 Page	18
LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
					*****	*******************	
				712 ************************************		·*************************************	
				714 ******	*****	·*************************************	
		00000000	00000001	716 RO	EQU 0		
		00000001 00000002	00000001 00000001	717 R1 718 R2	EQU 1 EQU 2		
		00000003	0000001	719 R3	EQU 3		
		00000004 00000005	00000001 00000001	720 R4 721 R5	EQU 4 EQU 5		
		00000006	0000001	722 R6	EQU 6		
		00000007 00000008	00000001 00000001	723 R7 724 R8	EQU 7 EQU 8 EQU 9		
		00000009	0000001	725 R9	EQU 9		
		0000000A 0000000B	00000001 00000001	726 R10 727 R11	EQU 1 EQU 1	10 1	
		000000C	0000001	728 R12	EQU 1		
		0000000D 0000000E	00000001 00000001	729 R13 730 R14	EQU 1 EQU 1	12 13 14	
		000000F	0000001	731 R15	EQU 1	15	
				733 ******* 734 *		·*************************************	
				735 *****	******	er equates ************************************	
		0000000	0000001	737 VO	EQU 0		
		00000001 00000002	00000001 00000001	738 V1 739 V2	EQU 1 EQU 2		
		0000003	00000001	740 V3	EQU 3		
		$00000004 \\ 00000005$	$00000001 \\ 00000001$	741 V4 742 V5	EQU 4		
		00000003	00000001	742 V3 743 V6	EQU 5 EQU 6		
		00000007 00000008	00000001 00000001	744 V7 745 V8	EQU 7		
		00000008	00000001	745 V8 746 V9	EQU 8 EQU 9		
		0000000A	00000001	747 V10	EQU 1	10	
		0000000B 0000000C	00000001 00000001	748 V11 749 V12	EQU 1	1 12	
		000000D 000000E	0000001	750 V13 751 V14	EQU 1	13 14	
		000000F	00000001 00000001	752 V15	EQU 1	15	
		$00000010 \\ 00000011$	00000001 00000001	753 V16 754 V17	EQU 1	16 17	
		0000012	0000001	755 V18	EQU 1	18	
		$00000013 \\ 00000014$	00000001 00000001	756 V19 757 V20	EQU 1 EQU 2	19 20	
		00000014	00000001	758 V21		21	

	0. 7. 0 zvector- e7	20 ISLDD						оз Ар	r 2025 15	. 10. 01	rage	19
LOC	OBJECT CODE	ADDR1	ADDR2	STMI								
		00000016	00000001	759 V22	EQU	22						
		00000017 00000018	00000001 00000001	760 V23 761 V24	EQU EQU	23 24						
		00000019 0000001A	00000001 00000001	762 V25 763 V26	EQU FOU	25 26						
		0000001B	0000001	764 V27	EQU EQU EQU EQU EQU EQU EQU EQU EQU	22 23 24 25 26 27 28 29 30 31						
		0000001C 0000001D	00000001 00000001	765 V28 766 V29	EQU EQU	28 29						
		0000001E 0000001F	00000001	767 V30 768 V31	EQU	30						
		000001F	0000001	<b>769</b>		31						
				770	END							

TITIO I 00000200	SYMBOL	ТҮРЕ	VALUE	LENGTH	DEEN	BEEE	'RENCE	S												_	
TIRRO F 000004RC 4 347 162 8 282 264 270 272  TESTS 4 000010074 16 388 282 264 270 272  TESTS 4 00001008 64 412 214  TESTS 4 000010148 18 393 263 271  TESTS 4 000010168 18 393 361  I 00000470 4 337 197  JIPSW D 0000470 4 337 3197  JIPSW D 00000470 4 337 3197  JIPSW D 0000048 8 333 337  MILES T 0 00000000 1 320 249  MILES T 0 00000000 1 320 249  MILES T 0 00000000 5 8 4 341 252  MILES T 1 00000000 5 8 4 341 252  MILES T 1 00000000 5 8 3 341  MILES T 1 00000000 5 8 4 341 252  MILES T 1 00000000 5 8 4 341 252  MILES T 0 00000000 5 8 181 25		1111																			
ENIM C 00001074 16 308 262 244 270 272  TRISTS F 00001088 4 682 204  TRISTS F 00001088 1 8 32 271  TRISTS F 00001070 4 337 197 251  JULY TRISTS F 00001070 4 337 197 251  JULY TRISTS F 00001000 1 1 238  JULY TRISTS F 00001000 1 2 238  JULY TRISTS F 000010			00000200	2					<b>150</b>												
TTESTS	ΓLRO	F	0000048C	4	347	162	163	164	165												
TTESTS	ECNUM	C	00001074	16	398	262	264	270	272												
THESTS F 00001388 4 697 204 DITT X 00001048 18 303 263 271 UTLEST U 00000311 1 248 207 251 UTLEST U 00000312 1 248 207 251 UTLEST U 00000305 1 238  ALLED F 00001000 4 375 240 ALLED F 00000300 1 232 ALLED F 00000300 1 232 ALLED F 00000000 1 300 304 10 20 20 20 20 20 20 20 20 20 20 20 20 20		4																			
DIT X 00001048 18 393 263 271 WITSTST U 00000476 4 337 197 251 U 0000476 4 337 197 251 U 0000476 4 337 197 251 U 0000476 6 32 337  ALLED F 00001000 4 375 240 249 ALLED F 00001000 4 375 240 249 ALLED F 00001000 1 375 240 249 ALLED F 00001000 1 384 341 252 ALLES U 0000478 8 3 339 341 ALLES T 00000478 8 3 341 252 ALLES U 0000478 8 3 341 252 ALLES U 0000487 8 3 341 252 ALLES U 0000480 1 361 362 ALLES U 0000480 1 361 362 ALLES U 00000400 1 361 361 B U 0000400 1 361 362 B U 0000400 1 361 362 B U 0000400 1 362 B U 0000487 9 5 328 304 325 302 B U 000038F 9 5 328 304 325 302 B SCAD C 000038F 9 5 328 304 325 302 B SCAD C 000038F 9 5 328 304 325 302 B SCAD C 000038F 9 5 328 304 325 302 B SCAD C 000038F 9 5 328 304 325 302 B SCAD C 0000038F 9 5 328 304 325 302 B SCAD C 0000038F 9 5 328 304 325 302 B SCAD C 0000038F 9 5 328 304 325 302 B SCAD C 0000038F 9 5 328 304 325 302 B SCAD C 0000038F 9 5 328 304 325 302 B SCAD C 0000000 B 4 321 314 317 B SCAN C C 0000038F 9 5 328 306 303 B SCAD C 0000000 B 4 324 304 307 B SCAN C C 00000038F 9 5 328 306 303 B SCAD C C 00000038F 9 5 328 306 303 B SCAD C C 00000038F 9 5 328 306 303 B SCAD C C 00000008 B 4 324 300 321 B SCAN C C 00000038F 9 5 328 306 303 B SCAD C C 00000008 B 4 324 300 321 B SCAN C C 00000008 B 4 324 300 321 B SCAN C C 00000008 B 4 324 300 321 B SCAN C C 00000000 B 4 324 300 321 B SCAN C C 00000000 B 4 324 300 300 300 300 300 300 300 300 300 30		Ē		_																	
NOTEST U 0000031E 1 248 209 10 00000470							271														
0.0		II		10			~ ' 1														
0.JPSW   D   0.0000460   8   335   337   337   337   338   337   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   338   3		T		1			951														
ALICONT U 0000030E 1 238 ALICONT U 0000030R 375 240 249 ALIANG U 0000030A 1 375 240 249 ALIANG U 0000030A 1 375 240 249 ALIANG U 0000030A 1 339 342 BOOLT F 00000280 8 181 185 186 188 ALICONT U 00000007 1 416 269 BOOLT F 00000280 8 181 185 186 188 ALICONT U 00000000 1 361 361 ALICONT U 00000000 1 361 361 BOOLT F 00000280 1 361 362 BOOLT F 00000000 1 361 361 BOOLT F 00000000 1 361 362 BOOLT F 000000000 1 361 363 BOOLT F 000000000 1 361 363 BOOLT F 000000000 1 361 362 BOOLT F 000000000 1 361 363 BOOLT F 00000000 1 361 363 BOOLT F 000000000 1 361 363 BOOLT F 000000000 1 361 363 363 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 360 361 362 363 3		D I			337		231														
AILED F 00001000 4 375 240 249				8	333	337															
AILMSG U 0000030A 1 232 222 AILTEST I 00000478 8 339 341 AILTEST I 00000478 8 339 341 AILTEST I 00000007 1 416 289  MACE I 000000007 1 416 289  MACE I 00000000 1 361 B U 00100000 1 361 B U 00100000 1 362 B U 00100000 1 362 B U 00100000 1 362 B U 00000000 1 363 B U 00000000 1 363 B U 00000000 1 368 B U 00000000 1 766 B S 263 B S 204 B				1		0.40	0.40														
ALIPSW   D		F		4			249														
AllTEST I 00000488		U		1																	
BROOL   F	AILPSW	D	00000478	8	339	341															
BOOOL   F	AI LTEST	I	00000488	4	341	252															
MGC 1 00000000 5084 0		F					186	188													
MGE   1 00000000   5084   0     1 359   360   361   362		Ū		1																	
U		ĭ		5084		~00															
64 U 00010000 1 361  B U 00100000 1 362  6G I 0000384 4 297 196 280  6GCMD C 000003F6 9 327 310 311  6GMCG C 000003F7 95 328 304 325 302  6GMC I 000003F0 6 325 308  6GMC I 000003F0 6 325 308  6GMC I 000003F0 6 325 308  6GOK I 000003F0 4 321 314  317  6GSAVC I 000003F2 4 321 314  5GSAVE F 000003F4 4 324 300 321  EXTET U 0000002F4 1 206 225 243  PMAME C 00001000 1 360  RT3 C 00001000 1 380  RT3 C 00001044 3 386 273  RT1LINE C 00001044 3 386 273  RT1LINE C 00001048 16 381 388 279  RT1LINE C 0000108 16 381 388 279  RT1LINE C 0000108 3 8 384 267  RTNAME C 0000108 3 8 384 267  RTNAME C 0000108 1 380  0 U 00000000 1 716 297 300 302 304 306 321 313 325 540 541 542 543 570 571 572  570  10 U 00000000 1 776 513 600 603 603 631 632 633 660 661 662 663  10 U 00000000 1 726 204 242 242  10 U 00000000 1 728 204 207 224 242  10 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  11 U 00000000 1 728 204 207 224 242  13 U 00000000 1 728 204 207 224 242  13 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  15 U 00000000 1 728 204 207 224 242  16 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  17 U 00000000 1 728 204 207 224 242  18 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  18 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  18 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  20 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  21 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  22 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  23 U 00000000 1 728 204 207 207 277 280 281 298 300 306 307 308 310 316  24 U 00000000 1 728 204 207 227 280 281 298 300 306 307 308 310 316  25 U 00000000 1 728 204 207 208 211 259 283 525 548 555 578 585 608 615 638 645 668  25 U 00000000 1 728 244 242 242 242 242 242 242 242 242 2		ij		1		360	361	362													
BE		II		1	203 201	300	301	302													
SGCM I 00000348		U		1																	
SGCMD C 000003FF 95 328 304 325 302   SGMSC C 000003FF 95 328 304 325 302   SGMSC I 000003FF 95 328 304 325 308   SGMSC I 000003FF 95 328 304 325 308   SGMSC I 000003FF 95 328 304 308 321   SGMSC I 000003FF 95 328 304 308 321   SGMSC I 000003FF 95 328 308 321   SGMSC I 0000003FF 95 328 308 321   SGMSC I 0000003FF 95 328 308 321   SGMSC I 0000003FF 95 328 328 328   SGMSC I 0 0000005F 95 328 328 328   SGMSC I 0 0000005F 95 328 328 328   SGMSC I 0 0000005F 95 328 328 328   SGMSC I 0 00000005F 95 328 328 328   SGMSC I 0 00000000F 95 328 304 308 321   SGMSC I 0 00000000F 95 328 304 308 321   SGMSC I 0 00000000F 95 328 304 308 321   SGMSC I 0 00000000F 95 328 304 308 321   SGMSC I 0 00000000F 95 328 304 308 321   SGMSC I 0 00000000F 95 328 304 308 321   SGMSC I 0 00000000F 95 328 304 308 321   SGMSC I 0 00000000F 95 328 304 308 308 308 308 308 308 308 308 308 308		U		I A		100	000														
SGMG   C   000003FF   95   328   304   325   308   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   305   3		I																			
SGMC I 000003BE 2 306 305 SGOK I 000003BE 2 306 305 SGOK I 000003BE 2 306 305 SGOK I 000003BE 4 321 314 317 SGOSAVE F 000003E4 4 321 314 317 SGOSAVE F 000003E4 1 206 225 243 PAMME C 000000008 8 418 267 AGE U 0000105E 18 306 263 264 265 271 272 273 RT14 C 0000105E 18 306 263 264 265 271 272 273 RT14 C 0000105E 18 306 263 264 265 271 272 273 RT14 C 00001044 3 386 273 ST14 C 00001044 3 386 275 ST14 C 00001044 3 386 267 ST14 C 00001044 3 388 279 ST14 C 00001044 3 388 279 ST14 C 00001048 3 384 267 ST14 C 00001048 3 384 267 ST14 C 00001048 3 388 2 265 ST14 C 00000000																					
SGOK I 000003BE 2 306 303 SKGRET I 000003DE 4 321 314 317 SKGRET I 000003E4 4 324 300 321 SKRET I 000002B4 1 206 225 243 SKRET I 0000002B4 1 206 225 243 SKRET I 0000002B4 1 206 225 243 SKRET I 000001000 1 360 SKRET I 00001000 1 386 SKRET I 00001000 1 388 273 SKRET I 000000000 1 388 278 SKRET I 000000000 1 388 278 SKRET I 000000000 1 388 278 SKRET I 000000000 1 716 112 162 165 185 187 188 189 194 213 214 239 240 277 278 281 SKRET I 00000000 1 716 112 162 165 185 187 188 189 194 213 214 239 240 277 278 281 SKRET I 00000000 1 716 112 162 165 185 187 188 189 194 213 214 239 240 277 278 281 SKRET I 00000000 1 716 112 162 165 185 187 188 189 194 213 214 239 240 277 278 281 SKRET I 00000000 1 716 112 162 165 185 187 188 189 194 213 214 239 240 277 278 281 SKRET I 00000000 1 718 195 220 221 249 250 279 311 325 540 541 542 543 570 571 572 SKRET I 00000000 1 728 204 207 224 242 13 10 00000000 1 728 204 207 224 242 13 10 00000000 1 729 14  00000000 1 729 14  00000000 1 731 233 258 284 285 12  10 00000000 1 731 233 258 284 285 12  10 00000000 1 731 233 258 284 285 12  10 00000000 1 729 14  00000000 1 729 14  00000000 1 729 14  00000000 1 729 14  00000000 1 720 15  10 00000000 1 720 15  10 0000000 1 720 15  10 00000000 1 720 15  10 00000000 1 720 15  10 00000000 1 720 15  10 00000000 1 720 15  10 00000000 1 722 10 00000000 1 723 10 00000000 1 723 10 0000000 1 723 10 00000000 1 723 10 00000000 1 723 10 0000000 1 723 10 00000000 1 724 148 152 153 154 156 150 150 150 150 150 150 150 150 150 150		C					325	302													
SGRET I 000003DE 4 321 314 317 SGSAVE F 000003DE 1 200 321 SEXTET U 000002D4 1 206 225 243 SEXTET U 000002D4 1 206 225 243 SEXTET U 00000008 8 418 267 SEXTET U 00001000 1 360 SEX	<b>SGMVC</b>	I	000003F0	6		<b>308</b>															
SGRET         I         000003DE         4         321         314         317         SGSAVE         F         000003F4         4         324         300         321         SETET         U         000002D4         1         206         225         243         PAME         C         00000008         8         418         267         AGE         U         00001000         1         360         PRAME         C         00001040         1         360         PRAME         C         00001044         3         386         273         272         273         RTIAG         C         00001044         3         386         273         278         273         273         273         273         273         273         273         274         274         275         277         278         281         278         281         279         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281         281 <td><b>I</b>SGOK</td> <td>I</td> <td>000003BE</td> <td>2</td> <td>306</td> <td>303</td> <td></td>	<b>I</b> SGOK	I	000003BE	2	306	303															
SGSAVE F 000003E4		I	000003DE	4			317														
EXTE7 U 00000204 1 206 225 243 PNAME C 00000008 8 418 267 AGE U 0000105E 18 366 RT3 C 0000105E 18 366 RT4 C 0000105E 18 366 RT5 C 0000105E 18 366 RT5 C 0000105E 18 366 RT6 U 00000008 16 381 388 273 RTLINE C 00001044 3 388 278 RTLINE C 00001008 16 381 388 278 RTLINE C 00001018 3 382 265 U 00000000 1 716 112 165 185 187 188 189 194 213 214 239 240 277 278 281 RTNMME C 00001018 3 382 265 U 00000000 1 716 112 165 185 187 188 189 194 213 214 239 240 277 278 281  1 U 00000000 1 716 112 165 185 187 188 189 194 213 214 239 240 277 278 281  1 U 00000000 1 717 195 220 221 249 250 279 311 325 540 541 542 543 570 571 572  10 U 0000000 1 726 150 159 160 11 U 0000000B 1 726 150 159 160 11 U 0000000B 1 729 141 218 546 576 606 636 666 12 U 0000000E 1 730 151 159 159 159 159 159 159 159 159 159		F		4																	
PNAME C 00000008 8 418 267  AGE U 0000105E 18 396 263 264 265 271 272 273  RT14 C 0000105E 18 396 263 264 265 271 272 273  RT14 C 00001044 3 3886 273  RTL1NE C 00001044 1 388 278  RTL1NG U 00000040 1 388 278  RTNAME C 00001018 3 382 265  0 U 00000000 1 716 112 162 165 185 187 188 189 194 213 214 239 240 277 278 281  RTNUM C 0000000 1 717 195 220 221 249 250 279 311 325 540 541 542 543 570 571 572		Ū		1																	
AGE   U 00001000		Č		Ŕ	418		~ 10														
RT3				1		201															
RT14				10		969	964	965	971	979	979										
RTLINE C 00001008 16 381 388 279 RTNOM U 00000040 1 388 278 RTNOM C 00001013 8 384 267 RTNUM C 00001018 3 382 265 0 U 00000000 1 716 112 162 165 185 187 188 189 194 213 214 239 240 277 278 281 1 U 00000001 1 717 195 220 221 249 250 279 311 325 540 541 542 543 570 571 572 10 U 00000000 1 726 150 159 160 11 U 00000000 1 726 150 159 160 11 U 00000000 1 727 217 218 546 576 606 636 666 12 U 00000000 1 729 14 U 00000000 1 729 15 U 00000000 1 730 15 U 00000000 1 731 233 258 284 285 2 U 00000000 1 730 321 322 3 U 00000000 1 720 4 U 00000000 1 720 5 U 00000000 1 720 5 U 00000000 1 720 5 U 00000000 1 720 6 U 00000000 1 720 6 U 00000000 1 720 6 U 00000000 1 720 7 U 00000000 1 720 7 U 00000000 1 722 7 U 00000000 1 722 7 U 00000000 1 723 8 U 00000000 1 725 149 156 157 159					390		204	203	211	212	213										
RTING U 00000040 1 388 278 RTNAME C 00001033 8 384 267 RTNAME C 00001018 3 382 265 0 U 00000000 1 716 112 162 165 185 187 188 189 194 213 214 239 240 277 278 281 297 300 302 304 306 321							070														
RTNAME C 00001033 8 384 267 RTNUM C 00001018 3 382 265 0 U 00000000 1 716 112 162 165 185 187 188 189 194 213 214 239 240 277 278 281 1 U 00000001 1 717 195 220 221 249 250 279 311 325 540 541 542 543 570 571 572 573 600 601 602 603 630 631 632 633 660 661 662 663 10 U 0000000A 1 726 150 159 160 11 U 0000000B 1 727 217 218 546 576 606 636 666 12 U 0000000C 1 728 204 207 224 242 13 U 0000000C 1 728 204 207 224 242 13 U 0000000E 1 730 15 U 0000000F 1 731 233 258 284 285 2 U 0000000F 1 731 233 258 284 285 2 U 0000000F 1 731 233 258 284 285 2 U 0000000F 1 731 233 258 284 285 2 U 0000000F 1 731 233 258 284 285 2 U 0000000F 1 731 233 258 284 285 2 U 0000000F 1 731 233 258 284 285 2 U 0000000F 1 731 233 258 284 285 2 U 0000000F 1 731 233 258 284 285 2 U 0000000F 1 731 232 25 3 U 00000005 1 721 207 208 211 259 283 525 548 555 578 585 608 615 638 645 668 4 U 00000006 1 722 7 U 00000006 1 722 7 U 00000006 1 723 8 U 00000008 1 724 148 152 153 154 156				16			279														
RTNUM C 00001018 3 382 265		_		1																	
0       U       00000000       1       716       112       162       165       185       187       188       189       194       213       214       239       240       277       278       281         1       U       00000001       1       717       195       220       221       249       250       279       311       325       540       541       542       543       570       571       572         10       U       0000000A       1       726       150       159       160       159       160       159       160       159       160       159       160       159       160       159       160       159       160       159       160       159       160       160       160       185       185       185       632       633       660       661       662       663       663       663       661       662       663       663       664       662       663       663       666       663       666       663       666       663       666       663       666       663       663       664       663       664       663       664       664       663																					
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	RTNUM	C	00001018	3	382	<b>265</b>															
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	20	U	00000000	1	716	112	162	165	185	187	188	189	194	213	214	239	240	277	278	281	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						297		302	304		321										
10	.1	U	00000001	1	717							311	325	540	541	542	543	570	571	572	
10 U 0000000A 1 726 150 159 160 11 U 0000000B 1 727 217 218 546 576 606 636 666 12 U 0000000C 1 728 204 207 224 242 13 U 0000000D 1 729 14 U 0000000E 1 730 15 U 0000000F 1 731 233 258 284 285 2 U 00000002 1 718 196 261 262 269 270 277 280 281 298 300 306 307 308 310 316 321 322 33 U 00000004 1 720 4 U 00000004 1 720 5 U 00000005 1 721 207 208 211 259 283 525 548 555 578 585 608 615 638 645 668 6 U 00000006 1 722 7 U 00000007 1 723 8 U 00000008 1 724 148 152 153 154 156 9 U 00000009 1 725 149 156 157 159	_	ŭ		-															~	J . ~	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	±10	Tī	0000000	1	79 <b>6</b>				30 <i>k</i>	500	550	<b>5</b> 01	30 <i>k</i>	000	500	<b>501</b>	30 <i>k</i>	000			
12		II		1					576	ይበይ	626	222									
13		U		1						000	030	000									
14       U       0000000E       1       730         15       U       0000000F       1       731       233       258       284       285         2       U       00000002       1       718       196       261       262       269       270       277       280       281       298       300       306       307       308       310       316         3       U       00000003       1       719       720       721       207       208       211       259       283       525       548       555       578       585       608       615       638       645       668         U       00000006       1       722       723       724       148       152       153       154       156       156       157       159       156       157       159       156       157       159       156       157       159       156       157       159       156       157       159       156       157       159       156       157       159       156       157       159       156       157       159       156       157       159       156       157       15		U		1		۵U4	207	<b>4</b>	242												
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		U		1																	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		U		1		000	0-0	00.	00-												
321 322 3		<u>U</u>		1																	
3     U     00000003     1     719       4     U     00000004     1     720       5     U     00000005     1     721     207     208     211     259     283     525     548     555     578     585     608     615     638     645     668       6     U     00000006     1     722       7     U     00000007     1     723       8     U     00000008     1     724     148     152     153     154     156       9     U     00000009     1     725     149     156     157     159	2	U	0000002	1	718			<b>262</b>	<b>269</b>	<b>270</b>	277	<b>280</b>	281	298	<b>300</b>	<b>306</b>	<b>307</b>	<b>308</b>	310	316	
3     U     00000003     1     719       4     U     00000004     1     720       5     U     00000005     1     721     207     208     211     259     283     525     548     555     578     585     608     615     638     645     668       6     U     00000006     1     722       7     U     00000007     1     723       8     U     00000008     1     724     148     152     153     154     156       9     U     00000009     1     725     149     156     157     159						321	322														
4     U     00000004     1     720       5     U     00000005     1     721     207     208     211     259     283     525     548     555     578     585     608     615     638     645     668       6     U     00000006     1     722       7     U     00000007     1     723       8     U     00000008     1     724     148     152     153     154     156       9     U     00000009     1     725     149     156     157     159	.3	U	0000003	1	719																
5     U     00000005     1     721     207     208     211     259     283     525     548     555     578     585     608     615     638     645     668       6     U     00000006     1     722       7     U     00000007     1     723       8     U     00000008     1     724     148     152     153     154     156       9     U     00000009     1     725     149     156     157     159		Ū		1																	
16     U     00000006     1     722       17     U     00000007     1     723       18     U     00000008     1     724     148     152     153     154     156       19     U     00000009     1     725     149     156     157     159		II		1		207	208	211	250	283	525	548	555	578	585	602	615	638	645	668	
7 U 00000007 1 723 8 U 00000008 1 724 148 152 153 154 156 9 U 0000009 1 725 149 156 157 159		II		1		~01	~00	~11	~00	~00	<i>0 ~ 0</i>	UTU	555	010	565	000	010	000	UTU	000	
8 U 00000008 1 724 148 152 153 154 156 9 U 00000009 1 725 149 156 157 159		U		1																	
9 U 00000009 1 725 149 156 157 159	7	U	<b>UUUUUUU/</b>	I.		1.10	150	150	1 ~ 4	150											
9 U 00000009 1 725 149 156 157 159		TI	00000000																		
E1 F 00001120 4 547 531 532 534	8	_		1						130											

SYMBOL	TYPE	VALUE	LENGTH	DEFN	DEED	RENCE	'C													
SINDUL	IIFE	VALUE	LENGIN	DEFN	KEFE	RENCE	io													
<b>E2</b>	F	000011B8	4	577	<b>561</b>	<b>562</b>	<b>564</b>													
<b>E3</b>	F	00001250	4	607	<b>591</b>	<b>592</b>	<b>594</b>													
<b>E4</b>	F	000012E8	4	637	621	622	624													
<b>E</b> 5	F	00001380	4	667	651	652	654													
EA1	A	000010D4	4	<b>534</b>																
EA2	A	0000116C	4	<b>564</b>																
EA3	Ā	00001204	$\bar{4}$	<b>594</b>																
EA4	Ä	0000129C	$\overline{4}$	624																
EA5	A	00001334	$\overline{4}$	654																
EADDR	Ä	0000001C	4	422	220															
EG2LOW	Ü	000000TC	1	365	~~0															
EG2PATT	Ü	AABBCCDD	1	364																
ELEN		00000018	1	421																
TDWSAV	A	00000018	4 8		977	281														
	D		_	290	277	<b>∠01</b>														
TERROR	1 E	0000032C	4	258	233	904														
TSAVE	F	00000390	4	287	258	284														
TSVR5	F	00000394	4	288	259	283														
L0001	Ų	0000004E	1	178	194															
T0001	<u>C</u>	0000022A	20	175	178	195														
OLDPSW	Ų	00000140	0	114																
-	A	000010B8	4	<b>526</b>	<b>700</b>															
	A	00001150	4	<b>556</b>	701															
}	A	000011E8	4	<b>586</b>	702															
	A	00001280	4	616	703															
	A	00001318	4	646	704															
ESTING	F	00001004	4	376	214															
IUM	H	00000004	2	414	213	261														
SUB	$\overline{\mathbf{A}}$	00000000	4	413	217															
ABLE	F	000013B8	$ar{4}$	699																
	Ū	00000000	1	737																
	Ŭ	00000001	î	738	216															
.0	Ŭ	00000001 0000000A	1	747	210															
.1	Ü	0000000A	1	748																
2	Ü	0000000B	1	748 749																
	Ü	0000000C	1	749 750																
	U TI		1																	
.4	U	000000E	1	751 759																
.5	U	0000000F	1	752 752																
6	U	00000011	ļ	753																
7	U	00000011	1	754																
8	Ü	00000012	1	755																
9	Ü	00000013	1	756	010															
FUDGE	X	00001094	16		216															
.01	X	000010E0	16		<b>545</b>															
02	X	00001178	16	566	575															
03	X	00001210	16	<b>596</b>	605															
04	X	000012A8	16	626	635															
05	X	00001340	16	656	665															
OUTPUT	X	00000028	16	424	221															
}	U	00000002	1	739																
<b>20</b>	Ŭ	00000014	1	757																
1	Ŭ	00000011	1	758																
22	II	00000013	1	759	<b>541</b>	<b>544</b>	<b>545</b>	571	<b>574</b>	575	601	604	605	631	634	635	661	664	665	
23	II	00000017	1	760	<b>543</b>	<b>544</b>	573	574	603	604	633	634		664	001	000	001	<b>501</b>	000	
24	II	00000017	1	761	J <b>T</b> J	777	010	374	003	<del>504</del>	000	<del>004</del>	000	UU4						
	I		1																	
25 2 <b>6</b>	U U	00000019 0000001A	1	762 763																



