in ver.	0. 7. 0 zvector- e7-	10- ADI EWM		03 Apr 2025 15: 39: 31 Page
LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 ************************************
				4 * Zvector E7 instruction tests for VRR-c encoded: 5 *
				6 * E785 VBPERM - Vector Bit Permute
				7 * 8 * James Wekel March 2025 9 ************************************
				11 *******************
				12 * 13 * basic instruction tests 14 *
				15 ************************************
				17 * Vector Bit Permute instruction.
				18 * 19 * Exceptions are not tested. 20 *
				21 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch 22 * obvious coding errors. None of the tests are thorough. They are 23 * NOT designed to test all aspects of any of the instructions.
				24 * 25 ********************************
				27 * *Testcase zvector-e7-18-VBPERM 28 * *
				30 * *
				31 * * E785 VBPERM - Vector Bit Permute 32 * *
				33 * * #
				36 * * #
				38 * mainsize 2
				39 * numcpu 1 40 * sysclear
				41 * archl vl z/Arch 42 *
				43 * loadcore "\$(testpath)/zvector-e7-18-VBPERM core" 0x0 44 *
				45 * diag8cmd enable # (needed for messages to Hercules console) 46 * runtest 5 47 * diag8cmd disable # (reset back to default)
				48 *
				50 * 51 **********************************

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI		
				53 *****	********************	*****
				54 *	FCHECK Macro - Is a Facility Bit set?	
				55 * 56 *	If the facility bit is NOT set, an message is issued and	i
				57 * 58 *	the test is skipped.	
				59 *	Fcheck uses R0, R1 and R2	
				60 * 61 * eg. 62 ******	FCHECK 134, 'vector-packed-decimal'	
				62 ******* 63	**************************************	·****
				64	FCHECK &BITNO, &NOTSETMSG	
				65 . * 66 . *	&BITNO: facility bit number to check &NOTSETMSG: 'facility name'	
				67 68	LCLA &FBBYTE Facility bit in Byte	
				69	LCLA &FBBIT Facility bit within Byte	
				70 71 &L(1)	LCLA &L(8) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte	
				72	·	
				73 &FBBYTI 74 &FBBIT	SETA &BITNO/8 SETA &L((&BITNO-(&FBBYTE*8))+1)	
				75 . * 76	MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBB	iIT'
				77	B X&SYSNDX	
				78 * 79 *	Fcheck data area skip messgae	
				80 SKT&SYS 81	OX DC C' Skipping tests: ' DC C&NOTSETMSG	
				82	DC C' (bit &BITNO) is not installed.'	
				83 SKL&SYS 84 *	OX EQU *-SKT&SYSNDX facility bits	
				85 86 FB&SYS!	DS FD gap	
				87	DS FD gap	
				88 * 89 X&SYSNI	EQU *	
				90	LA RO, ((X&SYSNDX-FB&SYSNDX)/8)-1	
				91 92	STFLE FB&SYSNDX get facility bits	
				93 94	XGR RO, RO IC RO, FB&SYSNDX+&FBBYTE get fbit byte	
				95	N RO, =F' &FBBIT' is bit set?	
				96 97 *	BNZ XC&SYSNDX	
					ty bit not set, issue message and exit	
				100	LA RO, SKL&SYSNDX message length	
				101 102	LA R1, SKT&SYSNDX message address BAL R2, MSG	
				103 104		
				105 XC&SYSI	K EQU *	
				106	MEND	

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LOC	OBJECT CODE	ADDR1	ADDR2	STM					
				109 *		Low co	ore PSWs	**********	
00000000		00000000 00000000	0000163B	111 ZV 112	VE7TST S	START		Low core addressability	
		00000140	00000000	113 114 SV	VOLDPSW H	E Q U	ZVE7TST+X' 140'	z/Arch Supervisor call old PSW	
0000000 000001A0 000001A8	00000001 80000000 00000000 00000200	00000000	000001A0	116 117 118	Ι	DC	ZVE7TST+X' 1A0' X' 000000018000000 AD(BEGIN)	z/Architecure RESTART PSW	
000001110	0000000 00000200			110	•		AD (DEGIN)		
000001B0 000001D0 000001D8	00020001 80000000 00000000 0000DEAD	000001B0	000001D0	120 121 122	Ι	ORG DC DC	ZVE7TST+X' 1D0' X' 000200018000000 AD(X' DEAD')	z/Architecure PROGRAM CHECK PSW 00'	
							, ,		
000001E0		000001E0	00000200	124	(ORG	ZVE7TST+X' 200'	Start of actual test program	
				129 * 130 * 131 *	******** ******* Archi te Regi ste	ecture	************* e Mode: z/Arch	**************************************	
				132 * 133 * 134 *	RO R1-4		vork) vork)		
				135 * 136 * 137 *	R5 R6- R7 R8	(v	esting control tal work) irst base register	ole - current test base	
				138 * 139 * 140 *	R9 R10 R11	Se Tł	econd base register nird base register TTEST call return	er	
				141 * 142 * 143 *	R12 R13 R14	E7 (v	TESTS register work) ubroutine call		
				144 * 145 * 146 **	R15		econdary Subrouti	ne call or work	
00000200 00000200 00000200		00000200 00001200 00002200		148 149 150	Į Į	USI NG	BEGIN, R8 BEGIN+4096, R9 BEGIN+8192, R10	FIRST Base Register SECOND Base Register THIRD Base Register	
00000202	0580 0680 0680			152 BF 153 154	I	BALR BCTR BCTR	R8, 0	Initalize FIRST base register Initalize FIRST base register Initalize FIRST base register	
	4190 8800 4190 9800		00000800 00000800	156 157 158		LA LA	R9, 2048(, R8) R9, 2048(, R9)	Initalize SECOND base register Initalize SECOND base register	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000020E 00000212	41A0 9800 41A0 A800		00000800 00000800	159 160	LA LA		Initalize THIRD base register Initalize THIRD base register
00000216 0000021A	B600 8324 9604 8325		00000524 00000525	161 162 163	$\mathbf{0I}$	CTLR0+1, X' 04'	Store CRO to enable AFP Turn on AFP bit
0000021E 00000222	9602 8325 B700 8324		00000525 00000524	164 165 166		RO, RO, CTLRO	Turn on Vector bit Reload updated CRO
				169 * Is 7/A	rchi te	cture vector facil	ity installed (bit 129) scements facility 1 installed (bit 135)
				170 ****** 171	*****	*******	**************************************
00000226	47F0 80A8		000002A8	172+	B	X0001	v
				173+* 174+*			Fcheck data area skip messgae
0000022A	40404040 E2928997			175+SKT0001	DC	C' Skipping to	ests: '
0000023E 0000025C	A961C199 838889A3 404D8289 A340F1F2	0000004E	0000001	176+ 177+ 178+SKL0001	DC DC EQU	C'z/Architecture C' (bit 129) is r *-SKT0001	vector facility not installed.'
00000070	0000000 0000000			179+*			facility bits
00000278 00000280	00000000 00000000 0000000 00000000			180+ 181+FB0001	DS DS	FD 4FD	gap
000002A0	00000000 00000000			182+	DS	FD	gap
		000002A8	00000001	183+* 184+X0001	EQU	*	
000002A8 000002AC	4100 0004 B2B0 8080		00000004 00000280	185+ 186+	LA STFLE	RO, ((X0001-FB0001 FB0001)/8)-1 get facility bits
000002B0 000002B4 000002B8	B982 0000 4300 8090		00000290 0000052C	187+ 188+	XGR I C	RO, RO RO, FB0001+16	get fbit byte is bit set?
000002BC	5400 832C 4770 80D0		0000032C 000002D0	189+ 190+	N BNZ	R0, =F' 64' XC0001	is bit set:
				191+* 192+* facili 193+*	ty bit	not set, issue me	essage and exit
000002C0	4100 004E		0000004E	194+	LA	RO, SKL0001	message length
000002C4 000002C8	4110 802A 4520 8240		0000022A 00000440	195+ 196+	LA BAL	R1, SKT0001 R2, MSG	message address
000002CC	47F0 8308	00000000	00000508	197+	В	EOJ	
		000002D0	0000001	198+XC0001 199	EQU FCHEC	⊤ K 135.′z/Arch vect	cor enhance facility 1'
000002D0	47F0 8158		00000358	200+ 201+* 202+*	В	X0002	Fcheck data area skip messgae
000002D4 000002E8 00000308	40404040 E2928997 A961C199 838840A5 404D8289 A340F1F3			203+SKT0002 204+ 205+	DC DC DC	C' Skipping to C'z/Arch vector of C' (bit 135) is n	ests: ' enhance facility 1'
		00000050	00000001	206+SKL0002 207+*	EQU	*- SKT0002	facility bits
00000328 00000330	0000000 00000000 0000000 00000000			208+ 209+FB0002	DS DS	FD 4FD	gap
00000350	00000000 00000000	000000		210+ 211+*	DS	FD	gap
00000358 0000035C	4100 0004 B2B0 8130	00000358	00000001 00000004 00000330	212+X0002 213+ 214+	EQU LA STFLE	* R0, ((X0002-FB0002 FB0002	2)/8)-1 get facility bits

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LOC	OBJECT CODE	ADDR1	ADDR2	STM				
				255 ******* 256 * result	****** not a	as expected:	************	
				257 * 258 * 259 ******	*****	and instruction	est number, instruction under test n m4 **************	
000003BA	45F0 81DC	000003BA	00000001 000003DC	260 FAILMSG 261	EQU BAL	* R15, RPTERROR		
				264 * contir	iue aft	ter a failed tes		
000003BE	5800 8330	000003BE	00000001 00000530	265 ********* 266 FAILCONT 267		**************************************	**************************************	
000003C2	5000 8E00		00001000	268 269	ST	RO, FAILED		
000003C6 000003CA	41C0 C004 47F0 8184		00000004 00000384	270 271	LA B	R12, 4(0, R12) NEXTE7	next test address	
						************** ng; set ending	**************************************	
000003CE 000003D2	5810 8E00 1211	000003CE	00000001 00001000	276 ENDTEST 277 278	EQU L LTR	* R1, FAILED R1, R1	did a test fail?	
000003D4 000003D8	4780 8308 47F0 8320		00000508 00000520	279 280	BZ B	EOJ FAI LTEST	No, exit Yes, exit with BAD PSW	

				282	*****	*****	******	*********
				283	*	RPTER	ROR	Report instruction test in error
				284	*****	*****	*******	Report instruction test in error **********************************
000003DC	50F0 8224		00000424		RPTERROR		R15, RPTSAVE	Save return address
000003E0	5050 8228		00000428	287 288	*	ST	R5, RPTSVR5	Save R5
000003E4	4820 5004		00000004	289		LH	R2, TNUM	get test number and convert
000003E8 000003EC	4E20 8E67 D211 8E51 8E3B	00001051	00001067 0000103B	290 291		CVD MVC	R2, DECNUM PRT3, EDIT	
000003F2	DE11 8E51 8E67	00001051	00001067	292		ED	PRT3, DECNUM	
000003F8	D202 8E18 8E5E	00001018	0000105E	293 294		MVC	PRTNUM(3), PRT3+13	fill in message with test #
000003FE	D207 8E33 5008	00001033	00000008	295		MVC	PRTNAME, OPNAME	fill in message with instruction
				296 297		Ugo U	angulas Diagnasa fa	n Magaga ta consola
				298		use n	lercures bragnose rol	r Message to console
00000404	9002 8230		00000430	299		STM	RO, R2, RPTDWSAV	save regs used by MSG
00000408	4100 0033		00000033	300		LA	RO, PRTLNG	message length
0000040C	4110 8E08		00001008	301		LA	R1, PRTLINE	messagfe address
00000410	4520 8240		00000440	302		BAL	R2, MSG	call Hercules console MSG display
00000414	9802 8230		00000430	303		LM	RO, R2, RPTDWSAV	restore regs
00000410	roro 0000		00000400	207			Dr DDTCVDr	Dente and Dr
00000418	5850 8228		00000428	305		Ļ	R5, RPTSVR5	Restore R5
0000041C	58F0 8224		00000424	306		L	R15, RPTSAVE	Restore return address
00000420	07FF			307		BR	R15	Return to caller
00000424	0000000			309	RPTSAVE	DC	F' 0'	R15 save area
00000428	0000000			310	RPTSVR5	DC	F' 0'	R5 save area
00000430	00000000 00000000			312	RPTDWSAV	DC	2D' 0'	RO-R2 save area for MSG call

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OBJECT CODE

ADDR1

STM

ADDR2

LOC

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LOC	OBJECT CODE	ADDR1	ADDR2	STM			
				314 ******** 315 * 316 * 317 ******	Issue	HERCULES MESSAGE poin R2 = return address	**************************************
00000440 00000444	4900 8338 07D2		00000538	319 MSG 320	CH BNHR	RO, =H' O' R2	Do we even HAVE a message? No, ignore
00000446	9002 827C		0000047C	322	STM	RO, R2, MSGSAVE	Save registers
0000044A 0000044E 00000452	4900 833A 47D0 8256 4100 005F		0000053A 00000456 0000005F	324 325 326	CH BNH LA	RO, =AL2(L' MSGMSG) MSGOK RO, L' MSGMSG	Message length within limits? Yes, continue No, set to maximum
00000456 00000458 0000045A	1820 0620 4420 8288		00000488	328 MSGOK 329 330	LR BCTR EX	R2, R0 R2, 0 R2, MSGMVC	Copy length to work register Minus-1 for execute Copy message to O/P buffer
0000045E 00000462	4120 200A 4110 828E		0000000A 0000048E	332 333	LA LA	R2, 1+L' MSGCMD(, R2) R1, MSGCMD	Calculate true command length Point to true command
00000466 0000046A	83120008 4780 8276		00000476	335 336	DC BZ	X' 83', X' 12', X' 0008' MSGRET	Issue Hercules Diagnose X'008' Return if successful
0000046E 00000470	1222 4780 8276		00000476	337 338 339	LTR BZ	R2, R2 MSGRET	Is Diag8 Ry (R2) 0? an error occurred but coninue
00000474	0000			340 341	DC	Н' О'	CRASH for debugging purposes
00000476 0000047A	9802 827C 07F2		0000047C	343 MSGRET 344	LM BR	RO, R2, MSGSAVE R2	Restore registers Return to caller
0000047C 00000488	00000000 00000000 D200 8297 1000	00000497	00000000	346 MSGSAVE 347 MSGMVC	DC MVC	3F' 0' MSGMSG(0), 0(R1)	Registers save area Executed instruction
00000400	μωυυ σωσι 1000	00000437		J47 NDGNNC	IVIV C		EXECUTER THEFT ACTION
0000048E 00000497	D4E2C7D5 D6C8405C 40404040 40404040			349 MSGCMD 350 MSGMSG 351	DC DC	C' MSGNOH * ' CL95' '	*** HERCULES MESSAGE COMMAND *** The message text to be displayed

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT					

000004F8	00020001 80000000			357	E0JPSW	DC	OD' O' , X' 000200	0180000000', AD(0)	
00000508	B2B2 82F8		000004F8	359	E0J	LPSWE	E0JPSW	Normal completion	
00000510	00020001 80000000			361	FAILPSW	DC	0D' 0' . X' 000200	0180000000', AD(X'BAD')	
00000520			00000510		FAI LTEST			Abnormal termination	
00000020	<i>B</i> \$\text{\$\}\$}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}}		00000010	000	IMILILOI	LISTE	THE SW	AMINITALL CCLIM HACEON	
				366	******* * *****		**************************************	************	
				307		1. 4. 4. 4. 4. 4. 4. 4. 4. 4. 4. 4. 4. 4.			
	00000000				CTLRO	DS	F	CRO	
00000528	0000000			370		DS	F		
0000052C 0000052C	0000040			372 373		LTORG	, =F' 64'	Literals pool	
00000530	0000001			374			=F' 1'		
00000534 00000538	00001608 0000			375 376			=A(E7TESTS) =H' 0'		
	005F			377 378			=AL2(L' MSGMSG)		
				379 380	*	some (constants		
		00000400	0000001	381		EQU	1024	One KB	
		00001000 00010000 00100000	00000001 00000001 00000001	382 383 384		EQU EQU EQU	(4*K) (64*K) (K*K)	Size of one page 64 KB 1 MB	
		AABBCCDD 000000DD	0000001 00000001	385 386	REG2PATT REG2LOW	EQU	X' AABBCCDD' X' DD'	Polluted Register pattern (last byte above)	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				389 *====================================	
				390 * 391 * NOTE: start data on an address that is easy to display 392 * within Hercules	
				393 *	
				394 *====================================	:====
0000053C 00001000	0000000	0000053C	00001000	396 ORG ZVE7TST+X' 1000' 397 FAILED DC F'O' some test failed?	
00001004	00000000			398 TESTING DC F'O' current test number	
				400 *	
				401 * failed message and associated editting 402 *	
00001008	40404040 40404040			403 PRTLINE DC C' Test # '	
0000101B	A7A7A7 40868189 93858440			404 PRTNUM DC C'xxx' 405 DC c' failed for instruction '	
00001033	A7A7A7A7 A7A7A7A7	00000033	00000001	406 PRTNAME DC CL8' xxxxxxxx' 407 PRTLNG EQU *- PRTLINE	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				428 *	E7TEST DSECT	Γ	***************************	
00000000 00000004 00000006 00000007 000000010 00000014 00000018 0000001C 00000020 00000028 00000038	00000000 000 00 00 40404040 40404040 00000000			431 E7TEST 432 TSUB 433 TNUM 434 435 436 437 OPNAME 438 V2ADDR 439 V3ADDR 440 RELEN 441 READDR 442 443 V10UTPUT 444 445 446 * 447 *	DS FD	E7 name address of address of RESULT LEN	r not used v2 source v3 source GTH pected) address	
		00000000	0000163B	447 448 * 449 * 451 ZVE7TST	followed by EXPECT	TED RESULT		
000010A8				455 * Ma	cros to helm	build test tables	****************************	
				460 * 461 462	to generate i MACRO VRR_C &INST	individual test	- VRR-c instruction under	n toot
				463 . * 464 . * 465 466 467 &TNUM 468 469	GBLA &TNUM SETA &TNUM DS OFD	+1	no m fields	
				470 471 472 T&TNUM 473 474 475	USING *, R5 DC A(X&T) DC H' &TNO DC X' 00' DC HL1' 00	NUM) address UM test nu D' m field		ine
				476 477	DC CL8' &1 DC A(RE&1	INST' instruc FNUM+16) address	tion name of v2 source	

	OD IECT CODE	ADDD4	ADDDO	CTM			03 Apr 2025 15: 39: 31 Page
LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				478 479	DC DC	A(RE&TNUM+32) A(16)	address of v3 source result length
				480 REA&T		A(RE&TNUM)	result address
				481	DS NUM DC	FD	gap V1 output
				482 V10&T 483	DS DS	XL16 FD	gap
				484 . *			O I
				485 * 486 X&TNU	M DS	OF	
				487	LGF	R1, V2ADDR	load v2 source
				488 489	VL	v22, 0(R1)	use v22 to test decoder
				490	LGF	R1, V3ADDR	load v3 source
				491 492	VL	v23, 0(R1)	use v23 to test decoder
				493	&I NST	V22, V22, V23	test instruction (dest is a source)
				494	VST	V22, V10&TNUM	save v1 output
				495 496	BR	R11	return
				497	IIM DC	OE.	rel 10 compared and married
				498 RE&TN 499	UM DC	OF	xl16 expected result
				500 501	DROP MEND	R 5	
				503 * 504 * mac	ro to gen	erate table of p	ointers to individual tests
				504 * mac 505 * 506	ro to gen MACRO	_	ointers to individual tests
				504 * mac 505 * 506 507	MACRO PTTAB	LE	ointers to individual tests
				504 * mac 505 * 506 507 508	MACRO PTTAB GBLA	LE &TNUM	ointers to individual tests
				504 * mac 505 * 506 507 508 509 510 &CUR	MACRO PTTAB GBLA	LE &TNUM &CUR	ointers to individual tests
				504 * mac 505 * 506 507 508 509 510 &CUR 511 . *	MACRO PTTAB GBLA LCLA SETA	LE &TNUM &CUR 1	ointers to individual tests
				504 * mac 505 * 506 507 508 509 510 &CUR 511 . * 512 TTABL 513 . LOOP	MACRO PTTAB GBLA LCLA SETA	LE &TNUM &CUR	ointers to individual tests
				504 * mac 505 * 506 507 508 509 510 &CUR 511 . * 512 TTABL 513 . LOOP 514 . *	MACRO PTTAB GBLA LCLA SETA E DS	LE &TNUM &CUR 1	ointers to individual tests
				504 * mac 505 * 506 507 508 509 510 &CUR 511 . * 512 TTABL 513 . LOOP 514 . * 515 516 . *	MACRO PTTAB GBLA LCLA SETA E DS ANOP DC	LE &TNUM &CUR 1 OF	ointers to individual tests
				504 * mac 505 * 506 507 508 509 510 &CUR 511 . * 512 TTABL 513 . LOOP 514 . * 515 516 . * 517 &CUR 518	MACRO PTTAB GBLA LCLA SETA E DS ANOP	LE &TNUM &CUR 1 OF	
				504 * mac 505 * 506 507 508 509 510 &CUR 511 . * 512 TTABL 513 . LOOP 514 . * 515 516 . * 517 &CUR 518 519 *	MACRO PTTAB GBLA LCLA SETA E DS ANOP DC SETA AIF	LE &TNUM &CUR 1 OF A(T&CUR) &CUR+1 (&CUR LE &TNUM)	. LOOP
				504 * mac 505 * 506 507 508 509 510 &CUR 511 .* 512 TTABL 513 . LOOP 514 .* 515 516 .* 517 &CUR 518 519 * 520	MACRO PTTAB GBLA LCLA SETA E DS ANOP DC SETA AIF DC	LE &TNUM &CUR 1 OF A(T&CUR) &CUR+1 (&CUR LE &TNUM) A(O)	
				504 * mac 505 * 506 507 508 509 510 &CUR 511 . * 512 TTABL 513 . LOOP 514 . * 515 516 . * 517 &CUR 518 519 * 520 521 522 . *	MACRO PTTAB GBLA LCLA SETA E DS ANOP DC SETA AIF DC DC	LE &TNUM &CUR 1 OF A(T&CUR) &CUR+1 (&CUR LE &TNUM)	. LOOP
				504 * mac 505 * 506 507 508 509 510 &CUR 511 .* 512 TTABL 513 . LOOP 514 .* 515 516 .* 517 &CUR 518 519 * 520 521	MACRO PTTAB GBLA LCLA SETA E DS ANOP DC SETA AIF DC	LE &TNUM &CUR 1 OF A(T&CUR) &CUR+1 (&CUR LE &TNUM) A(O)	. LOOP

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				526 ******	*****	*******	**********
				527 *	E7 VR	R-c tests	**********
				528 ******* 529	PRINT		• ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~
				530 *			
					5 VBPER	M - Vector Bit Per	rmute
				532 * 533 *	VRR- c	instruction	
				534 *	, 1010	followed by	
				535 * 536 *		16 byte expect	ted result (V1)
				537 *		16 byte V2 sou 16 byte V3 sou	irce
				538 *			
				539 * VBPE	RM - Ve	ctor Bit Permute	
				541			
				542		VBPERM	
00010A8 00010A8		000010A8		543+ 544+	DS USING	OFD * R5	base for test data and test routine
0010A8	000010E8	00001040		545+T1	DC	A(X1)	address of test routine
0010AC	0001			546+	DC	H' 1'	test number
0010AE 0010AF	00 00			547+ 548+	DC DC	X' 00' HL1' 00'	m field
0010B0	E5C2D7C5 D9D44040			549 +	DC	CL8' VBPERM	instruction name
0010B8	00001120			550+	DC	A(RE1+16)	address of v2 source
0010BC 0010C0	00001130 00000010			551+ 552+	DC DC	A(RE1+32) A(16)	address of v3 source result length
0010C4	00001110			553+REA1	DC	A(RE1)	result address
0010C8 0010D0	00000000 00000000 0000000 00000000			554+ 555+V101	DS DS	FD XL16	gap V1 output
0010D0	0000000 0000000			333+1101	ъз	ALIU	VI Output
0010E0	00000000 00000000			556+	DS	FD	gap
0010E8				557+* 558+X1	DS	0F	
0010E8	E310 5010 0014		0000010	559+	LGF	R1, V2ADDR	load v2 source
0010EE	E761 0000 0806		00000000	560+	VL	v22, 0(R1)	use v22 to test decoder
00010F4 00010FA	E310 5014 0014 E771 0000 0806		00000014 00000000	561+ 562+	LGF VL	R1, V3ADDR v23, O(R1)	load v3 source use v23 to test decoder
0001100	E766 7000 0E85			563 +	VBPER	M V22, V22, V23	test instruction (dest is a source)
001106 00110C	E760 5028 080E 07FB		000010D0	564+ 565+	VST BR	V22, V101 R11	save v1 output return
001110	U/FB			566+RE1	DC	OF	xl 16 expected result
001110				567+	DROP	R 5	•
001110	00000000 00000000 0000000 00000000			568	DC	XL16' 0000000000000	00000 00000000000000000000' result
001110	0000000 0000000			569	DC	XL16' 000000000000	00000 00000000000000000000000000000000
001128	0000000 00000000					VI 101 0000000000000	0000 0000000000000000000000000000000000
001130 001138	00000000 00000000 0000000 00000000			570	DC	XL16, 0000000000000	00000 0000000000000000000' v3
001100				571			
001140				572 572		VBPERM	
001140 001140		00001140		573+ 574+	DS USING	OFD *. R5	base for test data and test routine
001140	00001180	00001110		575+T2	DC	A(X2)	address of test routine
001144	0002			576+	DC	H' 2'	test number
001146	00			577+	DC	X' 00'	

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LOC	OBJECT CODE	ADDR1	ADDR2	STM			
00001147	00			578+	DC	HL1' 00'	m field
00001148	E5C2D7C5 D9D44040			579 +		CL8' VBPERM	instruction name
00001150	000011B8			580+		A(RE2+16)	address of v2 source
00001154	00001128			581+		A(RE2+32)	address of v3 source
0001154	00000010			582+	DC	A(16)	result length
00001138 0000115C	0000010 000011A8			583+REA2		A(RE2)	result address
0001130	0000000 00000000			584+	DS	FD	
0001160	0000000 0000000			585+V102	DS DS	XL16	gap V1 output
				J0J+1102	DЗ	ALIU	vi output
00001170	00000000 00000000			586 +	DS	FD	dan
00001178	00000000 00000000			587+*	DЗ	ΓU	gap
00001100					DC	OF	
00001180	E010 7010 0014		0000010	588+X2		OF	1 - 1 - 0
0001180	E310 5010 0014		00000010	589 +		R1, V2ADDR	load v2 source
0001186	E761 0000 0806		00000000	590+		v22, 0(R1)	use v22 to test decoder
0000118C	E310 5014 0014		00000014	591 +		R1, V3ADDR	load v3 source
00001192	E771 0000 0806		00000000	592 +	VL	v23, 0(R1)	use v23 to test decoder
00001198	E766 7000 0E85		00001100	593+		1 V22, V22, V23	test instruction (dest is a source)
000119E	E760 5028 080E		00001168	594+	VST	V22, V102	save v1 output
00011A4	07FB			595+		R11	return
00011A8				596+RE2	DC	0F	xl16 expected result
00011A8				597 +		R5	
00011A8	00000000 00000000			598	DC	XL16' 0000000000000	00000 00000000000000000' result
00011B0	0000000 00000000						
00011B8	FFFFFFFF FFFFFFF			599	DC	XL16' FFFFFFFFFF	FFFFF FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
00011C0	FFFFFFF FFFFFFF						
00011C8	FFFFFFFF FFFFFFF			600	DC	XL16' FFFFFFFFFFF	FFFFF FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
000011D0	FFFFFFFF FFFFFFFF			601 602	VRR C	VBPERM	
000011D8				603+		OFD	
000011D8		000011D8		604+	USING		base for test data and test routine
000011D8	00001218	00001120		605+T3		A(X3)	address of test routine
00011DC	0003			606+	DC	H' 3'	test number
00011DE	00			607+		X' 00'	cese number
00011DE	00			608+		HL1' 00'	m field
00011E0	E5C2D7C5 D9D44040			609+		CL8' VBPERM	instruction name
00011E0	00001250			610+		A(RE3+16)	address of v2 source
00011E8	00001230			611+		A(RE3+10) A(RE3+32)	address of v2 source
00011EC	00001200			612+	DC	A(16)	result length
00011F0	000010			613+REA3		A(RE3)	result address
00011F4	00001240			614+	DS DS	FD	
0001118				615+V103		XL16	gap V1 output
0001200	00000000 00000000			019+4109	אמ	VEIO	V1 output
0001208	00000000 00000000			616+	DS	ED	dan
0001210	00000000 00000000			617+*	אס	FD	gap
10001919					DC	OF	
	F210 5010 0014		00000010	618+X3		OF	land v9 gaunes
			00000010	619+		R1, V2ADDR	load v2 source
0001218	E310 5010 0014		00000000	620+		v22, 0(R1)	use v22 to test decoder
00001218 00001218 0000121E	E761 0000 0806		00000014		LGF	R1, V3ADDR	load v3 source
00001218 0000121E 00001224	E761 0000 0806 E310 5014 0014		00000014	621+		00 (\(\(\text{INT} \)	was voo to took deed deed
00001218 0000121E 00001224 0000122A	E761 0000 0806 E310 5014 0014 E771 0000 0806		00000014 00000000	622+	VL	v23, 0(R1)	use v23 to test decoder
0001218 0000121E 00001224 0000122A 00001230	E761 0000 0806 E310 5014 0014 E771 0000 0806 E766 7000 0E85		0000000	622+ 623+	VL VBPERN	1 V22, V22, V23	test instruction (dest is a source)
00001218 0000121E 00001224 0000122A 00001230 00001236	E761 0000 0806 E310 5014 0014 E771 0000 0806 E766 7000 0E85 E760 9000 080E			622+ 623+ 624+	VL VBPERN VST	1 V22, V22, V23 V22, V103	test instruction (dest is a source) save v1 output
00001218 0000121E 00001224 0000122A 00001230 00001236	E761 0000 0806 E310 5014 0014 E771 0000 0806 E766 7000 0E85		0000000	622+ 623+ 624+ 625+	VL VBPERN VST BR	M V22, V22, V23 V22, V103 R11	test instruction (dest is a source) save v1 output return
00001218 0000121E 00001224 0000122A 00001230 00001236 0000123C	E761 0000 0806 E310 5014 0014 E771 0000 0806 E766 7000 0E85 E760 9000 080E		0000000	622+ 623+ 624+ 625+ 626+RE3	VL VBPERN VST BR DC	1 V22, V22, V23 V22, V103 R11 OF	test instruction (dest is a source) save v1 output
0001218 0000121E 00001224 0000122A 00001230 00001236	E761 0000 0806 E310 5014 0014 E771 0000 0806 E766 7000 0E85 E760 9000 080E		0000000	622+ 623+ 624+ 625+	VL VBPERN VST BR DC DROP	1 V22, V22, V23 V22, V103 R11 OF R5	test instruction (dest is a source) save v1 output return

LOC	le.
00001250 FFFFFFF 629 DC XL16' FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	le.
00001260 0000000 00000000 630	l e
Control Cont	l e
00001270 00001270 634+ USING *, R5 base for test data and test routing address of test routine address of test routine test number 00001274 0004 636+ DC H' 4' test number 00001276 00 637+ DC X' 00' m field 00001277 00 638+ DC HL1' 00' m field 00001280 00001288 640+ DC A(RE4+16) address of v2 source 00001284 00001288 641+ DC A(RE4+32) address of v3 source 0000128C 000012B 642+ DC A(16) result length 00001290 00000000 644+ DS FD gap 00001298 00000000 645+V104 DS XL16 V1 output	ne
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	
0000128C 000012D8 643+REA4 DC A(RE4) result address 00001290 00000000 00000000 644+ DS FD gap 00001298 00000000 00000000 645+V104 DS XL16 V1 output	
00001298	
000012A0 00000000 00000000 000012A8 00000000 00000000 646+ DS FD gap	
647+* 000012B0	
000012B0 E310 5010 0014 00000010 649+ LGF R1, V2ADDR load v2 source 000012B6 E761 0000 0806 00000000 650+ VL v22, 0(R1) use v22 to test decoder 000012BC E310 5014 0014 00000014 651+ LGF R1, V3ADDR load v3 source	
000012C2 E771 0000 0806 00000000 652+ VL v23, 0(R1) use v23 to test decoder 000012C8 E766 7000 0E85 653+ VBPERM V22, V22, V23 test instruction (dest is a source 000012CE E760 5028 080E 00001298 654+ VST V22, V104 save v1 output	.)
000012D4 07FB 655+ BR R11 return 000012D8 656+RE4 DC 0F xl16 expected result	
000012D8 00000000 000000000 658 DC XL16'000000000000000000000000000000000000	
000012E8 00010203 04050607 659 DC XL16' 0001020304050607 08090A0B0C0D0E0F' v2 000012F0 08090A0B 0C0D0E0F 0C XL16' FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	
00001300 FFFFFFF FFFFFFF	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	e
0000130E 00 667+ DC X' 00' 0000130F 00 668+ DC HL1' 00' m field 00001310 E5C2D7C5 D9D44040 669+ DC CL8' VBPERM instruction name	
00001318 00001380 670+ DC A(RE5+16) address of v2 source 0000131C 00001390 671+ DC A(RE5+32) address of v3 source 00001320 00000010 672+ DC A(16) result length	
00001324 00001370 673+REA5 DC A(RE5) result address 00001328 00000000 00000000 674+ DS FD gap 00001330 00000000 00000000 675+V105 DS XL16 V1 output	
00001338	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI						
				677+*						
00001348				678+X5	DS	0F				
00001348	E310 5010 0014		00000010	679+	LGF	R1, V2ADDR	load v2 source			
0000134E	E761 0000 0806		00000000	680 +	VL	v22, 0(R1)	use v22 to test decoder			
00001354	E310 5014 0014		00000014	681 +	LGF	R1, V3ADDR	load v3 source			
0000135A	E771 0000 0806		00000000	682 +	VL	v23, 0(R1) M V22, V22, V23	use v23 to test decoder			
00001360	E766 7000 0E85			683 +	VBPER	M V22, V22, V23	test instruction (dest	is a source	e)	
00001366	E760 5028 080E		00001330	684+	VST	V22, V105	save v1 output			
0000136C	07FB			685+	BR	R11	return			
00001370				686+RE5	DC DDOD	OF	xl16 expected result			
00001370 00001370	0000000 000000FF			687+ 688	DROP DC	R5	00FF 0000000000000000'	nogul +		
00001370	0000000 0000000000000000000000000000000			000	DC	XL10 000000000000	OUFF OUUUUUUUUUUUUUUU	resul t		
00001378	FFFFFFF FFFFFFF			689	DC	YI 16' FFFFFFFFFFF	FFFF FFFFFFFFFFFFF	$\mathbf{v2}$		
00001388	FFFFFFF FFFFFFF			000	ЪС	XLIO IIIIIIIIIIII		₩~		
00001390				690	DC	XI.16' FOEODOCOBOAO	9080 7060504030201000'	v3		
00001398	70605040 30201000			000	20	1210 1020202010	700001000201000	••		
00001000				691						
				692		VBPERM				
000013A0				693+	DS	OFD				
000013A0		000013A0		694 +	USING		base for test data and	test routi	ne	
000013A0	000013E0			695+T6	DC	A(X6)	address of test routine			
000013A4	0006			696+	DC	H' 6'	test number			
000013A6	00			697+	DC	X' 00'	C: 11			
000013A7	00 E5C9D7C5 D0D44040			698+	DC	HL1' 00'	m field			
000013A8 000013B0	E5C2D7C5 D9D44040			699+ 700+	DC	CL8' VBPERM	instruction name			
000013B0 000013B4	00001418 00001428			700+ 701+	DC DC	A(RE6+16) A(RE6+32)	address of v2 source address of v3 source			
000013B4 000013B8	00001428			701+ 702+	DC DC	A(16)	result length			
000013BC	000010			702+ 703+REA6	DC	A(RE6)	result address			
000013C0	00000000 00000000			704+	DS	FD				
000013C8	00000000 00000000			705+V106	DS	XL16	gap V1 output			
000013D0	00000000 00000000						,			
000013D8	0000000 00000000			706 +	DS	FD	gap			
				707+*			<u> </u>			
000013E0				708+X6	DS	0F				
000013E0	E310 5010 0014		00000010	709 +	LGF	R1, V2ADDR	load v2 source			
000013E6	E761 0000 0806		00000000	710+	VL	v22, 0(R1)	use v22 to test decoder			
000013EC 000013F2	E310 5014 0014 E771 0000 0806		$00000014 \\ 00000000$	711+ 712+	LGF VL	R1, V3ADDR	load v3 source use v23 to test decoder			
000013F2 000013F8	E771 0000 0806 E766 7000 0E85		0000000	712+ 713+	V L VRDEDI	v23, 0(R1) M V22, V22, V23	test instruction (dest	is a source	ω)	
000013F8 000013FE	E760 7000 0E85 E760 5028 080E		000013C8	714+	VBFERI	V22, V106	save v1 output	is a soult	ر ر ا	
00001312	07FB		30001000	715+	BR	R11	return			
00001101	- , 			716+RE6	DC	0F	xl16 expected result			
00001408				717+	DROP	R5	r			
00001408	0000000 000000FF			718	DC	XL16' 000000000000	00FF 0000000000000000'	resul t		
00001410	0000000 00000000									
00001418	FFFFFF00 FFFFFF00			719	DC	XL16' FFFFFF00FFFF	FF00 FFFFFF00FFFFFFFF'	v2		
00001420				700	DC	VI 101 EOEODOGODO 40	0000 70007040000040004	0		
00001428				720	DC	YF10, LOFODOCOROYO	9080 7060504030201000'	v3		
00001430	70605040 30201000			721						
				721 722	VPR C	VBPERM				
00001438				723+	DS	OFD				
00001438		00001438		724+	USING		base for test data and	test routi	ne	
00001438	00001478			725+T7	DC	A(X7)	address of test routine			
						•				

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LOC	OBJECT CODE	ADDR1	ADDR2	STMF			
0000143C	0007			726+	DC	H' 7'	test number
0000143E	00			727+	DC	X' 00'	
0000143F	00			728 +	DC	HL1' 00'	m field
00001440	E5C2D7C5 D9D44040			729 +	DC	CL8' VBPERM	instruction name
00001448	000014B0			730+	DC	A(RE7+16)	address of v2 source
0000144C	000014C0			731+	DC	A(RE7+32)	address of v3 source
00001450	0000010			732+	DC	A(16)	result length
00001454	000014A0			733+REA7	DC	A(RE7)	result address
00001458	$00000000 \ 00000000$			734+	DS	FD	gap V1 output
00001460	00000000 00000000			735+V107	DS	XL16	VI output
00001468	00000000 00000000			700.	DC.	ED	
00001470	00000000 00000000			736+ 737+*	DS	FD	gap
00001479				737+** 738+X7	DC	OE	
00001478 00001478	E310 5010 0014		00000010	730+A7 739+	DS LGF	OF R1, V2ADDR	load v2 source
00001478 0000147E	E761 0000 0806		00000010	739+ 740+	VL	v22, O(R1)	use v22 to test decoder
0000147E	E310 5014 0014		0000000	740+ 741+	LGF	R1, V3ADDR	load v3 source
0000148A	E771 0000 0806		00000014	742+	VL	v23, 0(R1)	use v23 to test decoder
00001490	E766 7000 0E85		5555550	743+	VBPER	M V22, V22, V23	test instruction (dest is a source)
00001496	E760 5028 080E		00001460	744+	VST	V22, V107	save v1 output
0000149C	07FB			745+	BR	R11	return
000014A0				746+RE7	DC	OF	xl16 expected result
000014A0				747 +	DROP	R5	1
000014A0	0000000 00000980			748	DC	XL16' 000000000000	0980 0000000000000000' result
000014A8	0000000 00000000						
000014B0	11223344 55667788			749	DC	XL16' 112233445566	7788 99AABBCCDDEEFF00' v2
000014B8	99AABBCC DDEEFF00						
000014C0	020F1F20 31415161			750	DC	XL16' 020F1F203141	5161 718191A1B0B1B2B3' v3
000014C8	718191A1 B0B1B2B3			751			
				751 752	VDD C	VBPERM	
000014D0				752 753+	DS	OFD	
000014D0		000014D0		75 4 +	USING		base for test data and test routine
000011D0	00001510	00001120		755+T8	DC	A(X8)	address of test routine
000014D4	0008			756 +	DC	H' 8'	test number
000014D6				757+	DC	X' 00'	
000014D7	00			758 +	DC	HL1' 00'	m field
000014D8				759 +	DC	CL8' VBPERM	instruction name
000014E0				760+	DC	A(RE8+16)	address of v2 source
000014E4	00001558			761 +	DC	A(RE8+32)	address of v3 source
000014E8				762+	DC	A(16)	result length
000014EC				763+REA8	DC	A(RE8)	result address
000014F0				764+ 765 - V109	DS	FD VI 16	gap V1 output
000014F8 00001500				765+V108	DS	XL16	vi output
00001500				766 +	DS	FD	nan .
00001300				767+*	טע	1 <i>U</i>	gap
00001510				768+X8	DS	0F	
00001510	E310 5010 0014		00000010	769+	LGF	R1, V2ADDR	load v2 source
00001516			00000000	770+	VL	v22, 0(R1)	use v22 to test decoder
0000151C			00000014	771+	LGF	R1, V3ADDR	load v3 source
00001522	E771 0000 0806		00000000	772+	VL	v23, 0(R1)	use v23 to test decoder
00001528				773+		M V22, V22, V23	test instruction (dest is a source)
	E760 5028 080E		000014F8	774+	VST	V22, V108	save v1 output
00001534	07FB			775+	BR	R11	return
00001538				776+RE8	DC	0F	xl16 expected result

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI						
00001538 00001538	0000000 0000FF00			777+ 778	DROP DC	R5 XL16' 000000000000	F00 0000000000000000000'	result		
$00001540 \\ 00001548 \\ 00001550$	00000000 00000000 FFFFFFF FFFFFFF FFFFFFFF			779	DC	XL16' FFFFFFFFFFFF	FFF FFFFFFFFFFFFF	v2		
00001558 00001560	70605040 30201000 F0E0D0C0 B0A09080			780	DC	XL16' 7060504030201	000 F0E0D0C0B0A09080'	v3		
00001568 00001568 0000156C	000015A8 0009	00001568		781 782 783+ 784+ 785+T9 786+	DS USING DC DC	A(X9) H' 9'	base for test data and address of test routine test number		ıe	
0000156E 0000156F 00001570 00001578 0000157C 00001580 00001584	00 00 E5C2D7C5 D9D44040 000015E0 000015F0 00000010 000015D0			787+ 788+ 789+ 790+ 791+ 792+ 793+REA9	DC DC DC DC DC DC DC	CL8' VBPERM A(RE9+16) A(RE9+32) A(16)	m field instruction name address of v2 source address of v3 source result length result address			
00001588 00001590 00001598	00000000 00000000 0000000 00000000 000000			794+ 795+V109	DS DS	FD XL16	gap V1 output			
000015A0 000015A8	00000000 00000000			796+ 797+* 798+X9	DS	OF	gap			
000015A8 000015AE 000015B4	E310 5010 0014 E761 0000 0806 E310 5014 0014		00000010 00000000 0000014	799+ 800+ 801+	VL LGF	v22, 0(R1) R1, V3ADDR	load v2 source use v22 to test decoder load v3 source			
000015BA 000015C0 000015C6	E771 0000 0806 E766 7000 0E85 E760 5028 080E		00000000 00001590	802+ 803+ 804+	VL VBPERN VST	, , ,	use v23 to test decoder test instruction (dest save v1 output		e)	
000015CC 000015D0 000015D0	07FB			805+ 806+RE9 807+	BR DC DROP		return xl16 expected result			
000015D0 000015D8 000015E0	0000000 0000DB66 0000000 0000000 FFFFFFF FFFFFFF			808 809	DC DC		B66 0000000000000000' FFF FFFFFFFFFFFFFFFF	result v2		
000015E8 000015F0 000015F8	FFFFFFFF FFFFFFFF 0101FF02 02FF0304 FF0506FF FF0706FF			810			304 FF0506FFFF0706FF'	v3		
00001600 00001604	00000000 0000000			811 812 813	DC DC	F'O' END OF TA	BLE			
				816 *	-	nters to individual	load test			
00001608 00001608				817 E7TESTS 818 819+TTABLE	DS PTTABI DS	OF LE OF				
00001608 0000160C 00001610	000010A8 00001140 000011D8			820+ 821+ 822+	DC DC DC	A(T1) A(T2) A(T3)				
00001614 00001618	00001270 00001308 000013A0			823+ 824+ 825+	DC DC DC	A(T4) A(T5) A(T6)				

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI				
	00001438			826+	DC DC	A(T7)		
00001624 00001628	000014D0 00001568			827+ 828+	DC DC	A(T8) A(T9)		
0000162C	0000000			829+* 830+	DC	A(0)	END OF TABLE	
	00000000			831+ 832	DC	A(O)		
00001634 00001638	00000000 0000000			833 834	DC DC	F' 0' F' 0'	END OF TABLE	
00001030	0000000			004	ЪС	r		

BJECT CODE	00000017 00000018 00000019 0000001A 0000001B 0000001C 0000001D	00000001 00000001 00000001 00000001 000000	883 V22 884 V23 885 V24 886 V25 887 V26 888 V27 889 V28 890 V29 891 V30 892 V31 893 894	EQU EQU EQU EQU EQU EQU EQU EQU	22 23 24 25 26 27 28 29 30 31			
	00000017 00000018 00000019 0000001A 0000001B 0000001C 0000001D	00000001 00000001 00000001 00000001 000000	884 V23 885 V24 886 V25 887 V26 888 V27 889 V28 890 V29 891 V30 892 V31 893	EQU	22 23 24 25 26 27 28 29 30 31			
	00000017 00000018 00000019 0000001A 0000001B 0000001C 0000001D	00000001 00000001 00000001 00000001 000000	884 V23 885 V24 886 V25 887 V26 888 V27 889 V28 890 V29 891 V30 892 V31 893	EQU	23 24 25 26 27 28 29 30 31			
	00000019 0000001A 0000001B 0000001C 0000001D	00000001 00000001 00000001 00000001 000000	886 V25 887 V26 888 V27 889 V28 890 V29 891 V30 892 V31 893	EQU	24 25 26 27 28 29 30 31			
	000001A 000001B 0000001C 0000001D 0000001E	00000001 00000001 00000001 00000001	887 V26 888 V27 889 V28 890 V29 891 V30 892 V31 893	EQU	26 27 28 29 30 31			
	0000001C 0000001D 0000001E	00000001 00000001 00000001	889 V28 890 V29 891 V30 892 V31 893	EQU	27 28 29 30 31			
	0000001D 0000001E	00000001 00000001	890 V29 891 V30 892 V31 893	EQU	29 30 31			
	000001E 000001F	0000001	892 V31 893	EQU	30 31			
			893					
			894	END				

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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFE	RENCE	S													
BEGI N	I	00000200	2	152	118	148	149	150												
CTLRO	F	00000200	4	369	162	163	164	165												
DECNUM	r C	00000324	16	417	290	292	104	103												
E7TEST	4					292														
	4 E	0000000	64	431	239															
E7TESTS	F	00001608	4	817	232															
EDIT	X	0000103B	18	412	291															
ENDTEST	Ū	000003CE	I .	276	237	005	070													
EOJ	Ţ	00000508	4	359	197	225	279													
EOJPSW	D	000004F8	8	357	359															
FAILCONT	U	000003BE	1	266																
FAILED	F	00001000	4	397	268	277														
FAILMSG	U	000003BA	1	260	250															
FAILPSW	D	00000510	8	361	363															
FAILTEST	Ι	00000520	4	363	280															
FB0001	F	00000280	8	181	185	186	188													
FB0002	F	00000330	8	209	213	214	216													
I MAGE	1	00000000	5692	0																
K	U	00000400	1	381	382	383	384													
K64	U	00010000	1	383																
B	Ū	00100000	<u>1</u>	384																
MSG	Ĭ	00000440	4	319	196	224	302													
ASGCMD	Ĉ	0000048E	9	349	332	333	002													
MSGMSG	č	00000497	95	350	326	347	324													
ASGMVC	Ī	00000437	6	347	330	J47	JAT													
ASGOK	Ť	00000456	9	328	325															
ASGRET	Ť	00000436	<u>د</u> ۸	343	336	339														
WSGSAVE	E E	00000476 0000047C	4	346	322	343														
VEXTE7	r II	00000476	4	234																
	U C		1		253	271														
OPNAME DAGE	U	00000008	8	437	295															
PAGE	U	00001000	1	382	001	000	000													
PRT3	C	00001051	18	415	291	292	293													
PRTLINE	C	00001008	16	403	407	301														
PRTLNG	U	00000033	1	407	300															
PRTNAME	C	00001033	8	406	295															
PRTNUM	C	00001018	3	404	293															
RO	U	0000000	1	840	112	162	165	185	187	188	189	194	213	215	216	217	222	241	242	
					267	268	299	300	303	319	322	324	326	328	343					
R1	U	0000001	1	841	195	223	248	249	277	278	301	333	347	559	560	561	562	589	590	
					591	592	619	620	621	622	649	650	651	652	679	680	681	682	709	
					710	711	712	739	740	741	742	769	770	771	772	799	800	801	802	
R10	U	000000A	1	850	150	159	160													
R11	U	000000B	1	851	245	246	565	595	625	655	685	715	745	775	805					
R12	Ü	000000C	1	852	232	235	252	270												
R13	Ü	000000D	1	853																
R14	Ü	000000E	1	854																
R15	Ŭ	000000F	1	855	261	286	306	307												
22	Ŭ	00000002	ī	842	196	224	289	290	299	302	303	320	322	328	329	330	332	338	343	
-~	J	3000000		U-IW	344	~~1	200	~00	200	302	500	<i>5</i> ≈0	~~~	JAU	G N U	550	302	550	0-10	
23	U	0000003	1	843	344															
R4	Ü	00000003	1	844																
			1		995	996	990	907	205	511	507	574	507	604	607	694	657	GG A	607	
R 5	U	0000005	1	845	235	236	239	287	305	544 777	567 784	574	597	604	627	634	657	664	687	
ne .	T T	0000000	4	040	694	717	724	747	754	777	784	807								
26	U	00000006	1	846																
R7	U	0000007	1	847	1.40	150	150	1 - 4	150											
R8	U	00000008	1	848	148	152	153	154	156											
R9	U	00000009	1	849	149	156	157	159												

ASMA Ver. 0.7.0	zvector	- e7- 18- VBPE	RM						03 Apr	2025	15: 39: 31	Page	25
SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFE	RENCE	S						
RE1	F	00001110	4	566	550	551	553						
RE2	F	000011A8	4	596	580	581	583						
RE3	F	00001240	4	626	610	611	613						
RE4	F	000012D8	4	656	640	641	643						
RE5	F	00001370	4	686	670	671	673						
RE6	<u>F</u>	00001408	4	716	700	701	703						
RE7	F	000014A0	4	746	730	731	733						
RE8	F	00001538	4	776	760	761	763						
RE9	F	000015D0	4	806	790	791	793						
REA1	A	000010C4	4	553 583									
REA2 REA3	A	0000115C 000011F4	4 4	613									
REA4	A A	00001114 0000128C	4	643									
REA5	Ä	000012324	4	673									
REA6	A	00001321 000013BC	4	703									
REA7	Ä	00001454	$\overline{4}$	733									
REA8	Ä	000014EC	$\overline{4}$	763									
REA9	A	00001584	4	793									
READDR	A	000001C	4	441	248								
REG2LOW	U	00000DD	1	387									
REG2PATT	U	AABBCCDD	1	386									
RELEN	A	00000018	4	440									
RPTDWSAV	D	00000430	8	312	299	303							
RPTERROR	I F	000003DC	4	286	261	200							
RPTSAVE RPTSVR5	F F	$00000424 \\ 00000428$	4	309	286	306 305							
SKL0001	T U	00000428 0000004E	4	310 178	287 194	303							
SKL0001 SKL0002	Ŭ	0000004E 00000050	1	206	222								
SKT0001	č	0000030 0000022A	20	175	178	195							
SKT0002	č	000002D4	20	203	206	223							
SVOLDPSW	Ü	00000140	0	114	~~~	~~0							
T1	Ā	000010A8	4	545	820								
T2	A	00001140	4	575	821								
T3	A	000011D8	4	605	822								
T4	A	00001270	4	635	823								
T5	A	00001308	4	665	824								
T6	A	000013A0	4	695	825								
T7	A	00001438	4	725	826								
T8	A	000014D0	4	755 785	827								
T9 TESTING	A F	00001568 00001004	4	785 398	828 242								
TNUM	r H	00001004	4 2	433	242	289							
TSUB	A	00000004	4	433 432	245	203							
TTABLE	A F	00001608	4	819	₩ŦJ								
VO	Ū	00001000	1	861									
V1	Ŭ	00000001	1	862	244								
V10	Ŭ	000000A	$\bar{1}$	871	-								
V11	Ū	000000B	1	872									
V12	U	000000C	1	873									
V13	U	000000D	1	874									
V14	Ü	000000E	1	875									
V15	U	000000F	1	876									
V16	U	00000010	1	877									
V17	U	00000011	l 1	878									
V18	U	00000012	1	879									
V19	U	00000013	1	880									

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFE	RENCE	S													
SINDOL	1111	VALUE	LLMIII	DLIM	KLIL	ILLITOL														
1 FUDGE	X	00001088	16	424	244															
101	X	000010D0	16	555	564															
102	X	00001168	16	585	594															
103	X	00001200	16	615	624															
104	X	00001298	16	645	654															
105	X	00001330	16	675	684															
106	X	000013C8	16	705	714															
107	X	00001460	16	735	744															
108	X	000014F8	16	765	774															
109	X	00001590	16	795	804															
10UTPUT	X	00000028	16	443	249															
2	U	00000002	1	863																
20	U	00000014 00000015	1	881 882																
21 22	U U	00000015	1	883	560	562	5 G A	500	502	504	690	623	624	GEO	653	GE A	680	683	684	
Z.L	U	00000010	1	003	560 710	563 713	564 714	590 740	593 743	594 744	620 770	023 773	774	650 800	803	654 804	VOV	003	004	
23	U	0000017	1	884	562	563	592	593	622	623	652	653	682	683	712	713	742	743	772	
ະປ	U	0000017	1	004	773	802	803	333	022	023	UJL	033	002	003	112	713	142	743	112	
24	U	0000018	1	885	113	002	003													
25	Ü	00000013	1	886																
26	Ü	00000013 0000001A	1	887																
~0 27	Ü	0000001R 0000001B	1	888																
28	Ŭ	0000001B	1	889																
29	Ü	0000001D	1	890																
2ADDR	Ä	00000010	$\overline{4}$	438	559	589	619	649	679	709	739	769	799							
3	Ü	00000003	ī	864		000	010	0.10	0.0											
30	Ü	0000001E	1	891																
31	Ū	000001F	1	892																
3ADDR	A	0000014	4	439	561	591	621	651	681	711	741	771	801							
4	U	0000004	1	865																
5	U	00000005	1	866																
6	U	0000006	1	867																
7	U	0000007	1	868																
8	U	8000000	1	869																
9	U	0000009	1	870																
0001	U	000002A8	1	184	172	185														
0002	U	00000358	1	212	200	213														
1	F	000010E8	4	558	545															
2	F	00001180	4	588	575															
3	<u>F</u>	00001218	4	618	605															
4	F	000012B0	4	648	635															
5	F	00001348	4	678	665															
6	F	000013E0	4	708	695															
7	F	00001478	4	738	725															
8	F	00001510	4	768	755															
9	r T	000015A8	4	798	785															
C0001	U	000002D0	I 1	198	190															
C0002	U	00000380	1 5000	226	218	110	100	104	200	110										
VE7TST	J	0000000	5692	111	114	116	120	124	396	112										
A(E7TESTS)	A	00000534	4	375	232															
AL2(L'MSGMSG)	R	0000053A	2	377	324 217	967														
F' 1' F' 64'	F	00000530	4	374	217	267														
г 04	F	0000052C 00000538	4 2	373 376	189 319															



