```
   LOC         OBJECT CODE      ADDR1     ADDR2     STMT

                                                       2 ****************************************************************************
                                                       3 *
                                                       4 *    Zvector E7 instruction tests for VRR-c encoded:
                                                       5 *
                                                       6 *    E7A1 VMLH   - Vector Multiply Logical High
                                                       7 *    E7A2 VML    - Vector Multiply Low
                                                       8 *    E7A3 VMH    - Vector Multiply High
                                                       9 *    E7A4 VMLE   - Vector Multiply Logical Even
                                                      10 *    E7A5 VMLO   - Vector Multiply Logical Odd
                                                      11 *    E7A6 VME    - Vector Multiply Even
                                                      12 *    E7A7 VMO    - Vector Multiply Odd
                                                      13 *
                                                      14 *        James Wekel March 2025
                                                      15 *            July 2025 - Vector-enhancements facility 3 update
                                                      16 ****************************************************************************

                                                      18 ****************************************************************************
                                                      19 *
                                                      20 *        basic instruction tests
                                                      21 *
                                                      22 ****************************************************************************
                                                      23 *   This program tests proper functioning of the z/arch E7 VRR-c vector
                                                      24 *   multiply (logical high, low, high, logical even, logical odd,
                                                      25 *   even, and odd) instructions.
                                                      26 *   Exceptions are not tested.
                                                      27 *
                                                      28 *   PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                      29 *   obvious coding errors.  None of the tests are thorough.  They are
                                                      30 *   NOT designed to test all aspects of any of the instructions.
                                                      31 *
                                                      32 ****************************************************************************
                                                      33 *
                                                      34 *    *Testcase zvector-e7-09-multiply
                                                      35 *    *
                                                      36 *    *   Zvector E7 instruction tests for VRR-c encoded:
                                                      37 *    *
                                                      38 *    *   E7A1 VMLH   - Vector Multiply Logical High
                                                      39 *    *   E7A2 VML    - Vector Multiply Low
                                                      40 *    *   E7A3 VMH    - Vector Multiply High
                                                      41 *    *   E7A4 VMLE   - Vector Multiply Logical Even
                                                      42 *    *   E7A5 VMLO   - Vector Multiply Logical Odd
                                                      43 *    *   E7A6 VME    - Vector Multiply Even
                                                      44 *    *   E7A7 VMO    - Vector Multiply Odd
                                                      45 *    *
                                                      46 *    *   # ------------------------------------------------------------
                                                      47 *    *   #  This tests only the basic function of the instructions.
                                                      48 *    *   #  Exceptions are NOT tested.
                                                      49 *    *   # ------------------------------------------------------------
                                                      50 *    *
                                                      51 *    mainsize    2
                                                      52 *    numcpu      1
                                                      53 *    sysclear
                                                      54 *    archlvl     z/Arch
                                                      55 *
                                                      56 *    loadcore    "$(testpath)/zvector-e7-09-multiply.core" 0x0
```

```
 LOC        OBJECT CODE     ADDR1     ADDR2     STMT
                                                57 *
                                                58 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                59 *    runtest     2
                                                60 *    diag8cmd    disable   # (reset back to default)
                                                61 *
                                                62 *    *Done
                                                63 *
                                                64 ***********************************************************************
```

```
  LOC         OBJECT CODE      ADDR1    ADDR2    STMT

            66 ****************************************************************************
            67 *          FCHECK Macro - Is a Facility Bit set?
            68 *
            69 *          If the facility bit is NOT set, an message is issued and
            70 *          the test is skipped.
            71 *
            72 *          Fcheck uses R0, R1 and R2
            73 *
            74 * eg.      FCHECK 134,'vector-packed-decimal'
            75 ****************************************************************************
            76          MACRO
            77          FCHECK &BITNO,&NOTSETMSG
            78 .*                          &BITNO : facility bit number to check
            79 .*                          &NOTSETMSG : 'facility name'
            80          LCLA   &FBBYTE          Facility bit in Byte
            81          LCLA   &FBBIT           Facility bit within Byte
            82
            83          LCLA   &L(8)
            84 &L(1)    SetA   128,64,32,16,8,4,2,1  bit positions within byte
            85
            86 &FBBYTE  SETA   &BITNO/8
            87 &FBBIT   SETA   &L((&BITNO-(&FBBYTE*8))+1)
            88 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
            89
            90          B      X&SYSNDX                         Fcheck data area
            91 *                                                skip messgae
            92 *
            93 SKT&SYSNDX DC  C'     Skipping tests: '
            94          DC     C&NOTSETMSG
            95          DC     C' (bit &BITNO) is not installed.'
            96 SKL&SYSNDX EQU *-SKT&SYSNDX
            97 *                                                facility bits
            98          DS     FD                               gap
            99 FB&SYSNDX DS   4FD
           100          DS     FD                               gap
           101 *
           102 X&SYSNDX EQU *
           103          LA     R0,((X&SYSNDX-FB&SYSNDX)/8)-1
           104          STFLE  FB&SYSNDX               get facility bits
           105
           106          XGR    R0,R0
           107          IC     R0,FB&SYSNDX+&FBBYTE    get fbit byte
           108          N      R0,=F'&FBBIT'           is bit set?
           109          BNZ    XC&SYSNDX
           110 *
           111 * facility bit not set, issue message and exit
           112 *
           113          LA     R0,SKL&SYSNDX           message length
           114          LA     R1,SKT&SYSNDX           message address
           115          BAL    R2,MSG
           116
           117          B      EOJ
           118 XC&SYSNDX EQU *
           119          MEND
```

```
  LOC       OBJECT CODE      ADDR1     ADDR2     STMT

                                                 121 ********************************************************************
                                                 122 *       Low core PSWs
                                                 123 ********************************************************************
                             00000000  00005ECF  124 ZVE7TST  START 0
  00000000                   00000000            125          USING ZVE7TST,R0              Low core addressability
                                                 126
                             00000140  00000000  127 SVOLDPSW EQU   ZVE7TST+X'140'           z/Arch Supervisor call old PSW

  00000000                   00000000  000001A0  129          ORG   ZVE7TST+X'1A0'          z/Architecure RESTART PSW
  000001A0  00000001 80000000                    130          DC    X'0000000180000000'
  000001A8  00000000 00000200                    131          DC    AD(BEGIN)

  000001B0                   000001B0  000001D0  133          ORG   ZVE7TST+X'1D0'          z/Architecure PROGRAM CHECK PSW
  000001D0  00020001 80000000                    134          DC    X'0002000180000000'
  000001D8  00000000 0000DEAD                    135          DC    AD(X'DEAD')


  000001E0                   000001E0  00000200  137          ORG   ZVE7TST+X'200'          Start of actual test program..


                                                 139 ********************************************************************
                                                 140 *                The actual "ZVE7TST" program itself...
                                                 141 ********************************************************************
                                                 142 *
                                                 143 *   Architecture Mode: z/Arch
                                                 144 *   Register Usage:
                                                 145 *
                                                 146 *     R0          (work)
                                                 147 *     R1-4        (work)
                                                 148 *     R5          Testing control table - current test base
                                                 149 *     R6-R7       (work)
                                                 150 *     R8          First base register
                                                 151 *     R9          Second base register
                                                 152 *     R10         Third base register
                                                 153 *     R11         E7TEST call return
                                                 154 *     R12         E7TESTS register
                                                 155 *     R13         (work)
                                                 156 *     R14         Subroutine call
                                                 157 *     R15         Secondary Subroutine call or work
                                                 158 *
                                                 159 ********************************************************************

  00000200                   00000200            161          USING  BEGIN,R8              FIRST Base Register
  00000200                   00001200            162          USING  BEGIN+4096,R9         SECOND Base Register
  00000200                   00002200            163          USING  BEGIN+8192,R10        THIRD Base Register

  00000200  0580                                 165 BEGIN    BALR  R8,0                    Initialize FIRST base register
  00000202  0680                                 166          BCTR  R8,0                    Initialize FIRST base register
  00000204  0680                                 167          BCTR  R8,0                    Initialize FIRST base register

  00000206  4190 8800                  00000800  169          LA    R9,2048(,R8)            Initialize SECOND base register
  0000020A  4190 9800                  00000800  170          LA    R9,2048(,R9)            Initialize SECOND base register
                                                 171
```

```
  LOC        OBJECT CODE      ADDR1      ADDR2      STMT

0000020E  41A0 9800                    00000800    172            LA      R10,2048(,R9)      Initialize THIRD base register
00000212  41A0 A800                    00000800    173            LA      R10,2048(,R10)     Initialize THIRD base register
                                                   174
00000216  B600 833C                    0000053C    175            STCTL   R0,R0,CTLR0        Store CR0 to enable AFP
0000021A  9604 833D                    0000053D    176            OI      CTLR0+1,X'04'      Turn on AFP bit
0000021E  9602 833D                    0000053D    177            OI      CTLR0+1,X'02'      Turn on Vector bit
00000222  B700 833C                    0000053C    178            LCTL    R0,R0,CTLR0        Reload updated CR0
                                                   179
                                                   180  ********************************************************************
                                                   181  * Is z/Architecture vector facility installed  (bit 129)
                                                   182  ********************************************************************
                                                   183
                                                   184            FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                    000002A8    185+           B       X0001
                                                   186+*                                     Fcheck data area
                                                   187+*                                     skip messgae
0000022A  40404040 E2928997                        188+SKT0001    DC      C'    Skipping tests: '
0000023E  A961C199 838889A3                        189+           DC      C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                        190+           DC      C' (bit 129) is not installed.'
                             0000004E  00000001    191+SKL0001    EQU     *-SKT0001
                                                   192+*                                     facility bits
00000278  00000000 00000000                        193+           DS      FD                 gap
00000280  00000000 00000000                        194+FB0001     DS      4FD
000002A0  00000000 00000000                        195+           DS      FD                 gap
                                                   196+*
                             000002A8  00000001    197+X0001      EQU     *
000002A8  4100 0004                    00000004    198+           LA      R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                    00000280    199+           STFLE   FB0001             get facility bits
000002B0  B982 0000                                200+           XGR     R0,R0
000002B4  4300 8090                    00000290    201+           IC      R0,FB0001+16       get fbit byte
000002B8  5400 8344                    00000544    202+           N       R0,=F'64'          is bit set?
000002BC  4770 80D0                    000002D0    203+           BNZ     XC0001
                                                   204+*
                                                   205+* facility bit not set, issue message and exit
                                                   206+*
000002C0  4100 004E                    0000004E    207+           LA      R0,SKL0001         message length
000002C4  4110 802A                    0000022A    208+           LA      R1,SKT0001         message address
000002C8  4520 8258                    00000458    209+           BAL     R2,MSG
000002CC  47F0 8320                    00000520    210+           B       EOJ
                             000002D0  00000001    211+XC0001     EQU     *
```

```
  LOC        OBJECT CODE      ADDR1      ADDR2      STMT

                                                    213 ***********************************************************************
                                                    214 * Is z/Architecture vector facility installed  (bit 198)
                                                    215 ***********************************************************************
                                                    216
                                                    217         FCHECK 198,'Vector-enhancements facility 3'
000002D0   47F0 8158                      00000358  218+        B       X0002
                                                    219+*                                          Fcheck data area
                                                    220+*                                          skip messgae
000002D4   40404040 E2928997                        221+SKT0002 DC      C'    Skipping tests: '
000002E8   E58583A3 96996085                        222+        DC      C'Vector-enhancements facility 3'
00000306   404D8289 A340F1F9                        223+        DC      C' (bit 198) is not installed.'
                      0000004E   00000001  224+SKL0002 EQU     *-SKT0002
                                                    225+*                                          facility bits
00000328   00000000 00000000                        226+        DS      FD                         gap
00000330   00000000 00000000                        227+FB0002  DS      4FD
00000350   00000000 00000000                        228+        DS      FD                         gap
                                                    229+*
                      00000358   00000001  230+X0002   EQU     *
00000358   4100 0004                      00000004  231+        LA      R0,((X0002-FB0002)/8)-1
0000035C   B2B0 8130                      00000330  232+        STFLE   FB0002                     get facility bits
00000360   B982 0000                                233+        XGR     R0,R0
00000364   4300 8148                      00000348  234+        IC      R0,FB0002+24               get fbit byte
00000368   5400 8348                      00000548  235+        N       R0,=F'2'                   is bit set?
0000036C   4770 8180                      00000380  236+        BNZ     XC0002
                                                    237+*
                                                    238+* facility bit not set, issue message and exit
                                                    239+*
00000370   4100 004E                      0000004E  240+        LA      R0,SKL0002                 message length
00000374   4110 80D4                      000002D4  241+        LA      R1,SKT0002                 message address
00000378   4520 8258                      00000458  242+        BAL     R2,MSG
0000037C   47F0 8320                      00000520  243+        B       EOJ
                      00000380   00000001  244+XC0002  EQU     *
```

```
  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

                                                246 ****************************************************************************
                                                247 *                Do tests in the E7TESTS table
                                                248 ****************************************************************************
                                                249
00000380   58C0 834C                 0000054C   250         L     R12,=A(E7TESTS)      get table of test addresses
                                                251
                      00000384  00000001        252 NEXTE7  EQU   *
00000384   5850 C000                 00000000   253         L     R5,0(0,R12)          get test address
00000388   1255                                 254         LTR   R5,R5                    have a test?
0000038A   4780 81CE                 000003CE   255         BZ    ENDTEST                     done?
                                                256
0000038E             00000000                   257         USING E7TEST,R5
                                                258
0000038E   4800 5004                 00000004   259         LH    R0,TNUM              save current test number
00000392   5000 8E04                 00001004   260         ST    R0,TESTING           for easy reference
                                                261
00000396   E710 8E94 0006            00001094   262         VL    V1,V1FUDGE
0000039C   58B0 5000                 00000000   263         L     R11,TSUB             get address of test routine
000003A0   05BB                                 264         BALR  R11,R11              do test
                                                265
000003A2   E310 501C 0014            0000001C   266         LGF   R1,READDR            get address of expected result
000003A8   D50F 5028 1000   00000028  00000000  267         CLC   V10UTPUT,0(R1)       valid?
000003AE   4770 81BA                 000003BA   268         BNE   FAILMSG                 no, issue failed message
                                                269
000003B2   41C0 C004                 00000004   270         LA    R12,4(0,R12)         next test address
000003B6   47F0 8184                 00000384   271         B     NEXTE7
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				273 `*******************************************************************`
				274 `* result not as expected:`
				275 `*       issue message with test number, instruction under test`
				276 `*            and instruction m4`
				277 `*******************************************************************`
		000003BA	00000001	278 FAILMSG EQU `*`
000003BA	45F0 81DC		000003DC	279 BAL R15,RPTERROR
				281 `*******************************************************************`
				282 `* continue after a failed test`
				283 `*******************************************************************`
		000003BE	00000001	284 FAILCONT EQU `*`
000003BE	5800 8350		00000550	285 L R0,=F'1' set failed test indicator
000003C2	5000 8E00		00001000	286 ST R0,FAILED
				287
000003C6	41C0 C004		00000004	288 LA R12,4(0,R12) next test address
000003CA	47F0 8184		00000384	289 B NEXTE7
				291 `*******************************************************************`
				292 `* end of testing; set ending psw`
				293 `*******************************************************************`
		000003CE	00000001	294 ENDTEST EQU `*`
000003CE	5810 8E00		00001000	295 L R1,FAILED did a test fail?
000003D2	1211			296 LTR R1,R1
000003D4	4780 8320		00000520	297 BZ EOJ No, exit
000003D8	47F0 8338		00000538	298 B FAILTEST Yes, exit with BAD PSW

```
  LOC          OBJECT CODE      ADDR1      ADDR2     STMT

                                                     300  ****************************************************************
                                                     301  *          RPTERROR                    Report instruction test in error
                                                     302  ****************************************************************

000003DC  50F0 8240                       00000440   304  RPTERROR ST    R15,RPTSAVE         Save return address
000003E0  5050 8244                       00000444   305           ST    R5,RPTSVR5          Save R5
                                                     306  *
000003E4  4820 5004                       00000004   307           LH    R2,TNUM             get test number and convert
000003E8  4E20 8E73                       00001073   308           CVD   R2,DECNUM
000003EC  D211 8E5D 8E47   0000105D  00001047        309           MVC   PRT3,EDIT
000003F2  DE11 8E5D 8E73   0000105D  00001073        310           ED    PRT3,DECNUM
000003F8  D202 8E18 8E6A   00001018  0000106A        311           MVC   PRTNUM(3),PRT3+13   fill in message with test #
                                                     312
000003FE  D207 8E33 5008   00001033  00000008        313           MVC   PRTNAME,OPNAME      fill in message with instruction
                                                     314  *
00000404  E320 5007 0076                  00000007   315           LB    R2,m4               get m4 and convert
0000040A  4E20 8E73                       00001073   316           CVD   R2,DECNUM
0000040E  D211 8E5D 8E47   0000105D  00001047        317           MVC   PRT3,EDIT
00000414  DE11 8E5D 8E73   0000105D  00001073        318           ED    PRT3,DECNUM
0000041A  D201 8E44 8E6B   00001044  0000106B        319           MVC   PRTM4(2),PRT3+14    fill in message with m4 field

                                                     321  *
                                                     322  *         Use Hercules Diagnose for Message to console
                                                     323  *
00000420  9002 8248                       00000448   324           STM   R0,R2,RPTDWSAV      save regs used by MSG
00000424  4100 003F                       0000003F   325           LA    R0,PRTLNG           message length
00000428  4110 8E08                       00001008   326           LA    R1,PRTLINE          messagfe address
0000042C  4520 8258                       00000458   327           BAL   R2,MSG              call Hercules console MSG display
00000430  9802 8248                       00000448   328           LM    R0,R2,RPTDWSAV      restore regs


00000434  5850 8244                       00000444   330           L     R5,RPTSVR5          Restore R5
00000438  58F0 8240                       00000440   331           L     R15,RPTSAVE         Restore return address
0000043C  07FF                                       332           BR    R15                 Return to caller

00000440  00000000                                   334  RPTSAVE  DC    F'0'                R15 save area
00000444  00000000                                   335  RPTSVR5  DC    F'0'                R5 save area

00000448  00000000 00000000                          337  RPTDWSAV DC    2D'0'               R0-R2 save area for MSG call
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				339	**			
				340	*		Issue HERCULES MESSAGE pointed to by R1, length in R0	
				341	*		R2 = return address	
				342	**			
00000458	4900 8354		00000554	344	MSG	CH	R0,=H'0'	Do we even HAVE a message?
0000045C	07D2			345		BNHR	R2	No, ignore
0000045E	9002 8294		00000494	347		STM	R0,R2,MSGSAVE	Save registers
00000462	4900 8356		00000556	349		CH	R0,=AL2(L'MSGMSG)	Message length within limits?
00000466	47D0 826E		0000046E	350		BNH	MSGOK	Yes, continue
0000046A	4100 005F		0000005F	351		LA	R0,L'MSGMSG	No, set to maximum
0000046E	1820			353	MSGOK	LR	R2,R0	Copy length to work register
00000470	0620			354		BCTR	R2,0	Minus-1 for execute
00000472	4420 82A0		000004A0	355		EX	R2,MSGMVC	Copy message to O/P buffer
00000476	4120 200A		0000000A	357		LA	R2,1+L'MSGCMD(,R2)	Calculate true command length
0000047A	4110 82A6		000004A6	358		LA	R1,MSGCMD	Point to true command
0000047E	83120008			360		DC	X'83',X'12',X'0008'	Issue Hercules Diagnose X'008'
00000482	4780 828E		0000048E	361		BZ	MSGRET	Return if successful
				362				
00000486	1222			363		LTR	R2,R2	Is Diag8 Ry (R2) 0?
00000488	4780 828E		0000048E	364		BZ	MSGRET	an error occurred but coninue
				365				
0000048C	0000			366		DC	H'0'	CRASH for debugging purposes
0000048E	9802 8294		00000494	368	MSGRET	LM	R0,R2,MSGSAVE	Restore registers
00000492	07F2			369		BR	R2	Return to caller
00000494	00000000 00000000			371	MSGSAVE	DC	3F'0'	Registers save area
000004A0	D200 82AF 1000	000004AF	00000000	372	MSGMVC	MVC	MSGMSG(0),0(R1)	Executed instruction
000004A6	D4E2C7D5 D6C8405C			374	MSGCMD	DC	C'MSGNOH * '	*** HERCULES MESSAGE COMMAND ***
000004AF	40404040 40404040			375	MSGMSG	DC	CL95' '	The message text to be displayed
				376				

```
 LOC          OBJECT CODE      ADDR1    ADDR2    STMT

                                                 378 ****************************************************************************
                                                 379 *         Normal completion or Abnormal termination PSWs
                                                 380 ****************************************************************************


00000510   00020001 80000000                     382 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000520   B2B2 8310                  00000510    384 EOJ      LPSWE EOJPSW              Normal completion


00000528   00020001 80000000                     386 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

00000538   B2B2 8328                  00000528    388 FAILTEST LPSWE FAILPSW            Abnormal termination



                                                 390 ****************************************************************************
                                                 391 *         Working Storage
                                                 392 ****************************************************************************


0000053C   00000000                              394 CTLR0    DS    F                   CR0
00000540   00000000                              395          DS    F

00000544                                         397          LTORG ,                   Literals pool
00000544   00000040                              398                =F'64'
00000548   00000002                              399                =F'2'
0000054C   00005CC0                              400                =A(E7TESTS)
00000550   00000001                              401                =F'1'
00000554   0000                                  402                =H'0'
00000556   005F                                  403                =AL2(L'MSGMSG)
                                                 404
                                                 405 *        some constants
                                                 406
                       00000400    00000001      407 K        EQU   1024                One KB
                       00001000    00000001      408 PAGE     EQU   (4*K)               Size of one page
                       00010000    00000001      409 K64      EQU   (64*K)              64 KB
                       00100000    00000001      410 MB       EQU   (K*K)               1 MB
                                                 411
                       AABBCCDD    00000001      412 REG2PATT EQU   X'AABBCCDD'          Polluted Register pattern
                       000000DD    00000001      413 REG2LOW  EQU        X'DD'           (last byte above)
```

```
   LOC         OBJECT CODE      ADDR1     ADDR2     STMT

                                                    415 *====================================================================
                                                    416 *
                                                    417 *   NOTE: start data on an address that is easy to display
                                                    418 *         within Hercules
                                                    419 *
                                                    420 *====================================================================
                                                    421
00000558                        00000558  00001000  422          ORG    ZVE7TST+X'1000'
00001000  00000000                                  423 FAILED   DC     F'0'                        some test failed?
00001004  00000000                                  424 TESTING  DC     F'0'                        current test number

                                                    426 *
                                                    427 *          failed message and associated editting
                                                    428 *
00001008  40404040 40404040                         429 PRTLINE  DC     C'         Test # '
00001018  A7A7A7                                    430 PRTNUM   DC     C'xxx'
0000101B  40868189 93858440                         431          DC     c' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                          432 PRTNAME  DC     CL8'xxxxxxxx'
0000103B  40A689A3 884094F4                         433          DC     C' with m4='
00001044  A7A7                                      434 PRTm4    DC     C'xx'
00001046  4B                                        435          DC     C'.'
                                0000003F  00000001  436 PRTLNG   EQU    *-PRTLINE
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                  438 ***************************************************************************
                                                  439 *          TEST failed : message working storge
                                                  440 ***************************************************************************
00001047   40212020 20202020                      441 EDIT       DC     XL18'402120202020202020202020202020202020'
                                                  442
00001059   7E7E7E6E                               443            DC     C'===>'
0000105D   40404040 40404040                      444 PRT3       DC     CL18' '
0000106F   4C7E7E7E                               445            DC     C'<==='
00001073   00000000 00000000                      446 DECNUM     DS     CL16

                                                  448 ***************************************************************************
                                                  449 *          Vector instruction results, pollution and input
                                                  450 ***************************************************************************
00001084                                          451            DS     0F
00001084   00000000 00000000                      452            DS     XL16                                           gap
00001094   FFFFFFFF FFFFFFFF                       453 V1FUDGE    DC     XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010A4   00000000 00000000                      454            DS     XL16
```

```
  LOC         OBJECT CODE      ADDR1    ADDR2    STMT

                                                 456 ***********************************************************************
                                                 457 *          E7TEST DSECT
                                                 458 ***********************************************************************

                                                 460 E7TEST    DSECT ,
00000000   00000000                              461 TSUB      DC      A(0)            pointer  to test
00000004   0000                                  462 TNUM      DC      H'00'           Test Number
00000006   00                                    463          DC      X'00'
00000007   00                                    464 M4        DC      HL1'00'         m4 used
                                                 465
00000008   40404040 40404040                     466 OPNAME    DC      CL8' '          E7 name
00000010   00000000                              467 V2ADDR    DC      A(0)            address of v2 source
00000014   00000000                              468 V3ADDR    DC      A(0)            address of  v3 source
00000018   00000000                              469 RELEN     DC      A(0)            RESULT LENGTH
0000001C   00000000                              470 READDR    DC      A(0)            result (expected) address
00000020   00000000 00000000                     471          DS      FD                gap
00000028   00000000 00000000                     472 V1OUTPUT  DS      XL16            V1 Output
00000038   00000000 00000000                     473          DS      FD                gap
                                                 474
                                                 475 *       test routine will be here (from VRR-c macro)
                                                 476 *
                                                 477 *       followed by
                                                 478 *             EXPECTED RESULT

              00000000  00005ECF                480 ZVE7TST   CSECT ,
000010B4                                         481          DS      0F


                                                 483 ***********************************************************************
                                                 484 *     Macros to help build test tables
                                                 485 ***********************************************************************


                                                 487 *
                                                 488 * macro to generate individual test
                                                 489 *
                                                 490          MACRO
                                                 491          VRR_C &INST,&M4
                                                 492 .*                                   &INST   - VRR-c instruction under test
                                                 493 .*                                   &m4     - m4 field
                                                 494
                                                 495          GBLA   &TNUM
                                                 496 &TNUM    SETA   &TNUM+1
                                                 497
                                                 498          DS     0FD
                                                 499          USING  *,R5             base for test data and test routine
                                                 500
                                                 501 T&TNUM   DC      A(X&TNUM)        address of test routine
                                                 502          DC      H'&TNUM'        test number
                                                 503          DC      X'00'
                                                 504          DC      HL1'&M4'        m4
                                                 505          DC      CL8'&INST'      instruction name
                                                 506          DC      A(RE&TNUM+16)   address of v2 source
```

```
  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

                                                507            DC      A(RE&TNUM+32)       address of v3 source
                                                508            DC      A(16)               result length
                                                509 REA&TNUM DC        A(RE&TNUM)          result address
                                                510            DS      FD                  gap
                                                511 V10&TNUM DS        XL16                V1 output
                                                512            DS      FD                  gap
                                                513 .*
                                                514 *
                                                515 X&TNUM    DS      0F
                                                516            LGF     R1,V2ADDR           load v2 source
                                                517            VL      v22,0(R1)           use v22 to test decoder
                                                518
                                                519            LGF     R1,V3ADDR           load v3 source
                                                520            VL      v23,0(R1)           use v23 to test decoder
                                                521
                                                522            &INST V22,V22,V23,&M4        test instruction (dest is a source)
                                                523            VST     V22,V10&TNUM         save v1 output
                                                524
                                                525            BR      R11                 return
                                                526
                                                527 RE&TNUM   DC      0F                  xl16 expected result
                                                528
                                                529            DROP    R5
                                                530            MEND


                                                532 *
                                                533 * macro to generate table of pointers to individual tests
                                                534 *
                                                535            MACRO
                                                536            PTTABLE
                                                537            GBLA    &TNUM
                                                538            LCLA    &CUR
                                                539 &CUR       SETA    1
                                                540 .*
                                                541 TTABLE    DS      0F
                                                542 .LOOP     ANOP
                                                543 .*
                                                544            DC      A(T&CUR)
                                                545 .*
                                                546 &CUR       SETA    &CUR+1
                                                547            AIF     (&CUR LE &TNUM).LOOP
                                                548 *
                                                549            DC      A(0)                END OF TABLE
                                                550            DC      A(0)
                                                551 .*
                                                552            MEND
                                                553
```

```
  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

                                                    555 ****************************************************************************
                                                    556 *        E7 VRR-c tests
                                                    557 ****************************************************************************
                                                    558         PRINT DATA
                                                    559
                                                    560 *   E7A1 VMLH   - Vector Multiply Logical High
                                                    561 *   E7A2 VML    - Vector Multiply Low
                                                    562 *   E7A3 VMH    - Vector Multiply High
                                                    563 *   E7A4 VMLE   - Vector Multiply Logical Even
                                                    564 *   E7A5 VMLO   - Vector Multiply Logical Odd
                                                    565 *   E7A6 VME    - Vector Multiply Even
                                                    566 *   E7A7 VMO    - Vector Multiply Odd
                                                    567
                                                    568 *        VRR-c instruction, m4
                                                    569 *             followed by
                                                    570 *                16 byte expected result (V1)
                                                    571 *                16 byte V2 source
                                                    572 *                16 byte V3 source
                                                    573 *---------------------------------------------------------------------------
                                                    574 *  VMLH   - Vector Multiply Logical High
                                                    575 *---------------------------------------------------------------------------
                                                    576 * Byte
                                                    577         VRR_C VMLH,0
000010B8                                            578+         DS    0FD
000010B8                             000010B8       579+         USING *,R5              base for test data and test routine
000010B8  000010F8                                  580+T1       DC    A(X1)             address of test routine
000010BC  0001                                      581+         DC    H'1'              test number
000010BE  00                                        582+         DC    X'00'
000010BF  00                                        583+         DC    HL1'0'            m4
000010C0  E5D4D3C8 40404040                         584+         DC    CL8'VMLH'         instruction name
000010C8  00001130                                  585+         DC    A(RE1+16)         address of v2 source
000010CC  00001140                                  586+         DC    A(RE1+32)         address of v3 source
000010D0  00000010                                  587+         DC    A(16)             result length
000010D4  00001120                                  588+REA1     DC    A(RE1)            result address
000010D8  00000000 00000000                         589+         DS    FD                gap
000010E0  00000000 00000000                         590+V101     DS    XL16              V1 output
000010E8  00000000 00000000
000010F0  00000000 00000000                         591+         DS    FD                gap
                                                    592+*
000010F8                                            593+X1       DS    0F
000010F8  E310 5010 0014              00000010       594+         LGF   R1,V2ADDR         load v2 source
000010FE  E761 0000 0806              00000000       595+         VL    v22,0(R1)         use v22 to test decoder
00001104  E310 5014 0014              00000014       596+         LGF   R1,V3ADDR         load v3 source
0000110A  E771 0000 0806              00000000       597+         VL    v23,0(R1)         use v23 to test decoder
00001110  E766 7000 0EA1                             598+         VMLH  V22,V22,V23,0      test instruction (dest is a source)
00001116  E760 5028 080E              000010E0       599+         VST   V22,V101           save v1 output
0000111C  07FB                                       600+         BR    R11               return
00001120                                            601+RE1      DC    0F                xl16 expected result
00001120                                            602+         DROP  R5
00001120  FE000000 00000002                         603          DC    XL16'FE00000000000002 0000000C000000F4'   result
00001128  0000000C 000000F4
00001130  FF000000 00000019                         604          DC    XL16'FF0000000000019 00000038000000FA'    v2
00001138  00000038 000000FA
00001140  FF000000 00000019                         605          DC    XL16'FF00000000000019 00000038000000FA'   v3
00001148  00000038 000000FA
                                                    606
```

```
  LOC        OBJECT CODE      ADDR1     ADDR2      STMT


                                                   607            VRR_C VMLH, 0
00001150                                           608+           DS    0FD
00001150                               00001150    609+           USING *, R5              base for test data and test routine
00001150   00001190                               610+T2          DC    A(X2)              address of test routine
00001154   0002                                    611+           DC    H'2'               test number
00001156   00                                      612+           DC    X'00'
00001157   00                                      613+           DC    HL1'0'             m4
00001158   E5D4D3C8 40404040                        614+           DC    CL8'VMLH'          instruction name
00001160   000011C8                                615+           DC    A(RE2+16)          address of v2 source
00001164   000011D8                                616+           DC    A(RE2+32)          address of v3 source
00001168   00000010                                617+           DC    A(16)              result length
0000116C   000011B8                                618+REA2        DC    A(RE2)             result address
00001170   00000000 00000000                       619+           DS    FD                 gap
00001178   00000000 00000000                       620+V102        DS    XL16               V1 output
00001180   00000000 00000000
00001188   00000000 00000000                       621+           DS    FD                 gap
                                                   622+*
00001190                                           623+X2          DS    0F
00001190   E310 5010 0014              00000010    624+            LGF   R1, V2ADDR         load v2 source
00001196   E761 0000 0806              00000000    625+            VL    v22, 0(R1)         use v22 to test decoder
0000119C   E310 5014 0014              00000014    626+            LGF   R1, V3ADDR         load v3 source
000011A2   E771 0000 0806              00000000    627+            VL    v23, 0(R1)         use v23 to test decoder
000011A8   E766 7000 0EA1                          628+            VMLH  V22, V22, V23, 0    test instruction (dest is a source)
000011AE   E760 5028 080E              00001178    629+            VST   V22, V102           save v1 output
000011B4   07FB                                    630+            BR    R11                return
000011B8                                           631+RE2         DC    0F                 xl16 expected result
000011B8                                           632+            DROP  R5
000011B8   FE000000 00000019                       633             DC    XL16'FE00000000000019 00000038000000FA'    result
000011C0   00000038 000000FA
000011C8   FF020304 05060750                       634             DC    XL16'FF02030405060750 090A0B780C0D0EFD'    v2
000011D0   090A0B78 0C0D0EFD
000011D8   FF020304 05060750                       635             DC    XL16'FF02030405060750 090A0B780D0E0FFD'    v3
000011E0   090A0B78 0D0E0FFD
                                                   636
                                                   637            VRR_C VMLH, 0
000011E8                                           638+           DS    0FD
000011E8                               000011E8    639+           USING *, R5              base for test data and test routine
000011E8   00001228                                640+T3          DC    A(X3)              address of test routine
000011EC   0003                                    641+           DC    H'3'               test number
000011EE   00                                      642+           DC    X'00'
000011EF   00                                      643+           DC    HL1'0'             m4
000011F0   E5D4D3C8 40404040                        644+           DC    CL8'VMLH'          instruction name
000011F8   00001260                                645+           DC    A(RE3+16)          address of v2 source
000011FC   00001270                                646+           DC    A(RE3+32)          address of v3 source
00001200   00000010                                647+           DC    A(16)              result length
00001204   00001250                                648+REA3        DC    A(RE3)             result address
00001208   00000000 00000000                       649+           DS    FD                 gap
00001210   00000000 00000000                       650+V103        DS    XL16               V1 output
00001218   00000000 00000000
00001220   00000000 00000000                       651+           DS    FD                 gap
                                                   652+*
00001228                                           653+X3          DS    0F
00001228   E310 5010 0014              00000010    654+            LGF   R1, V2ADDR         load v2 source
0000122E   E761 0000 0806              00000000    655+            VL    v22, 0(R1)         use v22 to test decoder
00001234   E310 5014 0014              00000014    656+            LGF   R1, V3ADDR         load v3 source
0000123A   E771 0000 0806              00000000    657+            VL    v23, 0(R1)         use v23 to test decoder
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001240	E766 7000 0EA1			658+	VMLH	V22,V22,V23,0	test instruction (dest is a source)
00001246	E760 9010 080E		00001210	659+	VST	V22,V103	save v1 output
0000124C	07FB			660+	BR	R11	return
00001250				661+RE3	DC	0F	xl16 expected result
00001250				662+	DROP	R5	
00001250	FE000000 0000000C			663	DC	XL16'FE0000000000000C 0000001C000000FB'	result
00001258	0000001C 000000FB						
00001260	FF020304 05060750			664	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00001268	090A0B78 0C0D0EFD						
00001270	FF010102 02030328			665	DC	XL16'FF01010202030328 0405053C060707FE'	v3
00001278	0405053C 060707FE						
				666			
				667	VRR_C	VMLH,0	
00001280				668+	DS	0FD	
00001280		00001280		669+	USING	*,R5	base for test data and test routine
00001280	000012C0			670+T4	DC	A(X4)	address of test routine
00001284	0004			671+	DC	H'4'	test number
00001286	00			672+	DC	X'00'	
00001287	00			673+	DC	HL1'0'	m4
00001288	E5D4D3C8 40404040			674+	DC	CL8'VMLH'	instruction name
00001290	000012F8			675+	DC	A(RE4+16)	address of v2 source
00001294	00001308			676+	DC	A(RE4+32)	address of v3 source
00001298	00000010			677+	DC	A(16)	result length
0000129C	000012E8			678+REA4	DC	A(RE4)	result address
000012A0	00000000 00000000			679+	DS	FD	gap
000012A8	00000000 00000000			680+V104	DS	XL16	V1 output
000012B0	00000000 00000000						
000012B8	00000000 00000000			681+	DS	FD	gap
				682+*			
000012C0				683+X4	DS	0F	
000012C0	E310 5010 0014		00000010	684+	LGF	R1,V2ADDR	load v2 source
000012C6	E761 0000 0806		00000000	685+	VL	v22,0(R1)	use v22 to test decoder
000012CC	E310 5014 0014		00000014	686+	LGF	R1,V3ADDR	load v3 source
000012D2	E771 0000 0806		00000000	687+	VL	v23,0(R1)	use v23 to test decoder
000012D8	E766 7000 0EA1			688+	VMLH	V22,V22,V23,0	test instruction (dest is a source)
000012DE	E760 5028 080E		000012A8	689+	VST	V22,V104	save v1 output
000012E4	07FB			690+	BR	R11	return
000012E8				691+RE4	DC	0F	xl16 expected result
000012E8				692+	DROP	R5	
000012E8	FE000000 00000003			693	DC	XL16'FE00000000000003 00000007000000FC'	result
000012F0	00000007 000000FC						
000012F8	FF020304 05060750			694	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00001300	090A0B78 0C0D0EFD						
00001308	FF000000 0000000A			695	DC	XL16'FF0000000000000A 0101010F010101FF'	v3
00001310	0101010F 010101FF						
				696			
				697			
				698	* Halfword		
				699	VRR_C	VMLH,1	
00001318				700+	DS	0FD	
00001318		00001318		701+	USING	*,R5	base for test data and test routine
00001318	00001358			702+T5	DC	A(X5)	address of test routine
0000131C	0005			703+	DC	H'5'	test number
0000131E	00			704+	DC	X'00'	
0000131F	01			705+	DC	HL1'1'	m4
00001320	E5D4D3C8 40404040			706+	DC	CL8'VMLH'	instruction name

```
   LOC         OBJECT CODE       ADDR1     ADDR2    STMT

00001328   00001390                                 707+       DC      A(RE5+16)          address of v2 source
0000132C   000013A0                                 708+       DC      A(RE5+32)          address of v3 source
00001330   00000010                                 709+       DC      A(16)              result length
00001334   00001380                                 710+REA5   DC      A(RE5)             result address
00001338   00000000 00000000                        711+       DS      FD                 gap
00001340   00000000 00000000                        712+V105   DS      XL16               V1 output
00001348   00000000 00000000
00001350   00000000 00000000                        713+       DS      FD                 gap

                                                    714+*
00001358                                            715+X5     DS      0F
00001358   E310 5010 0014            00000010       716+       LGF     R1,V2ADDR          load v2 source
0000135E   E761 0000 0806            00000000       717+       VL      v22,0(R1)          use v22 to test decoder
00001364   E310 5014 0014            00000014       718+       LGF     R1,V3ADDR          load v3 source
0000136A   E771 0000 0806            00000000       719+       VL      v23,0(R1)          use v23 to test decoder
00001370   E766 7000 1EA1                           720+       VMLH    V22,V22,V23,1       test instruction (dest is a source)
00001376   E760 5028 080E            00001340       721+       VST     V22,V105            save v1 output
0000137C   07FB                                     722+       BR      R11                return
00001380                                            723+RE5    DC      0F                 xl16 expected result
00001380                                            724+       DROP    R5
00001380   FFFE0000 00000000                        725        DC      XL16'FFFE000000000000 000000000000DF15'    result
00001388   00000000 0000DF15
00001390   FFFF0000 00000019                        726        DC      XL16'FFFF000000000019 000000380000EEFA'    v2
00001398   00000038 0000EEFA
000013A0   FFFF0000 00000019                        727        DC      XL16'FFFF000000000019 000000380000EEFA'    v3
000013A8   00000038 0000EEFA

                                                    728
                                                    729        VRR_C   VMLH,1
000013B0                                            730+       DS      0FD
000013B0                         000013B0           731+       USING   *,R5               base for test data and test routine
000013B0   000013F0                                 732+T6     DC      A(X6)              address of test routine
000013B4   0006                                     733+       DC      H'6'               test number
000013B6   00                                       734+       DC      X'00'
000013B7   01                                       735+       DC      HL1'1'             m4
000013B8   E5D4D3C8 40404040                        736+       DC      CL8'VMLH'          instruction name
000013C0   00001428                                 737+       DC      A(RE6+16)          address of v2 source
000013C4   00001438                                 738+       DC      A(RE6+32)          address of v3 source
000013C8   00000010                                 739+       DC      A(16)              result length
000013CC   00001418                                 740+REA6   DC      A(RE6)             result address
000013D0   00000000 00000000                        741+       DS      FD                 gap
000013D8   00000000 00000000                        742+V106   DS      XL16               V1 output
000013E0   00000000 00000000
000013E8   00000000 00000000                        743+       DS      FD                 gap
                                                    744+*
000013F0                                            745+X6     DS      0F
000013F0   E310 5010 0014            00000010       746+       LGF     R1,V2ADDR          load v2 source
000013F6   E761 0000 0806            00000000       747+       VL      v22,0(R1)          use v22 to test decoder
000013FC   E310 5014 0014            00000014       748+       LGF     R1,V3ADDR          load v3 source
00001402   E771 0000 0806            00000000       749+       VL      v23,0(R1)          use v23 to test decoder
00001408   E766 7000 1EA1                           750+       VMLH    V22,V22,V23,1       test instruction (dest is a source)
0000140E   E760 5028 080E            000013D8       751+       VST     V22,V106            save v1 output
00001414   07FB                                     752+       BR      R11                return
00001418                                            753+RE6    DC      0F                 xl16 expected result
00001418                                            754+       DROP    R5
00001418   FE040009 00190035                        755        DC      XL16'FE04000900190035 00510083009D00EF'    result
00001420   00510083 009D00EF
00001428   FF020304 05060750                        756        DC      XL16'FF02030405060750 090A0B780C0D0EFD'    v2
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001430	090A0B78 0C0D0EFD							
00001438	FF020304 05060750			757		DC	XL16'FF02030405060750 090A0B780D0E0FFD'	v3
00001440	090A0B78 0D0E0FFD							
				758				
				759		VRR_C VMLH,1		
00001448				760+		DS	0FD	
00001448		00001448		761+		USING *,R5	base for test data and test routine	
00001448	00001488			762+T7		DC	A(X7)	address of test routine
0000144C	0007			763+		DC	H'7'	test number
0000144E	00			764+		DC	X'00'	
0000144F	01			765+		DC	HL1'1'	m4
00001450	E5D4D3C8 40404040			766+		DC	CL8'VMLH'	instruction name
00001458	000014C0			767+		DC	A(RE7+16)	address of v2 source
0000145C	000014D0			768+		DC	A(RE7+32)	address of v3 source
00001460	00000010			769+		DC	A(16)	result length
00001464	000014B0			770+REA7		DC	A(RE7)	result address
00001468	00000000 00000000			771+		DS	FD	gap
00001470	00000000 00000000			772+V107		DS	XL16	V1 output
00001478	00000000 00000000							
00001480	00000000 00000000			773+		DS	FD	gap
				774+*				
00001488				775+X7		DS	0F	
00001488	E310 5010 0014		00000010	776+		LGF	R1,V2ADDR	load v2 source
0000148E	E761 0000 0806		00000000	777+		VL	v22,0(R1)	use v22 to test decoder
00001494	E310 5014 0014		00000014	778+		LGF	R1,V3ADDR	load v3 source
0000149A	E771 0000 0806		00000000	779+		VL	v23,0(R1)	use v23 to test decoder
000014A0	E766 7000 1EA1			780+		VMLH	V22,V22,V23,1	test instruction (dest is a source)
000014A6	E760 5028 080E		00001470	781+		VST	V22,V107	save v1 output
000014AC	07FB			782+		BR	R11	return
000014B0				783+RE7		DC	0F	xl16 expected result
000014B0				784+		DROP	R5	
000014B0	FE030003 000A0017			785		DC	XL16'FE030003000A0017 0024003C00480077'	result
000014B8	0024003C 00480077							
000014C0	FF020304 05060750			786		DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
000014C8	090A0B78 0C0D0EFD							
000014D0	FF010102 02030328			787		DC	XL16'FF01010202030328 0405053C060707FE'	v3
000014D8	0405053C 060707FE							
				788				
				789		VRR_C VMLH,1		
000014E0				790+		DS	0FD	
000014E0		000014E0		791+		USING *,R5	base for test data and test routine	
000014E0	00001520			792+T8		DC	A(X8)	address of test routine
000014E4	0008			793+		DC	H'8'	test number
000014E6	00			794+		DC	X'00'	
000014E7	01			795+		DC	HL1'1'	m4
000014E8	E5D4D3C8 40404040			796+		DC	CL8'VMLH'	instruction name
000014F0	00001558			797+		DC	A(RE8+16)	address of v2 source
000014F4	00001568			798+		DC	A(RE8+32)	address of v3 source
000014F8	00000010			799+		DC	A(16)	result length
000014FC	00001548			800+REA8		DC	A(RE8)	result address
00001500	00000000 00000000			801+		DS	FD	gap
00001508	00000000 00000000			802+V108		DS	XL16	V1 output
00001510	00000000 00000000							
00001518	00000000 00000000			803+		DS	FD	gap
				804+*				
00001520				805+X8		DS	0F	

```
  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00001520  E310 5010 0014               00000010  806+        LGF    R1,V2ADDR           load v2 source
00001526  E761 0000 0806               00000000  807+        VL     v22,0(R1)           use v22 to test decoder
0000152C  E310 5014 0014               00000014  808+        LGF    R1,V3ADDR           load v3 source
00001532  E771 0000 0806               00000000  809+        VL     v23,0(R1)           use v23 to test decoder
00001538  E766 7000 1EA1                         810+        VMLH   V22,V22,V23,1        test instruction (dest is a source)
0000153E  E760 5028 080E               00001508  811+        VST    V22,V108            save v1 output
00001544  07FB                                   812+        BR     R11                 return
00001548                                         813+RE8     DC     0F                  xl16 expected result
00001548                                         814+        DROP   R5
00001548  FE020000 00000000                      815         DC     XL16'FE02000000000000 0009000C000C001D'    result
00001550  0009000C 000C001D
00001558  FF020304 05060750                      816         DC     XL16'FF02030405060750 090A0B780C0D0EFD'    v2
00001560  090A0B78 0C0D0EFD
00001568  FF000000 0000000A                      817         DC     XL16'FF000000000000000A 0101010F010101FF'  v3
00001570  0101010F 010101FF

                                                 818
                                                 819 * Word

                                                 820         VRR_C  VMLH,2
00001578                                         821+        DS     0FD
00001578                             00001578    822+        USING  *,R5                base for test data and test routine
00001578  000015B8                               823+T9      DC     A(X9)               address of test routine
0000157C  0009                                   824+        DC     H'9'                test number
0000157E  00                                     825+        DC     X'00'
0000157F  02                                     826+        DC     HL1'2'              m4
00001580  E5D4D3C8 40404040                      827+        DC     CL8'VMLH'           instruction name
00001588  000015F0                               828+        DC     A(RE9+16)           address of v2 source
0000158C  00001600                               829+        DC     A(RE9+32)           address of v3 source
00001590  00000010                               830+        DC     A(16)               result length
00001594  000015E0                               831+REA9    DC     A(RE9)              result address
00001598  00000000 00000000                      832+        DS     FD                  gap
000015A0  00000000 00000000                      833+V109    DS     XL16                V1 output
000015A8  00000000 00000000
000015B0  00000000 00000000                      834+        DS     FD                  gap
                                                 835+*
000015B8                                         836+X9      DS     0F
000015B8  E310 5010 0014               00000010  837+        LGF    R1,V2ADDR           load v2 source
000015BE  E761 0000 0806               00000000  838+        VL     v22,0(R1)           use v22 to test decoder
000015C4  E310 5014 0014               00000014  839+        LGF    R1,V3ADDR           load v3 source
000015CA  E771 0000 0806               00000000  840+        VL     v23,0(R1)           use v23 to test decoder
000015D0  E766 7000 2EA1                         841+        VMLH   V22,V22,V23,2        test instruction (dest is a source)
000015D6  E760 5028 080E               000015A0  842+        VST    V22,V109            save v1 output
000015DC  07FB                                   843+        BR     R11                 return
000015E0                                         844+RE9     DC     0F                  xl16 expected result
000015E0                                         845+        DROP   R5
000015E0  FFFFFFFE 00000002                      846         DC     XL16'FFFFFFFE00000002 00000000DF01235A'    result
000015E8  00000000 DF01235A
000015F0  FFFFFFFF 00019000                      847         DC     XL16'FFFFFFFF00019000 00000038EEEEEEFA'    v2
000015F8  00000038 EEEEEEFA
00001600  FFFFFFFF 00019000                      848         DC     XL16'FFFFFFFF00019000 00000038EEEEEEFA'    v3
00001608  00000038 EEEEEEFA

                                                 849
                                                 850         VRR_C  VMLH,2
00001610                                         851+        DS     0FD
00001610                             00001610    852+        USING  *,R5                base for test data and test routine
00001610  00001650                               853+T10     DC     A(X10)              address of test routine
00001614  000A                                   854+        DC     H'10'               test number
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001616	00			855+	DC	X'00'	
00001617	02			856+	DC	HL1'2'	m4
00001618	E5D4D3C8 40404040			857+	DC	CL8'VMLH'	instruction name
00001620	00001688			858+	DC	A(RE10+16)	address of v2 source
00001624	00001698			859+	DC	A(RE10+32)	address of v3 source
00001628	00000010			860+	DC	A(16)	result length
0000162C	00001678			861+REA10	DC	A(RE10)	result address
00001630	00000000 00000000			862+	DS	FD	gap
00001638	00000000 00000000			863+V1010	DS	XL16	V1 output
00001640	00000000 00000000						
00001648	00000000 00000000			864+	DS	FD	gap
				865+*			
00001650				866+X10	DS	0F	
00001650	E310 5010 0014		00000010	867+	LGF	R1,V2ADDR	load v2 source
00001656	E761 0000 0806		00000000	868+	VL	v22,0(R1)	use v22 to test decoder
0000165C	E310 5014 0014		00000014	869+	LGF	R1,V3ADDR	load v3 source
00001662	E771 0000 0806		00000000	870+	VL	v23,0(R1)	use v23 to test decoder
00001668	E766 7000 2EA1			871+	VMLH	V22,V22,V23,2	test instruction (dest is a source)
0000166E	E760 5028 080E		00001638	872+	VST	V22,V1010	save v1 output
00001674	07FB			873+	BR	R11	return
00001678				874+RE10	DC	0F	xl16 expected result
00001678				875+	DROP	R5	
00001678	FE050206 00193C6D			876	DC	XL16'FE05020600193C6D 0051B52B00AA6E58'	result
00001680	0051B52B 00AA6E58						
00001688	FF020304 05060750			877	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00001690	090A0B0C 0D0E0F7F						
00001698	FF020304 05060750			878	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v3
000016A0	090A0B0C 0D0E0F7F						
				879			
				880	VRR_C	VMLH,2	
000016A8				881+	DS	0FD	
000016A8		000016A8		882+	USING	*,R5	base for test data and test routine
000016A8	000016E8			883+T11	DC	A(X11)	address of test routine
000016AC	000B			884+	DC	H'11'	test number
000016AE	00			885+	DC	X'00'	
000016AF	02			886+	DC	HL1'2'	m4
000016B0	E5D4D3C8 40404040			887+	DC	CL8'VMLH'	instruction name
000016B8	00001720			888+	DC	A(RE11+16)	address of v2 source
000016BC	00001730			889+	DC	A(RE11+32)	address of v3 source
000016C0	00000010			890+	DC	A(16)	result length
000016C4	00001710			891+REA11	DC	A(RE11)	result address
000016C8	00000000 00000000			892+	DS	FD	gap
000016D0	00000000 00000000			893+V1011	DS	XL16	V1 output
000016D8	00000000 00000000						
000016E0	00000000 00000000			894+	DS	FD	gap
				895+*			
000016E8				896+X11	DS	0F	
000016E8	E310 5010 0014		00000010	897+	LGF	R1,V2ADDR	load v2 source
000016EE	E761 0000 0806		00000000	898+	VL	v22,0(R1)	use v22 to test decoder
000016F4	E310 5014 0014		00000014	899+	LGF	R1,V3ADDR	load v3 source
000016FA	E771 0000 0806		00000000	900+	VL	v23,0(R1)	use v23 to test decoder
00001700	E766 7000 2EA1			901+	VMLH	V22,V22,V23,2	test instruction (dest is a source)
00001706	E760 5028 080E		000016D0	902+	VST	V22,V1011	save v1 output
0000170C	07FB			903+	BR	R11	return
00001710				904+RE11	DC	0F	xl16 expected result
00001710				905+	DROP	R5	

```
   LOC          OBJECT CODE        ADDR1     ADDR2     STMT

00001710   FE040103 000A1B30                           906          DC      XL16'FE040103000A1B30 0024558D004EB01D'     result
00001718   0024558D 004EB01D
00001720   FF020304 05060750                           907          DC      XL16'FF02030405060750 090A0B0C0D0E0F7F'     v2
00001728   090A0B0C 0D0E0F7F
00001730   FF010102 02030328                           908          DC      XL16'FF010102 02030328 0405053C0607073F'    v3
00001738   0405053C 0607073F
                                                       909
                                                       910          VRR_C VMLH, 2
00001740                                               911+         DS      0FD
00001740                          00001740             912+         USING   *, R5                    base for test data and test routine
00001740   00001780                                    913+T12      DC      A(X12)                   address of test routine
00001744   000C                                        914+         DC      H'12'                    test number
00001746   00                                          915+         DC      X'00'
00001747   02                                          916+         DC      HL1'2'                   m4
00001748   E5D4D3C8 40404040                           917+         DC      CL8'VMLH'                instruction name
00001750   000017B8                                    918+         DC      A(RE12+16)               address of v2 source
00001754   000017C8                                    919+         DC      A(RE12+32)               address of v3 source
00001758   00000010                                    920+         DC      A(16)                    result length
0000175C   000017A8                                    921+REA12    DC      A(RE12)                  result address
00001760   00000000 00000000                           922+         DS      FD                       gap
00001768   00000000 00000000                           923+V1012    DS      XL16                     V1 output
00001770   00000000 00000000
00001778   00000000 00000000                           924+         DS      FD                       gap
                                                       925+*
00001780                                               926+X12      DS      0F
00001780   E310 5010 0014                   00000010   927+         LGF     R1, V2ADDR               load v2 source
00001786   E761 0000 0806                   00000000   928+         VL      v22, 0(R1)               use v22 to test decoder
0000178C   E310 5014 0014                   00000014   929+         LGF     R1, V3ADDR               load v3 source
00001792   E771 0000 0806                   00000000   930+         VL      v23, 0(R1)               use v23 to test decoder
00001798   E766 7000 2EA1                               931+         VMLH    V22, V22, V23, 2          test instruction (dest is a source)
0000179E   E760 5028 080E                   00001768   932+         VST     V22, V1012                save v1 output
000017A4   07FB                                         933+         BR      R11                      return
000017A8                                               934+RE12     DC      0F                       xl16 expected result
000017A8                                               935+         DROP    R5
000017A8   FE030100 00000000                           936          DC      XL16'FE03010000000000 0009131E000D1B2B'     result
000017B0   0009131E 000D1B2B
000017B8   FF020304 05060750                           937          DC      XL16'FF02030405060750 090A0B0C0D0E0F7F'     v2
000017C0   090A0B0C 0D0E0F7F
000017C8   FF000000 0000000A                           938          DC      XL16'FF0000000000000A 0101010F0101010F'     v3
000017D0   0101010F 0101010F
                                                       939
                                                       940  * Doubleword
                                                       941          VRR_C VMLH, 3
000017D8                                               942+         DS      0FD
000017D8                          000017D8             943+         USING   *, R5                    base for test data and test routine
000017D8   00001818                                    944+T13      DC      A(X13)                   address of test routine
000017DC   000D                                        945+         DC      H'13'                    test number
000017DE   00                                          946+         DC      X'00'
000017DF   03                                          947+         DC      HL1'3'                   m4
000017E0   E5D4D3C8 40404040                           948+         DC      CL8'VMLH'                instruction name
000017E8   00001850                                    949+         DC      A(RE13+16)               address of v2 source
000017EC   00001860                                    950+         DC      A(RE13+32)               address of v3 source
000017F0   00000010                                    951+         DC      A(16)                    result length
000017F4   00001840                                    952+REA13    DC      A(RE13)                  result address
000017F8   00000000 00000000                           953+         DS      FD                       gap
00001800   00000000 00000000                           954+V1013    DS      XL16                     V1 output
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001808	00000000 00000000						
00001810	00000000 00000000			955+	DS	FD	gap
				956+*			
00001818				957+X13	DS	0F	
00001818	E310 5010 0014		00000010	958+	LGF	R1,V2ADDR	load v2 source
0000181E	E761 0000 0806		00000000	959+	VL	v22,0(R1)	use v22 to test decoder
00001824	E310 5014 0014		00000014	960+	LGF	R1,V3ADDR	load v3 source
0000182A	E771 0000 0806		00000000	961+	VL	v23,0(R1)	use v23 to test decoder
00001830	E766 7000 3EA1			962+	VMLH	V22,V22,V23,3	test instruction (dest is a source)
00001836	E760 5028 080E		00001800	963+	VST	V22,V1013	save v1 output
0000183C	07FB			964+	BR	R11	return
00001840				965+RE13	DC	0F	xl16 expected result
00001840				966+	DROP	R5	
00001840	FFFFFFFE 00032000			967	DC	XL16'FFFFFFFE00032000 0000000000000C77'	result
00001848	00000000 00000C77						
00001850	FFFFFFFF 00019000			968	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00001858	00000038 EEEEEEFA						
00001860	FFFFFFFF 00019000			969	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00001868	00000038 0EEEEEFA						
				970			
				971	VRR_C	VMLH,3	
00001870				972+	DS	0FD	
00001870		00001870		973+	USING	*,R5	base for test data and test routine
00001870	000018B0			974+T14	DC	A(X14)	address of test routine
00001874	000E			975+	DC	H'14'	test number
00001876	00			976+	DC	X'00'	
00001877	03			977+	DC	HL1'3'	m4
00001878	E5D4D3C8 40404040			978+	DC	CL8'VMLH'	instruction name
00001880	000018E8			979+	DC	A(RE14+16)	address of v2 source
00001884	000018F8			980+	DC	A(RE14+32)	address of v3 source
00001888	00000010			981+	DC	A(16)	result length
0000188C	000018D8			982+REA14	DC	A(RE14)	result address
00001890	00000000 00000000			983+	DS	FD	gap
00001898	00000000 00000000			984+V1014	DS	XL16	V1 output
000018A0	00000000 00000000						
000018A8	00000000 00000000			985+	DS	FD	gap
				986+*			
000018B0				987+X14	DS	0F	
000018B0	E310 5010 0014		00000010	988+	LGF	R1,V2ADDR	load v2 source
000018B6	E761 0000 0806		00000000	989+	VL	v22,0(R1)	use v22 to test decoder
000018BC	E310 5014 0014		00000014	990+	LGF	R1,V3ADDR	load v3 source
000018C2	E771 0000 0806		00000000	991+	VL	v23,0(R1)	use v23 to test decoder
000018C8	E766 7000 3EA1			992+	VMLH	V22,V22,V23,3	test instruction (dest is a source)
000018CE	E760 5028 080E		00001898	993+	VST	V22,V1014	save v1 output
000018D4	07FB			994+	BR	R11	return
000018D8				995+RE14	DC	0F	xl16 expected result
000018D8				996+	DROP	R5	
000018D8	01010308 111F3396			997	DC	XL16'01010308111F3396 0051B52F8692B4F6'	result
000018E0	0051B52F 8692B4F6						
000018E8	FF020304 05060750			998	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
000018F0	090A0B0C 0D0E0F7F						
000018F8	01020304 05060750			999	DC	XL16'0102030405060750 090A0B780D0E0F7F'	v3
00001900	090A0B78 0D0E0F7F						
				1000			
				1001	VRR_C	VMLH,3	
00001908				1002+	DS	0FD	

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   LOC        OBJECT CODE      ADDR1     ADDR2     STMT


00001908                       00001908             1003+            USING *,R5                  base for test data and test routine
00001908   00001948                                 1004+T15         DC    A(X15)                address of test routine
0000190C   000F                                     1005+            DC    H'15'                 test number
0000190E   00                                       1006+            DC    X'00'
0000190F   03                                       1007+            DC    HL1'3'                m4
00001910   E5D4D3C8 40404040                        1008+            DC    CL8'VMLH'             instruction name
00001918   00001980                                 1009+            DC    A(RE15+16)            address of v2 source
0000191C   00001990                                 1010+            DC    A(RE15+32)            address of v3 source
00001920   00000010                                 1011+            DC    A(16)                 result length
00001924   00001970                                 1012+REA15       DC    A(RE15)               result address
00001928   00000000 00000000                        1013+            DS    FD                    gap
00001930   00000000 00000000                        1014+V1015       DS    XL16                  V1 output
00001938   00000000 00000000
00001940   00000000 00000000                        1015+            DS    FD                    gap
                                                     1016+*
00001948                                            1017+X15         DS    0F
00001948   E310 5010 0014                00000010   1018+            LGF   R1,V2ADDR             load v2 source
0000194E   E761 0000 0806                00000000   1019+            VL    v22,0(R1)             use v22 to test decoder
00001954   E310 5014 0014                00000014   1020+            LGF   R1,V3ADDR             load v3 source
0000195A   E771 0000 0806                00000000   1021+            VL    v23,0(R1)             use v23 to test decoder
00001960   E766 7000 3EA1                           1022+            VMLH  V22,V22,V23,3          test instruction (dest is a source)
00001966   E760 5028 080E                00001930   1023+            VST   V22,V1015              save v1 output
0000196C   07FB                                     1024+            BR    R11                   return
00001970                                            1025+RE15        DC    0F                    xl16 expected result
00001970                                            1026+            DROP  R5
00001970   00010003 050C1344                        1027             DC    XL16'00010003050C1344 0024558DB838C862'    result
00001978   0024558D B838C862
00001980   FF020304 05060750                        1028             DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00001988   090A0B0C 0D0E0F7F
00001990   00010102 02030328                        1029             DC    XL16'0001010202030328 0405053C0607073F'    v3
00001998   0405053C 0607073F

                                                     1030
                                                     1031             VRR_C VMLH,3
000019A0                                            1032+            DS    0FD
000019A0                       000019A0             1033+            USING *,R5                  base for test data and test routine
000019A0   000019E0                                 1034+T16         DC    A(X16)                address of test routine
000019A4   0010                                     1035+            DC    H'16'                 test number
000019A6   00                                       1036+            DC    X'00'
000019A7   03                                       1037+            DC    HL1'3'                m4
000019A8   E5D4D3C8 40404040                        1038+            DC    CL8'VMLH'             instruction name
000019B0   00001A18                                 1039+            DC    A(RE16+16)            address of v2 source
000019B4   00001A28                                 1040+            DC    A(RE16+32)            address of v3 source
000019B8   00000010                                 1041+            DC    A(16)                 result length
000019BC   00001A08                                 1042+REA16       DC    A(RE16)               result address
000019C0   00000000 00000000                        1043+            DS    FD                    gap
000019C8   00000000 00000000                        1044+V1016       DS    XL16                  V1 output
000019D0   00000000 00000000
000019D8   00000000 00000000                        1045+            DS    FD                    gap
                                                     1046+*
000019E0                                            1047+X16         DS    0F
000019E0   E310 5010 0014                00000010   1048+            LGF   R1,V2ADDR             load v2 source
000019E6   E761 0000 0806                00000000   1049+            VL    v22,0(R1)             use v22 to test decoder
000019EC   E310 5014 0014                00000014   1050+            LGF   R1,V3ADDR             load v3 source
000019F2   E771 0000 0806                00000000   1051+            VL    v23,0(R1)             use v23 to test decoder
000019F8   E766 7000 3EA1                           1052+            VMLH  V22,V22,V23,3          test instruction (dest is a source)
000019FE   E760 5028 080E                000019C8   1053+            VST   V22,V1016              save v1 output
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001A04	07FB			1054+	BR	R11		return
00001A08				1055+RE16	DC	0F		xl16 expected result
00001A08				1056+	DROP	R5		
00001A08	00000000 00000009			1057	DC	XL16'0000000000000009 0009131EA8C3DFFE'		result
00001A10	0009131E A8C3DFFE							
00001A18	FF020304 05060750			1058	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'		v2
00001A20	090A0B0C 0D0E0F7F							
00001A28	00000000 0000000A			1059	DC	XL16'000000000000000A 0101010F0101010F'		v3
00001A30	0101010F 0101010F							
				1060				
				1061	* Quadword			
				1062	VRR_C	VMLH,4		
00001A38				1063+	DS	0FD		
00001A38		00001A38		1064+	USING	*,R5		base for test data and test routine
00001A38	00001A78			1065+T17	DC	A(X17)		address of test routine
00001A3C	0011			1066+	DC	H'17'		test number
00001A3E	00			1067+	DC	X'00'		
00001A3F	04			1068+	DC	HL1'4'		m4
00001A40	E5D4D3C8 40404040			1069+	DC	CL8'VMLH'		instruction name
00001A48	00001AB0			1070+	DC	A(RE17+16)		address of v2 source
00001A4C	00001AC0			1071+	DC	A(RE17+32)		address of v3 source
00001A50	00000010			1072+	DC	A(16)		result length
00001A54	00001AA0			1073+REA17	DC	A(RE17)		result address
00001A58	00000000 00000000			1074+	DS	FD		gap
00001A60	00000000 00000000			1075+V1017	DS	XL16		V1 output
00001A68	00000000 00000000							
00001A70	00000000 00000000			1076+	DS	FD		gap
				1077+*				
00001A78				1078+X17	DS	0F		
00001A78	E310 5010 0014		00000010	1079+	LGF	R1,V2ADDR		load v2 source
00001A7E	E761 0000 0806		00000000	1080+	VL	v22,0(R1)		use v22 to test decoder
00001A84	E310 5014 0014		00000014	1081+	LGF	R1,V3ADDR		load v3 source
00001A8A	E771 0000 0806		00000000	1082+	VL	v23,0(R1)		use v23 to test decoder
00001A90	E766 7000 4EA1			1083+	VMLH	V22,V22,V23,4		test instruction (dest is a source)
00001A96	E760 5028 080E		00001A60	1084+	VST	V22,V1017		save v1 output
00001A9C	07FB			1085+	BR	R11		return
00001AA0				1086+RE17	DC	0F		xl16 expected result
00001AA0				1087+	DROP	R5		
00001AA0	FFFFFFFE 00032000			1088	DC	XL16'FFFFFFFE00032000 FFFCE0736EDDDD83'		result
00001AA8	FFFCE073 6EDDDD83							
00001AB0	FFFFFFFF 00019000			1089	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'		v2
00001AB8	00000038 EEEEEEFA							
00001AC0	FFFFFFFF 00019000			1090	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'		v3
00001AC8	00000038 0EEEEEFA							
				1091				
				1092	VRR_C	VMLH,4		
00001AD0				1093+	DS	0FD		
00001AD0		00001AD0		1094+	USING	*,R5		base for test data and test routine
00001AD0	00001B10			1095+T18	DC	A(X18)		address of test routine
00001AD4	0012			1096+	DC	H'18'		test number
00001AD6	00			1097+	DC	X'00'		
00001AD7	04			1098+	DC	HL1'4'		m4
00001AD8	E5D4D3C8 40404040			1099+	DC	CL8'VMLH'		instruction name
00001AE0	00001B48			1100+	DC	A(RE18+16)		address of v2 source
00001AE4	00001B58			1101+	DC	A(RE18+32)		address of v3 source
00001AE8	00000010			1102+	DC	A(16)		result length

```
  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

00001AEC   00001B38                                1103+REA18   DC    A(RE18)          result address
00001AF0   00000000 00000000                       1104+        DS    FD               gap
00001AF8   00000000 00000000                       1105+V1018   DS    XL16             V1 output
00001B00   00000000 00000000
00001B08   00000000 00000000                       1106+        DS    FD               gap
                                                   1107+*
00001B10                                           1108+X18     DS    0F
00001B10   E310 5010 0014             00000010      1109+        LGF   R1,V2ADDR        load v2 source
00001B16   E761 0000 0806             00000000      1110+        VL    v22,0(R1)        use v22 to test decoder
00001B1C   E310 5014 0014             00000014      1111+        LGF   R1,V3ADDR        load v3 source
00001B22   E771 0000 0806             00000000      1112+        VL    v23,0(R1)        use v23 to test decoder
00001B28   E766 7000 4EA1                           1113+        VMLH  V22,V22,V23,4     test instruction (dest is a source)
00001B2E   E760 5028 080E             00001AF8      1114+        VST   V22,V1018         save v1 output
00001B34   07FB                                    1115+        BR    R11              return
00001B38                                           1116+RE18    DC    0F               xl16 expected result
00001B38                                           1117+        DROP  R5
00001B38   01010308 111F3396                       1118         DC    XL16'01010308111F3396 72BF86C3CAFA7483'    result
00001B40   72BF86C3 CAFA7483
00001B48   FF020304 05060750                       1119         DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00001B50   090A0B0C 0D0E0F7F
00001B58   01020304 05060750                       1120         DC    XL16'0102030405060750 090A0B780D0E0F7F'    v3
00001B60   090A0B78 0D0E0F7F
                                                   1121
                                                   1122         VRR_C VMLH,4
00001B68                                           1123+        DS    0FD
00001B68                      00001B68             1124+        USING *,R5             base for test data and test routine
00001B68   00001BA8                                1125+T19     DC    A(X19)           address of test routine
00001B6C   0013                                    1126+        DC    H'19'            test number
00001B6E   00                                      1127+        DC    X'00'
00001B6F   04                                      1128+        DC    HL1'4'           m4
00001B70   E5D4D3C8 40404040                       1129+        DC    CL8'VMLH'        instruction name
00001B78   00001BE0                                1130+        DC    A(RE19+16)       address of v2 source
00001B7C   00001BF0                                1131+        DC    A(RE19+32)       address of v3 source
00001B80   00000010                                1132+        DC    A(16)            result length
00001B84   00001BD0                                1133+REA19   DC    A(RE19)          result address
00001B88   00000000 00000000                       1134+        DS    FD               gap
00001B90   00000000 00000000                       1135+V1019   DS    XL16             V1 output
00001B98   00000000 00000000
00001BA0   00000000 00000000                       1136+        DS    FD               gap
                                                   1137+*
00001BA8                                           1138+X19     DS    0F
00001BA8   E310 5010 0014             00000010      1139+        LGF   R1,V2ADDR        load v2 source
00001BAE   E761 0000 0806             00000000      1140+        VL    v22,0(R1)        use v22 to test decoder
00001BB4   E310 5014 0014             00000014      1141+        LGF   R1,V3ADDR        load v3 source
00001BBA   E771 0000 0806             00000000      1142+        VL    v23,0(R1)        use v23 to test decoder
00001BC0   E766 7000 4EA1                           1143+        VMLH  V22,V22,V23,4     test instruction (dest is a source)
00001BC6   E760 5028 080E             00001B90      1144+        VST   V22,V1019         save v1 output
00001BCC   07FB                                    1145+        BR    R11              return
00001BD0                                           1146+RE19    DC    0F               xl16 expected result
00001BD0                                           1147+        DROP  R5
00001BD0   00010003 050C1344                       1148         DC    XL16'00010003050C1344 0AD40FD0ABE579A1'    result
00001BD8   0AD40FD0 ABE579A1
00001BE0   FF020304 05060750                       1149         DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00001BE8   090A0B0C 0D0E0F7F
00001BF0   00010102 02030328                       1150         DC    XL16'0001010202030328 0405053C0607073F'    v3
00001BF8   0405053C 0607073F
```

```
  LOC          OBJECT CODE        ADDR1     ADDR2     STMT

                                                      1151
                                                      1152              VRR_C VMLH, 4
00001C00                                              1153+             DS    0FD
00001C00                            00001C00          1154+             USING *, R5              base for test data and test routine
00001C00     00001C40                                 1155+T20          DC    A(X20)             address of test routine
00001C04     0014                                     1156+             DC    H' 20'             test number
00001C06     00                                       1157+             DC    X' 00'
00001C07     04                                       1158+             DC    HL1' 4'            m4
00001C08     E5D4D3C8 40404040                         1159+             DC    CL8' VMLH'         instruction name
00001C10     00001C78                                 1160+             DC    A(RE20+16)         address of v2 source
00001C14     00001C88                                 1161+             DC    A(RE20+32)         address of v3 source
00001C18     00000010                                 1162+             DC    A(16)              result length
00001C1C     00001C68                                 1163+REA20        DC    A(RE20)            result address
00001C20     00000000 00000000                         1164+             DS    FD                 gap
00001C28     00000000 00000000                         1165+V1020       DS    XL16               V1 output
00001C30     00000000 00000000
00001C38     00000000 00000000                         1166+             DS    FD                 gap
                                                      1167+*
00001C40                                              1168+X20          DS    0F
00001C40     E310 5010 0014                 00000010  1169+             LGF   R1, V2ADDR         load v2 source
00001C46     E761 0000 0806                 00000000  1170+             VL    v22, 0(R1)         use v22 to test decoder
00001C4C     E310 5014 0014                 00000014  1171+             LGF   R1, V3ADDR         load v3 source
00001C52     E771 0000 0806                 00000000  1172+             VL    v23, 0(R1)         use v23 to test decoder
00001C58     E766 7000 4EA1                           1173+             VMLH  V22, V22, V23, 4     test instruction (dest is a source)
00001C5E     E760 5028 080E                 00001C28  1174+             VST   V22, V1020          save v1 output
00001C64     07FB                                     1175+             BR    R11                return
00001C68                                              1176+RE20         DC    0F                 xl16 expected result
00001C68                                              1177+             DROP  R5
00001C68     00000000 00000009                         1178              DC    XL16' 0000000000000009 F714203B2D668781'      result
00001C70     F714203B 2D668781
00001C78     FF020304 05060750                         1179              DC    XL16' FF02030405060750 090A0B0C0D0E0F7F'     v2
00001C80     090A0B0C 0D0E0F7F
00001C88     00000000 0000000A                         1180              DC    XL16' 000000000000000A 0101010F0101010F'     v3
00001C90     0101010F 0101010F
                                                      1181
                                                      1182 *-------------------------------------------------------------------
                                                      1183 *   VML     - Vector Multiply Low
                                                      1184 *-------------------------------------------------------------------
                                                      1185 * Byte
                                                      1186              VRR_C VML, 0
00001C98                                              1187+             DS    0FD
00001C98                            00001C98          1188+             USING *, R5              base for test data and test routine
00001C98     00001CD8                                 1189+T21          DC    A(X21)             address of test routine
00001C9C     0015                                     1190+             DC    H' 21'             test number
00001C9E     00                                       1191+             DC    X' 00'
00001C9F     00                                       1192+             DC    HL1' 0'            m4
00001CA0     E5D4D340 40404040                         1193+             DC    CL8' VML'          instruction name
00001CA8     00001D10                                 1194+             DC    A(RE21+16)         address of v2 source
00001CAC     00001D20                                 1195+             DC    A(RE21+32)         address of v3 source
00001CB0     00000010                                 1196+             DC    A(16)              result length
00001CB4     00001D00                                 1197+REA21        DC    A(RE21)            result address
00001CB8     00000000 00000000                         1198+             DS    FD                 gap
00001CC0     00000000 00000000                         1199+V1021       DS    XL16               V1 output
00001CC8     00000000 00000000
00001CD0     00000000 00000000                         1200+             DS    FD                 gap
                                                      1201+*
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001CD8				1202+X21	DS	0F	
00001CD8	E310 5010 0014		00000010	1203+	LGF	R1,V2ADDR	load v2 source
00001CDE	E761 0000 0806		00000000	1204+	VL	v22,0(R1)	use v22 to test decoder
00001CE4	E310 5014 0014		00000014	1205+	LGF	R1,V3ADDR	load v3 source
00001CEA	E771 0000 0806		00000000	1206+	VL	v23,0(R1)	use v23 to test decoder
00001CF0	E766 7000 0EA2			1207+	VML	V22,V22,V23,0	test instruction (dest is a source)
00001CF6	E760 5028 080E		00001CC0	1208+	VST	V22,V1021	save v1 output
00001CFC	07FB			1209+	BR	R11	return
00001D00				1210+RE21	DC	0F	xl16 expected result
00001D00				1211+	DROP	R5	
00001D00	01000000 00000071			1212	DC	XL16'010000000000071 0000004000000024'	result
00001D08	00000040 00000024						
00001D10	FF000000 00000019			1213	DC	XL16'FF00000000000019 00000038000000FA'	v2
00001D18	00000038 000000FA						
00001D20	FF000000 00000019			1214	DC	XL16'FF00000000000019 0000038000000FA'	v3
00001D28	00000038 000000FA						
				1215			
				1216	VRR_C	VML,0	
00001D30				1217+	DS	0FD	
00001D30		00001D30		1218+	USING	*,R5	base for test data and test routine
00001D30	00001D70			1219+T22	DC	A(X22)	address of test routine
00001D34	0016			1220+	DC	H'22'	test number
00001D36	00			1221+	DC	X'00'	
00001D37	00			1222+	DC	HL1'0'	m4
00001D38	E5D4D340 40404040			1223+	DC	CL8'VML'	instruction name
00001D40	00001DA8			1224+	DC	A(RE22+16)	address of v2 source
00001D44	00001DB8			1225+	DC	A(RE22+32)	address of v3 source
00001D48	00000010			1226+	DC	A(16)	result length
00001D4C	00001D98			1227+REA22	DC	A(RE22)	result address
00001D50	00000000 00000000			1228+	DS	FD	gap
00001D58	00000000 00000000			1229+V1022	DS	XL16	V1 output
00001D60	00000000 00000000						
00001D68	00000000 00000000			1230+	DS	FD	gap
				1231+*			
00001D70				1232+X22	DS	0F	
00001D70	E310 5010 0014		00000010	1233+	LGF	R1,V2ADDR	load v2 source
00001D76	E761 0000 0806		00000000	1234+	VL	v22,0(R1)	use v22 to test decoder
00001D7C	E310 5014 0014		00000014	1235+	LGF	R1,V3ADDR	load v3 source
00001D82	E771 0000 0806		00000000	1236+	VL	v23,0(R1)	use v23 to test decoder
00001D88	E766 7000 0EA2			1237+	VML	V22,V22,V23,0	test instruction (dest is a source)
00001D8E	E760 5028 080E		00001D58	1238+	VST	V22,V1022	save v1 output
00001D94	07FB			1239+	BR	R11	return
00001D98				1240+RE22	DC	0F	xl16 expected result
00001D98				1241+	DROP	R5	
00001D98	01040910 19243140			1242	DC	XL16'0104091019243140 51647990A9C4E100'	result
00001DA0	51647990 A9C4E100						
00001DA8	FF020304 05060708			1243	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00001DB0	090A0B0C 0D0E0F10						
00001DB8	FF020304 05060708			1244	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3
00001DC0	090A0B0C 0D0E0F10						
				1245			
				1246	VRR_C	VML,0	
00001DC8				1247+	DS	0FD	
00001DC8		00001DC8		1248+	USING	*,R5	base for test data and test routine
00001DC8	00001E08			1249+T23	DC	A(X23)	address of test routine
00001DCC	0017			1250+	DC	H'23'	test number

```
  LOC          OBJECT CODE       ADDR1     ADDR2     STMT

00001DCE  00                                         1251+         DC     X'00'
00001DCF  00                                         1252+         DC     HL1'0'                m4
00001DD0  E5D4D340 40404040                          1253+         DC     CL8'VML'              instruction name
00001DD8  00001E40                                   1254+         DC     A(RE23+16)            address of v2 source
00001DDC  00001E50                                   1255+         DC     A(RE23+32)            address of v3 source
00001DE0  00000010                                   1256+         DC     A(16)                result length
00001DE4  00001E30                                   1257+REA23    DC     A(RE23)              result address
00001DE8  00000000 00000000                          1258+         DS     FD                   gap
00001DF0  00000000 00000000                          1259+V1023    DS     XL16                 V1 output
00001DF8  00000000 00000000
00001E00  00000000 00000000                          1260+         DS     FD                   gap
                                                     1261+*
00001E08                                             1262+X23      DS     0F
00001E08  E310 5010 0014              00000010       1263+         LGF    R1,V2ADDR            load v2 source
00001E0E  E761 0000 0806              00000000       1264+         VL     v22,0(R1)            use v22 to test decoder
00001E14  E310 5014 0014              00000014       1265+         LGF    R1,V3ADDR            load v3 source
00001E1A  E771 0000 0806              00000000       1266+         VL     v23,0(R1)            use v23 to test decoder
00001E20  E766 7000 0EA2                             1267+         VML    V22,V22,V23,0         test instruction (dest is a source)
00001E26  E760 5028 080E              00001DF0       1268+         VST    V22,V1023             save v1 output
00001E2C  07FB                                       1269+         BR     R11                  return
00001E30                                             1270+RE23     DC     0F                   xl16 expected result
00001E30                                             1271+         DROP   R5
00001E30  01020308 0A121520                          1272          DC     XL16'010203080A121520 243237484E626980'      result
00001E38  24323748 4E626980
00001E40  FF020304 05060708                          1273          DC     XL16'FF02030405060708 090A0B0C0D0E0F10'      v2
00001E48  090A0B0C 0D0E0F10
00001E50  FF010102 02030304                          1274          DC     XL16'FF01010202030304 0405050606070708'      v3
00001E58  04050506 06070708
                                                     1275
                                                     1276          VRR_C  VML,0
00001E60                                             1277+         DS     0FD
00001E60                          00001E60           1278+         USING  *,R5                 base for test data and test routine
00001E60  00001EA0                                   1279+T24      DC     A(X24)               address of test routine
00001E64  0018                                       1280+         DC     H'24'                test number
00001E66  00                                         1281+         DC     X'00'
00001E67  00                                         1282+         DC     HL1'0'                m4
00001E68  E5D4D340 40404040                          1283+         DC     CL8'VML'              instruction name
00001E70  00001ED8                                   1284+         DC     A(RE24+16)            address of v2 source
00001E74  00001EE8                                   1285+         DC     A(RE24+32)            address of v3 source
00001E78  00000010                                   1286+         DC     A(16)                result length
00001E7C  00001EC8                                   1287+REA24    DC     A(RE24)              result address
00001E80  00000000 00000000                          1288+         DS     FD                   gap
00001E88  00000000 00000000                          1289+V1024    DS     XL16                 V1 output
00001E90  00000000 00000000
00001E98  00000000 00000000                          1290+         DS     FD                   gap
                                                     1291+*
00001EA0                                             1292+X24      DS     0F
00001EA0  E310 5010 0014              00000010       1293+         LGF    R1,V2ADDR            load v2 source
00001EA6  E761 0000 0806              00000000       1294+         VL     v22,0(R1)            use v22 to test decoder
00001EAC  E310 5014 0014              00000014       1295+         LGF    R1,V3ADDR            load v3 source
00001EB2  E771 0000 0806              00000000       1296+         VL     v23,0(R1)            use v23 to test decoder
00001EB8  E766 7000 0EA2                             1297+         VML    V22,V22,V23,0         test instruction (dest is a source)
00001EBE  E760 5028 080E              00001E88       1298+         VST    V22,V1024             save v1 output
00001EC4  07FB                                       1299+         BR     R11                  return
00001EC8                                             1300+RE24     DC     0F                   xl16 expected result
00001EC8                                             1301+         DROP   R5
```

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  LOC          OBJECT CODE      ADDR1     ADDR2     STMT

00001EC8  01000000 00000008                         1302        DC      XL16'0100000000000008 090A0B0C0D0E0F20'     result
00001ED0  090A0B0C 0D0E0F20
00001ED8  FF020304 05060708                         1303        DC      XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
00001EE0  090A0B0C 0D0E0F10
00001EE8  FF000000 00000001                         1304        DC      XL16'FF00000000000001 0101010101010102'     v3
00001EF0  01010101 01010102
                                                    1305
                                                    1306 * Halfword
                                                    1307        VRR_C  VML,1
00001EF8                                            1308+       DS      0FD
00001EF8                       00001EF8             1309+       USING  *,R5                    base for test data and test routine
00001EF8  00001F38                                  1310+T25    DC      A(X25)                  address of test routine
00001EFC  0019                                      1311+       DC      H'25'                   test number
00001EFE  00                                        1312+       DC      X'00'
00001EFF  01                                        1313+       DC      HL1'1'                  m4
00001F00  E5D4D340 40404040                         1314+       DC      CL8'VML'                instruction name
00001F08  00001F70                                  1315+       DC      A(RE25+16)              address of v2 source
00001F0C  00001F80                                  1316+       DC      A(RE25+32)              address of v3 source
00001F10  00000010                                  1317+       DC      A(16)                   result length
00001F14  00001F60                                  1318+REA25  DC      A(RE25)                 result address
00001F18  00000000 00000000                         1319+       DS      FD                      gap
00001F20  00000000 00000000                         1320+V1025  DS      XL16                    V1 output
00001F28  00000000 00000000
00001F30  00000000 00000000                         1321+       DS      FD                      gap
                                                    1322+*
00001F38                                            1323+X25    DS      0F
00001F38  E310 5010 0014                 00000010   1324+       LGF     R1,V2ADDR               load v2 source
00001F3E  E761 0000 0806                 00000000   1325+       VL      v22,0(R1)               use v22 to test decoder
00001F44  E310 5014 0014                 00000014   1326+       LGF     R1,V3ADDR               load v3 source
00001F4A  E771 0000 0806                 00000000   1327+       VL      v23,0(R1)               use v23 to test decoder
00001F50  E766 7000 1EA2                             1328+       VML     V22,V22,V23,1            test instruction (dest is a source)
00001F56  E760 5028 080E                 00001F20   1329+       VST     V22,V1025                save v1 output
00001F5C  07FB                                       1330+       BR      R11                     return
00001F60                                             1331+RE25   DC      0F                      xl16 expected result
00001F60                                             1332+       DROP    R5
00001F60  00010000 00000271                          1333        DC      XL16'0001000000000271 00000C400000CC24'     result
00001F68  00000C40 0000CC24
00001F70  FFFF0000 00000019                          1334        DC      XL16'FFFF000000000019 000000380000EEFA'     v2
00001F78  00000038 0000EEFA
00001F80  FFFF0000 00000019                          1335        DC      XL16'FFFF000000000019 000000380000EEFA'     v3
00001F88  00000038 0000EEFA
                                                    1336
                                                    1337        VRR_C  VML,1
00001F90                                            1338+       DS      0FD
00001F90                       00001F90             1339+       USING  *,R5                    base for test data and test routine
00001F90  00001FD0                                  1340+T26    DC      A(X26)                  address of test routine
00001F94  001A                                      1341+       DC      H'26'                   test number
00001F96  00                                        1342+       DC      X'00'
00001F97  01                                        1343+       DC      HL1'1'                  m4
00001F98  E5D4D340 40404040                         1344+       DC      CL8'VML'                instruction name
00001FA0  00002008                                  1345+       DC      A(RE26+16)              address of v2 source
00001FA4  00002018                                  1346+       DC      A(RE26+32)              address of v3 source
00001FA8  00000010                                  1347+       DC      A(16)                   result length
00001FAC  00001FF8                                  1348+REA26  DC      A(RE26)                 result address
00001FB0  00000000 00000000                         1349+       DS      FD                      gap
00001FB8  00000000 00000000                         1350+V1026  DS      XL16                    V1 output
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001FC0	00000000 00000000						
00001FC8	00000000 00000000			1351+	DS	FD	gap
				1352+*			
00001FD0				1353+X26	DS	0F	
00001FD0	E310 5010 0014		00000010	1354+	LGF	R1,V2ADDR	load v2 source
00001FD6	E761 0000 0806		00000000	1355+	VL	v22,0(R1)	use v22 to test decoder
00001FDC	E310 5014 0014		00000014	1356+	LGF	R1,V3ADDR	load v3 source
00001FE2	E771 0000 0806		00000000	1357+	VL	v23,0(R1)	use v23 to test decoder
00001FE8	E766 7000 1EA2			1358+	VML	V22,V22,V23,1	test instruction (dest is a source)
00001FEE	E760 5028 080E		00001FB8	1359+	VST	V22,V1026	save v1 output
00001FF4	07FB			1360+	BR	R11	return
00001FF8				1361+RE26	DC	0F	xl16 expected result
00001FF8				1362+	DROP	R5	
00001FF8	FC041810 3C247040			1363	DC	XL16'FC0418103C247040 B46408906CC4E100'	result
00002000	B4640890 6CC4E100						
00002008	FF020304 05060708			1364	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00002010	090A0B0C 0D0E0F10						
00002018	FF020304 05060708			1365	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3
00002020	090A0B0C 0D0E0F10						
				1366			
				1367	VRR_C VML,1		
00002028				1368+	DS	0FD	
00002028			00002028	1369+	USING *,R5		base for test data and test routine
00002028	00002068			1370+T27	DC	A(X27)	address of test routine
0000202C	001B			1371+	DC	H'27'	test number
0000202E	00			1372+	DC	X'00'	
0000202F	01			1373+	DC	HL1'1'	m4
00002030	E5D4D340 40404040			1374+	DC	CL8'VML'	instruction name
00002038	000020A0			1375+	DC	A(RE27+16)	address of v2 source
0000203C	000020B0			1376+	DC	A(RE27+32)	address of v3 source
00002040	00000010			1377+	DC	A(16)	result length
00002044	00002090			1378+REA27	DC	A(RE27)	result address
00002048	00000000 00000000			1379+	DS	FD	gap
00002050	00000000 00000000			1380+V1027	DS	XL16	V1 output
00002058	00000000 00000000						
00002060	00000000 00000000			1381+	DS	FD	gap
				1382+*			
00002068				1383+X27	DS	0F	
00002068	E310 5010 0014		00000010	1384+	LGF	R1,V2ADDR	load v2 source
0000206E	E761 0000 0806		00000000	1385+	VL	v22,0(R1)	use v22 to test decoder
00002074	E310 5014 0014		00000014	1386+	LGF	R1,V3ADDR	load v3 source
0000207A	E771 0000 0806		00000000	1387+	VL	v23,0(R1)	use v23 to test decoder
00002080	E766 7000 1EA2			1388+	VML	V22,V22,V23,1	test instruction (dest is a source)
00002086	E760 5028 080E		00002050	1389+	VST	V22,V1027	save v1 output
0000208C	07FB			1390+	BR	R11	return
00002090				1391+RE27	DC	0F	xl16 expected result
00002090				1392+	DROP	R5	
00002090	FD020A08 1B123420			1393	DC	XL16'FD020A081B123420 55327E48AF62E880'	result
00002098	55327E48 AF62E880						
000020A0	FF020304 05060708			1394	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
000020A8	090A0B0C 0D0E0F10						
000020B0	FF010102 02030304			1395	DC	XL16'FF01010202030304 0405050606070708'	v3
000020B8	04050506 06070708						
				1396			
				1397	VRR_C VML,1		
000020C0				1398+	DS	0FD	

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT


 000020C0                       000020C0            1399+          USING *,R5               base for test data and test routine
 000020C0   00002100                                1400+T28       DC    A(X28)             address of test routine
 000020C4   001C                                    1401+         DC    H'28'              test number
 000020C6   00                                      1402+         DC    X'00'
 000020C7   01                                      1403+         DC    HL1'1'             m4
 000020C8   E5D4D340 40404040                        1404+         DC    CL8'VML'           instruction name
 000020D0   00002138                                1405+         DC    A(RE28+16)         address of v2 source
 000020D4   00002148                                1406+         DC    A(RE28+32)         address of v3 source
 000020D8   00000010                                1407+         DC    A(16)              result length
 000020DC   00002128                                1408+REA28     DC    A(RE28)            result address
 000020E0   00000000 00000000                       1409+         DS    FD                 gap
 000020E8   00000000 00000000                       1410+V1028     DS    XL16               V1 output
 000020F0   00000000 00000000
 000020F8   00000000 00000000                       1411+         DS    FD                 gap
                                                    1412+*
 00002100                                           1413+X28       DS    0F
 00002100   E310 5010 0014                00000010  1414+         LGF   R1,V2ADDR          load v2 source
 00002106   E761 0000 0806                00000000  1415+         VL    v22,0(R1)          use v22 to test decoder
 0000210C   E310 5014 0014                00000014  1416+         LGF   R1,V3ADDR          load v3 source
 00002112   E771 0000 0806                00000000  1417+         VL    v23,0(R1)          use v23 to test decoder
 00002118   E766 7000 1EA2                          1418+         VML   V22,V22,V23,1       test instruction (dest is a source)
 0000211E   E760 5028 080E                000020E8  1419+         VST   V22,V1028           save v1 output
 00002124   07FB                                    1420+         BR    R11                return
 00002128                                           1421+RE28     DC    0F                 xl16 expected result
 00002128                                           1422+         DROP  R5
 00002128   FE000000 00000708                        1423          DC    XL16'FE00000000000708 130A170C1B0E2E20'     result
 00002130   130A170C 1B0E2E20
 00002138   FF020304 05060708                        1424          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'     v2
 00002140   090A0B0C 0D0E0F10
 00002148   FF000000 00000001                        1425          DC    XL16'FF00000000000001 0101010101010102'     v3
 00002150   01010101 01010102
                                                    1426
                                                    1427 * Word
                                                    1428          VRR_C VML,2
 00002158                                           1429+         DS    0FD
 00002158                       00002158            1430+          USING *,R5               base for test data and test routine
 00002158   00002198                                1431+T29       DC    A(X29)             address of test routine
 0000215C   001D                                    1432+         DC    H'29'              test number
 0000215E   00                                      1433+         DC    X'00'
 0000215F   02                                      1434+         DC    HL1'2'             m4
 00002160   E5D4D340 40404040                        1435+         DC    CL8'VML'           instruction name
 00002168   000021D0                                1436+         DC    A(RE29+16)         address of v2 source
 0000216C   000021E0                                1437+         DC    A(RE29+32)         address of v3 source
 00002170   00000010                                1438+         DC    A(16)              result length
 00002174   000021C0                                1439+REA29     DC    A(RE29)            result address
 00002178   00000000 00000000                       1440+         DS    FD                 gap
 00002180   00000000 00000000                       1441+V1029     DS    XL16               V1 output
 00002188   00000000 00000000
 00002190   00000000 00000000                       1442+         DS    FD                 gap
                                                    1443+*
 00002198                                           1444+X29       DS    0F
 00002198   E310 5010 0014                00000010  1445+         LGF   R1,V2ADDR          load v2 source
 0000219E   E761 0000 0806                00000000  1446+         VL    v22,0(R1)          use v22 to test decoder
 000021A4   E310 5014 0014                00000014  1447+         LGF   R1,V3ADDR          load v3 source
 000021AA   E771 0000 0806                00000000  1448+         VL    v23,0(R1)          use v23 to test decoder
 000021B0   E766 7000 2EA2                          1449+         VML   V22,V22,V23,2       test instruction (dest is a source)
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000021B6	E760 5028 080E		00002180	1450+	VST	V22,V1029	save v1 output
000021BC	07FB			1451+	BR	R11	return
000021C0				1452+RE29	DC	0F	xl16 expected result
000021C0				1453+	DROP	R5	
000021C0	00000001 71000000			1454	DC	XL16'0000000171000000 00000C400FEDCC24'	result
000021C8	00000C40 0FEDCC24						
000021D0	FFFFFFFF 00019000			1455	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
000021D8	00000038 EEEEEEFA						
000021E0	FFFFFFFF 00019000			1456	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v3
000021E8	00000038 EEEEEEFA						
				1457			
				1458	VRR_C	VML,2	
000021F0				1459+	DS	0FD	
000021F0			000021F0	1460+	USING	*,R5	base for test data and test routine
000021F0	00002230			1461+T30	DC	A(X30)	address of test routine
000021F4	001E			1462+	DC	H'30'	test number
000021F6	00			1463+	DC	X'00'	
000021F7	02			1464+	DC	HL1'2'	m4
000021F8	E5D4D340 40404040			1465+	DC	CL8'VML'	instruction name
00002200	00002268			1466+	DC	A(RE30+16)	address of v2 source
00002204	00002278			1467+	DC	A(RE30+32)	address of v3 source
00002208	00000010			1468+	DC	A(16)	result length
0000220C	00002258			1469+REA30	DC	A(RE30)	result address
00002210	00000000 00000000			1470+	DS	FD	gap
00002218	00000000 00000000			1471+V1030	DS	XL16	V1 output
00002220	00000000 00000000						
00002228	00000000 00000000			1472+	DS	FD	gap
				1473+*			
00002230				1474+X30	DS	0F	
00002230	E310 5010 0014		00000010	1475+	LGF	R1,V2ADDR	load v2 source
00002236	E761 0000 0806		00000000	1476+	VL	v22,0(R1)	use v22 to test decoder
0000223C	E310 5014 0014		00000014	1477+	LGF	R1,V3ADDR	load v3 source
00002242	E771 0000 0806		00000000	1478+	VL	v23,0(R1)	use v23 to test decoder
00002248	E766 7000 2EA2			1479+	VML	V22,V22,V23,2	test instruction (dest is a source)
0000224E	E760 A018 080E		00002218	1480+	VST	V22,V1030	save v1 output
00002254	07FB			1481+	BR	R11	return
00002258				1482+RE30	DC	0F	xl16 expected result
00002258				1483+	DROP	R5	
00002258	04191810 A4917040			1484	DC	XL16'04191810A4917040 B56A089046A2E100'	result
00002260	B56A0890 46A2E100						
00002268	FF020304 05060708			1485	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00002270	090A0B0C 0D0E0F10						
00002278	FF020304 05060708			1486	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v3
00002280	090A0B0C 0D0E0F10						
				1487			
				1488	VRR_C	VML,2	
00002288				1489+	DS	0FD	
00002288			00002288	1490+	USING	*,R5	base for test data and test routine
00002288	000022C8			1491+T31	DC	A(X31)	address of test routine
0000228C	001F			1492+	DC	H'31'	test number
0000228E	00			1493+	DC	X'00'	
0000228F	02			1494+	DC	HL1'2'	m4
00002290	E5D4D340 40404040			1495+	DC	CL8'VML'	instruction name
00002298	00002300			1496+	DC	A(RE31+16)	address of v2 source
0000229C	00002310			1497+	DC	A(RE31+32)	address of v3 source
000022A0	00000010			1498+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000022A4	000022F0			1499+REA31	DC	A(RE31)	result address
000022A8	00000000 00000000			1500+	DS	FD	gap
000022B0	00000000 00000000			1501+V1031	DS	XL16	V1 output
000022B8	00000000 00000000						
000022C0	00000000 00000000			1502+	DS	FD	gap
				1503+*			
000022C8				1504+X31	DS	0F	
000022C8	E310 5010 0014		00000010	1505+	LGF	R1,V2ADDR	load v2 source
000022CE	E761 0000 0806		00000000	1506+	VL	v22,0(R1)	use v22 to test decoder
000022D4	E310 5014 0014		00000014	1507+	LGF	R1,V3ADDR	load v3 source
000022DA	E771 0000 0806		00000000	1508+	VL	v23,0(R1)	use v23 to test decoder
000022E0	E766 7000 2EA2			1509+	VML	V22,V22,V23,2	test instruction (dest is a source)
000022E6	E760 5028 080E		000022B0	1510+	VST	V22,V1031	save v1 output
000022EC	07FB			1511+	BR	R11	return
000022F0				1512+RE31	DC	0F	xl16 expected result
000022F0				1513+	DROP	R5	
000022F0	FF0B0A08 4B453420			1514	DC	XL16'FF0B0A084B453420 CFAF7E489449E880'	result
000022F8	CFAF7E48 9449E880						
00002300	FF020304 05060708			1515	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
00002308	090A0B0C 0D0E0F10						
00002310	FF010102 02030304			1516	DC	XL16'FF01010202030304 0405050606070708'	v3
00002318	04050506 06070708						
				1517			
				1518	VRR_C	VML,2	
00002320				1519+	DS	0FD	
00002320		00002320		1520+	USING	*,R5	base for test data and test routine
00002320	00002360			1521+T32	DC	A(X32)	address of test routine
00002324	0020			1522+	DC	H'32'	test number
00002326	00			1523+	DC	X'00'	
00002327	02			1524+	DC	HL1'2'	m4
00002328	E5D4D340 40404040			1525+	DC	CL8'VML'	instruction name
00002330	00002398			1526+	DC	A(RE32+16)	address of v2 source
00002334	000023A8			1527+	DC	A(RE32+32)	address of v3 source
00002338	00000010			1528+	DC	A(16)	result length
0000233C	00002388			1529+REA32	DC	A(RE32)	result address
00002340	00000000 00000000			1530+	DS	FD	gap
00002348	00000000 00000000			1531+V1032	DS	XL16	V1 output
00002350	00000000 00000000						
00002358	00000000 00000000			1532+	DS	FD	gap
				1533+*			
00002360				1534+X32	DS	0F	
00002360	E310 5010 0014		00000010	1535+	LGF	R1,V2ADDR	load v2 source
00002366	E761 0000 0806		00000000	1536+	VL	v22,0(R1)	use v22 to test decoder
0000236C	E310 5014 0014		00000014	1537+	LGF	R1,V3ADDR	load v3 source
00002372	E771 0000 0806		00000000	1538+	VL	v23,0(R1)	use v23 to test decoder
00002378	E766 7000 2EA2			1539+	VML	V22,V22,V23,2	test instruction (dest is a source)
0000237E	E760 5028 080E		00002348	1540+	VST	V22,V1032	save v1 output
00002384	07FB			1541+	BR	R11	return
00002388				1542+RE32	DC	0F	xl16 expected result
00002388				1543+	DROP	R5	
00002388	FC000000 05060708			1544	DC	XL16'FC00000005060708 2A21170C473B2E20'	result
00002390	2A21170C 473B2E20						
00002398	FF020304 05060708			1545	DC	XL16'FF02030405060708 090A0B0C0D0E0F10'	v2
000023A0	090A0B0C 0D0E0F10						
000023A8	FF000000 00000001			1546	DC	XL16'FF00000000000001 0101010101010102'	v3
000023B0	01010101 01010102						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				1547			
				1548	* Doubleword		
				1549		VRR_C VML,3	
000023B8				1550+	DS	0FD	
000023B8		000023B8		1551+	USING *,R5		base for test data and test routine
000023B8	000023F8			1552+T33	DC	A(X33)	address of test routine
000023BC	0021			1553+	DC	H'33'	test number
000023BE	00			1554+	DC	X'00'	
000023BF	03			1555+	DC	HL1'3'	m4
000023C0	E5D4D340 40404040			1556+	DC	CL8'VML'	instruction name
000023C8	00002430			1557+	DC	A(RE33+16)	address of v2 source
000023CC	00002440			1558+	DC	A(RE33+32)	address of v3 source
000023D0	00000010			1559+	DC	A(16)	result length
000023D4	00002420			1560+REA33	DC	A(RE33)	result address
000023D8	00000000 00000000			1561+	DS	FD	gap
000023E0	00000000 00000000			1562+V1033	DS	XL16	V1 output
000023E8	00000000 00000000						
000023F0	00000000 00000000			1563+	DS	FD	gap
				1564+*			
000023F8				1565+X33	DS	0F	
000023F8	E310 5010 0014		00000010	1566+	LGF	R1,V2ADDR	load v2 source
000023FE	E761 0000 0806		00000000	1567+	VL	v22,0(R1)	use v22 to test decoder
00002404	E310 5014 0014		00000014	1568+	LGF	R1,V3ADDR	load v3 source
0000240A	E771 0000 0806		00000000	1569+	VL	v23,0(R1)	use v23 to test decoder
00002410	E766 7000 3EA2			1570+	VML	V22,V22,V23,3	test instruction (dest is a source)
00002416	E760 5028 080E		000023E0	1571+	VST	V22,V1033	save v1 output
0000241C	07FB			1572+	BR	R11	return
00002420				1573+RE33	DC	0F	xl16 expected result
00002420				1574+	DROP	R5	
00002420	FFFCE002 71000000			1575	DC	XL16'FFFCE00271000000 96789F9F4FEDCC24'	result
00002428	96789F9F 4FEDCC24						
00002430	FFFFFFFF 00019000			1576	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00002438	00000038 EEEEEEFA						
00002440	FFFFFFFF 00019000			1577	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00002448	00000038 0EEEEEFA						
				1578			
				1579		VRR_C VML,3	
00002450				1580+	DS	0FD	
00002450		00002450		1581+	USING *,R5		base for test data and test routine
00002450	00002490			1582+T34	DC	A(X34)	address of test routine
00002454	0022			1583+	DC	H'34'	test number
00002456	00			1584+	DC	X'00'	
00002457	03			1585+	DC	HL1'3'	m4
00002458	E5D4D340 40404040			1586+	DC	CL8'VML'	instruction name
00002460	000024C8			1587+	DC	A(RE34+16)	address of v2 source
00002464	000024D8			1588+	DC	A(RE34+32)	address of v3 source
00002468	00000010			1589+	DC	A(16)	result length
0000246C	000024B8			1590+REA34	DC	A(RE34)	result address
00002470	00000000 00000000			1591+	DS	FD	gap
00002478	00000000 00000000			1592+V1034	DS	XL16	V1 output
00002480	00000000 00000000						
00002488	00000000 00000000			1593+	DS	FD	gap
				1594+*			
00002490				1595+X34	DS	0F	
00002490	E310 5010 0014		00000010	1596+	LGF	R1,V2ADDR	load v2 source
00002496	E761 0000 0806		00000000	1597+	VL	v22,0(R1)	use v22 to test decoder

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  LOC          OBJECT CODE      ADDR1    ADDR2    STMT

0000249C  E310 5014 0014           00000014  1598+      LGF    R1,V3ADDR          load v3 source
000024A2  E771 0000 0806           00000000  1599+      VL     v23,0(R1)          use v23 to test decoder
000024A8  E766 7000 3EA2                     1600+      VML    V22,V22,V23,3       test instruction (dest is a source)
000024AE  E760 5028 080E           00002478  1601+      VST    V22,V1034          save v1 output
000024B4  07FB                               1602+      BR     R11                return
000024B8                                     1603+RE34  DC     0F                 xl16 expected result
000024B8                                     1604+      DROP   R5
000024B8  69B556ED 77F57900                  1605       DC     XL16'69B556ED77F57900 152B55D498D42101'   result
000024C0  152B55D4 98D42101
000024C8  FF020304 05060750                  1606       DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000024D0  090A0B0C 0D0E0F7F
000024D8  01020304 05060750                  1607       DC     XL16'0102030405060750 090A0B780D0E0F7F'   v3
000024E0  090A0B78 0D0E0F7F
                                             1608
                                             1609       VRR_C  VML,3
000024E8                                     1610+      DS     0FD
000024E8                         000024E8    1611+      USING  *,R5               base for test data and test routine
000024E8  00002528                           1612+T35   DC     A(X35)             address of test routine
000024EC  0023                               1613+      DC     H'35'              test number
000024EE  00                                 1614+      DC     X'00'
000024EF  03                                 1615+      DC     HL1'3'             m4
000024F0  E5D4D340 40404040                  1616+      DC     CL8'VML'           instruction name
000024F8  00002560                           1617+      DC     A(RE35+16)         address of v2 source
000024FC  00002570                           1618+      DC     A(RE35+32)         address of v3 source
00002500  00000010                           1619+      DC     A(16)              result length
00002504  00002550                           1620+REA35 DC     A(RE35)            result address
00002508  00000000 00000000                  1621+      DS     FD                 gap
00002510  00000000 00000000                  1622+V1035 DS     XL16               V1 output
00002518  00000000 00000000
00002520  00000000 00000000                  1623+      DS     FD                 gap
                                             1624+*
00002528                                     1625+X35   DS     0F
00002528  E310 5010 0014           00000010  1626+      LGF    R1,V2ADDR          load v2 source
0000252E  E761 0000 0806           00000000  1627+      VL     v22,0(R1)          use v22 to test decoder
00002534  E310 5014 0014           00000014  1628+      LGF    R1,V3ADDR          load v3 source
0000253A  E771 0000 0806           00000000  1629+      VL     v23,0(R1)          use v23 to test decoder
00002540  E766 7000 3EA2                     1630+      VML    V22,V22,V23,3       test instruction (dest is a source)
00002546  E760 5028 080E           00002510  1631+      VST    V22,V1035          save v1 output
0000254C  07FB                               1632+      BR     R11                return
00002550                                     1633+RE35  DC     0F                 xl16 expected result
00002550                                     1634+      DROP   R5
00002550  06D2FE70 90F71480                  1635       DC     XL16'06D2FE7090F71480 B47CD8D5FF5B4941'   result
00002558  B47CD8D5 FF5B4941
00002560  FF020304 05060750                  1636       DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002568  090A0B0C 0D0E0F7F
00002570  00010102 02030328                  1637       DC     XL16'0001010202030328 0405053C0607073F'   v3
00002578  0405053C 0607073F
                                             1638
                                             1639       VRR_C  VML,3
00002580                                     1640+      DS     0FD
00002580                         00002580    1641+      USING  *,R5               base for test data and test routine
00002580  000025C0                           1642+T36   DC     A(X36)             address of test routine
00002584  0024                               1643+      DC     H'36'              test number
00002586  00                                 1644+      DC     X'00'
00002587  03                                 1645+      DC     HL1'3'             m4
00002588  E5D4D340 40404040                  1646+      DC     CL8'VML'           instruction name
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002590	000025F8			1647+	DC	A(RE36+16)	address of v2 source
00002594	00002608			1648+	DC	A(RE36+32)	address of v3 source
00002598	00000010			1649+	DC	A(16)	result length
0000259C	000025E8			1650+REA36	DC	A(RE36)	result address
000025A0	00000000 00000000			1651+	DS	FD	gap
000025A8	00000000 00000000			1652+V1036	DS	XL16	V1 output
000025B0	00000000 00000000						
000025B8	00000000 00000000			1653+	DS	FD	gap
				1654+*			
000025C0				1655+X36	DS	0F	
000025C0	E310 5010 0014		00000010	1656+	LGF	R1,V2ADDR	load v2 source
000025C6	E761 0000 0806		00000000	1657+	VL	v22,0(R1)	use v22 to test decoder
000025CC	E310 5014 0014		00000014	1658+	LGF	R1,V3ADDR	load v3 source
000025D2	E771 0000 0806		00000000	1659+	VL	v23,0(R1)	use v23 to test decoder
000025D8	E766 7000 3EA2			1660+	VML	V22,V22,V23,3	test instruction (dest is a source)
000025DE	E760 5028 080E		000025A8	1661+	VST	V22,V1036	save v1 output
000025E4	07FB			1662+	BR	R11	return
000025E8				1663+RE36	DC	0F	xl16 expected result
000025E8				1664+	DROP	R5	
000025E8	F6141E28 323C4920			1665	DC	XL16'F6141E28323C4920 091C345060616771'	result
000025F0	091C3450 60616771						
000025F8	FF020304 05060750			1666	DC	XL16'FF020304050607 50 090A0B0C0D0E0F7F'	v2
00002600	090A0B0C 0D0E0F7F						
00002608	00000000 0000000A			1667	DC	XL16'000000000000000A 0101010F0101010F'	v3
00002610	0101010F 0101010F						
				1668			
				1669	* Quadword		
				1670		VRR_C VML,4	
00002618				1671+	DS	0FD	
00002618		00002618		1672+	USING	*,R5	base for test data and test routine
00002618	00002658			1673+T37	DC	A(X37)	address of test routine
0000261C	0025			1674+	DC	H'37'	test number
0000261E	00			1675+	DC	X'00'	
0000261F	04			1676+	DC	HL1'4'	m4
00002620	E5D4D340 40404040			1677+	DC	CL8'VML'	instruction name
00002628	00002690			1678+	DC	A(RE37+16)	address of v2 source
0000262C	000026A0			1679+	DC	A(RE37+32)	address of v3 source
00002630	00000010			1680+	DC	A(16)	result length
00002634	00002680			1681+REA37	DC	A(RE37)	result address
00002638	00000000 00000000			1682+	DS	FD	gap
00002640	00000000 00000000			1683+V1037	DS	XL16	V1 output
00002648	00000000 00000000						
00002650	00000000 00000000			1684+	DS	FD	gap
				1685+*			
00002658				1686+X37	DS	0F	
00002658	E310 5010 0014		00000010	1687+	LGF	R1,V2ADDR	load v2 source
0000265E	E761 0000 0806		00000000	1688+	VL	v22,0(R1)	use v22 to test decoder
00002664	E310 5014 0014		00000014	1689+	LGF	R1,V3ADDR	load v3 source
0000266A	E771 0000 0806		00000000	1690+	VL	v23,0(R1)	use v23 to test decoder
00002670	E766 7000 4EA2			1691+	VML	V22,V22,V23,4	test instruction (dest is a source)
00002676	E760 5028 080E		00002640	1692+	VST	V22,V1037	save v1 output
0000267C	07FB			1693+	BR	R11	return
00002680				1694+RE37	DC	0F	xl16 expected result
00002680				1695+	DROP	R5	
00002680	02D2AEB6 AACD4C77			1696	DC	XL16'02D2AEB6AACD4C77 96789F9F4FEDCC24'	result
00002688	96789F9F 4FEDCC24						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002690	FFFFFFFF 00019000			1697	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00002698	00000038 EEEEEEFA						
000026A0	FFFFFFFF 00019000			1698	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
000026A8	00000038 0EEEEEFA						
				1699			
				1700	VRR_C VML, 4		
000026B0				1701+	DS	0FD	
000026B0		000026B0		1702+	USING	*,R5	base for test data and test routine
000026B0	000026F0			1703+T38	DC	A(X38)	address of test routine
000026B4	0026			1704+	DC	H'38'	test number
000026B6	00			1705+	DC	X'00'	
000026B7	04			1706+	DC	HL1'4'	m4
000026B8	E5D4D340 40404040			1707+	DC	CL8'VML'	instruction name
000026C0	00002728			1708+	DC	A(RE38+16)	address of v2 source
000026C4	00002738			1709+	DC	A(RE38+32)	address of v3 source
000026C8	00000010			1710+	DC	A(16)	result length
000026CC	00002718			1711+REA38	DC	A(RE38)	result address
000026D0	00000000 00000000			1712+	DS	FD	gap
000026D8	00000000 00000000			1713+V1038	DS	XL16	V1 output
000026E0	00000000 00000000						
000026E8	00000000 00000000			1714+	DS	FD	gap
				1715+*			
000026F0				1716+X38	DS	0F	
000026F0	E310 5010 0014		00000010	1717+	LGF	R1,V2ADDR	load v2 source
000026F6	E761 0000 0806		00000000	1718+	VL	v22,0(R1)	use v22 to test decoder
000026FC	E310 5014 0014		00000014	1719+	LGF	R1,V3ADDR	load v3 source
00002702	E771 0000 0806		00000000	1720+	VL	v23,0(R1)	use v23 to test decoder
00002708	E766 7000 4EA2			1721+	VML	V22,V22,V23,4	test instruction (dest is a source)
0000270E	E760 5028 080E		000026D8	1722+	VST	V22,V1038	save v1 output
00002714	07FB			1723+	BR	R11	return
00002718				1724+RE38	DC	0F	xl16 expected result
00002718				1725+	DROP	R5	
00002718	499AFA6A 24295656			1726	DC	XL16'499AFA6A24295656 152B55D498D42101'	result
00002720	152B55D4 98D42101						
00002728	FF020304 05060750			1727	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00002730	090A0B0C 0D0E0F7F						
00002738	01020304 05060750			1728	DC	XL16'0102030405060750 090A0B780D0E0F7F'	v3
00002740	090A0B78 0D0E0F7F						
				1729			
				1730	VRR_C VML, 4		
00002748				1731+	DS	0FD	
00002748		00002748		1732+	USING	*,R5	base for test data and test routine
00002748	00002788			1733+T39	DC	A(X39)	address of test routine
0000274C	0027			1734+	DC	H'39'	test number
0000274E	00			1735+	DC	X'00'	
0000274F	04			1736+	DC	HL1'4'	m4
00002750	E5D4D340 40404040			1737+	DC	CL8'VML'	instruction name
00002758	000027C0			1738+	DC	A(RE39+16)	address of v2 source
0000275C	000027D0			1739+	DC	A(RE39+32)	address of v3 source
00002760	00000010			1740+	DC	A(16)	result length
00002764	000027B0			1741+REA39	DC	A(RE39)	result address
00002768	00000000 00000000			1742+	DS	FD	gap
00002770	00000000 00000000			1743+V1039	DS	XL16	V1 output
00002778	00000000 00000000						
00002780	00000000 00000000			1744+	DS	FD	gap
				1745+*			

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

 00002788                                         1746+X39      DS     0F
 00002788  E310 5010 0014               00000010  1747+         LGF    R1,V2ADDR          load v2 source
 0000278E  E761 0000 0806               00000000  1748+         VL     v22,0(R1)          use v22 to test decoder
 00002794  E310 5014 0014               00000014  1749+         LGF    R1,V3ADDR          load v3 source
 0000279A  E771 0000 0806               00000000  1750+         VL     v23,0(R1)          use v23 to test decoder
 000027A0  E766 7000 4EA2                         1751+         VML    V22,V22,V23,4       test instruction (dest is a source)
 000027A6  E760 5028 080E               00002770  1752+         VST    V22,V1039           save v1 output
 000027AC  07FB                                   1753+         BR     R11                return
 000027B0                                         1754+RE39     DC     0F                 xl16 expected result
 000027B0                                         1755+         DROP   R5
 000027B0  A5AC7D14 92F5ADEA                      1756          DC     XL16'A5AC7D1492F5ADEA B47CD8D5FF5B4941'      result
 000027B8  B47CD8D5 FF5B4941
 000027C0  FF020304 05060750                      1757          DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'      v2
 000027C8  090A0B0C 0D0E0F7F
 000027D0  00010102 02030328                      1758          DC     XL16'0001010202030328 0405053C0607073F'      v3
 000027D8  0405053C 0607073F
                                                  1759
                                                  1760          VRR_C VML,4
 000027E0                                         1761+         DS     0FD
 000027E0                        000027E0         1762+         USING  *,R5               base for test data and test routine
 000027E0  00002820                               1763+T40      DC     A(X40)             address of test routine
 000027E4  0028                                   1764+         DC     H'40'              test number
 000027E6  00                                     1765+         DC     X'00'
 000027E7  04                                     1766+         DC     HL1'4'             m4
 000027E8  E5D4D340 40404040                      1767+         DC     CL8'VML'           instruction name
 000027F0  00002858                               1768+         DC     A(RE40+16)         address of v2 source
 000027F4  00002868                               1769+         DC     A(RE40+32)         address of v3 source
 000027F8  00000010                               1770+         DC     A(16)              result length
 000027FC  00002848                               1771+REA40    DC     A(RE40)            result address
 00002800  00000000 00000000                      1772+         DS     FD                 gap
 00002808  00000000 00000000                      1773+V1040    DS     XL16               V1 output
 00002810  00000000 00000000
 00002818  00000000 00000000                      1774+         DS     FD                 gap
                                                  1775+*
 00002820                                         1776+X40      DS     0F
 00002820  E310 5010 0014               00000010  1777+         LGF    R1,V2ADDR          load v2 source
 00002826  E761 0000 0806               00000000  1778+         VL     v22,0(R1)          use v22 to test decoder
 0000282C  E310 5014 0014               00000014  1779+         LGF    R1,V3ADDR          load v3 source
 00002832  E771 0000 0806               00000000  1780+         VL     v23,0(R1)          use v23 to test decoder
 00002838  E766 7000 4EA2                         1781+         VML    V22,V22,V23,4       test instruction (dest is a source)
 0000283E  E760 5028 080E               00002808  1782+         VST    V22,V1040           save v1 output
 00002844  07FB                                   1783+         BR     R11                return
 00002848                                         1784+RE40     DC     0F                 xl16 expected result
 00002848                                         1785+         DROP   R5
 00002848  FD497B95 D40238A4                      1786          DC     XL16'FD497B95D40238A4 091C345060616771'      result
 00002850  091C3450 60616771
 00002858  FF020304 05060750                      1787          DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'      v2
 00002860  090A0B0C 0D0E0F7F
 00002868  00000000 0000000A                      1788          DC     XL16'000000000000000A 0101010F0101010F'      v3
 00002870  0101010F 0101010F
                                                  1789
                                                  1790 *-------------------------------------------------------------------
                                                  1791 *  VMH    - Vector Multiply High
                                                  1792 *-------------------------------------------------------------------
                                                  1793 * Byte
                                                  1794          VRR_C VMH,0
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  LOC           OBJECT CODE       ADDR1     ADDR2     STMT

  00002878                                            1795+          DS    0FD
  00002878                        00002878            1796+          USING *,R5              base for test data and test routine
  00002878  000028B8                                  1797+T41       DC    A(X41)            address of test routine
  0000287C  0029                                      1798+          DC    H'41'             test number
  0000287E  00                                        1799+          DC    X'00'
  0000287F  00                                        1800+          DC    HL1'0'            m4
  00002880  E5D4C840 40404040                         1801+          DC    CL8'VMH'          instruction name
  00002888  000028F0                                  1802+          DC    A(RE41+16)        address of v2 source
  0000288C  00002900                                  1803+          DC    A(RE41+32)        address of v3 source
  00002890  00000010                                  1804+          DC    A(16)             result length
  00002894  000028E0                                  1805+REA41     DC    A(RE41)           result address
  00002898  00000000 00000000                         1806+          DS    FD                gap
  000028A0  00000000 00000000                         1807+V1041     DS    XL16              V1 output
  000028A8  00000000 00000000
  000028B0  00000000 00000000                         1808+          DS    FD                gap
                                                      1809+*
  000028B8                                            1810+X41       DS    0F
  000028B8  E310 5010 0014                  00000010  1811+          LGF   R1,V2ADDR         load v2 source
  000028BE  E761 0000 0806                  00000000  1812+          VL    v22,0(R1)         use v22 to test decoder
  000028C4  E310 5014 0014                  00000014  1813+          LGF   R1,V3ADDR         load v3 source
  000028CA  E771 0000 0806                  00000000  1814+          VL    v23,0(R1)         use v23 to test decoder
  000028D0  E766 7000 0EA3                            1815+          VMH   V22,V22,V23,0      test instruction (dest is a source)
  000028D6  E760 5028 080E                  000028A0  1816+          VST   V22,V1041         save v1 output
  000028DC  07FB                                      1817+          BR    R11               return
  000028E0                                            1818+RE41      DC    0F                xl16 expected result
  000028E0                                            1819+          DROP  R5
  000028E0  00000000 00000002                         1820           DC    XL16'0000000000000002 0000000C00000000'     result
  000028E8  0000000C 00000000
  000028F0  FF000000 00000019                         1821           DC    XL16'FF00000000000019 00000038000000FA'     v2
  000028F8  00000038 000000FA
  00002900  FF000000 00000019                         1822           DC    XL16'FF00000000000019 00000038000000FA'     v3
  00002908  00000038 000000FA
                                                      1823
                                                      1824           VRR_C VMH,0
  00002910                                            1825+          DS    0FD
  00002910                        00002910            1826+          USING *,R5              base for test data and test routine
  00002910  00002950                                  1827+T42       DC    A(X42)            address of test routine
  00002914  002A                                      1828+          DC    H'42'             test number
  00002916  00                                        1829+          DC    X'00'
  00002917  00                                        1830+          DC    HL1'0'            m4
  00002918  E5D4C840 40404040                         1831+          DC    CL8'VMH'          instruction name
  00002920  00002988                                  1832+          DC    A(RE42+16)        address of v2 source
  00002924  00002998                                  1833+          DC    A(RE42+32)        address of v3 source
  00002928  00000010                                  1834+          DC    A(16)             result length
  0000292C  00002978                                  1835+REA42     DC    A(RE42)           result address
  00002930  00000000 00000000                         1836+          DS    FD                gap
  00002938  00000000 00000000                         1837+V1042     DS    XL16              V1 output
  00002940  00000000 00000000
  00002948  00000000 00000000                         1838+          DS    FD                gap
                                                      1839+*
  00002950                                            1840+X42       DS    0F
  00002950  E310 5010 0014                  00000010  1841+          LGF   R1,V2ADDR         load v2 source
  00002956  E761 0000 0806                  00000000  1842+          VL    v22,0(R1)         use v22 to test decoder
  0000295C  E310 5014 0014                  00000014  1843+          LGF   R1,V3ADDR         load v3 source
  00002962  E771 0000 0806                  00000000  1844+          VL    v23,0(R1)         use v23 to test decoder
  00002968  E766 7000 0EA3                            1845+          VMH   V22,V22,V23,0      test instruction (dest is a source)
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  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

0000296E  E760 5028 080E              00002938  1846+        VST    V22,V1042       save v1 output
00002974  07FB                                  1847+        BR     R11             return
00002978                                        1848+RE42    DC     0F              xl16 expected result
00002978                                        1849+        DROP   R5
00002978  FF000000 00000019                     1850         DC     XL16'FF00000000000019 000000050000003F'   result
00002980  00000005 0000003F
00002988  FF020304 05060750                     1851         DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00002990  090A0B0C 0D0E0F7F
00002998  01020304 05060750                     1852         DC     XL16'0102030405060750 090A0B780D0E0F7F'    v3
000029A0  090A0B78 0D0E0F7F
                                                1853
                                                1854         VRR_C  VMH,0
000029A8                                        1855+        DS     0FD
000029A8                            000029A8    1856+        USING  *,R5            base for test data and test routine
000029A8  000029E8                              1857+T43     DC     A(X43)          address of test routine
000029AC  002B                                  1858+        DC     H'43'           test number
000029AE  00                                    1859+        DC     X'00'
000029AF  00                                    1860+        DC     HL1'0'          m4
000029B0  E5D4C840 40404040                     1861+        DC     CL8'VMH'        instruction name
000029B8  00002A20                              1862+        DC     A(RE43+16)      address of v2 source
000029BC  00002A30                              1863+        DC     A(RE43+32)      address of v3 source
000029C0  00000010                              1864+        DC     A(16)           result length
000029C4  00002A10                              1865+REA43   DC     A(RE43)         result address
000029C8  00000000 00000000                     1866+        DS     FD              gap
000029D0  00000000 00000000                     1867+V1043   DS     XL16            V1 output
000029D8  00000000 00000000
000029E0  00000000 00000000                     1868+        DS     FD              gap
                                                1869+*
000029E8                                        1870+X43     DS     0F
000029E8  E310 5010 0014              00000010  1871+        LGF    R1,V2ADDR       load v2 source
000029EE  E761 0000 0806              00000000  1872+        VL     v22,0(R1)       use v22 to test decoder
000029F4  E310 5014 0014              00000014  1873+        LGF    R1,V3ADDR       load v3 source
000029FA  E771 0000 0806              00000000  1874+        VL     v23,0(R1)       use v23 to test decoder
00002A00  E766 7000 0EA3                        1875+        VMH    V22,V22,V23,0    test instruction (dest is a source)
00002A06  E760 5028 080E              000029D0  1876+        VST    V22,V1043        save v1 output
00002A0C  07FB                                  1877+        BR     R11             return
00002A10                                        1878+RE43    DC     0F              xl16 expected result
00002A10                                        1879+        DROP   R5
00002A10  00000000 0000000C                     1880         DC     XL16'000000000000000C 000000020000001F'    result
00002A18  00000002 0000001F
00002A20  FF020304 05060750                     1881         DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00002A28  090A0B0C 0D0E0F7F
00002A30  00010102 02030328                     1882         DC     XL16'0001010202030328 0405053C0607073F'    v3
00002A38  0405053C 0607073F
                                                1883
                                                1884         VRR_C  VMH,0
00002A40                                        1885+        DS     0FD
00002A40                            00002A40    1886+        USING  *,R5            base for test data and test routine
00002A40  00002A80                              1887+T44     DC     A(X44)          address of test routine
00002A44  002C                                  1888+        DC     H'44'           test number
00002A46  00                                    1889+        DC     X'00'
00002A47  00                                    1890+        DC     HL1'0'          m4
00002A48  E5D4C840 40404040                     1891+        DC     CL8'VMH'        instruction name
00002A50  00002AB8                              1892+        DC     A(RE44+16)      address of v2 source
00002A54  00002AC8                              1893+        DC     A(RE44+32)      address of v3 source
00002A58  00000010                              1894+        DC     A(16)           result length
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002A5C	00002AA8			1895+REA44	DC	A(RE44)	result address
00002A60	00000000 00000000			1896+	DS	FD	gap
00002A68	00000000 00000000			1897+V1044	DS	XL16	V1 output
00002A70	00000000 00000000						
00002A78	00000000 00000000			1898+	DS	FD	gap
				1899+*			
00002A80				1900+X44	DS	0F	
00002A80	E310 5010 0014		00000010	1901+	LGF	R1,V2ADDR	load v2 source
00002A86	E761 0000 0806		00000000	1902+	VL	v22,0(R1)	use v22 to test decoder
00002A8C	E310 5014 0014		00000014	1903+	LGF	R1,V3ADDR	load v3 source
00002A92	E771 0000 0806		00000000	1904+	VL	v23,0(R1)	use v23 to test decoder
00002A98	E766 7000 0EA3			1905+	VMH	V22,V22,V23,0	test instruction (dest is a source)
00002A9E	E760 5028 080E		00002A68	1906+	VST	V22,V1044	save v1 output
00002AA4	07FB			1907+	BR	R11	return
00002AA8				1908+RE44	DC	0F	xl16 expected result
00002AA8				1909+	DROP	R5	
00002AA8	00000000 00000003			1910	DC	XL16'0000000000000003 0000000000000007'	result
00002AB0	00000000 00000007						
00002AB8	FF020304 05060750			1911	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00002AC0	090A0B0C 0D0E0F7F						
00002AC8	00000000 0000000A			1912	DC	XL16'000000000000000A 0101010F0101010F'	v3
00002AD0	0101010F 0101010F						
				1913			
				1914	* Halfword		
				1915	VRR_C	VMH,1	
00002AD8				1916+	DS	0FD	
00002AD8		00002AD8		1917+	USING	*,R5	base for test data and test routine
00002AD8	00002B18			1918+T45	DC	A(X45)	address of test routine
00002ADC	002D			1919+	DC	H'45'	test number
00002ADE	00			1920+	DC	X'00'	
00002ADF	01			1921+	DC	HL1'1'	m4
00002AE0	E5D4C840 40404040			1922+	DC	CL8'VMH'	instruction name
00002AE8	00002B50			1923+	DC	A(RE45+16)	address of v2 source
00002AEC	00002B60			1924+	DC	A(RE45+32)	address of v3 source
00002AF0	00000010			1925+	DC	A(16)	result length
00002AF4	00002B40			1926+REA45	DC	A(RE45)	result address
00002AF8	00000000 00000000			1927+	DS	FD	gap
00002B00	00000000 00000000			1928+V1045	DS	XL16	V1 output
00002B08	00000000 00000000						
00002B10	00000000 00000000			1929+	DS	FD	gap
				1930+*			
00002B18				1931+X45	DS	0F	
00002B18	E310 5010 0014		00000010	1932+	LGF	R1,V2ADDR	load v2 source
00002B1E	E761 0000 0806		00000000	1933+	VL	v22,0(R1)	use v22 to test decoder
00002B24	E310 5014 0014		00000014	1934+	LGF	R1,V3ADDR	load v3 source
00002B2A	E771 0000 0806		00000000	1935+	VL	v23,0(R1)	use v23 to test decoder
00002B30	E766 7000 1EA3			1936+	VMH	V22,V22,V23,1	test instruction (dest is a source)
00002B36	E760 5028 080E		00002B00	1937+	VST	V22,V1045	save v1 output
00002B3C	07FB			1938+	BR	R11	return
00002B40				1939+RE45	DC	0F	xl16 expected result
00002B40				1940+	DROP	R5	
00002B40	00000000 00000000			1941	DC	XL16'0000000000000000 0000000000000121'	result
00002B48	00000000 00000121						
00002B50	FFFF0000 00000019			1942	DC	XL16'FFFF000000000019 000000380000EEFA'	v2
00002B58	00000038 0000EEFA						
00002B60	FFFF0000 00000019			1943	DC	XL16'FFFF000000000019 000000380000EEFA'	v3

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002B68	00000038 0000EEFA						
				1944			
				1945	VRR_C	VMH, 1	
00002B70				1946+	DS	0FD	
00002B70		00002B70		1947+	USING	*, R5	base for test data and test routine
00002B70	00002BB0			1948+T46	DC	A(X46)	address of test routine
00002B74	002E			1949+	DC	H'46'	test number
00002B76	00			1950+	DC	X'00'	
00002B77	01			1951+	DC	HL1'1'	m4
00002B78	E5D4C840 40404040			1952+	DC	CL8'VMH'	instruction name
00002B80	00002BE8			1953+	DC	A(RE46+16)	address of v2 source
00002B84	00002BF8			1954+	DC	A(RE46+32)	address of v3 source
00002B88	00000010			1955+	DC	A(16)	result length
00002B8C	00002BD8			1956+REA46	DC	A(RE46)	result address
00002B90	00000000 00000000			1957+	DS	FD	gap
00002B98	00000000 00000000			1958+V1046	DS	XL16	V1 output
00002BA0	00000000 00000000						
00002BA8	00000000 00000000			1959+	DS	FD	gap
				1960+*			
00002BB0				1961+X46	DS	0F	
00002BB0	E310 5010 0014		00000010	1962+	LGF	R1, V2ADDR	load v2 source
00002BB6	E761 0000 0806		00000000	1963+	VL	v22, 0(R1)	use v22 to test decoder
00002BBC	E310 5014 0014		00000014	1964+	LGF	R1, V3ADDR	load v3 source
00002BC2	E771 0000 0806		00000000	1965+	VL	v23, 0(R1)	use v23 to test decoder
00002BC8	E766 7000 1EA3			1966+	VMH	V22, V22, V23, 1	test instruction (dest is a source)
00002BCE	E760 5028 080E		00002B98	1967+	VST	V22, V1046	save v1 output
00002BD4	07FB			1968+	BR	R11	return
00002BD8				1969+RE46	DC	0F	xl16 expected result
00002BD8				1970+	DROP	R5	
00002BD8	FFFF0009 00190035			1971	DC	XL16'FFFF000900190035 0051007E00AA00F0'	result
00002BE0	0051007E 00AA00F0						
00002BE8	FF020304 05060750			1972	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00002BF0	090A0B0C 0D0E0F7F						
00002BF8	01020304 05060750			1973	DC	XL16'0102030405060750 090A0B780D0E0F7F'	v3
00002C00	090A0B78 0D0E0F7F						
				1974			
				1975	VRR_C	VMH, 1	
00002C08				1976+	DS	0FD	
00002C08		00002C08		1977+	USING	*, R5	base for test data and test routine
00002C08	00002C48			1978+T47	DC	A(X47)	address of test routine
00002C0C	002F			1979+	DC	H'47'	test number
00002C0E	00			1980+	DC	X'00'	
00002C0F	01			1981+	DC	HL1'1'	m4
00002C10	E5D4C840 40404040			1982+	DC	CL8'VMH'	instruction name
00002C18	00002C80			1983+	DC	A(RE47+16)	address of v2 source
00002C1C	00002C90			1984+	DC	A(RE47+32)	address of v3 source
00002C20	00000010			1985+	DC	A(16)	result length
00002C24	00002C70			1986+REA47	DC	A(RE47)	result address
00002C28	00000000 00000000			1987+	DS	FD	gap
00002C30	00000000 00000000			1988+V1047	DS	XL16	V1 output
00002C38	00000000 00000000						
00002C40	00000000 00000000			1989+	DS	FD	gap
				1990+*			
00002C48				1991+X47	DS	0F	
00002C48	E310 5010 0014		00000010	1992+	LGF	R1, V2ADDR	load v2 source
00002C4E	E761 0000 0806		00000000	1993+	VL	v22, 0(R1)	use v22 to test decoder

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  LOC           OBJECT CODE      ADDR1     ADDR2     STMT

00002C54  E310 5014 0014                   00000014  1994+        LGF    R1,V3ADDR          load v3 source
00002C5A  E771 0000 0806                   00000000  1995+        VL     v23,0(R1)          use v23 to test decoder
00002C60  E766 7000 1EA3                             1996+        VMH    V22,V22,V23,1       test instruction (dest is a source)
00002C66  E760 5028 080E                   00002C30  1997+        VST    V22,V1047           save v1 output
00002C6C  07FB                                       1998+        BR     R11                return
00002C70                                             1999+RE47    DC     0F                 xl16 expected result
00002C70                                             2000+        DROP   R5
00002C70  FFFF0003 000A0017                          2001         DC     XL16'FFFF0003000A0017 00240039004E0070'   result
00002C78  00240039 004E0070
00002C80  FF020304 05060750                          2002         DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002C88  090A0B0C 0D0E0F7F
00002C90  00010102 02030328                          2003         DC     XL16'0001010202030328 0405053C0607073F'   v3
00002C98  0405053C 0607073F
                                                     2004
                                                     2005         VRR_C VMH,1
00002CA0                                             2006+        DS     0FD
00002CA0                            00002CA0         2007+        USING  *,R5               base for test data and test routine
00002CA0  00002CE0                                   2008+T48     DC     A(X48)             address of test routine
00002CA4  0030                                       2009+        DC     H'48'              test number
00002CA6  00                                         2010+        DC     X'00'
00002CA7  01                                         2011+        DC     HL1'1'             m4
00002CA8  E5D4C840 40404040                          2012+        DC     CL8'VMH'           instruction name
00002CB0  00002D18                                   2013+        DC     A(RE48+16)         address of v2 source
00002CB4  00002D28                                   2014+        DC     A(RE48+32)         address of v3 source
00002CB8  00000010                                   2015+        DC     A(16)              result length
00002CBC  00002D08                                   2016+REA48   DC     A(RE48)            result address
00002CC0  00000000 00000000                          2017+        DS     FD                 gap
00002CC8  00000000 00000000                          2018+V1048   DS     XL16               V1 output
00002CD0  00000000 00000000
00002CD8  00000000 00000000                          2019+        DS     FD                 gap
                                                     2020+*
00002CE0                                             2021+X48     DS     0F
00002CE0  E310 5010 0014                   00000010  2022+        LGF    R1,V2ADDR          load v2 source
00002CE6  E761 0000 0806                   00000000  2023+        VL     v22,0(R1)          use v22 to test decoder
00002CEC  E310 5014 0014                   00000014  2024+        LGF    R1,V3ADDR          load v3 source
00002CF2  E771 0000 0806                   00000000  2025+        VL     v23,0(R1)          use v23 to test decoder
00002CF8  E766 7000 1EA3                             2026+        VMH    V22,V22,V23,1       test instruction (dest is a source)
00002CFE  E760 5028 080E                   00002CC8  2027+        VST    V22,V1048           save v1 output
00002D04  07FB                                       2028+        BR     R11                return
00002D08                                             2029+RE48    DC     0F                 xl16 expected result
00002D08                                             2030+        DROP   R5
00002D08  00000000 00000000                          2031         DC     XL16'0000000000000000 0009000B000D0010'   result
00002D10  0009000B 000D0010
00002D18  FF020304 05060750                          2032         DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002D20  090A0B0C 0D0E0F7F
00002D28  00000000 0000000A                          2033         DC     XL16'000000000000000A 0101010F0101010F'   v3
00002D30  0101010F 0101010F
                                                     2034
                                                     2035 * Word
                                                     2036         VRR_C VMH,2
00002D38                                             2037+        DS     0FD
00002D38                            00002D38         2038+        USING  *,R5               base for test data and test routine
00002D38  00002D78                                   2039+T49     DC     A(X49)             address of test routine
00002D3C  0031                                       2040+        DC     H'49'              test number
00002D3E  00                                         2041+        DC     X'00'
00002D3F  02                                         2042+        DC     HL1'2'             m4
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002D40	E5D4C840 40404040			2043+	DC	CL8'VMH'	instruction name
00002D48	00002DB0			2044+	DC	A(RE49+16)	address of v2 source
00002D4C	00002DC0			2045+	DC	A(RE49+32)	address of v3 source
00002D50	00000010			2046+	DC	A(16)	result length
00002D54	00002DA0			2047+REA49	DC	A(RE49)	result address
00002D58	00000000 00000000			2048+	DS	FD	gap
00002D60	00000000 00000000			2049+V1049	DS	XL16	V1 output
00002D68	00000000 00000000						
00002D70	00000000 00000000			2050+	DS	FD	gap
				2051+*			
00002D78				2052+X49	DS	0F	
00002D78	E310 5010 0014		00000010	2053+	LGF	R1,V2ADDR	load v2 source
00002D7E	E761 0000 0806		00000000	2054+	VL	v22,0(R1)	use v22 to test decoder
00002D84	E310 5014 0014		00000014	2055+	LGF	R1,V3ADDR	load v3 source
00002D8A	E771 0000 0806		00000000	2056+	VL	v23,0(R1)	use v23 to test decoder
00002D90	E766 7000 2EA3			2057+	VMH	V22,V22,V23,2	test instruction (dest is a source)
00002D96	E760 5028 080E		00002D60	2058+	VST	V22,V1049	save v1 output
00002D9C	07FB			2059+	BR	R11	return
00002DA0				2060+RE49	DC	0F	xl16 expected result
00002DA0				2061+	DROP	R5	
00002DA0	00000000 00000002			2062	DC	XL16'0000000000000002 00000000FF012345'	result
00002DA8	00000000 FF012345						
00002DB0	FFFFFFFF 00019000			2063	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00002DB8	00000038 EEEEEEFA						
00002DC0	FFFFFFFF 00019000			2064	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00002DC8	00000038 0EEEEEFA						
				2065			
				2066	VRR_C	VMH,2	
00002DD0				2067+	DS	0FD	
00002DD0		00002DD0		2068+	USING	*,R5	base for test data and test routine
00002DD0	00002E10			2069+T50	DC	A(X50)	address of test routine
00002DD4	0032			2070+	DC	H'50'	test number
00002DD6	00			2071+	DC	X'00'	
00002DD7	02			2072+	DC	HL1'2'	m4
00002DD8	E5D4C840 40404040			2073+	DC	CL8'VMH'	instruction name
00002DE0	00002E48			2074+	DC	A(RE50+16)	address of v2 source
00002DE4	00002E58			2075+	DC	A(RE50+32)	address of v3 source
00002DE8	00000010			2076+	DC	A(16)	result length
00002DEC	00002E38			2077+REA50	DC	A(RE50)	result address
00002DF0	00000000 00000000			2078+	DS	FD	gap
00002DF8	00000000 00000000			2079+V1050	DS	XL16	V1 output
00002E00	00000000 00000000						
00002E08	00000000 00000000			2080+	DS	FD	gap
				2081+*			
00002E10				2082+X50	DS	0F	
00002E10	E310 5010 0014		00000010	2083+	LGF	R1,V2ADDR	load v2 source
00002E16	E761 0000 0806		00000000	2084+	VL	v22,0(R1)	use v22 to test decoder
00002E1C	E310 5014 0014		00000014	2085+	LGF	R1,V3ADDR	load v3 source
00002E22	E771 0000 0806		00000000	2086+	VL	v23,0(R1)	use v23 to test decoder
00002E28	E766 7000 2EA3			2087+	VMH	V22,V22,V23,2	test instruction (dest is a source)
00002E2E	E760 5028 080E		00002DF8	2088+	VST	V22,V1050	save v1 output
00002E34	07FB			2089+	BR	R11	return
00002E38				2090+RE50	DC	0F	xl16 expected result
00002E38				2091+	DROP	R5	
00002E38	FFFF0004 00193C6D			2092	DC	XL16'FFFF000400193C6D 0051B52F00AA6E58'	result
00002E40	0051B52F 00AA6E58						

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  LOC          OBJECT CODE        ADDR1     ADDR2     STMT

00002E48   FF020304 05060750                          2093         DC      XL16'FF02030405060750 090A0B0C0D0E0F7F'     v2
00002E50   090A0B0C 0D0E0F7F
00002E58   01020304 05060750                          2094         DC      XL16'0102030405060750 090A0B780D0E0F7F'     v3
00002E60   090A0B78 0D0E0F7F
                                                      2095
                                                      2096         VRR_C VMH,2
00002E68                                              2097+        DS      0FD
00002E68                          00002E68            2098+        USING *,R5                  base for test data and test routine
00002E68   00002EA8                                   2099+T51     DC      A(X51)              address of test routine
00002E6C   0033                                       2100+        DC      H'51'               test number
00002E6E   00                                         2101+        DC      X'00'
00002E6F   02                                         2102+        DC      HL1'2'              m4
00002E70   E5D4C840 40404040                          2103+        DC      CL8'VMH'            instruction name
00002E78   00002EE0                                   2104+        DC      A(RE51+16)          address of v2 source
00002E7C   00002EF0                                   2105+        DC      A(RE51+32)          address of v3 source
00002E80   00000010                                   2106+        DC      A(16)               result length
00002E84   00002ED0                                   2107+REA51   DC      A(RE51)             result address
00002E88   00000000 00000000                          2108+        DS      FD                  gap
00002E90   00000000 00000000                          2109+V1051   DS      XL16                V1 output
00002E98   00000000 00000000
00002EA0   00000000 00000000                          2110+        DS      FD                  gap
                                                      2111+*
00002EA8                                              2112+X51     DS      0F
00002EA8   E310 5010 0014                 00000010    2113+        LGF     R1,V2ADDR           load v2 source
00002EAE   E761 0000 0806                 00000000    2114+        VL      v22,0(R1)           use v22 to test decoder
00002EB4   E310 5014 0014                 00000014    2115+        LGF     R1,V3ADDR           load v3 source
00002EBA   E771 0000 0806                 00000000    2116+        VL      v23,0(R1)           use v23 to test decoder
00002EC0   E766 7000 2EA3                             2117+        VMH     V22,V22,V23,2        test instruction (dest is a source)
00002EC6   E760 5028 080E                 00002E90    2118+        VST     V22,V1051            save v1 output
00002ECC   07FB                                       2119+        BR      R11                 return
00002ED0                                              2120+RE51    DC      0F                  xl16 expected result
00002ED0                                              2121+        DROP    R5
00002ED0   FFFFFF01 000A1B30                          2122         DC      XL16'FFFFFF01000A1B30 0024558D004EB01D'     result
00002ED8   0024558D 004EB01D
00002EE0   FF020304 05060750                          2123         DC      XL16'FF02030405060750 090A0B0C0D0E0F7F'     v2
00002EE8   090A0B0C 0D0E0F7F
00002EF0   00010102 02030328                          2124         DC      XL16'0001010202030328 0405053C0607073F'     v3
00002EF8   0405053C 0607073F
                                                      2125
                                                      2126         VRR_C VMH,2
00002F00                                              2127+        DS      0FD
00002F00                          00002F00            2128+        USING *,R5                  base for test data and test routine
00002F00   00002F40                                   2129+T52     DC      A(X52)              address of test routine
00002F04   0034                                       2130+        DC      H'52'               test number
00002F06   00                                         2131+        DC      X'00'
00002F07   02                                         2132+        DC      HL1'2'              m4
00002F08   E5D4C840 40404040                          2133+        DC      CL8'VMH'            instruction name
00002F10   00002F78                                   2134+        DC      A(RE52+16)          address of v2 source
00002F14   00002F88                                   2135+        DC      A(RE52+32)          address of v3 source
00002F18   00000010                                   2136+        DC      A(16)               result length
00002F1C   00002F68                                   2137+REA52   DC      A(RE52)             result address
00002F20   00000000 00000000                          2138+        DS      FD                  gap
00002F28   00000000 00000000                          2139+V1052   DS      XL16                V1 output
00002F30   00000000 00000000
00002F38   00000000 00000000                          2140+        DS      FD                  gap
                                                      2141+*
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002F40				2142+X52	DS	0F	
00002F40	E310 5010 0014		00000010	2143+	LGF	R1,V2ADDR	load v2 source
00002F46	E761 0000 0806		00000000	2144+	VL	v22,0(R1)	use v22 to test decoder
00002F4C	E310 5014 0014		00000014	2145+	LGF	R1,V3ADDR	load v3 source
00002F52	E771 0000 0806		00000000	2146+	VL	v23,0(R1)	use v23 to test decoder
00002F58	E766 7000 2EA3			2147+	VMH	V22,V22,V23,2	test instruction (dest is a source)
00002F5E	E760 5028 080E		00002F28	2148+	VST	V22,V1052	save v1 output
00002F64	07FB			2149+	BR	R11	return
00002F68				2150+RE52	DC	0F	xl16 expected result
00002F68				2151+	DROP	R5	
00002F68	00000000 00000000			2152	DC	XL16'0000000000000000 0009131E000D1B2B'	result
00002F70	0009131E 000D1B2B						
00002F78	FF020304 05060750			2153	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00002F80	090A0B0C 0D0E0F7F						
00002F88	00000000 0000000A			2154	DC	XL16'000000000000000A 0101010F0101010F'	v3
00002F90	0101010F 0101010F						
				2155			
				2156	* Doubleword		
				2157	VRR_C	VMH,3	
00002F98				2158+	DS	0FD	
00002F98		00002F98		2159+	USING	*,R5	base for test data and test routine
00002F98	00002FD8			2160+T53	DC	A(X53)	address of test routine
00002F9C	0035			2161+	DC	H'53'	test number
00002F9E	00			2162+	DC	X'00'	
00002F9F	03			2163+	DC	HL1'3'	m4
00002FA0	E5D4C840 40404040			2164+	DC	CL8'VMH'	instruction name
00002FA8	00003010			2165+	DC	A(RE53+16)	address of v2 source
00002FAC	00003020			2166+	DC	A(RE53+32)	address of v3 source
00002FB0	00000010			2167+	DC	A(16)	result length
00002FB4	00003000			2168+REA53	DC	A(RE53)	result address
00002FB8	00000000 00000000			2169+	DS	FD	gap
00002FC0	00000000 00000000			2170+V1053	DS	XL16	V1 output
00002FC8	00000000 00000000						
00002FD0	00000000 00000000			2171+	DS	FD	gap
				2172+*			
00002FD8				2173+X53	DS	0F	
00002FD8	E310 5010 0014		00000010	2174+	LGF	R1,V2ADDR	load v2 source
00002FDE	E761 0000 0806		00000000	2175+	VL	v22,0(R1)	use v22 to test decoder
00002FE4	E310 5014 0014		00000014	2176+	LGF	R1,V3ADDR	load v3 source
00002FEA	E771 0000 0806		00000000	2177+	VL	v23,0(R1)	use v23 to test decoder
00002FF0	E766 7000 3EA3			2178+	VMH	V22,V22,V23,3	test instruction (dest is a source)
00002FF6	E760 5028 080E		00002FC0	2179+	VST	V22,V1053	save v1 output
00002FFC	07FB			2180+	BR	R11	return
00003000				2181+RE53	DC	0F	xl16 expected result
00003000				2182+	DROP	R5	
00003000	00000000 00000000			2183	DC	XL16'0000000000000000 0000000000000C77'	result
00003008	00000000 00000C77						
00003010	FFFFFFFF 00019000			2184	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00003018	00000038 EEEEEEFA						
00003020	FFFFFFFF 00019000			2185	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00003028	00000038 0EEEEEFA						
				2186			
				2187	VRR_C	VMH,3	
00003030				2188+	DS	0FD	
00003030		00003030		2189+	USING	*,R5	base for test data and test routine
00003030	00003070			2190+T54	DC	A(X54)	address of test routine

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   LOC        OBJECT CODE      ADDR1      ADDR2     STMT

00003034   0036                                    2191+       DC     H'54'                test number
00003036   00                                      2192+       DC     X'00'
00003037   03                                      2193+       DC     HL1'3'               m4
00003038   E5D4C840 40404040                        2194+       DC     CL8'VMH'             instruction name
00003040   000030A8                                2195+       DC     A(RE54+16)           address of v2 source
00003044   000030B8                                2196+       DC     A(RE54+32)           address of v3 source
00003048   00000010                                2197+       DC     A(16)                result length
0000304C   00003098                                2198+REA54   DC     A(RE54)              result address
00003050   00000000 00000000                        2199+       DS     FD                   gap
00003058   00000000 00000000                        2200+V1054  DS     XL16                 V1 output
00003060   00000000 00000000
00003068   00000000 00000000                        2201+       DS     FD                   gap
                                                    2202+*
00003070                                            2203+X54    DS     0F
00003070   E310 5010 0014              00000010     2204+       LGF    R1,V2ADDR            load v2 source
00003076   E761 0000 0806              00000000     2205+       VL     v22,0(R1)            use v22 to test decoder
0000307C   E310 5014 0014              00000014     2206+       LGF    R1,V3ADDR            load v3 source
00003082   E771 0000 0806              00000000     2207+       VL     v23,0(R1)            use v23 to test decoder
00003088   E766 7000 3EA3                            2208+       VMH    V22,V22,V23,3         test instruction (dest is a source)
0000308E   E760 5028 080E              00003058     2209+       VST    V22,V1054             save v1 output
00003094   07FB                                     2210+       BR     R11                  return
00003098                                            2211+RE54   DC     0F                   xl16 expected result
00003098                                            2212+       DROP   R5
00003098   FFFF0004 0C192C46                        2213        DC     XL16'FFFF00040C192C46 0051B52F8692B4F6'    result
000030A0   0051B52F 8692B4F6
000030A8   FF020304 05060750                        2214        DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
000030B0   090A0B0C 0D0E0F7F
000030B8   01020304 05060750                        2215        DC     XL16'0102030405060750 090A0B780D0E0F7F'    v3
000030C0   090A0B78 0D0E0F7F
                                                    2216
                                                    2217        VRR_C  VMH,3
000030C8                                            2218+       DS     0FD
000030C8                           000030C8         2219+       USING  *,R5                 base for test data and test routine
000030C8   00003108                                2220+T55     DC     A(X55)               address of test routine
000030CC   0037                                     2221+       DC     H'55'                test number
000030CE   00                                       2222+       DC     X'00'
000030CF   03                                       2223+       DC     HL1'3'               m4
000030D0   E5D4C840 40404040                        2224+       DC     CL8'VMH'             instruction name
000030D8   00003140                                2225+       DC     A(RE55+16)           address of v2 source
000030DC   00003150                                2226+       DC     A(RE55+32)           address of v3 source
000030E0   00000010                                2227+       DC     A(16)                result length
000030E4   00003130                                2228+REA55   DC     A(RE55)              result address
000030E8   00000000 00000000                        2229+       DS     FD                   gap
000030F0   00000000 00000000                        2230+V1055  DS     XL16                 V1 output
000030F8   00000000 00000000
00003100   00000000 00000000                        2231+       DS     FD                   gap
                                                    2232+*
00003108                                            2233+X55    DS     0F
00003108   E310 5010 0014              00000010     2234+       LGF    R1,V2ADDR            load v2 source
0000310E   E761 0000 0806              00000000     2235+       VL     v22,0(R1)            use v22 to test decoder
00003114   E310 5014 0014              00000014     2236+       LGF    R1,V3ADDR            load v3 source
0000311A   E771 0000 0806              00000000     2237+       VL     v23,0(R1)            use v23 to test decoder
00003120   E766 7000 3EA3                            2238+       VMH    V22,V22,V23,3         test instruction (dest is a source)
00003126   E760 5028 080E              000030F0     2239+       VST    V22,V1055             save v1 output
0000312C   07FB                                     2240+       BR     R11                  return
00003130                                            2241+RE55   DC     0F                   xl16 expected result
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003130				2242+	DROP	R5	
00003130	FFFFFF01 0309101C			2243	DC	XL16'FFFFFF010309101C 0024558DB838C862'	result
00003138	0024558D B838C862						
00003140	FF020304 05060750			2244	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00003148	090A0B0C 0D0E0F7F						
00003150	00010102 02030328			2245	DC	XL16'0001010202030328 0405053C0607073F'	v3
00003158	0405053C 0607073F						
				2246			
				2247	VRR_C	VMH,3	
00003160				2248+	DS	0FD	
00003160		00003160		2249+	USING	*,R5	base for test data and test routine
00003160	000031A0			2250+T56	DC	A(X56)	address of test routine
00003164	0038			2251+	DC	H'56'	test number
00003166	00			2252+	DC	X'00'	
00003167	03			2253+	DC	HL1'3'	m4
00003168	E5D4C840 40404040			2254+	DC	CL8'VMH'	instruction name
00003170	000031D8			2255+	DC	A(RE56+16)	address of v2 source
00003174	000031E8			2256+	DC	A(RE56+32)	address of v3 source
00003178	00000010			2257+	DC	A(16)	result length
0000317C	000031C8			2258+REA56	DC	A(RE56)	result address
00003180	00000000 00000000			2259+	DS	FD	gap
00003188	00000000 00000000			2260+V1056	DS	XL16	V1 output
00003190	00000000 00000000						
00003198	00000000 00000000			2261+	DS	FD	gap
				2262+*			
000031A0				2263+X56	DS	0F	
000031A0	E310 5010 0014		00000010	2264+	LGF	R1,V2ADDR	load v2 source
000031A6	E761 0000 0806		00000000	2265+	VL	v22,0(R1)	use v22 to test decoder
000031AC	E310 5014 0014		00000014	2266+	LGF	R1,V3ADDR	load v3 source
000031B2	E771 0000 0806		00000000	2267+	VL	v23,0(R1)	use v23 to test decoder
000031B8	E766 7000 3EA3			2268+	VMH	V22,V22,V23,3	test instruction (dest is a source)
000031BE	E760 5028 080E		00003188	2269+	VST	V22,V1056	save v1 output
000031C4	07FB			2270+	BR	R11	return
000031C8				2271+RE56	DC	0F	xl16 expected result
000031C8				2272+	DROP	R5	
000031C8	FFFFFFFF FFFFFFFF			2273	DC	XL16'FFFFFFFFFFFFFFFF 0009131EA8C3DFFE'	result
000031D0	0009131E A8C3DFFE						
000031D8	FF020304 05060750			2274	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
000031E0	090A0B0C 0D0E0F7F						
000031E8	00000000 0000000A			2275	DC	XL16'000000000000000A 0101010F0101010F'	v3
000031F0	0101010F 0101010F						
				2276			
				2277	* Quadword		
				2278	VRR_C	VMH,4	
000031F8				2279+	DS	0FD	
000031F8		000031F8		2280+	USING	*,R5	base for test data and test routine
000031F8	00003238			2281+T57	DC	A(X57)	address of test routine
000031FC	0039			2282+	DC	H'57'	test number
000031FE	00			2283+	DC	X'00'	
000031FF	04			2284+	DC	HL1'4'	m4
00003200	E5D4C840 40404040			2285+	DC	CL8'VMH'	instruction name
00003208	00003270			2286+	DC	A(RE57+16)	address of v2 source
0000320C	00003280			2287+	DC	A(RE57+32)	address of v3 source
00003210	00000010			2288+	DC	A(16)	result length
00003214	00003260			2289+REA57	DC	A(RE57)	result address
00003218	00000000 00000000			2290+	DS	FD	gap

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  LOC           OBJECT CODE      ADDR1    ADDR2    STMT

00003220    00000000 00000000                     2291+V1057   DS    XL16          V1 output
00003228    00000000 00000000
00003230    00000000 00000000                     2292+        DS    FD            gap
                                                  2293+*
00003238                                          2294+X57     DS    0F
00003238    E310 5010 0014                00000010 2295+       LGF   R1,V2ADDR     load v2 source
0000323E    E761 0000 0806                00000000 2296+       VL    v22,0(R1)     use v22 to test decoder
00003244    E310 5014 0014                00000014 2297+       LGF   R1,V3ADDR     load v3 source
0000324A    E771 0000 0806                00000000 2298+       VL    v23,0(R1)     use v23 to test decoder
00003250    E766 7000 4EA3                         2299+       VMH   V22,V22,V23,4  test instruction (dest is a source)
00003256    E760 5028 080E                00003220 2300+       VST   V22,V1057      save v1 output
0000325C    07FB                                   2301+       BR    R11           return
00003260                                           2302+RE57   DC    0F            xl16 expected result
00003260                                           2303+       DROP  R5
00003260    00000000 00000001                      2304        DC    XL16'0000000000000001 FFFCE00270FFFF8F'    result
00003268    FFFCE002 70FFFF8F
00003270    FFFFFFFF 00019000                      2305        DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'    v2
00003278    00000038 EEEEEEFA
00003280    FFFFFFFF 00019000                      2306        DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'    v3
00003288    00000038 0EEEEEFA

                                                   2307
                                                   2308        VRR_C VMH,4
00003290                                           2309+       DS    0FD
00003290                              00003290     2310+       USING *,R5          base for test data and test routine
00003290    000032D0                               2311+T58    DC    A(X58)        address of test routine
00003294    003A                                   2312+       DC    H'58'         test number
00003296    00                                     2313+       DC    X'00'
00003297    04                                     2314+       DC    HL1'4'        m4
00003298    E5D4C840 40404040                      2315+       DC    CL8'VMH'      instruction name
000032A0    00003308                               2316+       DC    A(RE58+16)    address of v2 source
000032A4    00003318                               2317+       DC    A(RE58+32)    address of v3 source
000032A8    00000010                               2318+       DC    A(16)         result length
000032AC    000032F8                               2319+REA58  DC    A(RE58)       result address
000032B0    00000000 00000000                      2320+       DS    FD            gap
000032B8    00000000 00000000                      2321+V1058  DS    XL16          V1 output
000032C0    00000000 00000000
000032C8    00000000 00000000                      2322+       DS    FD            gap
                                                   2323+*
000032D0                                           2324+X58    DS    0F
000032D0    E310 5010 0014                00000010 2325+       LGF   R1,V2ADDR     load v2 source
000032D6    E761 0000 0806                00000000 2326+       VL    v22,0(R1)     use v22 to test decoder
000032DC    E310 5014 0014                00000014 2327+       LGF   R1,V3ADDR     load v3 source
000032E2    E771 0000 0806                00000000 2328+       VL    v23,0(R1)     use v23 to test decoder
000032E8    E766 7000 4EA3                         2329+       VMH   V22,V22,V23,4  test instruction (dest is a source)
000032EE    E760 5028 080E                000032B8 2330+       VST   V22,V1058      save v1 output
000032F4    07FB                                   2331+       BR    R11           return
000032F8                                           2332+RE58   DC    0F            xl16 expected result
000032F8                                           2333+       DROP  R5
000032F8    FFFF0004 0C192C45                      2334        DC    XL16'FFFF00040C192C45 69B57B4BBDEC6504'    result
00003300    69B57B4B BDEC6504
00003308    FF020304 05060750                      2335        DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'    v2
00003310    090A0B0C 0D0E0F7F
00003318    01020304 05060750                      2336        DC    XL16'0102030405060750 090A0B780D0E0F7F'    v3
00003320    090A0B78 0D0E0F7F

                                                   2337
                                                   2338        VRR_C VMH,4
```

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  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

00003328                                           2339+         DS     0FD
00003328                       00003328            2340+         USING  *,R5                base for test data and test routine
00003328   00003368                                2341+T59      DC     A(X59)              address of test routine
0000332C   003B                                    2342+         DC     H'59'               test number
0000332E   00                                      2343+         DC     X'00'
0000332F   04                                      2344+         DC     HL1'4'              m4
00003330   E5D4C840 40404040                        2345+         DC     CL8'VMH'            instruction name
00003338   000033A0                                2346+         DC     A(RE59+16)          address of v2 source
0000333C   000033B0                                2347+         DC     A(RE59+32)          address of v3 source
00003340   00000010                                2348+         DC     A(16)               result length
00003344   00003390                                2349+REA59    DC     A(RE59)             result address
00003348   00000000 00000000                       2350+         DS     FD                  gap
00003350   00000000 00000000                       2351+V1059    DS     XL16                V1 output
00003358   00000000 00000000
00003360   00000000 00000000                       2352+         DS     FD                  gap
                                                   2353+*
00003368                                           2354+X59      DS     0F
00003368   E310 5010 0014                 00000010 2355+         LGF    R1,V2ADDR           load v2 source
0000336E   E761 0000 0806                 00000000 2356+         VL     v22,0(R1)           use v22 to test decoder
00003374   E310 5014 0014                 00000014 2357+         LGF    R1,V3ADDR           load v3 source
0000337A   E771 0000 0806                 00000000 2358+         VL     v23,0(R1)           use v23 to test decoder
00003380   E766 7000 4EA3                          2359+         VMH    V22,V22,V23,4        test instruction (dest is a source)
00003386   E760 5028 080E                 00003350 2360+         VST    V22,V1059            save v1 output
0000338C   07FB                                    2361+         BR     R11                 return
00003390                                           2362+RE59     DC     0F                  xl16 expected result
00003390                                           2363+         DROP   R5
00003390   FFFFFF01 0309101B                       2364          DC     XL16'FFFFFF010309101B 06CF0A94A5DE7262'     result
00003398   06CF0A94 A5DE7262
000033A0   FF020304 05060750                       2365          DC     XL16'FF02030405060750 090A0B0C0D0E0F7F'     v2
000033A8   090A0B0C 0D0E0F7F
000033B0   00010102 02030328                       2366          DC     XL16'0001010202030328 0405053C0607073F'     v3
000033B8   0405053C 0607073F
                                                   2367
                                                   2368          VRR_C  VMH,4
000033C0                                           2369+         DS     0FD
000033C0                       000033C0            2370+         USING  *,R5                base for test data and test routine
000033C0   00003400                                2371+T60      DC     A(X60)              address of test routine
000033C4   003C                                    2372+         DC     H'60'               test number
000033C6   00                                      2373+         DC     X'00'
000033C7   04                                      2374+         DC     HL1'4'              m4
000033C8   E5D4C840 40404040                        2375+         DC     CL8'VMH'            instruction name
000033D0   00003438                                2376+         DC     A(RE60+16)          address of v2 source
000033D4   00003448                                2377+         DC     A(RE60+32)          address of v3 source
000033D8   00000010                                2378+         DC     A(16)               result length
000033DC   00003428                                2379+REA60    DC     A(RE60)             result address
000033E0   00000000 00000000                       2380+         DS     FD                  gap
000033E8   00000000 00000000                       2381+V1060    DS     XL16                V1 output
000033F0   00000000 00000000
000033F8   00000000 00000000                       2382+         DS     FD                  gap
                                                   2383+*
00003400                                           2384+X60      DS     0F
00003400   E310 5010 0014                 00000010 2385+         LGF    R1,V2ADDR           load v2 source
00003406   E761 0000 0806                 00000000 2386+         VL     v22,0(R1)           use v22 to test decoder
0000340C   E310 5014 0014                 00000014 2387+         LGF    R1,V3ADDR           load v3 source
00003412   E771 0000 0806                 00000000 2388+         VL     v23,0(R1)           use v23 to test decoder
00003418   E766 7000 4EA3                          2389+         VMH    V22,V22,V23,4        test instruction (dest is a source)
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000341E	E760 5028 080E		000033E8	2390+	VST	V22,V1060	save v1 output
00003424	07FB			2391+	BR	R11	return
00003428				2392+RE60	DC	0F	xl16 expected result
00003428				2393+	DROP	R5	
00003428	FFFFFFFF FFFFFFFE			2394	DC	XL16'FFFFFFFFFFFFFFFE F6131F2C2C658672'	result
00003430	F6131F2C 2C658672						
00003438	FF020304 05060750			2395	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00003440	090A0B0C 0D0E0F7F						
00003448	00000000 0000000A			2396	DC	XL16'000000000000000A 0101010F0101010F'	v3
00003450	0101010F 0101010F						
				2397			
				2398	*--		
				2399	* VMLE - Vector Multiply Logical Even		
				2400	*--		
				2401	* Byte		
				2402		VRR_C VMLE,0	
00003458				2403+	DS	0FD	
00003458		00003458		2404+	USING	*,R5	base for test data and test routine
00003458	00003498			2405+T61	DC	A(X61)	address of test routine
0000345C	003D			2406+	DC	H'61'	test number
0000345E	00			2407+	DC	X'00'	
0000345F	00			2408+	DC	HL1'0'	m4
00003460	E5D4D3C5 40404040			2409+	DC	CL8'VMLE'	instruction name
00003468	000034D0			2410+	DC	A(RE61+16)	address of v2 source
0000346C	000034E0			2411+	DC	A(RE61+32)	address of v3 source
00003470	00000010			2412+	DC	A(16)	result length
00003474	000034C0			2413+REA61	DC	A(RE61)	result address
00003478	00000000 00000000			2414+	DS	FD	gap
00003480	00000000 00000000			2415+V1061	DS	XL16	V1 output
00003488	00000000 00000000						
00003490	00000000 00000000			2416+	DS	FD	gap
				2417+*			
00003498				2418+X61	DS	0F	
00003498	E310 5010 0014		00000010	2419+	LGF	R1,V2ADDR	load v2 source
0000349E	E761 0000 0806		00000000	2420+	VL	v22,0(R1)	use v22 to test decoder
000034A4	E310 5014 0014		00000014	2421+	LGF	R1,V3ADDR	load v3 source
000034AA	E771 0000 0806		00000000	2422+	VL	v23,0(R1)	use v23 to test decoder
000034B0	E766 7000 0EA4			2423+	VMLE	V22,V22,V23,0	test instruction (dest is a source)
000034B6	E760 5028 080E		00003480	2424+	VST	V22,V1061	save v1 output
000034BC	07FB			2425+	BR	R11	return
000034C0				2426+RE61	DC	0F	xl16 expected result
000034C0				2427+	DROP	R5	
000034C0	FE010000 00000000			2428	DC	XL16'FE01000000000000 0C40000000000000'	result
000034C8	0C400000 00000000						
000034D0	FF000000 00000019			2429	DC	XL16'FF00000000000019 38000000000000FA'	v2
000034D8	38000000 000000FA						
000034E0	FF000000 00000019			2430	DC	XL16'FF00000000000019 38000000000000FA'	v3
000034E8	38000000 000000FA						
				2431			
				2432		VRR_C VMLE,0	
000034F0				2433+	DS	0FD	
000034F0		000034F0		2434+	USING	*,R5	base for test data and test routine
000034F0	00003530			2435+T62	DC	A(X62)	address of test routine
000034F4	003E			2436+	DC	H'62'	test number
000034F6	00			2437+	DC	X'00'	
000034F7	00			2438+	DC	HL1'0'	m4

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  LOC         OBJECT CODE      ADDR1     ADDR2     STMT

000034F8  E5D4D3C5 40404040                        2439+        DC    CL8'VMLE'          instruction name
00003500  00003568                                 2440+        DC    A(RE62+16)         address of v2 source
00003504  00003578                                 2441+        DC    A(RE62+32)         address of v3 source
00003508  00000010                                 2442+        DC    A(16)              result length
0000350C  00003558                                 2443+REA62   DC    A(RE62)            result address
00003510  00000000 00000000                        2444+        DS    FD                 gap
00003518  00000000 00000000                        2445+V1062   DS    XL16               V1 output
00003520  00000000 00000000
00003528  00000000 00000000                        2446+        DS    FD                 gap
                                                   2447+*
00003530                                           2448+X62     DS    0F
00003530  E310 5010 0014               00000010    2449+        LGF   R1,V2ADDR          load v2 source
00003536  E761 0000 0806               00000000    2450+        VL    v22,0(R1)          use v22 to test decoder
0000353C  E310 5014 0014               00000014    2451+        LGF   R1,V3ADDR          load v3 source
00003542  E771 0000 0806               00000000    2452+        VL    v23,0(R1)          use v23 to test decoder
00003548  E766 7000 0EA4                           2453+        VMLE  V22,V22,V23,0       test instruction (dest is a source)
0000354E  E760 5028 080E               00003518    2454+        VST   V22,V1062           save v1 output
00003554  07FB                                     2455+        BR    R11                return
00003558                                           2456+RE62    DC    0F                 xl16 expected result
00003558                                           2457+        DROP  R5
00003558  FE010009 00190031                        2458         DC    XL16'FE01000900190031 00510079009C00D2'    result
00003560  00510079 009C00D2
00003568  FF020304 05060750                        2459         DC    XL16'FF02030405060750 090A0B780C0D0EFD'    v2
00003570  090A0B78 0C0D0EFD
00003578  FF020304 05060750                        2460         DC    XL16'FF02030405060750 090A0B780D0E0FFD'    v3
00003580  090A0B78 0D0E0FFD

                                                   2461
                                                   2462         VRR_C VMLE,0
00003588                                           2463+        DS    0FD
00003588                          00003588         2464+        USING *,R5                base for test data and test routine
00003588  000035C8                                 2465+T63     DC    A(X63)             address of test routine
0000358C  003F                                     2466+        DC    H'63'              test number
0000358E  00                                       2467+        DC    X'00'
0000358F  00                                       2468+        DC    HL1'0'             m4
00003590  E5D4D3C5 40404040                        2469+        DC    CL8'VMLE'          instruction name
00003598  00003600                                 2470+        DC    A(RE63+16)         address of v2 source
0000359C  00003610                                 2471+        DC    A(RE63+32)         address of v3 source
000035A0  00000010                                 2472+        DC    A(16)              result length
000035A4  000035F0                                 2473+REA63   DC    A(RE63)            result address
000035A8  00000000 00000000                        2474+        DS    FD                 gap
000035B0  00000000 00000000                        2475+V1063   DS    XL16               V1 output
000035B8  00000000 00000000
000035C0  00000000 00000000                        2476+        DS    FD                 gap
                                                   2477+*
000035C8                                           2478+X63     DS    0F
000035C8  E310 5010 0014               00000010    2479+        LGF   R1,V2ADDR          load v2 source
000035CE  E761 0000 0806               00000000    2480+        VL    v22,0(R1)          use v22 to test decoder
000035D4  E310 5014 0014               00000014    2481+        LGF   R1,V3ADDR          load v3 source
000035DA  E771 0000 0806               00000000    2482+        VL    v23,0(R1)          use v23 to test decoder
000035E0  E766 7000 0EA4                           2483+        VMLE  V22,V22,V23,0       test instruction (dest is a source)
000035E6  E760 5028 080E               000035B0    2484+        VST   V22,V1063           save v1 output
000035EC  07FB                                     2485+        BR    R11                return
000035F0                                           2486+RE63    DC    0F                 xl16 expected result
000035F0                                           2487+        DROP  R5
000035F0  FE010003 000A0015                        2488         DC    XL16'FE010003000A0015 0024003700480062'    result
000035F8  00240037 00480062
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   LOC        OBJECT CODE      ADDR1     ADDR2      STMT

00003600   FF020304 05060750                         2489           DC      XL16'FF02030405060750 090A0B780C0D0EFD'    v2
00003608   090A0B78 0C0D0EFD
00003610   FF010102 02030328                         2490           DC      XL16'FF01010202030328 0405053C060707FE'    v3
00003618   0405053C 060707FE
                                                     2491
                                                     2492           VRR_C   VMLE,0
00003620                                             2493+          DS      0FD
00003620                         00003620            2494+          USING   *,R5                         base for test data and test routine
00003620   00003660                                  2495+T64       DC      A(X64)                       address of test routine
00003624   0040                                      2496+          DC      H'64'                        test number
00003626   00                                        2497+          DC      X'00'
00003627   00                                        2498+          DC      HL1'0'                       m4
00003628   E5D4D3C5 40404040                         2499+          DC      CL8'VMLE'                    instruction name
00003630   00003698                                  2500+          DC      A(RE64+16)                   address of v2 source
00003634   000036A8                                  2501+          DC      A(RE64+32)                   address of v3 source
00003638   00000010                                  2502+          DC      A(16)                        result length
0000363C   00003688                                  2503+REA64     DC      A(RE64)                      result address
00003640   00000000 00000000                         2504+          DS      FD                           gap
00003648   00000000 00000000                         2505+V1064     DS      XL16                         V1 output
00003650   00000000 00000000
00003658   00000000 00000000                         2506+          DS      FD                           gap
                                                     2507+*
00003660                                             2508+X64       DS      0F
00003660   E310 5010 0014                 00000010   2509+          LGF     R1,V2ADDR                    load v2 source
00003666   E761 0000 0806                 00000000   2510+          VL      v22,0(R1)                    use v22 to test decoder
0000366C   E310 5014 0014                 00000014   2511+          LGF     R1,V3ADDR                    load v3 source
00003672   E771 0000 0806                 00000000   2512+          VL      v23,0(R1)                    use v23 to test decoder
00003678   E766 7000 0EA4                            2513+          VMLE    V22,V22,V23,0                 test instruction (dest is a source)
0000367E   E760 5028 080E                 00003648   2514+          VST     V22,V1064                     save v1 output
00003684   07FB                                      2515+          BR      R11                          return
00003688                                             2516+RE64      DC      0F                           xl16 expected result
00003688                                             2517+          DROP    R5
00003688   FE010000 00000000                         2518           DC      XL16'FE01000000000000 0009000B000C000E'    result
00003690   0009000B 000C000E
00003698   FF020304 05060750                         2519           DC      XL16'FF02030405060750 090A0B780C0D0EFD'    v2
000036A0   090A0B78 0C0D0EFD
000036A8   FF000000 0000000A                         2520           DC      XL16'FF0000000000000A 0101010F010101FF'    v3
000036B0   0101010F 010101FF
                                                     2521
                                                     2522 * Halfword
                                                     2523           VRR_C   VMLE,1
000036B8                                             2524+          DS      0FD
000036B8                         000036B8            2525+          USING   *,R5                         base for test data and test routine
000036B8   000036F8                                  2526+T65       DC      A(X65)                       address of test routine
000036BC   0041                                      2527+          DC      H'65'                        test number
000036BE   00                                        2528+          DC      X'00'
000036BF   01                                        2529+          DC      HL1'1'                       m4
000036C0   E5D4D3C5 40404040                         2530+          DC      CL8'VMLE'                    instruction name
000036C8   00003730                                  2531+          DC      A(RE65+16)                   address of v2 source
000036CC   00003740                                  2532+          DC      A(RE65+32)                   address of v3 source
000036D0   00000010                                  2533+          DC      A(16)                        result length
000036D4   00003720                                  2534+REA65     DC      A(RE65)                      result address
000036D8   00000000 00000000                         2535+          DS      FD                           gap
000036E0   00000000 00000000                         2536+V1065     DS      XL16                         V1 output
000036E8   00000000 00000000
000036F0   00000000 00000000                         2537+          DS      FD                           gap
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				2538+*			
000036F8				2539+X65	DS	0F	
000036F8	E310 5010 0014		00000010	2540+	LGF	R1,V2ADDR	load v2 source
000036FE	E761 0000 0806		00000000	2541+	VL	v22,0(R1)	use v22 to test decoder
00003704	E310 5014 0014		00000014	2542+	LGF	R1,V3ADDR	load v3 source
0000370A	E771 0000 0806		00000000	2543+	VL	v23,0(R1)	use v23 to test decoder
00003710	E766 7000 1EA4			2544+	VMLE	V22,V22,V23,1	test instruction (dest is a source)
00003716	E760 5028 080E		000036E0	2545+	VST	V22,V1065	save v1 output
0000371C	07FB			2546+	BR	R11	return
00003720				2547+RE65	DC	0F	xl16 expected result
00003720				2548+	DROP	R5	
00003720	FFFE0001 00000000			2549	DC	XL16'FFFE000100000000 00000C4008000000'	result
00003728	00000C40 08000000						
00003730	FFFF0000 00000019			2550	DC	XL16'FFFF000000000019 003800001000EEFA'	v2
00003738	00380000 1000EEFA						
00003740	FFFF0000 00000019			2551	DC	XL16'FFFF000000000019 003800038000EEFA'	v3
00003748	00380003 8000EEFA						
				2552			
				2553	VRR_C	VMLE,1	
00003750				2554+	DS	0FD	
00003750		00003750		2555+	USING	*,R5	base for test data and test routine
00003750	00003790			2556+T66	DC	A(X66)	address of test routine
00003754	0042			2557+	DC	H'66'	test number
00003756	00			2558+	DC	X'00'	
00003757	01			2559+	DC	HL1'1'	m4
00003758	E5D4D3C5 40404040			2560+	DC	CL8'VMLE'	instruction name
00003760	000037C8			2561+	DC	A(RE66+16)	address of v2 source
00003764	000037D8			2562+	DC	A(RE66+32)	address of v3 source
00003768	00000010			2563+	DC	A(16)	result length
0000376C	000037B8			2564+REA66	DC	A(RE66)	result address
00003770	00000000 00000000			2565+	DS	FD	gap
00003778	00000000 00000000			2566+V1066	DS	XL16	V1 output
00003780	00000000 00000000						
00003788	00000000 00000000			2567+	DS	FD	gap
				2568+*			
00003790				2569+X66	DS	0F	
00003790	E310 5010 0014		00000010	2570+	LGF	R1,V2ADDR	load v2 source
00003796	E761 0000 0806		00000000	2571+	VL	v22,0(R1)	use v22 to test decoder
0000379C	E310 5014 0014		00000014	2572+	LGF	R1,V3ADDR	load v3 source
000037A2	E771 0000 0806		00000000	2573+	VL	v23,0(R1)	use v23 to test decoder
000037A8	E766 7000 1EA4			2574+	VMLE	V22,V22,V23,1	test instruction (dest is a source)
000037AE	E760 5028 080E		00003778	2575+	VST	V22,V1066	save v1 output
000037B4	07FB			2576+	BR	R11	return
000037B8				2577+RE66	DC	0F	xl16 expected result
000037B8				2578+	DROP	R5	
000037B8	FE04FC04 00193C24			2579	DC	XL16'FE04FC0400193C24 0051B464009D51B6'	result
000037C0	0051B464 009D51B6						
000037C8	FF020304 05060750			2580	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
000037D0	090A0B78 0C0D0EFD						
000037D8	FF020304 05060750			2581	DC	XL16'FF02030405060750 090A0B780D0E0FFD'	v3
000037E0	090A0B78 0D0E0FFD						
				2582			
				2583	VRR_C	VMLE,1	
000037E8				2584+	DS	0FD	
000037E8		000037E8		2585+	USING	*,R5	base for test data and test routine
000037E8	00003828			2586+T67	DC	A(X67)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000037EC	0043			2587+	DC	H'67'	test number
000037EE	00			2588+	DC	X'00'	
000037EF	01			2589+	DC	HL1'1'	m4
000037F0	E5D4D3C5 40404040			2590+	DC	CL8'VMLE'	instruction name
000037F8	00003860			2591+	DC	A(RE67+16)	address of v2 source
000037FC	00003870			2592+	DC	A(RE67+32)	address of v3 source
00003800	00000010			2593+	DC	A(16)	result length
00003804	00003850			2594+REA67	DC	A(RE67)	result address
00003808	00000000 00000000			2595+	DS	FD	gap
00003810	00000000 00000000			2596+V1067	DS	XL16	V1 output
00003818	00000000 00000000						
00003820	00000000 00000000			2597+	DS	FD	gap
				2598+*			
00003828				2599+X67	DS	0F	
00003828	E310 5010 0014		00000010	2600+	LGF	R1,V2ADDR	load v2 source
0000382E	E761 0000 0806		00000000	2601+	VL	v22,0(R1)	use v22 to test decoder
00003834	E310 5014 0014		00000014	2602+	LGF	R1,V3ADDR	load v3 source
0000383A	E771 0000 0806		00000000	2603+	VL	v23,0(R1)	use v23 to test decoder
00003840	E766 7000 1EA4			2604+	VMLE	V22,V22,V23,1	test instruction (dest is a source)
00003846	E760 5028 080E		00003810	2605+	VST	V22,V1067	save v1 output
0000384C	07FB			2606+	BR	R11	return
00003850				2607+RE67	DC	0F	xl16 expected result
00003850				2608+	DROP	R5	
00003850	FE03FD02 000A1B12			2609	DC	XL16'FE03FD02000A1B12 002455320048A25B'	result
00003858	00245532 0048A25B						
00003860	FF020304 05060750			2610	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00003868	090A0B78 0C0D0EFD						
00003870	FF010102 02030328			2611	DC	XL16'FF01010202030328 0405053C060707FE'	v3
00003878	0405053C 060707FE						
				2612			
				2613	VRR_C	VMLE,1	
00003880				2614+	DS	0FD	
00003880		00003880		2615+	USING	*,R5	base for test data and test routine
00003880	000038C0			2616+T68	DC	A(X68)	address of test routine
00003884	0044			2617+	DC	H'68'	test number
00003886	00			2618+	DC	X'00'	
00003887	01			2619+	DC	HL1'1'	m4
00003888	E5D4D3C5 40404040			2620+	DC	CL8'VMLE'	instruction name
00003890	000038F8			2621+	DC	A(RE68+16)	address of v2 source
00003894	00003908			2622+	DC	A(RE68+32)	address of v3 source
00003898	00000010			2623+	DC	A(16)	result length
0000389C	000038E8			2624+REA68	DC	A(RE68)	result address
000038A0	00000000 00000000			2625+	DS	FD	gap
000038A8	00000000 00000000			2626+V1068	DS	XL16	V1 output
000038B0	00000000 00000000						
000038B8	00000000 00000000			2627+	DS	FD	gap
				2628+*			
000038C0				2629+X68	DS	0F	
000038C0	E310 5010 0014		00000010	2630+	LGF	R1,V2ADDR	load v2 source
000038C6	E761 0000 0806		00000000	2631+	VL	v22,0(R1)	use v22 to test decoder
000038CC	E310 5014 0014		00000014	2632+	LGF	R1,V3ADDR	load v3 source
000038D2	E771 0000 0806		00000000	2633+	VL	v23,0(R1)	use v23 to test decoder
000038D8	E766 7000 1EA4			2634+	VMLE	V22,V22,V23,1	test instruction (dest is a source)
000038DE	E760 5028 080E		000038A8	2635+	VST	V22,V1068	save v1 output
000038E4	07FB			2636+	BR	R11	return
000038E8				2637+RE68	DC	0F	xl16 expected result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000038E8				2638+	DROP	R5	
000038E8	FE02FE00 00000000			2639	DC	XL16'FE02FE0000000000 0009130A000C190D'	result
000038F0	0009130A 000C190D						
000038F8	FF020304 05060750			2640	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00003900	090A0B78 0C0D0EFD						
00003908	FF000000 0000000A			2641	DC	XL16'FF0000000000000A 0101010F010101FF'	v3
00003910	0101010F 010101FF						
				2642			
				2643	* Word		
				2644	VRR_C	VMLE,2	
00003918				2645+	DS	0FD	
00003918		00003918		2646+	USING	*,R5	base for test data and test routine
00003918	00003958			2647+T69	DC	A(X69)	address of test routine
0000391C	0045			2648+	DC	H'69'	test number
0000391E	00			2649+	DC	X'00'	
0000391F	02			2650+	DC	HL1'2'	m4
00003920	E5D4D3C5 40404040			2651+	DC	CL8'VMLE'	instruction name
00003928	00003990			2652+	DC	A(RE69+16)	address of v2 source
0000392C	000039A0			2653+	DC	A(RE69+32)	address of v3 source
00003930	00000010			2654+	DC	A(16)	result length
00003934	00003980			2655+REA69	DC	A(RE69)	result address
00003938	00000000 00000000			2656+	DS	FD	gap
00003940	00000000 00000000			2657+V1069	DS	XL16	V1 output
00003948	00000000 00000000						
00003950	00000000 00000000			2658+	DS	FD	gap
				2659+*			
00003958				2660+X69	DS	0F	
00003958	E310 5010 0014		00000010	2661+	LGF	R1,V2ADDR	load v2 source
0000395E	E761 0000 0806		00000000	2662+	VL	v22,0(R1)	use v22 to test decoder
00003964	E310 5014 0014		00000014	2663+	LGF	R1,V3ADDR	load v3 source
0000396A	E771 0000 0806		00000000	2664+	VL	v23,0(R1)	use v23 to test decoder
00003970	E766 7000 2EA4			2665+	VMLE	V22,V22,V23,2	test instruction (dest is a source)
00003976	E760 5028 080E		00003940	2666+	VST	V22,V1069	save v1 output
0000397C	07FB			2667+	BR	R11	return
00003980				2668+RE69	DC	0F	xl16 expected result
00003980				2669+	DROP	R5	
00003980	FFFFFFFE 00000001			2670	DC	XL16'FFFFFFFE00000001 0000000000000C40'	result
00003988	00000000 00000C40						
00003990	FFFFFFFF 00019000			2671	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00003998	00000038 EEEEEEFA						
000039A0	FFFFFFFF 00019000			2672	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
000039A8	00000038 0EEEEEFA						
				2673			
				2674	VRR_C	VMLE,2	
000039B0				2675+	DS	0FD	
000039B0		000039B0		2676+	USING	*,R5	base for test data and test routine
000039B0	000039F0			2677+T70	DC	A(X70)	address of test routine
000039B4	0046			2678+	DC	H'70'	test number
000039B6	00			2679+	DC	X'00'	
000039B7	02			2680+	DC	HL1'2'	m4
000039B8	E5D4D3C5 40404040			2681+	DC	CL8'VMLE'	instruction name
000039C0	00003A28			2682+	DC	A(RE70+16)	address of v2 source
000039C4	00003A38			2683+	DC	A(RE70+32)	address of v3 source
000039C8	00000010			2684+	DC	A(16)	result length
000039CC	00003A18			2685+REA70	DC	A(RE70)	result address
000039D0	00000000 00000000			2686+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000039D8	00000000 00000000			2687+V1070	DS	XL16	V1 output
000039E0	00000000 00000000						
000039E8	00000000 00000000			2688+	DS	FD	gap
				2689+*			
000039F0				2690+X70	DS	0F	
000039F0	E310 5010 0014		00000010	2691+	LGF	R1,V2ADDR	load v2 source
000039F6	E761 0000 0806		00000000	2692+	VL	v22,0(R1)	use v22 to test decoder
000039FC	E310 5014 0014		00000014	2693+	LGF	R1,V3ADDR	load v3 source
00003A02	E771 0000 0806		00000000	2694+	VL	v23,0(R1)	use v23 to test decoder
00003A08	E766 7000 2EA4			2695+	VMLE	V22,V22,V23,2	test instruction (dest is a source)
00003A0E	E760 5028 080E		000039D8	2696+	VST	V22,V1070	save v1 output
00003A14	07FB			2697+	BR	R11	return
00003A18				2698+RE70	DC	0F	xl16 expected result
00003A18				2699+	DROP	R5	
00003A18	FE050206 04191810			2700	DC	XL16'FE05020604191810 0051B52F85A6B1A0'	result
00003A20	0051B52F 85A6B1A0						
00003A28	FF020304 05060750			2701	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00003A30	090A0B0C 0D0E0F7F						
00003A38	FF020304 05060750			2702	DC	XL16'FF02030405060750 090A0B780D0E0F7F'	v3
00003A40	090A0B78 0D0E0F7F						
				2703			
				2704		VRR_C VMLE,2	
00003A48				2705+	DS	0FD	
00003A48		00003A48		2706+	USING	*,R5	base for test data and test routine
00003A48	00003A88			2707+T71	DC	A(X71)	address of test routine
00003A4C	0047			2708+	DC	H'71'	test number
00003A4E	00			2709+	DC	X'00'	
00003A4F	02			2710+	DC	HL1'2'	m4
00003A50	E5D4D3C5 40404040			2711+	DC	CL8'VMLE'	instruction name
00003A58	00003AC0			2712+	DC	A(RE71+16)	address of v2 source
00003A5C	00003AD0			2713+	DC	A(RE71+32)	address of v3 source
00003A60	00000010			2714+	DC	A(16)	result length
00003A64	00003AB0			2715+REA71	DC	A(RE71)	result address
00003A68	00000000 00000000			2716+	DS	FD	gap
00003A70	00000000 00000000			2717+V1071	DS	XL16	V1 output
00003A78	00000000 00000000						
00003A80	00000000 00000000			2718+	DS	FD	gap
				2719+*			
00003A88				2720+X71	DS	0F	
00003A88	E310 5010 0014		00000010	2721+	LGF	R1,V2ADDR	load v2 source
00003A8E	E761 0000 0806		00000000	2722+	VL	v22,0(R1)	use v22 to test decoder
00003A94	E310 5014 0014		00000014	2723+	LGF	R1,V3ADDR	load v3 source
00003A9A	E771 0000 0806		00000000	2724+	VL	v23,0(R1)	use v23 to test decoder
00003AA0	E766 7000 2EA4			2725+	VMLE	V22,V22,V23,2	test instruction (dest is a source)
00003AA6	E760 5028 080E		00003A70	2726+	VST	V22,V1071	save v1 output
00003AAC	07FB			2727+	BR	R11	return
00003AB0				2728+RE71	DC	0F	xl16 expected result
00003AB0				2729+	DROP	R5	
00003AB0	FE040103 FF0B0A08			2730	DC	XL16'FE040103FF0B0A08 0024558DB7CDD2D0'	result
00003AB8	0024558D B7CDD2D0						
00003AC0	FF020304 05060750			2731	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00003AC8	090A0B0C 0D0E0F7F						
00003AD0	FF010102 02030328			2732	DC	XL16'FF01010202030328 0405053C0607073F'	v3
00003AD8	0405053C 0607073F						
				2733			
				2734		VRR_C VMLE,2	

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00003AE0                                         2735+          DS    0FD
00003AE0                      00003AE0           2736+          USING *,R5                    base for test data and test routine
00003AE0   00003B20                              2737+T72       DC    A(X72)                   address of test routine
00003AE4   0048                                  2738+          DC    H'72'                    test number
00003AE6   00                                    2739+          DC    X'00'
00003AE7   02                                    2740+          DC    HL1'2'                   m4
00003AE8   E5D4D3C5 40404040                     2741+          DC    CL8'VMLE'                instruction name
00003AF0   00003B58                              2742+          DC    A(RE72+16)               address of v2 source
00003AF4   00003B68                              2743+          DC    A(RE72+32)               address of v3 source
00003AF8   00000010                              2744+          DC    A(16)                    result length
00003AFC   00003B48                              2745+REA72     DC    A(RE72)                  result address
00003B00   00000000 00000000                     2746+          DS    FD                       gap
00003B08   00000000 00000000                     2747+V1072     DS    XL16                     V1 output
00003B10   00000000 00000000
00003B18   00000000 00000000                     2748+          DS    FD                       gap
                                                 2749+*
00003B20                                         2750+X72       DS    0F
00003B20   E310 5010 0014           00000010     2751+          LGF   R1,V2ADDR                load v2 source
00003B26   E761 0000 0806           00000000     2752+          VL    v22,0(R1)                use v22 to test decoder
00003B2C   E310 5014 0014           00000014     2753+          LGF   R1,V3ADDR                load v3 source
00003B32   E771 0000 0806           00000000     2754+          VL    v23,0(R1)                use v23 to test decoder
00003B38   E766 7000 2EA4                        2755+          VMLE  V22,V22,V23,2             test instruction (dest is a source)
00003B3E   E760 5028 080E           00003B08     2756+          VST   V22,V1072                save v1 output
00003B44   07FB                                  2757+          BR    R11                      return
00003B48                                         2758+RE72      DC    0F                       xl16 expected result
00003B48                                         2759+          DROP  R5
00003B48   FE030100 FC000000                     2760           DC    XL16'FE030100FC000000 0009131EA8ADB1B4'      result
00003B50   0009131E A8ADB1B4
00003B58   FF020304 05060750                     2761           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'      v2
00003B60   090A0B0C 0D0E0F7F
00003B68   FF000000 0000000A                     2762           DC    XL16'FF0000000000000A 0101010F0101010F'      v3
00003B70   0101010F 0101010F
                                                 2763
                                                 2764 * Doubleword
                                                 2765           VRR_C VMLE,3
00003B78                                         2766+          DS    0FD
00003B78                      00003B78           2767+          USING *,R5                    base for test data and test routine
00003B78   00003BB8                              2768+T73       DC    A(X73)                   address of test routine
00003B7C   0049                                  2769+          DC    H'73'                    test number
00003B7E   00                                    2770+          DC    X'00'
00003B7F   03                                    2771+          DC    HL1'3'                   m4
00003B80   E5D4D3C5 40404040                     2772+          DC    CL8'VMLE'                instruction name
00003B88   00003BF0                              2773+          DC    A(RE73+16)               address of v2 source
00003B8C   00003C00                              2774+          DC    A(RE73+32)               address of v3 source
00003B90   00000010                              2775+          DC    A(16)                    result length
00003B94   00003BE0                              2776+REA73     DC    A(RE73)                  result address
00003B98   00000000 00000000                     2777+          DS    FD                       gap
00003BA0   00000000 00000000                     2778+V1073     DS    XL16                     V1 output
00003BA8   00000000 00000000
00003BB0   00000000 00000000                     2779+          DS    FD                       gap
                                                 2780+*
00003BB8                                         2781+X73       DS    0F
00003BB8   E310 5010 0014           00000010     2782+          LGF   R1,V2ADDR                load v2 source
00003BBE   E761 0000 0806           00000000     2783+          VL    v22,0(R1)                use v22 to test decoder
00003BC4   E310 5014 0014           00000014     2784+          LGF   R1,V3ADDR                load v3 source
00003BCA   E771 0000 0806           00000000     2785+          VL    v23,0(R1)                use v23 to test decoder
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003BD0	E766 7000 3EA4			2786+	VMLE	V22,V22,V23,3	test instruction (dest is a source)
00003BD6	E760 5028 080E		00003BA0	2787+	VST	V22,V1073	save v1 output
00003BDC	07FB			2788+	BR	R11	return
00003BE0				2789+RE73	DC	0F	xl16 expected result
00003BE0				2790+	DROP	R5	
00003BE0	FFFFFFFE 00032000			2791	DC	XL16'FFFFFFFE00032000 FFFCE00271000000'	result
00003BE8	FFFCE002 71000000						
00003BF0	FFFFFFFF 00019000			2792	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00003BF8	00000038 EEEEEEFA						
00003C00	FFFFFFFF 00019000			2793	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00003C08	00000038 0EEEEEFA						
				2794			
				2795	VRR_C	VMLE,3	
00003C10				2796+	DS	0FD	
00003C10		00003C10		2797+	USING	*,R5	base for test data and test routine
00003C10	00003C50			2798+T74	DC	A(X74)	address of test routine
00003C14	004A			2799+	DC	H'74'	test number
00003C16	00			2800+	DC	X'00'	
00003C17	03			2801+	DC	HL1'3'	m4
00003C18	E5D4D3C5 40404040			2802+	DC	CL8'VMLE'	instruction name
00003C20	00003C88			2803+	DC	A(RE74+16)	address of v2 source
00003C24	00003C98			2804+	DC	A(RE74+32)	address of v3 source
00003C28	00000010			2805+	DC	A(16)	result length
00003C2C	00003C78			2806+REA74	DC	A(RE74)	result address
00003C30	00000000 00000000			2807+	DS	FD	gap
00003C38	00000000 00000000			2808+V1074	DS	XL16	V1 output
00003C40	00000000 00000000						
00003C48	00000000 00000000			2809+	DS	FD	gap
				2810+*			
00003C50				2811+X74	DS	0F	
00003C50	E310 5010 0014		00000010	2812+	LGF	R1,V2ADDR	load v2 source
00003C56	E761 0000 0806		00000000	2813+	VL	v22,0(R1)	use v22 to test decoder
00003C5C	E310 5014 0014		00000014	2814+	LGF	R1,V3ADDR	load v3 source
00003C62	E771 0000 0806		00000000	2815+	VL	v23,0(R1)	use v23 to test decoder
00003C68	E766 7000 3EA4			2816+	VMLE	V22,V22,V23,3	test instruction (dest is a source)
00003C6E	E760 5028 080E		00003C38	2817+	VST	V22,V1074	save v1 output
00003C74	07FB			2818+	BR	R11	return
00003C78				2819+RE74	DC	0F	xl16 expected result
00003C78				2820+	DROP	R5	
00003C78	01010308 111F3396			2821	DC	XL16'01010308111F3396 69B556ED77F57900'	result
00003C80	69B556ED 77F57900						
00003C88	FF020304 05060750			2822	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00003C90	090A0B0C 0D0E0F7F						
00003C98	01020304 05060750			2823	DC	XL16'0102030405060750 090A0B780D0E0F7F'	v3
00003CA0	090A0B78 0D0E0F7F						
				2824			
				2825	VRR_C	VMLE,3	
00003CA8				2826+	DS	0FD	
00003CA8		00003CA8		2827+	USING	*,R5	base for test data and test routine
00003CA8	00003CE8			2828+T75	DC	A(X75)	address of test routine
00003CAC	004B			2829+	DC	H'75'	test number
00003CAE	00			2830+	DC	X'00'	
00003CAF	03			2831+	DC	HL1'3'	m4
00003CB0	E5D4D3C5 40404040			2832+	DC	CL8'VMLE'	instruction name
00003CB8	00003D20			2833+	DC	A(RE75+16)	address of v2 source
00003CBC	00003D30			2834+	DC	A(RE75+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003CC0	00000010			2835+	DC	A(16)	result length
00003CC4	00003D10			2836+REA75	DC	A(RE75)	result address
00003CC8	00000000 00000000			2837+	DS	FD	gap
00003CD0	00000000 00000000			2838+V1075	DS	XL16	V1 output
00003CD8	00000000 00000000						
00003CE0	00000000 00000000			2839+	DS	FD	gap
				2840+*			
00003CE8				2841+X75	DS	0F	
00003CE8	E310 5010 0014		00000010	2842+	LGF	R1,V2ADDR	load v2 source
00003CEE	E761 0000 0806		00000000	2843+	VL	v22,0(R1)	use v22 to test decoder
00003CF4	E310 5014 0014		00000014	2844+	LGF	R1,V3ADDR	load v3 source
00003CFA	E771 0000 0806		00000000	2845+	VL	v23,0(R1)	use v23 to test decoder
00003D00	E766 7000 3EA4			2846+	VMLE	V22,V22,V23,3	test instruction (dest is a source)
00003D06	E760 5028 080E		00003CD0	2847+	VST	V22,V1075	save v1 output
00003D0C	07FB			2848+	BR	R11	return
00003D10				2849+RE75	DC	0F	xl16 expected result
00003D10				2850+	DROP	R5	
00003D10	00010003 050C1344			2851	DC	XL16'00010003050C1344 06D2FE7090F71480'	result
00003D18	06D2FE70 90F71480						
00003D20	FF020304 05060750			2852	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00003D28	090A0B0C 0D0E0F7F						
00003D30	00010102 02030328			2853	DC	XL16'0001010202030328 0405053C0607073F'	v3
00003D38	0405053C 0607073F						
				2854			
				2855	VRR_C	VMLE,3	
00003D40				2856+	DS	0FD	
00003D40		00003D40		2857+	USING	*,R5	base for test data and test routine
00003D40	00003D80			2858+T76	DC	A(X76)	address of test routine
00003D44	004C			2859+	DC	H'76'	test number
00003D46	00			2860+	DC	X'00'	
00003D47	03			2861+	DC	HL1'3'	m4
00003D48	E5D4D3C5 40404040			2862+	DC	CL8'VMLE'	instruction name
00003D50	00003DB8			2863+	DC	A(RE76+16)	address of v2 source
00003D54	00003DC8			2864+	DC	A(RE76+32)	address of v3 source
00003D58	00000010			2865+	DC	A(16)	result length
00003D5C	00003DA8			2866+REA76	DC	A(RE76)	result address
00003D60	00000000 00000000			2867+	DS	FD	gap
00003D68	00000000 00000000			2868+V1076	DS	XL16	V1 output
00003D70	00000000 00000000						
00003D78	00000000 00000000			2869+	DS	FD	gap
				2870+*			
00003D80				2871+X76	DS	0F	
00003D80	E310 5010 0014		00000010	2872+	LGF	R1,V2ADDR	load v2 source
00003D86	E761 0000 0806		00000000	2873+	VL	v22,0(R1)	use v22 to test decoder
00003D8C	E310 5014 0014		00000014	2874+	LGF	R1,V3ADDR	load v3 source
00003D92	E771 0000 0806		00000000	2875+	VL	v23,0(R1)	use v23 to test decoder
00003D98	E766 7000 3EA4			2876+	VMLE	V22,V22,V23,3	test instruction (dest is a source)
00003D9E	E760 5028 080E		00003D68	2877+	VST	V22,V1076	save v1 output
00003DA4	07FB			2878+	BR	R11	return
00003DA8				2879+RE76	DC	0F	xl16 expected result
00003DA8				2880+	DROP	R5	
00003DA8	00000000 00000009			2881	DC	XL16'0000000000000009 F6141E28323C4920'	result
00003DB0	F6141E28 323C4920						
00003DB8	FF020304 05060750			2882	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00003DC0	090A0B0C 0D0E0F7F						
00003DC8	00000000 0000000A			2883	DC	XL16'000000000000000A 0101010F0101010F'	v3

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  LOC        OBJECT CODE      ADDR1     ADDR2      STMT

00003DD0  0101010F 0101010F
                                                   2884
                                                   2885              VRR_C VMLE, 3
00003DD8                                           2886+      DS      0FD
00003DD8                               00003DD8    2887+      USING   *, R5                   base for test data and test routine
00003DD8  00003E18                                 2888+T77   DC      A(X77)                  address of test routine
00003DDC  004D                                     2889+      DC      H'77'                   test number
00003DDE  00                                       2890+      DC      X'00'
00003DDF  03                                       2891+      DC      HL1'3'                  m4
00003DE0  E5D4D3C5 40404040                        2892+      DC      CL8'VMLE'               instruction name
00003DE8  00003E50                                 2893+      DC      A(RE77+16)              address of v2 source
00003DEC  00003E60                                 2894+      DC      A(RE77+32)              address of v3 source
00003DF0  00000010                                 2895+      DC      A(16)                   result length
00003DF4  00003E40                                 2896+REA77 DC      A(RE77)                 result address
00003DF8  00000000 00000000                        2897+      DS      FD                      gap
00003E00  00000000 00000000                        2898+V1077 DS      XL16                    V1 output
00003E08  00000000 00000000
00003E10  00000000 00000000                        2899+      DS      FD                      gap
                                                   2900+*
00003E18                                           2901+X77   DS      0F
00003E18  E310 5010 0014               00000010    2902+      LGF     R1, V2ADDR              load v2 source
00003E1E  E761 0000 0806               00000000    2903+      VL      v22, 0(R1)              use v22 to test decoder
00003E24  E310 5014 0014               00000014    2904+      LGF     R1, V3ADDR              load v3 source
00003E2A  E771 0000 0806               00000000    2905+      VL      v23, 0(R1)              use v23 to test decoder
00003E30  E766 7000 3EA4                           2906+      VMLE    V22, V22, V23, 3         test instruction (dest is a source)
00003E36  E760 5028 080E               00003E00    2907+      VST     V22, V1077               save v1 output
00003E3C  07FB                                     2908+      BR      R11                     return
00003E40                                           2909+RE77  DC      0F                      xl16 expected result
00003E40                                           2910+      DROP    R5
00003E40  0009131E A8C3DFFE                         2911       DC      XL16'0009131EA8C3DFFE 091C345060616771'     result
00003E48  091C3450 60616771
00003E50  090A0B0C 0D0E0F7F                         2912       DC      XL16'090A0B0C0D0E0F7F FF02030405060750'     v2
00003E58  FF020304 05060750
00003E60  0101010F 0101010F                         2913       DC      XL16'0101010F0101010F 000000000000000A'     v3
00003E68  00000000 0000000A
                                                   2914
                                                   2915 *-------------------------------------------------------------------
                                                   2916 *  VMLO   - Vector Multiply Logical Odd
                                                   2917 *-------------------------------------------------------------------
                                                   2918 * Byte
                                                   2919              VRR_C VMLO, 0
00003E70                                           2920+      DS      0FD
00003E70                               00003E70    2921+      USING   *, R5                   base for test data and test routine
00003E70  00003EB0                                 2922+T78   DC      A(X78)                  address of test routine
00003E74  004E                                     2923+      DC      H'78'                   test number
00003E76  00                                       2924+      DC      X'00'
00003E77  00                                       2925+      DC      HL1'0'                  m4
00003E78  E5D4D3D6 40404040                        2926+      DC      CL8'VMLO'               instruction name
00003E80  00003EE8                                 2927+      DC      A(RE78+16)              address of v2 source
00003E84  00003EF8                                 2928+      DC      A(RE78+32)              address of v3 source
00003E88  00000010                                 2929+      DC      A(16)                   result length
00003E8C  00003ED8                                 2930+REA78 DC      A(RE78)                 result address
00003E90  00000000 00000000                        2931+      DS      FD                      gap
00003E98  00000000 00000000                        2932+V1078 DS      XL16                    V1 output
00003EA0  00000000 00000000
00003EA8  00000000 00000000                        2933+      DS      FD                      gap
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				2934+*			
00003EB0				2935+X78	DS	0F	
00003EB0	E310 5010 0014		00000010	2936+	LGF	R1,V2ADDR	load v2 source
00003EB6	E761 0000 0806		00000000	2937+	VL	v22,0(R1)	use v22 to test decoder
00003EBC	E310 5014 0014		00000014	2938+	LGF	R1,V3ADDR	load v3 source
00003EC2	E771 0000 0806		00000000	2939+	VL	v23,0(R1)	use v23 to test decoder
00003EC8	E766 7000 0EA5			2940+	VMLO	V22,V22,V23,0	test instruction (dest is a source)
00003ECE	E760 5028 080E		00003E98	2941+	VST	V22,V1078	save v1 output
00003ED4	07FB			2942+	BR	R11	return
00003ED8				2943+RE78	DC	0F	xl16 expected result
00003ED8				2944+	DROP	R5	
00003ED8	00000000 00000271			2945	DC	XL16'0000000000000271 000000000000F424'	result
00003EE0	00000000 0000F424						
00003EE8	FF000000 00000019			2946	DC	XL16'FF00000000000019 38000000000000FA'	v2
00003EF0	38000000 000000FA						
00003EF8	FF000000 00000019			2947	DC	XL16'FF00000000000019 38000000000000FA'	v3
00003F00	38000000 000000FA						
				2948			
				2949	VRR_C	VMLO,0	
00003F08				2950+	DS	0FD	
00003F08		00003F08		2951+	USING	*,R5	base for test data and test routine
00003F08	00003F48			2952+T79	DC	A(X79)	address of test routine
00003F0C	004F			2953+	DC	H'79'	test number
00003F0E	00			2954+	DC	X'00'	
00003F0F	00			2955+	DC	HL1'0'	m4
00003F10	E5D4D3D6 40404040			2956+	DC	CL8'VMLO'	instruction name
00003F18	00003F80			2957+	DC	A(RE79+16)	address of v2 source
00003F1C	00003F90			2958+	DC	A(RE79+32)	address of v3 source
00003F20	00000010			2959+	DC	A(16)	result length
00003F24	00003F70			2960+REA79	DC	A(RE79)	result address
00003F28	00000000 00000000			2961+	DS	FD	gap
00003F30	00000000 00000000			2962+V1079	DS	XL16	V1 output
00003F38	00000000 00000000						
00003F40	00000000 00000000			2963+	DS	FD	gap
				2964+*			
00003F48				2965+X79	DS	0F	
00003F48	E310 5010 0014		00000010	2966+	LGF	R1,V2ADDR	load v2 source
00003F4E	E761 0000 0806		00000000	2967+	VL	v22,0(R1)	use v22 to test decoder
00003F54	E310 5014 0014		00000014	2968+	LGF	R1,V3ADDR	load v3 source
00003F5A	E771 0000 0806		00000000	2969+	VL	v23,0(R1)	use v23 to test decoder
00003F60	E766 7000 0EA5			2970+	VMLO	V22,V22,V23,0	test instruction (dest is a source)
00003F66	E760 5028 080E		00003F30	2971+	VST	V22,V1079	save v1 output
00003F6C	07FB			2972+	BR	R11	return
00003F70				2973+RE79	DC	0F	xl16 expected result
00003F70				2974+	DROP	R5	
00003F70	00040010 00241900			2975	DC	XL16'0004001000241900 0064384000B6FA09'	result
00003F78	00643840 00B6FA09						
00003F80	FF020304 05060750			2976	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00003F88	090A0B78 0C0D0EFD						
00003F90	FF020304 05060750			2977	DC	XL16'FF02030405060750 090A0B780D0E0FFD'	v3
00003F98	090A0B78 0D0E0FFD						
				2978			
				2979	VRR_C	VMLO,0	
00003FA0				2980+	DS	0FD	
00003FA0		00003FA0		2981+	USING	*,R5	base for test data and test routine
00003FA0	00003FE0			2982+T80	DC	A(X80)	address of test routine

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   LOC         OBJECT CODE      ADDR1     ADDR2     STMT

00003FA4  0050                                      2983+          DC    H'80'                 test number
00003FA6  00                                        2984+          DC    X'00'
00003FA7  00                                        2985+          DC    HL1'0'                m4
00003FA8  E5D4D3D6 40404040                         2986+          DC    CL8'VMLO'             instruction name
00003FB0  00004018                                  2987+          DC    A(RE80+16)            address of v2 source
00003FB4  00004028                                  2988+          DC    A(RE80+32)            address of v3 source
00003FB8  00000010                                  2989+          DC    A(16)                 result length
00003FBC  00004008                                  2990+REA80     DC    A(RE80)               result address
00003FC0  00000000 00000000                         2991+          DS    FD                    gap
00003FC8  00000000 00000000                         2992+V1080     DS    XL16                  V1 output
00003FD0  00000000 00000000
00003FD8  00000000 00000000                         2993+          DS    FD                    gap
                                                    2994+*
00003FE0                                            2995+X80       DS    0F
00003FE0  E310 5010 0014                 00000010   2996+          LGF   R1,V2ADDR             load v2 source
00003FE6  E761 0000 0806                 00000000   2997+          VL    v22,0(R1)             use v22 to test decoder
00003FEC  E310 5014 0014                 00000014   2998+          LGF   R1,V3ADDR             load v3 source
00003FF2  E771 0000 0806                 00000000   2999+          VL    v23,0(R1)             use v23 to test decoder
00003FF8  E766 7000 0EA5                            3000+          VMLO  V22,V22,V23,0          test instruction (dest is a source)
00003FFE  E760 5028 080E                 00003FC8   3001+          VST   V22,V1080              save v1 output
00004004  07FB                                      3002+          BR    R11                   return
00004008                                            3003+RE80      DC    0F                    xl16 expected result
00004008                                            3004+          DROP  R5
00004008  00020008 00120C80                         3005           DC    XL16'0002000800120C80 00321C20005BFB06'     result
00004010  00321C20 005BFB06
00004018  FF020304 05060750                         3006           DC    XL16'FF02030405060750 090A0B780C0D0EFD'     v2
00004020  090A0B78 0C0D0EFD
00004028  FF010102 02030328                         3007           DC    XL16'FF01010202030328 0405053C060707FE'     v3
00004030  0405053C 060707FE
                                                    3008
                                                    3009           VRR_C VMLO,0
00004038                                            3010+          DS    0FD
00004038                      00004038              3011+          USING *,R5                  base for test data and test routine
00004038  00004078                                  3012+T81       DC    A(X81)                address of test routine
0000403C  0051                                      3013+          DC    H'81'                 test number
0000403E  00                                        3014+          DC    X'00'
0000403F  00                                        3015+          DC    HL1'0'                m4
00004040  E5D4D3D6 40404040                         3016+          DC    CL8'VMLO'             instruction name
00004048  000040B0                                  3017+          DC    A(RE81+16)            address of v2 source
0000404C  000040C0                                  3018+          DC    A(RE81+32)            address of v3 source
00004050  00000010                                  3019+          DC    A(16)                 result length
00004054  000040A0                                  3020+REA81     DC    A(RE81)               result address
00004058  00000000 00000000                         3021+          DS    FD                    gap
00004060  00000000 00000000                         3022+V1081     DS    XL16                  V1 output
00004068  00000000 00000000
00004070  00000000 00000000                         3023+          DS    FD                    gap
                                                    3024+*
00004078                                            3025+X81       DS    0F
00004078  E310 5010 0014                 00000010   3026+          LGF   R1,V2ADDR             load v2 source
0000407E  E761 0000 0806                 00000000   3027+          VL    v22,0(R1)             use v22 to test decoder
00004084  E310 5014 0014                 00000014   3028+          LGF   R1,V3ADDR             load v3 source
0000408A  E771 0000 0806                 00000000   3029+          VL    v23,0(R1)             use v23 to test decoder
00004090  E766 7000 0EA5                            3030+          VMLO  V22,V22,V23,0          test instruction (dest is a source)
00004096  E760 5028 080E                 00004060   3031+          VST   V22,V1081              save v1 output
0000409C  07FB                                      3032+          BR    R11                   return
000040A0                                            3033+RE81      DC    0F                    xl16 expected result
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000040A0				3034+		DROP	R5	
000040A0	00000000 00000320			3035		DC	XL16'0000000000000320 000A0708000DFC03'	result
000040A8	000A0708 000DFC03							
000040B0	FF020304 05060750			3036		DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
000040B8	090A0B78 0C0D0EFD							
000040C0	FF000000 0000000A			3037		DC	XL16'FF0000000000000A 0101010F010101FF'	v3
000040C8	0101010F 010101FF							
				3038				
				3039	* Halfword			
				3040		VRR_C	VMLO,1	
000040D0				3041+		DS	0FD	
000040D0		000040D0		3042+		USING	*,R5	base for test data and test routine
000040D0	00004110			3043+T82		DC	A(X82)	address of test routine
000040D4	0052			3044+		DC	H'82'	test number
000040D6	00			3045+		DC	X'00'	
000040D7	01			3046+		DC	HL1'1'	m4
000040D8	E5D4D3D6 40404040			3047+		DC	CL8'VMLO'	instruction name
000040E0	00004148			3048+		DC	A(RE82+16)	address of v2 source
000040E4	00004158			3049+		DC	A(RE82+32)	address of v3 source
000040E8	00000010			3050+		DC	A(16)	result length
000040EC	00004138			3051+REA82		DC	A(RE82)	result address
000040F0	00000000 00000000			3052+		DS	FD	gap
000040F8	00000000 00000000			3053+V1082		DS	XL16	V1 output
00004100	00000000 00000000							
00004108	00000000 00000000			3054+		DS	FD	gap
				3055+*				
00004110				3056+X82		DS	0F	
00004110	E310 5010 0014		00000010	3057+		LGF	R1,V2ADDR	load v2 source
00004116	E761 0000 0806		00000000	3058+		VL	v22,0(R1)	use v22 to test decoder
0000411C	E310 5014 0014		00000014	3059+		LGF	R1,V3ADDR	load v3 source
00004122	E771 0000 0806		00000000	3060+		VL	v23,0(R1)	use v23 to test decoder
00004128	E766 7000 1EA5			3061+		VMLO	V22,V22,V23,1	test instruction (dest is a source)
0000412E	E760 5028 080E		000040F8	3062+		VST	V22,V1082	save v1 output
00004134	07FB			3063+		BR	R11	return
00004138				3064+RE82		DC	0F	xl16 expected result
00004138				3065+		DROP	R5	
00004138	00000000 00000271			3066		DC	XL16'0000000000000271 00000000DF15CC24'	result
00004140	00000000 DF15CC24							
00004148	FFFF0000 00000019			3067		DC	XL16'FFFF000000000019 003800001000EEFA'	v2
00004150	00380000 1000EEFA							
00004158	FFFF0000 00000019			3068		DC	XL16'FFFF000000000019 003800038000EEFA'	v3
00004160	00380003 8000EEFA							
				3069				
				3070		VRR_C	VMLO,1	
00004168				3071+		DS	0FD	
00004168		00004168		3072+		USING	*,R5	base for test data and test routine
00004168	000041A8			3073+T83		DC	A(X83)	address of test routine
0000416C	0053			3074+		DC	H'83'	test number
0000416E	00			3075+		DC	X'00'	
0000416F	01			3076+		DC	HL1'1'	m4
00004170	E5D4D3D6 40404040			3077+		DC	CL8'VMLO'	instruction name
00004178	000041E0			3078+		DC	A(RE83+16)	address of v2 source
0000417C	000041F0			3079+		DC	A(RE83+32)	address of v3 source
00004180	00000010			3080+		DC	A(16)	result length
00004184	000041D0			3081+REA83		DC	A(RE83)	result address
00004188	00000000 00000000			3082+		DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004190	00000000 00000000			3083+V1083	DS	XL16	V1 output
00004198	00000000 00000000						
000041A0	00000000 00000000			3084+	DS	FD	gap
				3085+*			
000041A8				3086+X83	DS	0F	
000041A8	E310 5010 0014		00000010	3087+	LGF	R1,V2ADDR	load v2 source
000041AE	E761 0000 0806		00000000	3088+	VL	v22,0(R1)	use v22 to test decoder
000041B4	E310 5014 0014		00000014	3089+	LGF	R1,V3ADDR	load v3 source
000041BA	E771 0000 0806		00000000	3090+	VL	v23,0(R1)	use v23 to test decoder
000041C0	E766 7000 1EA5			3091+	VMLO	V22,V22,V23,1	test instruction (dest is a source)
000041C6	E760 5028 080E		00004190	3092+	VST	V22,V1083	save v1 output
000041CC	07FB			3093+	BR	R11	return
000041D0				3094+RE83	DC	0F	xl16 expected result
000041D0				3095+	DROP	R5	
000041D0	00091810 00357900			3096	DC	XL16'0009181000357900 0083884000EFA309'	result
000041D8	00838840 00EFA309						
000041E0	FF020304 05060750			3097	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
000041E8	090A0B78 0C0D0EFD						
000041F0	FF020304 05060750			3098	DC	XL16'FF02030405060750 090A0B780D0E0FFD'	v3
000041F8	090A0B78 0D0E0FFD						
				3099			
				3100	VRR_C	VMLO,1	
00004200				3101+	DS	0FD	
00004200		00004200		3102+	USING	*,R5	base for test data and test routine
00004200	00004240			3103+T84	DC	A(X84)	address of test routine
00004204	0054			3104+	DC	H'84'	test number
00004206	00			3105+	DC	X'00'	
00004207	01			3106+	DC	HL1'1'	m4
00004208	E5D4D3D6 40404040			3107+	DC	CL8'VMLO'	instruction name
00004210	00004278			3108+	DC	A(RE84+16)	address of v2 source
00004214	00004288			3109+	DC	A(RE84+32)	address of v3 source
00004218	00000010			3110+	DC	A(16)	result length
0000421C	00004268			3111+REA84	DC	A(RE84)	result address
00004220	00000000 00000000			3112+	DS	FD	gap
00004228	00000000 00000000			3113+V1084	DS	XL16	V1 output
00004230	00000000 00000000						
00004238	00000000 00000000			3114+	DS	FD	gap
				3115+*			
00004240				3116+X84	DS	0F	
00004240	E310 5010 0014		00000010	3117+	LGF	R1,V2ADDR	load v2 source
00004246	E761 0000 0806		00000000	3118+	VL	v22,0(R1)	use v22 to test decoder
0000424C	E310 5014 0014		00000014	3119+	LGF	R1,V3ADDR	load v3 source
00004252	E771 0000 0806		00000000	3120+	VL	v23,0(R1)	use v23 to test decoder
00004258	E766 7000 1EA5			3121+	VMLO	V22,V22,V23,1	test instruction (dest is a source)
0000425E	E760 5028 080E		00004228	3122+	VST	V22,V1084	save v1 output
00004264	07FB			3123+	BR	R11	return
00004268				3124+RE84	DC	0F	xl16 expected result
00004268				3125+	DROP	R5	
00004268	00030A08 00171480			3126	DC	XL16'00030A0800171480 003C08200077CA06'	result
00004270	003C0820 0077CA06						
00004278	FF020304 05060750			3127	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00004280	090A0B78 0C0D0EFD						
00004288	FF010102 02030328			3128	DC	XL16'FF01010202030328 0405053C060707FE'	v3
00004290	0405053C 060707FE						
				3129			
				3130	VRR_C	VMLO,1	

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00004298                                          3131+      DS     0FD
00004298                      00004298            3132+      USING  *,R5              base for test data and test routine
00004298   000042D8                               3133+T85   DC     A(X85)            address of test routine
0000429C   0055                                   3134+      DC     H'85'             test number
0000429E   00                                     3135+      DC     X'00'
0000429F   01                                     3136+      DC     HL1'1'            m4
000042A0   E5D4D3D6 40404040                       3137+     DC     CL8'VMLO'         instruction name
000042A8   00004310                               3138+      DC     A(RE85+16)        address of v2 source
000042AC   00004320                               3139+      DC     A(RE85+32)        address of v3 source
000042B0   00000010                               3140+      DC     A(16)             result length
000042B4   00004300                               3141+REA85 DC     A(RE85)           result address
000042B8   00000000 00000000                       3142+     DS     FD                gap
000042C0   00000000 00000000                       3143+V1085 DS    XL16              V1 output
000042C8   00000000 00000000
000042D0   00000000 00000000                       3144+     DS     FD                gap
                                                  3145+*
000042D8                                          3146+X85   DS     0F
000042D8   E310 5010 0014              00000010   3147+      LGF    R1,V2ADDR         load v2 source
000042DE   E761 0000 0806              00000000   3148+      VL     v22,0(R1)         use v22 to test decoder
000042E4   E310 5014 0014              00000014   3149+      LGF    R1,V3ADDR         load v3 source
000042EA   E771 0000 0806              00000000   3150+      VL     v23,0(R1)         use v23 to test decoder
000042F0   E766 7000 1EA5                         3151+      VMLO   V22,V22,V23,1      test instruction (dest is a source)
000042F6   E760 5028 080E              000042C0   3152+      VST    V22,V1085          save v1 output
000042FC   07FB                                   3153+      BR     R11               return
00004300                                          3154+RE85  DC     0F                xl16 expected result
00004300                                          3155+      DROP   R5
00004300   00000000 00004920                      3156       DC     XL16'0000000000004920 000C2408001DEB03'     result
00004308   000C2408 001DEB03
00004310   FF020304 05060750                      3157       DC     XL16'FF02030405060750 090A0B780C0D0EFD'     v2
00004318   090A0B78 0C0D0EFD
00004320   FF000000 0000000A                      3158       DC     XL16'FF0000000000000A 0101010F010101FF'     v3
00004328   0101010F 010101FF
                                                  3159
                                                  3160 * Word
                                                  3161       VRR_C VMLO,2
00004330                                          3162+      DS     0FD
00004330                      00004330            3163+      USING  *,R5              base for test data and test routine
00004330   00004370                               3164+T86   DC     A(X86)            address of test routine
00004334   0056                                   3165+      DC     H'86'             test number
00004336   00                                     3166+      DC     X'00'
00004337   02                                     3167+      DC     HL1'2'            m4
00004338   E5D4D3D6 40404040                       3168+     DC     CL8'VMLO'         instruction name
00004340   000043A8                               3169+      DC     A(RE86+16)        address of v2 source
00004344   000043B8                               3170+      DC     A(RE86+32)        address of v3 source
00004348   00000010                               3171+      DC     A(16)             result length
0000434C   00004398                               3172+REA86 DC     A(RE86)           result address
00004350   00000000 00000000                       3173+     DS     FD                gap
00004358   00000000 00000000                       3174+V1086 DS    XL16              V1 output
00004360   00000000 00000000
00004368   00000000 00000000                       3175+     DS     FD                gap
                                                  3176+*
00004370                                          3177+X86   DS     0F
00004370   E310 5010 0014              00000010   3178+      LGF    R1,V2ADDR         load v2 source
00004376   E761 0000 0806              00000000   3179+      VL     v22,0(R1)         use v22 to test decoder
0000437C   E310 5014 0014              00000014   3180+      LGF    R1,V3ADDR         load v3 source
00004382   E771 0000 0806              00000000   3181+      VL     v23,0(R1)         use v23 to test decoder
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004388	E766 7000 2EA5			3182+	VMLO	V22,V22,V23,2	test instruction (dest is a source)
0000438E	E760 5028 080E		00004358	3183+	VST	V22,V1086	save v1 output
00004394	07FB			3184+	BR	R11	return
00004398				3185+RE86	DC	0F	xl16 expected result
00004398				3186+	DROP	R5	
00004398	00000002 71000000			3187	DC	XL16'0000000271000000 0DF0123F4FEDCC24'	result
000043A0	0DF0123F 4FEDCC24						
000043A8	FFFFFFFF 00019000			3188	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
000043B0	00000038 EEEEEEFA						
000043B8	FFFFFFFF 00019000			3189	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
000043C0	00000038 0EEEEEFA						
				3190			
				3191	VRR_C	VMLO,2	
000043C8				3192+	DS	0FD	
000043C8		000043C8		3193+	USING	*,R5	base for test data and test routine
000043C8	00004408			3194+T87	DC	A(X87)	address of test routine
000043CC	0057			3195+	DC	H'87'	test number
000043CE	00			3196+	DC	X'00'	
000043CF	02			3197+	DC	HL1'2'	m4
000043D0	E5D4D3D6 40404040			3198+	DC	CL8'VMLO'	instruction name
000043D8	00004440			3199+	DC	A(RE87+16)	address of v2 source
000043DC	00004450			3200+	DC	A(RE87+32)	address of v3 source
000043E0	00000010			3201+	DC	A(16)	result length
000043E4	00004430			3202+REA87	DC	A(RE87)	result address
000043E8	00000000 00000000			3203+	DS	FD	gap
000043F0	00000000 00000000			3204+V1087	DS	XL16	V1 output
000043F8	00000000 00000000						
00004400	00000000 00000000			3205+	DS	FD	gap
				3206+*			
00004408				3207+X87	DS	0F	
00004408	E310 5010 0014		00000010	3208+	LGF	R1,V2ADDR	load v2 source
0000440E	E761 0000 0806		00000000	3209+	VL	v22,0(R1)	use v22 to test decoder
00004414	E310 5014 0014		00000014	3210+	LGF	R1,V3ADDR	load v3 source
0000441A	E771 0000 0806		00000000	3211+	VL	v23,0(R1)	use v23 to test decoder
00004420	E766 7000 2EA5			3212+	VMLO	V22,V22,V23,2	test instruction (dest is a source)
00004426	E760 5028 080E		000043F0	3213+	VST	V22,V1087	save v1 output
0000442C	07FB			3214+	BR	R11	return
00004430				3215+RE87	DC	0F	xl16 expected result
00004430				3216+	DROP	R5	
00004430	00193C6D 77F57900			3217	DC	XL16'00193C6D77F57900 00AA6E5898D42101'	result
00004438	00AA6E58 98D42101						
00004440	FF020304 05060750			3218	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00004448	090A0B0C 0D0E0F7F						
00004450	FF020304 05060750			3219	DC	XL16'FF02030405060750 090A0B780D0E0F7F'	v3
00004458	090A0B78 0D0E0F7F						
				3220			
				3221	VRR_C	VMLO,2	
00004460				3222+	DS	0FD	
00004460		00004460		3223+	USING	*,R5	base for test data and test routine
00004460	000044A0			3224+T88	DC	A(X88)	address of test routine
00004464	0058			3225+	DC	H'88'	test number
00004466	00			3226+	DC	X'00'	
00004467	02			3227+	DC	HL1'2'	m4
00004468	E5D4D3D6 40404040			3228+	DC	CL8'VMLO'	instruction name
00004470	000044D8			3229+	DC	A(RE88+16)	address of v2 source
00004474	000044E8			3230+	DC	A(RE88+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004478	00000010			3231+	DC	A(16)	result length
0000447C	000044C8			3232+REA88	DC	A(RE88)	result address
00004480	00000000 00000000			3233+	DS	FD	gap
00004488	00000000 00000000			3234+V1088	DS	XL16	V1 output
00004490	00000000 00000000						
00004498	00000000 00000000			3235+	DS	FD	gap
				3236+*			
000044A0				3237+X88	DS	0F	
000044A0	E310 5010 0014		00000010	3238+	LGF	R1,V2ADDR	load v2 source
000044A6	E761 0000 0806		00000000	3239+	VL	v22,0(R1)	use v22 to test decoder
000044AC	E310 5014 0014		00000014	3240+	LGF	R1,V3ADDR	load v3 source
000044B2	E771 0000 0806		00000000	3241+	VL	v23,0(R1)	use v23 to test decoder
000044B8	E766 7000 2EA5			3242+	VMLO	V22,V22,V23,2	test instruction (dest is a source)
000044BE	E760 5028 080E		00004488	3243+	VST	V22,V1088	save v1 output
000044C4	07FB			3244+	BR	R11	return
000044C8				3245+RE88	DC	0F	xl16 expected result
000044C8				3246+	DROP	R5	
000044C8	000A1B30 90F71480			3247	DC	XL16'000A1B3090F71480 004EB01DFF5B4941'	result
000044D0	004EB01D FF5B4941						
000044D8	FF020304 05060750			3248	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
000044E0	090A0B0C 0D0E0F7F						
000044E8	FF010102 02030328			3249	DC	XL16'FF01010202030328 0405053C0607073F'	v3
000044F0	0405053C 0607073F						
				3250			
				3251	VRR_C	VMLO,2	
000044F8				3252+	DS	0FD	
000044F8		000044F8		3253+	USING	*,R5	base for test data and test routine
000044F8	00004538			3254+T89	DC	A(X89)	address of test routine
000044FC	0059			3255+	DC	H'89'	test number
000044FE	00			3256+	DC	X'00'	
000044FF	02			3257+	DC	HL1'2'	m4
00004500	E5D4D3D6 40404040			3258+	DC	CL8'VMLO'	instruction name
00004508	00004570			3259+	DC	A(RE89+16)	address of v2 source
0000450C	00004580			3260+	DC	A(RE89+32)	address of v3 source
00004510	00000010			3261+	DC	A(16)	result length
00004514	00004560			3262+REA89	DC	A(RE89)	result address
00004518	00000000 00000000			3263+	DS	FD	gap
00004520	00000000 00000000			3264+V1089	DS	XL16	V1 output
00004528	00000000 00000000						
00004530	00000000 00000000			3265+	DS	FD	gap
				3266+*			
00004538				3267+X89	DS	0F	
00004538	E310 5010 0014		00000010	3268+	LGF	R1,V2ADDR	load v2 source
0000453E	E761 0000 0806		00000000	3269+	VL	v22,0(R1)	use v22 to test decoder
00004544	E310 5014 0014		00000014	3270+	LGF	R1,V3ADDR	load v3 source
0000454A	E771 0000 0806		00000000	3271+	VL	v23,0(R1)	use v23 to test decoder
00004550	E766 7000 2EA5			3272+	VMLO	V22,V22,V23,2	test instruction (dest is a source)
00004556	E760 5028 080E		00004520	3273+	VST	V22,V1089	save v1 output
0000455C	07FB			3274+	BR	R11	return
00004560				3275+RE89	DC	0F	xl16 expected result
00004560				3276+	DROP	R5	
00004560	00000000 323C4920			3277	DC	XL16'00000000323C4920 000D1B2B60616771'	result
00004568	000D1B2B 60616771						
00004570	FF020304 05060750			3278	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00004578	090A0B0C 0D0E0F7F						
00004580	FF000000 0000000A			3279	DC	XL16'FF0000000000000A 0101010F0101010F'	v3

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

00004588  0101010F 0101010F
                                                  3280
                                                  3281 * Doubleword
                                                  3282        VRR_C VMLO,3
00004590                                          3283+       DS    OFD
00004590                     00004590             3284+       USING *,R5                  base for test data and test routine
00004590  000045D0                                3285+T90    DC    A(X90)                address of test routine
00004594  005A                                    3286+       DC    H'90'                 test number
00004596  00                                      3287+       DC    X'00'
00004597  03                                      3288+       DC    HL1'3'                m4
00004598  E5D4D3D6 40404040                       3289+       DC    CL8'VMLO'             instruction name
000045A0  00004608                                3290+       DC    A(RE90+16)            address of v2 source
000045A4  00004618                                3291+       DC    A(RE90+32)            address of v3 source
000045A8  00000010                                3292+       DC    A(16)                 result length
000045AC  000045F8                                3293+REA90  DC    A(RE90)               result address
000045B0  00000000 00000000                       3294+       DS    FD                    gap
000045B8  00000000 00000000                       3295+V1090  DS    XL16                  V1 output
000045C0  00000000 00000000
000045C8  00000000 00000000                       3296+       DS    FD                    gap
                                                  3297+*
000045D0                                          3298+X90    DS    OF
000045D0  E310 5010 0014                00000010  3299+       LGF   R1,V2ADDR             load v2 source
000045D6  E761 0000 0806                00000000  3300+       VL    v22,0(R1)             use v22 to test decoder
000045DC  E310 5014 0014                00000014  3301+       LGF   R1,V3ADDR             load v3 source
000045E2  E771 0000 0806                00000000  3302+       VL    v23,0(R1)             use v23 to test decoder
000045E8  E766 7000 3EA5                          3303+       VMLO  V22,V22,V23,3          test instruction (dest is a source)
000045EE  E760 5028 080E                000045B8  3304+       VST   V22,V1090              save v1 output
000045F4  07FB                                    3305+       BR    R11                   return
000045F8                                          3306+RE90   DC    OF                    xl16 expected result
000045F8                                          3307+       DROP  R5
000045F8  00000000 00000C77                       3308        DC    XL16'0000000000000C77 96789F9F4FEDCC24'    result
00004600  96789F9F 4FEDCC24
00004608  FFFFFFFF 00019000                       3309        DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'    v2
00004610  00000038 EEEEEEFA
00004618  FFFFFFFF 00019000                       3310        DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'    v3
00004620  00000038 0EEEEEFA
                                                  3311
                                                  3312        VRR_C VMLO,3
00004628                                          3313+       DS    OFD
00004628                     00004628             3314+       USING *,R5                  base for test data and test routine
00004628  00004668                                3315+T91    DC    A(X91)                address of test routine
0000462C  005B                                    3316+       DC    H'91'                 test number
0000462E  00                                      3317+       DC    X'00'
0000462F  03                                      3318+       DC    HL1'3'                m4
00004630  E5D4D3D6 40404040                       3319+       DC    CL8'VMLO'             instruction name
00004638  000046A0                                3320+       DC    A(RE91+16)            address of v2 source
0000463C  000046B0                                3321+       DC    A(RE91+32)            address of v3 source
00004640  00000010                                3322+       DC    A(16)                 result length
00004644  00004690                                3323+REA91  DC    A(RE91)               result address
00004648  00000000 00000000                       3324+       DS    FD                    gap
00004650  00000000 00000000                       3325+V1091  DS    XL16                  V1 output
00004658  00000000 00000000
00004660  00000000 00000000                       3326+       DS    FD                    gap
                                                  3327+*
00004668                                          3328+X91    DS    OF
00004668  E310 5010 0014                00000010  3329+       LGF   R1,V2ADDR             load v2 source
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  LOC          OBJECT CODE       ADDR1     ADDR2     STMT

0000466E  E761 0000 0806                   00000000  3330+            VL      v22,0(R1)          use v22 to test decoder
00004674  E310 5014 0014                   00000014  3331+            LGF     R1,V3ADDR          load v3 source
0000467A  E771 0000 0806                   00000000  3332+            VL      v23,0(R1)          use v23 to test decoder
00004680  E766 7000 3EA5                             3333+            VMLO    V22,V22,V23,3       test instruction (dest is a source)
00004686  E760 5028 080E                   00004650  3334+            VST     V22,V1091          save v1 output
0000468C  07FB                                       3335+            BR      R11                return
00004690                                             3336+RE91        DC      0F                 xl16 expected result
00004690                                             3337+            DROP    R5
00004690  0051B52F 8692B4F6                          3338             DC      XL16'0051B52F8692B4F6 152B55D498D42101'   result
00004698  152B55D4 98D42101
000046A0  FF020304 05060750                          3339             DC      XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000046A8  090A0B0C 0D0E0F7F
000046B0  01020304 05060750                          3340             DC      XL16'0102030405060750 090A0B780D0E0F7F'   v3
000046B8  090A0B78 0D0E0F7F
                                                     3341
                                                     3342             VRR_C   VMLO,3
000046C0                                             3343+            DS      0FD
000046C0                     000046C0                3344+            USING   *,R5               base for test data and test routine
000046C0  00004700                                   3345+T92         DC      A(X92)             address of test routine
000046C4  005C                                       3346+            DC      H'92'              test number
000046C6  00                                         3347+            DC      X'00'
000046C7  03                                         3348+            DC      HL1'3'             m4
000046C8  E5D4D3D6 40404040                          3349+            DC      CL8'VMLO'          instruction name
000046D0  00004738                                   3350+            DC      A(RE92+16)         address of v2 source
000046D4  00004748                                   3351+            DC      A(RE92+32)         address of v3 source
000046D8  00000010                                   3352+            DC      A(16)              result length
000046DC  00004728                                   3353+REA92       DC      A(RE92)            result address
000046E0  00000000 00000000                          3354+            DS      FD                 gap
000046E8  00000000 00000000                          3355+V1092       DS      XL16               V1 output
000046F0  00000000 00000000
000046F8  00000000 00000000                          3356+            DS      FD                 gap
                                                     3357+*
00004700                                             3358+X92         DS      0F
00004700  E310 5010 0014                   00000010  3359+            LGF     R1,V2ADDR          load v2 source
00004706  E761 0000 0806                   00000000  3360+            VL      v22,0(R1)          use v22 to test decoder
0000470C  E310 5014 0014                   00000014  3361+            LGF     R1,V3ADDR          load v3 source
00004712  E771 0000 0806                   00000000  3362+            VL      v23,0(R1)          use v23 to test decoder
00004718  E766 7000 3EA5                             3363+            VMLO    V22,V22,V23,3       test instruction (dest is a source)
0000471E  E760 5028 080E                   000046E8  3364+            VST     V22,V1092          save v1 output
00004724  07FB                                       3365+            BR      R11                return
00004728                                             3366+RE92        DC      0F                 xl16 expected result
00004728                                             3367+            DROP    R5
00004728  0024558D B838C862                          3368             DC      XL16'0024558DB838C862 B47CD8D5FF5B4941'   result
00004730  B47CD8D5 FF5B4941
00004738  FF020304 05060750                          3369             DC      XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004740  090A0B0C 0D0E0F7F
00004748  00010102 02030328                          3370             DC      XL16'0001010202030328 0405053C0607073F'   v3
00004750  0405053C 0607073F
                                                     3371
                                                     3372             VRR_C   VMLO,3
00004758                                             3373+            DS      0FD
00004758                     00004758                3374+            USING   *,R5               base for test data and test routine
00004758  00004798                                   3375+T93         DC      A(X93)             address of test routine
0000475C  005D                                       3376+            DC      H'93'              test number
0000475E  00                                         3377+            DC      X'00'
0000475F  03                                         3378+            DC      HL1'3'             m4
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004760	E5D4D3D6 40404040			3379+	DC	CL8'VMLO'	instruction name
00004768	000047D0			3380+	DC	A(RE93+16)	address of v2 source
0000476C	000047E0			3381+	DC	A(RE93+32)	address of v3 source
00004770	00000010			3382+	DC	A(16)	result length
00004774	000047C0			3383+REA93	DC	A(RE93)	result address
00004778	00000000 00000000			3384+	DS	FD	gap
00004780	00000000 00000000			3385+V1093	DS	XL16	V1 output
00004788	00000000 00000000						
00004790	00000000 00000000			3386+	DS	FD	gap
				3387+*			
00004798				3388+X93	DS	0F	
00004798	E310 5010 0014		00000010	3389+	LGF	R1,V2ADDR	load v2 source
0000479E	E761 0000 0806		00000000	3390+	VL	v22,0(R1)	use v22 to test decoder
000047A4	E310 5014 0014		00000014	3391+	LGF	R1,V3ADDR	load v3 source
000047AA	E771 0000 0806		00000000	3392+	VL	v23,0(R1)	use v23 to test decoder
000047B0	E766 7000 3EA5			3393+	VMLO	V22,V22,V23,3	test instruction (dest is a source)
000047B6	E760 5028 080E		00004780	3394+	VST	V22,V1093	save v1 output
000047BC	07FB			3395+	BR	R11	return
000047C0				3396+RE93	DC	0F	xl16 expected result
000047C0				3397+	DROP	R5	
000047C0	0009131E A8C3DFFE			3398	DC	XL16'0009131EA8C3DFFE 091C345060616771'	result
000047C8	091C3450 60616771						
000047D0	FF020304 05060750			3399	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
000047D8	090A0B0C 0D0E0F7F						
000047E0	00000000 0000000A			3400	DC	XL16'000000000000000A 0101010F0101010F'	v3
000047E8	0101010F 0101010F						
				3401			
				3402	VRR_C	VMLO,3	
000047F0				3403+	DS	0FD	
000047F0		000047F0		3404+	USING	*,R5	base for test data and test routine
000047F0	00004830			3405+T94	DC	A(X94)	address of test routine
000047F4	005E			3406+	DC	H'94'	test number
000047F6	00			3407+	DC	X'00'	
000047F7	03			3408+	DC	HL1'3'	m4
000047F8	E5D4D3D6 40404040			3409+	DC	CL8'VMLO'	instruction name
00004800	00004868			3410+	DC	A(RE94+16)	address of v2 source
00004804	00004878			3411+	DC	A(RE94+32)	address of v3 source
00004808	00000010			3412+	DC	A(16)	result length
0000480C	00004858			3413+REA94	DC	A(RE94)	result address
00004810	00000000 00000000			3414+	DS	FD	gap
00004818	00000000 00000000			3415+V1094	DS	XL16	V1 output
00004820	00000000 00000000						
00004828	00000000 00000000			3416+	DS	FD	gap
				3417+*			
00004830				3418+X94	DS	0F	
00004830	E310 5010 0014		00000010	3419+	LGF	R1,V2ADDR	load v2 source
00004836	E761 0000 0806		00000000	3420+	VL	v22,0(R1)	use v22 to test decoder
0000483C	E310 5014 0014		00000014	3421+	LGF	R1,V3ADDR	load v3 source
00004842	E771 0000 0806		00000000	3422+	VL	v23,0(R1)	use v23 to test decoder
00004848	E766 7000 3EA5			3423+	VMLO	V22,V22,V23,3	test instruction (dest is a source)
0000484E	E760 5028 080E		00004818	3424+	VST	V22,V1094	save v1 output
00004854	07FB			3425+	BR	R11	return
00004858				3426+RE94	DC	0F	xl16 expected result
00004858				3427+	DROP	R5	
00004858	00000000 00000009			3428	DC	XL16'0000000000000009 F6141E28323C4920'	result
00004860	F6141E28 323C4920						

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   LOC          OBJECT CODE       ADDR1      ADDR2      STMT

00004868  090A0B0C 0D0E0F7F                             3429          DC     XL16'090A0B0C0D0E0F7F FF02030405060750'     v2
00004870  FF020304 05060750
00004878  0101010F 0101010F                             3430          DC     XL16'0101010F0101010F 000000000000000A'     v3
00004880  00000000 0000000A
                                                        3431
                                                        3432 *-------------------------------------------------------------
                                                        3433 *  VME    - Vector Multiply Even
                                                        3434 *-------------------------------------------------------------
                                                        3435 * Byte
                                                        3436          VRR_C VME,0
00004888                                                3437+         DS     0FD
00004888                       00004888                 3438+         USING *,R5                   base for test data and test routine
00004888  000048C8                                      3439+T95      DC     A(X95)                 address of test routine
0000488C  005F                                          3440+         DC     H'95'                  test number
0000488E  00                                            3441+         DC     X'00'
0000488F  00                                            3442+         DC     HL1'0'                 m4
00004890  E5D4C540 40404040                             3443+         DC     CL8'VME'               instruction name
00004898  00004900                                      3444+         DC     A(RE95+16)             address of v2 source
0000489C  00004910                                      3445+         DC     A(RE95+32)             address of v3 source
000048A0  00000010                                      3446+         DC     A(16)                  result length
000048A4  000048F0                                      3447+REA95    DC     A(RE95)                result address
000048A8  00000000 00000000                             3448+         DS     FD                     gap
000048B0  00000000 00000000                             3449+V1095    DS     XL16                   V1 output
000048B8  00000000 00000000
000048C0  00000000 00000000                             3450+         DS     FD                     gap
                                                        3451+*
000048C8                                                3452+X95      DS     0F
000048C8  E310 5010 0014                   00000010     3453+         LGF    R1,V2ADDR              load v2 source
000048CE  E761 0000 0806                   00000000     3454+         VL     v22,0(R1)              use v22 to test decoder
000048D4  E310 5014 0014                   00000014     3455+         LGF    R1,V3ADDR              load v3 source
000048DA  E771 0000 0806                   00000000     3456+         VL     v23,0(R1)              use v23 to test decoder
000048E0  E766 7000 0EA6                                3457+         VME    V22,V22,V23,0           test instruction (dest is a source)
000048E6  E760 5028 080E                   000048B0     3458+         VST    V22,V1095               save v1 output
000048EC  07FB                                          3459+         BR     R11                    return
000048F0                                                3460+RE95     DC     0F                     xl16 expected result
000048F0                                                3461+         DROP   R5
000048F0  00010000 00000000                             3462          DC     XL16'0001000000000000 0C40000000000000'     result
000048F8  0C400000 00000000
00004900  FF000000 00000019                             3463          DC     XL16'FF00000000000019 38000000000000FA'     v2
00004908  38000000 000000FA
00004910  FF000000 00000019                             3464          DC     XL16'FF00000000000019 38000000000000FA'     v3
00004918  38000000 000000FA
                                                        3465
                                                        3466          VRR_C VME,0
00004920                                                3467+         DS     0FD
00004920                       00004920                 3468+         USING *,R5                   base for test data and test routine
00004920  00004960                                      3469+T96      DC     A(X96)                 address of test routine
00004924  0060                                          3470+         DC     H'96'                  test number
00004926  00                                            3471+         DC     X'00'
00004927  00                                            3472+         DC     HL1'0'                 m4
00004928  E5D4C540 40404040                             3473+         DC     CL8'VME'               instruction name
00004930  00004998                                      3474+         DC     A(RE96+16)             address of v2 source
00004934  000049A8                                      3475+         DC     A(RE96+32)             address of v3 source
00004938  00000010                                      3476+         DC     A(16)                  result length
0000493C  00004988                                      3477+REA96    DC     A(RE96)                result address
00004940  00000000 00000000                             3478+         DS     FD                     gap
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004948	00000000 00000000			3479+V1096	DS	XL16	V1 output
00004950	00000000 00000000						
00004958	00000000 00000000			3480+	DS	FD	gap
				3481+*			
00004960				3482+X96	DS	0F	
00004960	E310 5010 0014		00000010	3483+	LGF	R1,V2ADDR	load v2 source
00004966	E761 0000 0806		00000000	3484+	VL	v22,0(R1)	use v22 to test decoder
0000496C	E310 5014 0014		00000014	3485+	LGF	R1,V3ADDR	load v3 source
00004972	E771 0000 0806		00000000	3486+	VL	v23,0(R1)	use v23 to test decoder
00004978	E766 7000 0EA6			3487+	VME	V22,V22,V23,0	test instruction (dest is a source)
0000497E	E760 5028 080E		00004948	3488+	VST	V22,V1096	save v1 output
00004984	07FB			3489+	BR	R11	return
00004988				3490+RE96	DC	0F	xl16 expected result
00004988				3491+	DROP	R5	
00004988	00010009 00190031			3492	DC	XL16'0001000900190031 00510079009C00D2'	result
00004990	00510079 009C00D2						
00004998	FF020304 05060750			3493	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
000049A0	090A0B78 0C0D0EFD						
000049A8	FF020304 05060750			3494	DC	XL16'FF02030405060750 090A0B780D0E0FFD'	v3
000049B0	090A0B78 0D0E0FFD						
				3495			
				3496	VRR_C	VME,0	
000049B8				3497+	DS	0FD	
000049B8		000049B8		3498+	USING	*,R5	base for test data and test routine
000049B8	000049F8			3499+T97	DC	A(X97)	address of test routine
000049BC	0061			3500+	DC	H'97'	test number
000049BE	00			3501+	DC	X'00'	
000049BF	00			3502+	DC	HL1'0'	m4
000049C0	E5D4C540 40404040			3503+	DC	CL8'VME'	instruction name
000049C8	00004A30			3504+	DC	A(RE97+16)	address of v2 source
000049CC	00004A40			3505+	DC	A(RE97+32)	address of v3 source
000049D0	00000010			3506+	DC	A(16)	result length
000049D4	00004A20			3507+REA97	DC	A(RE97)	result address
000049D8	00000000 00000000			3508+	DS	FD	gap
000049E0	00000000 00000000			3509+V1097	DS	XL16	V1 output
000049E8	00000000 00000000						
000049F0	00000000 00000000			3510+	DS	FD	gap
				3511+*			
000049F8				3512+X97	DS	0F	
000049F8	E310 5010 0014		00000010	3513+	LGF	R1,V2ADDR	load v2 source
000049FE	E761 0000 0806		00000000	3514+	VL	v22,0(R1)	use v22 to test decoder
00004A04	E310 5014 0014		00000014	3515+	LGF	R1,V3ADDR	load v3 source
00004A0A	E771 0000 0806		00000000	3516+	VL	v23,0(R1)	use v23 to test decoder
00004A10	E766 7000 0EA6			3517+	VME	V22,V22,V23,0	test instruction (dest is a source)
00004A16	E760 5028 080E		000049E0	3518+	VST	V22,V1097	save v1 output
00004A1C	07FB			3519+	BR	R11	return
00004A20				3520+RE97	DC	0F	xl16 expected result
00004A20				3521+	DROP	R5	
00004A20	00010003 000A0015			3522	DC	XL16'00010003000A0015 0024003700480062'	result
00004A28	00240037 00480062						
00004A30	FF020304 05060750			3523	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00004A38	090A0B78 0C0D0EFD						
00004A40	FF010102 02030328			3524	DC	XL16'FF01010202030328 0405053C060707FE'	v3
00004A48	0405053C 060707FE						
				3525			
				3526	VRR_C	VME,0	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004A50				3527+	DS	0FD	
00004A50		00004A50		3528+	USING	*,R5	base for test data and test routine
00004A50	00004A90			3529+T98	DC	A(X98)	address of test routine
00004A54	0062			3530+	DC	H'98'	test number
00004A56	00			3531+	DC	X'00'	
00004A57	00			3532+	DC	HL1'0'	m4
00004A58	E5D4C540 40404040			3533+	DC	CL8'VME'	instruction name
00004A60	00004AC8			3534+	DC	A(RE98+16)	address of v2 source
00004A64	00004AD8			3535+	DC	A(RE98+32)	address of v3 source
00004A68	00000010			3536+	DC	A(16)	result length
00004A6C	00004AB8			3537+REA98	DC	A(RE98)	result address
00004A70	00000000 00000000			3538+	DS	FD	gap
00004A78	00000000 00000000			3539+V1098	DS	XL16	V1 output
00004A80	00000000 00000000						
00004A88	00000000 00000000			3540+	DS	FD	gap
				3541+*			
00004A90				3542+X98	DS	0F	
00004A90	E310 5010 0014		00000010	3543+	LGF	R1,V2ADDR	load v2 source
00004A96	E761 0000 0806		00000000	3544+	VL	v22,0(R1)	use v22 to test decoder
00004A9C	E310 5014 0014		00000014	3545+	LGF	R1,V3ADDR	load v3 source
00004AA2	E771 0000 0806		00000000	3546+	VL	v23,0(R1)	use v23 to test decoder
00004AA8	E766 7000 0EA6			3547+	VME	V22,V22,V23,0	test instruction (dest is a source)
00004AAE	E760 5028 080E		00004A78	3548+	VST	V22,V1098	save v1 output
00004AB4	07FB			3549+	BR	R11	return
00004AB8				3550+RE98	DC	0F	xl16 expected result
00004AB8				3551+	DROP	R5	
00004AB8	00010000 00000000			3552	DC	XL16'0001000000000000 0009000B000C000E'	result
00004AC0	0009000B 000C000E						
00004AC8	FF020304 05060750			3553	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00004AD0	090A0B78 0C0D0EFD						
00004AD8	FF000000 0000000A			3554	DC	XL16'FF0000000000000A 0101010F010101FF'	v3
00004AE0	0101010F 010101FF						
				3555			
				3556 * Halfword			
				3557	VRR_C	VME,1	
00004AE8				3558+	DS	0FD	
00004AE8		00004AE8		3559+	USING	*,R5	base for test data and test routine
00004AE8	00004B28			3560+T99	DC	A(X99)	address of test routine
00004AEC	0063			3561+	DC	H'99'	test number
00004AEE	00			3562+	DC	X'00'	
00004AEF	01			3563+	DC	HL1'1'	m4
00004AF0	E5D4C540 40404040			3564+	DC	CL8'VME'	instruction name
00004AF8	00004B60			3565+	DC	A(RE99+16)	address of v2 source
00004AFC	00004B70			3566+	DC	A(RE99+32)	address of v3 source
00004B00	00000010			3567+	DC	A(16)	result length
00004B04	00004B50			3568+REA99	DC	A(RE99)	result address
00004B08	00000000 00000000			3569+	DS	FD	gap
00004B10	00000000 00000000			3570+V1099	DS	XL16	V1 output
00004B18	00000000 00000000						
00004B20	00000000 00000000			3571+	DS	FD	gap
				3572+*			
00004B28				3573+X99	DS	0F	
00004B28	E310 5010 0014		00000010	3574+	LGF	R1,V2ADDR	load v2 source
00004B2E	E761 0000 0806		00000000	3575+	VL	v22,0(R1)	use v22 to test decoder
00004B34	E310 5014 0014		00000014	3576+	LGF	R1,V3ADDR	load v3 source
00004B3A	E771 0000 0806		00000000	3577+	VL	v23,0(R1)	use v23 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004B40	E766 7000 1EA6			3578+	VME	V22,V22,V23,1	test instruction (dest is a source)
00004B46	E760 5028 080E		00004B10	3579+	VST	V22,V1099	save v1 output
00004B4C	07FB			3580+	BR	R11	return
00004B50				3581+RE99	DC	0F	xl16 expected result
00004B50				3582+	DROP	R5	
00004B50	00000001 00000000			3583	DC	XL16'0000000100000000 00000C40F8000000'	result
00004B58	00000C40 F8000000						
00004B60	FFFF0000 00000019			3584	DC	XL16'FFFF000000000019 003800001000EEFA'	v2
00004B68	00380000 1000EEFA						
00004B70	FFFF0000 00000019			3585	DC	XL16'FFFF000000000019 003800038000EEFA'	v3
00004B78	00380003 8000EEFA						
				3586			
				3587	VRR_C	VME,1	
00004B80				3588+	DS	0FD	
00004B80		00004B80		3589+	USING	*,R5	base for test data and test routine
00004B80	00004BC0			3590+T100	DC	A(X100)	address of test routine
00004B84	0064			3591+	DC	H'100'	test number
00004B86	00			3592+	DC	X'00'	
00004B87	01			3593+	DC	HL1'1'	m4
00004B88	E5D4C540 40404040			3594+	DC	CL8'VME'	instruction name
00004B90	00004BF8			3595+	DC	A(RE100+16)	address of v2 source
00004B94	00004C08			3596+	DC	A(RE100+32)	address of v3 source
00004B98	00000010			3597+	DC	A(16)	result length
00004B9C	00004BE8			3598+REA100	DC	A(RE100)	result address
00004BA0	00000000 00000000			3599+	DS	FD	gap
00004BA8	00000000 00000000			3600+V10100	DS	XL16	V1 output
00004BB0	00000000 00000000						
00004BB8	00000000 00000000			3601+	DS	FD	gap
				3602+*			
00004BC0				3603+X100	DS	0F	
00004BC0	E310 5010 0014		00000010	3604+	LGF	R1,V2ADDR	load v2 source
00004BC6	E761 0000 0806		00000000	3605+	VL	v22,0(R1)	use v22 to test decoder
00004BCC	E310 5014 0014		00000014	3606+	LGF	R1,V3ADDR	load v3 source
00004BD2	E771 0000 0806		00000000	3607+	VL	v23,0(R1)	use v23 to test decoder
00004BD8	E766 7000 1EA6			3608+	VME	V22,V22,V23,1	test instruction (dest is a source)
00004BDE	E760 5028 080E		00004BA8	3609+	VST	V22,V10100	save v1 output
00004BE4	07FB			3610+	BR	R11	return
00004BE8				3611+RE100	DC	0F	xl16 expected result
00004BE8				3612+	DROP	R5	
00004BE8	0000FC04 00193C24			3613	DC	XL16'0000FC0400193C24 0051B464009D51B6'	result
00004BF0	0051B464 009D51B6						
00004BF8	FF020304 05060750			3614	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00004C00	090A0B78 0C0D0EFD						
00004C08	FF020304 05060750			3615	DC	XL16'FF02030405060750 090A0B780D0E0FFD'	v3
00004C10	090A0B78 0D0E0FFD						
				3616			
				3617	VRR_C	VME,1	
00004C18				3618+	DS	0FD	
00004C18		00004C18		3619+	USING	*,R5	base for test data and test routine
00004C18	00004C58			3620+T101	DC	A(X101)	address of test routine
00004C1C	0065			3621+	DC	H'101'	test number
00004C1E	00			3622+	DC	X'00'	
00004C1F	01			3623+	DC	HL1'1'	m4
00004C20	E5D4C540 40404040			3624+	DC	CL8'VME'	instruction name
00004C28	00004C90			3625+	DC	A(RE101+16)	address of v2 source
00004C2C	00004CA0			3626+	DC	A(RE101+32)	address of v3 source

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  LOC         OBJECT CODE        ADDR1      ADDR2     STMT

00004C30   00000010                                  3627+        DC      A(16)              result length
00004C34   00004C80                                  3628+REA101  DC      A(RE101)           result address
00004C38   00000000 00000000                         3629+        DS      FD                 gap
00004C40   00000000 00000000                         3630+V10101  DS      XL16               V1 output
00004C48   00000000 00000000
00004C50   00000000 00000000                         3631+        DS      FD                 gap
                                                     3632+*
00004C58                                             3633+X101    DS      0F
00004C58   E310 5010 0014                  00000010  3634+        LGF     R1,V2ADDR          load v2 source
00004C5E   E761 0000 0806                  00000000  3635+        VL      v22,0(R1)          use v22 to test decoder
00004C64   E310 5014 0014                  00000014  3636+        LGF     R1,V3ADDR          load v3 source
00004C6A   E771 0000 0806                  00000000  3637+        VL      v23,0(R1)          use v23 to test decoder
00004C70   E766 7000 1EA6                            3638+        VME     V22,V22,V23,1       test instruction (dest is a source)
00004C76   E760 5028 080E                  00004C40  3639+        VST     V22,V10101          save v1 output
00004C7C   07FB                                      3640+        BR      R11                return
00004C80                                             3641+RE101   DC      0F                 xl16 expected result
00004C80                                             3642+        DROP    R5
00004C80   0000FD02 000A1B12                         3643         DC      XL16'0000FD02000A1B12 002455320048A25B'   result
00004C88   00245532 0048A25B
00004C90   FF020304 05060750                         3644         DC      XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00004C98   090A0B78 0C0D0EFD
00004CA0   FF010102 02030328                         3645         DC      XL16'FF01010202030328 0405053C060707FE'   v3
00004CA8   0405053C 060707FE
                                                     3646
                                                     3647         VRR_C   VME,1
00004CB0                                             3648+        DS      0FD
00004CB0                         00004CB0            3649+        USING   *,R5               base for test data and test routine
00004CB0   00004CF0                                  3650+T102    DC      A(X102)            address of test routine
00004CB4   0066                                      3651+        DC      H'102'             test number
00004CB6   00                                        3652+        DC      X'00'
00004CB7   01                                        3653+        DC      HL1'1'             m4
00004CB8   E5D4C540 40404040                         3654+        DC      CL8'VME'           instruction name
00004CC0   00004D28                                  3655+        DC      A(RE102+16)        address of v2 source
00004CC4   00004D38                                  3656+        DC      A(RE102+32)        address of v3 source
00004CC8   00000010                                  3657+        DC      A(16)              result length
00004CCC   00004D18                                  3658+REA102  DC      A(RE102)           result address
00004CD0   00000000 00000000                         3659+        DS      FD                 gap
00004CD8   00000000 00000000                         3660+V10102  DS      XL16               V1 output
00004CE0   00000000 00000000
00004CE8   00000000 00000000                         3661+        DS      FD                 gap
                                                     3662+*
00004CF0                                             3663+X102    DS      0F
00004CF0   E310 5010 0014                  00000010  3664+        LGF     R1,V2ADDR          load v2 source
00004CF6   E761 0000 0806                  00000000  3665+        VL      v22,0(R1)          use v22 to test decoder
00004CFC   E310 5014 0014                  00000014  3666+        LGF     R1,V3ADDR          load v3 source
00004D02   E771 0000 0806                  00000000  3667+        VL      v23,0(R1)          use v23 to test decoder
00004D08   E766 7000 1EA6                            3668+        VME     V22,V22,V23,1       test instruction (dest is a source)
00004D0E   E760 5028 080E                  00004CD8  3669+        VST     V22,V10102          save v1 output
00004D14   07FB                                      3670+        BR      R11                return
00004D18                                             3671+RE102   DC      0F                 xl16 expected result
00004D18                                             3672+        DROP    R5
00004D18   0000FE00 00000000                         3673         DC      XL16'0000FE0000000000 0009130A000C190D'   result
00004D20   0009130A 000C190D
00004D28   FF020304 05060750                         3674         DC      XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00004D30   090A0B78 0C0D0EFD
00004D38   FF000000 0000000A                         3675         DC      XL16'FF0000000000000A 0101010F010101FF'   v3
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004D40	0101010F 010101FF						
				3676			
				3677	* Word		
				3678		VRR_C	VME,2
00004D48				3679+	DS	0FD	
00004D48		00004D48		3680+	USING	*,R5	base for test data and test routine
00004D48	00004D88			3681+T103	DC	A(X103)	address of test routine
00004D4C	0067			3682+	DC	H'103'	test number
00004D4E	00			3683+	DC	X'00'	
00004D4F	02			3684+	DC	HL1'2'	m4
00004D50	E5D4C540 40404040			3685+	DC	CL8'VME'	instruction name
00004D58	00004DC0			3686+	DC	A(RE103+16)	address of v2 source
00004D5C	00004DD0			3687+	DC	A(RE103+32)	address of v3 source
00004D60	00000010			3688+	DC	A(16)	result length
00004D64	00004DB0			3689+REA103	DC	A(RE103)	result address
00004D68	00000000 00000000			3690+	DS	FD	gap
00004D70	00000000 00000000			3691+V10103	DS	XL16	V1 output
00004D78	00000000 00000000						
00004D80	00000000 00000000			3692+	DS	FD	gap
				3693+*			
00004D88				3694+X103	DS	0F	
00004D88	E310 5010 0014		00000010	3695+	LGF	R1,V2ADDR	load v2 source
00004D8E	E761 0000 0806		00000000	3696+	VL	v22,0(R1)	use v22 to test decoder
00004D94	E310 5014 0014		00000014	3697+	LGF	R1,V3ADDR	load v3 source
00004D9A	E771 0000 0806		00000000	3698+	VL	v23,0(R1)	use v23 to test decoder
00004DA0	E766 7000 2EA6			3699+	VME	V22,V22,V23,2	test instruction (dest is a source)
00004DA6	E760 5028 080E		00004D70	3700+	VST	V22,V10103	save v1 output
00004DAC	07FB			3701+	BR	R11	return
00004DB0				3702+RE103	DC	0F	xl16 expected result
00004DB0				3703+	DROP	R5	
00004DB0	00000000 00000001			3704	DC	XL16'0000000000000001 0000000000000C40'	result
00004DB8	00000000 00000C40						
00004DC0	FFFFFFFF 00019000			3705	DC	XL16'FFFFFFFF00019000 00000038EEEEEEFA'	v2
00004DC8	00000038 EEEEEEFA						
00004DD0	FFFFFFFF 00019000			3706	DC	XL16'FFFFFFFF00019000 000000380EEEEEFA'	v3
00004DD8	00000038 0EEEEEFA						
				3707			
				3708		VRR_C	VME,2
00004DE0				3709+	DS	0FD	
00004DE0		00004DE0		3710+	USING	*,R5	base for test data and test routine
00004DE0	00004E20			3711+T104	DC	A(X104)	address of test routine
00004DE4	0068			3712+	DC	H'104'	test number
00004DE6	00			3713+	DC	X'00'	
00004DE7	02			3714+	DC	HL1'2'	m4
00004DE8	E5D4C540 40404040			3715+	DC	CL8'VME'	instruction name
00004DF0	00004E58			3716+	DC	A(RE104+16)	address of v2 source
00004DF4	00004E68			3717+	DC	A(RE104+32)	address of v3 source
00004DF8	00000010			3718+	DC	A(16)	result length
00004DFC	00004E48			3719+REA104	DC	A(RE104)	result address
00004E00	00000000 00000000			3720+	DS	FD	gap
00004E08	00000000 00000000			3721+V10104	DS	XL16	V1 output
00004E10	00000000 00000000						
00004E18	00000000 00000000			3722+	DS	FD	gap
				3723+*			
00004E20				3724+X104	DS	0F	
00004E20	E310 5010 0014		00000010	3725+	LGF	R1,V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004E26	E761 0000 0806		00000000	3726+	VL	v22,0(R1)	use v22 to test decoder
00004E2C	E310 5014 0014		00000014	3727+	LGF	R1,V3ADDR	load v3 source
00004E32	E771 0000 0806		00000000	3728+	VL	v23,0(R1)	use v23 to test decoder
00004E38	E766 7000 2EA6			3729+	VME	V22,V22,V23,2	test instruction (dest is a source)
00004E3E	E760 5028 080E		00004E08	3730+	VST	V22,V10104	save v1 output
00004E44	07FB			3731+	BR	R11	return
00004E48				3732+RE104	DC	0F	xl16 expected result
00004E48				3733+	DROP	R5	
00004E48	FFFF0004 0C191810			3734	DC	XL16'FFFF00040C191810 0051B52F85A6B1A0'	result
00004E50	0051B52F 85A6B1A0						
00004E58	FF020304 05060750			3735	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00004E60	090A0B0C 0D0E0F7F						
00004E68	01020304 05060750			3736	DC	XL16'0102030405060750 090A0B780D0E0F7F'	v3
00004E70	090A0B78 0D0E0F7F						
				3737			
				3738	VRR_C	VME,2	
00004E78				3739+	DS	0FD	
00004E78		00004E78		3740+	USING	*,R5	base for test data and test routine
00004E78	00004EB8			3741+T105	DC	A(X105)	address of test routine
00004E7C	0069			3742+	DC	H'105'	test number
00004E7E	00			3743+	DC	X'00'	
00004E7F	02			3744+	DC	HL1'2'	m4
00004E80	E5D4C540 40404040			3745+	DC	CL8'VME'	instruction name
00004E88	00004EF0			3746+	DC	A(RE105+16)	address of v2 source
00004E8C	00004F00			3747+	DC	A(RE105+32)	address of v3 source
00004E90	00000010			3748+	DC	A(16)	result length
00004E94	00004EE0			3749+REA105	DC	A(RE105)	result address
00004E98	00000000 00000000			3750+	DS	FD	gap
00004EA0	00000000 00000000			3751+V10105	DS	XL16	V1 output
00004EA8	00000000 00000000						
00004EB0	00000000 00000000			3752+	DS	FD	gap
				3753+*			
00004EB8				3754+X105	DS	0F	
00004EB8	E310 5010 0014		00000010	3755+	LGF	R1,V2ADDR	load v2 source
00004EBE	E761 0000 0806		00000000	3756+	VL	v22,0(R1)	use v22 to test decoder
00004EC4	E310 5014 0014		00000014	3757+	LGF	R1,V3ADDR	load v3 source
00004ECA	E771 0000 0806		00000000	3758+	VL	v23,0(R1)	use v23 to test decoder
00004ED0	E766 7000 2EA6			3759+	VME	V22,V22,V23,2	test instruction (dest is a source)
00004ED6	E760 5028 080E		00004EA0	3760+	VST	V22,V10105	save v1 output
00004EDC	07FB			3761+	BR	R11	return
00004EE0				3762+RE105	DC	0F	xl16 expected result
00004EE0				3763+	DROP	R5	
00004EE0	FFFFFF01 030B0A08			3764	DC	XL16'FFFFFF01030B0A08 0024558DB7CDD2D0'	result
00004EE8	0024558D B7CDD2D0						
00004EF0	FF020304 05060750			3765	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00004EF8	090A0B0C 0D0E0F7F						
00004F00	00010102 02030328			3766	DC	XL16'0001010202030328 0405053C0607073F'	v3
00004F08	0405053C 0607073F						
				3767			
				3768	VRR_C	VME,2	
00004F10				3769+	DS	0FD	
00004F10		00004F10		3770+	USING	*,R5	base for test data and test routine
00004F10	00004F50			3771+T106	DC	A(X106)	address of test routine
00004F14	006A			3772+	DC	H'106'	test number
00004F16	00			3773+	DC	X'00'	
00004F17	02			3774+	DC	HL1'2'	m4

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004F18	E5D4C540 40404040			3775+	DC	CL8'VME'	instruction name
00004F20	00004F88			3776+	DC	A(RE106+16)	address of v2 source
00004F24	00004F98			3777+	DC	A(RE106+32)	address of v3 source
00004F28	00000010			3778+	DC	A(16)	result length
00004F2C	00004F78			3779+REA106	DC	A(RE106)	result address
00004F30	00000000 00000000			3780+	DS	FD	gap
00004F38	00000000 00000000			3781+V10106	DS	XL16	V1 output
00004F40	00000000 00000000						
00004F48	00000000 00000000			3782+	DS	FD	gap
				3783+*			
00004F50				3784+X106	DS	0F	
00004F50	E310 5010 0014		00000010	3785+	LGF	R1,V2ADDR	load v2 source
00004F56	E761 0000 0806		00000000	3786+	VL	v22,0(R1)	use v22 to test decoder
00004F5C	E310 5014 0014		00000014	3787+	LGF	R1,V3ADDR	load v3 source
00004F62	E771 0000 0806		00000000	3788+	VL	v23,0(R1)	use v23 to test decoder
00004F68	E766 7000 2EA6			3789+	VME	V22,V22,V23,2	test instruction (dest is a source)
00004F6E	E760 5028 080E		00004F38	3790+	VST	V22,V10106	save v1 output
00004F74	07FB			3791+	BR	R11	return
00004F78				3792+RE106	DC	0F	xl16 expected result
00004F78				3793+	DROP	R5	
00004F78	00000000 00000000			3794	DC	XL16'0000000000000000 0009131EA8ADB1B4'	result
00004F80	0009131E A8ADB1B4						
00004F88	FF020304 05060750			3795	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00004F90	090A0B0C 0D0E0F7F						
00004F98	00000000 0000000A			3796	DC	XL16'000000000000000A 0101010F0101010F'	v3
00004FA0	0101010F 0101010F						
				3797			
				3798 * Doubleword			
				3799	VRR_C	VME,3	
00004FA8				3800+	DS	0FD	
00004FA8		00004FA8		3801+	USING	*,R5	base for test data and test routine
00004FA8	00004FE8			3802+T107	DC	A(X107)	address of test routine
00004FAC	006B			3803+	DC	H'107'	test number
00004FAE	00			3804+	DC	X'00'	
00004FAF	03			3805+	DC	HL1'3'	m4
00004FB0	E5D4C540 40404040			3806+	DC	CL8'VME'	instruction name
00004FB8	00005020			3807+	DC	A(RE107+16)	address of v2 source
00004FBC	00005030			3808+	DC	A(RE107+32)	address of v3 source
00004FC0	00000010			3809+	DC	A(16)	result length
00004FC4	00005010			3810+REA107	DC	A(RE107)	result address
00004FC8	00000000 00000000			3811+	DS	FD	gap
00004FD0	00000000 00000000			3812+V10107	DS	XL16	V1 output
00004FD8	00000000 00000000						
00004FE0	00000000 00000000			3813+	DS	FD	gap
				3814+*			
00004FE8				3815+X107	DS	0F	
00004FE8	E310 5010 0014		00000010	3816+	LGF	R1,V2ADDR	load v2 source
00004FEE	E761 0000 0806		00000000	3817+	VL	v22,0(R1)	use v22 to test decoder
00004FF4	E310 5014 0014		00000014	3818+	LGF	R1,V3ADDR	load v3 source
00004FFA	E771 0000 0806		00000000	3819+	VL	v23,0(R1)	use v23 to test decoder
00005000	E766 7000 3EA6			3820+	VME	V22,V22,V23,3	test instruction (dest is a source)
00005006	E760 5028 080E		00004FD0	3821+	VST	V22,V10107	save v1 output
0000500C	07FB			3822+	BR	R11	return
00005010				3823+RE107	DC	0F	xl16 expected result
00005010				3824+	DROP	R5	
00005010	00000000 00000000			3825	DC	XL16'0000000000000000 FFFCE00271000000'	result

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  LOC          OBJECT CODE      ADDR1      ADDR2      STMT

00005018  FFFCE002 71000000
00005020  FFFFFFFF 00019000                           3826           DC      XL16'FFFFFFFF00019000 00000038EEEEEEFA'      v2
00005028  00000038 EEEEEEFA
00005030  FFFFFFFF 00019000                           3827           DC      XL16'FFFFFFFF00019000 000000380EEEEEFA'      v3
00005038  00000038 0EEEEEFA
                                                      3828
                                                      3829           VRR_C   VME,3
00005040                                              3830+          DS      0FD
00005040                       00005040               3831+          USING   *,R5                  base for test data and test routine
00005040  00005080                                    3832+T108      DC      A(X108)               address of test routine
00005044  006C                                        3833+          DC      H'108'                test number
00005046  00                                          3834+          DC      X'00'
00005047  03                                          3835+          DC      HL1'3'                m4
00005048  E5D4C540 40404040                           3836+          DC      CL8'VME'              instruction name
00005050  000050B8                                    3837+          DC      A(RE108+16)           address of v2 source
00005054  000050C8                                    3838+          DC      A(RE108+32)           address of v3 source
00005058  00000010                                    3839+          DC      A(16)                 result length
0000505C  000050A8                                    3840+REA108    DC      A(RE108)              result address
00005060  00000000 00000000                           3841+          DS      FD                    gap
00005068  00000000 00000000                           3842+V10108    DS      XL16                  V1 output
00005070  00000000 00000000
00005078  00000000 00000000                           3843+          DS      FD                    gap
                                                      3844+*
00005080                                              3845+X108      DS      0F
00005080  E310 5010 0014                  00000010    3846+          LGF     R1,V2ADDR             load v2 source
00005086  E761 0000 0806                  00000000    3847+          VL      v22,0(R1)             use v22 to test decoder
0000508C  E310 5014 0014                  00000014    3848+          LGF     R1,V3ADDR             load v3 source
00005092  E771 0000 0806                  00000000    3849+          VL      v23,0(R1)             use v23 to test decoder
00005098  E766 7000 3EA6                              3850+          VME     V22,V22,V23,3          test instruction (dest is a source)
0000509E  E760 5028 080E                  00005068    3851+          VST     V22,V10108             save v1 output
000050A4  07FB                                        3852+          BR      R11                   return
000050A8                                              3853+RE108     DC      0F                    xl16 expected result
000050A8                                              3854+          DROP    R5
000050A8  FFFF0004 0C192C46                           3855           DC      XL16'FFFF00040C192C46 69B556ED77F57900'      result
000050B0  69B556ED 77F57900
000050B8  FF020304 05060750                           3856           DC      XL16'FF02030405060750 090A0B0C0D0E0F7F'      v2
000050C0  090A0B0C 0D0E0F7F
000050C8  01020304 05060750                           3857           DC      XL16'0102030405060750 090A0B780D0E0F7F'      v3
000050D0  090A0B78 0D0E0F7F
                                                      3858
                                                      3859           VRR_C   VME,3
000050D8                                              3860+          DS      0FD
000050D8                       000050D8               3861+          USING   *,R5                  base for test data and test routine
000050D8  00005118                                    3862+T109      DC      A(X109)               address of test routine
000050DC  006D                                        3863+          DC      H'109'                test number
000050DE  00                                          3864+          DC      X'00'
000050DF  03                                          3865+          DC      HL1'3'                m4
000050E0  E5D4C540 40404040                           3866+          DC      CL8'VME'              instruction name
000050E8  00005150                                    3867+          DC      A(RE109+16)           address of v2 source
000050EC  00005160                                    3868+          DC      A(RE109+32)           address of v3 source
000050F0  00000010                                    3869+          DC      A(16)                 result length
000050F4  00005140                                    3870+REA109    DC      A(RE109)              result address
000050F8  00000000 00000000                           3871+          DS      FD                    gap
00005100  00000000 00000000                           3872+V10109    DS      XL16                  V1 output
00005108  00000000 00000000
00005110  00000000 00000000                           3873+          DS      FD                    gap
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				3874+*			
00005118				3875+X109	DS	0F	
00005118	E310 5010 0014		00000010	3876+	LGF	R1,V2ADDR	load v2 source
0000511E	E761 0000 0806		00000000	3877+	VL	v22,0(R1)	use v22 to test decoder
00005124	E310 5014 0014		00000014	3878+	LGF	R1,V3ADDR	load v3 source
0000512A	E771 0000 0806		00000000	3879+	VL	v23,0(R1)	use v23 to test decoder
00005130	E766 7000 3EA6			3880+	VME	V22,V22,V23,3	test instruction (dest is a source)
00005136	E760 5028 080E		00005100	3881+	VST	V22,V10109	save v1 output
0000513C	07FB			3882+	BR	R11	return
00005140				3883+RE109	DC	0F	xl16 expected result
00005140				3884+	DROP	R5	
00005140	FFFFFF01 0309101C			3885	DC	XL16'FFFFFF010309101C 06D2FE7090F71480'	result
00005148	06D2FE70 90F71480						
00005150	FF020304 05060750			3886	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00005158	090A0B0C 0D0E0F7F						
00005160	00010102 02030328			3887	DC	XL16'0001010202030328 0405053C0607073F'	v3
00005168	0405053C 0607073F						
				3888			
				3889	VRR_C	VME,3	
00005170				3890+	DS	0FD	
00005170		00005170		3891+	USING	*,R5	base for test data and test routine
00005170	000051B0			3892+T110	DC	A(X110)	address of test routine
00005174	006E			3893+	DC	H'110'	test number
00005176	00			3894+	DC	X'00'	
00005177	03			3895+	DC	HL1'3'	m4
00005178	E5D4C540 40404040			3896+	DC	CL8'VME'	instruction name
00005180	000051E8			3897+	DC	A(RE110+16)	address of v2 source
00005184	000051F8			3898+	DC	A(RE110+32)	address of v3 source
00005188	00000010			3899+	DC	A(16)	result length
0000518C	000051D8			3900+REA110	DC	A(RE110)	result address
00005190	00000000 00000000			3901+	DS	FD	gap
00005198	00000000 00000000			3902+V10110	DS	XL16	V1 output
000051A0	00000000 00000000						
000051A8	00000000 00000000			3903+	DS	FD	gap
				3904+*			
000051B0				3905+X110	DS	0F	
000051B0	E310 5010 0014		00000010	3906+	LGF	R1,V2ADDR	load v2 source
000051B6	E761 0000 0806		00000000	3907+	VL	v22,0(R1)	use v22 to test decoder
000051BC	E310 5014 0014		00000014	3908+	LGF	R1,V3ADDR	load v3 source
000051C2	E771 0000 0806		00000000	3909+	VL	v23,0(R1)	use v23 to test decoder
000051C8	E766 7000 3EA6			3910+	VME	V22,V22,V23,3	test instruction (dest is a source)
000051CE	E760 5028 080E		00005198	3911+	VST	V22,V10110	save v1 output
000051D4	07FB			3912+	BR	R11	return
000051D8				3913+RE110	DC	0F	xl16 expected result
000051D8				3914+	DROP	R5	
000051D8	FFFFFFFF FFFFFFFF			3915	DC	XL16'FFFFFFFFFFFFFFFF F6141E28323C4920'	result
000051E0	F6141E28 323C4920						
000051E8	FF020304 05060750			3916	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
000051F0	090A0B0C 0D0E0F7F						
000051F8	00000000 0000000A			3917	DC	XL16'000000000000000A 0101010F0101010F'	v3
00005200	0101010F 0101010F						
				3918			
				3919	VRR_C	VME,3	
00005208				3920+	DS	0FD	
00005208		00005208		3921+	USING	*,R5	base for test data and test routine
00005208	00005248			3922+T111	DC	A(X111)	address of test routine

```
  LOC        OBJECT CODE       ADDR1    ADDR2    STMT

0000520C  006F                                  3923+         DC    H'111'             test number
0000520E  00                                    3924+         DC    X'00'
0000520F  03                                    3925+         DC    HL1'3'             m4
00005210  E5D4C540 40404040                     3926+         DC    CL8'VME'           instruction name
00005218  00005280                              3927+         DC    A(RE111+16)        address of v2 source
0000521C  00005290                              3928+         DC    A(RE111+32)        address of v3 source
00005220  00000010                              3929+         DC    A(16)              result length
00005224  00005270                              3930+REA111   DC    A(RE111)           result address
00005228  00000000 00000000                     3931+         DS    FD                 gap
00005230  00000000 00000000                     3932+V10111   DS    XL16               V1 output
00005238  00000000 00000000
00005240  00000000 00000000                     3933+         DS    FD                 gap
                                                3934+*
00005248                                        3935+X111     DS    0F
00005248  E310 5010 0014                00000010 3936+        LGF   R1,V2ADDR          load v2 source
0000524E  E761 0000 0806                00000000 3937+        VL    v22,0(R1)          use v22 to test decoder
00005254  E310 5014 0014                00000014 3938+        LGF   R1,V3ADDR          load v3 source
0000525A  E771 0000 0806                00000000 3939+        VL    v23,0(R1)          use v23 to test decoder
00005260  E766 7000 3EA6                         3940+        VME   V22,V22,V23,3       test instruction (dest is a source)
00005266  E760 5028 080E                00005230 3941+        VST   V22,V10111          save v1 output
0000526C  07FB                                   3942+        BR    R11                return
00005270                                         3943+RE111   DC    0F                 xl16 expected result
00005270                                         3944+        DROP  R5
00005270  0009131E A8C3DFFE                      3945         DC    XL16'0009131EA8C3DFFE 091C345060616771'    result
00005278  091C3450 60616771
00005280  090A0B0C 0D0E0F7F                      3946         DC    XL16'090A0B0C0D0E0F7F FF02030405060750'    v2
00005288  FF020304 05060750
00005290  0101010F 0101010F                      3947         DC    XL16'0101010F0101010F 000000000000000A'    v3
00005298  00000000 0000000A
                                                 3948
                                                 3949 *-------------------------------------------------------------------------
                                                 3950 *   VMO     - Vector Multiply Odd
                                                 3951 *-------------------------------------------------------------------------
                                                 3952 * Byte
                                                 3953          VRR_C VMO,0
000052A0                                         3954+        DS    0FD
000052A0                     000052A0            3955+        USING *,R5               base for test data and test routine
000052A0  000052E0                               3956+T112    DC    A(X112)            address of test routine
000052A4  0070                                   3957+        DC    H'112'             test number
000052A6  00                                     3958+        DC    X'00'
000052A7  00                                     3959+        DC    HL1'0'             m4
000052A8  E5D4D640 40404040                      3960+        DC    CL8'VMO'           instruction name
000052B0  00005318                               3961+        DC    A(RE112+16)        address of v2 source
000052B4  00005328                               3962+        DC    A(RE112+32)        address of v3 source
000052B8  00000010                               3963+        DC    A(16)              result length
000052BC  00005308                               3964+REA112  DC    A(RE112)           result address
000052C0  00000000 00000000                      3965+        DS    FD                 gap
000052C8  00000000 00000000                      3966+V10112  DS    XL16               V1 output
000052D0  00000000 00000000
000052D8  00000000 00000000                      3967+        DS    FD                 gap
                                                 3968+*
000052E0                                         3969+X112    DS    0F
000052E0  E310 5010 0014                00000010 3970+        LGF   R1,V2ADDR          load v2 source
000052E6  E761 0000 0806                00000000 3971+        VL    v22,0(R1)          use v22 to test decoder
000052EC  E310 5014 0014                00000014 3972+        LGF   R1,V3ADDR          load v3 source
000052F2  E771 0000 0806                00000000 3973+        VL    v23,0(R1)          use v23 to test decoder
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000052F8	E766 7000 0EA7			3974+	VMO	V22,V22,V23,0	test instruction (dest is a source)
000052FE	E760 5028 080E		000052C8	3975+	VST	V22,V10112	save v1 output
00005304	07FB			3976+	BR	R11	return
00005308				3977+RE112	DC	0F	xl16 expected result
00005308				3978+	DROP	R5	
00005308	00000000 00000271			3979	DC	XL16'0000000000000271 0000000000000024'	result
00005310	00000000 00000024						
00005318	FF000000 00000019			3980	DC	XL16'FF00000000000019 38000000000000FA'	v2
00005320	38000000 000000FA						
00005328	FF000000 00000019			3981	DC	XL16'FF00000000000019 38000000000000FA'	v3
00005330	38000000 000000FA						
				3982			
				3983	VRR_C	VMO,0	
00005338				3984+	DS	0FD	
00005338		00005338		3985+	USING	*,R5	base for test data and test routine
00005338	00005378			3986+T113	DC	A(X113)	address of test routine
0000533C	0071			3987+	DC	H'113'	test number
0000533E	00			3988+	DC	X'00'	
0000533F	00			3989+	DC	HL1'0'	m4
00005340	E5D4D640 40404040			3990+	DC	CL8'VMO'	instruction name
00005348	000053B0			3991+	DC	A(RE113+16)	address of v2 source
0000534C	000053C0			3992+	DC	A(RE113+32)	address of v3 source
00005350	00000010			3993+	DC	A(16)	result length
00005354	000053A0			3994+REA113	DC	A(RE113)	result address
00005358	00000000 00000000			3995+	DS	FD	gap
00005360	00000000 00000000			3996+V10113	DS	XL16	V1 output
00005368	00000000 00000000						
00005370	00000000 00000000			3997+	DS	FD	gap
				3998+*			
00005378				3999+X113	DS	0F	
00005378	E310 5010 0014		00000010	4000+	LGF	R1,V2ADDR	load v2 source
0000537E	E761 0000 0806		00000000	4001+	VL	v22,0(R1)	use v22 to test decoder
00005384	E310 5014 0014		00000014	4002+	LGF	R1,V3ADDR	load v3 source
0000538A	E771 0000 0806		00000000	4003+	VL	v23,0(R1)	use v23 to test decoder
00005390	E766 7000 0EA7			4004+	VMO	V22,V22,V23,0	test instruction (dest is a source)
00005396	E760 5028 080E		00005360	4005+	VST	V22,V10113	save v1 output
0000539C	07FB			4006+	BR	R11	return
000053A0				4007+RE113	DC	0F	xl16 expected result
000053A0				4008+	DROP	R5	
000053A0	00040010 00241900			4009	DC	XL16'0004001000241900 0064384000B60009'	result
000053A8	00643840 00B60009						
000053B0	FF020304 05060750			4010	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
000053B8	090A0B78 0C0D0EFD						
000053C0	FF020304 05060750			4011	DC	XL16'FF02030405060750 090A0B780D0E0FFD'	v3
000053C8	090A0B78 0D0E0FFD						
				4012			
				4013	VRR_C	VMO,0	
000053D0				4014+	DS	0FD	
000053D0		000053D0		4015+	USING	*,R5	base for test data and test routine
000053D0	00005410			4016+T114	DC	A(X114)	address of test routine
000053D4	0072			4017+	DC	H'114'	test number
000053D6	00			4018+	DC	X'00'	
000053D7	00			4019+	DC	HL1'0'	m4
000053D8	E5D4D640 40404040			4020+	DC	CL8'VMO'	instruction name
000053E0	00005448			4021+	DC	A(RE114+16)	address of v2 source
000053E4	00005458			4022+	DC	A(RE114+32)	address of v3 source

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  LOC        OBJECT CODE      ADDR1     ADDR2     STMT

000053E8   00000010                              4023+          DC      A(16)              result length
000053EC   00005438                              4024+REA114    DC      A(RE114)           result address
000053F0   00000000 00000000                     4025+          DS      FD                 gap
000053F8   00000000 00000000                     4026+V10114    DS      XL16               V1 output
00005400   00000000 00000000
00005408   00000000 00000000                     4027+          DS      FD                 gap
                                                 4028+*
00005410                                         4029+X114      DS      0F
00005410   E310 5010 0014             00000010   4030+          LGF     R1,V2ADDR          load v2 source
00005416   E761 0000 0806             00000000   4031+          VL      v22,0(R1)          use v22 to test decoder
0000541C   E310 5014 0014             00000014   4032+          LGF     R1,V3ADDR          load v3 source
00005422   E771 0000 0806             00000000   4033+          VL      v23,0(R1)          use v23 to test decoder
00005428   E766 7000 0EA7                        4034+          VMO     V22,V22,V23,0       test instruction (dest is a source)
0000542E   E760 5028 080E             000053F8   4035+          VST     V22,V10114          save v1 output
00005434   07FB                                  4036+          BR      R11                return
00005438                                         4037+RE114     DC      0F                 xl16 expected result
00005438                                         4038+          DROP    R5
00005438   00020008 00120C80                     4039           DC      XL16'0002000800120C80 00321C20005B0006'    result
00005440   00321C20 005B0006
00005448   FF020304 05060750                     4040           DC      XL16'FF02030405060750 090A0B780C0D0EFD'    v2
00005450   090A0B78 0C0D0EFD
00005458   FF010102 02030328                     4041           DC      XL16'FF01010202030328 0405053C060707FE'    v3
00005460   0405053C 060707FE
                                                 4042
                                                 4043           VRR_C   VMO,0
00005468                                         4044+          DS      0FD
00005468                          00005468       4045+          USING   *,R5               base for test data and test routine
00005468   000054A8                              4046+T115      DC      A(X115)            address of test routine
0000546C   0073                                  4047+          DC      H'115'             test number
0000546E   00                                    4048+          DC      X'00'
0000546F   00                                    4049+          DC      HL1'0'             m4
00005470   E5D4D640 40404040                     4050+          DC      CL8'VMO'           instruction name
00005478   000054E0                              4051+          DC      A(RE115+16)        address of v2 source
0000547C   000054F0                              4052+          DC      A(RE115+32)        address of v3 source
00005480   00000010                              4053+          DC      A(16)              result length
00005484   000054D0                              4054+REA115    DC      A(RE115)           result address
00005488   00000000 00000000                     4055+          DS      FD                 gap
00005490   00000000 00000000                     4056+V10115    DS      XL16               V1 output
00005498   00000000 00000000
000054A0   00000000 00000000                     4057+          DS      FD                 gap
                                                 4058+*
000054A8                                         4059+X115      DS      0F
000054A8   E310 5010 0014             00000010   4060+          LGF     R1,V2ADDR          load v2 source
000054AE   E761 0000 0806             00000000   4061+          VL      v22,0(R1)          use v22 to test decoder
000054B4   E310 5014 0014             00000014   4062+          LGF     R1,V3ADDR          load v3 source
000054BA   E771 0000 0806             00000000   4063+          VL      v23,0(R1)          use v23 to test decoder
000054C0   E766 7000 0EA7                        4064+          VMO     V22,V22,V23,0       test instruction (dest is a source)
000054C6   E760 5028 080E             00005490   4065+          VST     V22,V10115          save v1 output
000054CC   07FB                                  4066+          BR      R11                return
000054D0                                         4067+RE115     DC      0F                 xl16 expected result
000054D0                                         4068+          DROP    R5
000054D0   00000000 00000320                     4069           DC      XL16'000000000000320 000A0708000D0003'    result
000054D8   000A0708 000D0003
000054E0   FF020304 05060750                     4070           DC      XL16'FF02030405060750 090A0B780C0D0EFD'    v2
000054E8   090A0B78 0C0D0EFD
000054F0   FF000000 0000000A                     4071           DC      XL16'FF0000000000000A 0101010F010101FF'    v3
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  LOC        OBJECT CODE     ADDR1     ADDR2     STMT

000054F8  0101010F 010101FF
                                                 4072
                                                 4073 * Halfword
                                                 4074          VRR_C VMO,1
00005500                                         4075+         DS    0FD
00005500                        00005500         4076+         USING *,R5                    base for test data and test routine
00005500  00005540                               4077+T116     DC    A(X116)                 address of test routine
00005504  0074                                   4078+         DC    H'116'                  test number
00005506  00                                     4079+         DC    X'00'
00005507  01                                      4080+         DC    HL1'1'                  m4
00005508  E5D4D640 40404040                      4081+         DC    CL8'VMO'                instruction name
00005510  00005578                               4082+         DC    A(RE116+16)             address of v2 source
00005514  00005588                               4083+         DC    A(RE116+32)             address of v3 source
00005518  00000010                               4084+         DC    A(16)                   result length
0000551C  00005568                               4085+REA116   DC    A(RE116)                result address
00005520  00000000 00000000                      4086+         DS    FD                      gap
00005528  00000000 00000000                      4087+V10116   DS    XL16                    V1 output
00005530  00000000 00000000
00005538  00000000 00000000                      4088+         DS    FD                      gap
                                                 4089+*
00005540                                         4090+X116     DS    0F
00005540  E310 5010 0014          00000010       4091+         LGF   R1,V2ADDR               load v2 source
00005546  E761 0000 0806          00000000       4092+         VL    v22,0(R1)               use v22 to test decoder
0000554C  E310 5014 0014          00000014       4093+         LGF   R1,V3ADDR               load v3 source
00005552  E771 0000 0806          00000000       4094+         VL    v23,0(R1)               use v23 to test decoder
00005558  E766 7000 1EA7                         4095+         VMO   V22,V22,V23,1            test instruction (dest is a source)
0000555E  E760 5028 080E          00005528       4096+         VST   V22,V10116               save v1 output
00005564  07FB                                   4097+         BR    R11                     return
00005568                                         4098+RE116    DC    0F                      xl16 expected result
00005568                                         4099+         DROP  R5
00005568  00000000 00000271                      4100          DC    XL16'000000000000271 000000000121CC24'    result
00005570  00000000 0121CC24
00005578  FFFF0000 00000000                      4101          DC    XL16'FFFF000000000019 003800001000EEFA'    v2
00005580  00380000 1000EEFA
00005588  FFFF0000 00000019                      4102          DC    XL16'FFFF000000000019 003800038000EEFA'    v3
00005590  00380003 8000EEFA
                                                 4103
                                                 4104          VRR_C VMO,1
00005598                                         4105+         DS    0FD
00005598                        00005598         4106+         USING *,R5                    base for test data and test routine
00005598  000055D8                               4107+T117     DC    A(X117)                 address of test routine
0000559C  0075                                   4108+         DC    H'117'                  test number
0000559E  00                                     4109+         DC    X'00'
0000559F  01                                      4110+         DC    HL1'1'                  m4
000055A0  E5D4D640 40404040                      4111+         DC    CL8'VMO'                instruction name
000055A8  00005610                               4112+         DC    A(RE117+16)             address of v2 source
000055AC  00005620                               4113+         DC    A(RE117+32)             address of v3 source
000055B0  00000010                               4114+         DC    A(16)                   result length
000055B4  00005600                               4115+REA117   DC    A(RE117)                result address
000055B8  00000000 00000000                      4116+         DS    FD                      gap
000055C0  00000000 00000000                      4117+V10117   DS    XL16                    V1 output
000055C8  00000000 00000000
000055D0  00000000 00000000                      4118+         DS    FD                      gap
                                                 4119+*
000055D8                                         4120+X117     DS    0F
000055D8  E310 5010 0014          00000010       4121+         LGF   R1,V2ADDR               load v2 source
```

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  LOC          OBJECT CODE      ADDR1      ADDR2     STMT

000055DE   E761 0000 0806              00000000   4122+          VL     v22,0(R1)          use v22 to test decoder
000055E4   E310 5014 0014              00000014   4123+          LGF    R1,V3ADDR          load v3 source
000055EA   E771 0000 0806              00000000   4124+          VL     v23,0(R1)          use v23 to test decoder
000055F0   E766 7000 1EA7                         4125+          VMO    V22,V22,V23,1       test instruction (dest is a source)
000055F6   E760 5028 080E              000055C0   4126+          VST    V22,V10117          save v1 output
000055FC   07FB                                   4127+          BR     R11                return
00005600                                          4128+RE117     DC     0F                 xl16 expected result
00005600                                          4129+          DROP   R5
00005600   00091810 00357900                      4130           DC     XL16'0009181000357900 0083884000EFA309'   result
00005608   00838840 00EFA309
00005610   FF020304 05060750                      4131           DC     XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005618   090A0B78 0C0D0EFD
00005620   FF020304 05060750                      4132           DC     XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00005628   090A0B78 0D0E0FFD
                                                  4133
                                                  4134           VRR_C  VMO,1
00005630                                          4135+          DS     0FD
00005630                         00005630         4136+          USING  *,R5              base for test data and test routine
00005630   00005670                               4137+T118      DC     A(X118)           address of test routine
00005634   0076                                   4138+          DC     H'118'            test number
00005636   00                                     4139+          DC     X'00'
00005637   01                                     4140+          DC     HL1'1'            m4
00005638   E5D4D640 40404040                      4141+          DC     CL8'VMO'          instruction name
00005640   000056A8                               4142+          DC     A(RE118+16)       address of v2 source
00005644   000056B8                               4143+          DC     A(RE118+32)       address of v3 source
00005648   00000010                               4144+          DC     A(16)             result length
0000564C   00005698                               4145+REA118    DC     A(RE118)          result address
00005650   00000000 00000000                      4146+          DS     FD                gap
00005658   00000000 00000000                      4147+V10118    DS     XL16              V1 output
00005660   00000000 00000000
00005668   00000000 00000000                      4148+          DS     FD                gap
                                                  4149+*
00005670                                          4150+X118      DS     0F
00005670   E310 5010 0014              00000010   4151+          LGF    R1,V2ADDR          load v2 source
00005676   E761 0000 0806              00000000   4152+          VL     v22,0(R1)          use v22 to test decoder
0000567C   E310 5014 0014              00000014   4153+          LGF    R1,V3ADDR          load v3 source
00005682   E771 0000 0806              00000000   4154+          VL     v23,0(R1)          use v23 to test decoder
00005688   E766 7000 1EA7                         4155+          VMO    V22,V22,V23,1       test instruction (dest is a source)
0000568E   E760 5028 080E              00005658   4156+          VST    V22,V10118          save v1 output
00005694   07FB                                   4157+          BR     R11                return
00005698                                          4158+RE118     DC     0F                 xl16 expected result
00005698                                          4159+          DROP   R5
00005698   00030A08 00171480                      4160           DC     XL16'00030A0800171480 003C08200077CA06'   result
000056A0   003C0820 0077CA06
000056A8   FF020304 05060750                      4161           DC     XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000056B0   090A0B78 0C0D0EFD
000056B8   FF010102 02030328                      4162           DC     XL16'FF01010202030328 0405053C060707FE'   v3
000056C0   0405053C 060707FE
                                                  4163
                                                  4164           VRR_C  VMO,1
000056C8                                          4165+          DS     0FD
000056C8                         000056C8         4166+          USING  *,R5              base for test data and test routine
000056C8   00005708                               4167+T119      DC     A(X119)           address of test routine
000056CC   0077                                   4168+          DC     H'119'            test number
000056CE   00                                     4169+          DC     X'00'
000056CF   01                                     4170+          DC     HL1'1'            m4
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000056D0	E5D4D640 40404040			4171+	DC	CL8'VMO'	instruction name
000056D8	00005740			4172+	DC	A(RE119+16)	address of v2 source
000056DC	00005750			4173+	DC	A(RE119+32)	address of v3 source
000056E0	00000010			4174+	DC	A(16)	result length
000056E4	00005730			4175+REA119	DC	A(RE119)	result address
000056E8	00000000 00000000			4176+	DS	FD	gap
000056F0	00000000 00000000			4177+V10119	DS	XL16	V1 output
000056F8	00000000 00000000						
00005700	00000000 00000000			4178+	DS	FD	gap
				4179+*			
00005708				4180+X119	DS	0F	
00005708	E310 5010 0014		00000010	4181+	LGF	R1,V2ADDR	load v2 source
0000570E	E761 0000 0806		00000000	4182+	VL	v22,0(R1)	use v22 to test decoder
00005714	E310 5014 0014		00000014	4183+	LGF	R1,V3ADDR	load v3 source
0000571A	E771 0000 0806		00000000	4184+	VL	v23,0(R1)	use v23 to test decoder
00005720	E766 7000 1EA7			4185+	VMO	V22,V22,V23,1	test instruction (dest is a source)
00005726	E760 5028 080E		000056F0	4186+	VST	V22,V10119	save v1 output
0000572C	07FB			4187+	BR	R11	return
00005730				4188+RE119	DC	0F	xl16 expected result
00005730				4189+	DROP	R5	
00005730	00000000 00004920			4190	DC	XL16'0000000000004920 000C2408001DEB03'	result
00005738	000C2408 001DEB03						
00005740	FF020304 05060750			4191	DC	XL16'FF02030405060750 090A0B780C0D0EFD'	v2
00005748	090A0B78 0C0D0EFD						
00005750	FF000000 0000000A			4192	DC	XL16'FF0000000000000A 0101010F010101FF'	v3
00005758	0101010F 010101FF						
				4193			
				4194	* Word		
				4195		VRR_C VMO,2	
00005760				4196+	DS	0FD	
00005760		00005760		4197+	USING	*,R5	base for test data and test routine
00005760	000057A0			4198+T120	DC	A(X120)	address of test routine
00005764	0078			4199+	DC	H'120'	test number
00005766	00			4200+	DC	X'00'	
00005767	02			4201+	DC	HL1'2'	m4
00005768	E5D4D640 40404040			4202+	DC	CL8'VMO'	instruction name
00005770	000057D8			4203+	DC	A(RE120+16)	address of v2 source
00005774	000057E8			4204+	DC	A(RE120+32)	address of v3 source
00005778	00000010			4205+	DC	A(16)	result length
0000577C	000057C8			4206+REA120	DC	A(RE120)	result address
00005780	00000000 00000000			4207+	DS	FD	gap
00005788	00000000 00000000			4208+V10120	DS	XL16	V1 output
00005790	00000000 00000000						
00005798	00000000 00000000			4209+	DS	FD	gap
				4210+*			
000057A0				4211+X120	DS	0F	
000057A0	E310 5010 0014		00000010	4212+	LGF	R1,V2ADDR	load v2 source
000057A6	E761 0000 0806		00000000	4213+	VL	v22,0(R1)	use v22 to test decoder
000057AC	E310 5014 0014		00000014	4214+	LGF	R1,V3ADDR	load v3 source
000057B2	E771 0000 0806		00000000	4215+	VL	v23,0(R1)	use v23 to test decoder
000057B8	E766 7000 2EA7			4216+	VMO	V22,V22,V23,2	test instruction (dest is a source)
000057BE	E760 5028 080E		00005788	4217+	VST	V22,V10120	save v1 output
000057C4	07FB			4218+	BR	R11	return
000057C8				4219+RE120	DC	0F	xl16 expected result
000057C8				4220+	DROP	R5	
000057C8	00000002 71000000			4221	DC	XL16'0000000271000000 FF0123454FEDCC24'	result

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  LOC        OBJECT CODE      ADDR1    ADDR2    STMT

000057D0  FF012345 4FEDCC24
000057D8  FFFFFFFF 00019000            4222          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'     v2
000057E0  00000038 EEEEEEFA
000057E8  FFFFFFFF 00019000            4223          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'     v3
000057F0  00000038 0EEEEEFA
                                       4224
                                       4225          VRR_C VMO,2
000057F8                               4226+         DS    0FD
000057F8            000057F8           4227+         USING *,R5                base for test data and test routine
000057F8  00005838                     4228+T121     DC    A(X121)             address of test routine
000057FC  0079                         4229+         DC    H'121'              test number
000057FE  00                           4230+         DC    X'00'
000057FF  02                           4231+         DC    HL1'2'              m4
00005800  E5D4D640 40404040            4232+         DC    CL8'VMO'            instruction name
00005808  00005870                     4233+         DC    A(RE121+16)         address of v2 source
0000580C  00005880                     4234+         DC    A(RE121+32)         address of v3 source
00005810  00000010                     4235+         DC    A(16)               result length
00005814  00005860                     4236+REA121   DC    A(RE121)            result address
00005818  00000000 00000000            4237+         DS    FD                  gap
00005820  00000000 00000000            4238+V10121   DS    XL16                V1 output
00005828  00000000 00000000
00005830  00000000 00000000            4239+         DS    FD                  gap
                                       4240+*
00005838                               4241+X121     DS    0F
00005838  E310 5010 0014      00000010 4242+         LGF   R1,V2ADDR           load v2 source
0000583E  E761 0000 0806      00000000 4243+         VL    v22,0(R1)           use v22 to test decoder
00005844  E310 5014 0014      00000014 4244+         LGF   R1,V3ADDR           load v3 source
0000584A  E771 0000 0806      00000000 4245+         VL    v23,0(R1)           use v23 to test decoder
00005850  E766 7000 2EA7               4246+         VMO   V22,V22,V23,2        test instruction (dest is a source)
00005856  E760 5028 080E      00005820 4247+         VST   V22,V10121           save v1 output
0000585C  07FB                         4248+         BR    R11                 return
00005860                               4249+RE121    DC    0F                  xl16 expected result
00005860                               4250+         DROP  R5
00005860  00193C6D 77F57900            4251          DC    XL16'00193C6D77F57900 00AA6E5898D42101'     result
00005868  00AA6E58 98D42101
00005870  FF020304 05060750            4252          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'     v2
00005878  090A0B0C 0D0E0F7F
00005880  FF020304 05060750            4253          DC    XL16'FF02030405060750 090A0B780D0E0F7F'     v3
00005888  090A0B78 0D0E0F7F
                                       4254
                                       4255          VRR_C VMO,2
00005890                               4256+         DS    0FD
00005890            00005890           4257+         USING *,R5                base for test data and test routine
00005890  000058D0                     4258+T122     DC    A(X122)             address of test routine
00005894  007A                         4259+         DC    H'122'              test number
00005896  00                           4260+         DC    X'00'
00005897  02                           4261+         DC    HL1'2'              m4
00005898  E5D4D640 40404040            4262+         DC    CL8'VMO'            instruction name
000058A0  00005908                     4263+         DC    A(RE122+16)         address of v2 source
000058A4  00005918                     4264+         DC    A(RE122+32)         address of v3 source
000058A8  00000010                     4265+         DC    A(16)               result length
000058AC  000058F8                     4266+REA122   DC    A(RE122)            result address
000058B0  00000000 00000000            4267+         DS    FD                  gap
000058B8  00000000 00000000            4268+V10122   DS    XL16                V1 output
000058C0  00000000 00000000
000058C8  00000000 00000000            4269+         DS    FD                  gap
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				4270+*			
000058D0				4271+X122	DS	0F	
000058D0	E310 5010 0014		00000010	4272+	LGF	R1,V2ADDR	load v2 source
000058D6	E761 0000 0806		00000000	4273+	VL	v22,0(R1)	use v22 to test decoder
000058DC	E310 5014 0014		00000014	4274+	LGF	R1,V3ADDR	load v3 source
000058E2	E771 0000 0806		00000000	4275+	VL	v23,0(R1)	use v23 to test decoder
000058E8	E766 7000 2EA7			4276+	VMO	V22,V22,V23,2	test instruction (dest is a source)
000058EE	E760 5028 080E		000058B8	4277+	VST	V22,V10122	save v1 output
000058F4	07FB			4278+	BR	R11	return
000058F8				4279+RE122	DC	0F	xl16 expected result
000058F8				4280+	DROP	R5	
000058F8	000A1B30 90F71480			4281	DC	XL16'000A1B3090F71480 004EB01DFF5B4941'	result
00005900	004EB01D FF5B4941						
00005908	FF020304 05060750			4282	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00005910	090A0B0C 0D0E0F7F						
00005918	FF010102 02030328			4283	DC	XL16'FF01010202030328 0405053C0607073F'	v3
00005920	0405053C 0607073F						
				4284			
				4285	VRR_C	VMO,2	
00005928				4286+	DS	0FD	
00005928		00005928		4287+	USING	*,R5	base for test data and test routine
00005928	00005968			4288+T123	DC	A(X123)	address of test routine
0000592C	007B			4289+	DC	H'123'	test number
0000592E	00			4290+	DC	X'00'	
0000592F	02			4291+	DC	HL1'2'	m4
00005930	E5D4D640 40404040			4292+	DC	CL8'VMO'	instruction name
00005938	000059A0			4293+	DC	A(RE123+16)	address of v2 source
0000593C	000059B0			4294+	DC	A(RE123+32)	address of v3 source
00005940	00000010			4295+	DC	A(16)	result length
00005944	00005990			4296+REA123	DC	A(RE123)	result address
00005948	00000000 00000000			4297+	DS	FD	gap
00005950	00000000 00000000			4298+V10123	DS	XL16	V1 output
00005958	00000000 00000000						
00005960	00000000 00000000			4299+	DS	FD	gap
				4300+*			
00005968				4301+X123	DS	0F	
00005968	E310 5010 0014		00000010	4302+	LGF	R1,V2ADDR	load v2 source
0000596E	E761 0000 0806		00000000	4303+	VL	v22,0(R1)	use v22 to test decoder
00005974	E310 5014 0014		00000014	4304+	LGF	R1,V3ADDR	load v3 source
0000597A	E771 0000 0806		00000000	4305+	VL	v23,0(R1)	use v23 to test decoder
00005980	E766 7000 2EA7			4306+	VMO	V22,V22,V23,2	test instruction (dest is a source)
00005986	E760 5028 080E		00005950	4307+	VST	V22,V10123	save v1 output
0000598C	07FB			4308+	BR	R11	return
00005990				4309+RE123	DC	0F	xl16 expected result
00005990				4310+	DROP	R5	
00005990	00000000 323C4920			4311	DC	XL16'00000000323C4920 000D1B2B60616771'	result
00005998	000D1B2B 60616771						
000059A0	FF020304 05060750			4312	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
000059A8	090A0B0C 0D0E0F7F						
000059B0	FF000000 0000000A			4313	DC	XL16'FF0000000000000A 0101010F0101010F'	v3
000059B8	0101010F 0101010F						
				4314			
				4315	* Doubleword		
				4316	VRR_C	VMO,3	
000059C0				4317+	DS	0FD	
000059C0		000059C0		4318+	USING	*,R5	base for test data and test routine

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   LOC         OBJECT CODE      ADDR1     ADDR2     STMT

   000059C0   00005A00                                4319+T124     DC      A(X124)              address of test routine
   000059C4   007C                                    4320+         DC      H'124'               test number
   000059C6   00                                      4321+         DC      X'00'
   000059C7   03                                      4322+         DC      HL1'3'               m4
   000059C8   E5D4D640 40404040                        4323+         DC      CL8'VMO'             instruction name
   000059D0   00005A38                                4324+         DC      A(RE124+16)          address of v2 source
   000059D4   00005A48                                4325+         DC      A(RE124+32)          address of v3 source
   000059D8   00000010                                4326+         DC      A(16)                result length
   000059DC   00005A28                                4327+REA124   DC      A(RE124)             result address
   000059E0   00000000 00000000                        4328+         DS      FD                   gap
   000059E8   00000000 00000000                        4329+V10124   DS      XL16                 V1 output
   000059F0   00000000 00000000
   000059F8   00000000 00000000                        4330+         DS      FD                   gap
                                                       4331+*
   00005A00                                            4332+X124     DS      0F
   00005A00   E310 5010 0014              00000010     4333+         LGF     R1,V2ADDR            load v2 source
   00005A06   E761 0000 0806              00000000     4334+         VL      v22,0(R1)            use v22 to test decoder
   00005A0C   E310 5014 0014              00000014     4335+         LGF     R1,V3ADDR            load v3 source
   00005A12   E771 0000 0806              00000000     4336+         VL      v23,0(R1)            use v23 to test decoder
   00005A18   E766 7000 3EA7                           4337+         VMO     V22,V22,V23,3         test instruction (dest is a source)
   00005A1E   E760 5028 080E              000059E8     4338+         VST     V22,V10124            save v1 output
   00005A24   07FB                                     4339+         BR      R11                  return
   00005A28                                            4340+RE124    DC      0F                   xl16 expected result
   00005A28                                            4341+         DROP    R5
   00005A28   00000000 00000C77                        4342          DC      XL16'0000000000000C77 96789F9F4FEDCC24'    result
   00005A30   96789F9F 4FEDCC24
   00005A38   FFFFFFFF 00019000                        4343          DC      XL16'FFFFFFFF00019000 00000038EEEEEEFA'    v2
   00005A40   00000038 EEEEEEFA
   00005A48   FFFFFFFF 00019000                        4344          DC      XL16'FFFFFFFF00019000 000000380EEEEEFA'    v3
   00005A50   00000038 0EEEEEFA

                                                       4345
                                                       4346          VRR_C VMO,3
   00005A58                                            4347+         DS      0FD
   00005A58                          00005A58          4348+         USING   *,R5                 base for test data and test routine
   00005A58   00005A98                                4349+T125     DC      A(X125)              address of test routine
   00005A5C   007D                                    4350+         DC      H'125'               test number
   00005A5E   00                                      4351+         DC      X'00'
   00005A5F   03                                      4352+         DC      HL1'3'               m4
   00005A60   E5D4D640 40404040                        4353+         DC      CL8'VMO'             instruction name
   00005A68   00005AD0                                4354+         DC      A(RE125+16)          address of v2 source
   00005A6C   00005AE0                                4355+         DC      A(RE125+32)          address of v3 source
   00005A70   00000010                                4356+         DC      A(16)                result length
   00005A74   00005AC0                                4357+REA125   DC      A(RE125)             result address
   00005A78   00000000 00000000                        4358+         DS      FD                   gap
   00005A80   00000000 00000000                        4359+V10125   DS      XL16                 V1 output
   00005A88   00000000 00000000
   00005A90   00000000 00000000                        4360+         DS      FD                   gap
                                                       4361+*
   00005A98                                            4362+X125     DS      0F
   00005A98   E310 5010 0014              00000010     4363+         LGF     R1,V2ADDR            load v2 source
   00005A9E   E761 0000 0806              00000000     4364+         VL      v22,0(R1)            use v22 to test decoder
   00005AA4   E310 5014 0014              00000014     4365+         LGF     R1,V3ADDR            load v3 source
   00005AAA   E771 0000 0806              00000000     4366+         VL      v23,0(R1)            use v23 to test decoder
   00005AB0   E766 7000 3EA7                           4367+         VMO     V22,V22,V23,3         test instruction (dest is a source)
   00005AB6   E760 5028 080E              00005A80     4368+         VST     V22,V10125            save v1 output
   00005ABC   07FB                                     4369+         BR      R11                  return
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005AC0				4370+RE125	DC	0F	xl16 expected result
00005AC0				4371+	DROP	R5	
00005AC0	0051B52F 8692B4F6			4372	DC	XL16'0051B52F8692B4F6 152B55D498D42101'	result
00005AC8	152B55D4 98D42101						
00005AD0	FF020304 05060750			4373	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00005AD8	090A0B0C 0D0E0F7F						
00005AE0	01020304 05060750			4374	DC	XL16'0102030405060750 090A0B780D0E0F7F'	v3
00005AE8	090A0B78 0D0E0F7F						
				4375			
				4376	VRR_C	VMO,3	
00005AF0				4377+	DS	0FD	
00005AF0		00005AF0		4378+	USING	*,R5	base for test data and test routine
00005AF0	00005B30			4379+T126	DC	A(X126)	address of test routine
00005AF4	007E			4380+	DC	H'126'	test number
00005AF6	00			4381+	DC	X'00'	
00005AF7	03			4382+	DC	HL1'3'	m4
00005AF8	E5D4D640 40404040			4383+	DC	CL8'VMO'	instruction name
00005B00	00005B68			4384+	DC	A(RE126+16)	address of v2 source
00005B04	00005B78			4385+	DC	A(RE126+32)	address of v3 source
00005B08	00000010			4386+	DC	A(16)	result length
00005B0C	00005B58			4387+REA126	DC	A(RE126)	result address
00005B10	00000000 00000000			4388+	DS	FD	gap
00005B18	00000000 00000000			4389+V10126	DS	XL16	V1 output
00005B20	00000000 00000000						
00005B28	00000000 00000000			4390+	DS	FD	gap
				4391+*			
00005B30				4392+X126	DS	0F	
00005B30	E310 5010 0014		00000010	4393+	LGF	R1,V2ADDR	load v2 source
00005B36	E761 0000 0806		00000000	4394+	VL	v22,0(R1)	use v22 to test decoder
00005B3C	E310 5014 0014		00000014	4395+	LGF	R1,V3ADDR	load v3 source
00005B42	E771 0000 0806		00000000	4396+	VL	v23,0(R1)	use v23 to test decoder
00005B48	E766 7000 3EA7			4397+	VMO	V22,V22,V23,3	test instruction (dest is a source)
00005B4E	E760 5028 080E		00005B18	4398+	VST	V22,V10126	save v1 output
00005B54	07FB			4399+	BR	R11	return
00005B58				4400+RE126	DC	0F	xl16 expected result
00005B58				4401+	DROP	R5	
00005B58	0024558D B838C862			4402	DC	XL16'0024558DB838C862 B47CD8D5FF5B4941'	result
00005B60	B47CD8D5 FF5B4941						
00005B68	FF020304 05060750			4403	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00005B70	090A0B0C 0D0E0F7F						
00005B78	00010102 02030328			4404	DC	XL16'0001010202030328 0405053C0607073F'	v3
00005B80	0405053C 0607073F						
				4405			
				4406	VRR_C	VMO,3	
00005B88				4407+	DS	0FD	
00005B88		00005B88		4408+	USING	*,R5	base for test data and test routine
00005B88	00005BC8			4409+T127	DC	A(X127)	address of test routine
00005B8C	007F			4410+	DC	H'127'	test number
00005B8E	00			4411+	DC	X'00'	
00005B8F	03			4412+	DC	HL1'3'	m4
00005B90	E5D4D640 40404040			4413+	DC	CL8'VMO'	instruction name
00005B98	00005C00			4414+	DC	A(RE127+16)	address of v2 source
00005B9C	00005C10			4415+	DC	A(RE127+32)	address of v3 source
00005BA0	00000010			4416+	DC	A(16)	result length
00005BA4	00005BF0			4417+REA127	DC	A(RE127)	result address
00005BA8	00000000 00000000			4418+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005BB0	00000000 00000000			4419+V10127	DS	XL16	V1 output
00005BB8	00000000 00000000						
00005BC0	00000000 00000000			4420+	DS	FD	gap
				4421+*			
00005BC8				4422+X127	DS	0F	
00005BC8	E310 5010 0014		00000010	4423+	LGF	R1,V2ADDR	load v2 source
00005BCE	E761 0000 0806		00000000	4424+	VL	v22,0(R1)	use v22 to test decoder
00005BD4	E310 5014 0014		00000014	4425+	LGF	R1,V3ADDR	load v3 source
00005BDA	E771 0000 0806		00000000	4426+	VL	v23,0(R1)	use v23 to test decoder
00005BE0	E766 7000 3EA7			4427+	VMO	V22,V22,V23,3	test instruction (dest is a source)
00005BE6	E760 5028 080E		00005BB0	4428+	VST	V22,V10127	save v1 output
00005BEC	07FB			4429+	BR	R11	return
00005BF0				4430+RE127	DC	0F	xl16 expected result
00005BF0				4431+	DROP	R5	
00005BF0	0009131E A8C3DFFE			4432	DC	XL16'0009131EA8C3DFFE 091C345060616771'	result
00005BF8	091C3450 60616771						
00005C00	FF020304 05060750			4433	DC	XL16'FF02030405060750 090A0B0C0D0E0F7F'	v2
00005C08	090A0B0C 0D0E0F7F						
00005C10	00000000 0000000A			4434	DC	XL16'000000000000000A 0101010F0101010F'	v3
00005C18	0101010F 0101010F						
				4435			
				4436	VRR_C	VMO,3	
00005C20				4437+	DS	0FD	
00005C20		00005C20		4438+	USING	*,R5	base for test data and test routine
00005C20	00005C60			4439+T128	DC	A(X128)	address of test routine
00005C24	0080			4440+	DC	H'128'	test number
00005C26	00			4441+	DC	X'00'	
00005C27	03			4442+	DC	HL1'3'	m4
00005C28	E5D4D640 40404040			4443+	DC	CL8'VMO'	instruction name
00005C30	00005C98			4444+	DC	A(RE128+16)	address of v2 source
00005C34	00005CA8			4445+	DC	A(RE128+32)	address of v3 source
00005C38	00000010			4446+	DC	A(16)	result length
00005C3C	00005C88			4447+REA128	DC	A(RE128)	result address
00005C40	00000000 00000000			4448+	DS	FD	gap
00005C48	00000000 00000000			4449+V10128	DS	XL16	V1 output
00005C50	00000000 00000000						
00005C58	00000000 00000000			4450+	DS	FD	gap
				4451+*			
00005C60				4452+X128	DS	0F	
00005C60	E310 5010 0014		00000010	4453+	LGF	R1,V2ADDR	load v2 source
00005C66	E761 0000 0806		00000000	4454+	VL	v22,0(R1)	use v22 to test decoder
00005C6C	E310 5014 0014		00000014	4455+	LGF	R1,V3ADDR	load v3 source
00005C72	E771 0000 0806		00000000	4456+	VL	v23,0(R1)	use v23 to test decoder
00005C78	E766 7000 3EA7			4457+	VMO	V22,V22,V23,3	test instruction (dest is a source)
00005C7E	E760 5028 080E		00005C48	4458+	VST	V22,V10128	save v1 output
00005C84	07FB			4459+	BR	R11	return
00005C88				4460+RE128	DC	0F	xl16 expected result
00005C88				4461+	DROP	R5	
00005C88	FFFFFFFF FFFFFFFF			4462	DC	XL16'FFFFFFFFFFFFFFFF F6141E28323C4920'	result
00005C90	F6141E28 323C4920						
00005C98	090A0B0C 0D0E0F7F			4463	DC	XL16'090A0B0C0D0E0F7F FF02030405060750'	v2
00005CA0	FF020304 05060750						
00005CA8	0101010F 0101010F			4464	DC	XL16'0101010F0101010F 000000000000000A'	v3
00005CB0	00000000 0000000A						
				4465			
				4466			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00005CB8	00000000			4467		DC	F'0'	END OF TABLE
00005CBC	00000000			4468		DC	F'0'	
				4469	*			
				4470	* table of pointers to individual load test			
				4471	*			
00005CC0				4472	E7TESTS	DS	0F	
				4473		PTTABLE		
00005CC0				4474+	TTABLE	DS	0F	
00005CC0	000010B8			4475+		DC	A(T1)	
00005CC4	00001150			4476+		DC	A(T2)	
00005CC8	000011E8			4477+		DC	A(T3)	
00005CCC	00001280			4478+		DC	A(T4)	
00005CD0	00001318			4479+		DC	A(T5)	
00005CD4	000013B0			4480+		DC	A(T6)	
00005CD8	00001448			4481+		DC	A(T7)	
00005CDC	000014E0			4482+		DC	A(T8)	
00005CE0	00001578			4483+		DC	A(T9)	
00005CE4	00001610			4484+		DC	A(T10)	
00005CE8	000016A8			4485+		DC	A(T11)	
00005CEC	00001740			4486+		DC	A(T12)	
00005CF0	000017D8			4487+		DC	A(T13)	
00005CF4	00001870			4488+		DC	A(T14)	
00005CF8	00001908			4489+		DC	A(T15)	
00005CFC	000019A0			4490+		DC	A(T16)	
00005D00	00001A38			4491+		DC	A(T17)	
00005D04	00001AD0			4492+		DC	A(T18)	
00005D08	00001B68			4493+		DC	A(T19)	
00005D0C	00001C00			4494+		DC	A(T20)	
00005D10	00001C98			4495+		DC	A(T21)	
00005D14	00001D30			4496+		DC	A(T22)	
00005D18	00001DC8			4497+		DC	A(T23)	
00005D1C	00001E60			4498+		DC	A(T24)	
00005D20	00001EF8			4499+		DC	A(T25)	
00005D24	00001F90			4500+		DC	A(T26)	
00005D28	00002028			4501+		DC	A(T27)	
00005D2C	000020C0			4502+		DC	A(T28)	
00005D30	00002158			4503+		DC	A(T29)	
00005D34	000021F0			4504+		DC	A(T30)	
00005D38	00002288			4505+		DC	A(T31)	
00005D3C	00002320			4506+		DC	A(T32)	
00005D40	000023B8			4507+		DC	A(T33)	
00005D44	00002450			4508+		DC	A(T34)	
00005D48	000024E8			4509+		DC	A(T35)	
00005D4C	00002580			4510+		DC	A(T36)	
00005D50	00002618			4511+		DC	A(T37)	
00005D54	000026B0			4512+		DC	A(T38)	
00005D58	00002748			4513+		DC	A(T39)	
00005D5C	000027E0			4514+		DC	A(T40)	
00005D60	00002878			4515+		DC	A(T41)	
00005D64	00002910			4516+		DC	A(T42)	
00005D68	000029A8			4517+		DC	A(T43)	
00005D6C	00002A40			4518+		DC	A(T44)	
00005D70	00002AD8			4519+		DC	A(T45)	
00005D74	00002B70			4520+		DC	A(T46)	
00005D78	00002C08			4521+		DC	A(T47)	
00005D7C	00002CA0			4522+		DC	A(T48)	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00005D80	00002D38			4523+	DC	A(T49)
00005D84	00002DD0			4524+	DC	A(T50)
00005D88	00002E68			4525+	DC	A(T51)
00005D8C	00002F00			4526+	DC	A(T52)
00005D90	00002F98			4527+	DC	A(T53)
00005D94	00003030			4528+	DC	A(T54)
00005D98	000030C8			4529+	DC	A(T55)
00005D9C	00003160			4530+	DC	A(T56)
00005DA0	000031F8			4531+	DC	A(T57)
00005DA4	00003290			4532+	DC	A(T58)
00005DA8	00003328			4533+	DC	A(T59)
00005DAC	000033C0			4534+	DC	A(T60)
00005DB0	00003458			4535+	DC	A(T61)
00005DB4	000034F0			4536+	DC	A(T62)
00005DB8	00003588			4537+	DC	A(T63)
00005DBC	00003620			4538+	DC	A(T64)
00005DC0	000036B8			4539+	DC	A(T65)
00005DC4	00003750			4540+	DC	A(T66)
00005DC8	000037E8			4541+	DC	A(T67)
00005DCC	00003880			4542+	DC	A(T68)
00005DD0	00003918			4543+	DC	A(T69)
00005DD4	000039B0			4544+	DC	A(T70)
00005DD8	00003A48			4545+	DC	A(T71)
00005DDC	00003AE0			4546+	DC	A(T72)
00005DE0	00003B78			4547+	DC	A(T73)
00005DE4	00003C10			4548+	DC	A(T74)
00005DE8	00003CA8			4549+	DC	A(T75)
00005DEC	00003D40			4550+	DC	A(T76)
00005DF0	00003DD8			4551+	DC	A(T77)
00005DF4	00003E70			4552+	DC	A(T78)
00005DF8	00003F08			4553+	DC	A(T79)
00005DFC	00003FA0			4554+	DC	A(T80)
00005E00	00004038			4555+	DC	A(T81)
00005E04	000040D0			4556+	DC	A(T82)
00005E08	00004168			4557+	DC	A(T83)
00005E0C	00004200			4558+	DC	A(T84)
00005E10	00004298			4559+	DC	A(T85)
00005E14	00004330			4560+	DC	A(T86)
00005E18	000043C8			4561+	DC	A(T87)
00005E1C	00004460			4562+	DC	A(T88)
00005E20	000044F8			4563+	DC	A(T89)
00005E24	00004590			4564+	DC	A(T90)
00005E28	00004628			4565+	DC	A(T91)
00005E2C	000046C0			4566+	DC	A(T92)
00005E30	00004758			4567+	DC	A(T93)
00005E34	000047F0			4568+	DC	A(T94)
00005E38	00004888			4569+	DC	A(T95)
00005E3C	00004920			4570+	DC	A(T96)
00005E40	000049B8			4571+	DC	A(T97)
00005E44	00004A50			4572+	DC	A(T98)
00005E48	00004AE8			4573+	DC	A(T99)
00005E4C	00004B80			4574+	DC	A(T100)
00005E50	00004C18			4575+	DC	A(T101)
00005E54	00004CB0			4576+	DC	A(T102)
00005E58	00004D48			4577+	DC	A(T103)
00005E5C	00004DE0			4578+	DC	A(T104)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005E60	00004E78			4579+	DC	A(T105)	
00005E64	00004F10			4580+	DC	A(T106)	
00005E68	00004FA8			4581+	DC	A(T107)	
00005E6C	00005040			4582+	DC	A(T108)	
00005E70	000050D8			4583+	DC	A(T109)	
00005E74	00005170			4584+	DC	A(T110)	
00005E78	00005208			4585+	DC	A(T111)	
00005E7C	000052A0			4586+	DC	A(T112)	
00005E80	00005338			4587+	DC	A(T113)	
00005E84	000053D0			4588+	DC	A(T114)	
00005E88	00005468			4589+	DC	A(T115)	
00005E8C	00005500			4590+	DC	A(T116)	
00005E90	00005598			4591+	DC	A(T117)	
00005E94	00005630			4592+	DC	A(T118)	
00005E98	000056C8			4593+	DC	A(T119)	
00005E9C	00005760			4594+	DC	A(T120)	
00005EA0	000057F8			4595+	DC	A(T121)	
00005EA4	00005890			4596+	DC	A(T122)	
00005EA8	00005928			4597+	DC	A(T123)	
00005EAC	000059C0			4598+	DC	A(T124)	
00005EB0	00005A58			4599+	DC	A(T125)	
00005EB4	00005AF0			4600+	DC	A(T126)	
00005EB8	00005B88			4601+	DC	A(T127)	
00005EBC	00005C20			4602+	DC	A(T128)	
				4603+*			
00005EC0	00000000			4604+	DC	A(0)	END OF TABLE
00005EC4	00000000			4605+	DC	A(0)	
				4606			
00005EC8	00000000			4607	DC	F'0'	END OF TABLE
00005ECC	00000000			4608	DC	F'0'	

```
 LOC        OBJECT CODE      ADDR1     ADDR2     STMT

                                                4610 ****************************************************************
                                                4611 *          Register equates
                                                4612 ****************************************************************

           00000000  00000001  4614 R0         EQU    0
           00000001  00000001  4615 R1         EQU    1
           00000002  00000001  4616 R2         EQU    2
           00000003  00000001  4617 R3         EQU    3
           00000004  00000001  4618 R4         EQU    4
           00000005  00000001  4619 R5         EQU    5
           00000006  00000001  4620 R6         EQU    6
           00000007  00000001  4621 R7         EQU    7
           00000008  00000001  4622 R8         EQU    8
           00000009  00000001  4623 R9         EQU    9
           0000000A  00000001  4624 R10        EQU    10
           0000000B  00000001  4625 R11        EQU    11
           0000000C  00000001  4626 R12        EQU    12
           0000000D  00000001  4627 R13        EQU    13
           0000000E  00000001  4628 R14        EQU    14
           0000000F  00000001  4629 R15        EQU    15


                                                4631 ****************************************************************
                                                4632 *          Register equates
                                                4633 ****************************************************************

           00000000  00000001  4635 V0         EQU    0
           00000001  00000001  4636 V1         EQU    1
           00000002  00000001  4637 V2         EQU    2
           00000003  00000001  4638 V3         EQU    3
           00000004  00000001  4639 V4         EQU    4
           00000005  00000001  4640 V5         EQU    5
           00000006  00000001  4641 V6         EQU    6
           00000007  00000001  4642 V7         EQU    7
           00000008  00000001  4643 V8         EQU    8
           00000009  00000001  4644 V9         EQU    9
           0000000A  00000001  4645 V10        EQU    10
           0000000B  00000001  4646 V11        EQU    11
           0000000C  00000001  4647 V12        EQU    12
           0000000D  00000001  4648 V13        EQU    13
           0000000E  00000001  4649 V14        EQU    14
           0000000F  00000001  4650 V15        EQU    15
           00000010  00000001  4651 V16        EQU    16
           00000011  00000001  4652 V17        EQU    17
           00000012  00000001  4653 V18        EQU    18
           00000013  00000001  4654 V19        EQU    19
           00000014  00000001  4655 V20        EQU    20
           00000015  00000001  4656 V21        EQU    21
```

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
		00000016	00000001	4657	V22	EQU	22
		00000017	00000001	4658	V23	EQU	23
		00000018	00000001	4659	V24	EQU	24
		00000019	00000001	4660	V25	EQU	25
		0000001A	00000001	4661	V26	EQU	26
		0000001B	00000001	4662	V27	EQU	27
		0000001C	00000001	4663	V28	EQU	28
		0000001D	00000001	4664	V29	EQU	29
		0000001E	00000001	4665	V30	EQU	30
		0000001F	00000001	4666	V31	EQU	31
				4667			
				4668		END	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
BEGIN	I	00000200	2	165	131	161	162	163									
CTLR0	F	0000053C	4	394	175	176	177	178									
DECNUM	C	00001073	16	446	308	310	316	318									
E7TEST	4	00000000	64	460	257												
E7TESTS	F	00005CC0	4	4472	250												
EDIT	X	00001047	18	441	309	317											
ENDTEST	U	000003CE	1	294	255												
EOJ	I	00000520	4	384	210	243	297										
EOJPSW	D	00000510	8	382	384												
FAILCONT	U	000003BE	1	284													
FAILED	F	00001000	4	423	286	295											
FAILMSG	U	000003BA	1	278	268												
FAILPSW	D	00000528	8	386	388												
FAILTEST	I	00000538	4	388	298												
FB0001	F	00000280	8	194	198	199	201										
FB0002	F	00000330	8	227	231	232	234										
IMAGE	1	00000000	24272	0													
K	U	00000400	1	407	408	409	410										
K64	U	00010000	1	409													
M4	U	00000007	1	464	315												
MB	U	00100000	1	410													
MSG	I	00000458	4	344	209	242	327										
MSGCMD	C	000004A6	9	374	357	358											
MSGMSG	C	000004AF	95	375	351	372	349										
MSGMVC	I	000004A0	6	372	355												
MSGOK	I	0000046E	2	353	350												
MSGRET	I	0000048E	4	368	361	364											
MSGSAVE	F	00000494	4	371	347	368											
NEXTE7	U	00000384	1	252	271	289											
OPNAME	C	00000008	8	466	313												
PAGE	U	00001000	1	408													
PRT3	C	0000105D	18	444	309	310	311	317	318	319							
PRTLINE	C	00001008	16	429	436	326											
PRTLNG	U	0000003F	1	436	325												
PRTM4	C	00001044	2	434	319												
PRTNAME	C	00001033	8	432	313												
PRTNUM	C	00001018	3	430	311												
R0	U	00000000	1	4614	125	175	178	198	200	201	202	207	231	233	234	235	240
					259	260	285	286	324	325	328	344	347	349	351	353	368
R1	U	00000001	1	4615	208	241	266	267	295	296	326	358	372	594	595	596	597
					624	625	626	627	654	655	656	657	684	685	686	687	716
					717	718	719	746	747	748	749	776	777	778	779	806	807
					808	809	837	838	839	840	867	868	869	870	897	898	899
					900	927	928	929	930	958	959	960	961	988	989	990	991
					1018	1019	1020	1021	1048	1049	1050	1051	1079	1080	1081	1082	1109
					1110	1111	1112	1139	1140	1141	1142	1169	1170	1171	1172	1203	1204
					1205	1206	1233	1234	1235	1236	1263	1264	1265	1266	1293	1294	1295
					1296	1324	1325	1326	1327	1354	1355	1356	1357	1384	1385	1386	1387
					1414	1415	1416	1417	1445	1446	1447	1448	1475	1476	1477	1478	1505
					1506	1507	1508	1535	1536	1537	1538	1566	1567	1568	1569	1596	1597
					1598	1599	1626	1627	1628	1629	1656	1657	1658	1659	1687	1688	1689
					1690	1717	1718	1719	1720	1747	1748	1749	1750	1777	1778	1779	1780
					1811	1812	1813	1814	1841	1842	1843	1844	1871	1872	1873	1874	1901
					1902	1903	1904	1932	1933	1934	1935	1962	1963	1964	1965	1992	1993
					1994	1995	2022	2023	2024	2025	2053	2054	2055	2056	2083	2084	2085
					2086	2113	2114	2115	2116	2143	2144	2145	2146	2174	2175	2176	2177

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					2204	2205	2206	2207	2234	2235	2236	2237	2264	2265	2266	2267	2295
					2296	2297	2298	2325	2326	2327	2328	2355	2356	2357	2358	2385	2386
					2387	2388	2419	2420	2421	2422	2449	2450	2451	2452	2479	2480	2481
					2482	2509	2510	2511	2512	2540	2541	2542	2543	2570	2571	2572	2573
					2600	2601	2602	2603	2630	2631	2632	2633	2661	2662	2663	2664	2691
					2692	2693	2694	2721	2722	2723	2724	2751	2752	2753	2754	2782	2783
					2784	2785	2812	2813	2814	2815	2842	2843	2844	2845	2872	2873	2874
					2875	2902	2903	2904	2905	2936	2937	2938	2939	2966	2967	2968	2969
					2996	2997	2998	2999	3026	3027	3028	3029	3057	3058	3059	3060	3087
					3088	3089	3090	3117	3118	3119	3120	3147	3148	3149	3150	3178	3179
					3180	3181	3208	3209	3210	3211	3238	3239	3240	3241	3268	3269	3270
					3271	3299	3300	3301	3302	3329	3330	3331	3332	3359	3360	3361	3362
					3389	3390	3391	3392	3419	3420	3421	3422	3453	3454	3455	3456	3483
					3484	3485	3486	3513	3514	3515	3516	3543	3544	3545	3546	3574	3575
					3576	3577	3604	3605	3606	3607	3634	3635	3636	3637	3664	3665	3666
					3667	3695	3696	3697	3698	3725	3726	3727	3728	3755	3756	3757	3758
					3785	3786	3787	3788	3816	3817	3818	3819	3846	3847	3848	3849	3876
					3877	3878	3879	3906	3907	3908	3909	3936	3937	3938	3939	3970	3971
					3972	3973	4000	4001	4002	4003	4030	4031	4032	4033	4060	4061	4062
					4063	4091	4092	4093	4094	4121	4122	4123	4124	4151	4152	4153	4154
					4181	4182	4183	4184	4212	4213	4214	4215	4242	4243	4244	4245	4272
					4273	4274	4275	4302	4303	4304	4305	4333	4334	4335	4336	4363	4364
					4365	4366	4393	4394	4395	4396	4423	4424	4425	4426	4453	4454	4455
					4456												
R10	U	0000000A	1	4624	163	172	173										
R11	U	0000000B	1	4625	263	264	600	630	660	690	722	752	782	812	843	873	903
					933	964	994	1024	1054	1085	1115	1145	1175	1209	1239	1269	1299
					1330	1360	1390	1420	1451	1481	1511	1541	1572	1602	1632	1662	1693
					1723	1753	1783	1817	1847	1877	1907	1938	1968	1998	2028	2059	2089
					2119	2149	2180	2210	2240	2270	2301	2331	2361	2391	2425	2455	2485
					2515	2546	2576	2606	2636	2667	2697	2727	2757	2788	2818	2848	2878
					2908	2942	2972	3002	3032	3063	3093	3123	3153	3184	3214	3244	3274
					3305	3335	3365	3395	3425	3459	3489	3519	3549	3580	3610	3640	3670
					3701	3731	3761	3791	3822	3852	3882	3912	3942	3976	4006	4036	4066
					4097	4127	4157	4187	4218	4248	4278	4308	4339	4369	4399	4429	4459
R12	U	0000000C	1	4626	250	253	270	288									
R13	U	0000000D	1	4627													
R14	U	0000000E	1	4628													
R15	U	0000000F	1	4629	279	304	331	332									
R2	U	00000002	1	4616	209	242	307	308	315	316	324	327	328	345	347	353	354
					355	357	363	368	369								
R3	U	00000003	1	4617													
R4	U	00000004	1	4618													
R5	U	00000005	1	4619	253	254	257	305	330	579	602	609	632	639	662	669	692
					701	724	731	754	761	784	791	814	822	845	852	875	882
					905	912	935	943	966	973	996	1003	1026	1033	1056	1064	1087
					1094	1117	1124	1147	1154	1177	1188	1211	1218	1241	1248	1271	1278
					1301	1309	1332	1339	1362	1369	1392	1399	1422	1430	1453	1460	1483
					1490	1513	1520	1543	1551	1574	1581	1604	1611	1634	1641	1664	1672
					1695	1702	1725	1732	1755	1762	1785	1796	1819	1826	1849	1856	1879
					1886	1909	1917	1940	1947	1970	1977	2000	2007	2030	2038	2061	2068
					2091	2098	2121	2128	2151	2159	2182	2189	2212	2219	2242	2249	2272
					2280	2303	2310	2333	2340	2363	2370	2393	2404	2427	2434	2457	2464
					2487	2494	2517	2525	2548	2555	2578	2585	2608	2615	2638	2646	2669
					2676	2699	2706	2729	2736	2759	2767	2790	2797	2820	2827	2850	2857
					2880	2887	2910	2921	2944	2951	2974	2981	3004	3011	3034	3042	3065

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES											
					3072	3095	3102	3125	3132	3155	3163	3186	3193	3216	3223	3246	3253
					3276	3284	3307	3314	3337	3344	3367	3374	3397	3404	3427	3438	3461
					3468	3491	3498	3521	3528	3551	3559	3582	3589	3612	3619	3642	3649
					3672	3680	3703	3710	3733	3740	3763	3770	3793	3801	3824	3831	3854
					3861	3884	3891	3914	3921	3944	3955	3978	3985	4008	4015	4038	4045
					4068	4076	4099	4106	4129	4136	4159	4166	4189	4197	4220	4227	4250
					4257	4280	4287	4310	4318	4341	4348	4371	4378	4401	4408	4431	4438
					4461												
R6	U	00000006	1	4620													
R7	U	00000007	1	4621													
R8	U	00000008	1	4622	161	165	166	167	169								
R9	U	00000009	1	4623	162	169	170	172									
RE1	F	00001120	4	601	585	586	588										
RE10	F	00001678	4	874	858	859	861										
RE100	F	00004BE8	4	3611	3595	3596	3598										
RE101	F	00004C80	4	3641	3625	3626	3628										
RE102	F	00004D18	4	3671	3655	3656	3658										
RE103	F	00004DB0	4	3702	3686	3687	3689										
RE104	F	00004E48	4	3732	3716	3717	3719										
RE105	F	00004EE0	4	3762	3746	3747	3749										
RE106	F	00004F78	4	3792	3776	3777	3779										
RE107	F	00005010	4	3823	3807	3808	3810										
RE108	F	000050A8	4	3853	3837	3838	3840										
RE109	F	00005140	4	3883	3867	3868	3870										
RE11	F	00001710	4	904	888	889	891										
RE110	F	000051D8	4	3913	3897	3898	3900										
RE111	F	00005270	4	3943	3927	3928	3930										
RE112	F	00005308	4	3977	3961	3962	3964										
RE113	F	000053A0	4	4007	3991	3992	3994										
RE114	F	00005438	4	4037	4021	4022	4024										
RE115	F	000054D0	4	4067	4051	4052	4054										
RE116	F	00005568	4	4098	4082	4083	4085										
RE117	F	00005600	4	4128	4112	4113	4115										
RE118	F	00005698	4	4158	4142	4143	4145										
RE119	F	00005730	4	4188	4172	4173	4175										
RE12	F	000017A8	4	934	918	919	921										
RE120	F	000057C8	4	4219	4203	4204	4206										
RE121	F	00005860	4	4249	4233	4234	4236										
RE122	F	000058F8	4	4279	4263	4264	4266										
RE123	F	00005990	4	4309	4293	4294	4296										
RE124	F	00005A28	4	4340	4324	4325	4327										
RE125	F	00005AC0	4	4370	4354	4355	4357										
RE126	F	00005B58	4	4400	4384	4385	4387										
RE127	F	00005BF0	4	4430	4414	4415	4417										
RE128	F	00005C88	4	4460	4444	4445	4447										
RE13	F	00001840	4	965	949	950	952										
RE14	F	000018D8	4	995	979	980	982										
RE15	F	00001970	4	1025	1009	1010	1012										
RE16	F	00001A08	4	1055	1039	1040	1042										
RE17	F	00001AA0	4	1086	1070	1071	1073										
RE18	F	00001B38	4	1116	1100	1101	1103										
RE19	F	00001BD0	4	1146	1130	1131	1133										
RE2	F	000011B8	4	631	615	616	618										
RE20	F	00001C68	4	1176	1160	1161	1163										
RE21	F	00001D00	4	1210	1194	1195	1197										
RE22	F	00001D98	4	1240	1224	1225	1227										

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
RE23	F	00001E30	4	1270	1254	1255	1257
RE24	F	00001EC8	4	1300	1284	1285	1287
RE25	F	00001F60	4	1331	1315	1316	1318
RE26	F	00001FF8	4	1361	1345	1346	1348
RE27	F	00002090	4	1391	1375	1376	1378
RE28	F	00002128	4	1421	1405	1406	1408
RE29	F	000021C0	4	1452	1436	1437	1439
RE3	F	00001250	4	661	645	646	648
RE30	F	00002258	4	1482	1466	1467	1469
RE31	F	000022F0	4	1512	1496	1497	1499
RE32	F	00002388	4	1542	1526	1527	1529
RE33	F	00002420	4	1573	1557	1558	1560
RE34	F	000024B8	4	1603	1587	1588	1590
RE35	F	00002550	4	1633	1617	1618	1620
RE36	F	000025E8	4	1663	1647	1648	1650
RE37	F	00002680	4	1694	1678	1679	1681
RE38	F	00002718	4	1724	1708	1709	1711
RE39	F	000027B0	4	1754	1738	1739	1741
RE4	F	000012E8	4	691	675	676	678
RE40	F	00002848	4	1784	1768	1769	1771
RE41	F	000028E0	4	1818	1802	1803	1805
RE42	F	00002978	4	1848	1832	1833	1835
RE43	F	00002A10	4	1878	1862	1863	1865
RE44	F	00002AA8	4	1908	1892	1893	1895
RE45	F	00002B40	4	1939	1923	1924	1926
RE46	F	00002BD8	4	1969	1953	1954	1956
RE47	F	00002C70	4	1999	1983	1984	1986
RE48	F	00002D08	4	2029	2013	2014	2016
RE49	F	00002DA0	4	2060	2044	2045	2047
RE5	F	00001380	4	723	707	708	710
RE50	F	00002E38	4	2090	2074	2075	2077
RE51	F	00002ED0	4	2120	2104	2105	2107
RE52	F	00002F68	4	2150	2134	2135	2137
RE53	F	00003000	4	2181	2165	2166	2168
RE54	F	00003098	4	2211	2195	2196	2198
RE55	F	00003130	4	2241	2225	2226	2228
RE56	F	000031C8	4	2271	2255	2256	2258
RE57	F	00003260	4	2302	2286	2287	2289
RE58	F	000032F8	4	2332	2316	2317	2319
RE59	F	00003390	4	2362	2346	2347	2349
RE6	F	00001418	4	753	737	738	740
RE60	F	00003428	4	2392	2376	2377	2379
RE61	F	000034C0	4	2426	2410	2411	2413
RE62	F	00003558	4	2456	2440	2441	2443
RE63	F	000035F0	4	2486	2470	2471	2473
RE64	F	00003688	4	2516	2500	2501	2503
RE65	F	00003720	4	2547	2531	2532	2534
RE66	F	000037B8	4	2577	2561	2562	2564
RE67	F	00003850	4	2607	2591	2592	2594
RE68	F	000038E8	4	2637	2621	2622	2624
RE69	F	00003980	4	2668	2652	2653	2655
RE7	F	000014B0	4	783	767	768	770
RE70	F	00003A18	4	2698	2682	2683	2685
RE71	F	00003AB0	4	2728	2712	2713	2715
RE72	F	00003B48	4	2758	2742	2743	2745
RE73	F	00003BE0	4	2789	2773	2774	2776

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
RE74	F	00003C78	4	2819	2803	2804	2806
RE75	F	00003D10	4	2849	2833	2834	2836
RE76	F	00003DA8	4	2879	2863	2864	2866
RE77	F	00003E40	4	2909	2893	2894	2896
RE78	F	00003ED8	4	2943	2927	2928	2930
RE79	F	00003F70	4	2973	2957	2958	2960
RE8	F	00001548	4	813	797	798	800
RE80	F	00004008	4	3003	2987	2988	2990
RE81	F	000040A0	4	3033	3017	3018	3020
RE82	F	00004138	4	3064	3048	3049	3051
RE83	F	000041D0	4	3094	3078	3079	3081
RE84	F	00004268	4	3124	3108	3109	3111
RE85	F	00004300	4	3154	3138	3139	3141
RE86	F	00004398	4	3185	3169	3170	3172
RE87	F	00004430	4	3215	3199	3200	3202
RE88	F	000044C8	4	3245	3229	3230	3232
RE89	F	00004560	4	3275	3259	3260	3262
RE9	F	000015E0	4	844	828	829	831
RE90	F	000045F8	4	3306	3290	3291	3293
RE91	F	00004690	4	3336	3320	3321	3323
RE92	F	00004728	4	3366	3350	3351	3353
RE93	F	000047C0	4	3396	3380	3381	3383
RE94	F	00004858	4	3426	3410	3411	3413
RE95	F	000048F0	4	3460	3444	3445	3447
RE96	F	00004988	4	3490	3474	3475	3477
RE97	F	00004A20	4	3520	3504	3505	3507
RE98	F	00004AB8	4	3550	3534	3535	3537
RE99	F	00004B50	4	3581	3565	3566	3568
REA1	A	000010D4	4	588			
REA10	A	0000162C	4	861			
REA100	A	00004B9C	4	3598			
REA101	A	00004C34	4	3628			
REA102	A	00004CCC	4	3658			
REA103	A	00004D64	4	3689			
REA104	A	00004DFC	4	3719			
REA105	A	00004E94	4	3749			
REA106	A	00004F2C	4	3779			
REA107	A	00004FC4	4	3810			
REA108	A	0000505C	4	3840			
REA109	A	000050F4	4	3870			
REA11	A	000016C4	4	891			
REA110	A	0000518C	4	3900			
REA111	A	00005224	4	3930			
REA112	A	000052BC	4	3964			
REA113	A	00005354	4	3994			
REA114	A	000053EC	4	4024			
REA115	A	00005484	4	4054			
REA116	A	0000551C	4	4085			
REA117	A	000055B4	4	4115			
REA118	A	0000564C	4	4145			
REA119	A	000056E4	4	4175			
REA12	A	0000175C	4	921			
REA120	A	0000577C	4	4206			
REA121	A	00005814	4	4236			
REA122	A	000058AC	4	4266			
REA123	A	00005944	4	4296			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA124	A	000059DC	4	4327	
REA125	A	00005A74	4	4357	
REA126	A	00005B0C	4	4387	
REA127	A	00005BA4	4	4417	
REA128	A	00005C3C	4	4447	
REA13	A	000017F4	4	952	
REA14	A	0000188C	4	982	
REA15	A	00001924	4	1012	
REA16	A	000019BC	4	1042	
REA17	A	00001A54	4	1073	
REA18	A	00001AEC	4	1103	
REA19	A	00001B84	4	1133	
REA2	A	0000116C	4	618	
REA20	A	00001C1C	4	1163	
REA21	A	00001CB4	4	1197	
REA22	A	00001D4C	4	1227	
REA23	A	00001DE4	4	1257	
REA24	A	00001E7C	4	1287	
REA25	A	00001F14	4	1318	
REA26	A	00001FAC	4	1348	
REA27	A	00002044	4	1378	
REA28	A	000020DC	4	1408	
REA29	A	00002174	4	1439	
REA3	A	00001204	4	648	
REA30	A	0000220C	4	1469	
REA31	A	000022A4	4	1499	
REA32	A	0000233C	4	1529	
REA33	A	000023D4	4	1560	
REA34	A	0000246C	4	1590	
REA35	A	00002504	4	1620	
REA36	A	0000259C	4	1650	
REA37	A	00002634	4	1681	
REA38	A	000026CC	4	1711	
REA39	A	00002764	4	1741	
REA4	A	0000129C	4	678	
REA40	A	000027FC	4	1771	
REA41	A	00002894	4	1805	
REA42	A	0000292C	4	1835	
REA43	A	000029C4	4	1865	
REA44	A	00002A5C	4	1895	
REA45	A	00002AF4	4	1926	
REA46	A	00002B8C	4	1956	
REA47	A	00002C24	4	1986	
REA48	A	00002CBC	4	2016	
REA49	A	00002D54	4	2047	
REA5	A	00001334	4	710	
REA50	A	00002DEC	4	2077	
REA51	A	00002E84	4	2107	
REA52	A	00002F1C	4	2137	
REA53	A	00002FB4	4	2168	
REA54	A	0000304C	4	2198	
REA55	A	000030E4	4	2228	
REA56	A	0000317C	4	2258	
REA57	A	00003214	4	2289	
REA58	A	000032AC	4	2319	
REA59	A	00003344	4	2349	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA6	A	000013CC	4	740		
REA60	A	000033DC	4	2379		
REA61	A	00003474	4	2413		
REA62	A	0000350C	4	2443		
REA63	A	000035A4	4	2473		
REA64	A	0000363C	4	2503		
REA65	A	000036D4	4	2534		
REA66	A	0000376C	4	2564		
REA67	A	00003804	4	2594		
REA68	A	0000389C	4	2624		
REA69	A	00003934	4	2655		
REA7	A	00001464	4	770		
REA70	A	000039CC	4	2685		
REA71	A	00003A64	4	2715		
REA72	A	00003AFC	4	2745		
REA73	A	00003B94	4	2776		
REA74	A	00003C2C	4	2806		
REA75	A	00003CC4	4	2836		
REA76	A	00003D5C	4	2866		
REA77	A	00003DF4	4	2896		
REA78	A	00003E8C	4	2930		
REA79	A	00003F24	4	2960		
REA8	A	000014FC	4	800		
REA80	A	00003FBC	4	2990		
REA81	A	00004054	4	3020		
REA82	A	000040EC	4	3051		
REA83	A	00004184	4	3081		
REA84	A	0000421C	4	3111		
REA85	A	000042B4	4	3141		
REA86	A	0000434C	4	3172		
REA87	A	000043E4	4	3202		
REA88	A	0000447C	4	3232		
REA89	A	00004514	4	3262		
REA9	A	00001594	4	831		
REA90	A	000045AC	4	3293		
REA91	A	00004644	4	3323		
REA92	A	000046DC	4	3353		
REA93	A	00004774	4	3383		
REA94	A	0000480C	4	3413		
REA95	A	000048A4	4	3447		
REA96	A	0000493C	4	3477		
REA97	A	000049D4	4	3507		
REA98	A	00004A6C	4	3537		
REA99	A	00004B04	4	3568		
READDR	A	0000001C	4	470	266	
REG2LOW	U	000000DD	1	413		
REG2PATT	U	AABBCCDD	1	412		
RELEN	A	00000018	4	469		
RPTDWSAV	D	00000448	8	337	324	328
RPTERROR	I	000003DC	4	304	279	
RPTSAVE	F	00000440	4	334	304	331
RPTSVR5	F	00000444	4	335	305	330
SKL0001	U	0000004E	1	191	207	
SKL0002	U	0000004E	1	224	240	
SKT0001	C	0000022A	20	188	191	208
SKT0002	C	000002D4	20	221	224	241

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SVOLDPSW	U	00000140	0	127	
T1	A	000010B8	4	580	4475
T10	A	00001610	4	853	4484
T100	A	00004B80	4	3590	4574
T101	A	00004C18	4	3620	4575
T102	A	00004CB0	4	3650	4576
T103	A	00004D48	4	3681	4577
T104	A	00004DE0	4	3711	4578
T105	A	00004E78	4	3741	4579
T106	A	00004F10	4	3771	4580
T107	A	00004FA8	4	3802	4581
T108	A	00005040	4	3832	4582
T109	A	000050D8	4	3862	4583
T11	A	000016A8	4	883	4485
T110	A	00005170	4	3892	4584
T111	A	00005208	4	3922	4585
T112	A	000052A0	4	3956	4586
T113	A	00005338	4	3986	4587
T114	A	000053D0	4	4016	4588
T115	A	00005468	4	4046	4589
T116	A	00005500	4	4077	4590
T117	A	00005598	4	4107	4591
T118	A	00005630	4	4137	4592
T119	A	000056C8	4	4167	4593
T12	A	00001740	4	913	4486
T120	A	00005760	4	4198	4594
T121	A	000057F8	4	4228	4595
T122	A	00005890	4	4258	4596
T123	A	00005928	4	4288	4597
T124	A	000059C0	4	4319	4598
T125	A	00005A58	4	4349	4599
T126	A	00005AF0	4	4379	4600
T127	A	00005B88	4	4409	4601
T128	A	00005C20	4	4439	4602
T13	A	000017D8	4	944	4487
T14	A	00001870	4	974	4488
T15	A	00001908	4	1004	4489
T16	A	000019A0	4	1034	4490
T17	A	00001A38	4	1065	4491
T18	A	00001AD0	4	1095	4492
T19	A	00001B68	4	1125	4493
T2	A	00001150	4	610	4476
T20	A	00001C00	4	1155	4494
T21	A	00001C98	4	1189	4495
T22	A	00001D30	4	1219	4496
T23	A	00001DC8	4	1249	4497
T24	A	00001E60	4	1279	4498
T25	A	00001EF8	4	1310	4499
T26	A	00001F90	4	1340	4500
T27	A	00002028	4	1370	4501
T28	A	000020C0	4	1400	4502
T29	A	00002158	4	1431	4503
T3	A	000011E8	4	640	4477
T30	A	000021F0	4	1461	4504
T31	A	00002288	4	1491	4505
T32	A	00002320	4	1521	4506

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T33	A	000023B8	4	1552	4507
T34	A	00002450	4	1582	4508
T35	A	000024E8	4	1612	4509
T36	A	00002580	4	1642	4510
T37	A	00002618	4	1673	4511
T38	A	000026B0	4	1703	4512
T39	A	00002748	4	1733	4513
T4	A	00001280	4	670	4478
T40	A	000027E0	4	1763	4514
T41	A	00002878	4	1797	4515
T42	A	00002910	4	1827	4516
T43	A	000029A8	4	1857	4517
T44	A	00002A40	4	1887	4518
T45	A	00002AD8	4	1918	4519
T46	A	00002B70	4	1948	4520
T47	A	00002C08	4	1978	4521
T48	A	00002CA0	4	2008	4522
T49	A	00002D38	4	2039	4523
T5	A	00001318	4	702	4479
T50	A	00002DD0	4	2069	4524
T51	A	00002E68	4	2099	4525
T52	A	00002F00	4	2129	4526
T53	A	00002F98	4	2160	4527
T54	A	00003030	4	2190	4528
T55	A	000030C8	4	2220	4529
T56	A	00003160	4	2250	4530
T57	A	000031F8	4	2281	4531
T58	A	00003290	4	2311	4532
T59	A	00003328	4	2341	4533
T6	A	000013B0	4	732	4480
T60	A	000033C0	4	2371	4534
T61	A	00003458	4	2405	4535
T62	A	000034F0	4	2435	4536
T63	A	00003588	4	2465	4537
T64	A	00003620	4	2495	4538
T65	A	000036B8	4	2526	4539
T66	A	00003750	4	2556	4540
T67	A	000037E8	4	2586	4541
T68	A	00003880	4	2616	4542
T69	A	00003918	4	2647	4543
T7	A	00001448	4	762	4481
T70	A	000039B0	4	2677	4544
T71	A	00003A48	4	2707	4545
T72	A	00003AE0	4	2737	4546
T73	A	00003B78	4	2768	4547
T74	A	00003C10	4	2798	4548
T75	A	00003CA8	4	2828	4549
T76	A	00003D40	4	2858	4550
T77	A	00003DD8	4	2888	4551
T78	A	00003E70	4	2922	4552
T79	A	00003F08	4	2952	4553
T8	A	000014E0	4	792	4482
T80	A	00003FA0	4	2982	4554
T81	A	00004038	4	3012	4555
T82	A	000040D0	4	3043	4556
T83	A	00004168	4	3073	4557

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
T84	A	00004200	4	3103	4558	
T85	A	00004298	4	3133	4559	
T86	A	00004330	4	3164	4560	
T87	A	000043C8	4	3194	4561	
T88	A	00004460	4	3224	4562	
T89	A	000044F8	4	3254	4563	
T9	A	00001578	4	823	4483	
T90	A	00004590	4	3285	4564	
T91	A	00004628	4	3315	4565	
T92	A	000046C0	4	3345	4566	
T93	A	00004758	4	3375	4567	
T94	A	000047F0	4	3405	4568	
T95	A	00004888	4	3439	4569	
T96	A	00004920	4	3469	4570	
T97	A	000049B8	4	3499	4571	
T98	A	00004A50	4	3529	4572	
T99	A	00004AE8	4	3560	4573	
TESTING	F	00001004	4	424	260	
TNUM	H	00000004	2	462	259	307
TSUB	A	00000000	4	461	263	
TTABLE	F	00005CC0	4	4474		
V0	U	00000000	1	4635		
V1	U	00000001	1	4636	262	
V10	U	0000000A	1	4645		
V11	U	0000000B	1	4646		
V12	U	0000000C	1	4647		
V13	U	0000000D	1	4648		
V14	U	0000000E	1	4649		
V15	U	0000000F	1	4650		
V16	U	00000010	1	4651		
V17	U	00000011	1	4652		
V18	U	00000012	1	4653		
V19	U	00000013	1	4654		
V1FUDGE	X	00001094	16	453	262	
V101	X	000010E0	16	590	599	
V1010	X	00001638	16	863	872	
V10100	X	00004BA8	16	3600	3609	
V10101	X	00004C40	16	3630	3639	
V10102	X	00004CD8	16	3660	3669	
V10103	X	00004D70	16	3691	3700	
V10104	X	00004E08	16	3721	3730	
V10105	X	00004EA0	16	3751	3760	
V10106	X	00004F38	16	3781	3790	
V10107	X	00004FD0	16	3812	3821	
V10108	X	00005068	16	3842	3851	
V10109	X	00005100	16	3872	3881	
V1011	X	000016D0	16	893	902	
V10110	X	00005198	16	3902	3911	
V10111	X	00005230	16	3932	3941	
V10112	X	000052C8	16	3966	3975	
V10113	X	00005360	16	3996	4005	
V10114	X	000053F8	16	4026	4035	
V10115	X	00005490	16	4056	4065	
V10116	X	00005528	16	4087	4096	
V10117	X	000055C0	16	4117	4126	
V10118	X	00005658	16	4147	4156	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V10119	X	000056F0	16	4177	4186
V1012	X	00001768	16	923	932
V10120	X	00005788	16	4208	4217
V10121	X	00005820	16	4238	4247
V10122	X	000058B8	16	4268	4277
V10123	X	00005950	16	4298	4307
V10124	X	000059E8	16	4329	4338
V10125	X	00005A80	16	4359	4368
V10126	X	00005B18	16	4389	4398
V10127	X	00005BB0	16	4419	4428
V10128	X	00005C48	16	4449	4458
V1013	X	00001800	16	954	963
V1014	X	00001898	16	984	993
V1015	X	00001930	16	1014	1023
V1016	X	000019C8	16	1044	1053
V1017	X	00001A60	16	1075	1084
V1018	X	00001AF8	16	1105	1114
V1019	X	00001B90	16	1135	1144
V102	X	00001178	16	620	629
V1020	X	00001C28	16	1165	1174
V1021	X	00001CC0	16	1199	1208
V1022	X	00001D58	16	1229	1238
V1023	X	00001DF0	16	1259	1268
V1024	X	00001E88	16	1289	1298
V1025	X	00001F20	16	1320	1329
V1026	X	00001FB8	16	1350	1359
V1027	X	00002050	16	1380	1389
V1028	X	000020E8	16	1410	1419
V1029	X	00002180	16	1441	1450
V103	X	00001210	16	650	659
V1030	X	00002218	16	1471	1480
V1031	X	000022B0	16	1501	1510
V1032	X	00002348	16	1531	1540
V1033	X	000023E0	16	1562	1571
V1034	X	00002478	16	1592	1601
V1035	X	00002510	16	1622	1631
V1036	X	000025A8	16	1652	1661
V1037	X	00002640	16	1683	1692
V1038	X	000026D8	16	1713	1722
V1039	X	00002770	16	1743	1752
V104	X	000012A8	16	680	689
V1040	X	00002808	16	1773	1782
V1041	X	000028A0	16	1807	1816
V1042	X	00002938	16	1837	1846
V1043	X	000029D0	16	1867	1876
V1044	X	00002A68	16	1897	1906
V1045	X	00002B00	16	1928	1937
V1046	X	00002B98	16	1958	1967
V1047	X	00002C30	16	1988	1997
V1048	X	00002CC8	16	2018	2027
V1049	X	00002D60	16	2049	2058
V105	X	00001340	16	712	721
V1050	X	00002DF8	16	2079	2088
V1051	X	00002E90	16	2109	2118
V1052	X	00002F28	16	2139	2148
V1053	X	00002FC0	16	2170	2179

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1054	X	00003058	16	2200	2209
V1055	X	000030F0	16	2230	2239
V1056	X	00003188	16	2260	2269
V1057	X	00003220	16	2291	2300
V1058	X	000032B8	16	2321	2330
V1059	X	00003350	16	2351	2360
V106	X	000013D8	16	742	751
V1060	X	000033E8	16	2381	2390
V1061	X	00003480	16	2415	2424
V1062	X	00003518	16	2445	2454
V1063	X	000035B0	16	2475	2484
V1064	X	00003648	16	2505	2514
V1065	X	000036E0	16	2536	2545
V1066	X	00003778	16	2566	2575
V1067	X	00003810	16	2596	2605
V1068	X	000038A8	16	2626	2635
V1069	X	00003940	16	2657	2666
V107	X	00001470	16	772	781
V1070	X	000039D8	16	2687	2696
V1071	X	00003A70	16	2717	2726
V1072	X	00003B08	16	2747	2756
V1073	X	00003BA0	16	2778	2787
V1074	X	00003C38	16	2808	2817
V1075	X	00003CD0	16	2838	2847
V1076	X	00003D68	16	2868	2877
V1077	X	00003E00	16	2898	2907
V1078	X	00003E98	16	2932	2941
V1079	X	00003F30	16	2962	2971
V108	X	00001508	16	802	811
V1080	X	00003FC8	16	2992	3001
V1081	X	00004060	16	3022	3031
V1082	X	000040F8	16	3053	3062
V1083	X	00004190	16	3083	3092
V1084	X	00004228	16	3113	3122
V1085	X	000042C0	16	3143	3152
V1086	X	00004358	16	3174	3183
V1087	X	000043F0	16	3204	3213
V1088	X	00004488	16	3234	3243
V1089	X	00004520	16	3264	3273
V109	X	000015A0	16	833	842
V1090	X	000045B8	16	3295	3304
V1091	X	00004650	16	3325	3334
V1092	X	000046E8	16	3355	3364
V1093	X	00004780	16	3385	3394
V1094	X	00004818	16	3415	3424
V1095	X	000048B0	16	3449	3458
V1096	X	00004948	16	3479	3488
V1097	X	000049E0	16	3509	3518
V1098	X	00004A78	16	3539	3548
V1099	X	00004B10	16	3570	3579
V10UTPUT	X	00000028	16	472	267
V2	U	00000002	1	4637	
V20	U	00000014	1	4655	
V21	U	00000015	1	4656	
V22	U	00000016	1	4657	595 598 599 625 628 629 655 658 659 685 688 689 717
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
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					1385	1388	1389	1415	1418	1419	1446	1449	1450	1476	1479	1480	1506
					1509	1510	1536	1539	1540	1567	1570	1571	1597	1600	1601	1627	1630
					1631	1657	1660	1661	1688	1691	1692	1718	1721	1722	1748	1751	1752
					1778	1781	1782	1812	1815	1816	1842	1845	1846	1872	1875	1876	1902
					1905	1906	1933	1936	1937	1963	1966	1967	1993	1996	1997	2023	2026
					2027	2054	2057	2058	2084	2087	2088	2114	2117	2118	2144	2147	2148
					2175	2178	2179	2205	2208	2209	2235	2238	2239	2265	2268	2269	2296
					2299	2300	2326	2329	2330	2356	2359	2360	2386	2389	2390	2420	2423
					2424	2450	2453	2454	2480	2483	2484	2510	2513	2514	2541	2544	2545
					2571	2574	2575	2601	2604	2605	2631	2634	2635	2662	2665	2666	2692
					2695	2696	2722	2725	2726	2752	2755	2756	2783	2786	2787	2813	2816
					2817	2843	2846	2847	2873	2876	2877	2903	2906	2907	2937	2940	2941
					2967	2970	2971	2997	3000	3001	3027	3030	3031	3058	3061	3062	3088
					3091	3092	3118	3121	3122	3148	3151	3152	3179	3182	3183	3209	3212
					3213	3239	3242	3243	3269	3272	3273	3300	3303	3304	3330	3333	3334
					3360	3363	3364	3390	3393	3394	3420	3423	3424	3454	3457	3458	3484
					3487	3488	3514	3517	3518	3544	3547	3548	3575	3578	3579	3605	3608
					3609	3635	3638	3639	3665	3668	3669	3696	3699	3700	3726	3729	3730
					3756	3759	3760	3786	3789	3790	3817	3820	3821	3847	3850	3851	3877
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					4005	4031	4034	4035	4061	4064	4065	4092	4095	4096	4122	4125	4126
					4152	4155	4156	4182	4185	4186	4213	4216	4217	4243	4246	4247	4273
					4276	4277	4303	4306	4307	4334	4337	4338	4364	4367	4368	4394	4397
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V23	U	00000017	1	4658	597	598	627	628	657	658	687	688	719	720	749	750	779
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					991	992	1021	1022	1051	1052	1082	1083	1112	1113	1142	1143	1172
					1173	1206	1207	1236	1237	1266	1267	1296	1297	1327	1328	1357	1358
					1387	1388	1417	1418	1448	1449	1478	1479	1508	1509	1538	1539	1569
					1570	1599	1600	1629	1630	1659	1660	1690	1691	1720	1721	1750	1751
					1780	1781	1814	1815	1844	1845	1874	1875	1904	1905	1935	1936	1965
					1966	1995	1996	2025	2026	2056	2057	2086	2087	2116	2117	2146	2147
					2177	2178	2207	2208	2237	2238	2267	2268	2298	2299	2328	2329	2358
					2359	2388	2389	2422	2423	2452	2453	2482	2483	2512	2513	2543	2544
					2573	2574	2603	2604	2633	2634	2664	2665	2694	2695	2724	2725	2754
					2755	2785	2786	2815	2816	2845	2846	2875	2876	2905	2906	2939	2940
					2969	2970	2999	3000	3029	3030	3060	3061	3090	3091	3120	3121	3150
					3151	3181	3182	3211	3212	3241	3242	3271	3272	3302	3303	3332	3333
					3362	3363	3392	3393	3422	3423	3456	3457	3486	3487	3516	3517	3546
					3547	3577	3578	3607	3608	3637	3638	3667	3668	3698	3699	3728	3729
					3758	3759	3788	3789	3819	3820	3849	3850	3879	3880	3909	3910	3939
					3940	3973	3974	4003	4004	4033	4034	4063	4064	4094	4095	4124	4125
					4154	4155	4184	4185	4215	4216	4245	4246	4275	4276	4305	4306	4336
					4337	4366	4367	4396	4397	4426	4427	4456	4457				
V24	U	00000018	1	4659													
V25	U	00000019	1	4660													
V26	U	0000001A	1	4661													
V27	U	0000001B	1	4662													
V28	U	0000001C	1	4663													
V29	U	0000001D	1	4664													
V2ADDR	A	00000010	4	467	594	624	654	684	716	746	776	806	837	867	897	927	958
					988	1018	1048	1079	1109	1139	1169	1203	1233	1263	1293	1324	1354

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					1384	1414	1445	1475	1505	1535	1566	1596	1626	1656	1687	1717	1747
					1777	1811	1841	1871	1901	1932	1962	1992	2022	2053	2083	2113	2143
					2174	2204	2234	2264	2295	2325	2355	2385	2419	2449	2479	2509	2540
					2570	2600	2630	2661	2691	2721	2751	2782	2812	2842	2872	2902	2936
					2966	2996	3026	3057	3087	3117	3147	3178	3208	3238	3268	3299	3329
					3359	3389	3419	3453	3483	3513	3543	3574	3604	3634	3664	3695	3725
					3755	3785	3816	3846	3876	3906	3936	3970	4000	4030	4060	4091	4121
					4151	4181	4212	4242	4272	4302	4333	4363	4393	4423	4453		
V3	U	00000003	1	4638													
V30	U	0000001E	1	4665													
V31	U	0000001F	1	4666													
V3ADDR	A	00000014	4	468	596	626	656	686	718	748	778	808	839	869	899	929	960
					990	1020	1050	1081	1111	1141	1171	1205	1235	1265	1295	1326	1356
					1386	1416	1447	1477	1507	1537	1568	1598	1628	1658	1689	1719	1749
					1779	1813	1843	1873	1903	1934	1964	1994	2024	2055	2085	2115	2145
					2176	2206	2236	2266	2297	2327	2357	2387	2421	2451	2481	2511	2542
					2572	2602	2632	2663	2693	2723	2753	2784	2814	2844	2874	2904	2938
					2968	2998	3028	3059	3089	3119	3149	3180	3210	3240	3270	3301	3331
					3361	3391	3421	3455	3485	3515	3545	3576	3606	3636	3666	3697	3727
					3757	3787	3818	3848	3878	3908	3938	3972	4002	4032	4062	4093	4123
					4153	4183	4214	4244	4274	4304	4335	4365	4395	4425	4455		
V4	U	00000004	1	4639													
V5	U	00000005	1	4640													
V6	U	00000006	1	4641													
V7	U	00000007	1	4642													
V8	U	00000008	1	4643													
V9	U	00000009	1	4644													
X0001	U	000002A8	1	197	185	198											
X0002	U	00000358	1	230	218	231											
X1	F	000010F8	4	593	580												
X10	F	00001650	4	866	853												
X100	F	00004BC0	4	3603	3590												
X101	F	00004C58	4	3633	3620												
X102	F	00004CF0	4	3663	3650												
X103	F	00004D88	4	3694	3681												
X104	F	00004E20	4	3724	3711												
X105	F	00004EB8	4	3754	3741												
X106	F	00004F50	4	3784	3771												
X107	F	00004FE8	4	3815	3802												
X108	F	00005080	4	3845	3832												
X109	F	00005118	4	3875	3862												
X11	F	000016E8	4	896	883												
X110	F	000051B0	4	3905	3892												
X111	F	00005248	4	3935	3922												
X112	F	000052E0	4	3969	3956												
X113	F	00005378	4	3999	3986												
X114	F	00005410	4	4029	4016												
X115	F	000054A8	4	4059	4046												
X116	F	00005540	4	4090	4077												
X117	F	000055D8	4	4120	4107												
X118	F	00005670	4	4150	4137												
X119	F	00005708	4	4180	4167												
X12	F	00001780	4	926	913												
X120	F	000057A0	4	4211	4198												
X121	F	00005838	4	4241	4228												
X122	F	000058D0	4	4271	4258												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X123	F	00005968	4	4301	4288
X124	F	00005A00	4	4332	4319
X125	F	00005A98	4	4362	4349
X126	F	00005B30	4	4392	4379
X127	F	00005BC8	4	4422	4409
X128	F	00005C60	4	4452	4439
X13	F	00001818	4	957	944
X14	F	000018B0	4	987	974
X15	F	00001948	4	1017	1004
X16	F	000019E0	4	1047	1034
X17	F	00001A78	4	1078	1065
X18	F	00001B10	4	1108	1095
X19	F	00001BA8	4	1138	1125
X2	F	00001190	4	623	610
X20	F	00001C40	4	1168	1155
X21	F	00001CD8	4	1202	1189
X22	F	00001D70	4	1232	1219
X23	F	00001E08	4	1262	1249
X24	F	00001EA0	4	1292	1279
X25	F	00001F38	4	1323	1310
X26	F	00001FD0	4	1353	1340
X27	F	00002068	4	1383	1370
X28	F	00002100	4	1413	1400
X29	F	00002198	4	1444	1431
X3	F	00001228	4	653	640
X30	F	00002230	4	1474	1461
X31	F	000022C8	4	1504	1491
X32	F	00002360	4	1534	1521
X33	F	000023F8	4	1565	1552
X34	F	00002490	4	1595	1582
X35	F	00002528	4	1625	1612
X36	F	000025C0	4	1655	1642
X37	F	00002658	4	1686	1673
X38	F	000026F0	4	1716	1703
X39	F	00002788	4	1746	1733
X4	F	000012C0	4	683	670
X40	F	00002820	4	1776	1763
X41	F	000028B8	4	1810	1797
X42	F	00002950	4	1840	1827
X43	F	000029E8	4	1870	1857
X44	F	00002A80	4	1900	1887
X45	F	00002B18	4	1931	1918
X46	F	00002BB0	4	1961	1948
X47	F	00002C48	4	1991	1978
X48	F	00002CE0	4	2021	2008
X49	F	00002D78	4	2052	2039
X5	F	00001358	4	715	702
X50	F	00002E10	4	2082	2069
X51	F	00002EA8	4	2112	2099
X52	F	00002F40	4	2142	2129
X53	F	00002FD8	4	2173	2160
X54	F	00003070	4	2203	2190
X55	F	00003108	4	2233	2220
X56	F	000031A0	4	2263	2250
X57	F	00003238	4	2294	2281
X58	F	000032D0	4	2324	2311

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
X59	F	00003368	4	2354	2341				
X6	F	000013F0	4	745	732				
X60	F	00003400	4	2384	2371				
X61	F	00003498	4	2418	2405				
X62	F	00003530	4	2448	2435				
X63	F	000035C8	4	2478	2465				
X64	F	00003660	4	2508	2495				
X65	F	000036F8	4	2539	2526				
X66	F	00003790	4	2569	2556				
X67	F	00003828	4	2599	2586				
X68	F	000038C0	4	2629	2616				
X69	F	00003958	4	2660	2647				
X7	F	00001488	4	775	762				
X70	F	000039F0	4	2690	2677				
X71	F	00003A88	4	2720	2707				
X72	F	00003B20	4	2750	2737				
X73	F	00003BB8	4	2781	2768				
X74	F	00003C50	4	2811	2798				
X75	F	00003CE8	4	2841	2828				
X76	F	00003D80	4	2871	2858				
X77	F	00003E18	4	2901	2888				
X78	F	00003EB0	4	2935	2922				
X79	F	00003F48	4	2965	2952				
X8	F	00001520	4	805	792				
X80	F	00003FE0	4	2995	2982				
X81	F	00004078	4	3025	3012				
X82	F	00004110	4	3056	3043				
X83	F	000041A8	4	3086	3073				
X84	F	00004240	4	3116	3103				
X85	F	000042D8	4	3146	3133				
X86	F	00004370	4	3177	3164				
X87	F	00004408	4	3207	3194				
X88	F	000044A0	4	3237	3224				
X89	F	00004538	4	3267	3254				
X9	F	000015B8	4	836	823				
X90	F	000045D0	4	3298	3285				
X91	F	00004668	4	3328	3315				
X92	F	00004700	4	3358	3345				
X93	F	00004798	4	3388	3375				
X94	F	00004830	4	3418	3405				
X95	F	000048C8	4	3452	3439				
X96	F	00004960	4	3482	3469				
X97	F	000049F8	4	3512	3499				
X98	F	00004A90	4	3542	3529				
X99	F	00004B28	4	3573	3560				
XC0001	U	000002D0	1	211	203				
XC0002	U	00000380	1	244	236				
ZVE7TST	J	00000000	24272	124	127	129	133	137	422	125
=A(E7TESTS)	A	0000054C	4	400	250				
=AL2(L'MSGMSG)	R	00000556	2	403	349				
=F'1'	F	00000550	4	401	285				
=F'2'	F	00000548	4	399	235				
=F'64'	F	00000544	4	398	202				
=H'0'	H	00000554	2	402	344				

MACRO	DEFN	REFERENCES															
FCHECK	77	184	217														
PTTABLE	536	4473															
VRR_C	491	577	607	637	667	699	729	759	789	820	850	880	910	941	971	1001	1031	1062
		1092	1122	1152	1186	1216	1246	1276	1307	1337	1367	1397	1428	1458	1488	1518	1549	1579
		1609	1639	1670	1700	1730	1760	1794	1824	1854	1884	1915	1945	1975	2005	2036	2066	2096
		2126	2157	2187	2217	2247	2278	2308	2338	2368	2402	2432	2462	2492	2523	2553	2583	2613
		2644	2674	2704	2734	2765	2795	2825	2855	2885	2919	2949	2979	3009	3040	3070	3100	3130
		3161	3191	3221	3251	3282	3312	3342	3372	3402	3436	3466	3496	3526	3557	3587	3617	3647
		3678	3708	3738	3768	3799	3829	3859	3889	3919	3953	3983	4013	4043	4074	4104	4134	4164
		4195	4225	4255	4285	4316	4346	4376	4406	4436								

DESC	SYMBOL	SIZE	POS	ADDR

Entry: 0

DESC	SYMBOL	SIZE	POS	ADDR
Image	IMAGE	24272	0000-5ECF	0000-5ECF
Region		24272	0000-5ECF	0000-5ECF
CSECT	ZVE7TST	24272	0000-5ECF	0000-5ECF

       STMT   FILE NAME

1   /home/tn529/sharedvfp/tests/zvector-e7-09-multiply.asm

** NO ERRORS FOUND **