南方科技大学
SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Project Sprint 1

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CATALOGUE
目录

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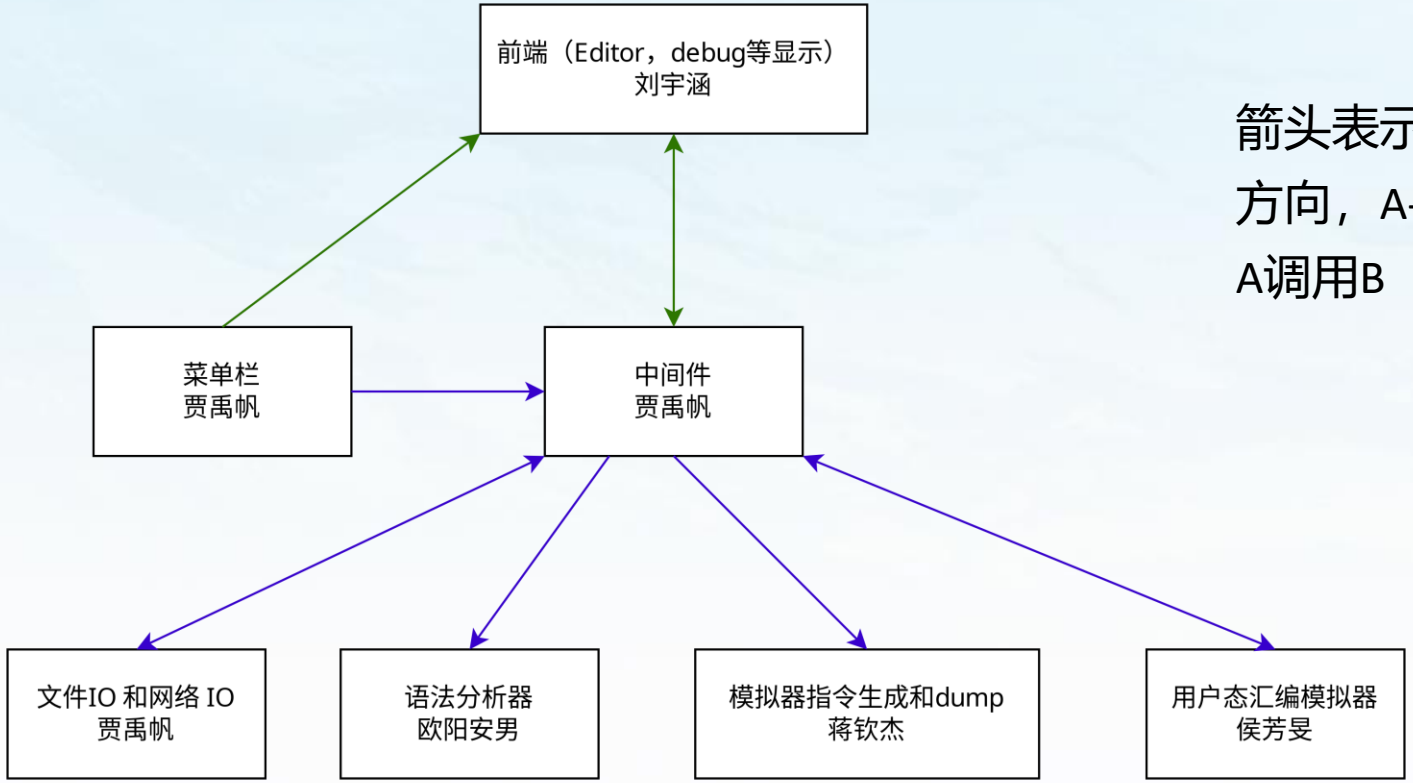
01

Structure

Task Assignment



箭头表示调用方向，A->B表示A调用B

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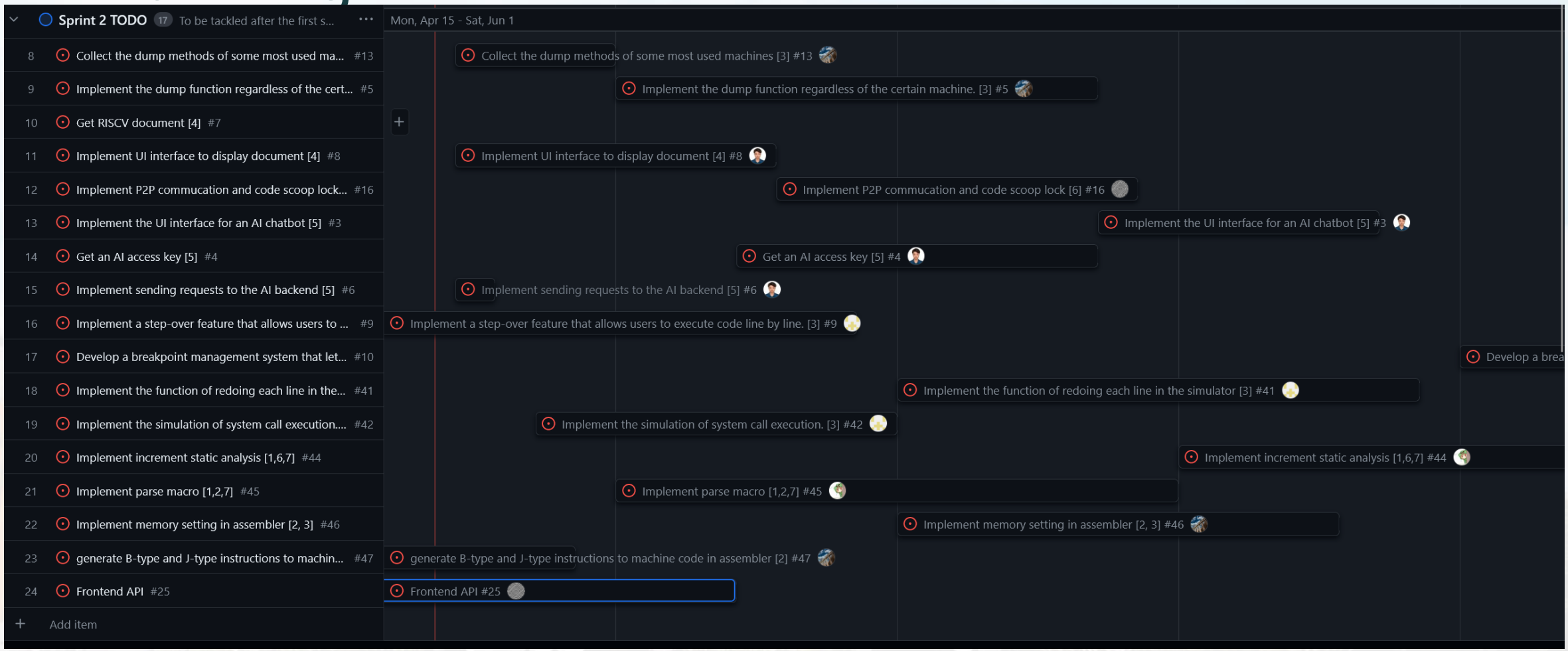
Planning



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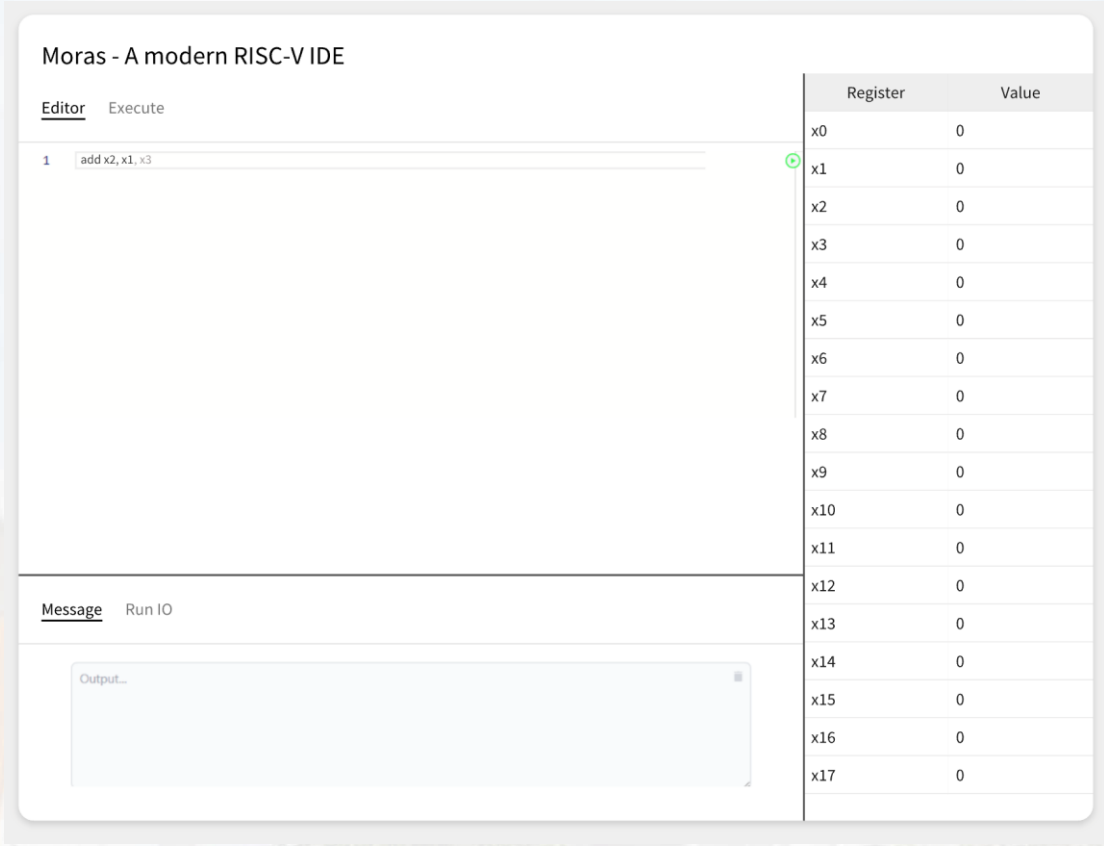
02

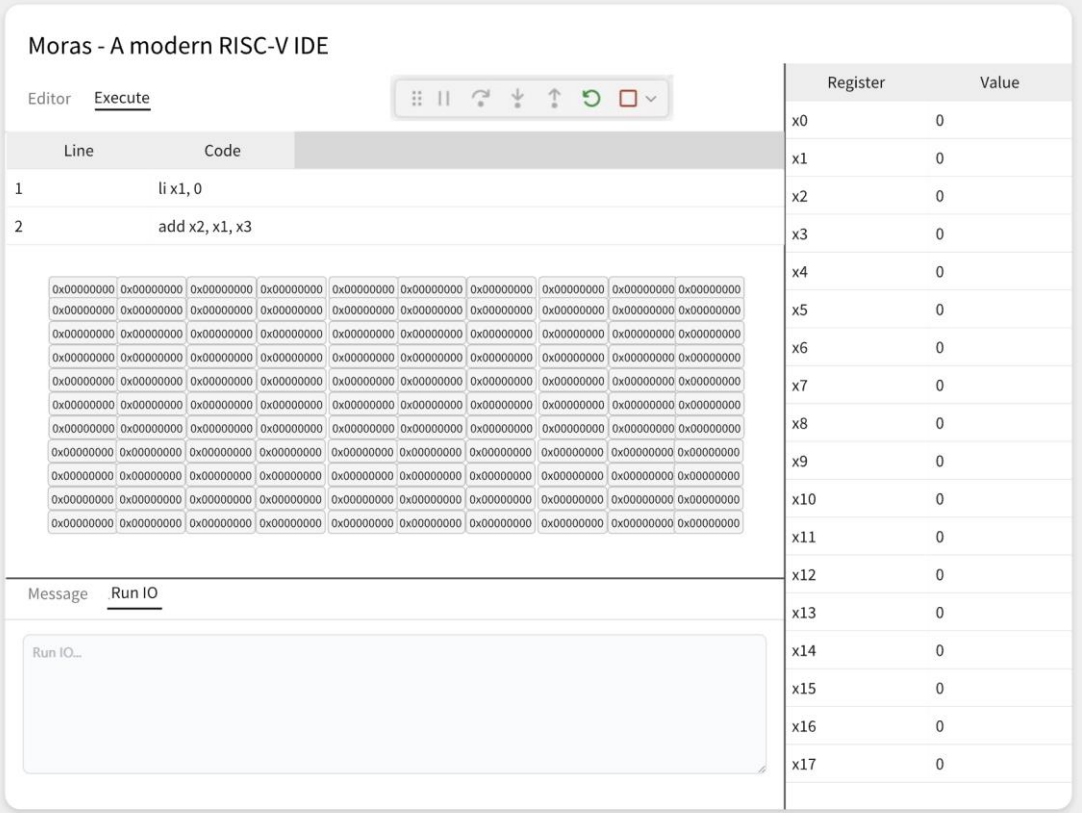
Demo & Deliverable

Architectural Design


```
.
├── README.md
├── docs                          // report and documents of our project
├── references                    // to add assembly document
├── src-tauri                     // backend
│   ├── Cargo.lock
│   ├── Cargo.toml
│   ├── build.rs
│   ├── src                       // backend source code root folder
│   │   ├── assembler
│   │   ├── interface             // interface of each components
│   │   │   ├── assembler.rs
│   │   │   ├── frontend.rs
│   │   │   ├── middleware.rs
│   │   │   ├── mod.rs
│   │   │   ├── parser.rs
│   │   │   ├── simulator.rs
│   │   │   └── storage.rs
│   │   ├── io
│   │   ├── main.rs               // entry of the backend
│   │   ├── menu
│   │   ├── middleware
│   │   ├── modules               // implemntation of each architecture
│   │   │   ├── mips              // mips
│   │   │   ├── mod.rs
│   │   │   └── riscv             // riscv
│   │   │       ├── basic         // basic file of each components (parser, assembler, s
│   │   │       ├── mod.rs
│   │   │       └── rv32i         // some constants of rv32i
│   │   │                         // to add more extension of riscv
│   │   ├── parser
│   │   ├── simulator
│   │   ├── storage
│   │   ├── types
│   │   └── utility
│   └── tauri.conf.json
└── src-ui                        // frontend
    ├── README.md
    ├── app
    │   ├── favicon.ico
    │   ├── globals.css
    │   ├── layout.js
    │   ├── page.js
    │   └── providers.jsx
    ├── components
    │   ├── Code.jsx
    │   ├── MessageIO.jsx
    │   ├── Register.jsx
    │   ├── Taskbar.jsx
    │   └── TestPage.jsx
    ├── jsconfig.json
    ├── next.config.mjs
    ├── package-lock.json
    ├── package.json
    ├── postcss.config.js
    └── tailwind.config.js
```

UI Design


Moras - A modern RISC-V IDE
Editor
Execute
1
add x2, x1, x3
Message
Run IO
Output...
Register
Value
x0 0
x1 0
x2 0
x3 0
x4 0
x5 0
x6 0
x7 0
x8 0
x9 0
x10 0
x11 0
x12 0
x13 0
x14 0
x15 0
x16 0
x17 0


Moras - A modern RISC-V IDE
Editor
Execute
Line
Code
1 li x1, 0
2 add x2, x1, x3
0x00000000
Message
Run IO
Run IO...
Register
Value
x0 0
x1 0
x2 0
x3 0
x4 0
x5 0
x6 0
x7 0
x8 0
x9 0
x10 0
x11 0
x12 0
x13 0
x14 0
x15 0
x16 0
x17 0

UI Design

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RISC-V Document UI

This is version 2.2 of the document describing the RISC-V user-level architecture. The document contains the following versions of the RISC-V ISA modules:

Base	Version	Frozen?
RV32I	2.0	Y
RV32E	1.9	N
RV64I	2.0	Y
RV128I	1.7	N
Extension	Version	Frozen?
M	2.0	Y
A	2.0	Y
F	2.0	Y
D	2.0	Y
Q	2.0	Y
L	0.0	N
C	2.0	Y
B	0.0	N
J	0.0	N
T	0.0	N
P	0.1	N
V	0.2	N
N	1.1	N

UI Demo

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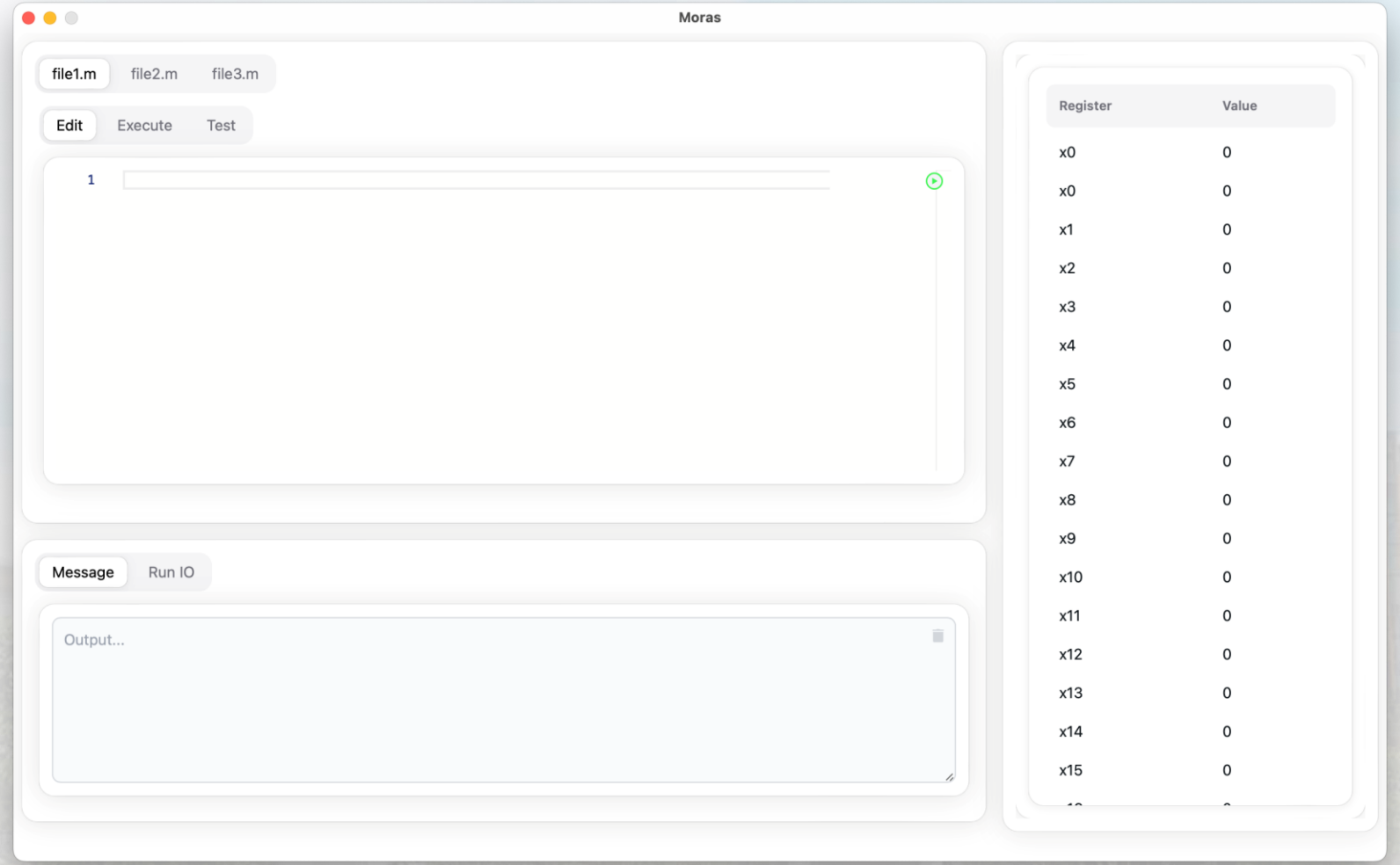

UI Demo

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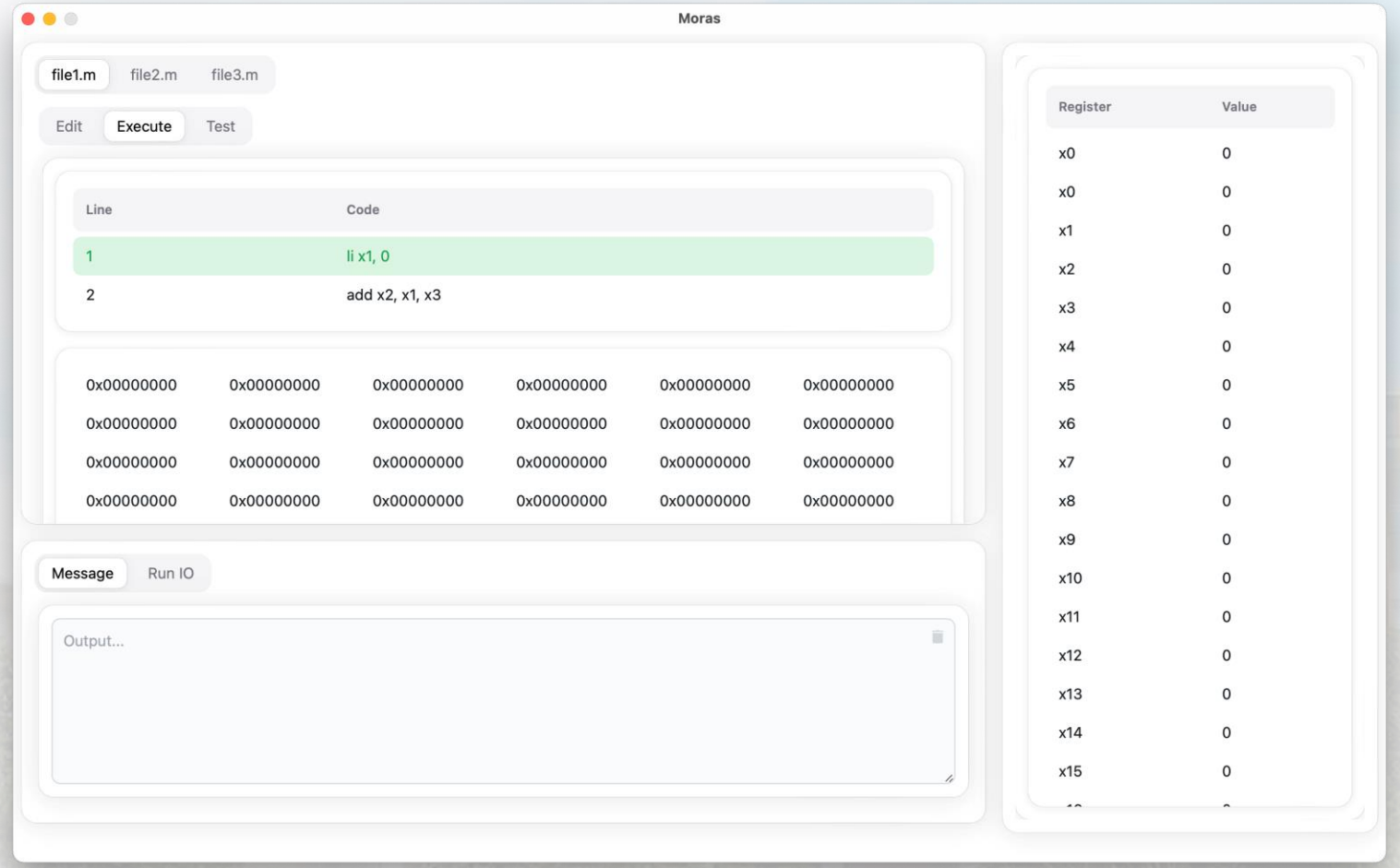

UI Demo

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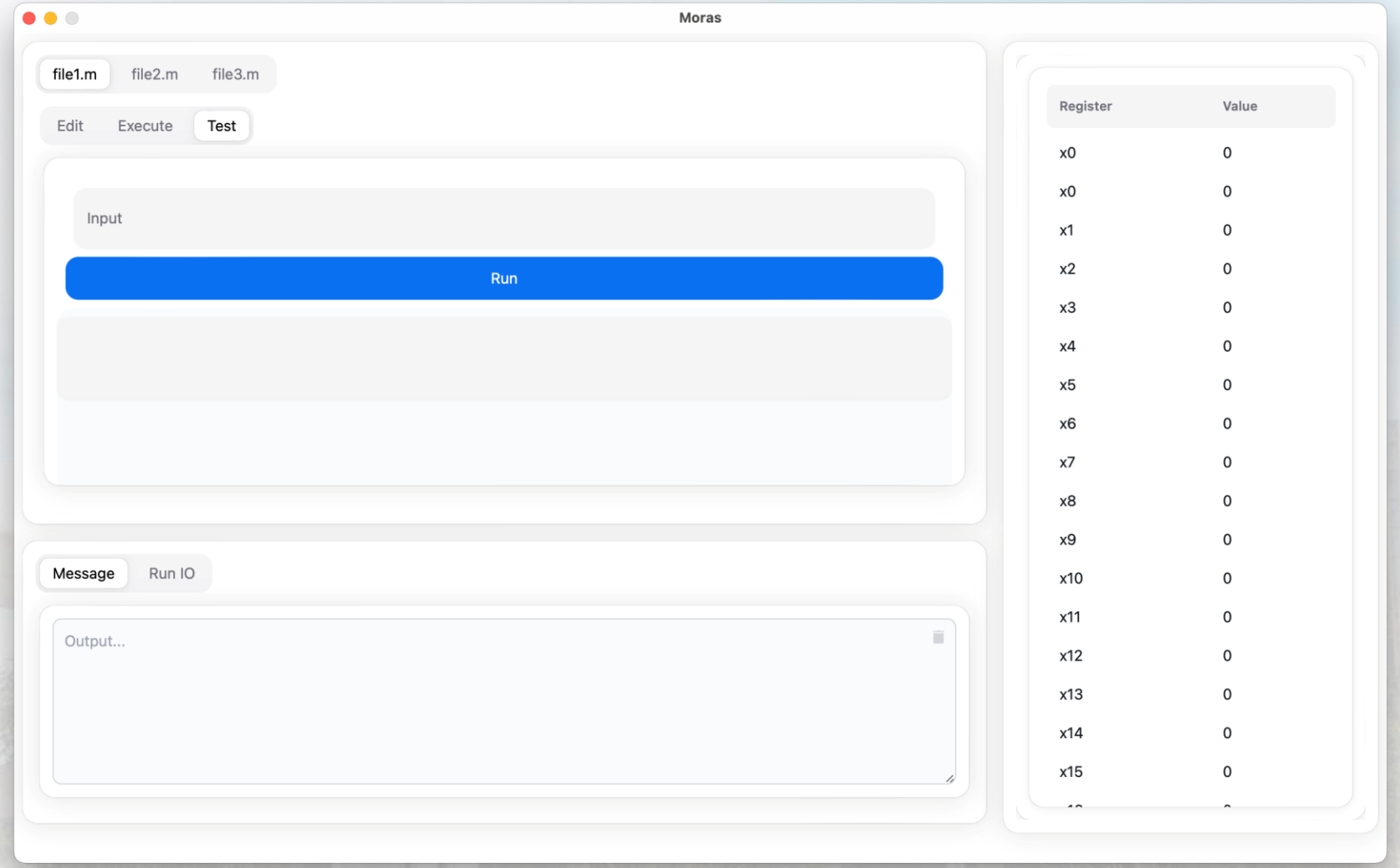

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Contribution

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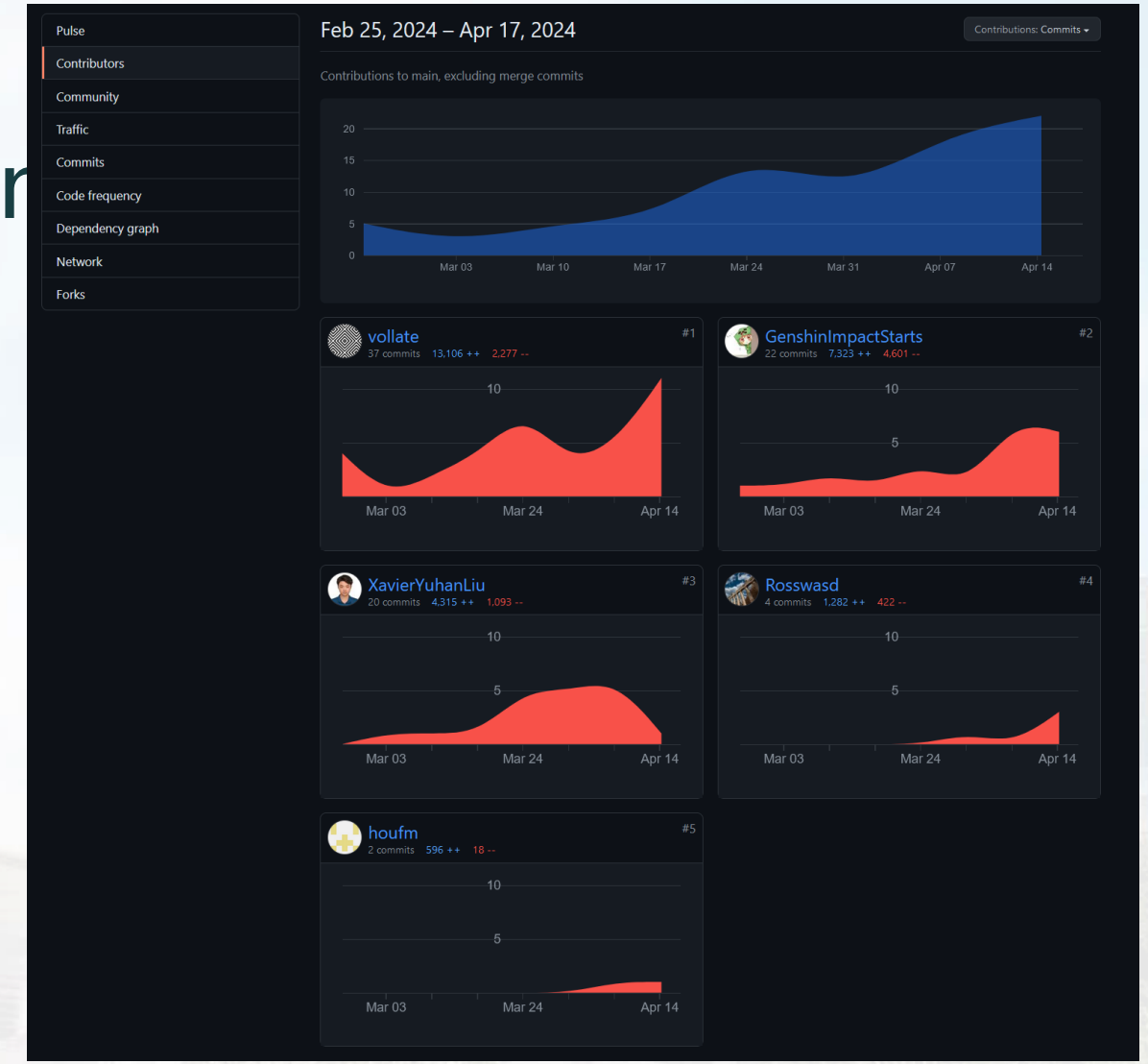
Collaboration



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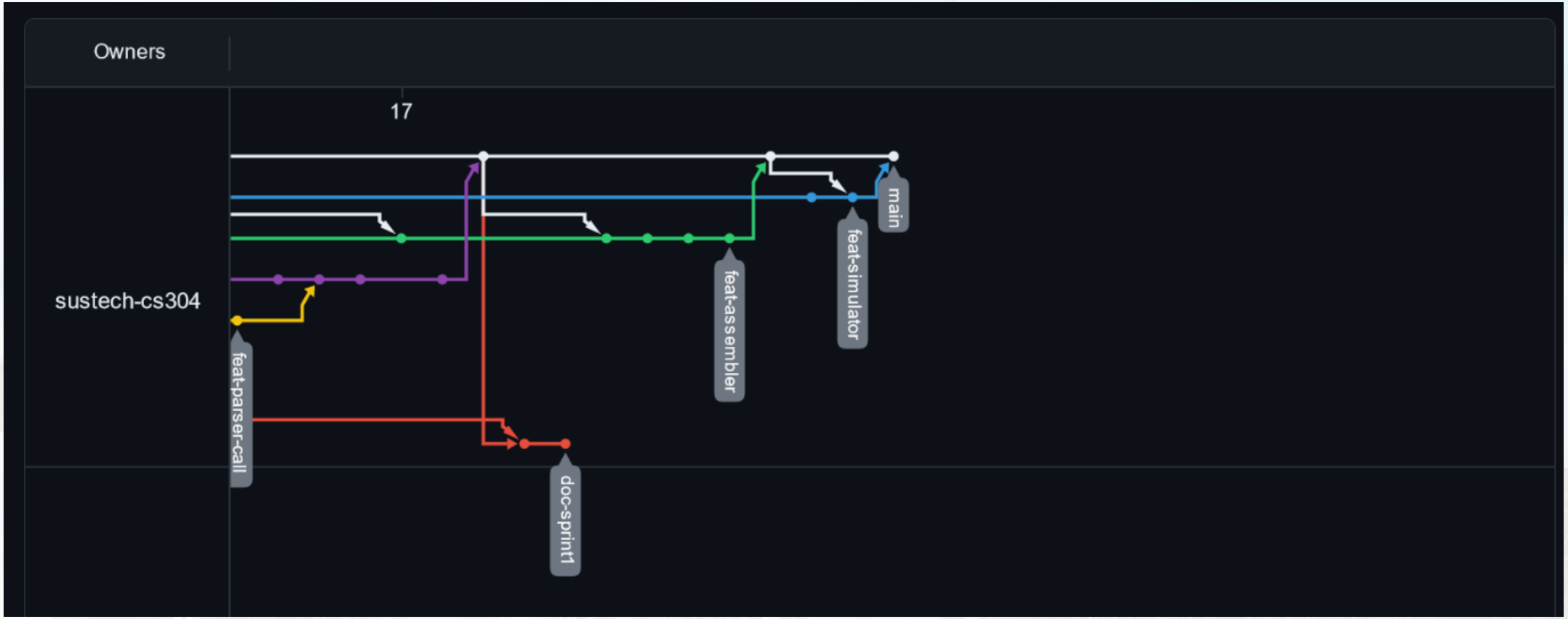
Network



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感谢您的观看

THANKS FOR WATCHING