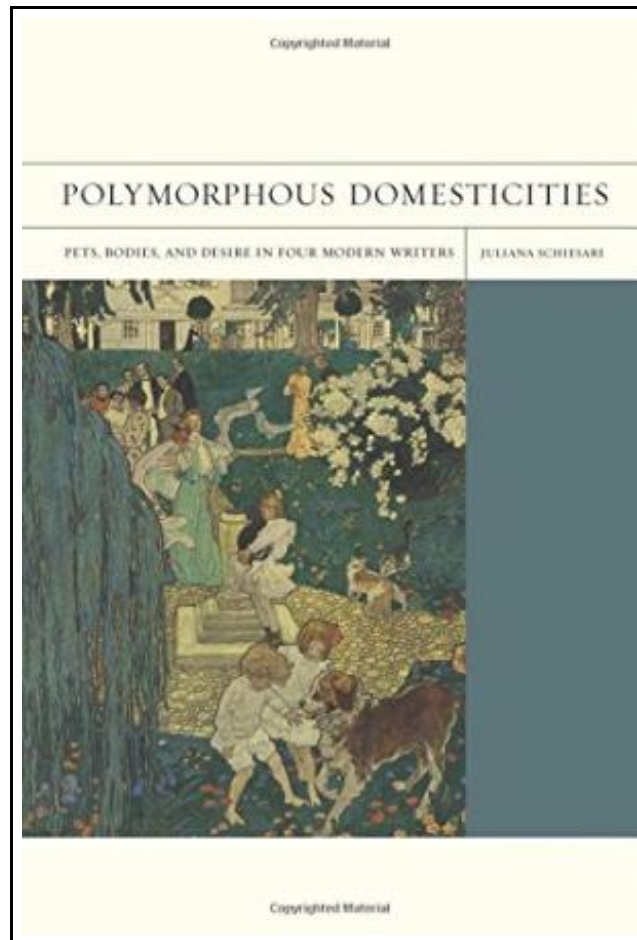# Latchup

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LATCHUP

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Wiley. Hardcover. Condition: New. 474 pages. Dimensions: 9.8in. x 6.8in. x 1.3in.Interest in latchup is being renewed with the evolution of complimentary metal-oxide semiconductor (CMOS) technology, metal-oxide-semiconductor field-effect transistor (MOSFET) scaling, and high-level system-on-chip (SOC) integration. Clear methodologies that grant protection from latchup, with insight into the physics, technology and circuit issues involved, are in increasing demand. This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena, from basic over-voltage and over-current conditions, single event latchup (SEL) and cable discharge events (CDE), to latchup domino phenomena. It contains chapters focusing on bipolar physics, latchup theory, latchup and guard ring characterization structures, characterization testing, product level test systems, product level testing and experimental results. Discussions on state-of-the-art semiconductor processes, design layout, and circuit level and system level latchup solutions are also included, as well as: latchup semiconductor process solutions for both CMOS to BiCMOS, such as shallow trench, deep trench, retrograde wells, connecting implants, sub-collectors, heavily-doped buried layers, and buried grids from single- to triple-well CMOS;practical latchup design methods, automated and bench-level latchup testing methods and techniques, latchup theory of logarithm resistance space, generalized alpha (a) space, beta (b) space, new latchup design methods connecting the theoretical to the practical analysis, and;examples of latchup computer aided design (CAD) methodologies, from design rule checking (DRC) and logical-to-physical design, to new latchup CAD methodologies that address latchup for internal and external latchup on a local as well as global design level. Latchup acts as a companion text to the authors series of books on ESD (electrostatic discharge) protection, serving as an invaluable reference for the professional semiconductor chip and system-level ESD engineer. Semiconductor device, process and circuit designers, and quality, reliability and failure analysis engineers will find it informative on the issues that confront modern CMOS technology....

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