i.MX8M PWR

U1M

NVCC_SNVS_3V3 → W18 NVCC_SNVS
VDD_SNVS_0V9 → R18 VDD_SNVS
C13 1uF 6.3V, C5 100nF 10V

VDD_SOC_0V9 → R8 R9 R10 R11 R12 R13 R14 R15 R16 T8 K12 L12 M12 P16 P12 P15 L13 M13 N13 P13 T17 VDD_SOC1–VDD_SOC21
C15 22uF 10V, C6 C16 C17 1uF 6.3V, C7 C18 C19 1uF 6.3V
C23 C24 22uF 10V, C25 C26 C8 C27 1uF 6.3V
L1 Murata BLM03AX241SN1D
C28 1uF 6.3V

V18 VDDA_0P9

VDD_ARM_0V9 → G15 H15 J15 K15 L15 M15 G16 H16 J16 K16 L16 M16 G14 H14 VDD_ARM1–VDD_ARM14
C32 C33 C34 22uF 10V, C35 C36 C37 C38 C39 1uF 6.3V
C49 C43 C44 C45 1uF 6.3V

VDD_VPU_0V9 → N8 N9 N10 P9 P10 VDD_VPU1–VDD_VPU5
C54 C55 C56 22uF 10V, C57 C47 C48 C58 1uF 6.3V

VDD_GPU_0V9 → J9 K9 L9 M9 J10 K10 L10 M10 VDD_GPU1–VDD_GPU8
C61 C62 C63 22uF 10V, C64 C65 C66 C67 C68 C69 C71 1uF 6.3V

VDD_DRAM_0V9 → V9 V15 V14 V13 V12 V11 V10 U11 U14 U12 U10 U13 Y6 Y8 Y20 Y18 Y16 Y10 VDD_DRAM1–VDD_DRAM18
C76 C77 22uF 10V, C78 C79 C80 C81 1uF 6.3V, C82 10nF 6.3V, C83 10nF 6.3V, C84 C85 4.7nF 10V
C92 C93 C94 C95 C96 C97 C98 C99 4.7nF 10V, C100 1uF 6.3V, C101 4.7nF 10V

VDDA_1V8 → AA11 K14 U17 W17 N11 T15 U23 T16 W23 W24 R17
VDDA_DRAM VDDA_1P8_FPLL_ARM VDDA_1P8_FPLL VDDA_1P8_SPLL VDDA_1P8_SPLL_VIDEO2 VDDA_1P8_SPLL_DRAM VDDA_1P8_LVDS VDDA_1P8_TSENSOR VDDA_1P8_XTAL_27M VDDA_1P8_XTAL_25M EFUSE_VQPS
C102 22uF 10V, C103 C104 C105 C106 C107 C108 100nF 10V

NVCC_DRAM_1V1 → AB23 AA10 AB17 AA15 AB8 AB3 AC14 AC17 AC20 AC3 AC23 AC8 AC6 AD21 AD18 AD5 Y14 Y12 NVCC_DRAM1–NVCC_DRAM18
C109 C110 22uF 10V, C111 C112 C113 C114 C115 C116 C117 C118 1uF 6.3V
C119 22uF 10V, C120 C121 C122 C123 C124 C125 C126 C127 C128 C129 1uF 6.3V
C1132 C1133 C1134 1uF 6.3V

MIMX8MD6DVAJZAB

NVCC_JTAG W4
NVCC_NAND1 L18
NVCC_NAND2 M18
NVCC_SAI1_1 L3
NVCC_SAI1_2 K3
NVCC_SAI2 J7
NVCC_SAI3 E3
NVCC_SAI5 M3
NVCC_GPIO1 R5
NVCC_GPIO2 R6
NVCC_I2C H7
NVCC_UART D8
NVCC_ECSPI F5
NVCC_SD1_1 M23
NVCC_SD1_2 L23
NVCC_SD2 N23
NVCC_ENET T18

C1 C9 C2 C3 C10 C11 C4 C12 C14 100nF 10V → NVCC_3V3
C20 C21 C22 100nF 10V → NVCC_SD2
NVCC_SD1_1V8
NVCC_ENET_2V5

USB1_VDD33 G12
USB2_VDD33 G11
USB1_VPH F12
USB2_VPH F11
USB1_VPTX C12
USB2_VPTX C11
USB1_VP D12
USB2_VP D11
USB1_DVDD E12
USB2_DVDD E11

C29 C30 100nF 10V, C31 2.2uF 10V → VDD_PHY_3V3
C40 C41 100nF 10V, C42 2.2uF 10V → VDD_PHY_0V9

PCIE_VPH1 H23
PCIE_VPH2 J23
PCIE_VPTX1 G23
PCIE_VPTX2 F23
PCIE_VP1 G22
PCIE_VP2 F22

C52 C53 100nF 10V, C46 2.2uF 10V → VDD_PHY_0V9
C50 100nF 10V, C51 2.2uF 10V → VDD_PHY_3V3

HDMI_AVDDIO P2
HDMI_AVDDCLK V3
HDMI_AVDDCORE2 U3
HDMI_AVDDCORE1 U4

C70 C72 100nF 10V, C73 2.2uF 10V → VDD_PHY_0V9
C59 100nF 10V, C60 2.2uF 10V → VDD_PHY_1V8

MIPI_VDDHA1 C18
MIPI_VDDHA2 D17
MIPI_VDDHA3 D18
MIPI_VDDA1 E17
MIPI_VDDA2 E18
MIPI_VDDA3 F18
MIPI_VDDA4 F17
MIPI_VDD1 E15
MIPI_VDD2 F15
MIPI_VDDPLL F19

C74 100nF 10V, C75 2.2uF 10V → VDD_PHY_1V8
C90 100nF 10V, C91 100nF 10V
L2 BLM18AG121SN1D <Rating>
C86 C87 C88 100nF 10V, C89 2.2uF 10V → VDD_PHY_0V9

VDD_3V3 → NVCC_3V3, NVCC_JTAG_3V3, NVCC_NAND_3V3, NVCC_SAI1_3V3, NVCC_I2C_3V3, NVCC_SD2
R1 0 5% DNP

U1N

V23 W22 B25 C8 C10 C13 C15 A24 C24 D10 D13 D15 D23 A2 E4 E10 E13 E14 E20 E16 E19 E21 E22 E23 F10 F13 F14 F20 F16 G9 G10 G13 G17 G18 G24 H8 H9 H10 H11 H12 H13 H17 H18 J3 B1 J8 J11 J12 J13 J14 J17 J18 J19 K8 K11 N18 K17 K18 K23 L8 L11 L14 L17 M8 M11 M14 M17 N3 N17 N14 P6 P8 P11 VSS1–VSS71
VSSA_XTAL_25M VSSA_XTAL_27M

K13 U16 N12 V17 T14 AE2 AD25 AD16 AD13 AD11 AD9 AD7 AD1 AC22 AC19 AC4 AB24 AB18 AB11 AB9 AB2 AA21 AA16 AA5 Y24 Y23 Y22 Y21 Y19 Y17 Y15 Y13 Y11 Y9 Y7 Y5 Y4 Y3 Y2 W25 W16 W15 W14 W13 W12 W11 W10 W8 W7 W1 AE24 V16 V8 V4 U18 U15 U9 U8 AE21 AE5 T13 T12 T11 T10 T9 T4 T3 W9 R7 P23 P18 P17 N15 N16 P14 VSS72–VSS141
VSSA_FPLL_ARM VSSA_FPLL VSSA_SPLL_VIDEO2 VSSA_SPLL VSSA_SPLL_DRAM

MIMX8MD6DVAJZAB

Title	Rototype - RLB		
Size C	Document Number i.MX8M - 01 - MC - C-04 CPU PWR		Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47		

LPDDR4

U1A

i.MX8M - DDR
(LPDDR4/DDR4/DDR3)

DRAM_CA0_A	AD17	CA0_A / A12 / A12(BC#)	DRAM_DQ00	AE23	DRAM_DATA0_A
DRAM_CA1_A	AE16	CA1_A / A11 / A11	DRAM_DQ01	AD24	DRAM_DATA1_A
DRAM_CA2_A	AD20	CA2_A / A7 / A7	DRAM_DQ02	AE22	DRAM_DATA2_A
DRAM_CA3_A	AE20	CA3_A / A8 / A8	DRAM_DQ03	AD22	DRAM_DATA3_A
DRAM_CA4_A	AD19	CA4_A / A6 / A6	DRAM_DQ04	AA24	DRAM_DATA4_A
DRAM_CA5_A	AE19	CA5_A / A5 / A5	DRAM_DQ05	Y25	DRAM_DATA5_A
			DRAM_DQ06	AA25	DRAM_DATA6_A
DRAM_nCS0_A	AE18	CS0_A / CS0_n / CS0#	DRAM_DQ07	AB25	DRAM_DATA7_A
DRAM_nCS1_A	AC18	CS1_A / C0 / --	DRAM_DQ08	AB22	DRAM_DATA8_A
			DRAM_DQ09	AA22	DRAM_DATA9_A
DRAM_CKE0_A	AC16	CKE0_A / CKE0 / CKE0	DRAM_DQ10	AA23	DRAM_DATA10_A
DRAM_CKE1_A	AE17	CKE1_A / CKE1 / CKE1	DRAM_DQ11	AA20	DRAM_DATA11_A
			DRAM_DQ12	AA18	DRAM_DATA12_A
DRAM_CK_T_A	AD14	CK_t_A / BG0 / BA2	DRAM_DQ13	AB19	DRAM_DATA13_A
DRAM_CK_C_A	AE14	CK_c_A / BG1 / A14	DRAM_DQ14	AA19	DRAM_DATA14_A
			DRAM_DQ15	AA17	DRAM_DATA15_A
	AB16	-- / A4 / A4	DRAM_DM0	AD23	DRAM_DMI0_A
			DRAM_DM1	AB20	DRAM_DMI1_A
DRAM_CA0_B	AE8	CA0_B / C2 / --	DRAM_DQS0_P	AC24	DRAM_SDQS0_T_A
DRAM_CA1_B	AE9	CA1_B / CAS_n(A15) / CAS#	DRAM_DQS0_N	AC25	DRAM_SDQS0_C_A
DRAM_CA2_B	AC7	CA2_B / A13 / A13		AB21	DRAM_SDQS1_T_A
DRAM_CA3_B	AE7	CA3_B / BA0 / BA0	DRAM_DQS1_P	AC21	DRAM_SDQS1_C_A
DRAM_CA4_B	AE6	CA4_B / A10(AP) / A10(AP)	DRAM_DQS1_N		
DRAM_CA5_B	AD6	CA5_B / A0 / A0			
DRAM_nCS0_B	AC9	CS0_B / -- / --	DRAM_DQ16	AE3	DRAM_DATA0_B
DRAM_nCS1_B	AD8	CS1_B / -- / --	DRAM_DQ17	AD2	DRAM_DATA1_B
			DRAM_DQ18	AE4	DRAM_DATA2_B
DRAM_CKE0_B	AD10	CKE0_B / CK_t_B / CK_B	DRAM_DQ19	AD4	DRAM_DATA3_B
DRAM_CKE1_B	AE10	CKE1_B / CK_c_B / CK#_B	DRAM_DQ20	AA2	DRAM_DATA4_B
			DRAM_DQ21	Y1	DRAM_DATA5_B
DRAM_CK_T_B	AD12	CK_t_B / A2 / A2	DRAM_DQ22	AA1	DRAM_DATA6_B
DRAM_CK_C_B	AE12	CK_c_B / A1 / A1	DRAM_DQ23	AB1	DRAM_DATA7_B
			DRAM_DQ24	AB4	DRAM_DATA8_B
	AC10	-- / WE_n(A14) / WE#	DRAM_DQ25	AA4	DRAM_DATA9_B
			DRAM_DQ26	AA3	DRAM_DATA10_B
			DRAM_DQ27	AA6	DRAM_DATA11_B
			DRAM_DQ28	AA8	DRAM_DATA12_B
			DRAM_DQ29	AB7	DRAM_DATA13_B
			DRAM_DQ30	AA7	DRAM_DATA14_B
			DRAM_DQ31	AA9	DRAM_DATA15_B
	AD15	-- / CK_c_A / CK#_A			
	AE15	-- / CK_t_A / CK_A			
	AC12	-- / ODT0 / ODT0		AD3	DRAM_DMI0_B
	AE11	-- / ODT1 / ODT1	DRAM_DM2	AB6	DRAM_DMI1_B
	AC15	-- / A3 / A3	DRAM_DM3		
	AB15	-- / A9 / A9			
	AE13	-- / ACT_n / A15	DRAM_DQS2_P	AC2	DRAM_SDQS0_T_B
	AC11	-- / CS1_n / CS1#	DRAM_DQS2_N	AC1	DRAM_SDQS0_C_B
	AB10	-- / RAS_n(A16) / RAS#			
	AB12	-- / BA1 / BA1		AB5	DRAM_SDQS1_T_B
	AA12	-- / PARITY / --	DRAM_DQS3_P	AC5	DRAM_SDQS1_C_B
			DRAM_DQS3_N		
DRAM_nRESET	AB13	RESET_n / RESET_n / RESET#			
	AA14	VREF / VREF / VREF			
	AA13	ZQ / ZQ / ZQ			
	AB14	MTEST / MTEST / MTEST			
	AC13	MTEST1 / MTEST1(ALERT_n) / MTEST1			

MIMX8MD6DVAJZAB

GND — R6 1 — 10K 5% — DRAM_nRESET

DRAM_VREF — R8 1 — 240 1% — ZQ

C130 100nF 50V

TP1 TP2

GND GND

U2A

DRAM_nCS0_A	H4	CS0_A	DMI0_A	C3	DRAM_DMI0_A
DRAM_nCS1_A	H3	NC_H3			
	K5	NC_K5	DQ0_A	B2	DRAM_DATA0_A
			DQ1_A	C2	DRAM_DATA1_A
DRAM_CKE0_A	J4	CKE0_A	DQ2_A	E2	DRAM_DATA2_A
DRAM_CKE1_A	J5	NC_J5	DQ3_A	F2	DRAM_DATA3_A
	K8	NC_K8	DQ4_A	F4	DRAM_DATA4_A
			DQ5_A	E4	DRAM_DATA5_A
DRAM_CK_T_A	J8	CK_t_A	DQ6_A	C4	DRAM_DATA6_A
DRAM_CK_C_A	J9	CK_c_A	DQ7_A	B4	DRAM_DATA7_A
			DQS0_t_A	D3	DRAM_SDQS0_T_A
DRAM_CA0_A	H2	CA0_A	DQS0_c_A	E3	DRAM_SDQS0_C_A
DRAM_CA1_A	J2	CA1_A			
DRAM_CA2_A	H9	CA2_A	DMI1_A	C10	DRAM_DMI1_A
DRAM_CA3_A	H10	CA3_A			
DRAM_CA4_A	H11	CA4_A	DQ8_A	B11	DRAM_DATA8_A
DRAM_CA5_A	J11	CA5_A	DQ9_A	C11	DRAM_DATA9_A
			DQ10_A	E11	DRAM_DATA10_A
ODT_CA_A	G2	ODT_CA_A	DQ11_A	F11	DRAM_DATA11_A
			DQ12_A	F9	DRAM_DATA12_A
DRAM_nCS0_B	R4	CS0_B	DQ13_A	E9	DRAM_DATA13_A
DRAM_nCS1_B	R3	NC_R3	DQ14_A	C9	DRAM_DATA14_A
	N5	NC_N5	DQ15_A	B9	DRAM_DATA15_A
DRAM_CKE0_B	P4	CKE0_B	DQS1_t_A	D10	DRAM_SDQS1_T_A
DRAM_CKE1_B	P5	NC_P5	DQS1_c_A	E10	DRAM_SDQS1_C_A
	N8	NC_N8			
DRAM_CK_T_B	P8	CK_t_B	DMI0_B	Y3	DRAM_DMI0_B
DRAM_CK_C_B	P9	CK_c_B			
			DQ0_B	AA2	DRAM_DATA0_B
DRAM_CA0_B	R2	CA0_B	DQ1_B	Y2	DRAM_DATA1_B
DRAM_CA1_B	P2	CA1_B	DQ2_B	V2	DRAM_DATA2_B
DRAM_CA2_B	R9	CA2_B	DQ3_B	U2	DRAM_DATA3_B
DRAM_CA3_B	R10	CA3_B	DQ4_B	U4	DRAM_DATA4_B
DRAM_CA4_B	R11	CA4_B	DQ5_B	V4	DRAM_DATA5_B
DRAM_CA5_B	P11	CA5_B	DQ6_B	Y4	DRAM_DATA6_B
			DQ7_B	AA4	DRAM_DATA7_B
ODT_CA_B	T2	ODT_CA_B	DQS0_t_B	W3	DRAM_SDQS0_T_B
			DQS0_c_B	V3	DRAM_SDQS0_C_B
DRAM_nRESET	T11	RESET_N	DMI1_B	Y10	DRAM_DMI1_B
DRAM_ZQ0	A5	ZQ0			
DRAM_ZQ1	A8	NC_A8	DQ8_B	AA11	DRAM_DATA8_B
	G11	NC_G11	DQ9_B	Y11	DRAM_DATA9_B
			DQ10_B	V11	DRAM_DATA10_B
			DQ11_B	U11	DRAM_DATA11_B
			DQ12_B	U9	DRAM_DATA12_B
			DQ13_B	V9	DRAM_DATA13_B
			DQ14_B	Y9	DRAM_DATA14_B
			DQ15_B	AA9	DRAM_DATA15_B
			DQS1_t_B	W10	DRAM_SDQS1_T_B
			DQS1_c_B	V10	DRAM_SDQS1_C_B
			DNU_AB12	AB12	
			DNU_AB11	AB11	
			DNU_AB2	AB2	
			DNU_AB1	AB1	
			DNU_AA12	AA12	
			DNU_AA1	AA1	
			DNU_B12	B12	
			DNU_B1	B1	
			DNU_A12	A12	
			DNU_A11	A11	
			DNU_A2	A2	
			DNU_A1	A1	

MT53D512M32D2DS-053 WT:D

NVCC_DRAM_1V1 — R3 150 DNP — R2 150 DNP — GND

NVCC_DRAM_1V1 — R721 10K 5% — ODT_CA_A

R721 e R722 come su demoboard
valutare se introdurre 0R

NVCC_DRAM_1V1 — R4 150 DNP — R5 150 DNP — GND

NVCC_DRAM_1V1 — R722 10K 5% — ODT_CA_B

NVCC_DRAM_1V1 — R7 240 — R9 240 DNP — DRAM_ZQ0 — DRAM_ZQ1

NVCC_DRAM_1V1

DRAM VREF

R10 1K5 0.1% DNP — C131 100nF 50V DNP — C132 4.7uF 6.3V — DRAM_VREF

R13 1K5 0.1% DNP — C137 100nF 50V DNP — R14 0 — VREFDDR

GND GND GND

DRAM_CK_T_A — R11 150 1% — DRAM_CK_C_A

DRAM_CK_T_B — R12 150 1% — DRAM_CK_C_B

DCDC_3V3 — C142 1uF 25V — C143 100nF 50V — R17 100K — PG_SEQ0 — R181 20

U3 LDCL015MR: IN, EN, GND, OUT, ADJ

R15 698K — R16 562K — Vfb=0.8V

C144 1uF 25V — C145 100nF 50V — VDD_SNVS_0V9

Power supply voltage ramp:

RESET_n is held LOW.
VDD1 >= VDD2
VDD2 >= VDDQ

VDD_1V8

U2B

F1	VDD1_F1		VSS_A3	A3	
F12	VDD1_F12		VSS_A10	A10	
G4	VDD1_G4		VSS_C1	C1	
G9	VDD1_G9		VSS_C5	C5	
T4	VDD1_T4		VSS_C8	C8	
T9	VDD1_T9		VSS_C12	C12	
U1	VDD1_U1		VSS_D2	D2	
U12	VDD1_U12		VSS_D4	D4	
			VSS_D9	D9	
			VSS_D11	D11	
A4	VDD2_A4		VSS_E1	E1	
A9	VDD2_A9		VSS_E5	E5	
F5	VDD2_F5		VSS_E8	E8	
F8	VDD2_F8		VSS_E12	E12	
H1	VDD2_H1		VSS_G1	G1	
H5	VDD2_H5		VSS_G3	G3	
H8	VDD2_H8		VSS_G5	G5	
H12	VDD2_H12		VSS_G8	G8	
K1	VDD2_K1		VSS_G10	G10	
K3	VDD2_K3		VSS_G12	G12	
K10	VDD2_K10		VSS_J1	J1	
K12	VDD2_K12		VSS_J3	J3	
N1	VDD2_N1		VSS_J10	J10	
N3	VDD2_N3		VSS_J12	J12	
N10	VDD2_N10		VSS_K2	K2	
N12	VDD2_N12		VSS_K4	K4	
R1	VDD2_R1		VSS_K9	K9	
R5	VDD2_R5		VSS_K11	K11	
R8	VDD2_R8		VSS_N2	N2	
R12	VDD2_R12		VSS_N4	N4	
U5	VDD2_U5		VSS_N9	N9	
U8	VDD2_U8		VSS_N11	N11	
AB4	VDD2_AB4		VSS_P1	P1	
AB9	VDD2_AB9		VSS_P3	P3	
			VSS_P10	P10	
			VSS_P12	P12	
			VSS_T1	T1	
			VSS_T3	T3	
1.06-1.17V B3	VDDQ_B3		VSS_T5	T5	
B5	VDDQ_B5		VSS_T8	T8	
B8	VDDQ_B8		VSS_T10	T10	
B10	VDDQ_B10		VSS_T12	T12	
D1	VDDQ_D1		VSS_V1	V1	
D5	VDDQ_D5		VSS_V5	V5	
D8	VDDQ_D8		VSS_V8	V8	
D12	VDDQ_D12		VSS_V12	V12	
F3	VDDQ_F3		VSS_W2	W2	
F10	VDDQ_F10		VSS_W4	W4	
U3	VDDQ_U3		VSS_W9	W9	
U10	VDDQ_U10		VSS_W11	W11	
W1	VDDQ_W1		VSS_Y1	Y1	
W5	VDDQ_W5		VSS_Y5	Y5	
W8	VDDQ_W8		VSS_Y8	Y8	
W12	VDDQ_W12		VSS_Y12	Y12	
AA3	VDDQ_AA3		VSS_AB3	AB3	
AA5	VDDQ_AA5		VSS_AB5	AB5	
AA8	VDDQ_AA8		VSS_AB8	AB8	
AA10	VDDQ_AA10		VSS_AB10	AB10	

MT53D512M32D2DS-053 WT:D

C933 22uF 10V — C934 4.7uF 6.3V — C935 4.7uF 6.3V — C936 4.7uF 6.3V — C937 4.7uF 6.3V — GND

NVCC_DRAM_1V1 — C938 22uF 10V — C939 4.7uF 6.3V — C940 4.7uF 6.3V — C941 4.7uF 6.3V — C942 4.7uF 6.3V — GND

NVCC_DRAM_1V1 — C943 22uF 10V — C944 4.7uF 6.3V — C945 4.7uF 6.3V — C946 4.7uF 6.3V — C947 4.7uF 6.3V — GND

GND

Title	Rototype - RLB	
Size C	Document Number i.MX8M - 01 - MC - C-05 LPDDR4	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

MIMX8MD6DVAJZAB

NAND/QSPI

U1H — i.MX8M - NAND

NAND_CE0_B	H19	NAND_nCE0	QSPIA_nSS0 9
NAND_CE1_B	G21	NAND_nCE1	QSPIA_nSS1 16,17
NAND_CE2_B	F21	NAND_nCE2	TCPC_nINT
NAND_CE3_B	H20	NAND_nCE3	QSPIA_nSS3 16,17
NAND_ALE	G19	NAND_ALE	QSPIA_SCLK 9
NAND_CLE	H21	NAND_CLE	R19 0 5% DNP — POD_nRST 11
NAND_RE_B	K19	NAND_nRE	USB1_SS_SEL 12
NAND_WE_B	K22	NAND_nWE	
NAND_WP_B	K21	NAND_nWP	TP14
NAND_READY_B	K20	NAND_nREADY	TP15, TP17
NAND_DQS	M20	NAND_DQS	TP18
NAND_DATA00	G20	NAND_DATA0	QSPIA_DATA0 9
NAND_DATA01	J20	NAND_DATA1	QSPIA_DATA1 9
NAND_DATA02	H22	NAND_DATA2	QSPIA_DATA2 9
NAND_DATA03	J21	NAND_DATA3	QSPIA_DATA3 9
NAND_DATA04	L20	NAND_DATA4	
NAND_DATA05	J22	NAND_DATA5	TP23
NAND_DATA06	L19	NAND_DATA6	TP24
NAND_DATA07	M19	NAND_DATA7	TP26, TP27

NVCC_NAND

MIMX8MD6DVAJZAB

U1J — i.MX8M - eNET

ENET_MDC	N20	ENET_MDC	ENET_MDC 15
ENET_MDIO	N19	ENET_MDIO	ENET_MDIO 15
ENET_TX_CTL	P19	ENET_TX_CTL	ENET_TX_CTL 15
ENET_TXC	T19	ENET_TXC	ENET_TXC 15
ENET_TD0	R20	ENET_TD0	ENET_TD0 15
ENET_TD1	R21	ENET_TD1	ENET_TD1 15
ENET_TD2	R19	ENET_TD2	ENET_TD2 15
ENET_TD3	P20	ENET_TD3	ENET_TD3 15
ENET_RX_CTL	T21	ENET_RX_CTL	ENET_RX_CTL 15
ENET_RXC	T20	ENET_RXC	ENET_RXC 15
ENET_RD0	U19	ENET_RD0	ENET_RD0 15
ENET_RD1	U21	ENET_RD1	ENET_RD1 15
ENET_RD2	U20	ENET_RD2	ENET_RD2 15
ENET_RD3	V19	ENET_RD3	ENET_RD3 15

NVCC_ENET

MIMX8MD6DVAJZAB

U1I — i.MX8M - SD

9 SD1_CLK	SD1_CLK	L25	SD1_CLK
9 SD1_CMD	SD1_CMD	L24	SD1_CMD
9 SD1_DATA0	SD1_DATA0	M25	SD1_DATA0
9 SD1_DATA1	SD1_DATA1	M24	SD1_DATA1
9 SD1_DATA2	SD1_DATA2	N25	SD1_DATA2
9 SD1_DATA3	SD1_DATA3	P25	SD1_DATA3
9 SD1_DATA4	SD1_DATA4	N24	SD1_DATA4
9 SD1_DATA5	SD1_DATA5	P24	SD1_DATA5
9 SD1_DATA6	SD1_DATA6	R25	SD1_DATA6
9 SD1_DATA7	SD1_DATA7	T25	SD1_DATA7
9,18 SD1_nRST	SD1_nRST	R24	SD1_RESET_B
9 SD1_STROBE	SD1_STROBE	T24	SD1_STROBE

NVCC_SD1

SD2_CLK	L22	SD2_CLK	SD2_CLK 17,19
SD2_CMD	M22	SD2_CMD	SD2_CMD 17,19
SD2_DATA0	N22	SD2_DATA0	SD2_DATA0 17,19
SD2_DATA1	N21	SD2_DATA1	SD2_DATA1 17,19
SD2_DATA2	P22	SD2_DATA2	SD2_DATA2 17,19
SD2_DATA3	P21	SD2_DATA3	SD2_DATA3 17,19
SD2_WP	M21	SD2_WP	
SD2_CD_B	L21	SD2_nCD	SD2_nCD 19
SD2_RESET_B	R22	SD2_nRST	SD2_nRST 17,19

NVCC_SD2

R26 4K7 2 1 1%

MIMX8MD6DVAJZAB

U1G — i.MX8M - SAI

-Internal pullup resistors 27 kOhm;
-Internal pulldown resistor of 90k0hm is always enabled

TP3	SAI5_MCLK	K4	SAI5_MCLK
TP4	SAI5_RXFS	N4	SAI5_RXFS
TP5	SAI5_RXC	L5	SAI5_RXC
TP10	SAI5_RXD0	M5	SAI5_RXD0
TP11	SAI5_RXD1	L4	SAI5_RXD1
TP12	SAI5_RXD2	M4	SAI5_RXD2
TP13	SAI5_RXD3	K5	SAI5_RXD3
TP16	SAI3_MCLK	D3	SAI3_MCLK
	SAI3_TXFS	G3	SAI3_TXFS
	SAI3_TXC	C4	SAI3_TXC
	SAI3_TXD	C3	SAI3_TXD
TP21	SAI3_RXFS	G4	SAI3_RXFS
TP22	SAI3_RXC	F4	SAI3_RXC
	SAI3_RXD	F3	SAI3_RXD
TP25	SPDIF_TX	F6	SPDIF_TX
	SPDIF_RX	G6	SPDIF_RX
	SPDIF_EXT_CLK	E6	SPDIF_EXT_CLK

NVCC_SAI5 / NVCC_SAI3

R20 2 4K7 1%; R21 2 4K7 1%

SAI1_MCLK	A3	SAI1_MCLK	TP6
SAI1_TXFS	H1	SAI1_TXFS	TP7
SAI1_TXC	E1	SAI1_TXC	TP8
SAI1_TXD0	F2	SAI1_TXD0	SAI1_TXD0 11,21
SAI1_TXD1	E2	SAI1_TXD1	SAI1_TXD1 11,21
SAI1_TXD2	B2	SAI1_TXD2	SAI1_TXD2 11,21
SAI1_TXD3	D1	SAI1_TXD3	SAI1_TXD3 11,21
SAI1_TXD4	D2	SAI1_TXD4	SAI1_TXD4 11,21
SAI1_TXD5	C2	SAI1_TXD5	SAI1_TXD5 11,21
SAI1_TXD6	B3	SAI1_TXD6	SAI1_TXD6 11,21
SAI1_TXD7	C1	SAI1_TXD7	SAI1_TXD7 11,21
SAI1_RXFS	L1	SAI1_RXFS	TP19
SAI1_RXC	K1	SAI1_RXC	TP20
SAI1_RXD0	K2	SAI1_RXD0	SAI1_RXD0 11,21
SAI1_RXD1	L2	SAI1_RXD1	SAI1_RXD1 11,21
SAI1_RXD2	H2	SAI1_RXD2	SAI1_RXD2 11,21
SAI1_RXD3	J2	SAI1_RXD3	SAI1_RXD3 11,21
SAI1_RXD4	J1	SAI1_RXD4	SAI1_RXD4 11,21
SAI1_RXD5	F1	SAI1_RXD5	SAI1_RXD5 11,21
SAI1_RXD6	G2	SAI1_RXD6	SAI1_RXD6 11,21
SAI1_RXD7	G1	SAI1_RXD7	SAI1_RXD7 11,21
SAI2_MCLK	H5	SAI2_MCLK	SAI2_MCLK 14
SAI2_TXFS	H4	SAI2_TXFS	SAI2_TXFS 14
SAI2_TXC	J5	SAI2_TXC	SAI2_TXC 14
SAI2_TXD0	G5	SAI2_TXD	SAI2_TXD 14
SAI2_RXFS	J4		
SAI2_RXC	H3		
SAI2_RXD0	H6		

NVCC_SAI1 / NVCC_SAI2

MIMX8MD6DVAJZAB

U1K

20 UART1_RXD	UART1_RXD	C7	UART1_RXD
20 UART1_TXD	UART1_TXD	A7	UART1_TXD
20 UART2_RXD	UART2_RXD	R723 0 5%	B6 UART2_RXD
20 UART2_TXD	UART2_TXD	R724 0 5%	D6 UART2_TXD
TP114	UART3_RXD	A6	UART3_RXD
TP115	UART3_TXD	B7	UART3_TXD
TP116	UART4_RXD	C6	UART4_RXD
TP117	UART4_TXD	D7	UART4_TXD
10,12,18 I2C1_SCL	I2C1_SCL	E7	I2C1_SCL
10,12,18 I2C1_SDA	I2C1_SDA	E8	I2C1_SDA
11,16,17,18 I2C2_SCL	I2C2_SCL	G7	I2C2_SCL
11,16,17,18 I2C2_SDA	I2C2_SDA	F7	I2C2_SDA
TP29	I2C3_SCL	G8	I2C3_SCL
TP30	I2C3_SDA	E9	I2C3_SDA
16 PCIE1_nCLKREQ	PCIE1_nCLKREQ	F8	I2C4_SCL
TP31	PCIE2_nCLKREQ	F9	I2C4_SDA

NVCC_I2C

ECSPI1_SS0	D4	ECSPI1_SS0	ECSPI1_SS0
ECSPI1_MOSI	A4	ECSPI1_MOSI	ECSPI1_MOSI
ECSPI1_MISO	B4	ECSPI1_MISO	ECSPI1_MISO
ECSPI1_SCLK	D5	ECSPI1_SCLK	ECSPI1_SCLK
ECSPI2_SS0	A5	ECSPI2_SS0	ECSPI2_SS0
ECSPI2_MOSI	E5	ECSPI2_MOSI	ECSPI2_MOSI
ECSPI2_MISO	B5	ECSPI2_MISO	ECSPI2_MISO
ECSPI2_SCLK	C5	ECSPI2_SCLK	ECSPI2_SCLK
GPIO1_IO00	T6	MC_Rst_SOC_ok	MC_Rst_SOC_ok
GPIO1_IO01	T7	MC_Boot_FPGA	MC_Boot_FPGA 10,19
GPIO1_IO02	R4	GPIO1_IO02	nWDOG 10
GPIO1_IO03	P4	MC_Boot_SOC	MC_Boot_SOC
GPIO1_IO04	P5	GPIO1_IO04	SD2_VSELECT 19
GPIO1_IO05	P7	MC_Rst_SOC	MC_Rst_SOC
GPIO1_IO06	N5	MC_SOC_Done	MC_SOC_Done
GPIO1_IO07	N6	GPIO1_IO07	PMIC_nINT 10
GPIO1_IO08	N7	GPIO1_IO08	AUD_nMUTE 14
GPIO1_IO09	M6	GPIO1_IO09	ENET_nRST 15
GPIO1_IO10	M7	GPIO1_IO10	ENET_WoL 15
GPIO1_IO11	L6	GPIO1_IO11	ENET_nINT 15
GPIO1_IO12	L7	MC_FPGA_Done	MC_FPGA_Done 10,19
GPIO1_IO13	K6	GPIO1_IO13	PWM_LED 10,19
GPIO1_IO14	K7	GPIO1_IO14	CLKO_25MHz 15
GPIO1_IO15	J6	nQSPIA_access_EN	nQSPIA_access_EN 10,19

NVCC_ECSPI1 / NVCC_ECSPI2 / NVCC_GPIO1

MIMX8MD6DVAJZAB

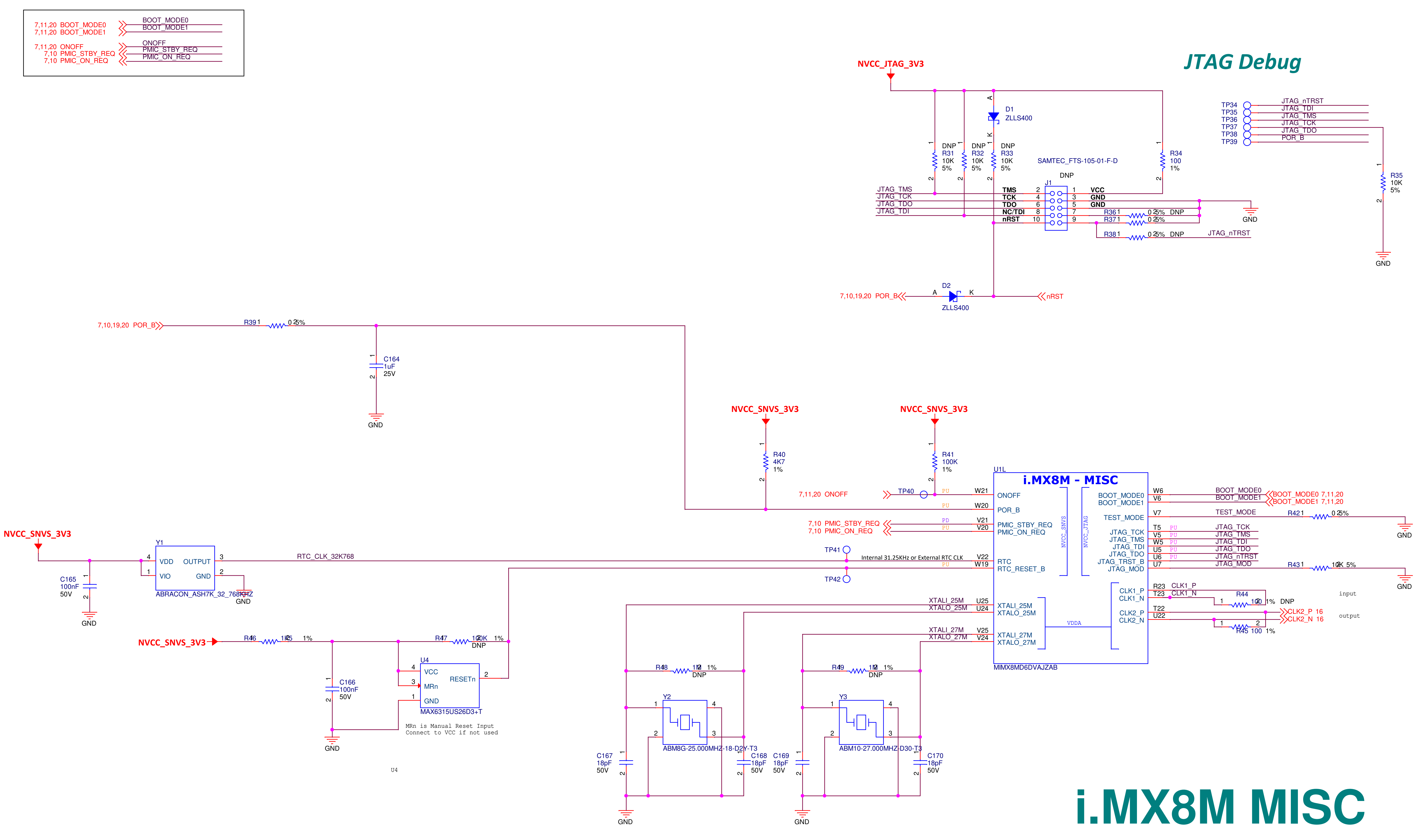
Note: MC_Boot_FPGA shall be set at '1' at the end of Linux boot to boot FPGA

Note: MC_Boot_Soc shall be set at '1' at the end of Linux boot to boot SOC

NVCC_I2C_3V3

R221	2k7 1%	I2C1_SCL	
R231	2k7 1%	I2C1_SDA	
R241	2k7 1%	I2C2_SCL	
R251	2k7 1%	I2C2_SDA	
R271	2k7 1%	I2C3_SCL	
R281	2k7 1%	I2C3_SDA	
R291	2k7 1% DNP	PCIE1_nCLKREQ	
R301	2k7 1% DNP	PCIE2_nCLKREQ	

Title	Rototype - RLB	
Size C	Document Number i.MX8M - 01 - MC - C-06 CPU IO	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	



Title	Rototype - RLB	
Size C	Document Number i.MX8M - 01 - MC - C-07 CPU MISC	Rev 1.0
Date: Monday, January 18, 2021	Sheet 0 of 47	

i.MX8M PHY

VDD_PHY_3V3 → VDD_PHY_3V3
VDD_PHY_1V8 → VDD_PHY_1V8
VDD_PHY_0V9 → VDD_PHY_0V9

USB_RESREF: Attach a 200-¦, 1% 100-ppm/C precision resistor-to-ground on the board.
MIPIDSI_REXT: 15K-¦.
PCIE: 200-¦,¡Ä1% ¡À 100 ppm/¡ãC precision resistor to-ground on the board.
HDMI:a 499¦, (¡Ä1% tolerance) resistor to-ground on the board

U1E
i.MX8M - CSI
MIMX8MD6DVAJZAB

MIPI_CSI1_CLK_N	A22	CSI_P1_CKN	TP43
MIPI_CSI1_CLK_P	B22	CSI_P1_CKP	TP44
MIPI_CSI1_D0_N	A23	CSI_P1_DN0	TP45
MIPI_CSI1_D0_P	B23	CSI_P1_DP0	TP46
MIPI_CSI1_D1_N	C22	CSI_P1_DN1	TP47
MIPI_CSI1_D1_P	D22	CSI_P1_DP1	TP48
MIPI_CSI1_D2_N	B24	CSI_P1_DN2	TP49
MIPI_CSI1_D2_P	C23	CSI_P1_DP2	TP50
MIPI_CSI1_D3_N	C21	CSI_P1_DN3	TP51
MIPI_CSI1_D3_P	D21	CSI_P1_DP3	TP52
MIPI_CSI2_CLK_N	A19	CSI_P2_CKN	TP53
MIPI_CSI2_CLK_P	B19	CSI_P2_CKP	TP54
MIPI_CSI2_D0_N	C20	CSI_P2_DN0	TP55
MIPI_CSI2_D0_P	D20	CSI_P2_DP0	TP56
MIPI_CSI2_D1_N	A20	CSI_P2_DN1	TP57
MIPI_CSI2_D1_P	B20	CSI_P2_DP1	TP58
MIPI_CSI2_D2_N	A21	CSI_P2_DN2	TP59
MIPI_CSI2_D2_P	B21	CSI_P2_DP2	TP60
MIPI_CSI2_D3_N	C19	CSI_P2_DN3	TP61
MIPI_CSI2_D3_P	D19	CSI_P2_DP3	TP62

CSI_P1_VDDHA, CSI_P2_VDDHA

U1F
i.MX8M - HDMI
MIMX8MD6DVAJZAB

HDMI_DDC_SCL	R3	HDMI_DDC_SCL	HDMI_DDC_SCL 13
HDMI_DDC_SDA	P3	HDMI_DDC_SDA	HDMI_DDC_SDA 13
HDMI_HPD	W2	HDMI_HPD	HDMI_HPD 13
HDMI_CEC	W3	HDMI_CEC	HDMI_CEC 13
HDMI_REFCLK_N	R1	HDMI_REFCLKN	AC coupled differential low swing clock (HCSL levels)
HDMI_REFCLK_P	R2	HDMI_REFCLKP	
HDMI_TX_M_LN_0	T2	HDMI_TXN0	HDMI_TXN0 13
HDMI_TX_P_LN_0	T1	HDMI_TXP0	HDMI_TXP0 13
HDMI_TX_M_LN_1	U1	HDMI_TXN1	HDMI_TXN1 13
HDMI_TX_P_LN_1	U2	HDMI_TXP1	HDMI_TXP1 13
HDMI_TX_M_LN_2	N1	HDMI_TXN2	HDMI_TXN2 13
HDMI_TX_P_LN_2	N2	HDMI_TXP2	HDMI_TXP2 13
HDMI_TX_M_LN_3	M2	HDMI_TXN3	HDMI_CLKN 13
HDMI_TX_P_LN_3	M1	HDMI_TXP3	HDMI_CLKP 13
HDMI_AUX_N	V2	HDMI_AUXN	HDMI_AUXN 13
HDMI_AUX_P	V1	HDMI_AUXP	HDMI_AUXP 13
HDMI_REXT	P1	R591 2499 1%	GND

HDMI_AVDD1TO

U1C
i.MX8M - PCIe
MIMX8MD6DVAJZAB

PCIE1_TXN_N	J24	PCIE1_TXN	PCIE1_TXN 16
PCIE1_TXN_P	J25	PCIE1_TXP	PCIE1_TXP 16
PCIE1_RXN_N	H24	PCIE1_RXN	PCIE1_RXN 16
PCIE1_RXN_P	H25	PCIE1_RXP	PCIE1_RXP 16
PCIE1_REF_PAD_CLK_N	K24	PCIE1_REF_CLKN	PCIE1_REF_CLKN 16
PCIE1_REF_PAD_CLK_P	K25	PCIE1_REF_CLKP	PCIE1_REF_CLKP 16
PCIE1_RESREF	G25	R501 200 1%	GND
PCIE2_TXN_N	E24	PCIE2_TXN	
PCIE2_TXN_P	E25	PCIE2_TXP	
PCIE2_RXN_N	D24	PCIE2_RXN	
PCIE2_RXP_P	D25	PCIE2_RXP	
PCIE2_REF_PAD_CLK_N	F24	PCIE2_REF_CLKN	
PCIE2_REF_PAD_CLK_P	F25	PCIE2_REF_CLKP	
PCIE2_RESREF	C25	R511 200 1%	GND

PCIE0_VPH, PCIE1_VPH

R52 49.9 1%, R57 49.9 1%, R53 49.9 1%, R54 49.9 1%, R55 49.9 1%, R56 49.9 1% → GND

U1D
i.MX8M - DSI
MIMX8MD6DVAJZAB

MIPI_DSI_CLK_N	C16	DSI_CKN	TP63
MIPI_DSI_CLK_P	D16	DSI_CKP	TP64
MIPI_DSI_D0_N	A17	DSI_DN0	TP65
MIPI_DSI_D0_P	B17	DSI_DP0	TP66
MIPI_DSI_D1_N	A16	DSI_DN1	TP67
MIPI_DSI_D1_P	B16	DSI_DP1	TP68
MIPI_DSI_D2_N	A18	DSI_DN2	TP69
MIPI_DSI_D2_P	B18	DSI_DP2	TP70
MIPI_DSI_D3_N	A15	DSI_DN3	TP71
MIPI_DSI_D3_P	B15	DSI_DP3	TP72
MIPI_DSI_REXT	C17	R581 2K 5%	GND

DSI_VDDHA

U1B
i.MX8M - USB
MIMX8MD6DVAJZAB

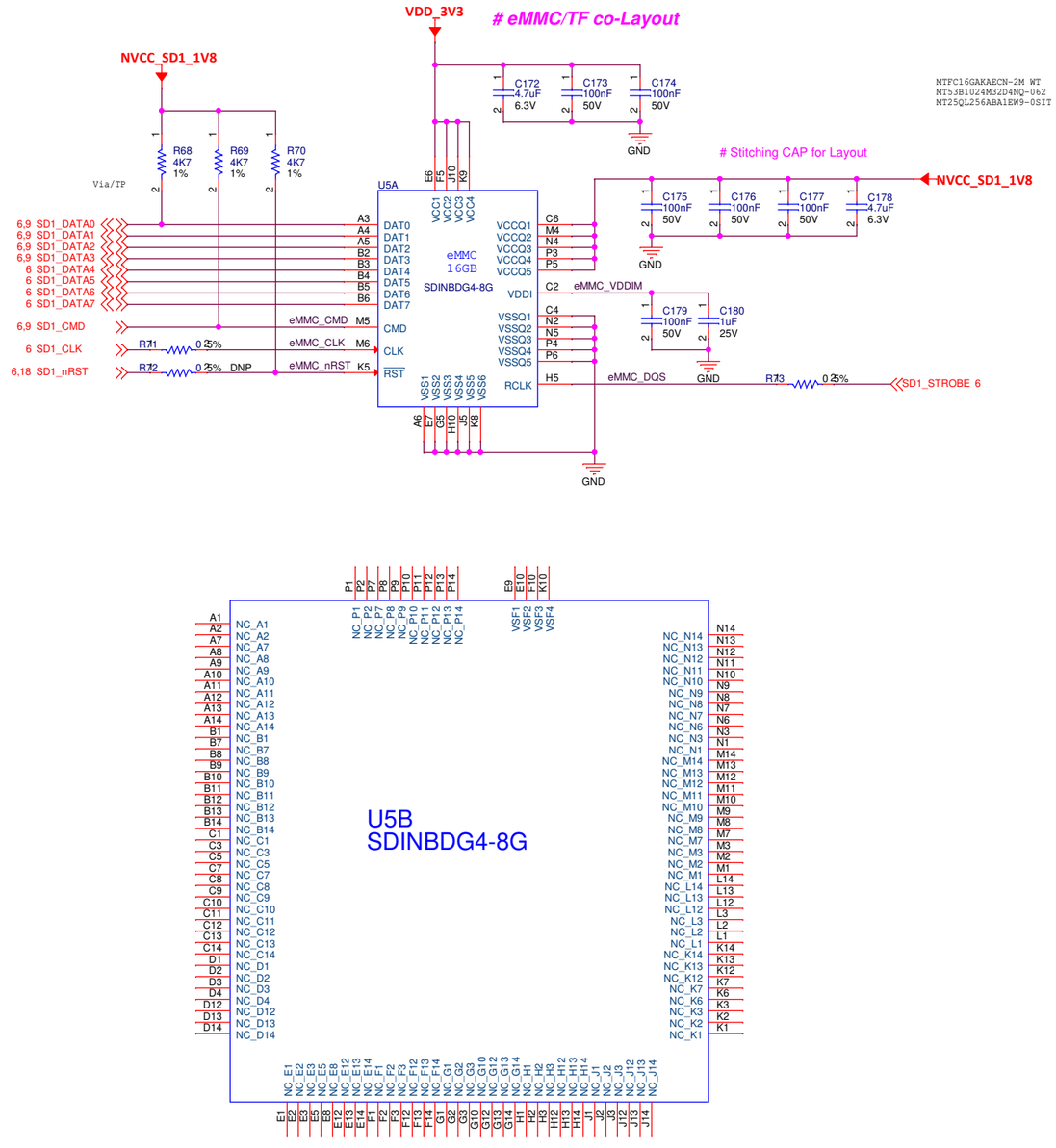
USB1_VBUS	D14	USB1_VBUS	USB1_VBUS 12
USB1_DN	B14	USB1_DN	USB1_DN 12,20
USB1_DP	A14	USB1_DP	USB1_DP 12,20
USB1_ID	C14	USB1_ID	TP73
USB1_TX_P	A13	USB1_TXP	USB1_TXP 12
USB1_TX_N	B13	USB1_TXN	USB1_TXN 12
USB1_RX_P	A12	USB1_RXP	USB1_RXP 12
USB1_RX_N	B12	USB1_RXN	USB1_RXN 12
USB1_RESREF	A11	R601 200 1%	GND
USB2_VBUS	D9	USB2_VBUS	USB2_VBUS 12
USB2_DN	B10	USB2_DN	USB2_DN 12,17
USB2_DP	A10	USB2_DP	USB2_DP 12,17
USB2_ID	C9	USB2_ID	TP74
USB2_TX_P	A9	USB2_TXP	USB2_TXP 12
USB2_TX_N	B9	USB2_TXN	USB2_TXN 12
USB2_RX_P	A8	USB2_RXP	USB2_RXP 12
USB2_RX_N	B8	USB2_RXN	USB2_RXN 12
USB2_RESREF	B11	R631 200 1%	GND

USB_P0_VDD33, USB_P0_VPH, USB_P1_VDD33, USB_P1_VPH

VDD_3V3
R61 100K 1%
R62 100K 1%
C171 100nF 10V → GND
Y4 (HCSL): OE (1), NC (2), GND (3), VCC (6), Q (4), Q̄ (5)
Microchip DSC1104CE2-027.0000T
R64 20 5% → HDMI_REFCLKP
R65 20 5% → HDMI_REFCLKN
R66 49.9 1% DNP, R67 49.9 1% DNP → GND
AC coupled differential low swing clock (HCSL levels)
GND

Title	Rototype - RLB	
Size C	Document Number i.MX8M - 01 - MC - C-08 CPU PHY	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

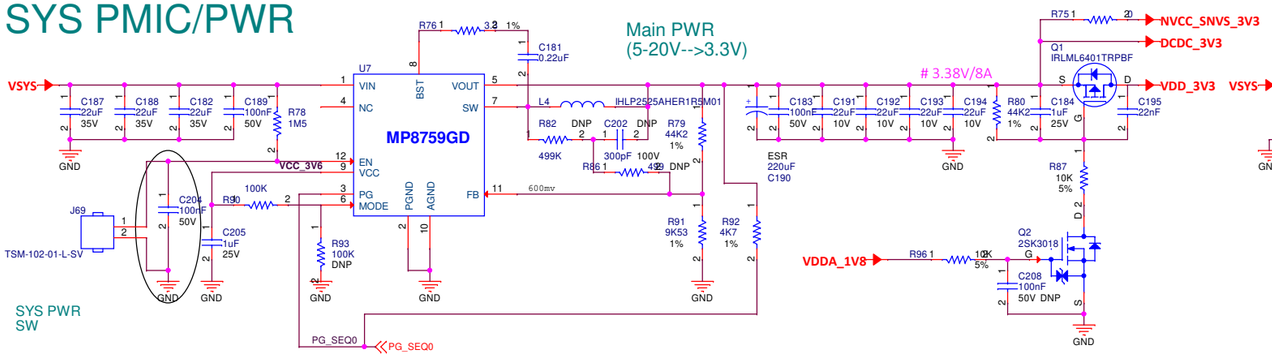
eMMC 5.0 Footprint



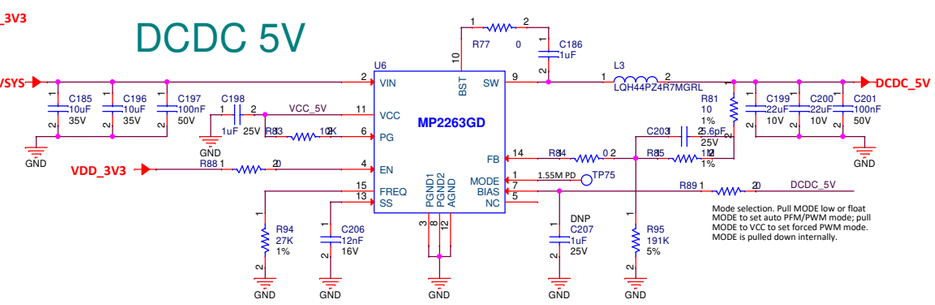
Title	Rototype - RLB		
Size C	Document Number i.MX8M - 01 - MC - C-09eMMC/NAND/TF/QSPI		Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47		

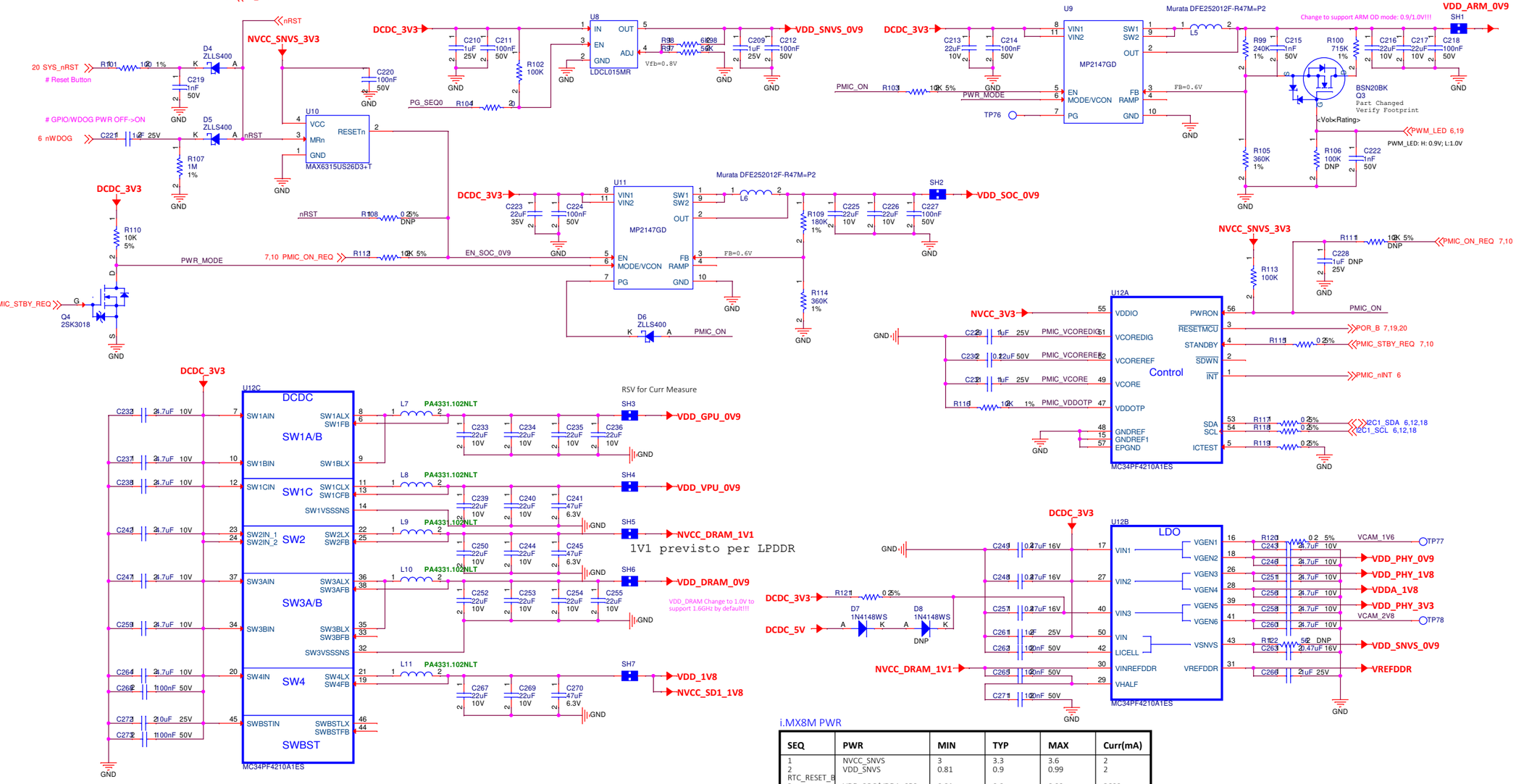
SYS PMIC/PWR

Main PWR (5-20V-->3.3V)



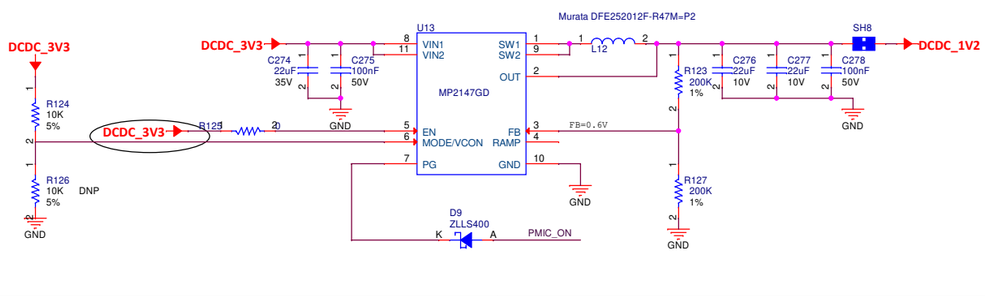
DCDC 5V





i.MX8M PWR

SEQ	PWR	MIN	TYP	MAX	Curr(mA)
1	NVCC_SNVS	3	3.3	3.6	2
2	VDD_SNVS	0.81	0.9	0.99	2
RTC_RESET_B					
3	VDD_SOC/VDDA_0P9	0.81	0.9	0.99	3600
4	VDD_GPU	0.81	0.9/1.0	1.1	2000
4	VDD_VPU	0.81	0.9/1.0	1.1	1000
4	VDD_DRAM	0.81	1.0	1.05	2500
4	VDD_ARM	0.81	0.9/1.0	1.1	4000
5	VDDA_1P8_xxx	1.62	1.8	1.89	250
5	VDDA_DRAM	1.71	1.8	1.89	50
6	NVCC_DRAM		1.1/1.2/1.35		2170
6	NVCC_3V3	3	3.3	3.6	100
6	NVCC_1V8	1.65	1.8	1.95	450
7	3.3V PHY	3.069	3.3	3.63	100
7	1.8V PHY	1.674	1.8	1.98	50
7	0.9V PHY	0.837	0.9	0.99	250
POR_B					



Title	Rototype - RLB
Size A2	Document Number LMX8M - 01 - MC - C-10 PMIC
Rev	1.0
Date:	Monday, January 18, 2021
Sheet	0 of 47

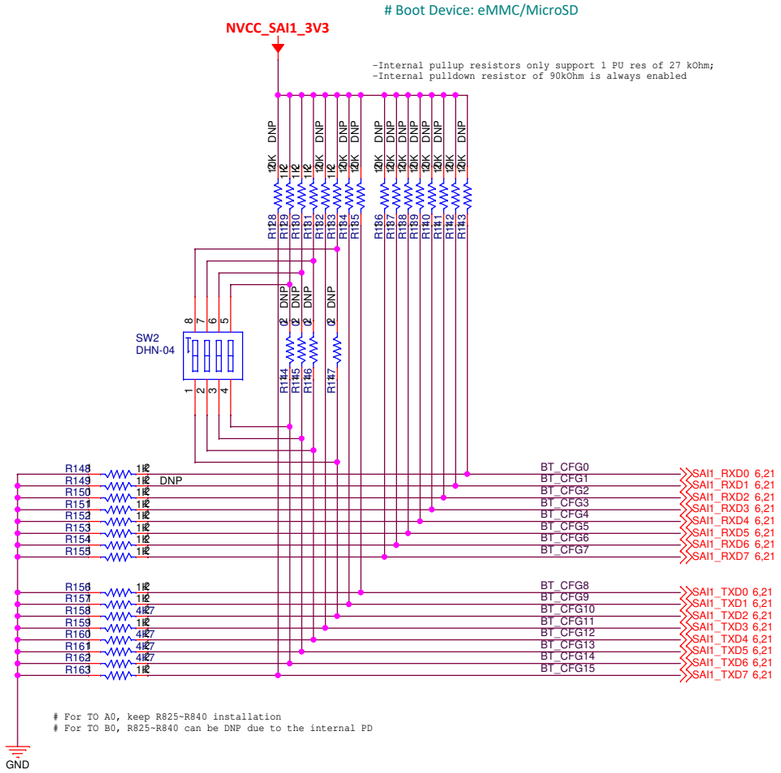
Boot ROM Fuse

<Default: eMMC BOOT>, QSPI boot is not supported by ROM

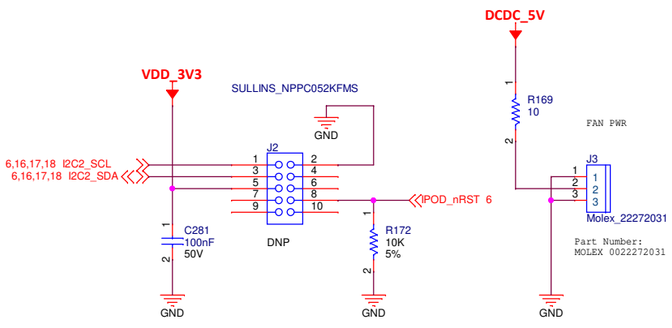
	Address	7	6	5	4	3	2	1	0
	0x470[15:8]	**BOOT_CFG[15]**	**BOOT_CFG[14]**	**BOOT_CFG[13]**	**BOOT_CFG[12]**	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**
	0x470[15:8]	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - eSDHC1 01 - eSDHC2		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			QSPI Instance 0 - QuadSPI0 1 - Reserved	SDR SMP: "000" : Default "001-111"		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC1 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	USDHC2 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'- 15 GPMICLK cycles.			Reserved
QSPI	0x470[7:0]	HSPHS: Half Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay selection 0 : one clock delay 1: two clock delay	Reserved	Reserved	Reserved	Reserved
SPINOR	0x470[7:0]	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

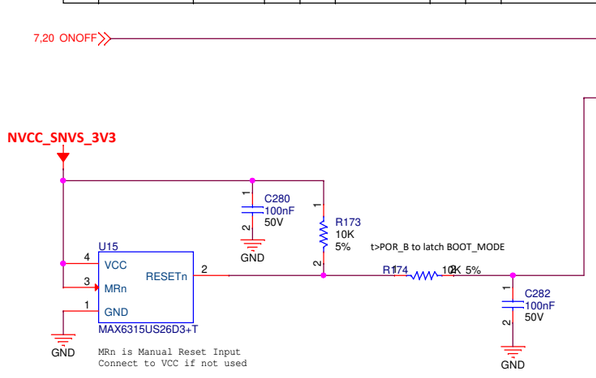
BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

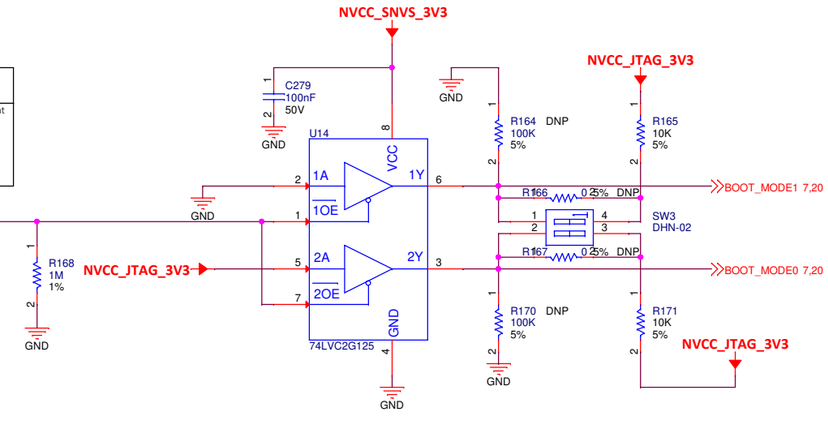
Boot Device: eMMC/MicroSD



item	Power state	ONOFF	RST	OE	DIP SW	BM1	BM0	Note	Description
1	During Power Up	H (No press)	L	H	1-4 : OFF; 2-3 : ON	0	1	Serial Downloader	item 1/2 for system development
2	During Power Up	H (No press)	L	H	1-4 : ON; 2-3 : OFF	1	0	Internal Boot	item 2/3 for system upgrade
3	During Power Up	L (Press)	L	L	1-4 : ON; 2-3 : OFF	0	1	Serial Downloader	
4	After Power Up	H (No press)	H	H	/	/	/	No power key event	Normal power key function
5	After Power Up	L (Short Press)	H	H	/	/	/	Power key event	
6	After Power Up	L (Long Press)	H	H	/	/	/	System power down	

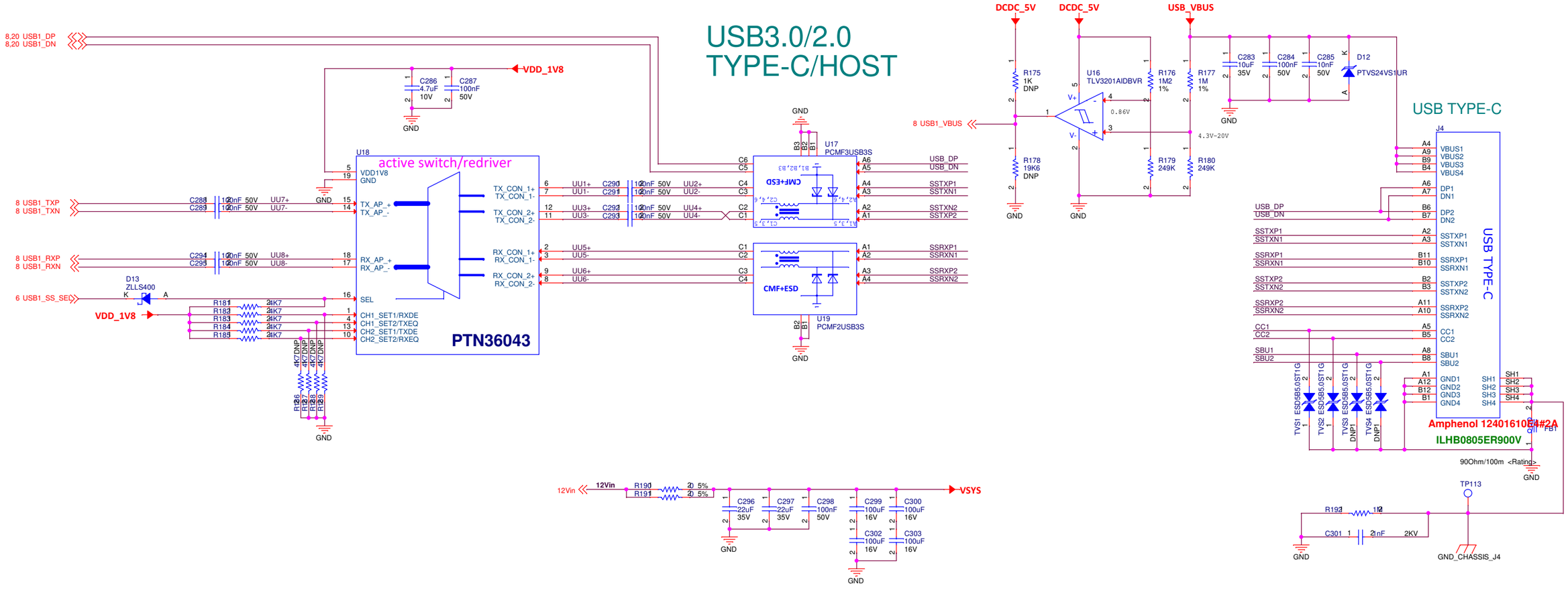


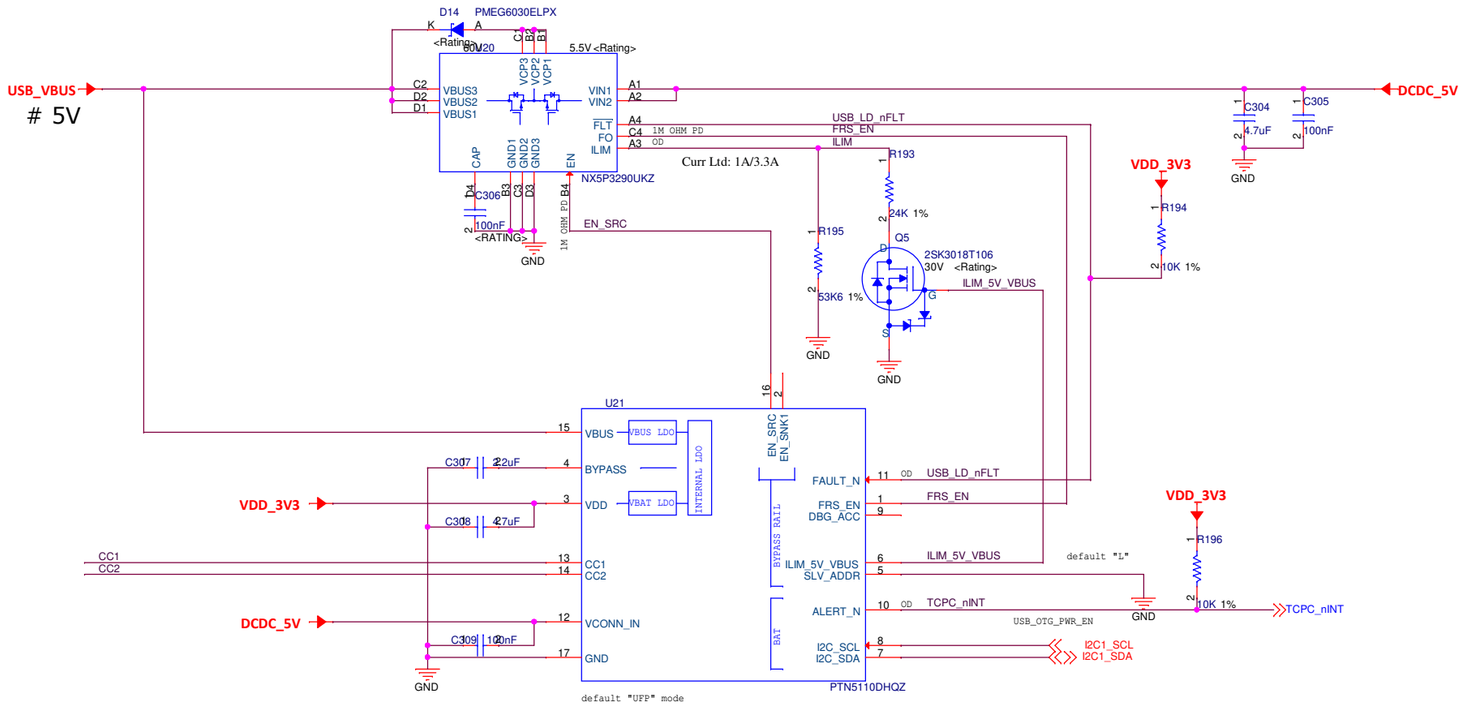




Title	Rototype - RLB
Size C	Document Number i.MX8M - 01 - MC - C-11 BOOT CFG
Rev	1.0
Date:	Wednesday, December 02, 2020
Sheet	0 of 47

USB3.0/2.0 TYPE-C/HOST

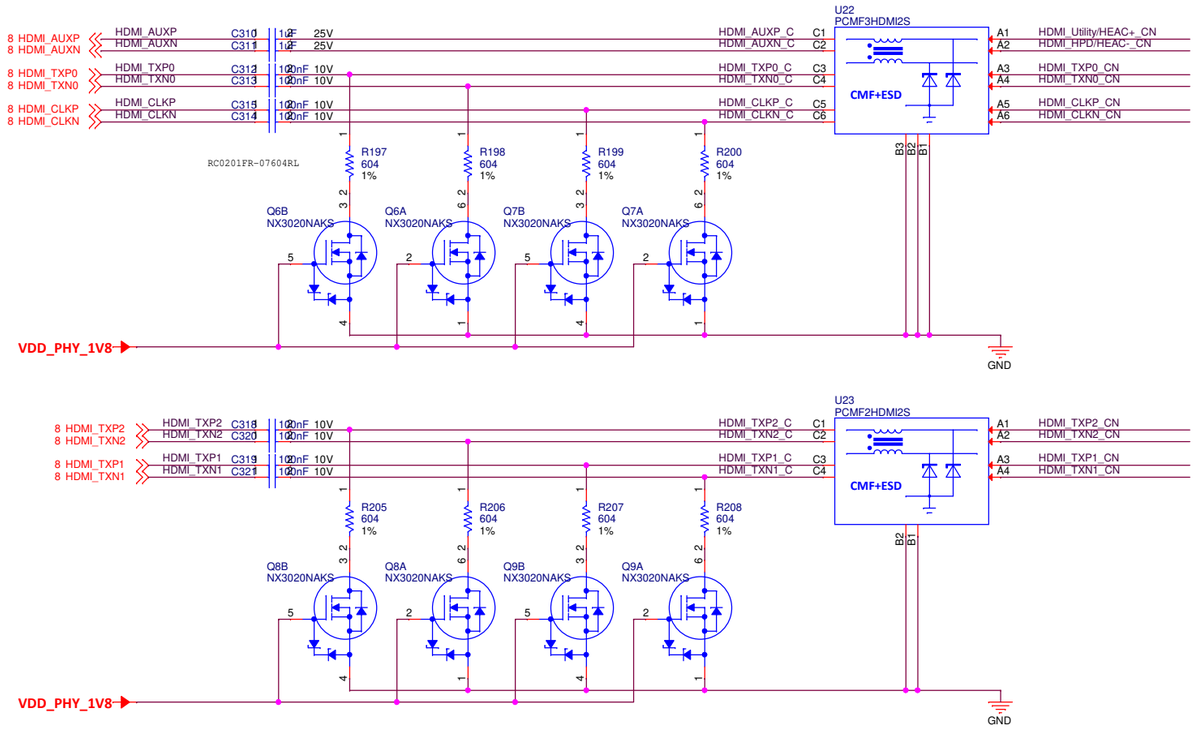


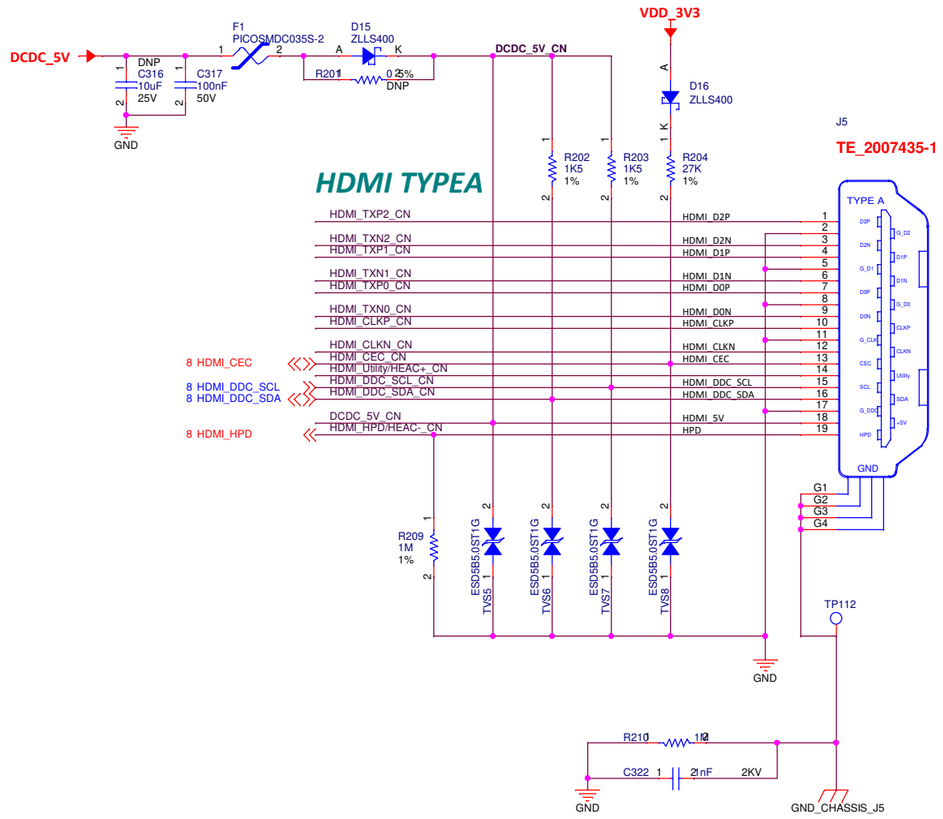


Title	Rototype - RLB	
Size C	Document Number i.MX8M - 01 - MC - C-12 USB TYPE-C/HOST	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

HDMI 2.0a TX

HDMI data EMI/ESD

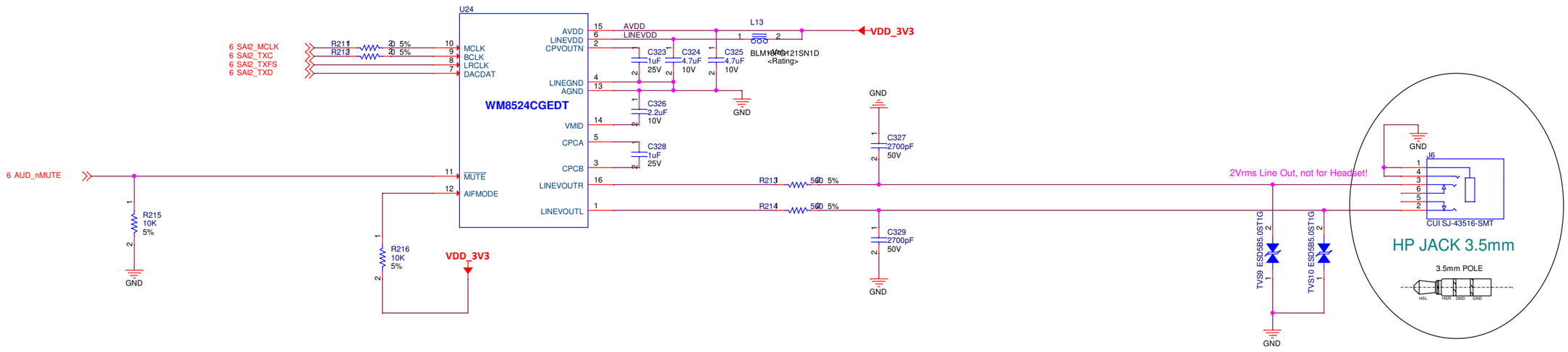




Title	Rototype - RLB	
Size C	Document Number i.MX8M - 01 - MC - C-13 HDMI	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

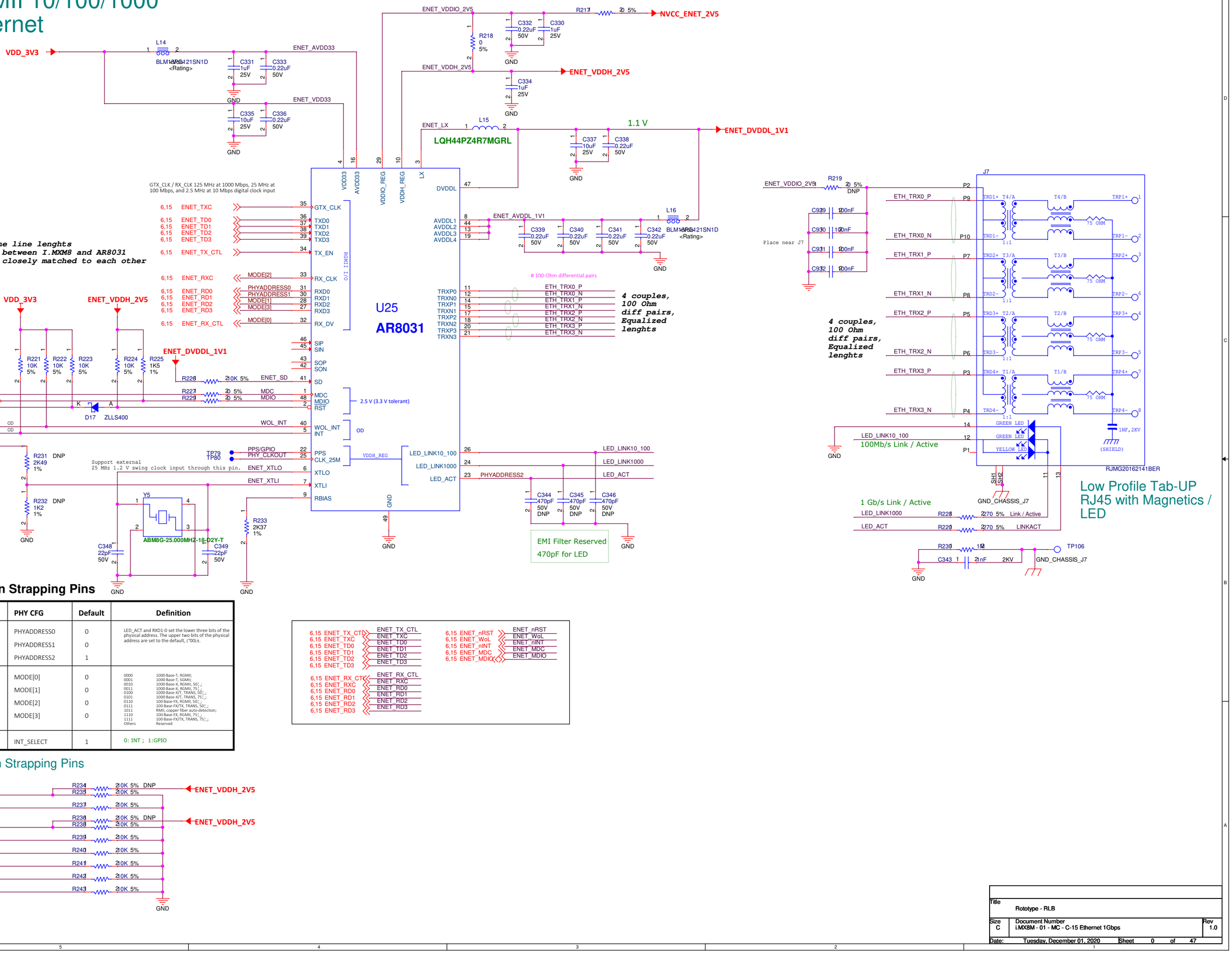
Audio DAC

24-bit 192kHz Stereo DAC 2Vrms Line Out



Title	Rototype - RLB	
Size C	Document Number iMX8M - 01 - MC - C-14 CODEC	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

RGMII 10/100/1000 Ethernet



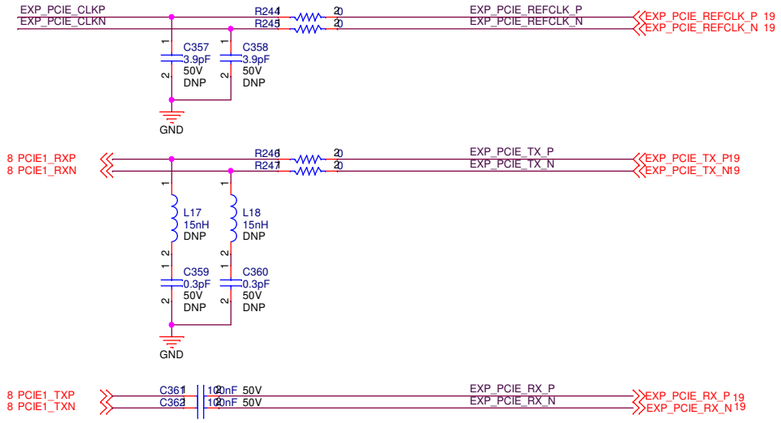
Power-on Strapping Pins

PHY PIN	PHY CFG	Default	Definition
RXD0	PHYADDRESS0	0	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, i"00i±.
RXD1	PHYADDRESS1	0	
LED_ACT	PHYADDRESS2	1	
RX_DV	MODE[0]	0	0000 1000 Base-T, RGMII; 0001 1000 Base-T, SGMII; 0010 1000 Base-X, RGMII, 50¦¸; 0011 1000 Base-X, RGMII, 75¦¸; 0100 1000 Base-X/T, TRANS, 50¦¸; 0101 1000 Base-X/T, TRANS, 75¦¸; 0110 100 Base-FX, RGMII, 50¦¸; 0111 100 Base-FX/TX, TRANS, 50¦¸; 1011 RMII, copper fiber auto-detection; 1110 100 Base-FX, RGMII, 75¦¸; 1111 100 Base-FX/TX, TRANS, 75¦¸; Others Reserved
RXD2	MODE[1]	0	
RX_CLK	MODE[2]	0	
RXD3	MODE[3]	0	
LED_LINK1000	INT_SELECT	1	0: INT ; 1:GPIO

Power-on Strapping Pins CFG

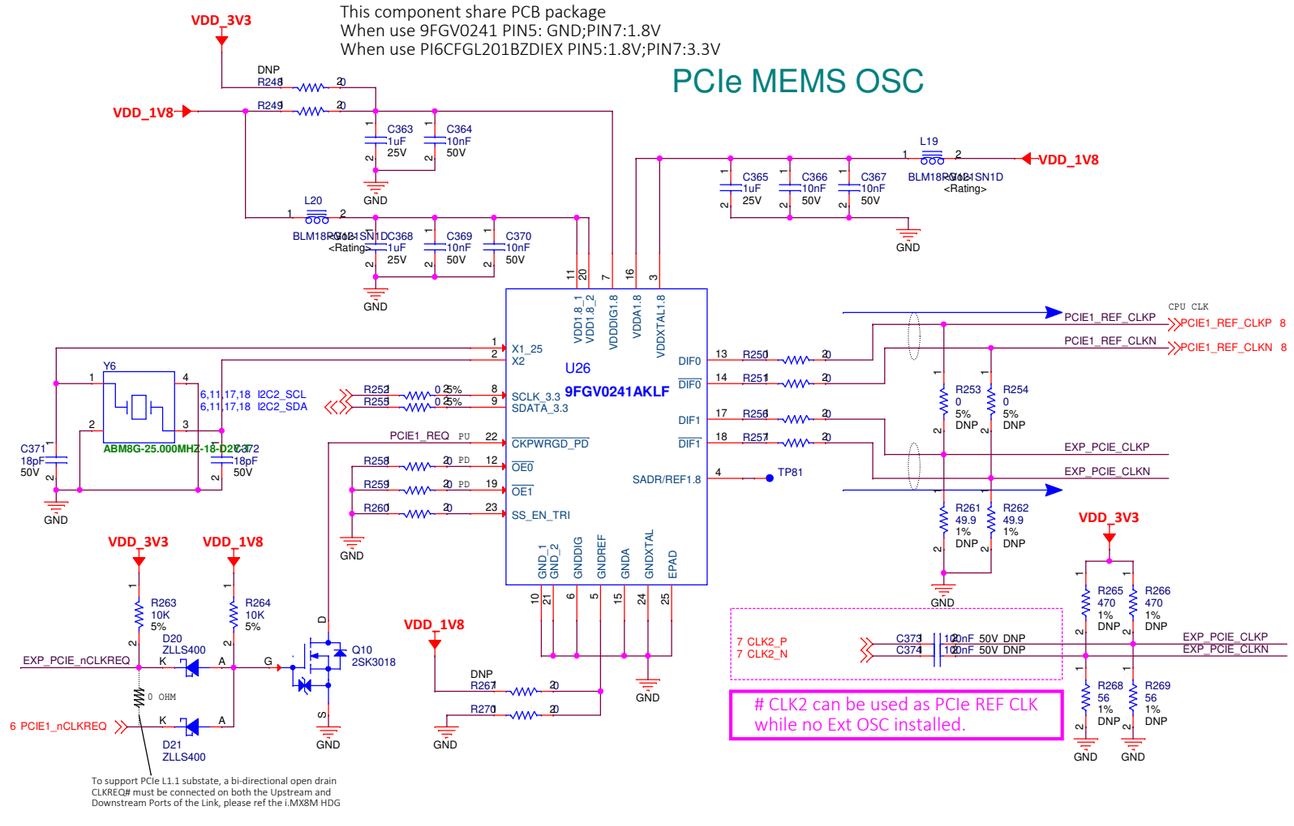
Title	Rototype - RLB	
Size C	Document Number i.MX8M - 01 - MC - C-15 Ethernet 1Gbps	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

PCIE1
connect



NOTE:
This component share PCB package
When use 9FGV0241 PIN5: GND;PIN7:1.8V
When use PI6CFGL201BZDIEX PIN5:1.8V;PIN7:3.3V

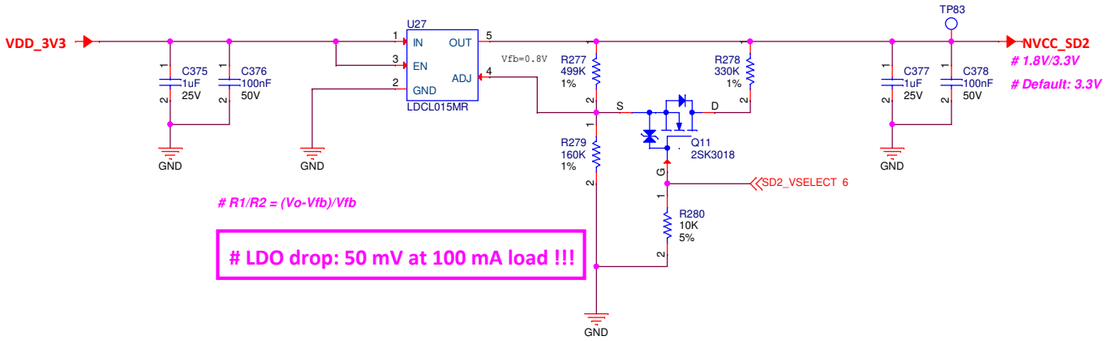
PCIe MEMS OSC



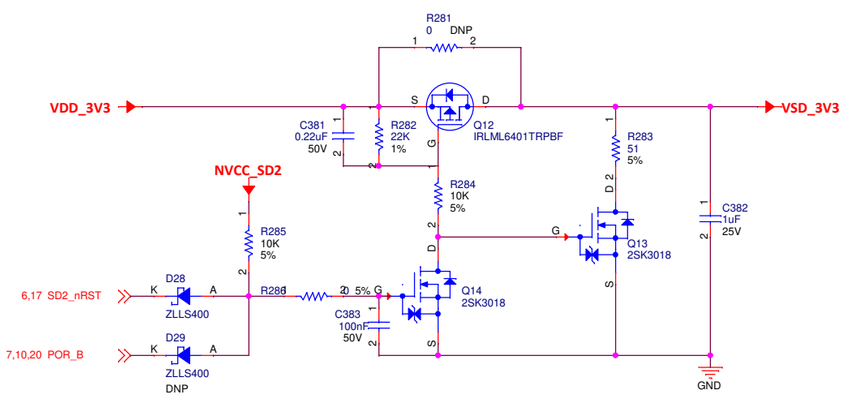
Title	Rototype - RLB	
Size C	Document Number i.MX8M - 01 - MC - C-16 PCI1 Conn e CLK	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

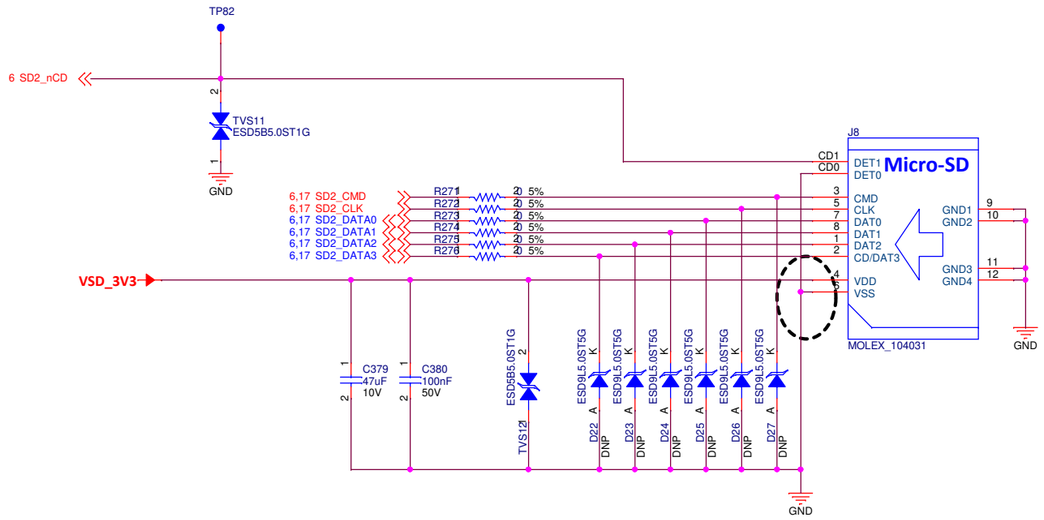
MicroSD/Infrared/LED

SD3.0 IO PWR



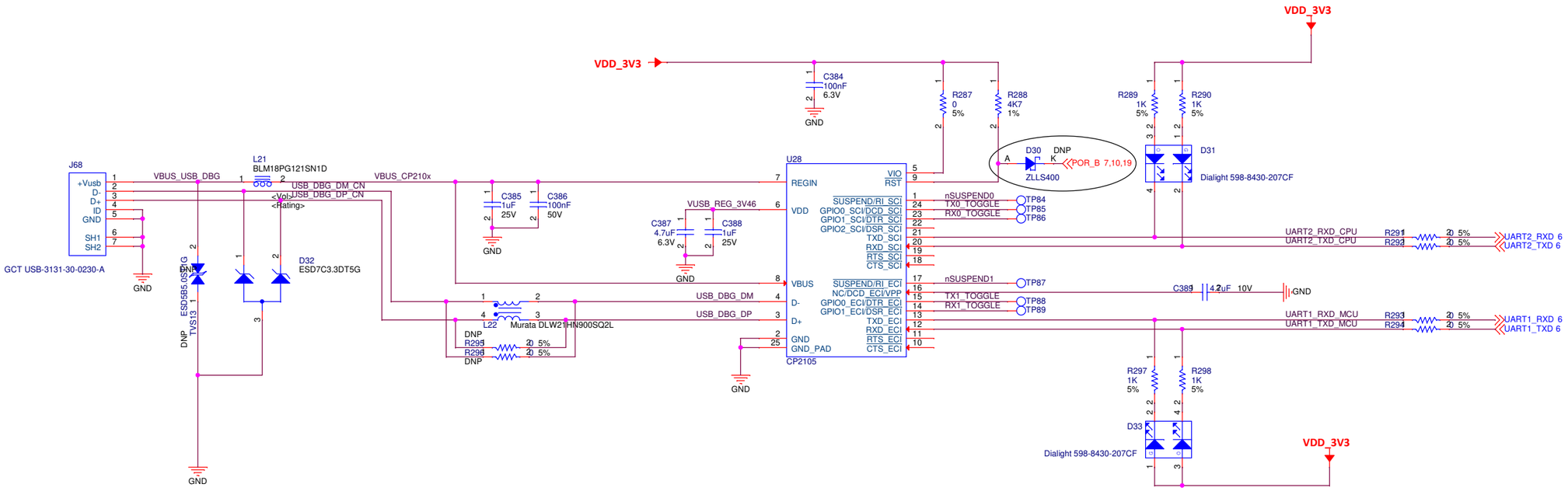
SD3.0 PWR



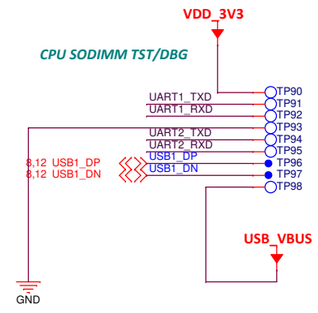


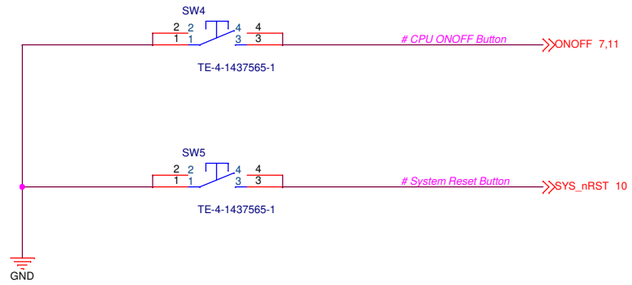
Title: Rototype - RLB		
Size: C	Document Number: i.MX8M - 01 - MC - C-19 mSD/Infr/LED/BTN	Rev: 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

UART-USB DBG



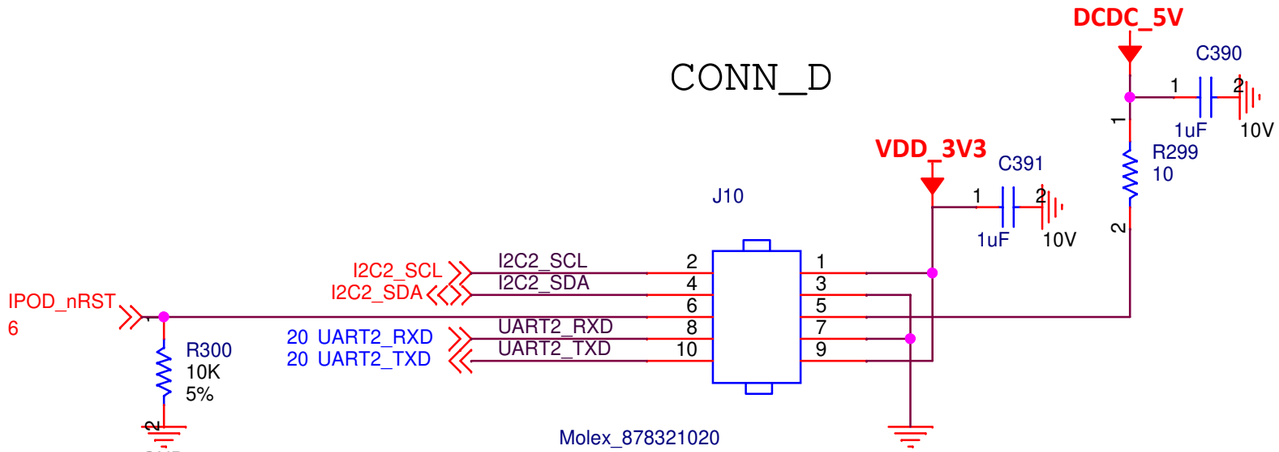
TP for on-line MFG





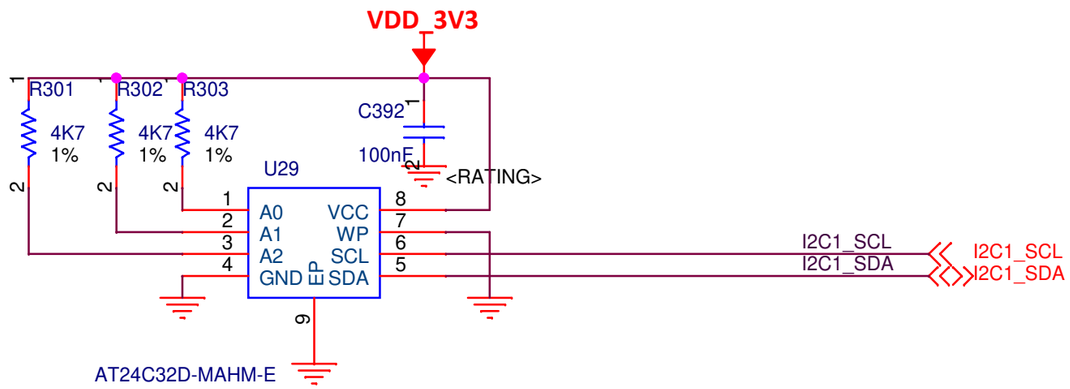
Title	Rototype - RLB	
Size C	Document Number i.MX8M - 01 - MC - C-20 Debug	Rev 1.0
Date: Wednesday, December 02, 2020	Sheet 0 of 47	

i.MX8M Display & Fan



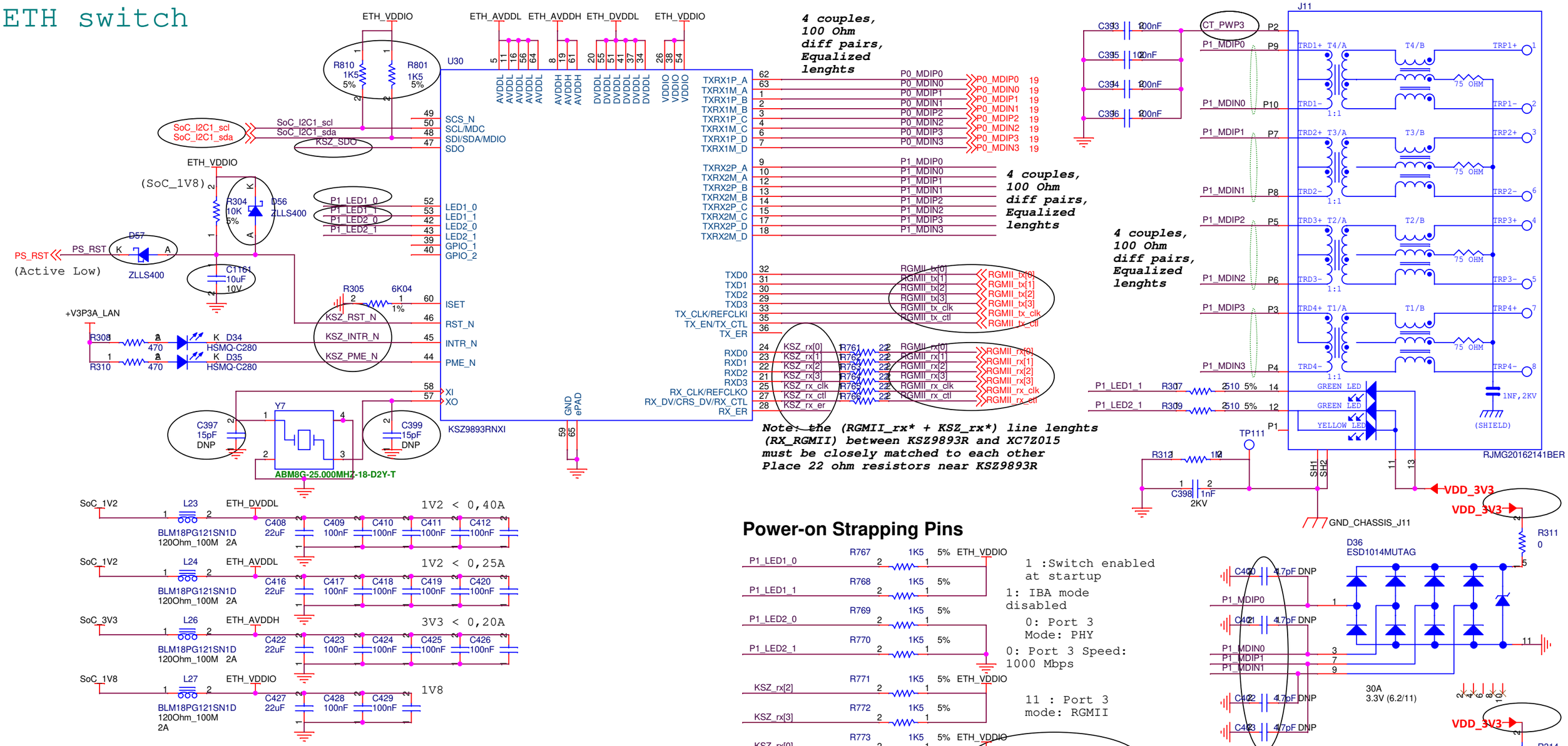
Title	Rototype - RLB	
Size: A4	Document Number: i.MX8M - 01 - MC - D - Display Fan	Rev: 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

i.MX8M EEPROM



Title	Rototype - RLB	
Size A4	Document Number i.MX8M - 01 - MC - D - EEPROM	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

ETH switch



Power-on Strapping Pins

Title	Rototype - RLB	
Size A3	Document Number i.MX8M - 01 - MC - D - ETH switch	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

i.MX8M - I210 PCI to ETH

VDD_3V3
L28
BLM18PG121SN1D
120Ohm_100M
<Rating>
+V3P3A_LAN

VDD_3V3 VDD_3V3
R318 10K 1%
R319 10K 1%

U32

13 EXP_PCIE_RX_P → EXP_PCIE_RX_P (24) PE_RP
13 EXP_PCIE_RX_N → EXP_PCIE_RX_N (23) PE_RN
13 EXP_PCIE_REFCLK_P → EXP_PCIE_REFCLK_P (26) PE_CLKP
13 EXP_PCIE_REFCLK_N → EXP_PCIE_REFCLK_N (25) PE_CLKN
PU 10K TO 3V3 LAN → (17) PE_RST_N
(16) PE_WAKE_N

C430 100nF <RATING>
6,11,17,18 I2C2_SCL → R320 0 5% → (34) SMB_CLK
6,11,17,18 I2C2_SDA → R324 0 5% → (36) SMB_DATA
I2C 100KHz
(35) SMB_ALRT_N

+V3P3A_LAN
R329 4K7 5%
R330 4K7 5%
R331 10K 1%
R332 10K 1%
R333 10K 1%
R334 10K 1%

TP122 → (63) SDP0
TP123 → (61) SDP1/PCIE_DIS
TP124 → (62) SDP2
TP125 → (60) SDP3
Place these seven TP Near I211

TP126 → (31) LED0
TP128 → (30) LED1
TP127 → (33) LED2

R335 0 → (46) XTAL1
R336 0 → (45) XTAL2
Y8 TSX-3225 25.0000MF10P-C3 <Rating>
C431 18pF <RATING>
C432 18pF <RATING>

PU 10K TO 3V3 LAN → (19) JTAG_CLK
PU 10K TO 3V3 LAN → (29) JTAG_TDI
PU 10K TO 3V3 LAN → (4) JTAG_TDO
PU 10K TO 3V3 LAN → (18) JTAG_TMS

(48) RSET
PU 3.3K TO 3V3 LAN → (28) DEV_OFF_N
PU 3.3K TO 3V3 LAN → (1) LAN_PWR_GOOD
R338 4K99 1%

+V0P9A_LAN +V1P5A_LAN → (22) RSVD_22_G
(56) VDD1P5_56
(47) VDD1P5_47
(42) VDD0P90_42
(32) VDD0P9_32
(11) VDD0P9_11
(59) VDD0P9_59
+V3P3A_LAN
(27) VDD3P3_27
(10) VDD3P3_10
(64) VDD3P3_64
(41) VDD3P3_41
(51) VDD3P3_51

Intel WGI210AT

(21) PE_TP ← EXP_PCIE_TX_P → EXP_PCIE_TX_P 13
(20) PE_TN ← EXP_PCIE_TX_N → EXP_PCIE_TX_N 13

(2) NC_SI_CLK_IN ← PD 10K TO GND R321 10K 1%
(3) NC_SI_CRS_DV ← PD 10K TO GND R322 10K 1%
(7) NC_SI_TX_EN ← PD 10K TO GND R323 10K 1%
(43) NC_SI_ARB_IN
(44) NC_SI_ARB_OUT
(9) NC_SI_TXD0 ← PU 10K TO 3V3 LAN R325 10K 1%
(8) NC_SI_TXD1 ← PU 10K TO 3V3 LAN R326 10K 1%
(6) NC_SI_RXD0 ← PU 10K TO 3V3 LAN R327 10K 1%
(5) NC_SI_RXD1 ← PU 10K TO 3V3 LAN R328 10K 1%
+V3P3A_LAN

(49) MDI_3_N ← P0_MDIN3 → P0_MDIN3 18
(50) MDI_3_P ← P0_MDIP3 → P0_MDIP3 18
(52) MDI_2_N ← P0_MDIN2 → P0_MDIN2 18
(53) MDI_2_P ← P0_MDIP2 → P0_MDIP2 18
(54) MDI_1_N ← P0_MDIN1 → P0_MDIN1 18
(55) MDI_1_P ← P0_MDIP1 → P0_MDIP1 18
(57) MDI_0_N ← P0_MDIN0 → P0_MDIN0 18
(58) MDI_0_P ← P0_MDIP0 → P0_MDIP0 18

4 couples, 100 Ohm diff pairs, Equalized lenghts

(15) NVM_CS_N → TP118
(12) NVM_SI → TP119
(14) NVM_SO ← PU 3.3K TO 3V3 LAN
(13) NVM_SK

+V3P3A_LAN
R337 4K7 5%
TP120
Place these four TP Near I210
TP121

+V0P9A_LAN +V1P5A_LAN
(39) VDD1P5_OUT
(38) VDD0P9_OUT
(40) CTOP
(37) CBOT
(65) EPAD

C433 39nF <RATING>
C434 10uF <RATING>
C435 10uF <RATING>

+V3P3A_LAN
C436 100nF <RATING>
C437 100nF <RATING>
C438 10uF <RATING>
C439 10uF <RATING>

+V1P5A_LAN
C440 100nF <RATING>
C441 100nF <RATING>
C442 10uF <RATING>
C443 10uF <RATING>

+V0P9A_LAN
C444 100nF <RATING>
C445 100nF <RATING>
C446 10uF <RATING>
C447 10uF <RATING>

Title: Rototype - RLB		
Size: A3	Document Number: i.MX8M - 01 - MC - D - I210 CPI to ETH	Rev: 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

i.MX8M QSPI - SoC & FPGA

C1162
100nF
<RATING>
VDD_3V3

Note: these resistors should be placed on top near MIMX8M (U1)

6 QSPIA_nSS1 — QSPIA_nSS1 — R784 10Ω 5%
6 QSPIA_nSS3 — QSPIA_nSS3 — R783 10Ω 5%
6 QSPIA_SCLK — MC_SPI_CLK — R340 10Ω 5%
6 QSPIA_DATA0 — QSPIA_DATA0 — R341 10Ω 5%
6 QSPIA_DATA1 — QSPIA_DATA1 — R342 10Ω 5%
6 QSPIA_DATA2 — QSPIA_DATA2 — R343 10Ω 5%
6 QSPIA_DATA3 — QSPIA_DATA3 — R344 10Ω 5%

U63 IDTQS3VH244

20	VCC		
2	1A1	1Y1	18
4	1A2	1Y2	16
6	1A3	1Y3	14
8	1A4	1Y4	12
1	1G		
11	2A1	2Y1	9
13	2A2	2Y2	7
15	2A3	2Y3	5
17	2A4	2Y4	3
19	2G		
	GND		10

Note: This IDTQS3VH244 and related resistors shall be placed on top near ZynQ QSPI (U45, U46)

R791 10Ω 5% — SoC_SPI_CS — SoC_SPI_CS
R787 10Ω 5% — SoC_SPI-SCK/MODE4 — SoC_SPI-SCK/MODE4
R788 10Ω 5% — SoC_SPI-DQ0/MODE0 — SoC_SPI-DQ0/MODE0
R789 10Ω 5% — SoC_SPI-DQ1/MODE1 — SoC_SPI-DQ1/MODE1
R790 10Ω 5% — SoC_SPI-DQ2/MODE2 — SoC_SPI-DQ2/MODE2
R792 10Ω 5% — SoC_SPI-DQ3/MODE3 — SoC_SPI-DQ3/MODE3

VDD_3V3
C1163
100nF
<RATING>

U64 IDTQS3VH244

20	VCC		
2	1A1	1Y1	18
4	1A2	1Y2	16
6	1A3	1Y3	14
8	1A4	1Y4	12
1	1G		
11	2A1	2Y1	9
13	2A2	2Y2	7
15	2A3	2Y3	5
17	2A4	2Y4	3
19	2G		
	GND		10

Note: This IDTQS3VH244 and related resistors shall be placed on top near Spartan7 QSPI (U57, U58)

R798 10Ω 5% — QSPI_FPGA_SPI_CS — QSPI_FPGA_SPI_CS
R797 10Ω 5% — QSPI_FPGA_SPI-SCK — QSPI_FPGA_SPI-SCK
R796 10Ω 5% — QSPI_FPGA_SPI-DQ0 — QSPI_FPGA_SPI-DQ0
R795 10Ω 5% — QSPI_FPGA_SPI-DQ1 — QSPI_FPGA_SPI-DQ1
R794 10Ω 5% — QSPI_FPGA_SPI-DQ2 — QSPI_FPGA_SPI-DQ2
R793 10Ω 5% — QSPI_FPGA_SPI-DQ3 — QSPI_FPGA_SPI-DQ3

6 nQSPIA_access_EN — nQSPIA_access_EN
R807 2K4 1%

Note: This signal shall be set at '1' at the end of Linux boot to permit FPGA to QSPI connection

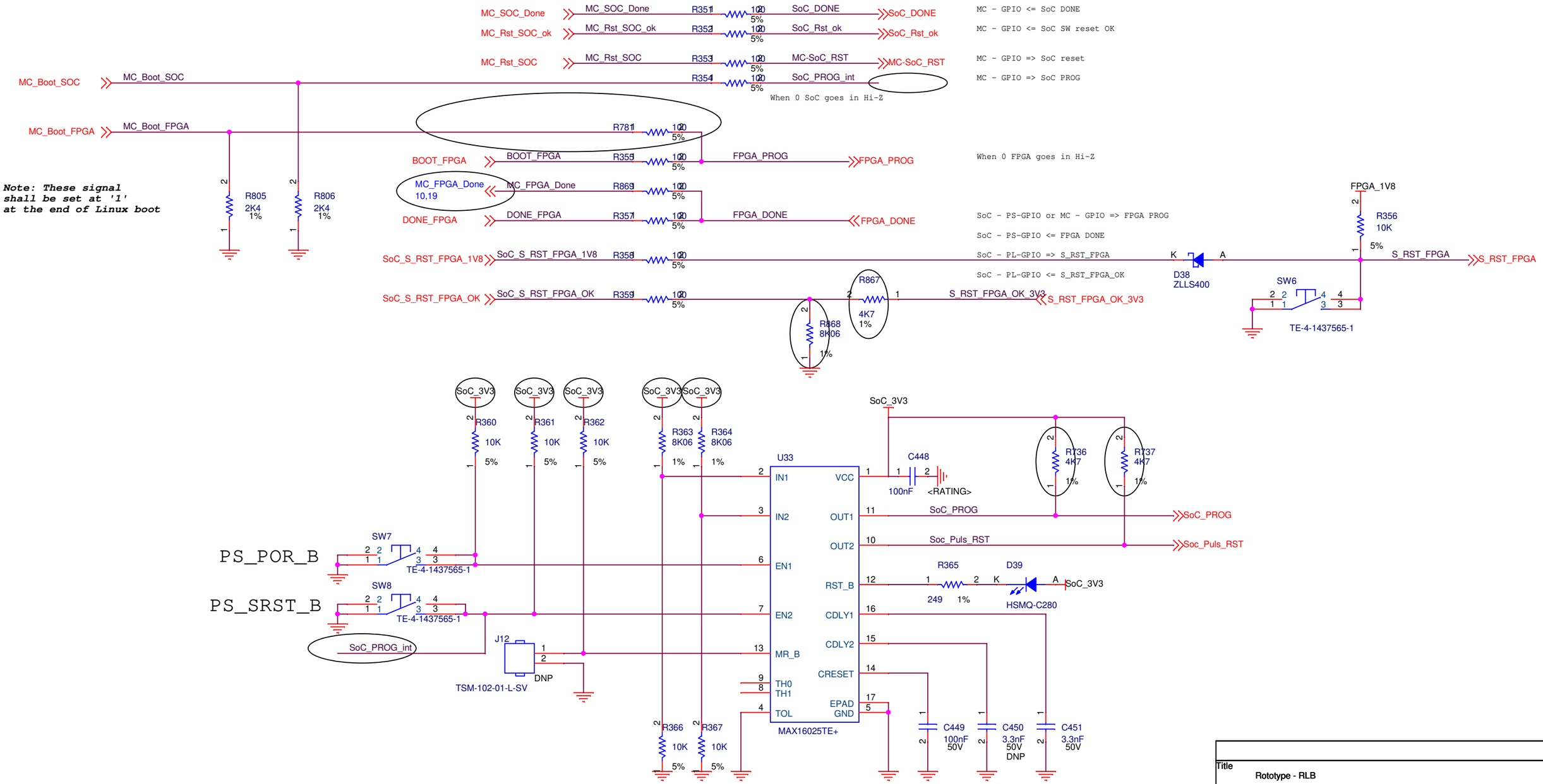
A=Y when G = '0'
Hi-Z when G = '1'

Title	Rototype - RLB	
Size A4	Document Number i.MX8M - 01 - MC - D - QSPI	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

i.MX8M Reset SoC e FPGA

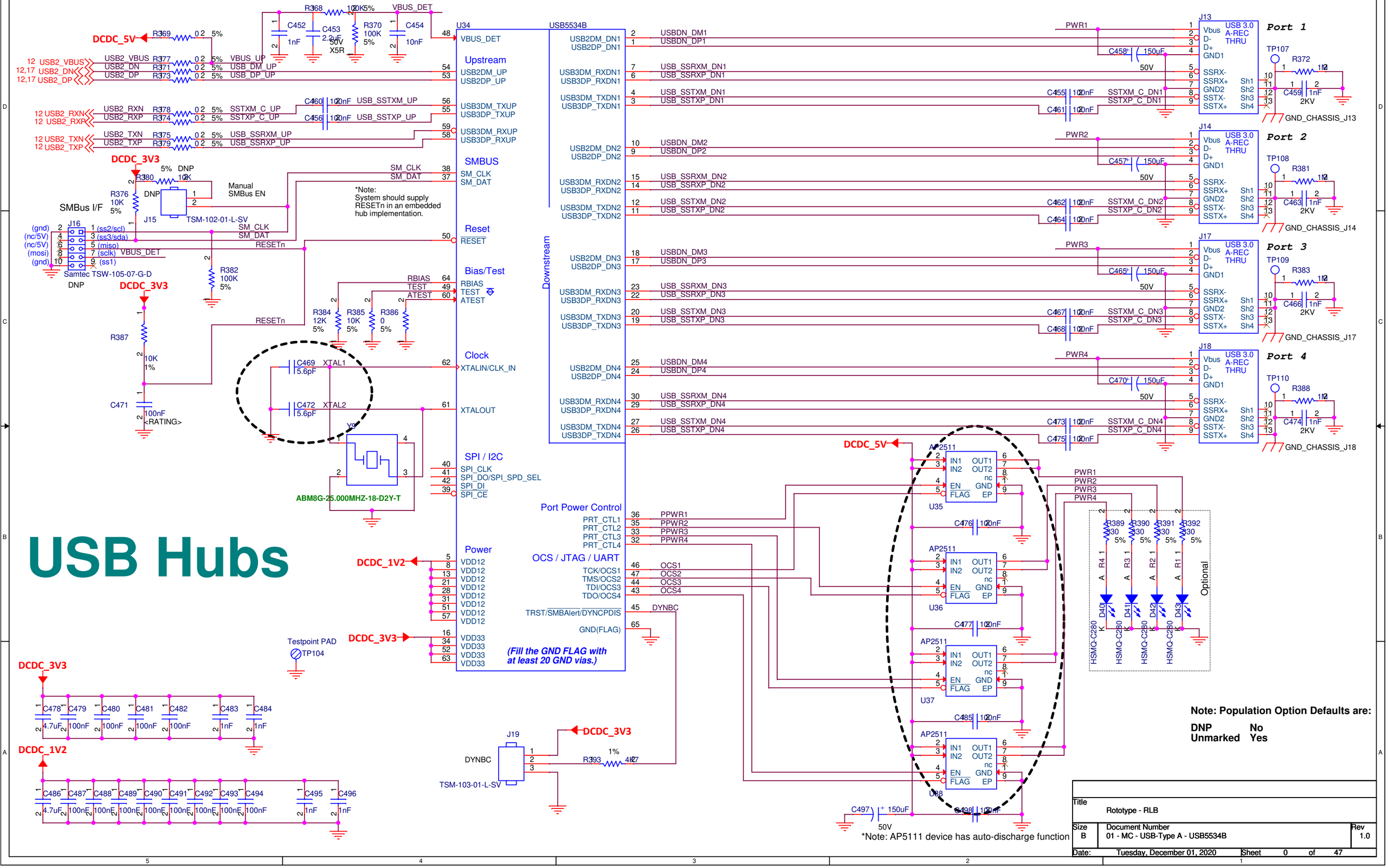
Logica di reset, la MC controlla il reset della SoC e il SoC il reset dell' FPGA

~~Logica di boot, la MC controlla il boot della SoC e della FPGA (indipendenti), il SoC puo' comunque controllare il boot dell' FPGA~~



Title	Rototype - RLB	
Size A3	Document Number i.MX8M - 01 - MC - D - Reset	Rev 1.0
Date: Wednesday, December 02, 2020	Sheet 0 of 47	

USB Hubs

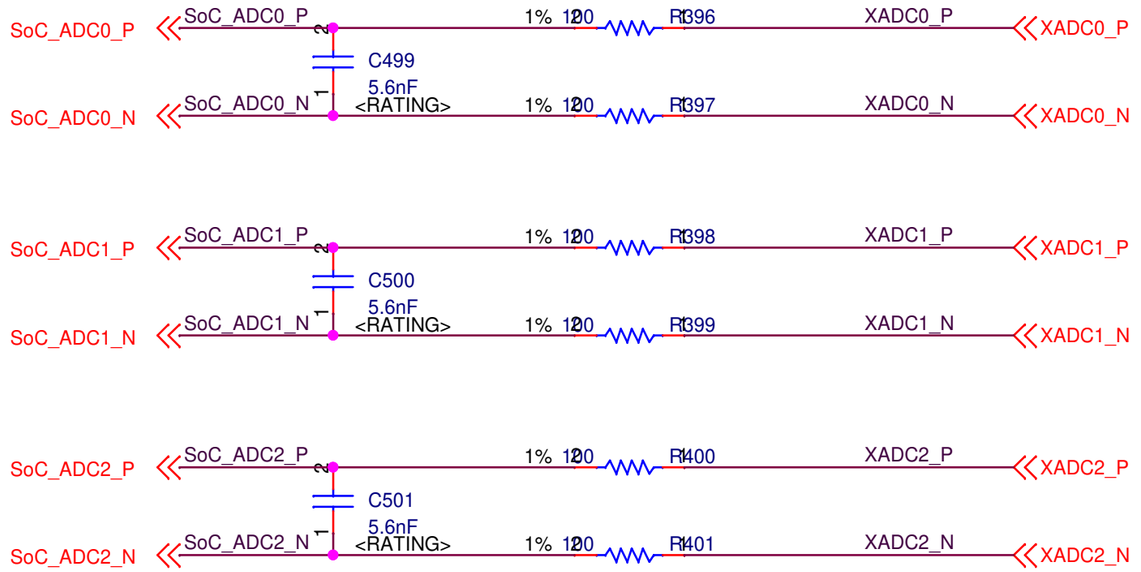


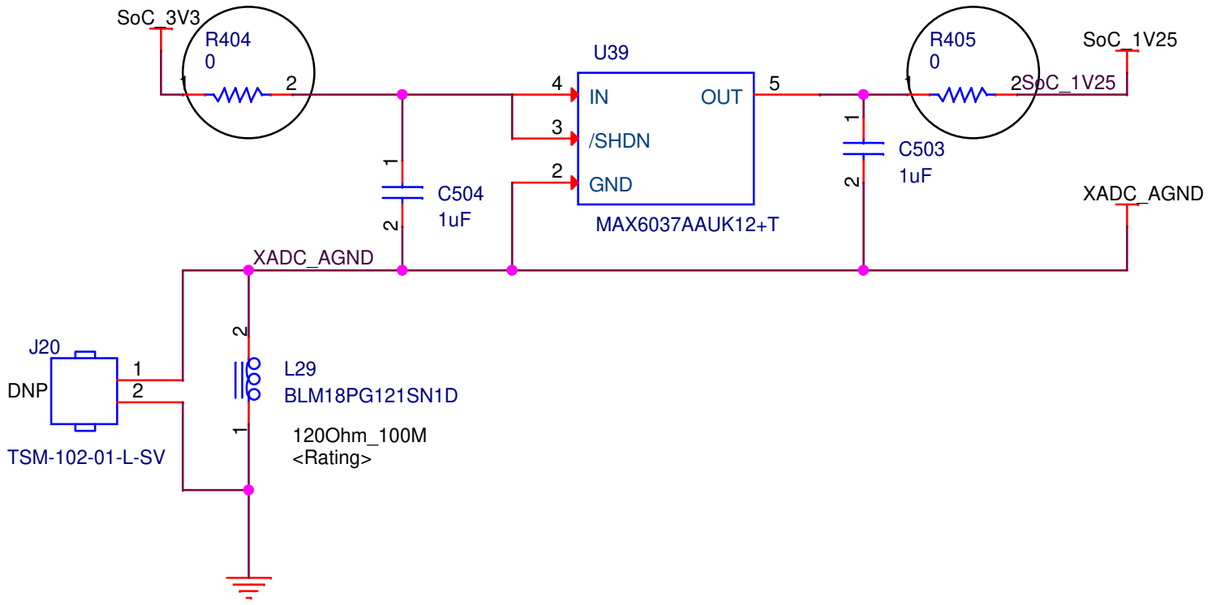
Title	Rototype - RLB		
Size B	Document Number 01 - MC - USB-Type A - USB5534B		Rev 1.0
Date: Tuesday, December 01, 2020		Sheet 0 of 47	

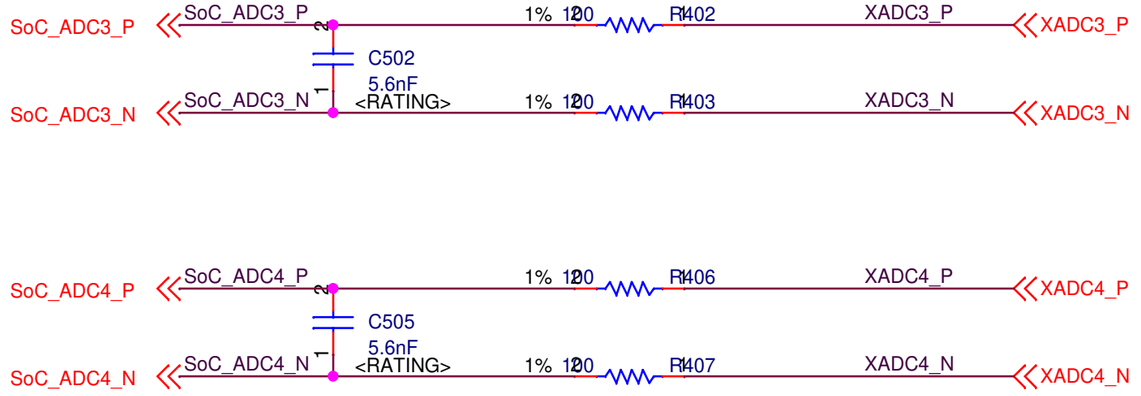
SoC - ADCn

According to Xapp 795 ("Driving the Xilinx Analog-to-Digital Converter" pag. 3)

See Anti-Aliasing_calculetion.xls; Fcut = ~300kHz @ 12 bit resolution

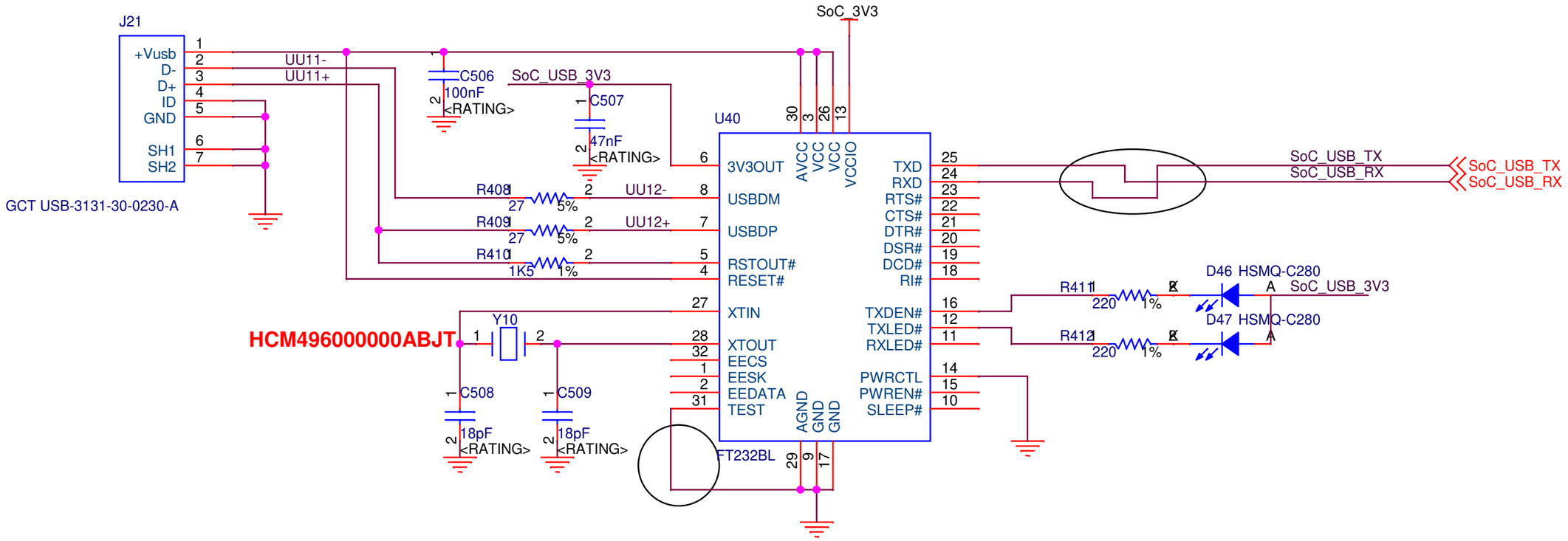






Title: Rototype - RLB		
Size: A4	Document Number: SoC - 02 - SoC - ADC	Rev: 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

SoC - USB Debug



Title	Rototype - RLB	
Size A4	Document Number SoC - 02 - SoC - DBG UART	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

SoC - DDR3

Stefano - 17/12/2019

U41 MT41J128M16JT-125K TR (DDR3)

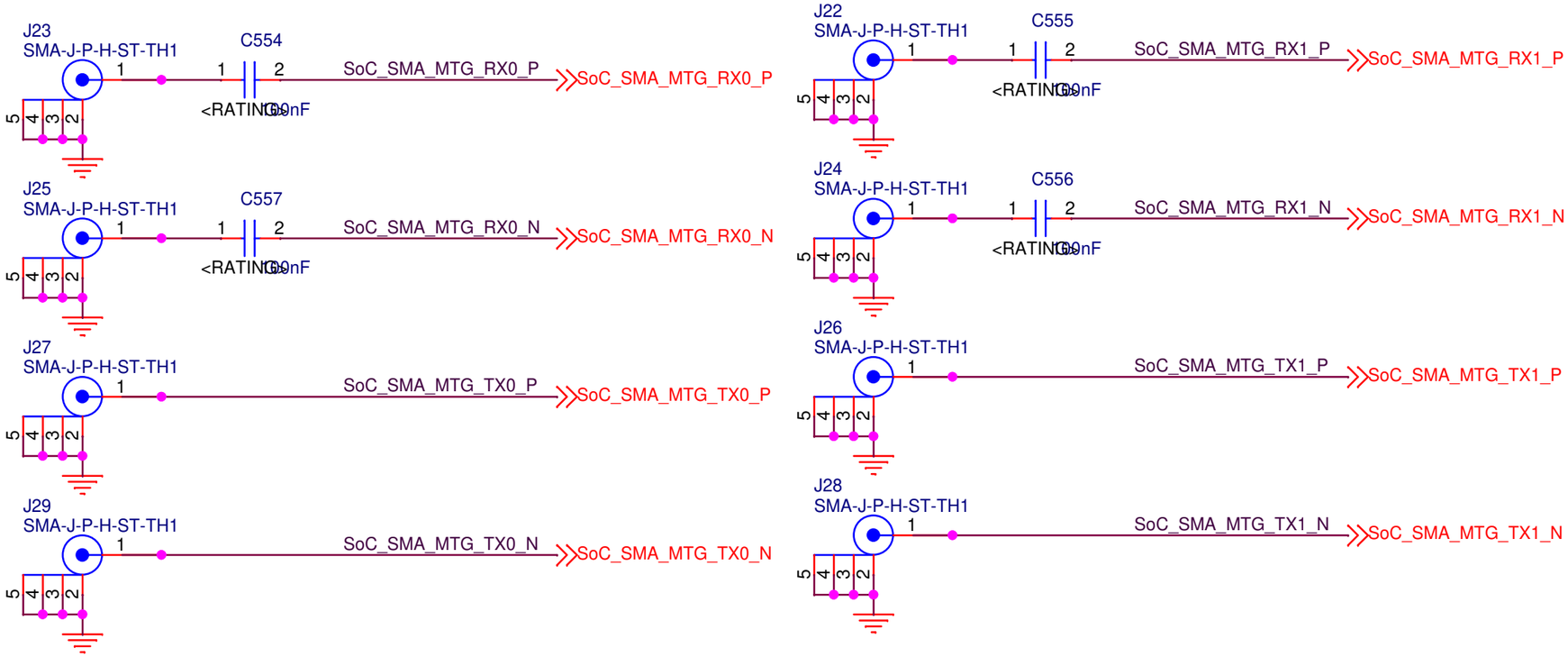
U42 MT41J128M16JT-125K TR (DDR3)

U43 MAX1510ETB

SoC_DDR_1V5 · SoC_3V3 · SoC_1V5 · SoC_DDR_VREF · SoC_DDR0V75

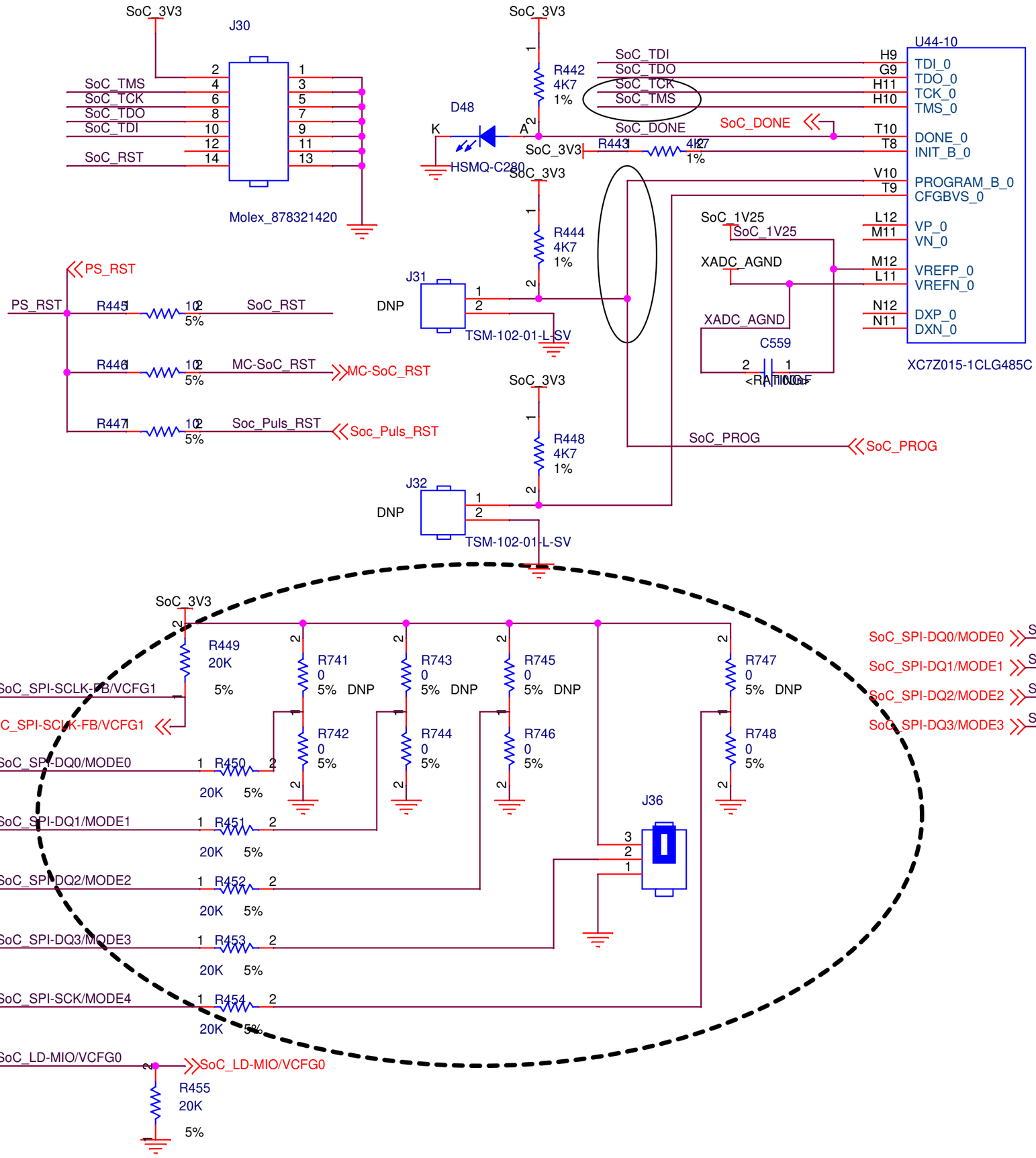
Title	Rototype - RLB		
Size A3	Document Number SoC - 02 - SoC - DDR3		Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47		

SoC - EXP



Title	Rototype - RLB	
Size A4	Document Number SoC - 02 - SoC - HWC_EXP	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

SoC - JTAG



Title	Rototype - RLB	
Size A4	Document Number SoC - 02 - SoC - JTAG	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

SoC - PL

U44-7

BANK 13

IO_0_13	T16					SoC_S_RST_FPGA
IO_25_13	U16			R456	0	C2C_TX_DATA11
IO_L10N_T1_13	Y13			R457	0	C2C_RX_DATA3
IO_L10P_T1_13	Y12			R458	0	C2C_RX_DATA7
IO_L11N_T1_SRCC_13	AA15	R459	100 1%	R460	0	C2C_TX_CLK_N
IO_L11P_T1_SRCC_13	AA14	R461	100 1%	R462	0	C2C_TX_CLK_P
IO_L12N_T1_MRCC_13	Y15	SoC_200_CLK_N				SoC_200_CLK_N
IO_L12P_T1_MRCC_13	Y14	SoC_200_CLK_P				SoC_200_CLK_P
IO_L13N_T2_MRCC_13	Y19	SoC_156_CLK_N				SoC_156_CLK_N
IO_L13P_T2_MRCC_13	Y18	SoC_156_CLK_P				SoC_156_CLK_P
IO_L14N_T2_SRCC_13	AA17	R463	100 1%	R464	0	C2C_RX_CLK_N
IO_L14P_T2_SRCC_13	AA16	R465	100 1%	R466	0	C2C_RX_CLK_P
IO_L15N_T2_DQS_13	AB22					SoC_S_RST_FPGA_OK
IO_L15P_T2_DQS_13	AB21			R467	0	C2C_X2M_IRQ_OUT0
IO_L16N_T2_13	AB19			R468	0	C2C_TX_DATA1
IO_L16P_T2_13	AB18			R469	0	C2C_TX_DATA5
IO_L17N_T2_13	AB17			R470	0	C2C_TX_DATA10
IO_L17P_T2_13	AB16			R471	0	C2C_TX_DATA14
IO_L18N_T2_13	AA20			R472	0	C2C_X2M_IRQ_OUT1
IO_L18P_T2_13	AA19			R473	0	C2C_TX_DATA0
IO_L19N_T3_VREF_13	T17					
IO_L19P_T3_13	R17			R474	0	C2C_TX_DATA6
IO_L1N_T0_13	V14			R475	0	C2C_X2M_IRQ_IN2
IO_L1P_T0_13	V13			R476	0	C2C_RX_DATA1
IO_L20N_T3_13	V19			R477	0	C2C_X2M_IRQ_OUT3
IO_L20P_T3_13	U19			R478	0	C2C_X2M_IRQ_OUT2
IO_L21N_T3_DQS_13	W18			R479	0	C2C_TX_DATA4
IO_L21P_T3_DQS_13	V18			R480	0	C2C_TX_DATA3
IO_L22N_T3_13	U18			R481	0	C2C_TX_DATA2
IO_L22P_T3_13	U17			R482	0	C2C_TX_DATA7
IO_L23N_T3_13	W16			R483	0	C2C_TX_DATA13
IO_L23P_T3_13	V16			R484	0	C2C_TX_DATA12
IO_L24N_T3_13	Y17			R485	0	C2C_TX_DATA9
IO_L24P_T3_13	W17			R486	0	C2C_TX_DATA8
IO_L2N_T0_13	W15			R487	0	C2C_X2M_IRQ_IN1
IO_L2P_T0_13	V15			R488	0	C2C_X2M_IRQ_IN0
IO_L3N_T0_DQS_13	W13			R489	0	C2C_RX_DATA2
IO_L3P_T0_DQS_13	W12			R491	0	C2C_RX_DATA6
IO_L4N_T0_13	W11			R492	0	C2C_RX_DATA12
IO_L4P_T0_13	V11			R493	0	C2C_RX_DATA11
IO_L5N_T0_13	U12			R494	0	C2C_RX_DATA5
IO_L5P_T0_13	U11			R495	0	C2C_RX_DATA10
IO_L6N_T0_VREF_13	U14			R496	0	S_spare → TP105
IO_L6P_T0_13	U13			R497	0	C2C_RX_DATA0
IO_L7N_T1_13	AB11			R498	0	C2C_RX_DATA14
IO_L7P_T1_13	AA11			R500	0	C2C_RX_DATA13
IO_L8N_T1_13	AB12			R501	0	C2C_RX_DATA8
IO_L8P_T1_13	AA12			R502	0	C2C_RX_DATA9
IO_L9N_T1_DQS_13	AB14			R503	0	C2C_X2M_IRQ_IN3
IO_L9P_T1_DQS_13	AB13			R504	0	C2C_RX_DATA4

XC7Z015-1CLG485C

place 10 ohm resistors on Top near to XC7Z015

U44-9

BANK 35

IO_0_35	H6	tst_9	
IO_25_35	H5	ZPL_IO_2	ZPL_IO_2
IO_L10N_T1_AD11N_35	A4	MICR0_MISO_N	MICR0_MISO_N
IO_L10P_T1_AD11P_35	A5	MICR0_MISO_P	MICR0_MISO_P
IO_L11N_T1_SRCC_35	C5	ZPL_IO_6	ZPL_IO_6
IO_L11P_T1_SRCC_35	C6	ZPL_IO_0	ZPL_IO_0
IO_L12N_T1_MRCC_35	C4	ZPL_IO_7	ZPL_IO_7
IO_L12P_T1_MRCC_35	D5	ZPL_IO_5	ZPL_IO_5
IO_L13N_T2_MRCC_35	B3	ZPL_IO_9	ZPL_IO_9
IO_L13P_T2_MRCC_35	C3	SoC_ADC4_N	SoC_ADC4_N
IO_L14N_T2_AD4N_SRCC_35	D3	SoC_ADC4_P	SoC_ADC4_P
IO_L14P_T2_AD4P_SRCC_35	A1	MICR1_CS1_N	MICR1_CS1_N
IO_L15N_T2_DQS_AD12N_35	A2	MICR1_CS1_P	MICR1_CS1_P
IO_L15P_T2_DQS_AD12P_35	C1	MICR1_MISO_N	MICR1_MISO_N
IO_L16N_T2_35	D1	MICR1_MISO_P	MICR1_MISO_P
IO_L16P_T2_35	D2	MICR0_CS2_N	MICR0_CS2_N
IO_L17N_T2_AD5N_35	E2	MICR0_CS2_P	MICR0_CS2_P
IO_L17P_T2_AD5P_35	B1	MICR1_MOSI_N	MICR1_MOSI_N
IO_L18N_T2_AD13N_35	B2	MICR1_MOSI_P	MICR1_MOSI_P
IO_L18P_T2_AD13P_35	H3		
IO_L19N_T3_VREF_35	H4		
IO_L19P_T3_35	E7	SoC_ADC0_N	
IO_L1N_T0_AD0N_35	F7	SoC_ADC0_P	SoC_ADC0_N
IO_L1P_T0_AD0P_35	F4	MICR0_SCLK_N	SoC_ADC0_P
IO_L20N_T3_AD6N_35	G4	MICR0_SCLK_P	MICR0_SCLK_N
IO_L20P_T3_AD6P_35	E3	MICR0_MOSI_N	MICR0_SCLK_P
IO_L21N_T3_DQS_AD14N_35	E4	MICR0_MOSI_P	MICR0_MOSI_N
IO_L21P_T3_DQS_AD14P_35	G2	MICR0_CS1_N	MICR0_MOSI_P
IO_L22N_T3_AD7N_35	G3	MICR0_CS1_P	MICR0_CS1_N
IO_L22P_T3_AD7P_35	F1	MICR1_SCLK_N	MICR0_CS1_P
IO_L23N_T3_35	F2	MICR1_SCLK_P	MICR1_SCLK_N
IO_L23P_T3_35	G1	MICR1_CS2_N	MICR1_SCLK_P
IO_L24N_T3_AD15N_35	H1	MICR1_CS2_P	MICR1_CS2_N
IO_L24P_T3_AD15P_35	D6	tst_11	MICR1_CS2_P
IO_L2N_T0_AD8N_35	D7	tst_7	
IO_L2P_T0_AD8P_35	D8	SoC_ADC1_N	
IO_L3N_T0_DQS_AD1N_35	E8	SoC_ADC1_P	SoC_ADC1_N
IO_L3P_T0_DQS_AD1P_35	G7	tst_6	SoC_ADC1_P
IO_L4N_T0_35	G8	tst_5	
IO_L4P_T0_35	E5	ZPL_IO_4	ZPL_IO_4
IO_L5N_T0_AD9N_35	F5	ZPL_IO_3	ZPL_IO_3
IO_L5P_T0_AD9P_35	F6		
IO_L6N_T0_VREF_35	G6	tst_10	
IO_L6P_T0_35	B8	SoC_ADC2_N	
IO_L7N_T1_AD2N_35	C8	SoC_ADC2_P	SoC_ADC2_N
IO_L7P_T1_AD2P_35	B6	ZPL_IO_1	SoC_ADC2_P
IO_L8N_T1_AD10N_35	B7	tst_8	ZPL_IO_1
IO_L8P_T1_AD10P_35	A6	SoC_ADC3_N	
IO_L9N_T1_DQS_AD3N_35	A7	SoC_ADC3_P	SoC_ADC3_N
IO_L9P_T1_DQS_AD3P_35	B4	ZPL_IO_8	SoC_ADC3_P
IO_L13P_T2_MRCC_35			ZPL_IO_8

XC7Z015-1CLG485C

place Test Points on Top, nearest to XC7Z017

tst_5 → J38
tst_6 → J39
tst_7 → J40
tst_8 → J41
tst_9 → J42
tst_10 → J43
tst_11 → J44

SoC_3V3

R490 4K7 1%

R499 4K7 1%

S_spare connesso ma non presente in EXCEL

U44-8

BANK 34

IO_0_34	H8		
IO_25_34	R8		
IO_L10N_T1_34	L1	IKJ1_DIN2	IKJ1_DIN2
IO_L10P_T1_34	L2	IKJ1_DIN1	IKJ1_DIN1
IO_L11N_T1_SRCC_34	K3	IKJ0_PWFIRE	IKJ0_PWFIRE
IO_L11P_T1_SRCC_34	K4	IKJ0_HFIRE	IKJ0_HFIRE
IO_L12N_T1_MRCC_34	L4		
IO_L12P_T1_MRCC_34	L5		
IO_L13N_T2_MRCC_34	T1	clk1_tst_N	
IO_L13P_T2_MRCC_34	T2	clk1_tst_P	
IO_L14N_T2_SRCC_34	U1	tst_3	
IO_L14P_T2_SRCC_34	U2	tst_4	
IO_L15N_T2_DQS_34	M1	IKJ2_DOUT	IKJ2_DOUT
IO_L15P_T2_DQS_34	M2	IKJ2_HCLK	IKJ2_HCLK
IO_L16N_T2_34	P1	IKJ3_DIN1	IKJ3_DIN1
IO_L16P_T2_34	N1		
IO_L17N_T2_34	R2	IKJ3_PWFIRE	IKJ3_PWFIRE
IO_L17P_T2_34	R3	tst_0	
IO_L18N_T2_34	P2	IKJ3_DIN2	
IO_L18P_T2_34	P3	IKJ3_DCLK	IKJ3_DIN2
IO_L19N_T3_VREF_34	N5	IKJ3_DOUT	IKJ3_DCLK
IO_L19P_T3_34	N6	IKJ3_HCLK	IKJ3_DOUT
IO_L1N_T0_34	K8	IKJ3_HFIRE	IKJ3_HCLK
IO_L1P_T0_34	J8		IKJ3_HFIRE
IO_L20N_T3_34	P5	IKJ3_DLOAD	
IO_L20P_T3_34	P6	IKJ2_DLOAD	IKJ3_DLOAD
IO_L21N_T3_DQS_34	N3	IKJ2_HFIRE	IKJ2_DLOAD
IO_L21P_T3_DQS_34	N4	IKJ2_PWFIRE	IKJ2_HFIRE
IO_L22N_T3_34	M3	IKJ2_DIN1	IKJ2_PWFIRE
IO_L22P_T3_34	M4	IKJ2_DIN2	IKJ2_DIN1
IO_L23N_T3_34	R4	tst_1	IKJ2_DIN2
IO_L23P_T3_34	R5	tst_2	
IO_L24N_T3_34	R7	IKJ1_PWFIRE	
IO_L24P_T3_34	P7	IKJ1_HFIRE	IKJ1_PWFIRE
IO_L2N_T0_34	J6	IKJ0_DOUT	IKJ1_HFIRE
IO_L2P_T0_34	J7	IKJ1_DCLK	IKJ0_DOUT
IO_L3N_T0_DQS_34	L7		IKJ1_DCLK
IO_L3P_T0_DQS_PUDC_B_34	K7	IKJ1_DLOAD	
IO_L4N_T0_34	M6	IKJ2_DCLK	IKJ1_DLOAD
IO_L4P_T0_34	L6	IKJ1_HCLK	IKJ2_DCLK
IO_L5N_T0_34	P8		IKJ1_HCLK
IO_L5P_T0_34	N8		
IO_L6N_T0_VREF_34	M7		
IO_L6P_T0_34	M8		
IO_L7N_T1_34	K5	IKJ0_DLOAD	
IO_L7P_T1_34	J5	IKJ0_HCLK	IKJ0_DLOAD
IO_L8N_T1_34	J1	IKJ0_DCLK	IKJ0_HCLK
IO_L8P_T1_34	J2	IKJ0_DIN2	IKJ0_DCLK
IO_L9N_T1_DQS_34	K2	IKJ1_DOUT	IKJ0_DIN2
IO_L9P_T1_DQS_34	J3	IKJ0_DIN1	IKJ1_DOUT
			IKJ0_DIN1

XC7Z015-1CLG485C

clk1_tst_N → J45
clk1_tst_P → J46
tst_0 → J47

place Test Points on Top, nearest to XC7Z016

tst_1 → J48
tst_2 → J49
tst_3 → J51
tst_4 → J53

U44-11

BANK 112

MGTPRXN0_112	AB7	SoC_SMA_MTG_RX0_N	SoC_SMA_MTG_RX0_N
MGTPRXN1_112	Y8	SoC_SMA_MTG_RX1_N	SoC_SMA_MTG_RX1_N
MGTPRXN2_112	AB9		
MGTPRXN3_112	Y6		
MGTPRXP0_112	AA7	SoC_SMA_MTG_RX0_P	SoC_SMA_MTG_RX0_P
MGTPRXP1_112	W8	SoC_SMA_MTG_RX1_P	SoC_SMA_MTG_RX1_P
MGTPRXP2_112	AA9		
MGTPRXP3_112	W6		
MGTPTXN0_112	AB3	SoC_SMA_MTG_TX0_N	SoC_SMA_MTG_TX0_N
MGTPTXN1_112	Y4	SoC_SMA_MTG_TX1_N	SoC_SMA_MTG_TX1_N
MGTPTXN2_112	AB5		
MGTPTXN3_112	Y2		
MGTPTXP0_112	AA3	SoC_SMA_MTG_TX0_P	SoC_SMA_MTG_TX0_P
MGTPTXP1_112	W4	SoC_SMA_MTG_TX1_P	SoC_SMA_MTG_TX1_P
MGTPTXP2_112	AA5		
MGTPTXP3_112	W2		
MGTREFCLK0N_112	V9	MGT_156_CLK_N	MGT_156_CLK_N
MGTREFCLK0P_112	U9	MGT_156_CLK_P	MGT_156_CLK_P
MGTREFCLK1N_112	V5		
MGTREFCLK1P_112	U5	R808 100 1%	
MGTREFCLK1P_112	U7		
MGTRREF_112			

XC7Z015-1CLG485C

place 100 Ohm resistor on Top near XC7Z015

R505 100 1%

SoC_1V2

the same of MGTAVTT

SoC_200_CLK_N → J50
SoC_200_CLK_P → J52
SoC_156_CLK_N → J71
SoC_156_CLK_P → J72

place Clock Test Points on Top, avoiding stubs, nearest to XC7Z016

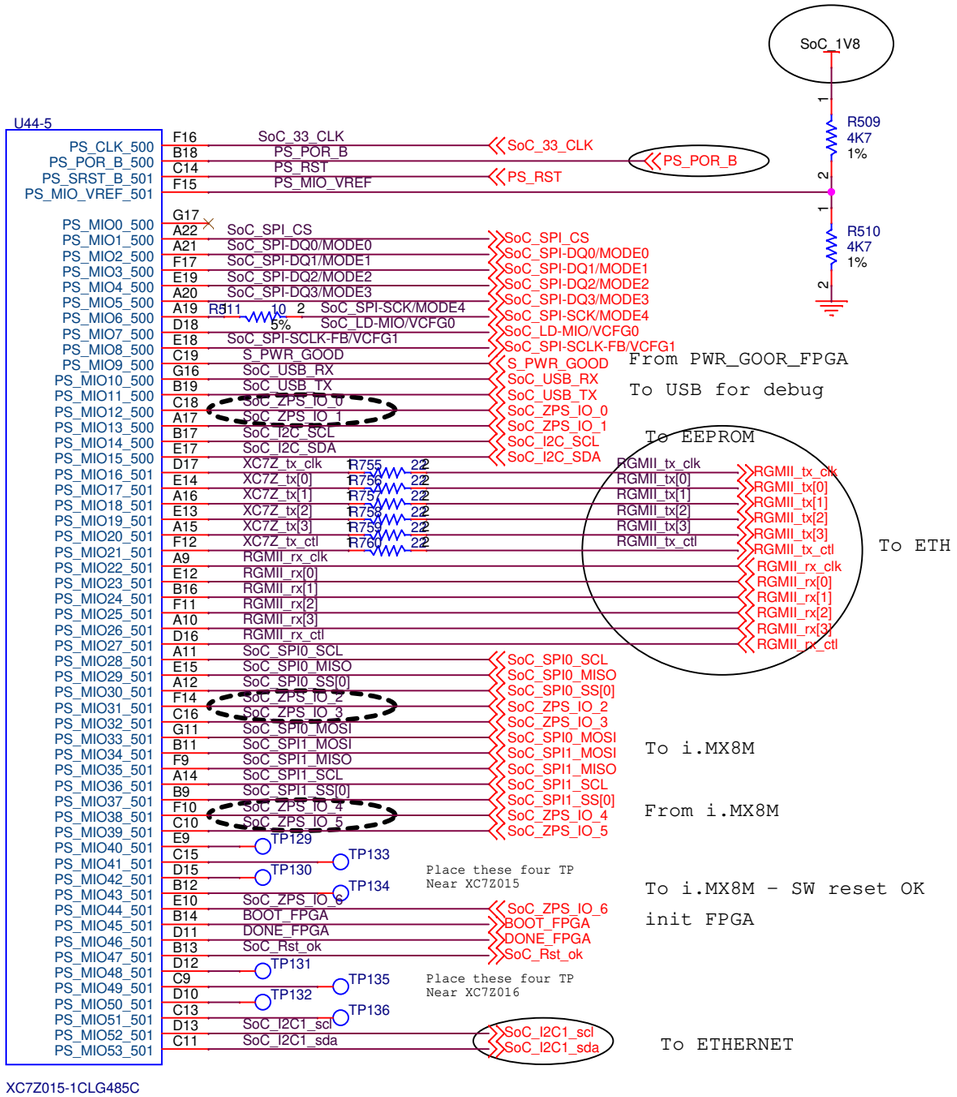
Title	Rototype - RLB		
Size A3	Document Number SoC - 02 - SoC - PL		Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47		

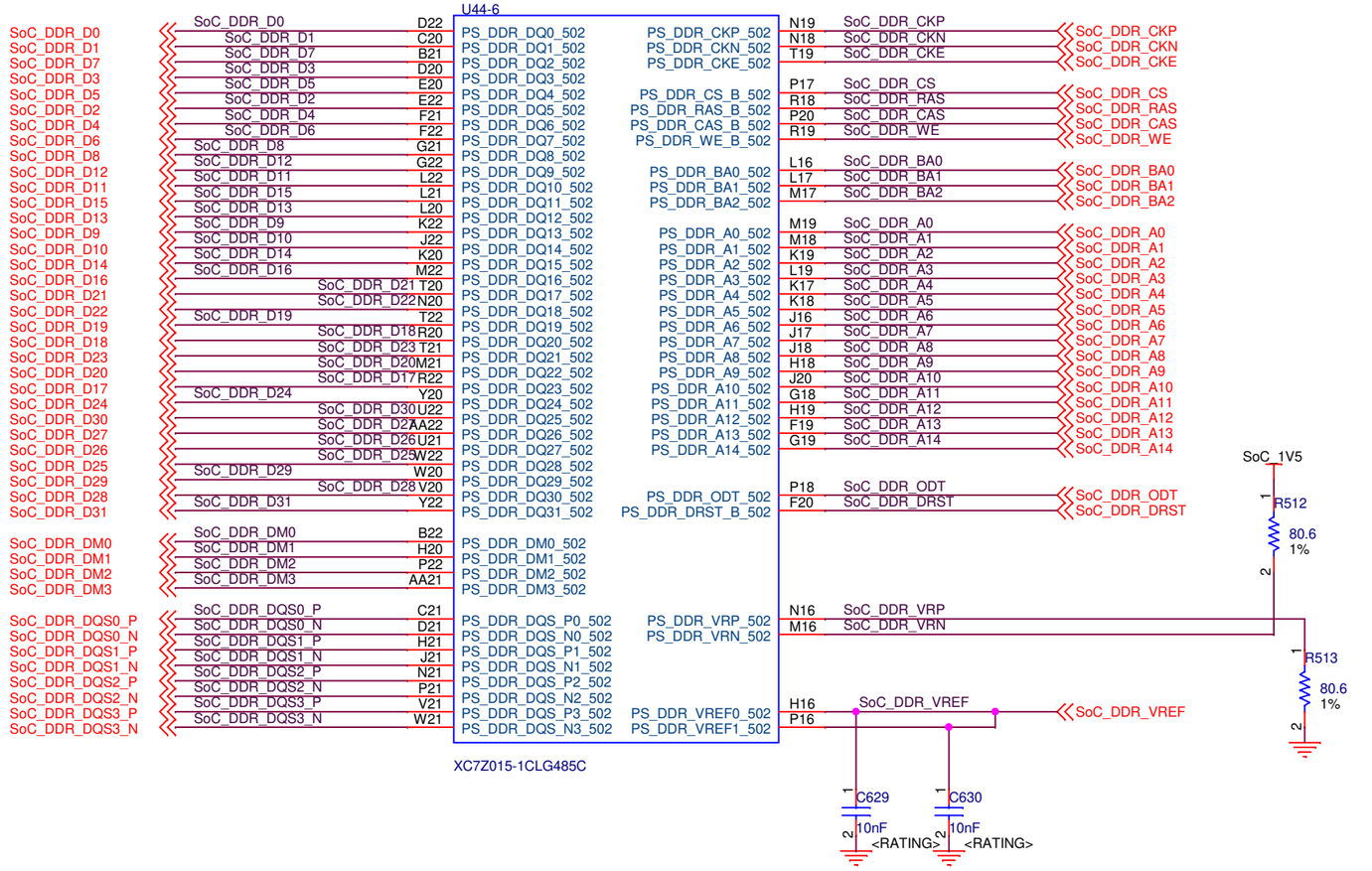
SoC - POWER

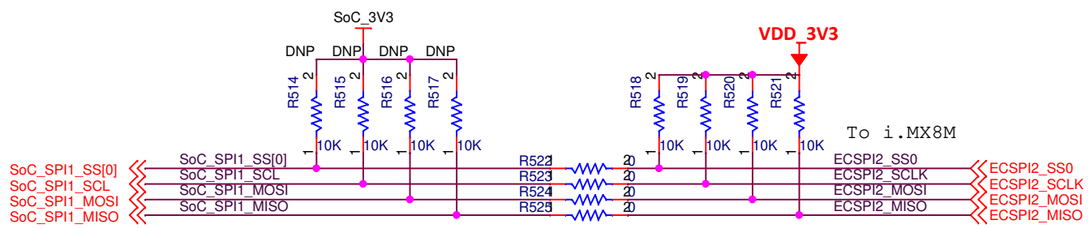
U44-2
XC7Z015-1CLG485C
U44-3
XC7Z015-1CLG485C
U44-1
XC7Z015-1CLG485C
U44-4
XC7Z015-1CLG485C
L31 LQW18ANR25J8ZD
L32 LQW18ANR25J8ZD
L33 BLM18PG121SN1D
C561 100nF <RATING>
R506 0 5%
C562 100nF <RATING>
C608 4.7uF <RATING>
C618 100nF <RATING>
C619 470nF <RATING>
C1055 470nF
C1056 470nF <RATING>
VCCPINT: C1034 C1035 C1036 C1037 C1038 — 100uF 4.7uF 470nF 470nF 470nF <RATING>
VCCPAUX: C1040 C1041 C1042 — 100uF 4.7uF 470nF <RATING>
VCCO_DDR: C1150 C1149 C1148 C1147 C1146 C1145 C1043 C1044 C1045 C1046 C1047 C1048 — 470nF 470nF 470nF 470nF 470nF 4.7uF 4.7uF 100uF 4.7uF 470nF 470nF 470nF 470nF <RATING>
VCCPLL: C1057 C1058 — 4.7uF 4.7uF <RATING>
VCCADC: C1059 C1060 — 4.7uF 4.7uF <RATING>
MGTAVCC: C1082 C1073 C1075 C1076 — 100uF 4.7uF 470nF 470nF <RATING>
MGTAVTT: C1083 C1078 C1080 C1081 — 100uF 4.7uF 470nF 470nF <RATING>
VCCO_MIO0: C1049 C1050 C1051 — 100uF 4.7uF 470nF <RATING>
VCCO_MIO1: C1052 C1053 C1054 — 100uF 4.7uF 470nF <RATING>
VCCBRAM: C1069 C1070 C1071 — 100uF 4.7uF 470nF <RATING>
VCCAUX: C1084 C1085 C1086 — 47uF 4.7uF 470nF <RATING>
VCCINT: C1063 C1062 C1064 C1065 C1066 C1067 C1068 — 330uF 4.7uF 4.7uF 470nF 470nF 470nF 470nF <RATING>
VCCO_13: C1087 C1088 C1089 C1090 C1091 C1092 C1093 — 100uF 4.7uF 4.7uF 470nF 470nF 470nF 470nF <RATING>
VCCO_34: C1094 C1095 C1096 C1097 C1098 C1099 C1100 — 100uF 4.7uF 4.7uF 470nF 470nF 470nF 470nF <RATING>
VCCO_35: C1101 C1102 C1103 C1104 C1105 C1106 C1107 — 100uF 4.7uF 4.7uF 470nF 470nF 470nF 470nF <RATING>

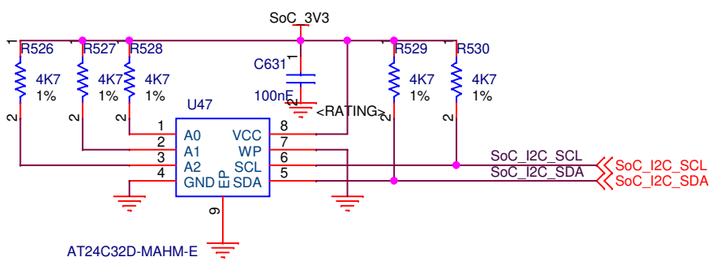
Title	Rototype - RLB	
Size A4	Document Number SoC - 02 - SoC - Power	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

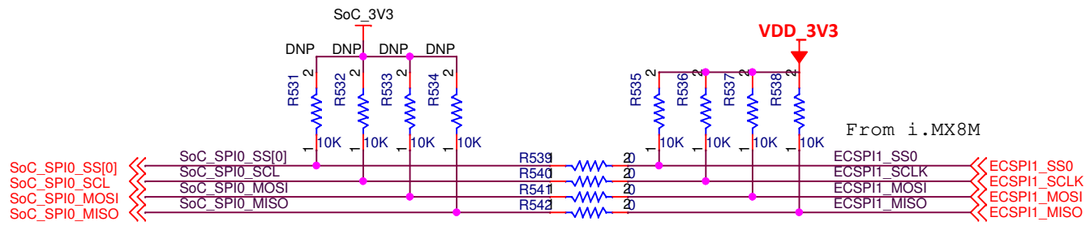
SoC - PS







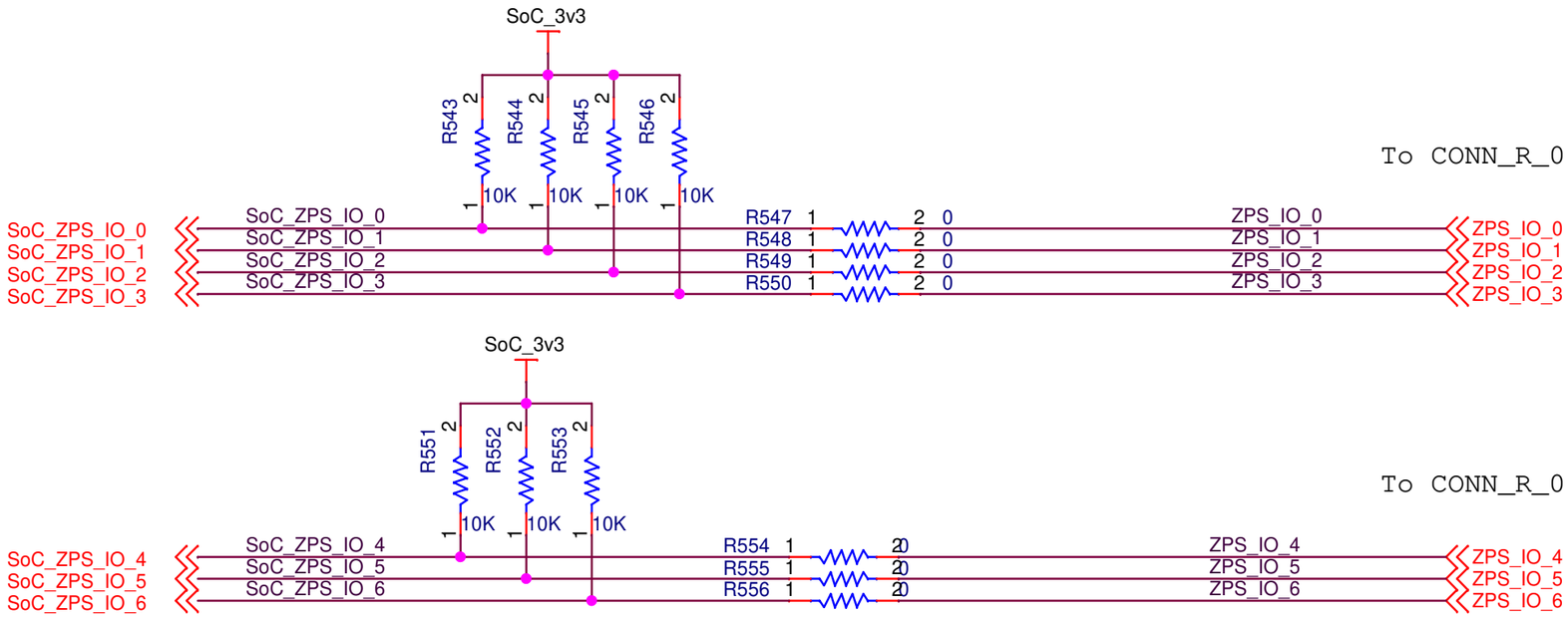




Note: the (XCZ_tx+ + RGMII_tx*) line lenghts (TX_RGMII) between XC7Z015 and KSZ9893R must be closely matched to each other Place 22 ohm resistors near XC7Z015

Title	Rototype - RLB	
Size A3	Document Number SoC - 02 - SoC - PS	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

SoC - PS IO Spare



Title	Rototype - RLB	
Size A4	Document Number SoC - 02 - SoC - PS IO Spare	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

SoC - Regulator

Vin : 2.5V ... 5.5V

Vout1 : 3.3V @ 4A

Vout2 : 1.8V @ 2A

Vout1 : 1.0V @ 4A

Vout2 : 1.5V @ 2A

threshold 2V38

threshold 0V9

threshold 1V4

threshold 0V8

Power supply sequence

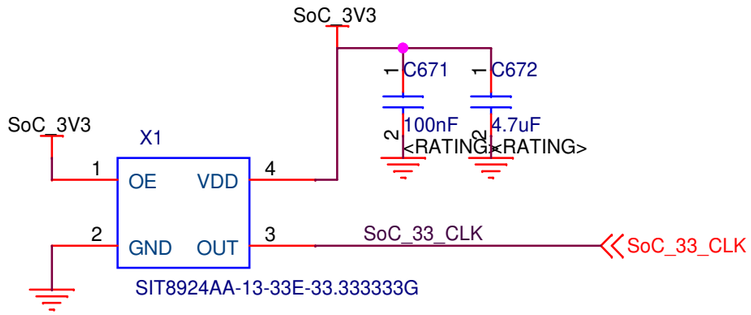
SoC_PG_5V0	R584 0	SoC_EN_1V0
SoC_PG_1V0	R586 0	SoC_EN_1V8
SoC_PG_1V8	R588 0	SoC_EN_1V5
	R589 0	SoC_EN_3V3

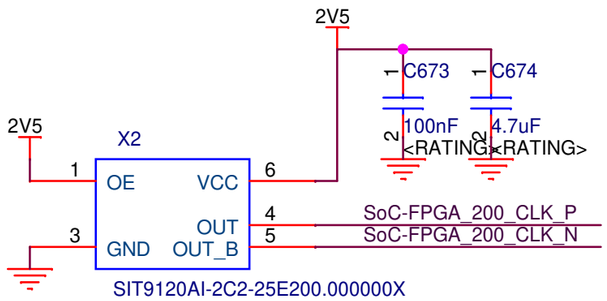
Title	Rototype - RLB		
Size A3	Document Number SoC - 02 - SoC - Regolatori		Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47		

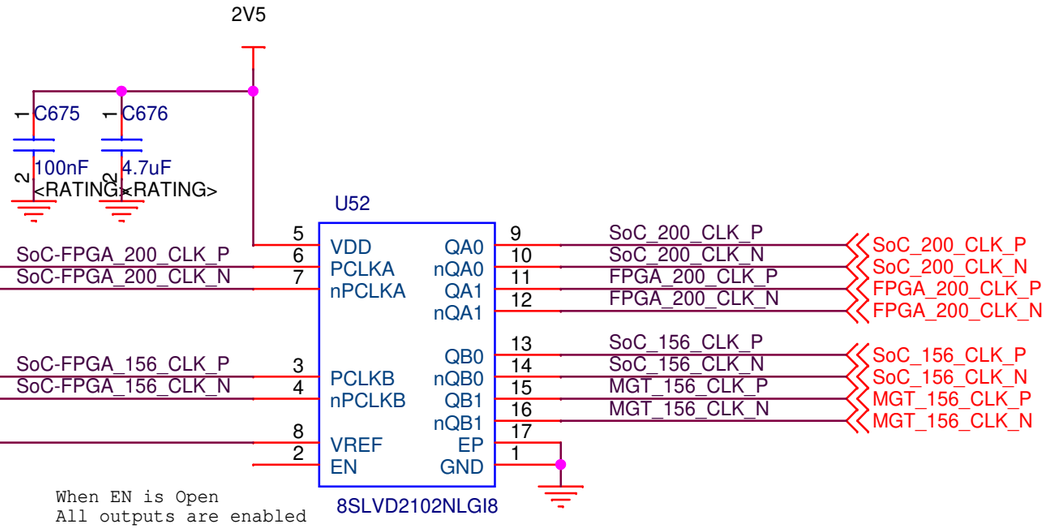
this page is intentionally blank

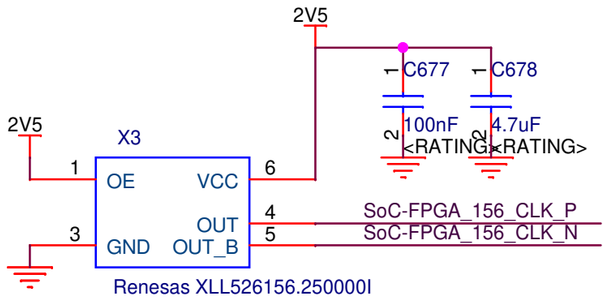
Title	Rototype - RLB	
Size: A4	Document Number: SoC - FPGA - 03 - SoC-FPGA - C2C termination	Rev: 1.0
Date: Thursday, November 26, 2020	Sheet 0 of 47	

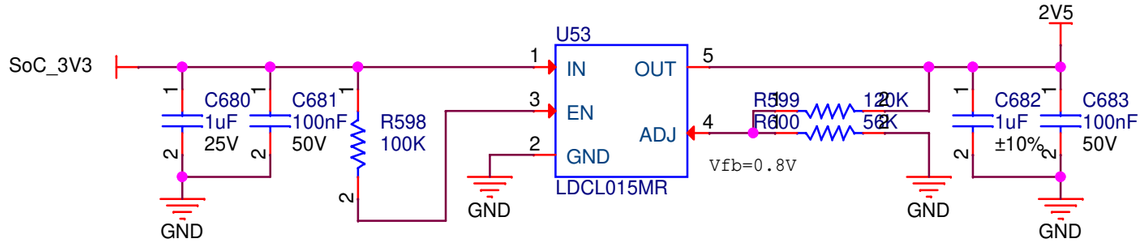
FPGA - SoC - CLK











Title: Rototype - RLB		
Size: A4	Document Number: SoC - FPGA - 03 - SoC-FPGA - CLK	Rev: 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

U54-6

BANK 14

IO_L24P_T3_D17_14	Y21 SM10_ENA	SM10_ENA
IO_L24N_T3_D16_14	Y22 SM10_M2P	SM10_M2P
IO_L23P_T3_D19_14	AA22 SM11_M2P	SM11_M2P
IO_L23N_T3_D18_14	AA23 SM11_M1P	SM11_M1P
IO_L22P_T3_D21_14	AA24 SM11_REF	SM11_REF
IO_L22N_T3_D20_14	AA25 SM11_DIR	SM11_DIR
IO_L21P_T3_DQS_14	W23 SM9_M2P	SM9_M2P
IO_L21N_T3_DQS_D22_14	Y23 SM10_M1P	SM10_M1P
IO_L20P_T3_D24_14	Y25 SM10_REF	SM10_REF
IO_L20N_T3_D23_14	Y26 SM10_DIR	SM10_DIR
IO_L19P_T3_D26_14	W25 SM9_REF	SM9_REF
IO_L19N_T3_D25_VREF_14	W26 SM9_DIR	SM9_DIR
IO_L18P_T2_D28_14	V23 SM8_M2P	SM8_M2P
IO_L18N_T2_D27_14	W24 SM9_M1P	SM9_M1P
IO_L17P_T2_D30_14	V21 SM8_CLK	SM8_CLK
IO_L17N_T2_D29_14	V22 SM8_ENA	SM8_ENA
IO_L16P_T2_CSI_B_14	W20 SM9_CLK	SM9_CLK
IO_L16N_T2_D31_14	W21 SM9_ENA	SM9_ENA
IO_L15P_T2_DQS_RDWR_B_14	U24 SM7_M2P	SM7_M2P
IO_L15N_T2_DQS_DOUT_CSO_B_14	V24 SM8_M1P	SM8_M1P
IO_L14P_T2_SRCC_14	T22 SM6_CLK	SM6_CLK
IO_L14N_T2_SRCC_14	U22 SM7_ENA	SM7_ENA
IO_L13P_T2_MRCC_14	U20 SM8_DIR	SM8_DIR
IO_L13N_T2_MRCC_14	U21 SM7_CLK	SM7_CLK
IO_L12P_T1_MRCC_14	T23 SM6_ENA	SM6_ENA
IO_L12N_T1_MRCC_14	T24 SM6_M2P	SM6_M2P
IO_L11P_T1_SRCC_14	U25 SM7_M1P	SM7_M1P
IO_L11N_T1_SRCC_14	V26 SM8_REF	SM8_REF
IO_L10P_T1_D14_14	T25 SM6_M1P	SM6_M1P
IO_L10N_T1_D15_14	U26 SM7_REF	SM7_REF
IO_L9P_T1_DQS_14	P25 SM5_DIR	SM5_DIR
IO_L9N_T1_DQS_D13_14	R26 SM5_ENA	SM5_ENA
IO_L8P_T1_D11_14	P24 SM5_REF	SM5_REF
IO_L8N_T1_D12_14	R25 SM5_CLK	SM5_CLK
IO_L7P_T1_D09_14	N26 SM4_M1P	SM4_M1P
IO_L7N_T1_D10_14	P26 SM4_CLK	SM4_CLK
IO_L6P_T0_FCS_B_14	R20 FPGA_SPI_CS	FPGA_SPI_CS
IO_L6N_T0_D08_VREF_14	T20 SM7_DIR	SM7_DIR
IO_L5P_T0_D06_14	P20 SM5_M2P	SM5_M2P
IO_L5N_T0_D07_14	P21 SM5_M1P	SM5_M1P
IO_L4P_T0_D04_14	R21 SM6_REF	SM6_REF
IO_L4N_T0_D05_14	R22 SM6_DIR	SM6_DIR
IO_L3P_T0_DQS_PUDC_B_14	N21 SM4_ENA	SM4_ENA
IO_L3N_T0_DQS_EMCCLK_14	N22 SM4_M2P	SM4_M2P
IO_L2P_T0_D02_14	P23 FPGA_SPI-DQ2	FPGA_SPI-DQ2
IO_L2N_T0_D03_14	R23 FPGA_SPI-DQ3	FPGA_SPI-DQ3
IO_L1P_T0_D00_MOSI_14	N23 FPGA_SPI-DQ0	FPGA_SPI-DQ0
IO_L1N_T0_D01_DIN_14	N24 FPGA_SPI-DQ1	FPGA_SPI-DQ1
IO_25_14	Y20 SM10_CLK	SM10_CLK
IO_0_14	M26 SM4_REF	SM4_REF

XC7S100-1FGGA676C

U54-5

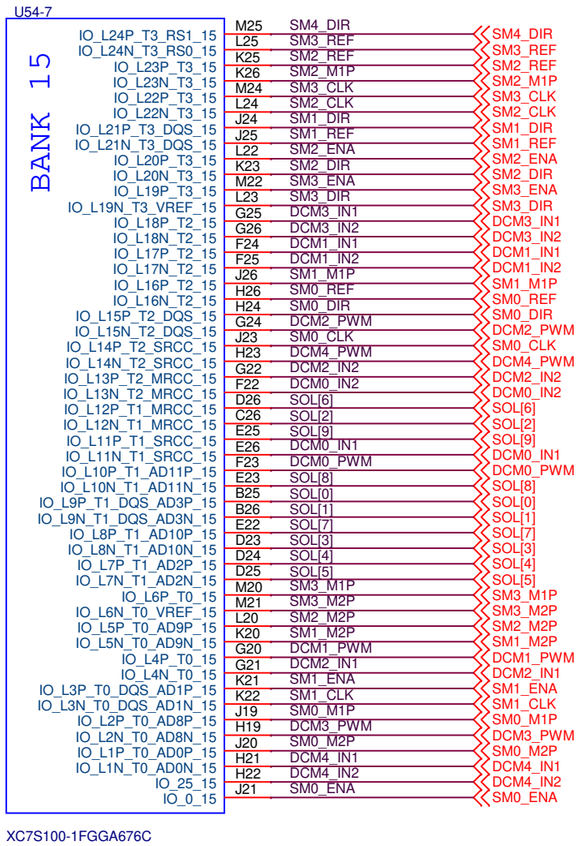
BANK 13

IO_L24P_T3_13	AE15 SM19_ENA	SM19_ENA
IO_L24N_T3_13	AF15 SM19_CLK	SM19_CLK
IO_L23P_T3_13	AD15 SM19_M2P	SM19_M2P
IO_L23N_T3_13	AE16 SM19_M1P	SM19_M1P
IO_L22P_T3_13	AA17 SM18_REF	SM18_REF
IO_L22N_T3_13	AA18 SM17_M1P	SM17_M1P
IO_L21P_T3_DQS_13	AC16 SM19_DIR	SM19_DIR
IO_L21N_T3_DQS_13	AD16 SM19_REF	SM19_REF
IO_L20P_T3_13	AF17 SM18_CLK	SM18_CLK
IO_L20N_T3_13	AF18 SM18_DIR	SM18_DIR
IO_L19P_T3_13	AB17 SM18_M1P	SM18_M1P
IO_L19N_T3_VREF_13	AC17 SM18_M2P	SM18_M2P
IO_L18P_T2_13	AC18 SM17_M2P	SM17_M2P
IO_L18N_T2_13	AD18 SM17_ENA	SM17_ENA
IO_L17P_T2_13	AD20 SM16_DIR	SM16_DIR
IO_L17N_T2_13	AE21 SM15_M2P	SM15_M2P
IO_L16P_T2_13	AC19 SM16_CLK	SM16_CLK
IO_L16N_T2_13	AD19 SM17_DIR	SM17_DIR
IO_L15P_T2_DQS_13	AE18 SM17_CLK	SM17_CLK
IO_L15N_T2_DQS_13	AF19 SM17_REF	SM17_REF
IO_L14P_T2_SRCC_13	AE20 SM16_REF	SM16_REF
IO_L14N_T2_SRCC_13	AF20 SM16_M1P	SM16_M1P
IO_L13P_T2_MRCC_13	AA19 SM16_M2P	SM16_M2P
IO_L13N_T2_MRCC_13	AB19 SM16_ENA	SM16_ENA
IO_L12P_T1_MRCC_13	AD21 SM15_M1P	SM15_M1P
IO_L12N_T1_MRCC_13	AE22 SM14_ENA	SM14_ENA
IO_L11P_T1_SRCC_13	AB21 SM15_DIR	SM15_DIR
IO_L11N_T1_SRCC_13	AC21 SM15_REF	SM15_REF
IO_L10P_T1_13	AB22 SM14_M1P	SM14_M1P
IO_L10N_T1_13	AC22 SM14_M2P	SM14_M2P
IO_L9P_T1_DQS_13	AA20 SM15_ENA	SM15_ENA
IO_L9N_T1_DQS_13	AB20 SM15_CLK	SM15_CLK
IO_L8P_T1_13	AF22 SM14_CLK	SM14_CLK
IO_L8N_T1_13	AF23 SM14_REF	SM14_REF
IO_L7P_T1_13	AD23 SM13_CLK	SM13_CLK
IO_L7N_T1_13	AE23 SM14_DIR	SM14_DIR
IO_L6P_T0_13	AE25 SM12_ENA	SM12_ENA
IO_L6N_T0_VREF_13	AF25 SM12_CLK	SM12_CLK
IO_L5P_T0_13	AC23 SM13_ENA	SM13_ENA
IO_L5N_T0_13	AC24 SM13_REF	SM13_REF
IO_L4P_T0_13	AD24 SM13_M1P	SM13_M1P
IO_L4N_T0_13	AD25 SM12_M2P	SM12_M2P
IO_L3P_T0_DQS_13	AD26 SM12_DIR	SM12_DIR
IO_L3N_T0_DQS_13	AE26 SM12_REF	SM12_REF
IO_L2P_T0_13	AB24 SM13_DIR	SM13_DIR
IO_L2N_T0_13	AB25 SM12_M1P	SM12_M1P
IO_L1P_T0_13	AB26 SM11_ENA	SM11_ENA
IO_L1N_T0_13	AC26 SM11_CLK	SM11_CLK
IO_25_13	AE17 SM18_ENA	SM18_ENA
IO_0_13	AF24 SM13_M2P	SM13_M2P

XC7S100-1FGGA676C

FPGA - BANK 13 - 14 - Stepper motor

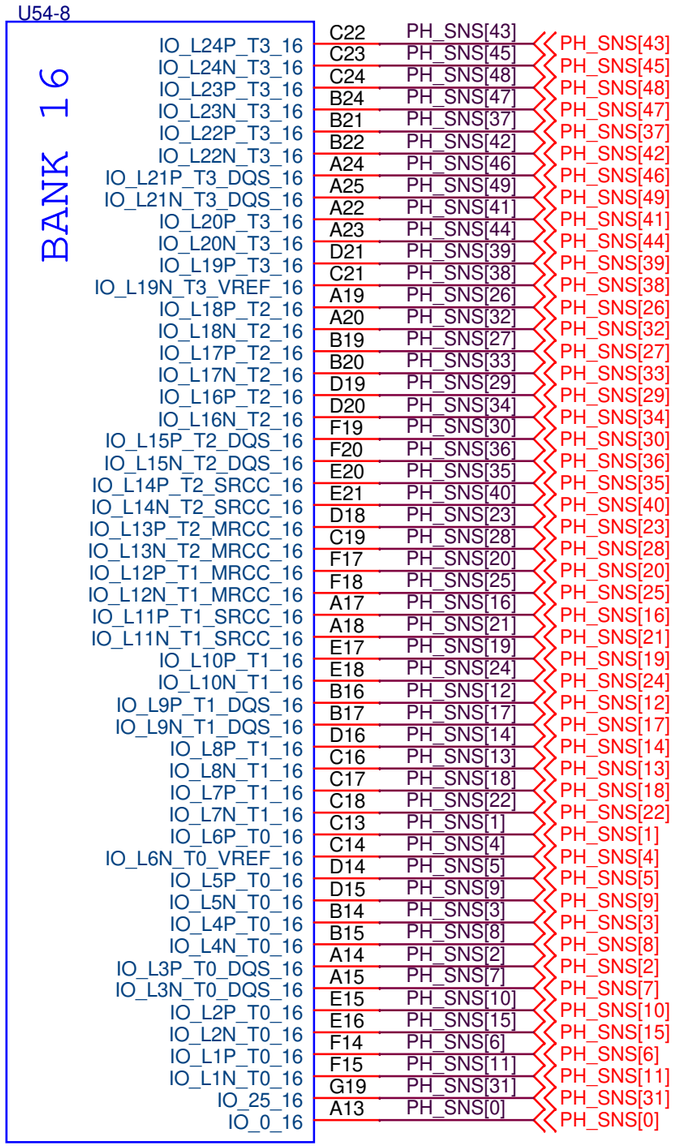
Title: Rototype - RLB		
Size: A3	Document Number: FPGA - 04 - FPGA - BANK 13 - 14	Rev: 1.0
Date: Thursday, November 26, 2020	Sheet 0 of 47	



FPGA - BANK 15 - stepper motor

Title: Rototype - RLB		
Size: A3	Document Number: FPGA - 04 - FPGA - BANK 15	Rev: 1.0
Date: Thursday, November 26, 2020	Sheet 0 of 47	

FPGA - BANK 16
read photo transistor



Title	Rototype - RLB	
Size A4	Document Number FPGA - 04 - FPGA - BANK 16	Rev 1.0
Date: Thursday, November 26, 2020	Sheet 0 of 47	

FPGA - BANK 33/34 (CIS) - 35(C2C)

U54-10

BANK 34

IO_L24P_T3_34	Y7	CIS1_LED_B_P
IO_L24N_T3_34	AA7	CIS1_LED_B_N
IO_L23P_T3_34	AA4	CIS1_LED_R_P
IO_L23N_T3_34	AA3	CIS1_LED_R_N
IO_L22P_T3_34	AB5	CIS1_LVDS_D0_P
IO_L22N_T3_34	AB4	CIS1_LVDS_D0_N
IO_L21P_T3_DQS_34	W6	CIS1_CS1
IO_L21N_T3_DQS_34	Y6	CIS1_CS2
IO_L20P_T3_34	Y5	CIS1_LED_G_P
IO_L20N_T3_34	AA5	CIS1_LED_G_N
IO_L19P_T3_34	W5	CIS0_LVDS_D2_P
IO_L19N_T3_VREF_34	W4	CIS0_LVDS_D2_N
IO_L18P_T2_34	V4	CIS0_LVDS_D1_P
IO_L18N_T2_34	W3	CIS0_LVDS_D1_N
IO_L17P_T2_34	T3	CIS0_LED_B_P
IO_L17N_T2_34	U2	CIS0_LED_B_N
IO_L16P_T2_34	V7	CIS0_LVDS_D0_P
IO_L16N_T2_34	V6	CIS0_LVDS_D0_N
IO_L15P_T2_DQS_34	T4	CIS0_SI_P
IO_L15N_T2_DQS_34	U4	CIS0_SI_N
IO_L14P_T2_SRCC_34	U6	CIS0_CLK_P
IO_L14N_T2_SRCC_34	U5	CIS0_CLK_N
IO_L13P_T2_MRCC_34	T7	CIS0_LVDS_CLK_P
IO_L13N_T2_MRCC_34	U7	CIS0_LVDS_CLK_N
IO_L12P_T1_MRCC_34	V3	CIS1_LVDS_CLK_P
IO_L12N_T1_MRCC_34	V2	CIS1_LVDS_CLK_N
IO_L11P_T1_SRCC_34	U1	CIS1_CLK_P
IO_L11N_T1_SRCC_34	V1	CIS1_CLK_N
IO_L10P_T1_34	W1	CIS1_MOSI
IO_L10N_T1_34	Y1	CIS1_MISO
IO_L9P_T1_DQS_34	AA2	CIS1_SI_P
IO_L9N_T1_DQS_34	AB1	CIS1_SI_N
IO_L8P_T1_34	Y3	CIS1_CS0
IO_L8N_T1_34	Y2	CIS1_SCKL
IO_L7P_T1_34	AB2	CIS1_LVDS_D1_P
IO_L7N_T1_34	AC1	CIS1_LVDS_D1_N
IO_L6P_T0_34	R7	CIS0_CS1
IO_L6N_T0_VREF_34	R6	CIS0_CS0
IO_L5P_T0_34	R5	CIS0_LED_G_P
IO_L5N_T0_34	T5	CIS0_LED_G_N
IO_L4P_T0_34	R2	CIS0_LED_R_P
IO_L4N_T0_34	T2	CIS0_LED_R_N
IO_L3P_T0_DQS_34	P5	S_IO_2
IO_L3N_T0_DQS_34	P4	S_IO_1
IO_L2P_T0_34	P1	S_IO_0
IO_L2N_T0_34	R1	S_IO_3
IO_L1P_T0_34	P3	CIS0_MISO
IO_L1N_T0_34	R3	CIS0_SCKL
IO_25_34	Y8	CIS0_CS2
IO_0_34	P6	CIS0_MOSI

XC7S100-1FGGA676C

U54-9

BANK 33

IO_L24P_T3_33	AD14	CIS3_LVDS_D1_P
IO_L24N_T3_33	AD13	CIS3_LVDS_D1_N
IO_L23P_T3_33	AB11	CIS3_LED_G_P
IO_L23N_T3_33	AC11	CIS3_LED_G_N
IO_L22P_T3_33	AF14	CIS3_LVDS_D2_P
IO_L22N_T3_33	AF13	CIS3_LVDS_D2_N
IO_L21P_T3_DQS_33	AE11	CIS3_LED_B_P
IO_L21N_T3_DQS_33	AE10	CIS3_LED_B_N
IO_L20P_T3_33	AE12	CIS3_LVDS_D0_P
IO_L20N_T3_33	AF12	CIS3_LVDS_D0_N
IO_L19P_T3_33	AC12	CIS3_SI_P
IO_L19N_T3_VREF_33	AD11	CIS3_SI_N
IO_L18P_T2_33	AA9	CIS2_LVDS_D2_P
IO_L18N_T2_33	AB9	CIS2_LVDS_D2_N
IO_L17P_T2_33	AF10	CIS3_LED_R_P
IO_L17N_T2_33	AF9	CIS3_LED_R_N
IO_L16P_T2_33	AD10	CIS3_CS1
IO_L16N_T2_33	AD9	CIS3_CS0
IO_L15P_T2_DQS_33	AC9	CIS3_SCKL
IO_L15N_T2_DQS_33	AD8	CIS3_MISO
IO_L14P_T2_SRCC_33	AF8	CIS3_CLK_P
IO_L14N_T2_SRCC_33	AF7	CIS3_CLK_N
IO_L13P_T2_MRCC_33	AA10	CIS3_LVDS_CLK_P
IO_L13N_T2_MRCC_33	AB10	CIS3_LVDS_CLK_N
IO_L12P_T1_MRCC_33	AE8	CIS2_CLK_P
IO_L12N_T1_MRCC_33	AE7	CIS2_CLK_N
IO_L11P_T1_SRCC_33	AC8	CIS2_LVDS_CLK_P
IO_L11N_T1_SRCC_33	AC7	CIS2_LVDS_CLK_N
IO_L10P_T1_33	AB6	CIS2_LED_B_P
IO_L10N_T1_33	AC6	CIS2_LED_B_N
IO_L9P_T1_DQS_33	AA8	CIS2_LVDS_D1_P
IO_L9N_T1_DQS_33	AB7	CIS2_LVDS_D1_N
IO_L8P_T1_33	AD6	CIS2_SI_P
IO_L8N_T1_33	AD5	CIS2_SI_N
IO_L7P_T1_33	AE6	CIS2_LVDS_D0_P
IO_L7N_T1_33	AE5	CIS2_LVDS_D0_N
IO_L6P_T0_33	AD3	CIS2_CS0
IO_L6N_T0_VREF_33	AE3	CIS2_SCKL
IO_L5P_T0_33	AC4	CIS2_LED_R_P
IO_L5N_T0_33	AD4	CIS2_LED_R_N
IO_L4P_T0_33	AF5	CIS2_LED_G_P
IO_L4N_T0_33	AF4	CIS2_LED_G_N
IO_L3P_T0_DQS_33	AF3	CIS2_CS2
IO_L3N_T0_DQS_33	AF2	CIS2_CS1
IO_L2P_T0_33	AC3	CIS2_MISO
IO_L2N_T0_33	AC2	CIS2_MOSI
IO_L1P_T0_33	AD1	CIS1_LVDS_D2_P
IO_L1N_T0_33	AE1	CIS1_LVDS_D2_N
IO_25_33	AE13	CIS3_CS2
IO_0_33	AE2	CIS3_MOSI

XC7S100-1FGGA676C

U54-11

BANK 35

IO_L24P_T3_35	M2	C2C_RX_DATA9
IO_L24N_T3_35	M1	C2C_RX_DATA10
IO_L23P_T3_35	K1	C2C_RX_DATA1
IO_L23N_T3_35	J1	C2C_X2M_IRQ_OUT0
IO_L22P_T3_35	N2	C2C_RX_DATA14
IO_L22N_T3_35	N1	FPGA_USB_RX
IO_L21P_T3_DQS_35	L2	C2C_RX_DATA5
IO_L21N_T3_DQS_35	K2	C2C_RX_DATA0
IO_L20P_T3_35	K3	C2C_X2M_IRQ_OUT3
IO_L20N_T3_35	J3	C2C_TX_DATA14
IO_L19P_T3_35	N4	C2C_RX_DATA12
IO_L19N_T3_VREF_35	N3	C2C_RX_DATA13
IO_L18P_T2_35	L4	C2C_RX_DATA3
IO_L18N_T2_35	L3	C2C_RX_DATA4
IO_L17P_T2_35	M5	C2C_RX_DATA7
IO_L17N_T2_35	M4	C2C_RX_DATA8
IO_L16P_T2_35	N6	C2C_RX_DATA11
IO_L16N_T2_35	M6	C2C_RX_DATA6
IO_L15P_T2_DQS_35	L5	C2C_RX_DATA2
IO_L15N_T2_DQS_35	K5	C2C_X2M_IRQ_OUT2
IO_L14P_T2_SRCC_35	M7	R601 102 1% C2C_TX_CLK_P
IO_L14N_T2_SRCC_35	L7	R602 102 1% C2C_TX_CLK_N
IO_L13P_T2_MRCC_35	K7	FPGA_200_CLK_P
IO_L13N_T2_MRCC_35	K6	FPGA_200_CLK_N
IO_L12P_T1_MRCC_35	J4	FPGA_SPARE_CLK_P R809 100 1%
IO_L12N_T1_MRCC_35	H4	FPGA_SPARE_CLK_N
IO_L11P_T1_SRCC_35	H3	R603 102 1% C2C_RX_CLK_P
IO_L11N_T1_SRCC_35	H2	R604 102 1% C2C_RX_CLK_N
IO_L10P_T1_AD15P_35	E2	C2C_X2M_IRQ_IN0
IO_L10N_T1_AD15N_35	E1	C2C_X2M_IRQ_IN1
IO_L9P_T1_DQS_AD7P_35	H1	C2C_TX_DATA10
IO_L9N_T1_DQS_AD7N_35	G1	C2C_TX_DATA7
IO_L8P_T1_AD14P_35	F3	C2C_TX_DATA0
IO_L8N_T1_AD14N_35	E3	S_RST_FPGA_OK
IO_L7P_T1_AD6P_35	G2	C2C_TX_DATA6
IO_L7N_T1_AD6N_35	F2	C2C_TX_DATA1
IO_L6P_T0_35	H7	C2C_TX_DATA8
IO_L6N_T0_VREF_35	G7	C2C_TX_DATA2
IO_L5P_T0_AD13P_35	J6	C2C_TX_DATA12
IO_L5N_T0_AD13N_35	J5	C2C_TX_DATA13
IO_L4P_T0_35	H6	C2C_TX_DATA9
IO_L4N_T0_35	G6	C2C_TX_DATA3
IO_L3P_T0_DQS_AD5P_35	G4	C2C_TX_DATA5
IO_L3N_T0_DQS_AD5N_35	F4	C2C_X2M_IRQ_IN3
IO_L2P_T0_AD12P_35	K8	C2C_X2M_IRQ_OUT1
IO_L2N_T0_AD12N_35	J8	C2C_TX_DATA11
IO_L1P_T0_AD4P_35	G5	C2C_TX_DATA4
IO_L1N_T0_AD4N_35	F5	C2C_X2M_IRQ_IN2
IO_25_35	N7	FPGA_USB_TX
IO_0_35	H8	S_RST_FPGA

XC7S100-1FGGA676C

place 10 ohm resistors on Top near XC7S100

place FPGA_SPARE_CLK resistor on Top

Title	Rototype - RLB	
Size A3	Document Number FPGA - 04 - FPGA - BANK 33 - 34 - 35	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

U54-12

BANK 36

IO_L24P_T3_36	D4	F_PWM9
IO_L24N_T3_36	D3	F_PWM6
IO_L23P_T3_36	D1	F_PWM0
IO_L23N_T3_36	C1	F_PWM1
IO_L22P_T3_36	A3	F_PWM8
IO_L22N_T3_36	A2	F_PWM5
IO_L21P_T3_DQS_36	B2	F_PWM4
IO_L21N_T3_DQS_36	B1	F_PWM2
IO_L20P_T3_36	C4	F_PWM10
IO_L20N_T3_36	B4	F_PWM11
IO_L19P_T3_36	C3	F_PWM7
IO_L19N_T3_VREF_36	C2	F_PWM3
IO_L18P_T2_36	B5	F_PWM15
IO_L18N_T2_36	A5	F_PWM16
IO_L17P_T2_36	E5	F_PWM13
IO_L17N_T2_36	D5	F_PWM14
IO_L16P_T2_36	F7	F_PWM21
IO_L16N_T2_36	E7	F_PWM22
IO_L15P_T2_DQS_36	E6	F_PWM17
IO_L15N_T2_DQS_36	D6	F_PWM18
IO_L14P_T2_SRCC_36	B7	F_PWM24
IO_L14N_T2_SRCC_36	B6	F_PWM20
IO_L13P_T2_MRCC_36	C7	F_PWM23
IO_L13N_T2_MRCC_36	C6	F_PWM19
IO_L12P_T1_MRCC_36	D9	F_PWM32
IO_L12N_T1_MRCC_36	D8	F_PWM28
IO_L11P_T1_SRCC_36	A8	F_PWM30
IO_L11N_T1_SRCC_36	A7	F_PWM25
IO_L10P_T1_36	F10	F_PWM36
IO_L10N_T1_36	F9	F_PWM31
IO_L9P_T1_DQS_36	B9	F_PWM34
IO_L9N_T1_DQS_36	A9	F_PWM35
IO_L8P_T1_36	C9	F_PWM33
IO_L8N_T1_36	C8	F_PWM29
IO_L7P_T1_36	F8	F_PWM26
IO_L7N_T1_36	E8	F_PWM27
IO_L6P_T0_36	B12	F_PWM48
IO_L6N_T0_VREF_36	B11	F_PWM44
IO_L5P_T0_36	C12	F_PWM47
IO_L5N_T0_36	C11	F_PWM43
IO_L4P_T0_36	B10	F_PWM39
IO_L4N_T0_36	A10	F_PWM40
IO_L3P_T0_DQS_36	D11	F_PWM42
IO_L3N_T0_DQS_36	D10	F_PWM38
IO_L2P_T0_36	F12	F_PWM45
IO_L2N_T0_36	E12	F_PWM46
IO_L1P_T0_36	E11	F_PWM41
IO_L1N_T0_36	E10	F_PWM37
IO_25_36	A4	F_PWM12
IO_0_36	A12	F_PWM49

XC7S100-1FGGA676C

F_PWM0 R607 100K 1% PH_LD[0] C686 22nF <RATING> PH_LD[0]

F_PWM1 R611 100K 1% PH_LD[1] C690 22nF <RATING> PH_LD[1]

F_PWM2 R615 100K 1% PH_LD[2] C694 22nF <RATING> PH_LD[2]

F_PWM3 R619 100K 1% PH_LD[3] C698 22nF <RATING> PH_LD[3]

F_PWM4 R623 100K 1% PH_LD[4] C702 22nF <RATING> PH_LD[4]

F_PWM5 R627 100K 1% PH_LD[5] C706 22nF <RATING> PH_LD[5]

F_PWM6 R631 100K 1% PH_LD[6] C710 22nF <RATING> PH_LD[6]

F_PWM7 R635 100K 1% PH_LD[7] C714 22nF <RATING> PH_LD[7]

F_PWM8 R639 100K 1% PH_LD[8] C718 22nF <RATING> PH_LD[8]

F_PWM9 R643 100K 1% PH_LD[9] C722 22nF <RATING> PH_LD[9]

F_PWM10 R605 100K 1% PH_LD[10] C684 22nF <RATING> PH_LD[10]

F_PWM11 R609 100K 1% PH_LD[11] C688 22nF <RATING> PH_LD[11]

F_PWM12 R613 100K 1% PH_LD[12] C692 22nF <RATING> PH_LD[12]

F_PWM13 R617 100K 1% PH_LD[13] C696 22nF <RATING> PH_LD[13]

F_PWM14 R621 100K 1% PH_LD[14] C700 22nF <RATING> PH_LD[14]

F_PWM15 R625 100K 1% PH_LD[15] C704 22nF <RATING> PH_LD[15]

F_PWM16 R629 100K 1% PH_LD[16] C708 22nF <RATING> PH_LD[16]

F_PWM17 R633 100K 1% PH_LD[17] C712 22nF <RATING> PH_LD[17]

F_PWM18 R637 100K 1% PH_LD[18] C716 22nF <RATING> PH_LD[18]

F_PWM19 R641 100K 1% PH_LD[19] C720 22nF <RATING> PH_LD[19]

F_PWM20 R608 100K 1% PH_LD[20] C687 22nF <RATING> PH_LD[20]

F_PWM21 R612 100K 1% PH_LD[21] C691 22nF <RATING> PH_LD[21]

F_PWM22 R616 100K 1% PH_LD[22] C695 22nF <RATING> PH_LD[22]

F_PWM23 R620 100K 1% PH_LD[23] C699 22nF <RATING> PH_LD[23]

F_PWM24 R624 100K 1% PH_LD[24] C703 22nF <RATING> PH_LD[24]

F_PWM25 R628 100K 1% PH_LD[25] C707 22nF <RATING> PH_LD[25]

F_PWM26 R632 100K 1% PH_LD[26] C711 22nF <RATING> PH_LD[26]

F_PWM27 R636 100K 1% PH_LD[27] C715 22nF <RATING> PH_LD[27]

F_PWM28 R640 100K 1% PH_LD[28] C719 22nF <RATING> PH_LD[28]

F_PWM29 R644 100K 1% PH_LD[29] C723 22nF <RATING> PH_LD[29]

F_PWM30 R606 100K 1% PH_LD[30] C685 22nF <RATING> PH_LD[30]

F_PWM31 R610 100K 1% PH_LD[31] C689 22nF <RATING> PH_LD[31]

F_PWM32 R614 100K 1% PH_LD[32] C693 22nF <RATING> PH_LD[32]

F_PWM33 R618 100K 1% PH_LD[33] C697 22nF <RATING> PH_LD[33]

F_PWM34 R622 100K 1% PH_LD[34] C701 22nF <RATING> PH_LD[34]

F_PWM35 R626 100K 1% PH_LD[35] C705 22nF <RATING> PH_LD[35]

F_PWM36 R630 100K 1% PH_LD[36] C709 22nF <RATING> PH_LD[36]

F_PWM37 R634 100K 1% PH_LD[37] C713 22nF <RATING> PH_LD[37]

F_PWM38 R638 100K 1% PH_LD[38] C717 22nF <RATING> PH_LD[38]

F_PWM39 R642 100K 1% PH_LD[39] C721 22nF <RATING> PH_LD[39]

F_PWM40 R646 100K 1% PH_LD[40] C725 22nF <RATING> PH_LD[40]

F_PWM41 R648 100K 1% PH_LD[41] C727 22nF <RATING> PH_LD[41]

F_PWM42 R650 100K 1% PH_LD[42] C729 22nF <RATING> PH_LD[42]

F_PWM43 R652 100K 1% PH_LD[43] C731 22nF <RATING> PH_LD[43]

F_PWM44 R654 100K 1% PH_LD[44] C733 22nF <RATING> PH_LD[44]

F_PWM45 R645 100K 1% PH_LD[45] C724 22nF <RATING> PH_LD[45]

F_PWM46 R647 100K 1% PH_LD[46] C726 22nF <RATING> PH_LD[46]

F_PWM47 R649 100K 1% PH_LD[47] C728 22nF <RATING> PH_LD[47]

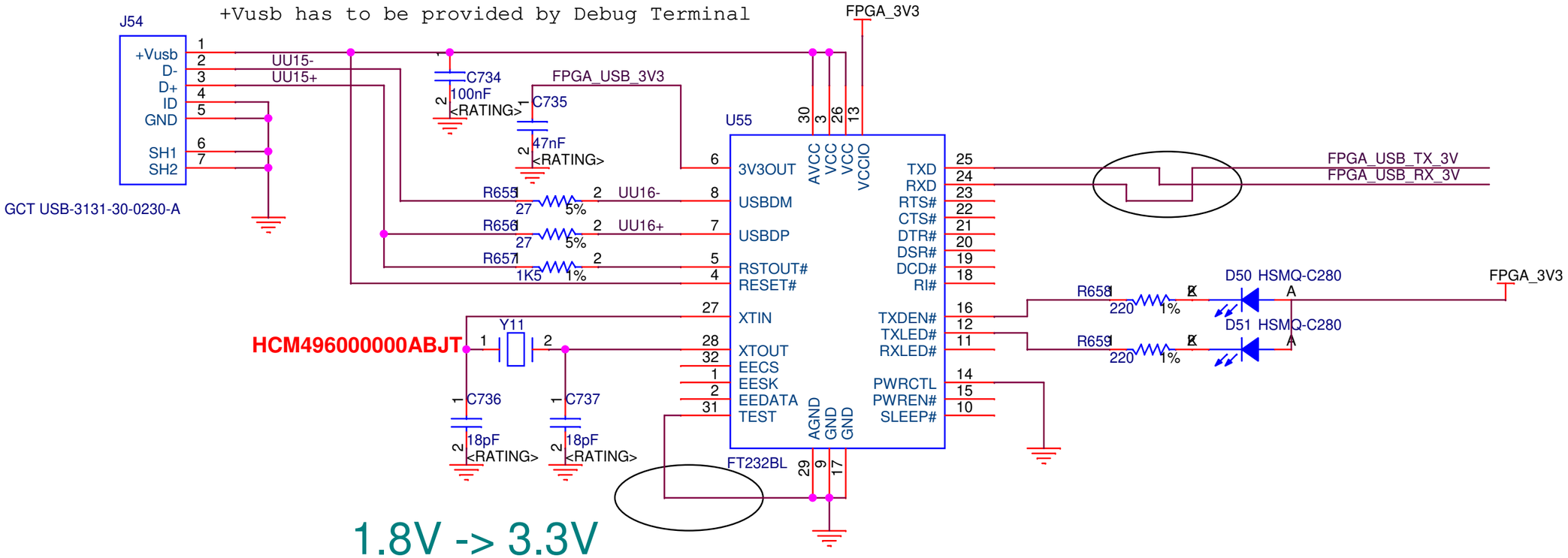
F_PWM48 R651 100K 1% PH_LD[48] C730 22nF <RATING> PH_LD[48]

F_PWM49 R653 100K 1% PH_LD[49] C732 22nF <RATING> PH_LD[49]

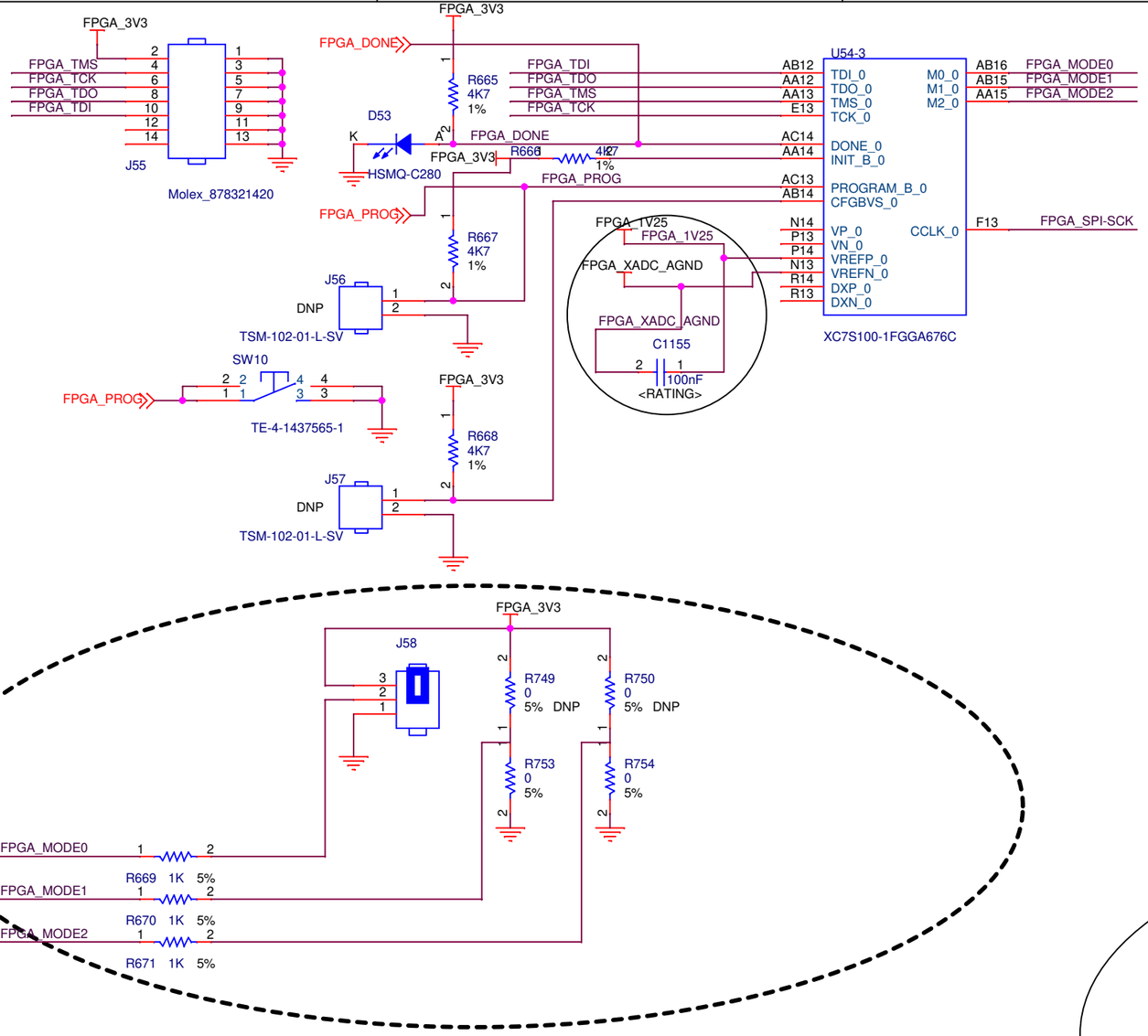
FPGA - BANK 36 - LED

Title	Rototype - RLB	
Size A4	Document Number FPGA - 04 - FPGA - BANK 36	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

FPGA - USB Debug



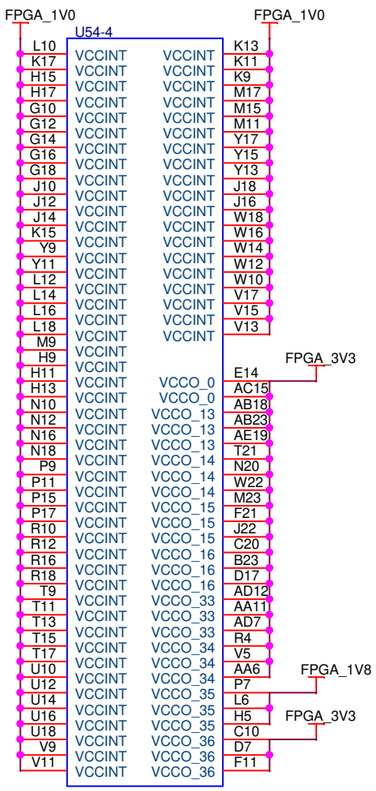
Title	Rototype - RLB	
Size A4	Document Number FPGA - 04 - FPGA - DBG UART	Rev 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

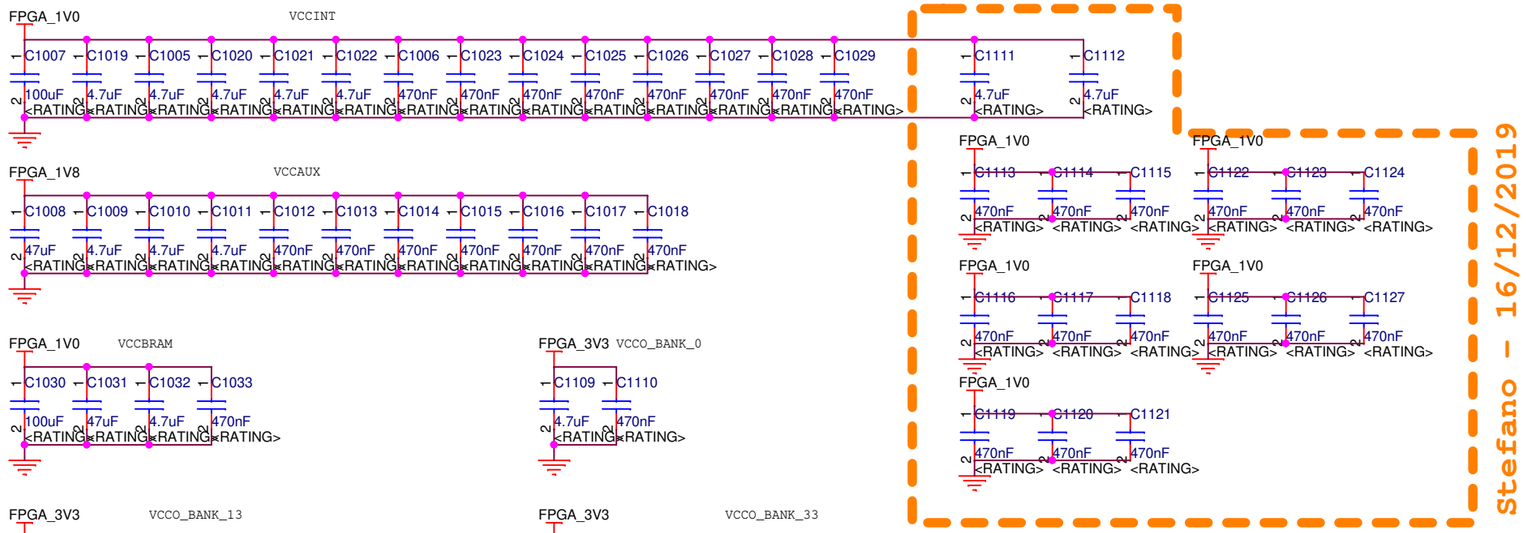


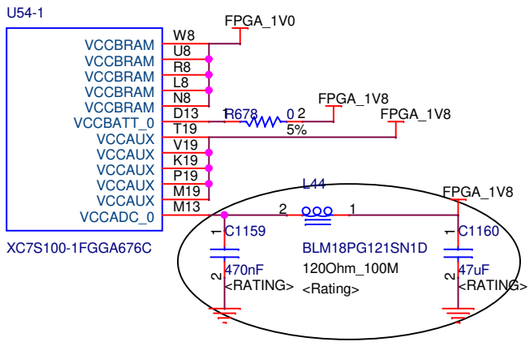
Pin Name	Bank	JTAG (Only)	Slave Serial	Master Serial	Master SPI		
					x1	x2	x4
CFGBVS	0	CFGBVS	CFGBVS	CFGBVS	CFGBVS	CFGBVS	CFGBVS
M[2:0]	0	M[2:0]=101	M[2:0]=111	M[2:0]=000	M[2:0]=001	M[2:0]=001	M[2:0]=001

FPGA - JTAG

Title: Rototype - RLB		
Size: A3	Document Number: FPGA - 04 - FPGA - JTAG	Rev: 1.0
Date: Wednesday, December 02, 2020	Sheet 0 of 47	

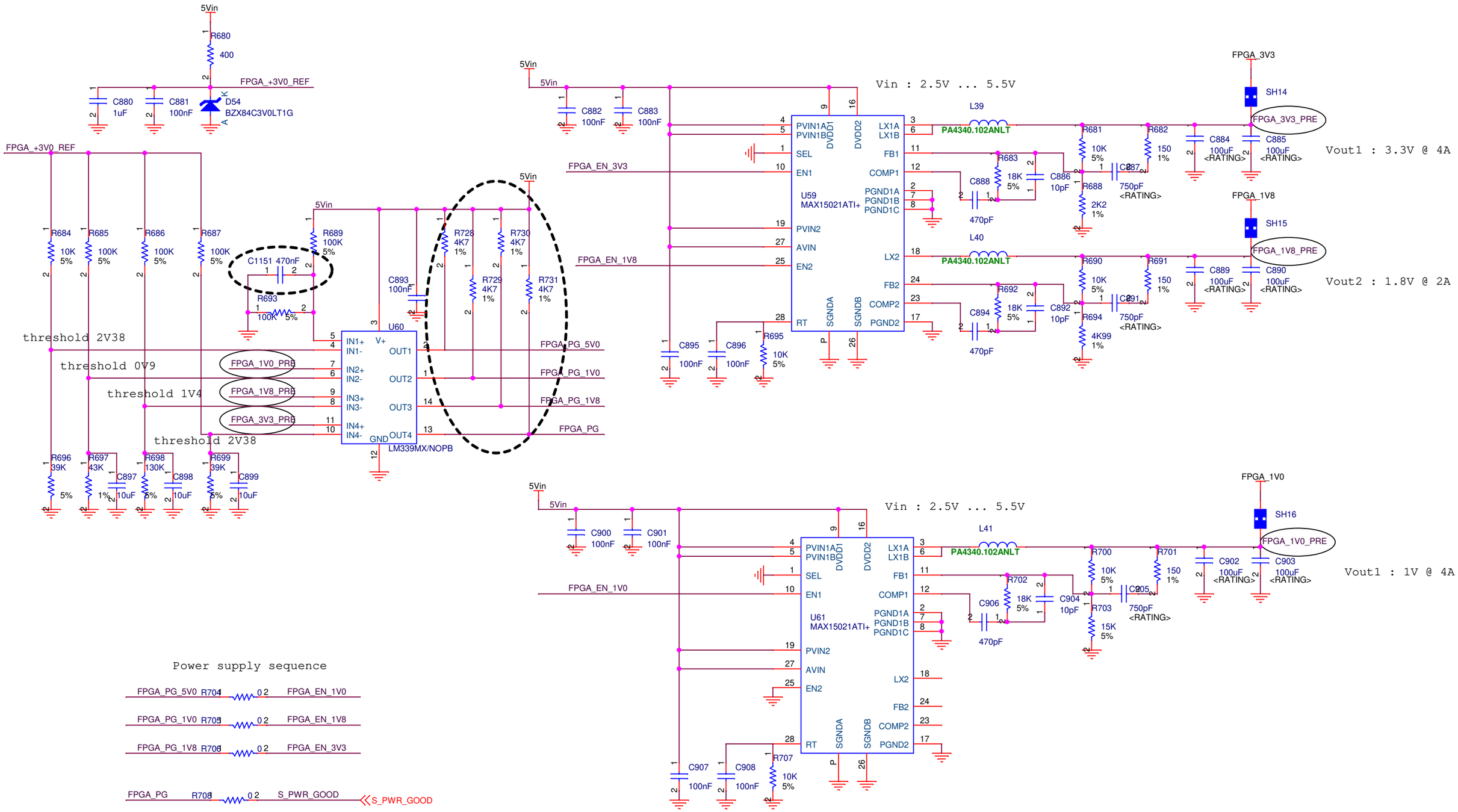






FPGA - POWER

Title: Rototype - RLB		
Size: A3	Document Number: FPGA - 04 - FPGA - Power	Rev: 1.0
Date: Monday, November 30, 2020	Sheet 0 of 47	



FPGA - Regulator

Title: Rototype - RLB		
Size: A3	Document Number: SoC - 02 - SoC - Regolatori	Rev: 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

12V
Alim Board

J61
Molex_0039300020
F2
Littelfuse 0440007WR
DC_IN
D55
PTVS17VS1UR
R709
1M
1%
C910
0.47uF
50V
Q15
AON7405
C909
22nF
50V
12Vin
Very Thick Net
R710
220K
GND

XAL1060-122MEC
L42
Vout : 5V0 @ 25A
5Vin
SH17

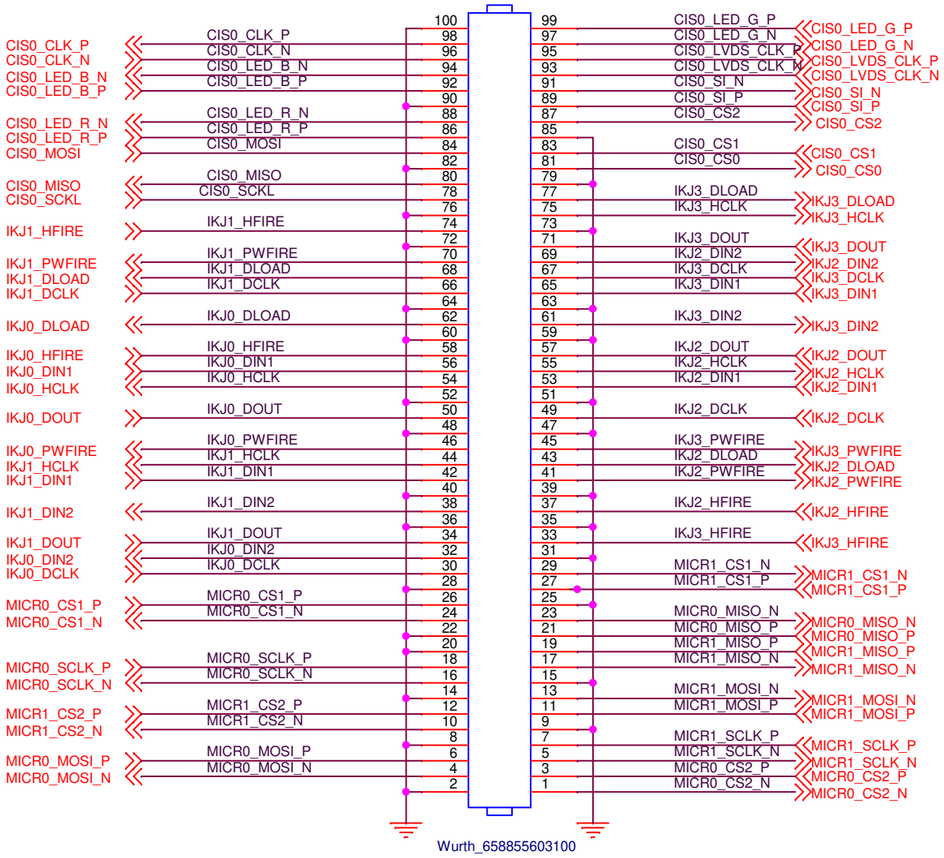
U62
MAX8686ETL+

C911 22uF
C915 22uF
C912 22uF
C913 22uF
R711
0.01
1%
C921
220nF
R715
182K
1%
C916
220nF
R712
47
1%
C917
1uF
R714
100
R713
4K7
1%
C918 47uF <RATING>
C919 47uF <RATING>
C914 47uF <RATING>
C920 47uF <RATING>
R716
9K1
1%
R717
10K
5%
R718
10
5%
R719
4K5
5%
C922
330pF
<RATING>
C923
15pF
<RATING>
C926
150pF
<RATING>
C927
15nF
<RATING>
C928
20nF
<RATING>
R720
182K
1%
C924
1uF
<RATING>
C925
220nF
<RATING>
PG_5V1

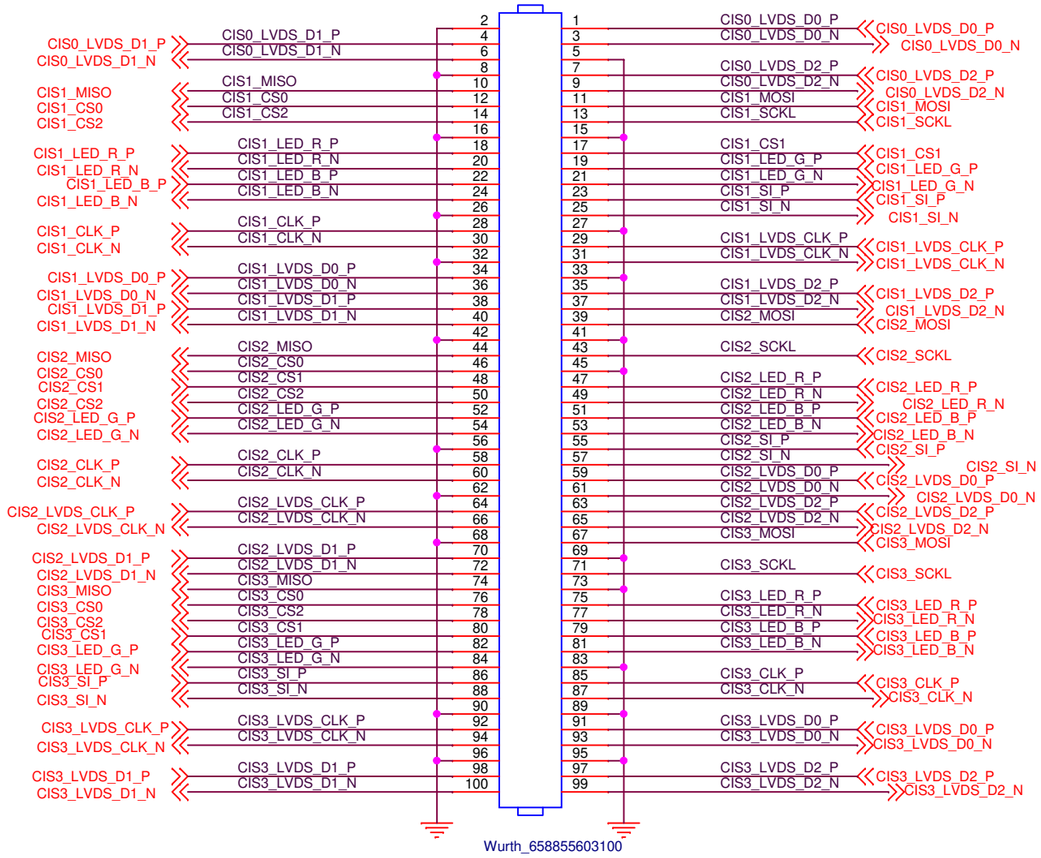
Power In

Title: Rototype - RLB		
Size: A4	Document Number: SoC - 05 - POWER IN	Rev: 1.0
Date: Tuesday, December 01, 2020	Sheet 0 of 47	

CONN_B_0



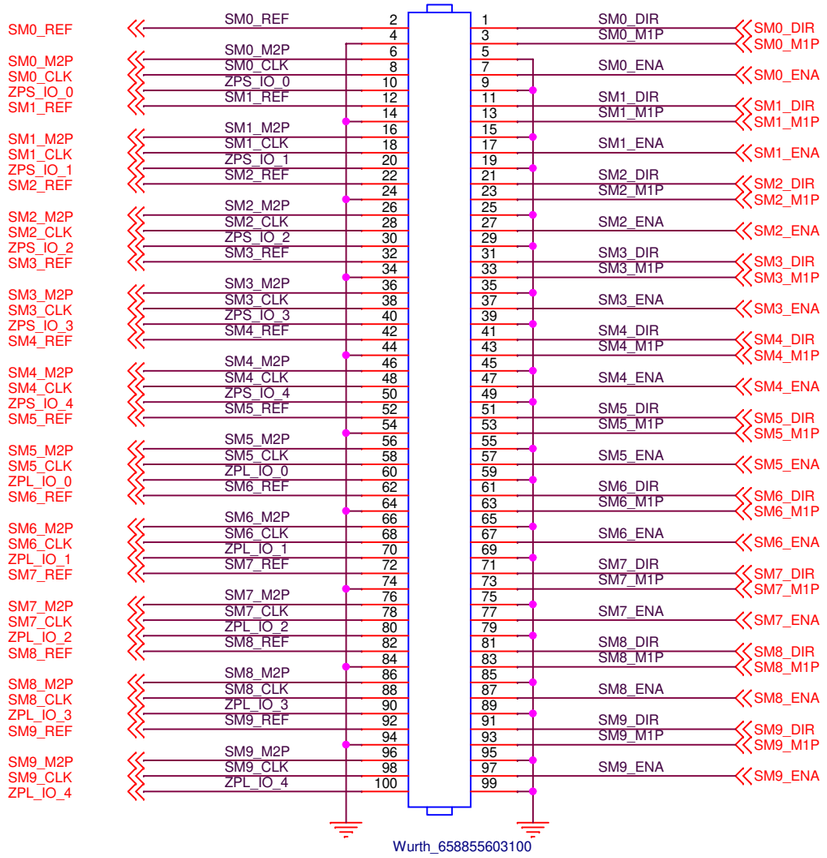
CONN_B_1



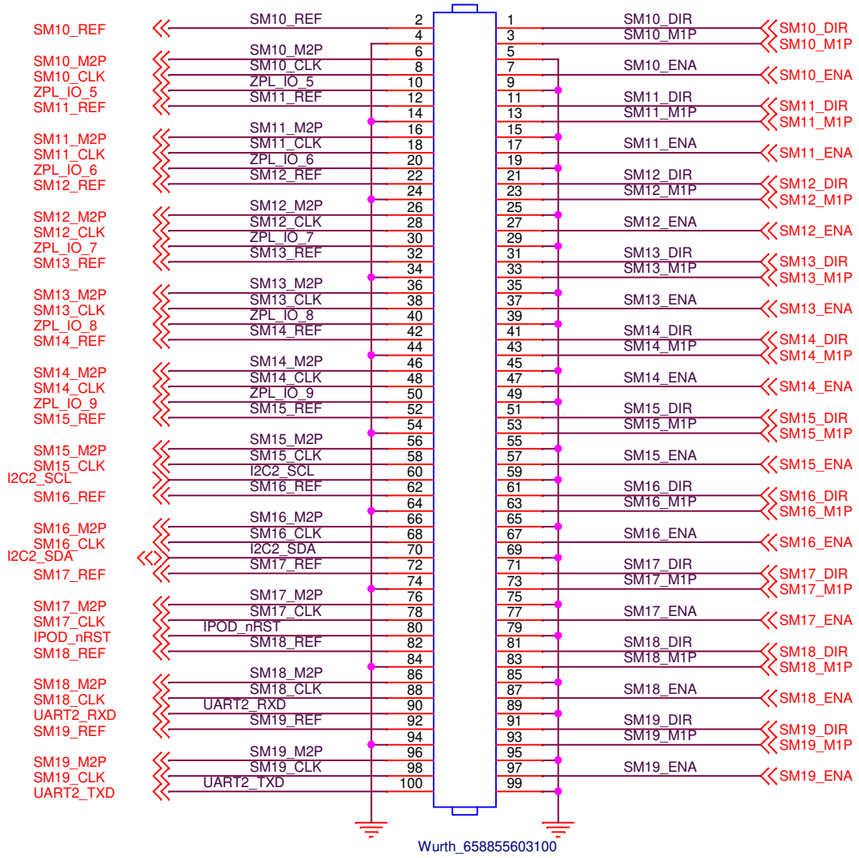
B - Conector

Title: Rototype - RLB		
Size: A3	Document Number: Connector - 06 - CONN - B	Rev: 1.0
Date: Thursday, November 26, 2020	Sheet 0 of 47	

CONN_R_0



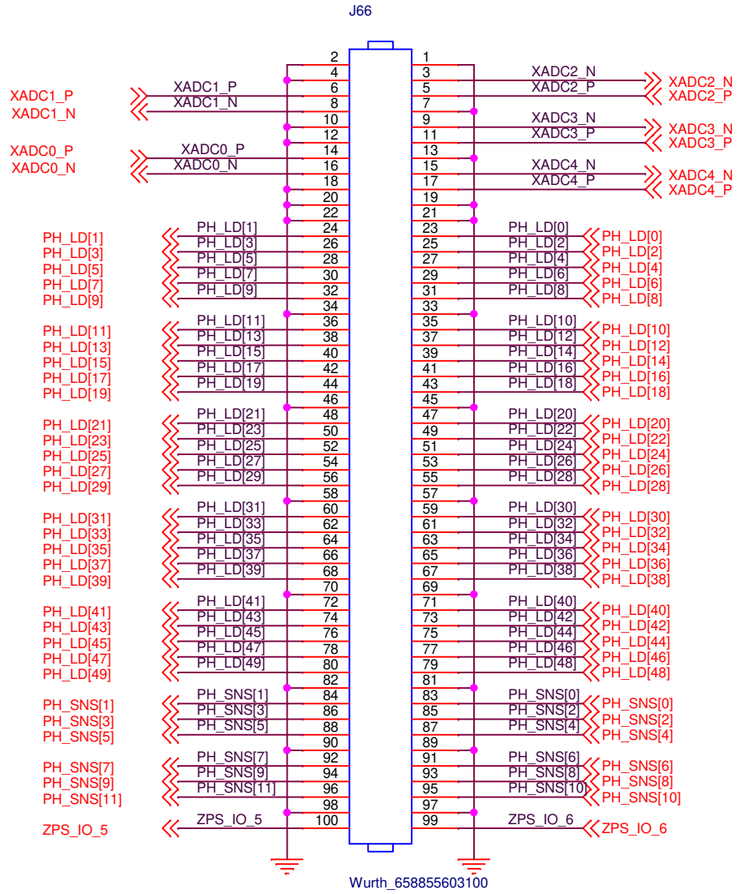
CONN_R_1



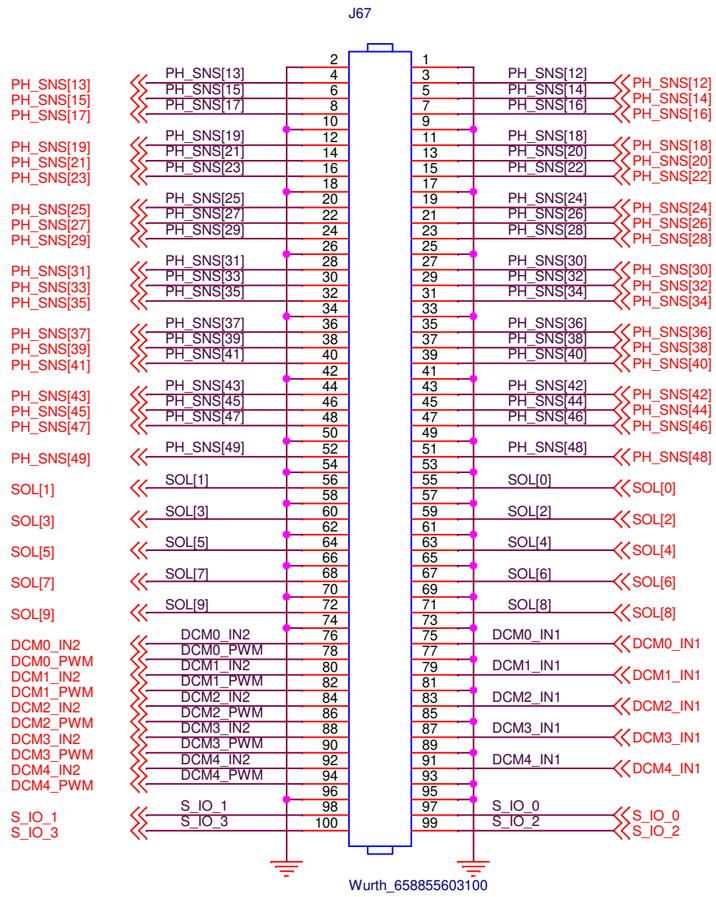
R - Conector

Title: Rototype - RLB		
Size: A3	Document Number: Connector - 06 - CONN - R	Rev: 1.0
Date: Thursday, November 26, 2020	Sheet 0 of 47	

CONN_T_0



CONN_T_1



T - Connector

Title: Rototype - RLB		
Size: A3	Document Number: Connector - 06 - CONN - T	Rev: 1.0
Date: Thursday, November 26, 2020	Sheet 0 of 47	