University of Central Florida

Department of Computer Science

CDA 5106: Fall 2020

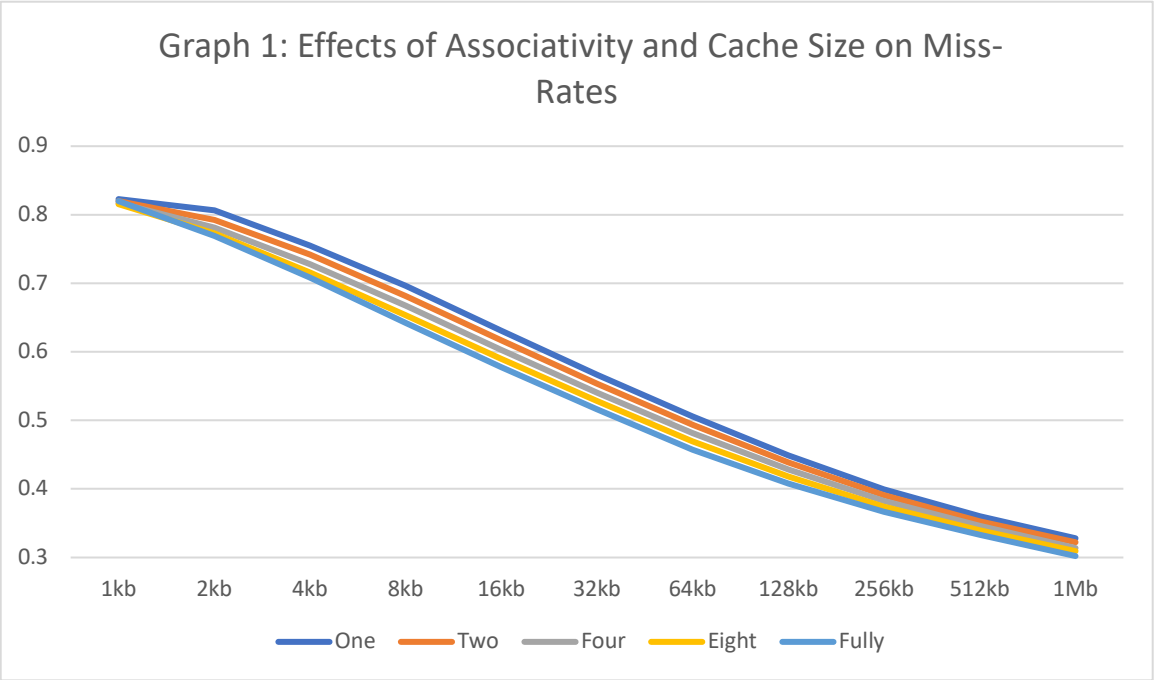
Machine Problem 1: Cache Design, Memory Hierarchy Design

by

<< Alexander Roustai >>

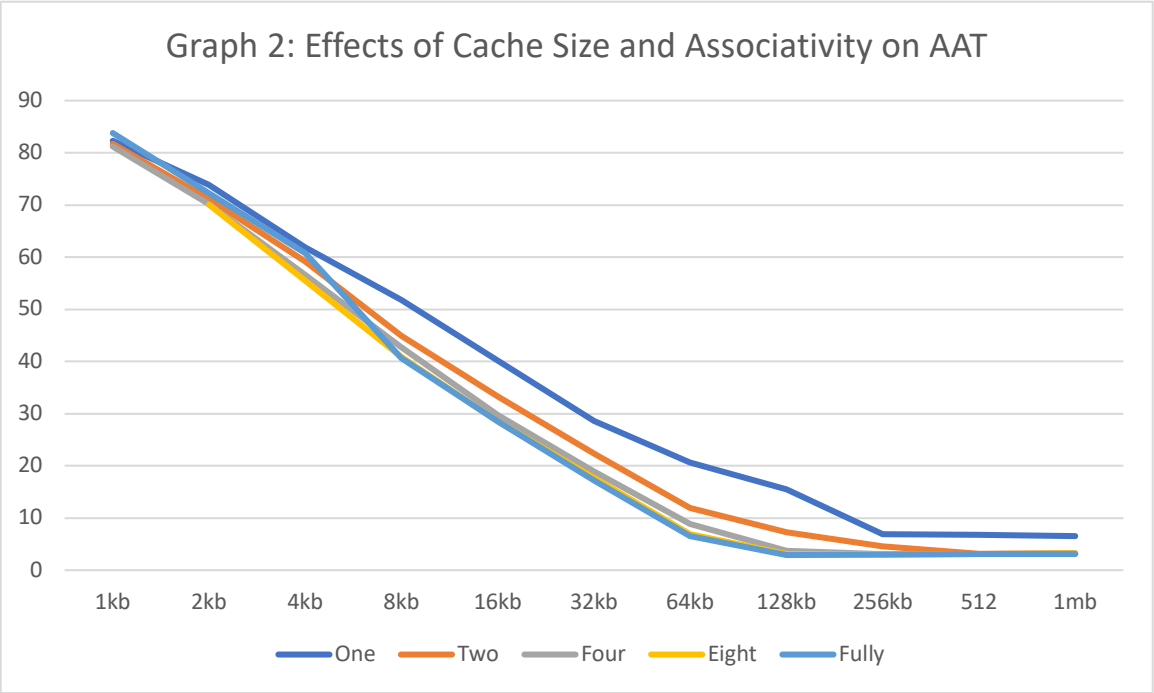
Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student's electronic signature: _____Alexander Roustai_____
(sign by typing your name)

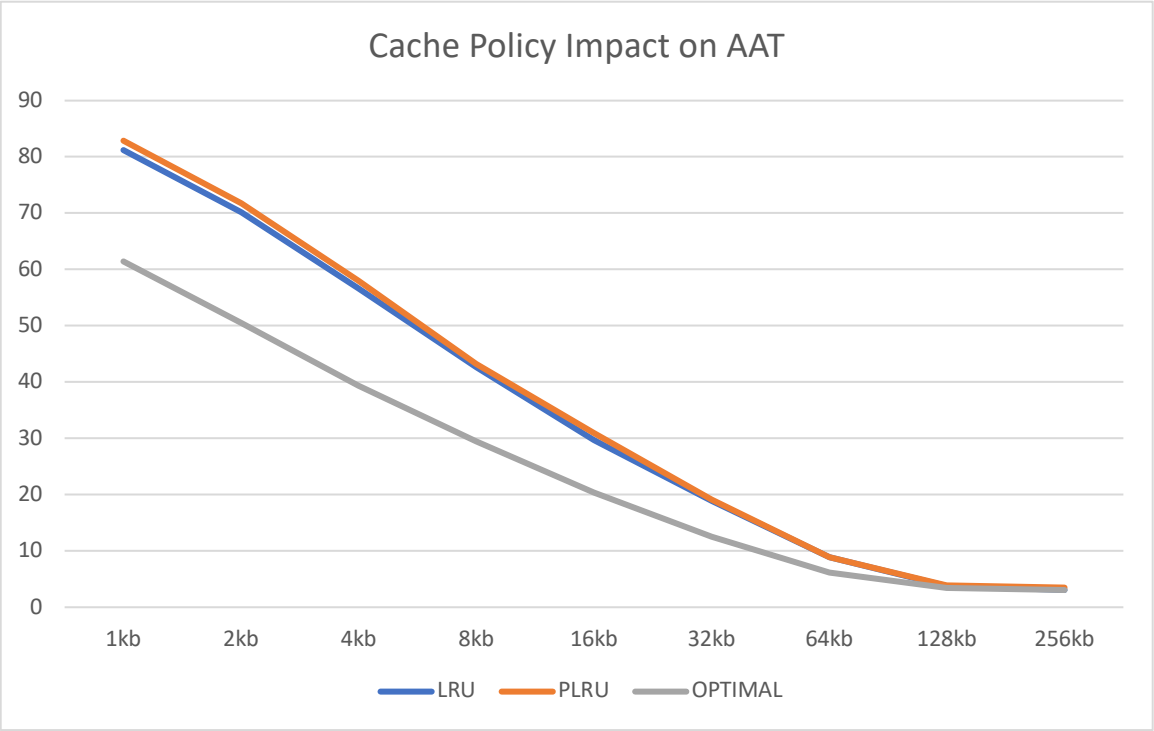


This graph shows the impact that cache size and associativity levels have on the system. As we can see the fully associative cache performs better than the other levels, but not by any significant degree. We also can see that miss rates have a direct relationship with both associativity and cache size and that by increasing either, or both of them we can see a reduction in the miss rates.

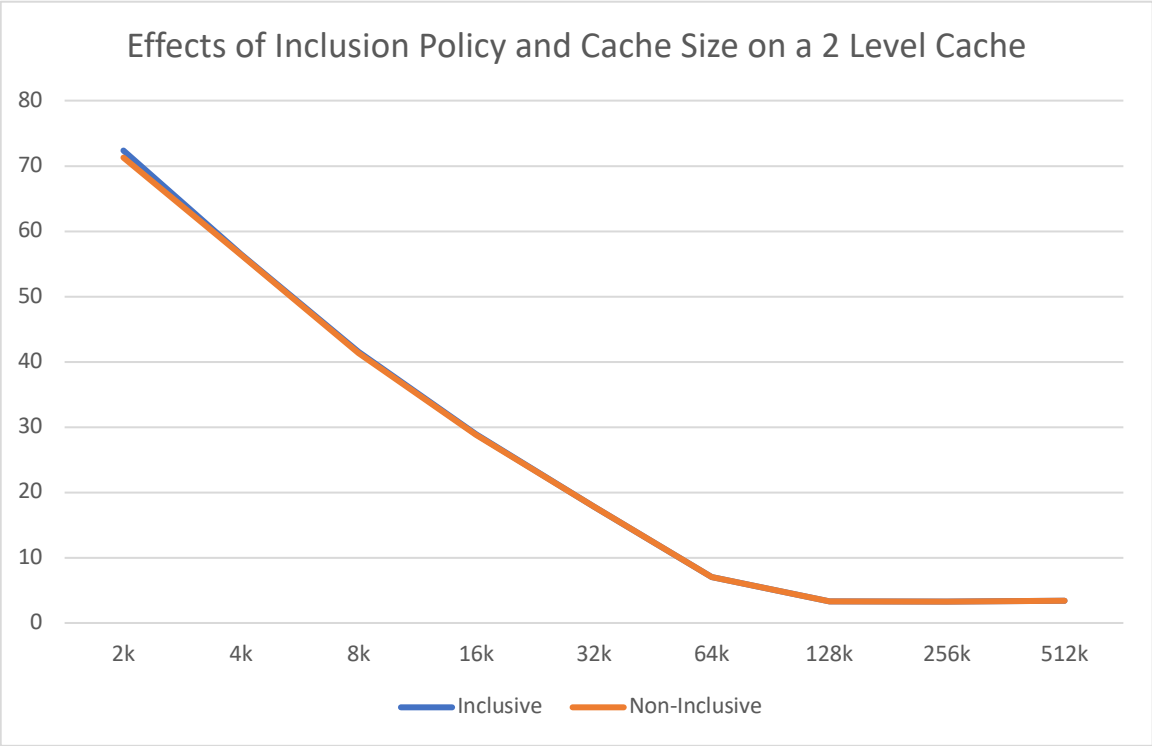
Judging by the graph and what we know about miss-rates, it is safe to say that the compulsory miss rate will increase as associativity increases. However, this will mean that our conflict miss-rate will decrease with more repeated variables being called. I would estimate that the compulsory miss rate is low, under 10 percent and the conflict is high. If the conflict rate were higher we would see less a sharp drop in the graph.



In this graph we can see the impact that cache size has on AAT. Due to the high miss penalty and the relatively low access time (ratios of over 100 times greater) we see that there is only benefits to increasing cache size. If however the difference between the hit and memory access wasn't as great, we would see the negative impacts of increasing size. Associativity does not confer anywhere near the same benefits how-ever. We do not see any real benefits to increasing the associativity beyond 4, and 2 way stops lagging behind rather quickly.



In the graph above we can see all of the different policy types for our cache. Unsurprisingly, the optimal performs the best and the PLRU performs the worst, though not much worse than LRU. What we do see however is that the difference between the three starts to converge as we keep increasing the cache size. This is to be expected because as the values of the cache size increase, the miss-rate will naturally go down. This will cause the difference in misses to be minimized between the different policies.



Here we can see the impact, or lack of impact, that the inclusion vs non-inclusion has on the system. While inclusive has a small lead in AAT in the beginning, it becomes virtually indistinguishable from non-inclusive cache policies. From here we can say as cache size grows bigger, the AAT will be about the same between the two.