Modeling and Design Challenges and Solutions for Carbon Nanotube-Based Interconnect in Future High Performance Integrated Circuits

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Single-walled carbon nanotube (SWCNT) bundles have the potential to provide an attractive solution for the resistivity and electromigration problems faced by traditional copper interconnect as technology scales into the nanoscale regime. In this article, we evaluate the performance and reliability of nanotube bundles for both local and global interconnect in future VLSI applications. To provide a holistic evaluation of SWCNT bundles for on-chip interconnect, we have developed an efficient equivalent circuit model that captures the statistical distribution of individual metallic and semiconducting nanotubes while accurately incorporating recent experimental and theoretical results on inductance, contact resistance, and ohmic resistance. Leveraging the circuit model, we examine the performance and reliability of nanotube bundles for both individual signal lines and system-level designs. SWCNT interconnect bundles can provide significant improvement in delay and maximum current density over traditional copper interconnect, depending on bundle geometry and process technology. However, for system-level designs, the statistical variation in the delay of SWCNT bundles may lead to reliability issues in future process technology. Consequently, if the SWCNT chirality can be effectively controlled and other manufacturing challenges are met, SWCNT bundles potentially are a viable alternative to standard copper interconnect as process technology scales.

Categories and Subject Descriptors: B.7.0 [**Integrated Circuits**]: General

General Terms: Design, Performance, Reliability

Additional Key Words and Phrases: Carbon nanotube, interconnect, nanotube bundle, resistance, inductance

1. INTRODUCTION

The modeling, design, and implementation of on-chip interconnect continues to be a fundamental roadblock to realizing high-performance integrated systems.

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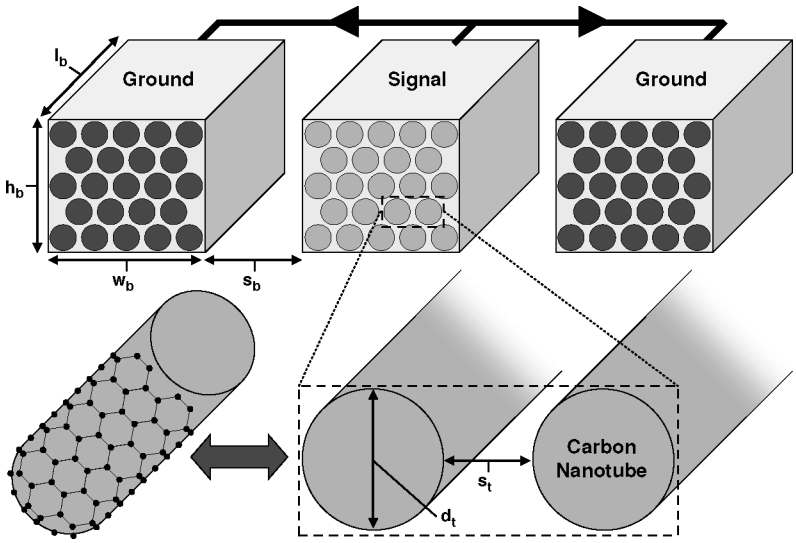

Fig. 1. System of single-walled carbon nanotube interconnect bundles implementing a signal line and two adjacent ground return paths.

As wire width decreases, traditional copper interconnect in high-performance VLSI systems will suffer significant increases in resistivity due to surface roughness and grain boundary scattering [ITRS 2005; Rossnagel and Kuan 2004; Steinhogl et al. 2002]. The increase in resistance will lead to delay and electromigration problems, which will limit both performance and reliability [ITRS 2005; Kapur et al. 2002; Naeemi et al. 2005]. Given the long-term scaling problems associated with traditional copper interconnect, radical alternatives are required. Single-walled carbon nanotubes (SWCNT) have been proposed as a possible replacement for on-chip copper interconnect due to their large conductivity and current carrying capabilities [McEuen and Park 2004; Kreupl et al. 2004]. While SWCNTs have desirable material properties, individual nanotubes suffer from a large intrinsic resistance that is not dependent on the length of the nanotube [Yao et al. 2000]. To alleviate the intrinsic resistance problem, bundles or ropes of SWCNTs in parallel, depicted in Figure 1, have been proposed and physically demonstrated as a possible interconnect medium for local and global interconnect as well as vias connecting metal layers [Kreupl et al. 2004; Li et al. 2003; Thess et al. 1996].

In this article, we provide a comprehensive analysis of the performance and reliability of SWCNT bundles for both local and global interconnect in future VLSI applications. We develop an efficient equivalent circuit model that captures the statistical distribution of individual metallic and semiconducting nanotubes while accurately incorporating recent experimental and theoretical results on inductance, contact resistance, and ohmic resistance [Zhou et al. 2005; Kim et al. 2005; Pennington and Goldsman 2005; Suzuura and Ando 2002; Leonard and Talin 2006]. The circuit model provides significantly better accuracy in both resistance and inductance than previously proposed SWCNT bundle models. Leveraging the circuit model, we examine the performance and

reliability of nanotube bundles for individual signal lines and their associated ground return paths for various bundle geometries and process parameters. The results indicate that SWCNT interconnect bundles can provide significant improvement in delay over traditional copper interconnect, depending on bundle geometry, individual nanotube diameter, and the statistical distribution of metallic nanotubes within the bundle. For system-level designs, the results indicate that the statistical variation in delay for SWCNT bundles can potentially lead to reliability issues in future process technology. Consequently, if the SWCNT chirality can be effectively controlled and other manufacturing challenges are met, SWCNT bundles may be a viable alternative to standard copper interconnect as process technology scales.

The rest of the article is organized in the following manner. Section 2 describes the current technology scaling problems associated with standard copper interconnect technology and introduces radical alternatives based on SWCNT bundles. In Section 3, we present and evaluate our circuit model for SWCNT bundle interconnect. Section 4 assesses the performance and reliability for SWCNT bundle interconnect. Section 5 concludes the article.

2. BACKGROUND AND MOTIVATION

The tremendous advancement in the field of integrated circuit manufacturing achieved in the past decade can largely be attributed to the successful scaling of CMOS technology. Substantial performance enhancement has been realized through evolutionary device scaling and increases in overall die size, which has led to increased processor speeds and high performance system-on-chip (SoC) technology. While transistor scaling and increased operating frequencies have improved overall performance, the impact of interconnect on performance and reliability has continued to increase [ITRS 2005; Rao et al. 2004; Acar et al. 2002; Uchino and Cong 2001; Schaumont et al. 2001; Hassoun and Alpert 2003; Doucet et al. 2004]. Crosstalk due to capacitive and inductive coupling in the global interconnect continues to limit the performance and reliability of high-performance nanoscale integrated circuits [Mondal and Massoud 2005; Gala et al. 2001; Beattie and Pileggi 2001; Elbouazzati et al. 2004]. In the future, process technology scaling coupled with increasing operating frequencies will exacerbate the delay, noise, and power problems that already plague interconnects in today's designs [Davis et al. 2001; Anis and Massoud 2003; Massoud et al. 2002; Su et al. 2006; Hu et al. 2003; Cong et al. 2001]. Furthermore, traditional interconnect materials will suffer from high resistivity, electromigration, and electromagnetic interference problems [Massoud and Ismail 2001; Kamon et al. 1999; Mondal and Massoud 2005]. As CMOS technology is pushed to its basic physical limits, alternate technologies are required for the realization of future high-performance integrated circuits. While interconnect has greatly benefited from advances in technology such as lower resistivity copper structures and low-k interconductor dielectrics [Maex et al. 2003], these solutions only provide one-time benefits. Therefore, future interconnect solutions will require more radical alternatives.

To alleviate the problems associated with today's interconnect technologies, several alternatives have been proposed [Floyd et al. 2002; Chang et al. 2001;

Chen et al. 2004; Miller 2000; Kobrinsky et al. 2004]. Three-dimensional integrated circuits have the potential to relieve the projected problems with both copper interconnect and mixed-signal SoC integration [Joyner et al. 2004; Das et al. 2003; Zhang et al. 2001]. By distributing components across multiple device layers, average interconnect length will be substantially reduced, thereby reducing the power and delay requirements imposed by global interconnect [Davis et al. 2001; Massoud and Ismail 2001]. While possibly a viable near-term solution, 3-D interconnect solutions have fundamental thermal and manufacturing problems that may limit their scalability. With wireless/RF interconnect, global data and clock signals are transmitted across the entire chip using RF mediums, which promises to increase bandwidth, decrease delay, and reduce the dependence on standard copper interconnect [Chang et al. 2001; Floyd et al. 2002]. However, the size and complexity of integrated transceivers coupled with substantial electromagnetic interference issues seriously limit the feasibility of wireless/RF interconnect [Chen et al. 2004]. Optical interconnects offer the promise of increased bandwidth, decreased delays, lower power consumption, and reduced electromagnetic interference [Miller 2000], but several challenges such as subwavelength optical confinement and the efficient design and implementation of modulators, detectors, and transimpedance amplifiers are still open research questions that need to be addressed [Berglind et al. 1999; Kapur et al. 2002]. Given the challenges facing these interconnect solutions, other technologies must also be considered for on-chip communication in future VLSI applications.

Single-walled carbon nanotubes (SWCNT) have been proposed as a possible replacement for on-chip copper interconnect due to their large conductivity and current carrying capabilities [McEuen and Park 2004; Kreupl et al. 2004]. SWCNTs are rolled graphitic sheets that can either be metallic or semiconducting, depending on their chirality [Wildoeer et al. 1998]. SWCNTs with diameters ranging from 0.4nm to 4nm have been reported [Qin et al. 2000; Zhou et al. 2005]. With reported current densities as large as $10^9 A/cm^2$, SWCNTs have significantly larger current carrying capabilities than traditional metallic interconnect which typically have current densities on the order of $10^5 A/cm^2$ [Baughman et al. 2002]. In Wei et al. [2001], carbon nanotubes were subjected to large current densities ($>10^9 A/cm^2$) and high temperatures (250 $^\circ$C) for approximately two weeks with no measurable deformation or breakdown. Therefore, due to their covalently bonded structure, carbon nanotubes are extremely resistant to electromigration and other sources of physical breakdown [Baughman et al. 2002]. In addition, carbon nanotubes can have significantly lower ohmic resistance than standard copper interconnect [McEuen and Park 2004]. While SWCNTs have desirable material properties, individual nanotubes suffer from a large intrinsic resistance of approximately 6.5kΩ that is not dependent on the length of the nanotube [Yao et al. 2000]. Therefore, individual SWCNTs cannot be used alone in many VLSI applications to construct high-performance interconnect.

To alleviate the intrinsic resistance problem, bundles or ropes of SWCNTs in parallel, depicted in Figure 1, have been proposed and physically demonstrated as a possible interconnect medium for local and global interconnect

as well as vias connecting metal layers [Kreupl et al. 2004; Li et al. 2003; Thess et al. 1996]. SWCNT bundles have sparsely packed metallic nanotubes that are randomly distributed within the bundle. With no special separation techniques, the metallic nanotubes are distributed with probability 1/3 since approximately one-third of possible SWCNT chiralities are metallic [Wildoeer et al. 1998]. However, techniques such as alternating current dielectrophoresis [Krupke et al. 2003], sequence-dependent DNA assembly [Zheng et al. 2003], and ion-exchange chromatography [Lustig et al. 2005] have the potential to increase the proportion of metallic nanotubes. Furthermore, nanotubes with diameters less than 0.5nm tend to be metallic regardless of chirality due to the steep angle of curvature in the graphene sheet [Qin et al. 2000]. Previous studies have failed to consider the implications of the statistically distributed nature of metallic SWCNTs in nanotube bundles. However, as we demonstrate in this article, the statistical distribution of metallic nanotubes can have important reliability and performance implications for nanotube bundles with interconnect geometries predicted in future process technologies [ITRS 2005].

3. MODELING OF SWCNT BUNDLE INTERCONNECT

3.1 Previous Modeling Techniques

In order to determine the performance and reliability of SWCNT bundle interconnect for future VLSI applications, we must develop a scalable circuit model that accurately captures the statistical distribution of metallic nanotubes while incorporating recent experimental and theoretical results. Several circuit models have been developed for individual metallic SWCNTs [Burke 2002, 2003, Salahuddin et al. 2005] or bundles of SWCNTs in parallel [Raychowdhury and Roy 2006; Naeemi and Meindl 2005b; Naeemi et al. 2005; Srivastava and Banerjee 2005]. Previous nanotube bundle models have either assumed that all nanotubes are metallic [Raychowdhury and Roy 2006; Naeemi and Meindl 2005b; Naeemi et al. 2005] or neglected the performance and reliability implications of the statistical distribution of the metallic nanotubes [Srivastava and Banerjee 2005; Srivastava et al. 2005]. Furthermore, we demonstrate, based on the new theoretical and experimental results presented in Zhou et al. [2005], Kim et al. [2005], Pennington and Goldsman [2005], Suzuura and Ando [2002], and Leonard and Talin [2006], that the diameter dependence of SWCNT ohmic and contact resistance can have a drastic impact on performance, which has not been previously considered when evaluating SWCNT bundle interconnect for VLSI applications.

For SWCNT inductance modeling, which consists of both magnetic and kinetic inductances, RLC models for SWCNTs have assumed that the current returns through a ground plane [Burke 2002, 2003, Salahuddin et al. 2005], which is only valid in specific interconnect configurations [Su et al. 2006]. Several previous models for SWCNT bundles have not considered magnetic inductance since it is predicted to be significantly less than the kinetic inductance for a single nanotube [Raychowdhury and Roy 2006; Naeemi and Meindl 2005b; Naeemi et al. 2005]. However, the magnetic inductance can exceed the kinetic

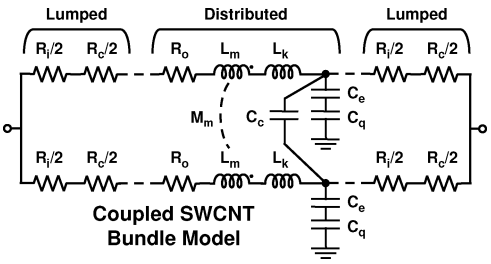

Fig. 2. Equivalent circuit model for two coupled SWCNT bundles.

inductance in realistic interconnect geometries as we discuss in Section 3.5.3. Other models have ignored the mutual magnetic inductance between nanotubes [Srivastava and Banerjee 2005], which can lead to nonphysical results [Beattie and Pileggi 2001]. Comprehensive models are needed to provide a holistic evaluation of SWCNT bundles for VLSI applications.

3.2 Circuit Model for SWCNT Bundles

This section describes our SWCNT bundle model and compares its accuracy and speed with previously proposed modeling techniques. We also discuss the sensitivity of the model parameters to the statistical distribution of metallic SWCNTs within a bundle. Figure 2 displays the RLC equivalent circuit model for two coupled SWCNT bundles, which is based on the Luttinger liquid model for individual SWCNTs presented in Burke [2002]. Each SWCNT in the circuit model has lumped resistances representing both the intrinsic ballistic resistance (R_i) and an additional contact resistance (R_c) between the SWCNTs and on-chip metal components. A distributed resistance (R_o) captures the ohmic resistance of the SWCNT which is determined by the nanotube's length and the mean free path of acoustic-phonon scattering when low-bias voltages are applied. C_e and C_c represent the electrostatic capacitance to ground and between SWCNTs, respectively. C_q is the quantum capacitance of the SWCNT, which is a per unit length quantity. L_k models the kinetic inductance, which is also a per unit length quantity. L_m and M_m represent the partial self and mutual inductances of the coupled SWCNTs which, when combined together for a signal bundle and its associated ground return paths (*ground-signal-ground* (GSG) *configuration* depicted in Figure 1), determine the loop magnetic inductance of the SWCNT bundle interconnect system. Note that M_m exists between each combination of nanotubes in the nanotube bundles. In each of the following sections, we discuss the modeling of resistance (Section 3.3), capacitance (Section 3.4), and inductance (Section 3.5) for SWCNT bundles and examine the impact of the statistically distributed metallic nanotubes on each circuit element.

3.3 Resistance Modeling

The resistance of an individual SWCNT depends on the applied bias voltage. For nanotubes operating in the low bias regime ($V_b \leq\approx 0.1V$), the resistance is the summation of the lumped intrinsic (R_i) and contact (R_c) resistances and

distributed per unit length ohmic resistance (R_o),

$$R_{low} = R_i + R_c \; if \; l_b \leq \lambda_{ap} \tag{1}$$

$$R_{low} = R_o + R_c \; if \; l_b > \lambda_{ap}, \tag{2}$$

where l_b is the length of the nanotube and λ_{ap} is the mean free path for acoustic-phonon scattering [Park et al. 2004; McEuen and Park 2004]. For high bias voltages ($V_b \geq\approx 0.1V$), the resistance of an individual nanotube depends on the applied bias voltage,

$$R_{high} = R_{low} + \frac{V_b}{I_o}, \tag{3}$$

where I_o is the maximum current that can flow through an individual nanotube, which is approximately 20 to 25μA [Yao et al. 2000]. For short nanotubes with ballistic and quasiballistic conduction ($l_b \leq$ 300nm), significantly higher saturation currents have been reported [Javey et al. 2004]. The maximum voltage drop across a SWCNT bundle [Naeemi and Meindl 2005a] is

$$V_{\max} = 2\left(\sqrt{b^2 - 4V_{dd}R_{low}I_o} - b\right) \tag{4}$$

$$b = R_{low}I_o + n_bR_{tr}I_o - V_{dd}, \tag{5}$$

where V_{dd} is the on-chip supply voltage, n_b is the number of metallic nanotubes in the bundle, and R_{tr} is the effective resistance of the driver connected to the interconnect. While high bias voltages can significantly increase the resistance of a SWCNT bundle, the worst case analysis presented in Naeemi and Meindl [2005a] suggests that the maximum voltage drop does not greatly impact the resistance unless the number of nanotubes in a bundle is small ($n_b < 50$), and the SWCNT length is small ($l_b < 10\lambda_{ap}$). Therefore, minimum pitch local interconnect constructed from SWCNT bundles in future process technologies will see the greatest impact from high bias voltages.

3.3.1 *Intrinsic and Contact Resistance.* The intrinsic resistance (R_i) of a ballistic SWCNT is

$$R_i = \frac{h}{4e^2} \approx 6.5k\Omega, \tag{6}$$

where h is Planck's constant, and e is the charge of a single electron [McEuen and Park 2004]. Regardless of its length, an individual SWCNT will have a minimum resistance of R_i. R_c models the increased lumped resistance due to imperfect metal contacts. As nanotube fabrication and bonding techniques have been improved, the additional resistance due to imperfect contacts has been significantly reduced and, in several experimental cases, has approached 0 (i.e., $R_i+R_c = R_i$) [McEuen and Park 2004; Liang et al. 2001; Kong et al. 2001]. However, recent experimental and theoretical results have revealed that the contact resistance of a SWCNT greatly increases when the diameter of the nanotube (d_t) is less than 2.0nm [Kim et al. 2005; Leonard and Talin 2006]. In addition, the saturation current (I_o) decreases substantially to approximately 5μA for $d_t =$ 1nm [Kim et al. 2005]. Based on the experimental data obtained in Kim et al. [2005] for Palladium and Rhodium contacts, the normalized increase in

contact resistance (D_{rc}) due to the decrease in nanotube diameter can be modeled using a quadratic rational function. Note that the empirical expression for D_{rc} should be modified based on experimental data for different fabrication techniques, contact materials, and contact bonding configurations. Based on Kim et al. [2005], the contact resistance remains relatively constant near the nominal value, R_{cnom}, for nanotubes with diameters greater than 2nm. While nanotubes with diameters less than 1.0nm were not measured in Kim et al. [2005], the results suggest that the contact resistance continues to increase as the nanotube diameter decreases. We model the overall contact resistance using

$$R_c = D_{rc} R_{cnom} \, if \, 1.0 \leq d_t \leq 2.0\text{nm} \tag{7}$$

$$R_c = R_{cnom} \, if \, d_t > 2.0\text{nm}. \tag{8}$$

As a result, nanotubes with small diameter experience significant increases in contact resistance.

3.3.2 *Ohmic Resistance.* When low bias voltages are applied to the SWCNT, the ohmic resistance [McEuen and Park 2004] (R_o) is

$$R_o = \frac{h}{4e^2} \frac{l_b}{\lambda_{ap}}, \tag{9}$$

which is valid if the length of the SWCNT exceeds the mean free path of acoustic-phonon scattering, $l_b > \lambda_{ap}$. Recent experimental evidence and theoretical formulations have demonstrated that λ_{ap} depends on the diameter of the SWCNT [Zhou et al. 2005; Pennington and Goldsman 2005; Suzuura and Ando 2002]. The resistance of an individual SWCNT versus diameter is governed by

$$R_o = \frac{h \alpha l_b T}{4e^2 v_F d_t}, \tag{10}$$

where v_F is the Fermi velocity in graphene, $v_F = 800,000\text{m/s}$, T is the temperature in Kelvin, and α is the total scattering rate of the SWCNT [Zhou et al. 2005; Suzuura and Ando 2002]. For metallic armchair nanotubes, Equation (10) is valid across a broad range of temperatures [Suzuura and Ando 2002]. Using atomic force microscopy, the electronic mean free path of a metallic SWCNT with a diameter of 1.8nm was measured to be approximately 1.6μm [Park et al. 2004]. Using this experimental measurement for λ_{ap} and the diameter-dependent expression for R_o, we calculate the diameter-dependent equivalent ohmic resistivity of a SWCNT using

$$\rho_t = \frac{h}{4e^2 C_\lambda d_t}, \tag{11}$$

where C_λ is a mean free path-to-nanotube diameter proportionality constant defined as

$$C_\lambda = \frac{\lambda_o}{d_{to}} \approx \frac{1600\text{nm}}{1.8\text{nm}} \approx 888.9, \tag{12}$$

based on the experimental data obtained in Park et al. [2004]. As nanotube fabrication techniques improve, the mean free path should increase, thereby enlarging C_λ.

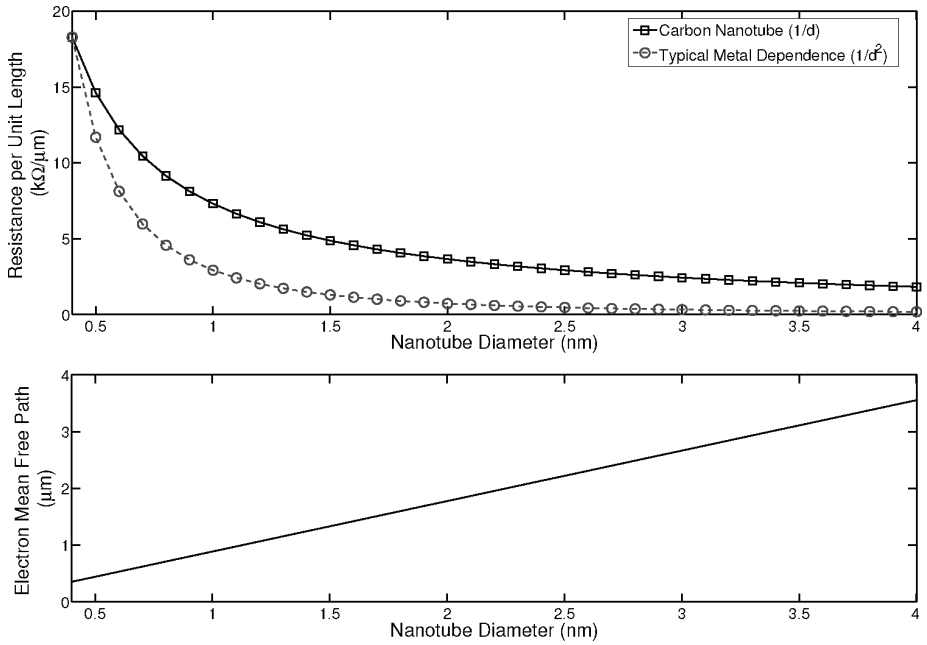

Fig. 3. Ohmic resistance per unit length versus carbon nanotube diameter (d_t). The ohmic resistance per unit length for carbon nanotubes is proportional to $1/d$, while, for standard copper conductors, the per unit length resistance has a $1/d^2$ dependence at low frequencies. Note that the ohmic resistance is approximately equivalent to the total resistance for bundles with large length values.

Using the previously defined diameter-dependent nanotube effective resistivity, we calculate the resistance per unit length and λ_{ap} for SWCNTs of various diameters as depicted in Figure 3. As d_t is increased, λ_{ap} increases linearly, which corresponds to a $1/\lambda_{ap}$ decrease in resistance [Suzuura and Ando 2002]. The resistance per unit length for carbon nanotubes is proportional to $1/d$, while, for standard copper conductors, the resistance has a $1/d^2$ dependence at low frequencies. Therefore, the resistance of SWCNTs is proportional to the surface area of the nanotube. In contrast, the resistance of a metallic conductor is proportional to the cross-sectional area of the conductor. Given the fact that the diameter of SWCNTs can be controlled relatively well in the fabrication process [McEuen and Park 2004; Zheng et al. 2003; Lustig et al. 2005; Cheung et al. 2002], understanding and modeling the impact of d_t on bundle resistance is crucial. The resistance of the SWCNT bundle, assuming no current redistribution due to magnetic inductance, is defined by the parallel combination of the individual SWCNT resistances,

$$R_b = R_t/n_b, \tag{13}$$

where R_t is the total resistance of an individual SWCNT and n_b is the number of metallic nanotubes in a given bundle, which can be expressed as

$$n_b = P_m(n_h n_w - \lfloor n_h/2 \rfloor), \tag{14}$$

where P_m is the probability that a nanotube is metallic, n_h is the number of nanotubes in the vertical dimension,

$$n_h = \lfloor h_b/d_t \rfloor, \tag{15}$$

and n_w is the number of nanotubes in the horizontal dimension,

$$n_w = \lfloor w_b/d_t \rfloor. \tag{16}$$

Note that we do not consider the coupling resistance between the nanotubes in a bundle since it has been physically measured to be larger than 2MΩ, which is significantly larger than the intrinsic resistance of 6.5kΩ for the individual SWCNTs in the bundle [Stahl et al. 2000]. For the GSG interconnect configuration, the resistance depends on the total number of ground return paths (n_{grp}),

$$R_b = \frac{(1 + 1/n_{grp})R_t}{n_b}, \tag{17}$$

assuming that the current is distributed equally in each of the ground return paths and that all bundle cross-sectional dimensions are the same. Note that R_b is substantially reduced as the number of nanotubes in the bundle increases.

3.3.3 *Accuracy of Diameter-Dependent Resistance Formulation.* The diameter dependence of the ohmic and contact resistance of an individual SWCNT has interesting implications for the design of SWCNT bundle interconnect and its suitability as a replacement for traditional copper interconnect as process technology scales. To investigate the diameter-dependent impact of effective ohmic resistivity of the SWCNT bundle, we calculate the per unit area ohmic resistivity of both densely ($P_m = 1$) and sparsely ($P_m = 1/3$) packed bundles which is depicted in Figure 4. SWCNT diameters range from 0.4nm, which corresponds to the smallest possible metallic nanotube [Qin et al. 2000], to 4.0nm [Zhou et al. 2005]. For comparison purposes, we plot the resistivity of bulk copper and predicted resistivity of global copper wires with minimum pitch in 45nm and 22nm process technologies [ITRS 2005]. To highlight the comparison between the ohmic resistance of copper and SWCNT bundles, we neglect the contact resistance for this experiment, which is valid for long interconnect lengths and bundles with a large number of nanotubes. We also plot the effective ohmic resistance for bundles with a nanotube diameter-independent resistance, which was assumed in previous SWCNT bundle models. The percentage difference in ohmic resistance between the proposed diameter-dependent formulation and previous diameter-independent models is displayed in Figure 5. The results indicate that neglecting the diameter-dependent nature of ohmic resistance can produce errors as high as 120 percent. To accurately determine the relative performance of SWCNT bundles and traditional copper interconnect, the diameter-dependent resistance of the SWCNTs must be taken into account.

To determine the effect of the diameter-dependent contact resistance on SWCNT bundles, we calculate the contact resistance of bundles with different individual nanotube diameters and bundle width values. The calculated contact resistances, normalized to the contact resistance of a single SWCNT

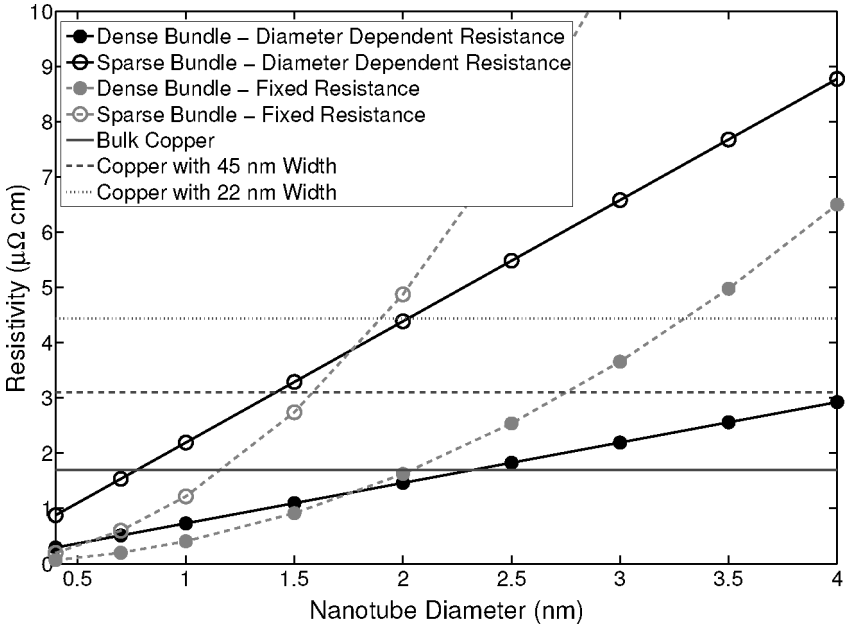

Fig. 4. Effective ohmic resistivity versus d_t for dense and sparse nanotube bundles modeled with and without the diameter-dependent resistance formulation. The resistivity of bulk copper and predicted resistivity of global copper wires with minimum pitch in the 45nm and 22nm process technologies are shown for reference. Note that the ohmic resistance is approximately equivalent to the total resistance for bundles with large length values.

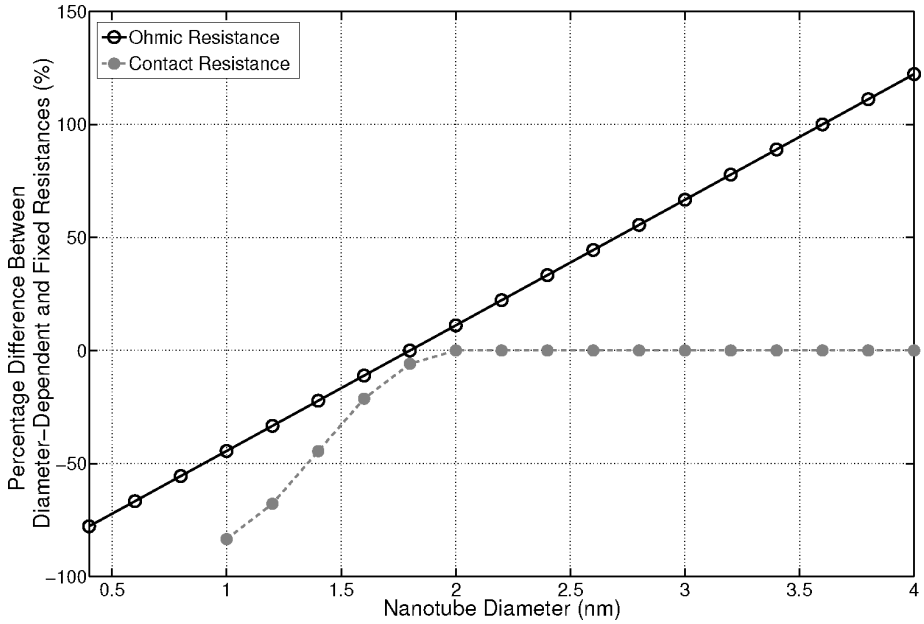

Fig. 5. Percentage difference between the diameter-dependent and fixed diameter-independent resistances for both ohmic and contact resistance.

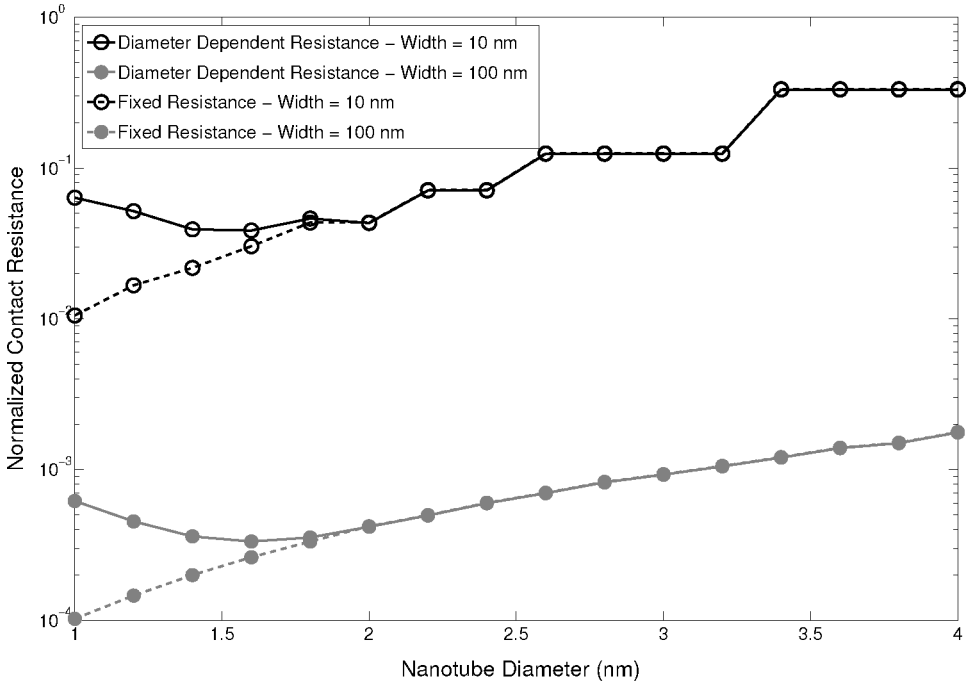

Fig. 6. Contact resistance of a SWCNT bundle with the specified nanotube diameters normalized to the contact resistance of an individual nanotube. Both the diameter-dependent and fixed diameter-independent resistances are depicted.

with large diameter (R_{cnom}), are depicted in Figure 6 for densely packed nanotube bundles. For sparse bundles, the normalized contact resistance values are three times larger if the probability of a given nanotube being metallic is one-third. The percentage difference in contact resistance between the proposed diameter-dependent formulation and previous diameter-independent models is displayed in Figure 5. The diameter-dependent contact resistance produces significantly higher overall contact resistances for the bundles with nanotubes diameters less than 1.8nm. For $d_t = 1$nm, neglecting the diameter dependence on contact resistance underestimates the resistance by 85 percent. Therefore, to accurately determine the relative performance of SWCNT bundles and traditional copper interconnect, the diameter-dependent resistance of the SWCNTs must be taken into account.

3.3.4 *Comparison between SWCNT and Copper Resistance.* To examine the impact of the overall SWCNT bundle resistance for realistic interconnect geometries, we calculated the total resistance of dense SWCNT bundles for various bundle length and width values, $d_t = 1.0$nm, $R_{cnom} = 20\text{k}\Omega$, and $I_o = 20\mu$A. We assume that the supply voltage is 0.8V, and the driver resistance is 2.5kΩ, which are predicted by the 2005 International Technology Roadmap for Semiconductors (ITRS) for the 22nm process technology [ITRS 2005]. The maximum voltage drop across a SWCNT bundle for a particular supply voltage and driver resistance was formulated in Naeemi and Meindl [2005a]. The results

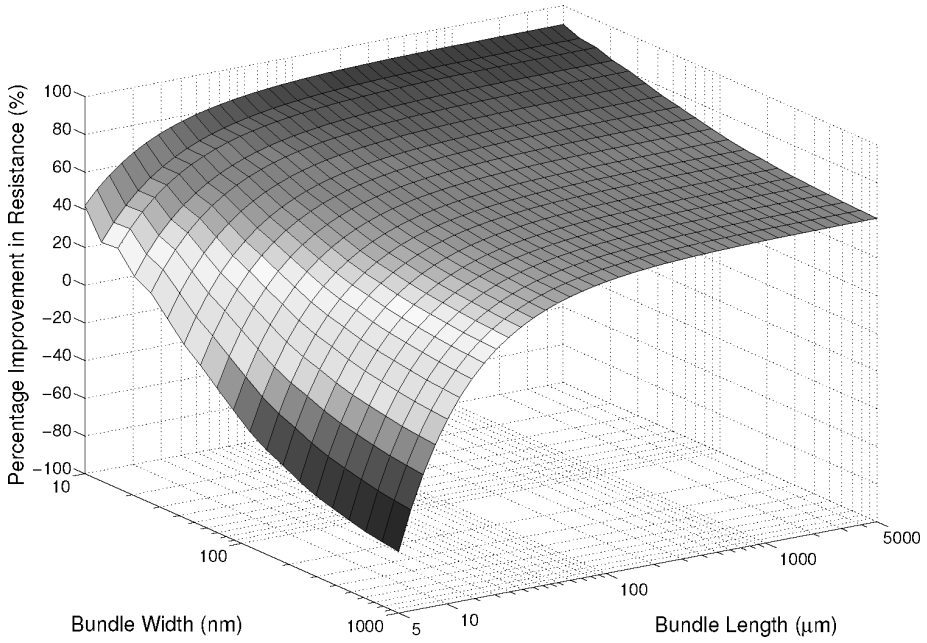

Fig. 7. Percentage improvement in SWCNT bundle resistance over copper interconnect resistance for typical interconnect geometries.

are displayed in Figure 7. The percentage improvement in resistance obtained by using SWCNT bundles can be categorized based on the width and length of the bundles. For long bundles with large widths, the contact resistance of the bundle is insignificant, and the nanotube bundle completely benefits from the decrease in effective resistivity displayed in Figure 4. For $d_t = 1.0$nm, the overall resistance is decreased by 61 percent over copper interconnect. For long bundles, with small widths of approximately 22nm, this improvement in resistance increases to 82 percent due to the increase in copper resistivity. The diameter of the individual SWCNTs in the bundle greatly impacts its relative resistive improvement over traditional copper interconnect. For example, dense bundles with individual nanotube diameters of 2.0nm have only a 22 percent improvement in resistance based on the diameter-dependent resistance model.

SWCNT bundles are at a disadvantage for short interconnect lengths and large widths when the contact resistance is significant compared to the ohmic resistance and the resistivity of the standard copper interconnect is near its bulk value. For short bundle lengths with narrow widths, the increased resistivity of standard copper interconnect can cause the SWCNT interconnect to become more favorable despite its large contact resistance. At a certain bundle length, the resistance of the SWCNT bundle is the same as standard copper interconnect, shown in Figure 7. For narrow bundles, this length is decreased due to the increased ohmic resistance of narrow copper interconnect wires. The l_b value for which the resistance of the SWCNT bundle equals that of copper interconnect for a given bundle width can be calculated by equating the

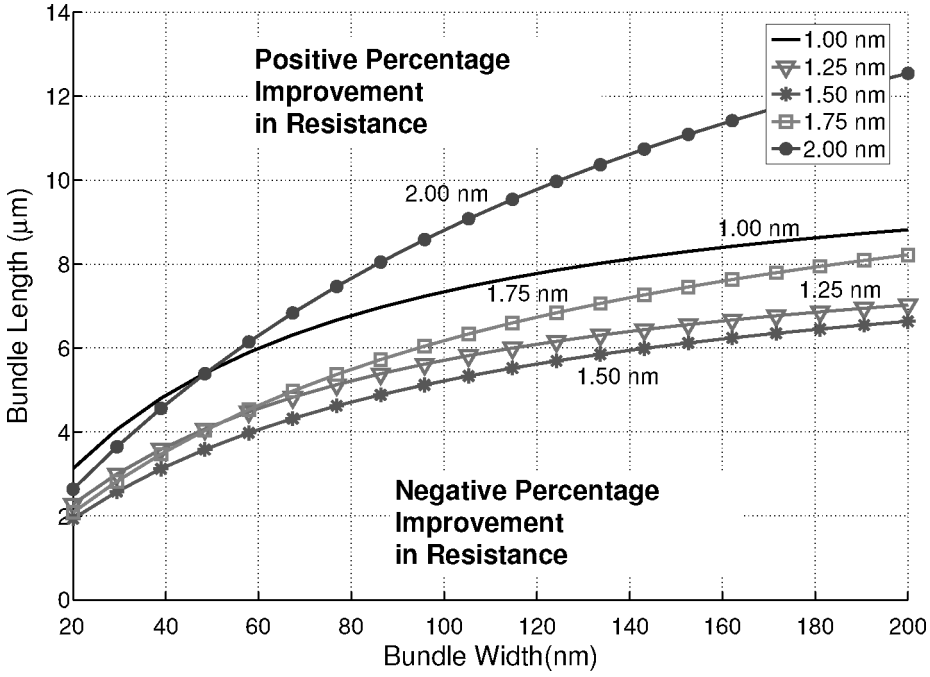

Fig. 8. Bundle geometry where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various d_t values.

resistance of copper and SWCNT bundle interconnect for a particular conductor geometry:

$$R_{Cu} - R_b = 0 \Rightarrow \frac{\rho_{Cu} l_b}{w_b h_b} - \frac{R_c + \rho_t l_b}{n_b} = 0, \tag{18}$$

where R_{Cu} is the total resistance of a copper conductor with the same dimensions as the nanotube bundle, and ρ_{Cu} is the copper conductor's width-dependent resistivity. Solving Equation (18) for l_b yields

$$l_b = \frac{R_c w_b h_b}{\rho_{Cu} n_b - \rho_t w_b h_b}. \tag{19}$$

Using Equation (19), the minimum length for which SWCNT bundle interconnect has an advantage over copper technology for a particular conductor geometry can be determined.

Figure 8 depicts the bundle length and width where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various nanotube diameters based on Equation (19). For this set of simulations, we assume that $P_m = 1$ and $R_{cnom} = 20\text{k}\Omega$. Two conflicting design parameters impact the minimum interconnect length where SWCNT bundles have an advantage in resistance over copper interconnect. As the nanotube diameter is decreased, the contact resistance of the individual SWCNTs substantially increases as described in Section 3.3.1. However, the number of nanotubes in the bundle increases as the nanotube diameter decreases, which leads to

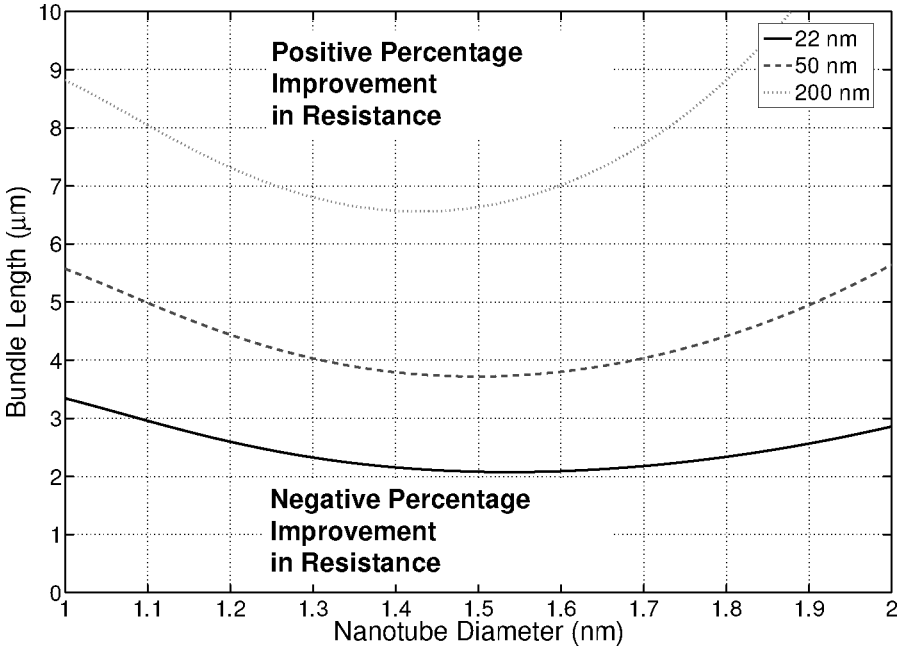

Fig. 9. Bundle length and nanotube diameter where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for $w_b = 22$, 50, and 200nm. Note that the bundle has a optimum d_t value that depends on w_b and l_b.

lower overall resistance as described by Equation (13). Due to the interaction between these two conflicting trends, an optimum individual nanotube diameter exists for a given nanotube bundle width. Figure 9 shows the bundle length and nanotube diameter where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various bundle width configurations. The optimal diameter can be determined be minimizing Equation (19) with respect to d_t, which is encapsulated in ρ_t, for a given bundle length.

For realistic interconnect configurations, multiple gates may need to be driven from a single source. In the absence of several possible nanotube bundle splitting techniques [Ting and Chang 2002; Chiu et al. 2002; Meng et al. 2005], accommodating fanout with SWCNT bundle interconnect will require multiple metal contacts as depicted Figure 10. By adding additional metal contacts to the nanotube bundle interconnect, the minimum distance for which nanotubes have a resistance advantage over copper increases due to the larger contact resistance. Figure 11 display the bundle length and number of individual segments in a nanotube interconnect where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various w_b values with $R_{cnom} = 20\text{k}\Omega$. Since the resistivity of copper decreases for larger width values for the aforementioned reasons, larger width interconnect requires longer wire lengths for SWCNT interconnect to become advantageous. The length required for SWCNT interconnect to have lower resistance for multiple segment is a multiple of the length required for one segment.

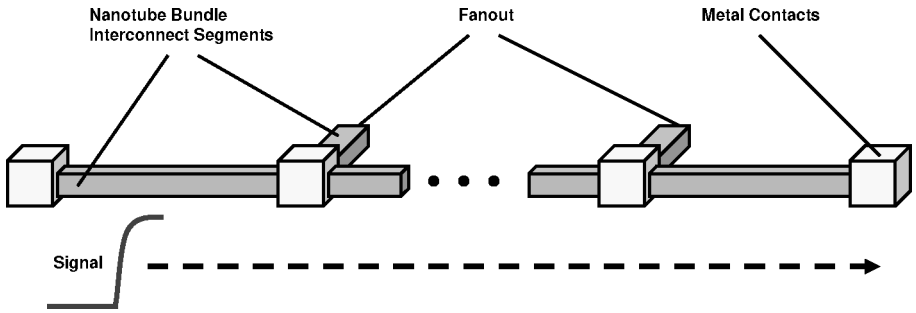

Fig. 10. Nanotube bundle interconnect with fanout may require multiple metal contacts that result in increased contact resistance.

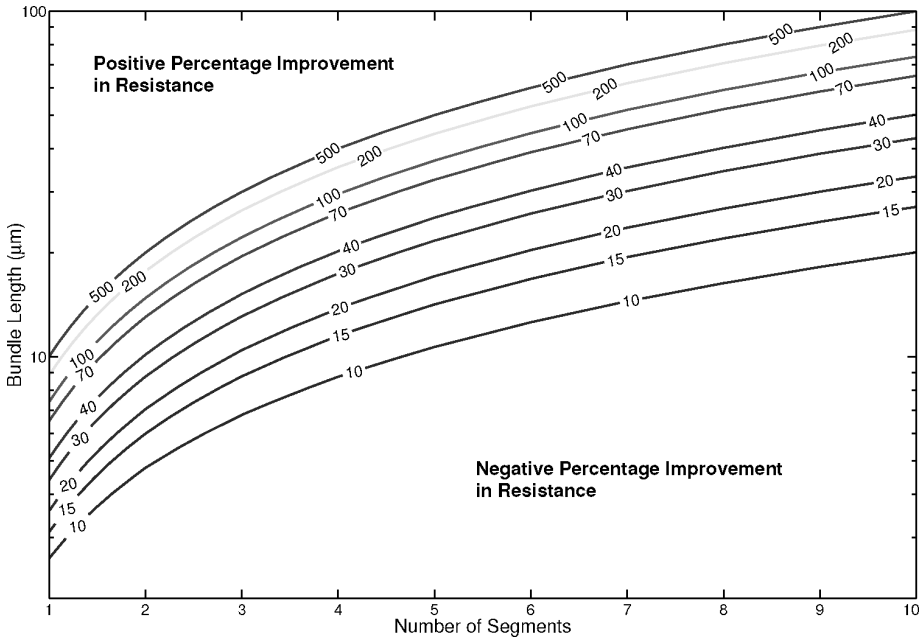

Fig. 11. Bundle length and number of segments in a nanotube interconnect where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various w_b values (in nm).

The contact resistance of an individual nanotube also plays an important role in determining the relative advantage of SWCNT bundle interconnect over standard copper technology. Figure 12 depicts the bundle length where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various contact resistance values, w_b values, and numbers of segments. From Figures 11 and 12, it is clear that the impact of multiple contacts depends on the contact resistance and number of segments. In cases where the number of segments is relatively low and the contact resistance is near its intrinsic value of 6.5kΩ, SWCNT interconnect with fanout may have

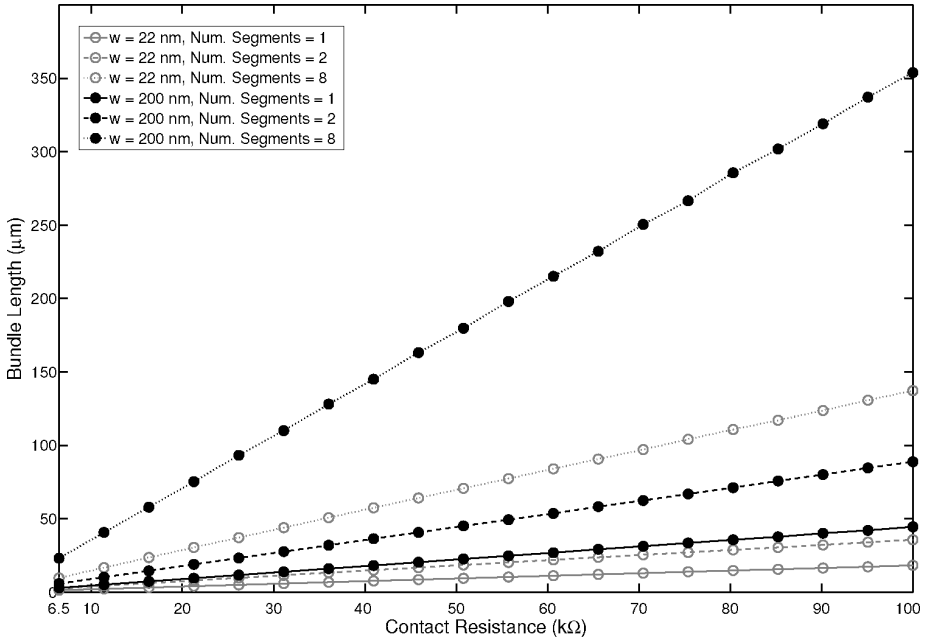

Fig. 12. Bundle length where the percentage improvement in SWCNT bundle resistance over copper interconnect resistance is zero for various contact resistance values (R_{cnom}), w_b values, and numbers of segments.

performance advantages for local and intermediate interconnect applications. However, for large fanout requirements and large contact resistances, SWCNT interconnect will have a resistive advantage only for global interconnect. Connecting multiple SWCNT interconnect lines to a single metal contact can also significantly reduce the impact of contact resistance on fanout. While many factors will ultimately contribute to the realization of SWCNT bundle interconnect, the results indicate that SWCNTs have the resistive properties to potentially be a viable replacement for copper interconnect, depending on the interconnect geometry, contact resistance, fanout, individual nanotube diameter, and probability that a given nanotube in the bundle is metallic.

3.4 Capacitance Modeling

The capacitance of a nanotube bundle consists of both a quantum capacitance (C_q) and an electrical capacitance ($C_e + C_c$). The quantum capacitance is a per unit length quantity for a given nanotube and has a theoretical value of $e^2/2hv_F \approx 25\text{aF}/\mu\text{m}$ [Burke 2003]. The electrical capacitance between a nanotube bundle and adjacent nanotube bundles depends on the bundle geometry and spacing between bundles. We have developed a model for determining the capacitance between the signal and ground bundles in the geometry depicted in Figure 1. The model is capable of handling the probabilistic distribution of metallic and semiconducting nanotubes. As the number of nanotubes increases

within the bundle, the variation in capacitance values arising from the variation in nanotube locations will be reduced. To verify this assumption, we performed Monte Carlo simulations for capacitance using the interconnect analysis program FastCap [Nabors and White 1991] for different probabilities of metallic nanotubes and different bundle dimensions. We found that, when the bundles were more than fifteen nanotubes wide, the absolute variation in the capacitance value was less than 3% for $P_m = 0.3$. For larger values of P_m, the variation was even less. This allows us to model the capacitance of the bundles by assuming a fixed placement of the SWCNTs, which greatly reduces the computational resources required. An *equivalent height* approach is used in our model where we represent each bundle as a single conductor of width equal to the width of the bundle and an equivalent height h_{eq} given by $h_{eq} = h_b(0.5 + 0.3P_m)$. The constants in this formulation were determined using linear least-squares regression for a large number of bundle geometries simulated using FastCap. Once the bundles are approximated with single conductors, the capacitance is found using the analytical capacitance model presented in Sohn et al. [2001]. The capacitance values obtained using our model were compared to the results from FastCap for a number of cases, and the error was found to be less than 5%.

3.5 Inductance Modeling

3.5.1 *Magnetic Inductance.* SWCNTs have both *magnetic* and *kinetic* inductances that can affect interconnect delay, noise, and power consumption [Burke 2003; Massoud and Ismail 2001; Massoud et al. 2002; El-Moursy and Friedman 2004]. The magnetic inductance captures the impact of the voltage induced by the magnetic fields produced by time varying currents which is encapsulated in Ampere's and Faraday's laws [Massoud and Ismail 2001]. Unlike resistance, capacitance, and kinetic inductance, which are per unit length quantities at frequencies where magnetoquasistatic assumptions are valid, magnetic inductance is dependent on the entire current loop which typically consists of a signal line and its associated ground return paths as depicted in Figure 1 [Beattie and Pileggi 2001]. Since the distribution of the current in the loop may not be known a priori, the concept of *partial inductance* is used to model the magnetic inductance. Partial inductance is a mathematical construct that assumes that the current flowing in a particular conductor, in the case of partial *self* inductance, or the current flowing in adjacent conductors, in the case of partial *mutual* inductance, has a current return path at infinity. The partial inductance construct has no physical meaning by itself. However, when the partial self and mutual inductances are combined in a particular manner over an entire current loop, the total loop inductance, which is the physical inductance that impacts delay, noise, and power consumption, can be calculated [Beattie and Pileggi 2001]. Assuming that each nanotube is current carrying filament, the nanotube's partial self inductance (L_m) is

$$L_m = 200 l_t \left(\ln \frac{l_t}{d_t} + 0.5 + \frac{2d_t}{3l_t} \right), \tag{20}$$

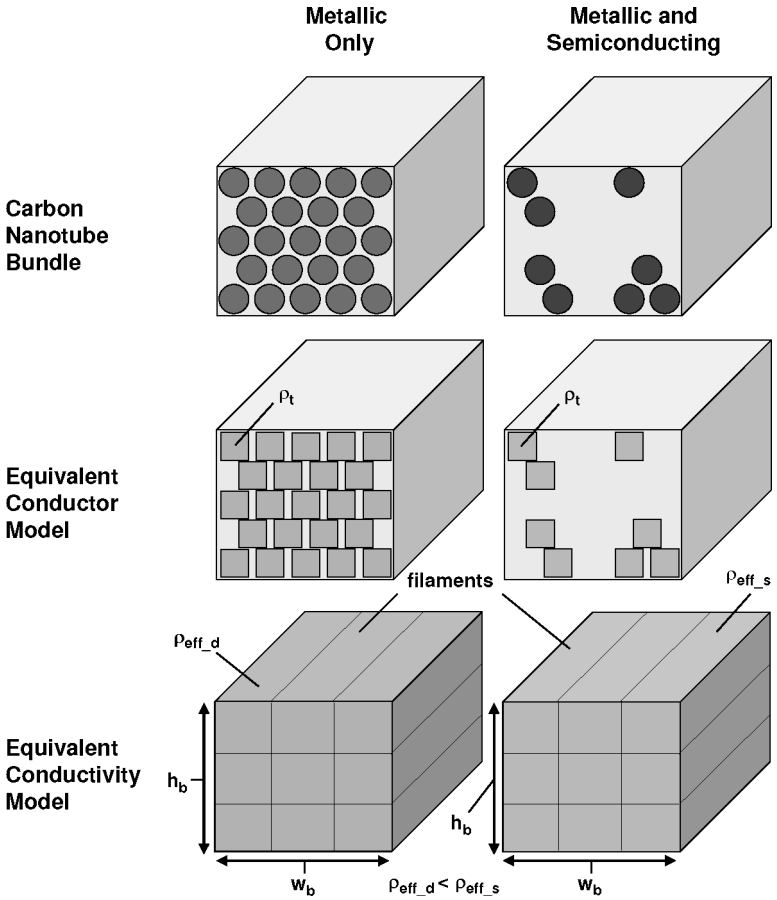

Fig. 13. Geometric representation of the modeling techniques we utilize to characterize the magnetic inductance for both dense metallic and sparse metallic/semiconducting carbon nanotube bundles.

where l_t and d_t are the length and diameter of an individual nanotube. The mutual inductance (M_m) between two parallel current carrying nanotubes of the same length is

$$M_m = 200 l_t \left(\ln\left(r + \sqrt{1+r^2}\right) - \sqrt{1+\left(\frac{1}{r}\right)^2} + \frac{1}{r} \right), \tag{21}$$

where $r = l_t/s_t$ and s_t is the center-to-center spacing between the two nanotubes [Nieuwoudt et al. 2005; Yue and Wong 2000].

In order to determine the loop inductance for SWCNT bundles, we utilize the Partial Element Equivalent Circuit (PEEC) method [Beattie and Pileggi 2001; Kamon et al. 1994]. To apply the PEEC method to SWCNT bundles, we model each nanotube in the bundle as an individual current carrying filament. We call this modeling method the *equivalent conductor model* which is graphically depicted in Figure 13. Using a conservation of energy approach,

the loop inductance for the signal bundle and its parallel ground return bundles is

$$L_{loop} = i_t^T L_{mat} i_t = \tag{22}$$

$$= i_t^T \begin{bmatrix} L_{m1} & M_{m12} & \cdots & M_{m1n} \\ M_{m21} & L_{m2} & \cdots & M_{m2n} \\ \vdots & \vdots & \ddots & \vdots \\ \vdots & \vdots & \ddots & \vdots \\ M_{mn1} & M_{mn2} & \cdots & L_{mn} \end{bmatrix} i_t, \tag{23}$$

where i_t is a vector with the normalized current in each nanotube, and L_{mat} is the partial inductance matrix.

To more efficiently model the magnetic inductance, we have developed the *equivalent conductivity model*, which approximates the magnetic inductance of the discrete SWCNTs with one conductor that has the same dimensions as the nanotube bundle. The conductor can have multiple current carrying filaments to more accurately model the magnetic inductance as shown in Figure 13. To capture the relationship between the magnetic inductance and the ohmic resistance of the SWCNT bundle, we adjust the resistivity of the single conductor to obtain a new effective resistivity,

$$\rho_{eff} = \frac{\rho_t d_t^2}{P_m(1 - P_{mod})}, \tag{24}$$

where $P_{mod} = (\lfloor n_h/2 \rfloor d_t^2)/(w_b h_b)$ is a modifier that accounts for the hexagonal spacing of the nanotubes, d_t is the individual SWCNT diameter, and P_m is the probability that a given nanotube is metallic.

To evaluate the speed and accuracy of the proposed magnetic inductance model, we performed 2,500 simulations on the GSG configuration, which consists of a signal line placed between two parallel ground return paths [Mondal and Massoud 2005], for a wide-range of realistic bundle geometries for future process technologies as predicted by ITRS [2005]. The geometric parameters have the following ranges of values: $10\mu\text{m} \leq l_b \leq 5000\mu\text{m}$, $10d_t \leq w_b \leq 20d_t$, $d_t \leq h_b \leq 20d_t$, $0.1w_b \leq s_b \leq 1000w_b$, and $1\text{GHz} \leq f \leq 20\text{GHz}$ where f is the operating frequency for the interconnect; l_b is the length of the SWCNT bundle, and s_b is the edge-to-edge spacing between the signal and ground bundles. Note that, for this set of experiments, $d_t = 1\text{nm}$ and the nanotubes are assumed to be densely packed. Table 1 lists the maximum and mean errors of the equivalent conductivity model with respect to the discrete equivalent conductor model. The equivalent conductivity model with 5 filaments achieved a maximum error of 6.49 percent with typical errors of 0.80 percent. These errors will most likely be within the manufacturing tolerances of future SWCNT bundle interconnect technology. We also compare the magnetic inductance models to previous expressions that only model the self inductance for the SWCNTs in the bundle [Srivastava and Banerjee 2005], $L_{nomut} = L_{oneloop}/n_b$, which significantly underestimates the magnetic inductance of the bundle with typical errors of 94.3 percent.

Table I. Results for Magnetic Inductance Models

Magnetic Inductance Modeling Method	Maximum Error (%)	Mean Error (%)	CPU Time (s)
Equivalent Conductivity - 5 Filaments	6.49	0.80	0.64
Equivalent Conductivity - 3 Filaments	9.53	0.74	0.14
Equivalent Conductivity - 1 Filaments	354	3.04	0.09
Self Inductance Only	99.7	94.3	2.10^{-5}
Equivalent Conductor	N/A	N/A	27.7

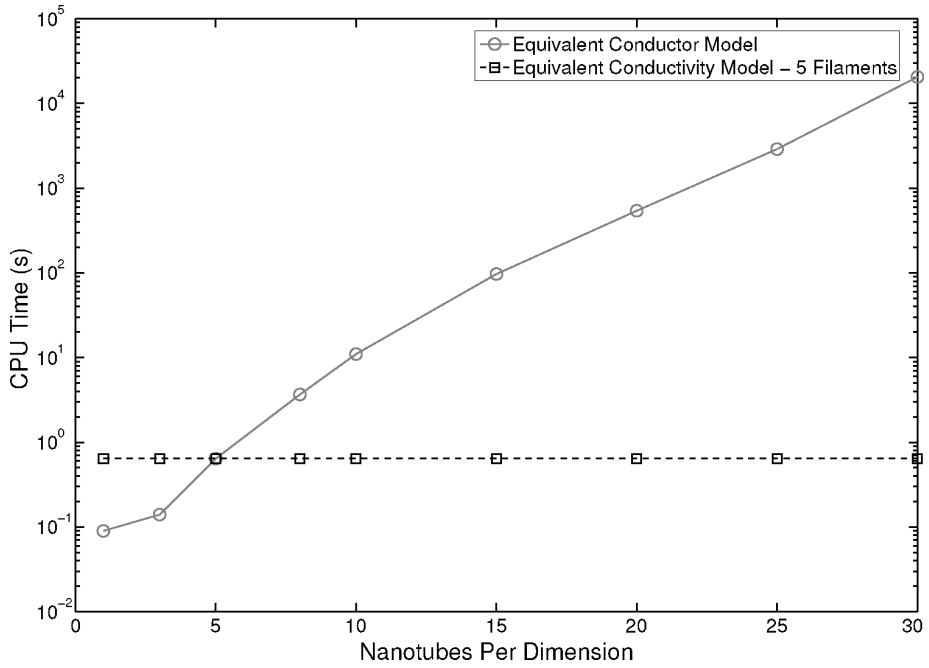

Fig. 14. CPU time as the number of nanotubes per dimension increases. The equivalent conductivity model provides a scalable solution as the number of nanotubes in a bundle increases.

In terms of CPU time, once the number of nanotubes per dimension in a bundle exceeds 30 for the GSG configuration, calculating the loop magnetic inductance using the equivalent conductor model becomes intractable as shown in Figure 14. For evaluating SWCNT bundles with a large number of nanotubes, which is necessary to reduce the overall resistance of the bundle, the equivalent conductivity model must be utilized. Therefore, the equivalent conductivity model provides a scalable solution for the magnetic inductance modeling of SWCNT bundles.

In order to apply the equivalent conductivity model to sparsely packed SWCNT bundles, we must determine what bundle size is required to make the random nanotube distribution statistically insignificant. We examined 80 nanotube bundle GSG configurations with the following geometric parameters: $10\mu\text{m} \leq l_b \leq 1000\mu\text{m}$, $10d_t \leq w_b \leq 20d_t$, and $0.1w_b \leq s_b \leq 1000w_b$. We assume that $h_b = w_b$ and $d_t = 1\text{nm}$. For the 80 simulated SWCNT bundle

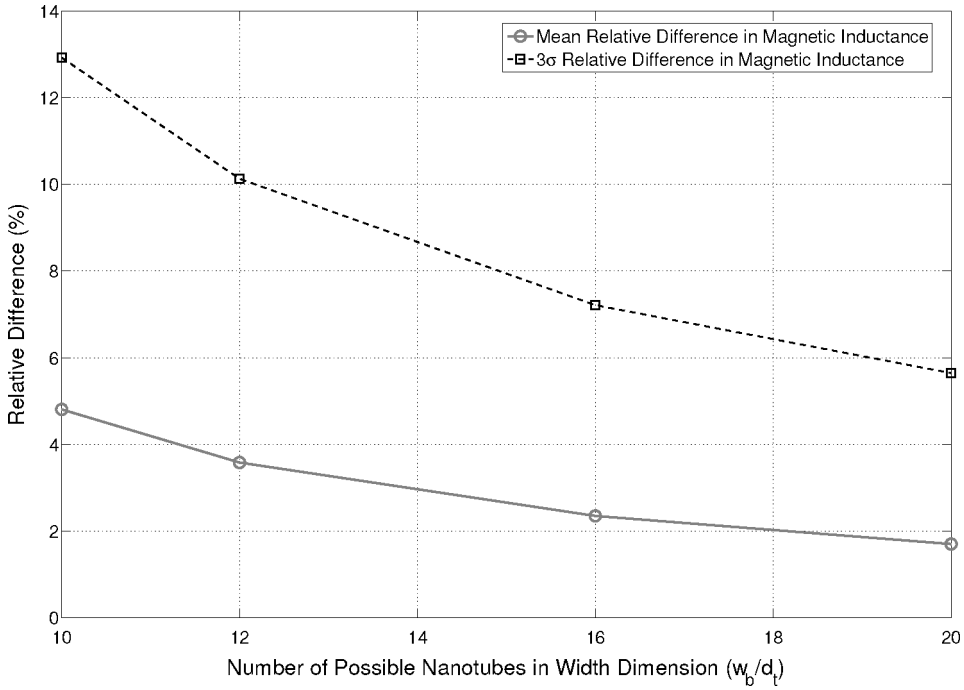

Fig. 15. Mean and $3 \cdot \sigma$ percentage relative difference in magnetic inductance between a random distribution of metallic carbon nanotubes ($P_m = 1/3$) and the deterministic model for SWCNT bundles versus w_b/d_t.

configurations, we performed a Monte Carlo simulation with 100 random sample points and with metallic nanotubes uniformly distributed within the bundle with probability 1/3. Figure 15 depicts the mean and $3 \cdot \sigma$ variation in magnetic inductance (L_{loop}). As the bundle width increases, the statistical variation in L_{loop} decreases due to the increase in the total possible number of SWCNTs in the bundle. Once w_b reaches $12d_t$, the $3 \cdot \sigma$ variation in L_{loop} is less than 10 percent.

3.5.2 *Kinetic Inductance.* In a metallic SWCNT, the kinetic inductance (L_k) is dependent on the net sum of the kinetic energy of left and right moving electrons in the nanotube, and, as a result, it is a per unit length quantity [Burke 2002]. For the kinetic inductance of individual metallic carbon nanotubes, conflicting experimental results have been reported in the literature. In Tarkiainen et al. [2001], kinetic inductance values of $0.1 - 4.2\text{nH}/\mu\text{m}$ were reported, while in Yu and Burke [2005], no kinetic inductance was observed for frequencies up to 10GHz. Until experimental research comes to a consensus on the impact of kinetic inductance in SWCNTs, it should be considered in circuit models for SWCNT bundle interconnect.

For one quantum channel, the theoretical expression for kinetic inductance [Burke 2002, 2003] is

$$L_{kone} = \frac{h}{2e^2 v_F} \approx 16\text{nH}/\mu\text{m}, \tag{25}$$

where h is Planck's constant, e is the charge of a single electron, and v_F is the Fermi velocity in graphite. Individual SWCNTs have two propagating channels due to the band structure of carbon with spin up or spin down electrons, which results in a total of four total channels per nanotube. Therefore, the kinetic inductance of an individual SWCNT [Burke 2002] is

$$L_k = \frac{L_{kone}}{4} \approx 4\text{nH}/\mu\text{m}. \tag{26}$$

Since kinetic inductance is dependent on the kinetic energy in the nanotube, there is no kinetic inductance analog to partial mutual magnetic inductance. Consequently, for SWCNT bundles, the kinetic inductance can be modeled as an additional self-inductance element [Majer et al. 2005; Guan et al. 1997; Nakazato and Okabe 1997; Sheen et al. 1991]. Equivalently, for a single SWCNT bundle, the kinetic inductance is defined as

$$L_{kb} = \frac{L_k}{n_b}. \tag{27}$$

For the GSG interconnect configuration, the total kinetic inductance depends on the total number of ground return paths (n_{grp}),

$$L_{kb} = \frac{(1 + 1/n_{grp})L_k}{n_b}, \tag{28}$$

assuming that the current is distributed equally in each ground return path and that all of the bundle cross-sectional dimensions are the same. Therefore, like resistance, kinetic inductance is substantially reduced as the number of nanotubes in the bundle is increased.

3.5.3 *Relative Impact of Magnetic and Kinetic Inductance.* The magnetic inductance depends on the size of the current loop in the GSG interconnect configuration, while the kinetic inductance is inversely proportional to the number of SWCNTs in the bundle ($\propto 1/n_b$). To determine the relative impact of kinetic inductance and magnetic inductance, we simulated GSG interconnect configurations with both densely and sparsely packed nanotubes with $2\text{nm} \leq w_b \leq 3\mu\text{m}$, $h_b = w_b$, $s_b = 2w_b$, and $l_b = 1\text{mm}$. Figure 16 displays the the inductance versus w_b for GSG SWCNT bundle interconnect configuration with the aforementioned geometric parameters. For the densely and sparsely packed bundles, the magnetic loop inductance and kinetic inductance have equal values when the bundle width reaches approximately 125nm and 375nm, respectively. The threefold increase in the equal inductive width corresponds to the 3x decrease in nanotube density in the sparsely packed bundles.

To determine at what bundle width magnetic inductance becomes important relative to kinetic inductance for more general configurations, we simulated 400 interconnect geometries in the GSG configuration with bundle spacing ranging from $0.1w_b$ to $1000w_b$ and per unit length kinetic inductance values for single SWCNTs ranging from $0.1\text{nH}/\mu\text{m}$ to $4\text{nH}/\mu\text{m}$. $4\text{nH}/\mu\text{m}$ corresponds to the theoretical values for the kinetic inductance of an individual nanotube obtained from Equation (26), while $0.1\text{nH}/\mu\text{m}$ is the smallest experimentally observed value of kinetic inductance [Tarkiainen et al. 2001]. We assumed that

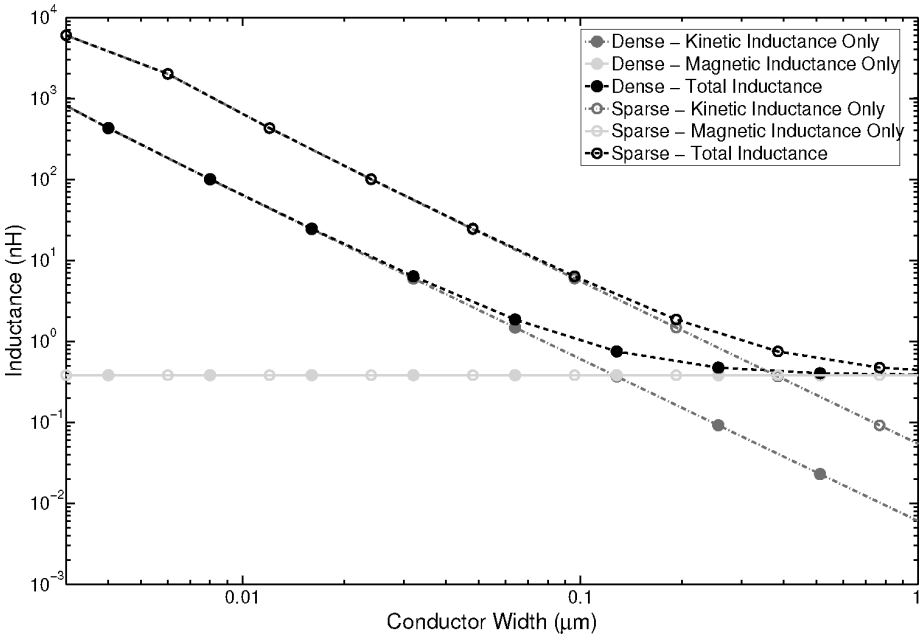

Fig. 16. Magnetic and kinetic inductance of a GSG interconnect configuration versus w_b for 1mm long densely and sparsely packed nanotube bundles. The spacing between the signal and ground bundles is assumed to be equal to the bundle width.

$w_b = h_b$, $d_t = 1$nm, $l_b = 1$mm and that the bundles consist of all metallic nanotubes.

Figure 17 displays the bundle width for which the total inductance of a GSG interconnect configuration has the following characteristics: (a) $L_m = 10L_k$ and (b) $10L_m = L_k$. The bundle separation has a large impact since the magnetic inductance increases with larger current loops. Therefore, the magnetic inductance has the largest effect when the signal and ground return bundles are spaced far apart from one another, and w_b is sufficiently large to reduce the per unit length contribution of the kinetic inductance. For bundle width values greater than the values displayed in Figure 17(a), the magnetic inductance is more than 10 times greater than the kinetic inductance. Depending on the per unit length value of the kinetic inductance and the spacing between the signal bundle and the ground bundles, the magnetic inductance dominates in bundles with w_b values ranging from 30nm to 400nm, which are within the range of typical interconnect width values for both local and global interconnect predicted by ITRS for future process technologies [ITRS 2005]. For bundle widths less than the values displayed in Figure 17(b), the kinetic inductance dominates the magnetic inductance which can occur for w_b between 3nm and 40nm. These width values correspond to local and intermediate-level interconnect in future process technologies.

The geometry of the interconnect greatly impacts the relative importance of magnetic and kinetic inductance. Figure 18 displays the number of SWCNTs in a nanotube bundle for which the total inductance of a GSG interconnect

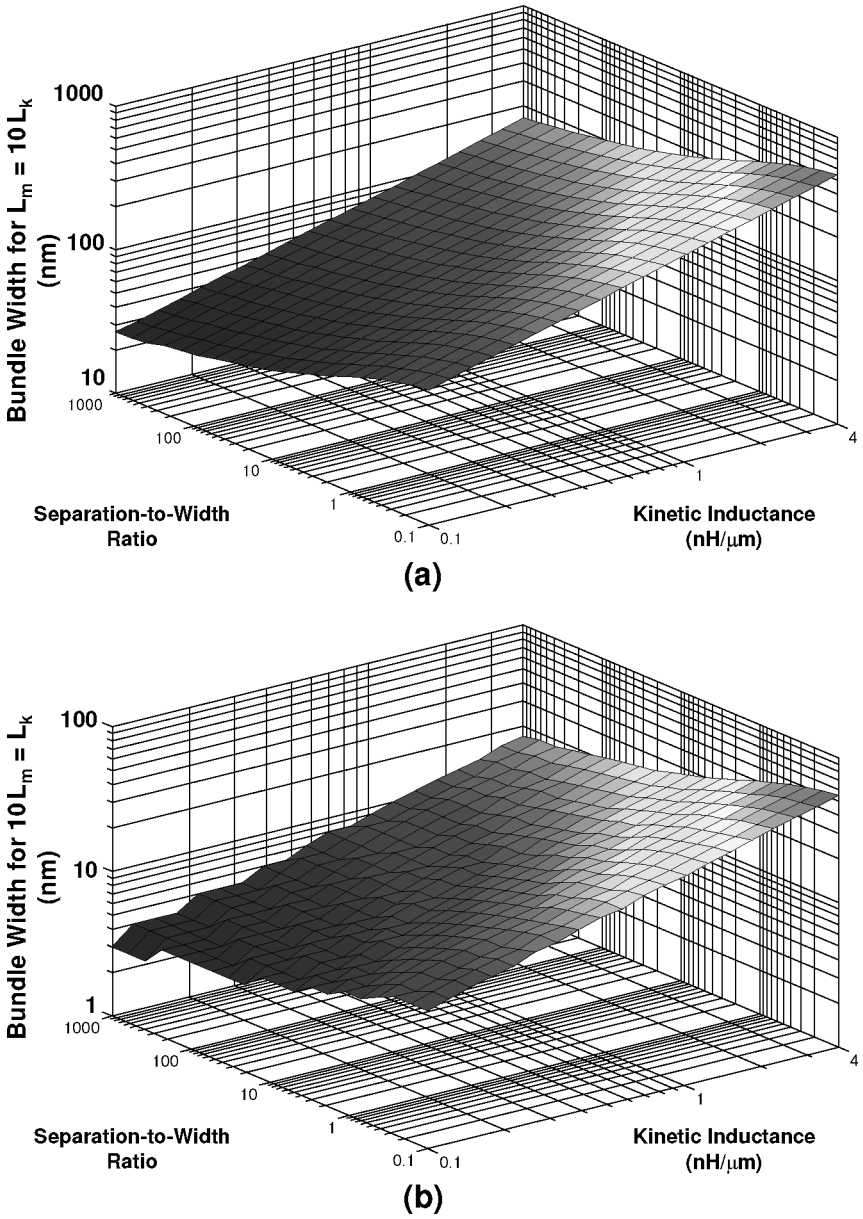

Fig. 17. Dense carbon nanotube bundle width values for which the total inductance of a GSG interconnect configuration has the following characteristics: (a) $L_m = 10L_k$ and (b) $10L_m = L_k$.

configuration has $L_m = L_k$, which is highly dependent on the separation-to-width ratio of the conductors and the per unit length kinetic inductance. The number of nanotubes required for $L_m = L_k$ ranges from 80 to 30,000. In Salahuddin et al. [2005], the number of channels predicted for $L_m = L_k$ was on the order of 10,000 which corresponds to a bundle with approximately 2,500

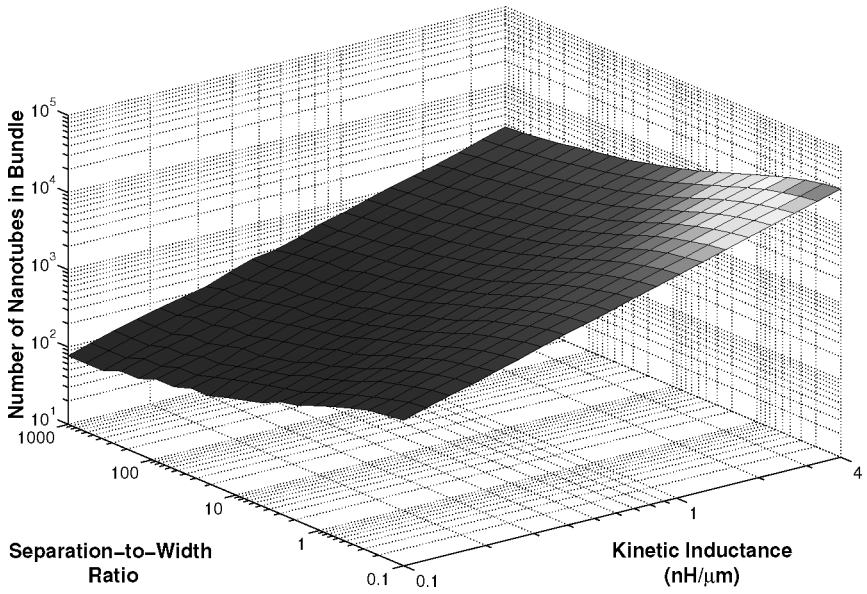

Fig. 18. Number of carbon nanotubes within a bundle for which the total inductance of a GSG interconnect configuration has $L_m = L_k$.

nanotubes. For the per unit length kinetic inductance value of 4nH/μm and the separation-to-width ratio of 10 assumed in Salahuddin et al. [2005], we predict that the number of channels necessary for $L_m = L_k$ is approximately 16,000, which corresponds to a bundle with 4,000 SWCNTs. Therefore, the theoretical results presented in Salahuddin et al. [2005] for a quantum wire with many propagating modes is on the same order of magnitude as the results predicted for SWCNT bundle interconnect.

Since the magnetic inductance primarily depends on the loops enclosed by the current in the signal bundle and associated ground return paths, it is relatively constant for typical variations in bundle cross-sectional geometry. The kinetic inductance per unit length for the SWCNT bundle depends on the number of nanotube in the bundle. Therefore, the results from Figure 17 can be scaled to approximately determine the relative impact of magnetic and kinetic inductance for the GSG configuration with different geometries and nanotube sparsity levels. For bundles with different individual nanotube diameters, the scaling of the bundle width in Figure 17 is proportional to the area increase of the nanotubes. For example, if $d_t = 2$nm, then the width should be scaled by a factor of four since $d_t = 1$nm for the width values displayed in Figure 17. Similarly, if the density of the metallic SWCNTs in the bundle is 1/3, then the width values displayed in Figure 17 should be scaled by a factor of three. Note that the length of the nanotube bundles (l_b) does not play a large role in the relative importance of L_m and L_k since increases in the length linearly increase both the area enclosed by the current loop in the GSG interconnect configuration and the total length of the interconnect lines. Since both the magnetic and kinetic inductance can have similar relative values for typical

interconnect geometries in future process technologies, modeling both of these phenomena is vital for evaluating SWCNT bundles in future VLSI interconnect applications.

4. PERFORMANCE AND RELIABILITY OF SWCNT BUNDLE INTERCONNECT

In this section, we characterize and analyze the performance and reliability of SWCNT bundles for VLSI applications using the interconnect model presented in Section 3.2. For individual local interconnect lines discussed in Section 4.1, we primarily focus on the current density in the individual nanotubes and its statistical variation due to the random number of metallic nanotubes in a bundle. For individual global interconnect lines, the delay and its statistical variation are the most important figures of merit as described in Section 4.2. In Section 4.3, we discuss the impact of inductance on SWCNT performance and reliability. Finally, in Section 4.4, we discuss the system-level implications of statistical variations in the number of metallic nanotubes for SWCNT interconnect. We extract the RLC model for the GSG configuration depicted in Figure 1 using the modeling techniques described in Section 3.2. We then perform HSPICE simulations on the extracted RLC netlist with driver parameters and load capacitances specified by ITRS [2005] to determine the delay and current density for the simulated SWCNT bundle configurations.

4.1 Local Interconnect Delay and Current Density

To evaluate the performance of SWCNT bundles for local interconnect, we simulated approximately 40,000 different configurations with varying individual nanotube diameters (d_t), nominal contact resistances (R_{cnom}), bundle length values (l_b), and probabilities that an individual nanotube is metallic (P_m). We use the process parameters from the 2015 node ($w_b = 25$nm) of ITRS 2005. We assume that the interconnect has a fanout of 5 gates when calculating the load capacitance and assume that the per unit length kinetic inductance for the nanotubes in a bundle is its predicted theoretical value, 4nH/μm. We assume the ITRS predicted clock frequency of 10GHz [ITRS 2005].

Figure 19(a) displays the maximum current density per nanotube within the bundle versus d_t and R_{cnom} for local interconnect with $P_m = 1/3$ and $l_b = 10\mu$m. The current density is the largest when the contact resistance is near its intrinsic value (R_i) and d_t is large. When $d_t = 2$nm and $R_i + R_c = 6.5$kΩ, the maximum current density is 3.5μA per nanotube, which is significantly lower than the 20μA maximum current density for nanotubes with 2nm diameters and also lower than the 5μA maximum current density for nanotubes with 1nm diameters. Figure 19(b) depicts the maximum current density per nanotube versus P_m and l_b for local interconnect with $d_t = 1.5$nm, $R_{cnom} = 20$kΩ, and $f = 10$GHz. The maximum current density per nanotube was 2.9μA for the range of values simulated which is also well below the limit for SWCNTs. Therefore, the nominal current density in SWCNT bundles in local interconnect does not pose a significant performance or reliability issue.

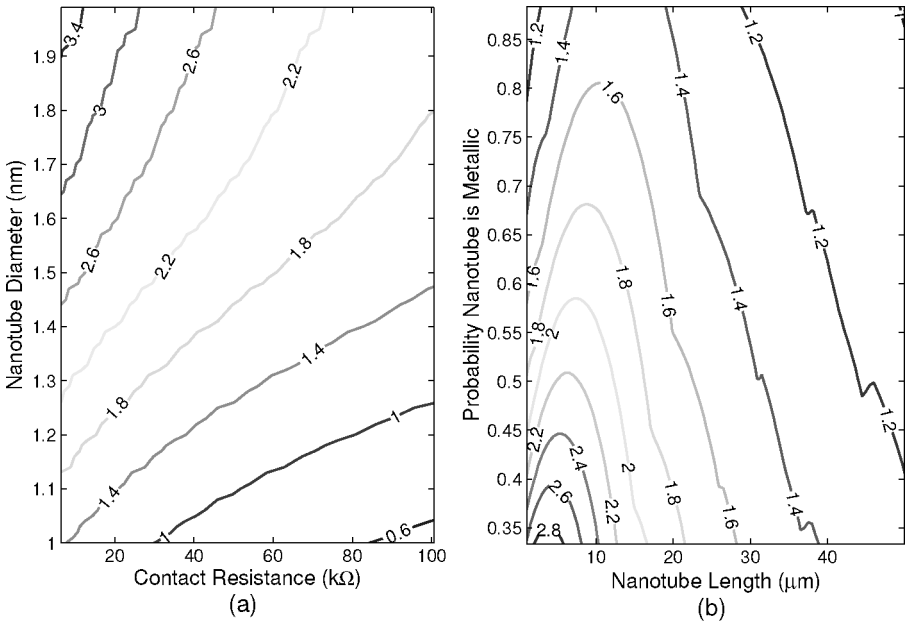

Fig. 19. Maximum current density per nanotube (μA) versus (a) d_t and R_{cnom} and (b) P_m and l_b for local interconnect.

In terms of delay, the SWCNT bundle performance relative to standard copper interconnect primarily depends on R_{cnom}, l_b, and P_m. Figure 20 depicts the percentage improvement in SWCNT bundle delay over standard copper interconnect versus P_m and l_b for local interconnect with $d_t = 1.5$nm and $R_{cnom} = 20$kΩ. Note that $d_t = 1.5$nm is optimum diameter for 22nm wide bundles as described in Section 3.3.4. For short interconnect length values, the standard copper interconnect has less delay than SWCNT bundle interconnect since the fixed contact resistance of the SWCNTs dominates the overall resistance. However, the negative resistive impact of the short SWCNT bundles is offset by the effective resistance of the interconnect driver circuit. For longer interconnect, the advantage of the improved ohmic resistance of SWCNT bundle interconnect over standard copper interconnect leads to an improvement in delay, especially in bundles where a large percentage of the nanotubes are metallic. Furthermore, the longer bundle length increases the overall interconnect resistance which reduces the relative impact of driver resistance. When $l_b > 100$nm, the resistance of the SWCNT bundle interconnect is primarily dominated by R_o, and, consequently, its relative performance with standard copper interconnect is not dependent on l_b.

To assess the reliability of local SWCNT bundle interconnect in relation to statistical variations in metallic nanotubes in the bundle, we performed Monte Carlo simulations on 300 SWCNT bundle geometries with varying bundle width values (10nm $\leq w_b \leq$ 40nm), individual nanotube diameters (1nm $\leq d_t \leq$ 2nm), and probabilities that an individual nanotube is metallic ($1/3 \leq P_m \leq 1$). Each Monte Carlo simulation has 200 random samples with the

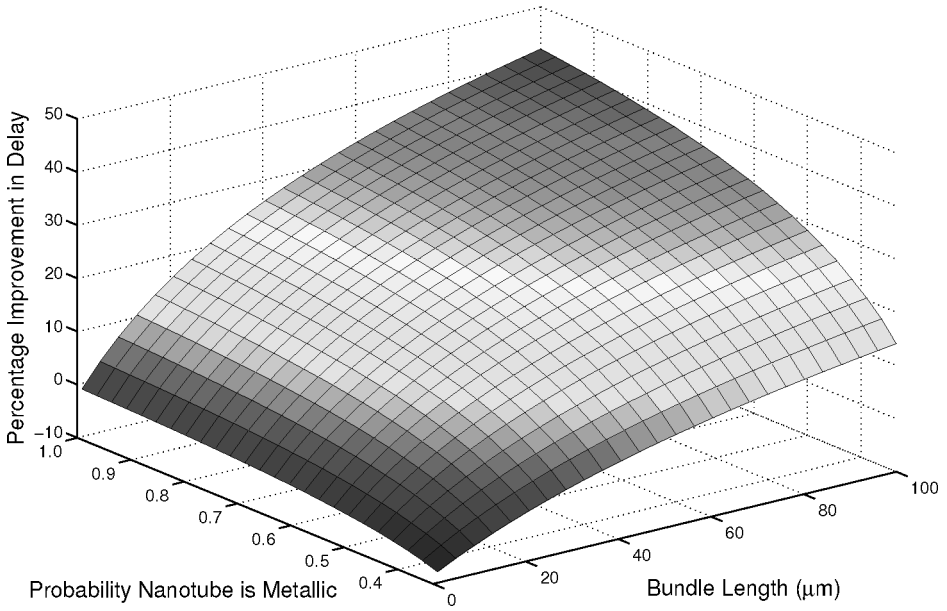

Fig. 20. Percentage improvement in SWCNT bundle delay over standard copper interconnect versus P_m and l_b for local interconnect.

number of metallic nanotubes within a bundle as the random variable. We found that the maximum 3-sigma current density is approximately 10% of the average value. Therefore, for the worst case current density of 3.5μA per nanotube, the probability that the current density is 5μA is essentially 0. Consequently, the variation in current density should not cause reliability problems for SWCNT bundle interconnect. We found that the statistical variation in delay is similar to the results we obtain for global interconnect in Section 4.2 which can impact performance and reliability in cases where the local interconnect delay is significant.

4.2 Global Interconnect Delay and Current Density

To evaluate the performance of SWCNT bundles for global interconnect, we simulated approximately 1,500 different interconnect configurations with varying d_t and P_m values. We make the same assumptions for load capacitance, kinetic inductance, and rise time as we did for the local interconnect simulations. We use the process parameters from the 2015 node ($w_b = 37.5$nm) of ITRS 2005 for global interconnect. We assume that the interconnect has a fanout of 5 gates when calculating the load capacitance and assume that the per unit length kinetic inductance for the nanotubes in a bundle is its predicted theoretical value, 4nH/μm. We find that the current density per nanotube is similar to the values obtained for the local interconnect cases and, therefore, does not pose a serious performance or reliability concern for global interconnect applications.

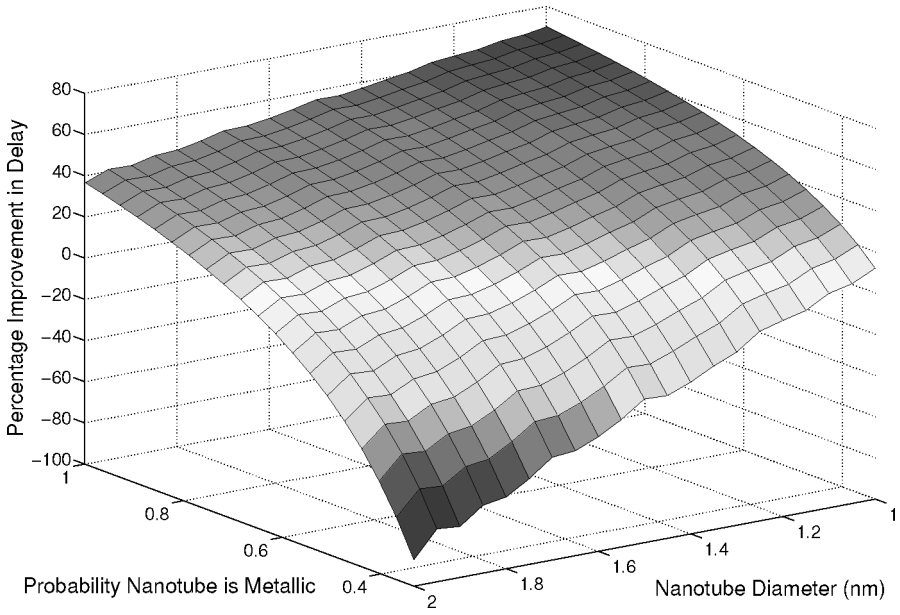

Fig. 21. Percentage improvement in SWCNT bundle delay over standard copper interconnect versus P_m and d_t for global interconnect.

Figure 21 displays the percentage improvement in SWCNT bundle delay over standard copper interconnect versus P_m and d_t for global interconnect with $l_b = 1\text{mm}$, $s_b = 2w_b$, and $R_{cnom} = 20\text{k}\Omega$. Both P_m and d_t have a large impact on SWCNT bundle delay, which primarily stems from the relative difference in resistance between SWCNT and copper technology depicted in Figure 4. For small individual nanotube diameters, the SWCNT bundle has less delay than standard copper interconnect for the full range of P_m values (1/3 to 1). However, for larger individual nanotube diameters, P_m will determine if SWCNT bundles offer a performance advantage over standard copper interconnect. Therefore, based on the delay results presented in Figure 21, developing techniques that control the diameter and chirality of SWCNTs will be vital for the effective utilization of SWCNT bundles for global interconnect applications [Cheung et al. 2002; Krupke et al. 2003; Zheng et al. 2003; McEuen and Park 2004; Lustig et al. 2005].

To assess the reliability of global SWCNT bundle interconnect in relation to statistical variations in metallic nanotubes in the bundle, we performed Monte Carlo simulations on 300 SWCNT bundle geometries with varying bundle width values ($10\text{nm} \leq w_b \leq 40\text{nm}$), individual nanotube diameters ($1\text{nm} \leq d_t \leq 2\text{nm}$), and probabilities that an individual nanotube is metallic ($1/3 \leq P_m \leq 1$). For global interconnect, we found that the delay can experience 3-sigma variations as high as 60% from the nominal value as depicted in Figure 22 for interconnect with $l_b = 1\text{mm}$, $s_b = 2w_b$, and $R_{cnom} = 20\text{k}\Omega$. As process technology scales downward and the typical bundle width values decrease, the variation in delay will have important performance

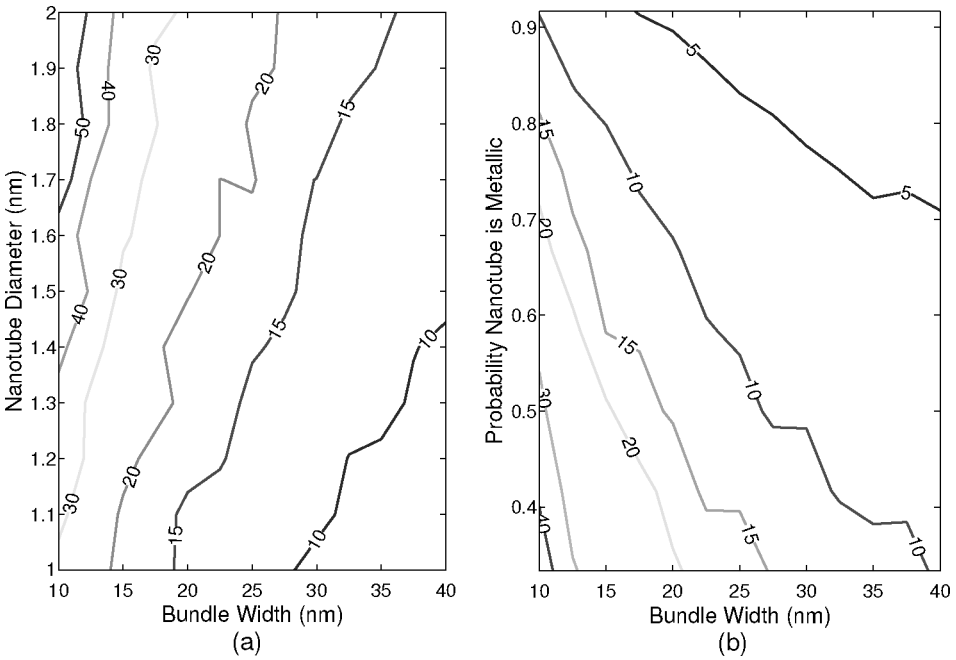

Fig. 22. 3-sigma percentage variation in SWCNT bundle delay versus (a) d_t and w_b and (b) P_m and w_b for global interconnect.

and reliability implications on system-level design which we analyze in Section 4.4.

4.3 Impact of Inductance on Delay in SWCNT Bundles

Given the importance of inductive effects for global interconnect in standard copper technology for both performance and reliability [Mondal and Massoud 2005; Massoud et al. 2002], we investigate the impact of inductance on SWCNT bundle interconnect. Figure 23 displays the percentage improvement in SWCNT bundle delay over standard copper interconnect versus w_b and the width-to-bundle separation ratio when inductive effects are taken into account. We assume that $P_m = 1$, $d_t = 1$nm, and $l_b = 1\mu$m. For bundle width values of less than 100nm and a width-to-bundle separation ratio between the signal and ground lines of less than 10, the performance improvement of the SWCNT bundles closely matches the improvement in resistance displayed in Figure 7. For interconnect with these geometries, the resistance dominates the overall impedance ($R \gg \omega L$). Therefore, the decreased resistance of the SWCNT bundles largely determines the delay enhancement. For larger SWCNT bundle width values which result in decreased resistance, or larger width-to-separation ratios which results in increased inductance, the relative improvement in the delay of the SWCNT bundle over standard copper interconnect decreases since the inductance begins to dominate the overall resistance ($R \ll \omega L$). Because the inductance of the SWCNT bundle is typically greater than or equal to

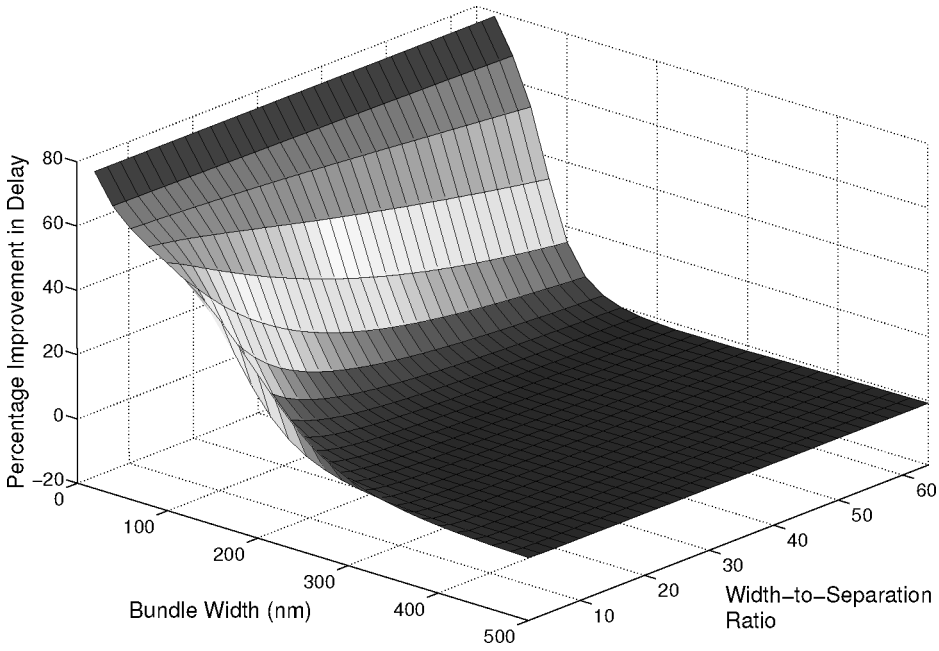

Fig. 23. Percentage improvement in SWCNT bundle delay over standard copper interconnect versus bundle width and the width-to-bundle separation ratio when inductive effects are taken into account.

that of standard copper interconnect, the SWCNT bundle interconnect loses its delay advantage over standard copper interconnect for large bundle width values. Note that for SWCNT bundles with large width values, the magnetic inductance dominates the kinetic inductance as displayed if Figure 17. Therefore, the impact of inductance on delay primarily stems from the magnetic inductance. The delay improvement when magnetic inductive effects are neglected, which is depicted in Figure 24, closely matches the improvement in resistance displayed in Figure 7. This confirms that the behavior displayed in Figure 23 is primarily due to the magnetic inductance.

Inductive effects can also cause voltage overshoot, which can damage transistors and cause logic failures [Mondal and Massoud 2005; Massoud et al. 2002]. Figure 25 displays the percentage voltage overshoot in SWCNT bundle interconnect over the nominal supply voltage versus bundle width and the width-to-bundle separation ratio when inductive effects are taken into account. Similar to the delay behavior, little or no overshoot occurs when $(R \gg \omega L)$. However, when inductive effects become significant, voltage overshoot can become an important issue that must be effectively controlled. Figure 26 depicts the absolute difference in percentage voltage overshoot between SWCNT bundle interconnect and standard copper interconnect over the nominal supply voltage. Since the resistance of SWCNT bundles is typically lower than that of standard copper interconnect, inductive effects impact the performance and reliability of SWCNT bundles with smaller dimensions than standard copper interconnect. Therefore, it is critical that certain steps be taken in the design of

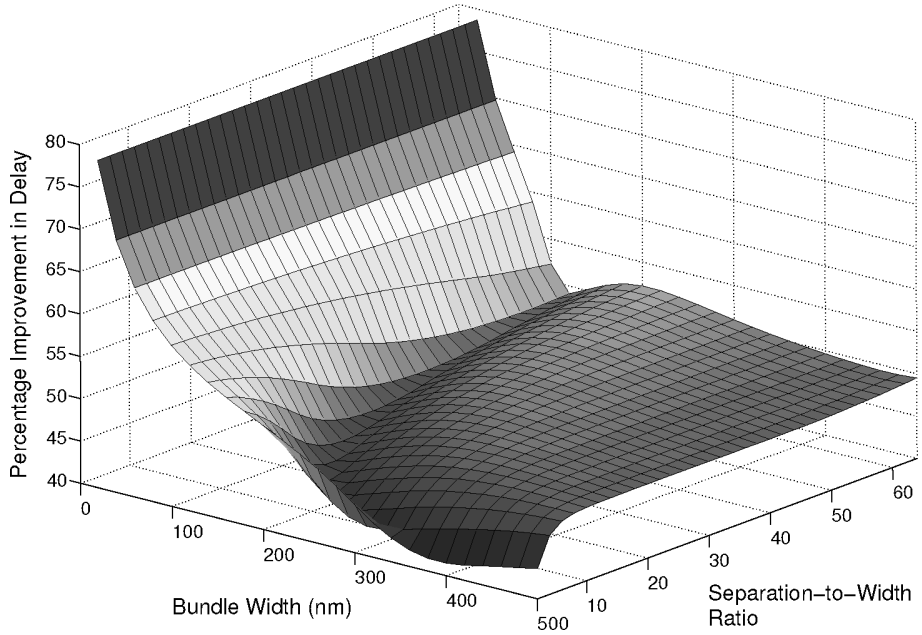

Fig. 24. Percentage improvement in SWCNT bundle delay over standard copper interconnect versus bundle width and the width-to-bundle separation ratio when magnetic inductance is not modeled.

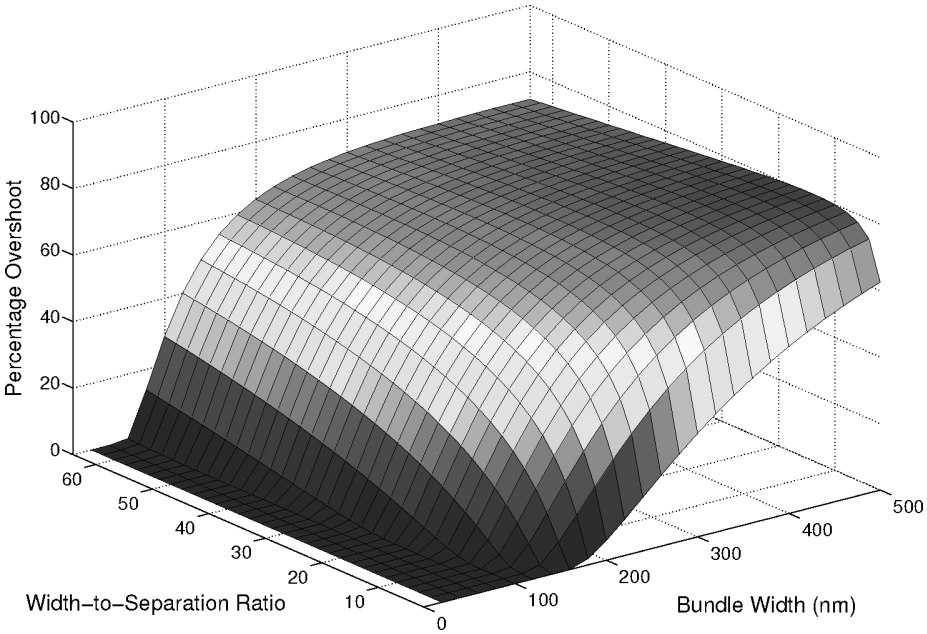

Fig. 25. Percentage voltage overshoot in SWCNT bundle interconnect over the nominal supply voltage versus bundle width and the width-to-bundle separation ratio when inductive effects are taken into account.

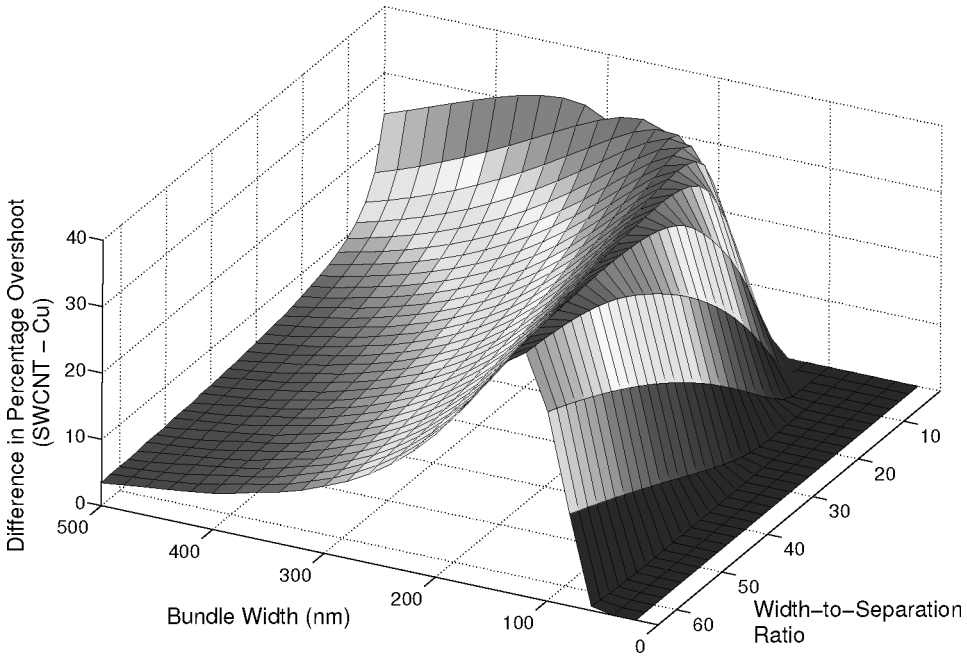

Fig. 26. Absolute difference in percentage voltage overshoot between SWCNT bundle interconnect and standard copper interconnect over the nominal supply voltage versus bundle width and the width-to-bundle separation ratio when inductive effects are taken into account.

SWCNT bundle interconnect systems to reduce the impact of inductive effects [Massoud et al. 2002].

4.4 System-Level Reliability of SWCNT-Based Interconnect

The performance and reliability of global SWCNT interconnect is impacted by statistical variations in the delay. Figure 27 displays the probability of a timing violation for an individual global SWCNT bundle interconnect versus w_b and the additional percentage delay that the design can handle without having a timing violation for the process and geometric parameters described in Section 4.2. The individual nanotube diameter was 1.5nm. Note that global interconnect in the 2015 and 2020 nodes of ITRS 2005 have a wire width values of 37.5nm and 21nm, respectively. The individual delay distributions for a fixed interconnect configuration are Gaussian. For individual SWCNT bundles used in global interconnect, approximately 10 percent slack in nominal delay causes a 1 percent timing violation rate for individual SWCNT bundles when $w_b =$ 37.5nm. For $w_b = 21$nm, at least 15 percent slack in nominal delay is needed to produce less than a 1 percent timing violation rate when the number of metallic nanotubes within a SWCNT bundle has statistical varaition. As shown in Figure 28 for nanotube bundles with $w_b = 22$nm, d_t can also impact the failure rate for SWCNT bundle interconnect. Bundles with larger d_t values have a small number of nanotubes, and, therefore, the variance of the possible delay values increases.

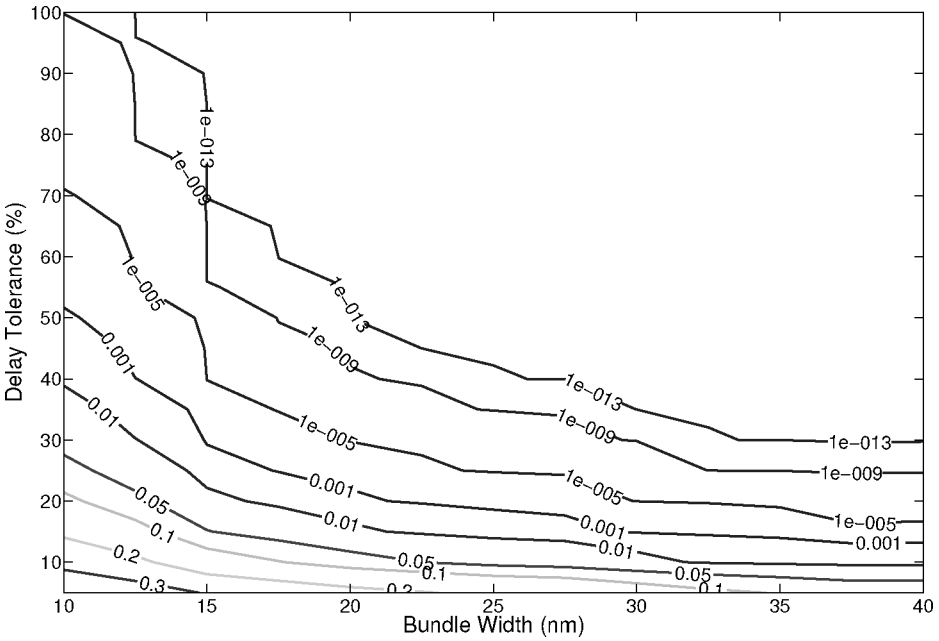

Fig. 27. Probability of a timing violation for an individual SWCNT bundle interconnect versus w_b and the additional percentage delay that the design can handle without having a timing violation.

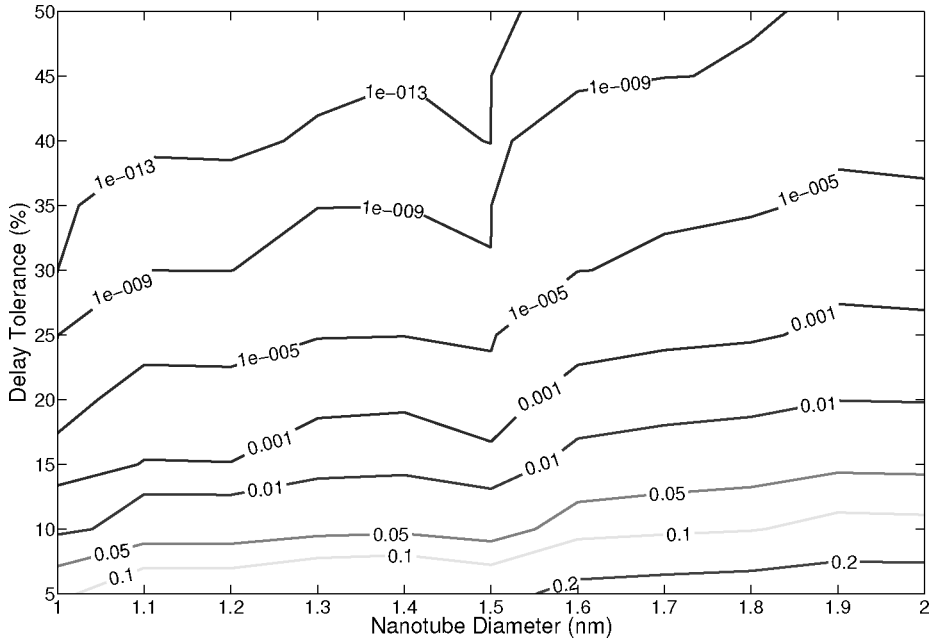

Fig. 28. Probability of a timing violation for an individual SWCNT bundle interconnect versus d_t and the additional percentage delay that the design can handle without having a timing violation.

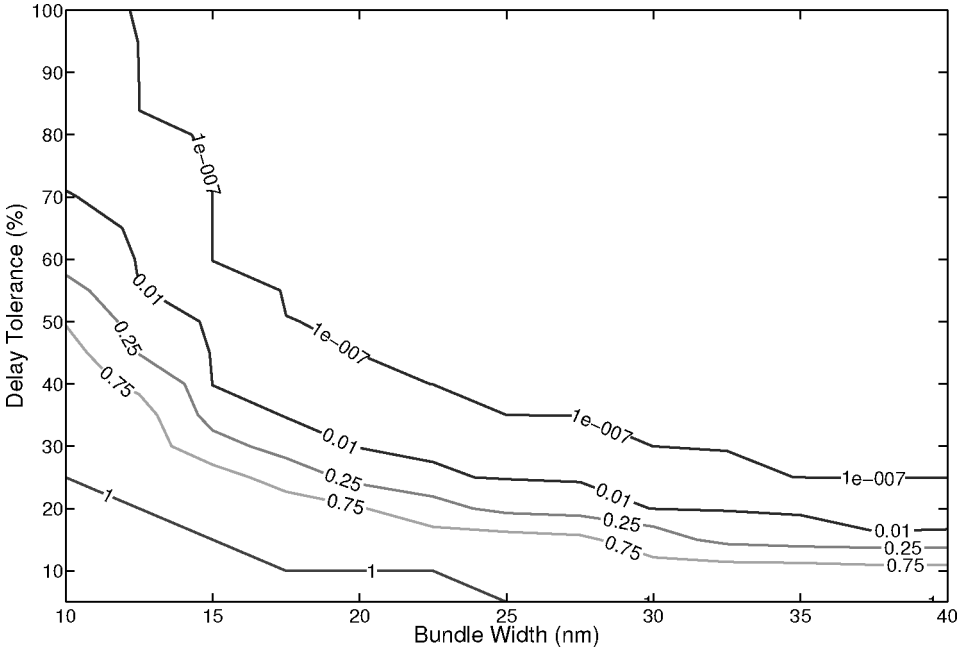

Fig. 29. Probability of a timing violation for 1,000 SWCNT bundle interconnect lines versus w_b and the additional percentage delay that the design can handle without having a timing violation.

Since the time required to cross large portions of the chip is significantly larger than the clock period in current and future process technologies, retiming and buffer insertion cause the delay of many of the global interconnect lines to be close to the critical path delay [Bai et al. 2002]. Statistical variation in delay for global interconnect lines with delay values near the critical path delay can cause serious performance and reliability problems. Therefore, in a particular design, thousands of global interconnect lines must meet the chip timing requirements. According to the 2015 node of ITRS 2005, the total length of local and intermediate lines will be approximately 4000m/cm^2. If the global interconnect lines have an average length of 1mm and a similar density, up to 1,000,000 total global interconnect lines are possible in future VLSI designs.

Assuming the timing violation percentages for individual global SWCNT bundles depicted in Figure 27, Figure 29 displays the probability of a timing violation on one SWCNT interconnect line for 1,000 total global SWCNT bundle interconnect lines versus w_b and the additional percentage delay that the design can handle without having a timing violation. Similarly, Figure 30 displays the probability of a timing violation for 1,000 total global SWCNT bundle interconnect lines for various d_t values. We also calculated the probability of a timing violation for 1,000,000 total global SWCNT bundle interconnect lines. For $w_b = 37.5$nm, a 1% failure rate occurs when the timing variation tolerance is 17% and 21% for 1,000 and 1,000,000 global SWCNT bundle interconnect lines, respectivly. For $w_b = 21$nm, a 1% failure rate requires an increased timing variation tolerance of 29% and 38% for 1,000 and 1,000,000 global SWCNT

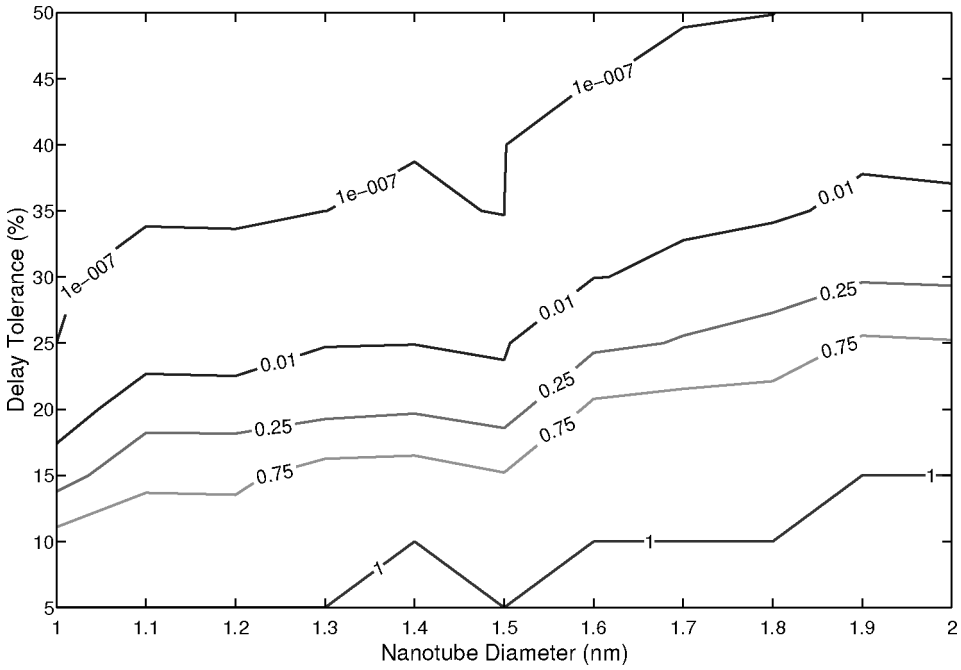

Fig. 30. Probability of a timing violation for 1,000 SWCNT bundle interconnect lines versus d_t and the additional percentage delay that the design can handle without having a timing violation.

bundle interconnect lines, respectivly. Therefore, to ensure reasonable reliability and yield, 20–40% additional delay tolerance must be designed into systems when utilizing SWCNT bundles for global interconnect in future process technologies. This additional delay tolerance will most likely come at the expense of system performance. However, standard copper interconnect will also experience significant variation in delay due to resistance variation caused by multi-conductor pattern erosion and dishing within individual conductors due to chemical-mechanical polishing, which can have a large impact on conductor thickness with 3-sigma variations of up to 35% for future process technologies [Nassif 2001; Agarwal et al. 2004; ITRS 2005]. Given the fact that standard copper interconnect will also have significant statistical variation in delay in future process technologies and that SWCNT nanotube interconnect can offer up to 70% performance improvement over standard copper interconnect when $w_b = 37.5$nm as depicted Figure 21, SWCNT bundles can offer a viable alternative to standard copper interconnect, depending on the geometric and process parameters.

5. CONCLUSION

In this article, we provide a comprehensive analysis of the performance and reliability of bundles of statistically distributed metallic SWCNTs for both local and global interconnect in future VLSI applications. We develop a scalable equivalent circuit model that captures the statistical distribution of individual

metallic nanotubes, while accurately incorporating recent experimental and theoretical results. The results indicate that SWCNT interconnect bundles can provide significant improvement in delay over traditional copper interconnect, especially for global interconnect applications, depending on the interconnect geometry, contact resistance, fanout, individual nanotube diameter, and probability that a given nanotube in the bundle is metallic. Since nanotube interconnect can have less resistance and more inductance than copper interconnect, employing design techniques to mitigate the impact of inductance for SWCNT-based global interconnect will be crucial [Massoud et al. 2002]. Furthermore, like scaled copper interconnect, the statistical variation in delay in SWCNT bundles can lead to reliability issues in future process technology. Consequently, manufacturing and fabrication technology will be crucial for the realization of nanotube-based interconnect.

The results point to important manufacturing challenges for nanotube interconnect that must be addressed. The individual nanotube diameter and the probability that a given nanotube in the bundle is metallic both have a large role in determining the SWCNT interconnect performance. Controlling these two properties will require more sophisticated methods for manufacturing nanotubes with a given chirality, which determines the diameter of the nanotube and if it is semiconducting or metallic. Techniques such as alternating current dielectrophoresis [Krupke et al. 2003], sequence-dependent DNA assembly [Zheng et al. 2003], and ion-exchange chromatography [Lustig et al. 2005] have shown the potential to increase the proportion of metallic nanotubes. Another obstacle to the realization of SWCNT-based interconnect solutions is the cost effective fabrication and integration of carbon nanotubes in future integrated circuit manufacturing processes which remains an important area of research [Liebau et al. 2005; Avouris et al. 2003; Cassell et al. 2004]. While many factors will ultimately contribute to the realization of SWCNT bundle interconnect, the results indicate that SWCNTs have the properties to potentially be a viable replacement for copper interconnect, especially for global interconnect, in many high performance VLSI applications as process technology scales.

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