Carbon Nanotube Transistor Compact Model for Circuit Design and Performance Optimization

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In this paper, we describe the development of the Stanford University Carbon Nanotube FET (CNFET) Compact Model. The CNFET Model is a circuit-compatible, compact model which describes enhancement-mode, CMOS-like CNFETs. It can be used to simulate both functionality and performance of large-scale circuits with hundreds of CNFETs. To produce realistic and relevant results, the model accounts for several practical non-idealities such as scattering in the near-ballistic channel, effects of the source/drain extension region, and charge-screening for multiple-nanotube CNFETs. The model also includes a full transcapacitance network for more accurate transient and AC results. The Stanford University CNFET Model is implemented in both HSPICE macro language and VerilogA. The VerilogA implementation shows speedups of roughly 7x∼15x over HSPICE. Applications of the model suggest that n- and p-CNFETs will have 6x and 13x speed advantage over Si n- and p-MOSFETs respectively at the 32nm node, and that a CNT density of 250 CNTs/um is ideal for multiple-nanotube gates. Such a compact CNFET model will be absolutely essential in ushering in the Design Era of CNFET circuits as carbon nanotube technology outgrows its "science discovery" phase.

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1. INTRODUCTION

As semiconductor devices and ICs continue to scale into the Nanoscale Era, the semiconductor industry faces several increasingly difficult challenges, of which the most notable are: (1) continued improvement in power and performance, (2) device fabrication and the control of variations, and (3) integration of a diverse set of devices and materials [Wong et al. 2006; Wong 2002; Skotnicki et al. 2005]. As several Si CMOS limitations projected by the International Technology Roadmap for Semiconductors [ITRS 2006] remain unsolved, nanotechnology has been put forward as the key to overcoming these challenges. In particular, carbon nanotube field effect transistors (CNFETs), due to its excellent CV/I device performance [Guo et al. 2004; Wong et al. 2003], have become a very promising extension to Si CMOS well into the Nanoscale Era.

While many promising experimental results have been published in the recent years establishing the technical merits of the CNFET as a future technology, most of these experiments focus only on scientific discovery and only investigate a single carbon nanotube (CNT) or a stand-alone device. Scientific discovery aims to explore and explain materials and phenomena, but cannot move CNFET technology forward into the design phase. In order to develop CNFETs into a viable, widely-adopted IC technology, methods and tools for the design, not just discovery, of CNFET devices and circuits must be developed.

Device models and design tools with the appropriate level of abstraction are required to enable the design of a useful system with CNFETs. In this paper, we discuss the development of the Stanford University CNFET Model, a circuit-compatible, compact model, to aid in circuit design. Using this model, we were able to obtain important design information for both device design, such as the optimal number of CNTs per device, and circuit design, such as the effects of various fabrication variations on gate delay.

This article aims to present and describe the CNFET model, which is described in full detail in Deng and Wong [2007a, 2007b, 2007c], with the goal of providing an understanding of the capabilities and assumptions of the model on a high level. The article then builds upon this understanding to explore the applications and results of the model, as well as its implications for CNT device and circuit design. This article is organized as follows. In Section 2, the CNFET Model, with its assumptions and approximations, and implementation are described. Section 3 presents the validation of the model through simulations and experiments, and Section 4 compares the VerilogA speedup over the alternative HSPICE implementation. Several applications are illustrated in Section 5, demonstrating the capabilities of the model, and lastly Section 6 presents a final summary.

2. THE CNFET COMPACT MODEL

In order to simulate a practical circuit with possibly hundreds of CNFETs, a compact model is necessary. The compact model must contain the essential device physics required for accurate simulation, yet be simple enough to allow the simulation of a large scale circuit within a reasonable time. There have been a few models proposed in the recent years to project CNFET performance

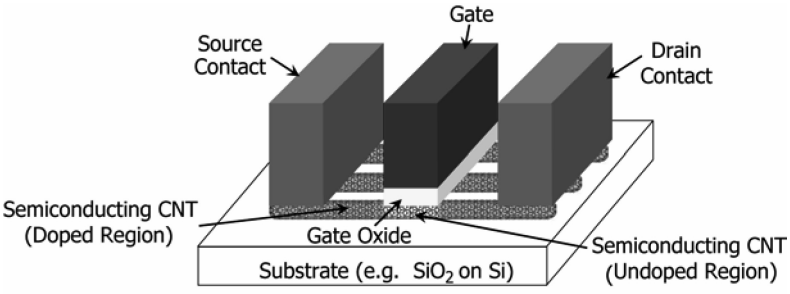

Fig. 1. Device structure of CNFET modeled.

[Natori et al. 2005; Guo et al. 2002; Raychowdhury et al. 2004; Dwyer et al. 2004; Balijepalli et al. 2007]. They have helped advance CNFET modeling greatly and provide a foundation upon which to build. Many use either one or more lumped static gate capacitances or treat only ballistic transport; but such simplifications can significantly affect the results for transients and circuit dynamic performance. In addition, the integral function used in Natori et al. [2005] and Guo et al. [2002] requires intensive calculations and can be hard to implement in a circuit simulator such as HSPICE. On the other hand, the polynomial curve fitting approach in Raychowdhury et al. [2004] improves simulation time, but makes simulation of CNFETs with various different device parameters unintuitive and inconvenient. The coaxial structures or simple planar structures used in Natori et al. [2005], Guo et al. [2002], Dwyer et al. [2004], and Balijepalli et al. [2007] differ significantly from realistic/feasible CNFET structures and cannot take into account the CNT-to-CNT charge screening effects when there are multiple-CNTs per gate. The Stanford University CNFET Model aims to improve upon the above by considering a realistic, circuit-compatible CNFET structure and by including practical device nonidealities—parasitics, charge-screening effects, Schottky-barrier effects at the contacts, doped source-drain extension regions, scattering (nonideal near-ballistic transport), back-gate (substrate bias) effect, . . . etc. The model also includes a full transcapacitance network for more accurate transient and dynamic performance simulations.

2.1 Overview of the Model

The Stanford University CNFET Model is a circuit-compatible, compact model which describes enhancement-mode, CMOS-like CNFETs [Deng and Wong 2007a; Deng and Wong 2007b], scalable down to 10nm channel lengths. It obtains improved accuracy by accounting for several practical nonidealities, such as scattering, effects of the doped source/drain extension region, and inter-CNT charge screening effects. In addition, by including a full transcapacitance network, it produces better predictions of the dynamic performance and transient response. Figure 1 shows the modeled CNFET device structure. The CNFET modeled is an enhancement-mode, CMOS-like CNFET. The semiconducting, intrinsic CNT region under the gate acts as the channel and the heavily doped CNT regions outside the gate form the source/drain extension regions. (The CMOS-like CNFET was chosen for modeling over the Schottky Barrier

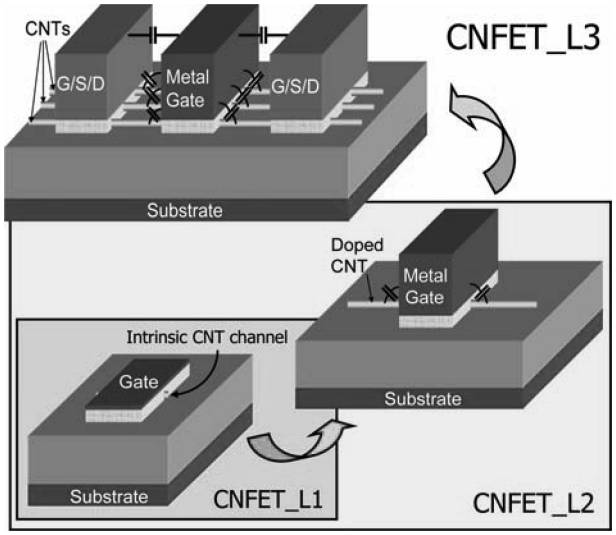

Fig. 2. Three-level hierarchy of the CNFET model.

controlled CNFET due to its superior performance and fabrication feasibility [Chen et al. 2005; Deng and Wong 2007a].)

The model is organized hierarchically into three levels, each dealing with a different part of the entire modeling problem (Figure 2). The first level (CNFET_L1) is the core of the model and describes the intrinsic CNT region that forms the channel under the gate. Several non-idealities, such as near-ballistic transport (versus ideal ballistic transport) and parasitics, are taken into account here. The second level (CNFET_L2) builds on top of the first level to include the source/drain extension regions. The parasitic resistances and capacitances from the source/drain extension region can significantly affect the magnitude of the CNFET drive current. The third and last level (CNFET_L3) then builds upon CNFET_L2 and completes the device model. Here, it enables the modeling of multiple CNTs under the same gate and accounts for CNT-to-CNT charge screening effects.

The three levels of the hierarchy interact with each other by passing critical parameters from the higher level down to the lower level. For example, charge-screening effects accounted in CNFET_L3 affect parameters used to simulate the intrinsic channel region in CNFET_L1 by passing down information regarding charge screening to CNFET_L1; similarly, information regarding metal contacts is passed down to CNFET_L2 to correctly calculate the Schottky-barrier effects.

The following sections describe the three levels in the model, and extensive derivations, equations, and discussions can be found in Deng and Wong [2007a, 2007b, 2007c].

2.2 CNFET Model Level 1 (CNFET_L1)

CNFET_L1 has two main parts. It includes 3 dependent current sources to model the intrinsic channel current and it also includes a 5-capacitor

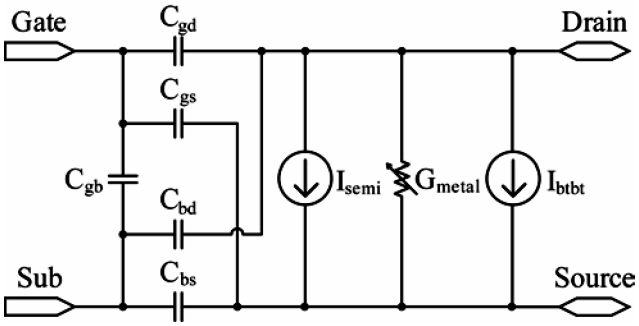

Fig. 3. Equivalent circuit for the level 1 model (CNFET_L1).

transcapacitance network to model the AC response. The equivalent circuit of the Level 1 model is shown in Figure 3.

CNFET_L1 models the intrinsic CNT channel current by considering three contributing sources: (1) thermionic current contributed by the semiconducting subbands, I_{semi}; (2) band-to-band tunneling (BTBT) current through the semiconducting subbands, I_{BTBT}; and (3) current contributed by the metallic subbands, $I_{metallic}$ (if any). Each of these contributions is discussed below.

For a CMOS-like n-type CNFET, the hole current is usually negligible compared to the electron current for semiconducting subbands. This is because in the heavily doped source/drain extension regions (n-type), the hole carrier density is negligible compared to the electron carrier density. The opposite is true for p-type CNFETs. Thus, to simplify computation, the model only includes electron current for calculating I_{semi}. (For the remainder of this article, we present the model equations and derivations for an n-type CNFET, as equations for a p-type CNFET can be similarly derived. The model implementation includes both n-type and p-type CNFETs.) The total I_{semi} is the sum of the current components flowing from the drain to the source ($+k$ components) minus the current components flowing from the source to the drain ($-k$ components) summed over all subbands and substates [Deng and Wong 2007a]:

$$I_{semi}\left(V_{ch,DS}, V_{ch,GS}\right) = 2\sum_{m=1}^{k_m}\sum_{l=1}^{k_l}\left[T_{LR}\cdot J_{m,l}(0, \Delta\Phi_B)|_{+k} - T_{RL}\cdot J_{m,l}(V_{ch,DS}, \Delta\Phi_B)|_{-k}\right] \quad (1)$$

$V_{ch,DS}$ and $V_{ch,GS}$ denote the Fermi level near the source-side of the channel. The factor of 2 is from the double degeneracy of the subbands. M is the number of subbands and L is the number of substates, so that k_m denotes the wave-number of the mth subband in the circumferential direction and k_l denotes the wave-number of the lth substate in the axial direction. T_{LR} and T_{RL} are the transmission probabilities in each direction, and $J_{m,l}$ is the current contribution from the (m,l) substate. Lastly, $\Delta\Phi_B$ is the change in the channel surface potential due to an applied bias.

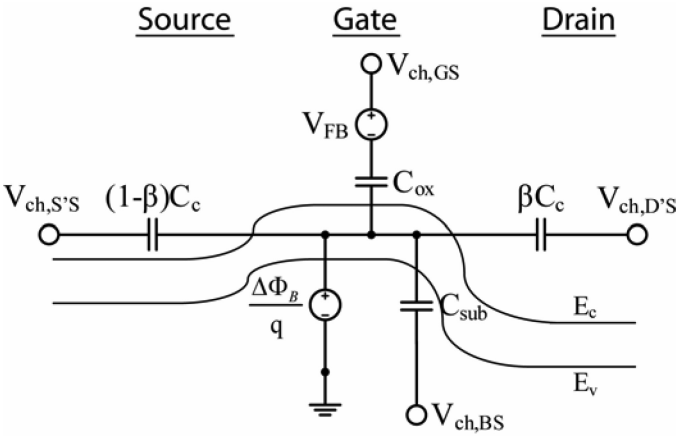

Fig. 4. Electrostatic capacitance model superimposed on the energy band diagram. Charge conservation is used to find the change in the channel surface potential due to a change in bias ($\Delta\Phi_B$).

For short channel devices ($L_g < 100$nm), Equation (1) is used. But for long channel devices ($L_g > 100$nm), the wave-number in the axial direction (k_l) approaches continuous values, so the inner summation in (1) can be approximated with an integral and evaluated to give

$$I_{semi}\left(V_{ch,DS}, V_{ch,GS}\right) \approx \frac{4q^2}{h} \sum_{\substack{k_m \\ m=1}}^{M} T_m \cdot \left[V_{ch,DS} + \frac{kT}{q} \ln\left(\frac{1 + e^{\frac{E_{m,0} - \Delta\Phi_B}{kt}}}{1 + e^{\frac{E_{m,0} - \Delta\Phi_B + qV_{ch,DS}}{kT}}} \right) \right], \quad (2)$$

where $E_{m,l}$ is the carrier energy of the (m, l) sub-state relative to the intrinsic Fermi level (so $E_{m,0}$ is the half band gap of the mth sub-band). Equation (2) has also made use of the assumption that $T_{LR} = T_{RL} = T_m$ (i.e., the transmission probabilities are symmetric and equal to a value T_m).

Perhaps the most important parameter in (1) and (2) is $\Delta\Phi_B$. In order to correctly predict the current and dynamic performance, $\Delta\Phi_B$ must be computed accurately. Unlike several current approaches to calculating $\Delta\Phi_B$, the Stanford CNFET Model finds $\Delta\Phi_B$ by applying the law of charge conservation to the electrostatic capacitances instead of using the constant quantum capacitance approach. This results in a much more accurate computation of $\Delta\Phi_B$ as a function of the applied bias. Figure 4 shows the electrostatic capacitance model superimposed on the energy band diagram for a CNFET. $V_{ch,GS}$ ($V_{ch,BS}$) is the potential difference from the gate (bulk/substrate) to the source-side channel region; and $V_{ch,S'S}$ ($V_{ch,D'S}$) is the potential difference from the external source (drain) outside the channel region to the source-side channel region. C_{ox} is the electrostatic coupling capacitor from the gate to the channel; C_{sub} is the capacitance between the channel and substrate; and $(1 - \beta)C_c$ and βC_c are the

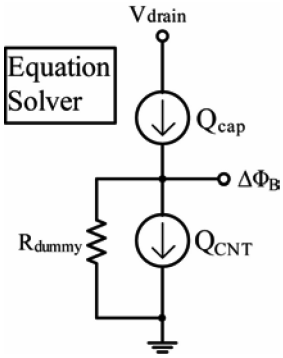

Fig. 5. Equation solver circuit used to implicitly solve for $\Delta\Phi_B$.

coupling capacitances from the channel to the source and drain respectively (the total channel to source/drain capacitance is C_c) [Deng and Wong 2007a]. Note that β and C_c are fitting parameters in the model. Charge conservation then dictates that the charge induced by the electrodes (Q_{cap}) is equal to the charge induced on the CNT surface (Q_{CNT}):

$$Q_{cap} = Q_{CNT}, \tag{3}$$

where

$$\begin{aligned} Q_{cap} \;=\; & C_{ox}\left(V_{ch,GS} - V_{FB}\right) + C_{sub}V_{ch,BS} + \beta C_c V_{ch,D'S} + (1-\beta)C_c V_{ch,S'S} \\ & - (C_{ox} + C_{sub} + C_c)\,\frac{\Delta\Phi_B}{q} \end{aligned} \tag{4}$$

and

$$Q_{CNT} = \frac{4q}{L_g} \sum_{\substack{k_m \\ m=m_0}}^{M} \sum_{\substack{k_l \\ l=0}}^{L} \left[\frac{1}{1 + e^{\frac{\left(E_{m,l} - \Delta\Phi_B\right)}{kT}}} + \frac{1}{1 + e^{\frac{\left(E_{m,l} - \Delta\Phi_B + qV_{DS}\right)}{kT}}} \right]. \tag{5}$$

m_0 is 1 for semiconducting CNTs, and 0 for metallic CNTs (i.e., the metallic subband is not included for semiconducting CNTs and is included for metallic CNTs).

Equations (3)–(5) must be solved to find $\Delta\Phi_B$; however, there is no explicit, closed-form solution for $\Delta\Phi_B$ given these expressions for Q_{cap} and Q_{CNT}. Approximations can be made to arrive at a closed-form solution, but accuracy will be compromised. Instead, we implement the model to compute $\Delta\Phi_B$ iteratively from these equations. Using constructs available in circuit simulation tools such as VerilogA (and HSPICE), $\Delta\Phi_B$ can be found very quickly (versus writing explicit code to perform the iteration). The technique is illustrated in Figure 5, which uses an "Equation Solver Circuit" to solve for $\Delta\Phi_B$. Two voltage-dependent current sources, with current expressions equal to the expressions of Q_{cap} and Q_{CNT} above, are placed in series. They are both dependent on a dummy voltage which plays the role of $\Delta\Phi_B$ in the equations. R_{dummy}

in Figure 5 is a very large resistor used to aid convergence. The two current sources are forced to have equal currents (and thus $Q_{cap} = Q_{CNT}$) and VerilogA (and HSPICE) will automatically, iteratively calculate the value of the dependent voltage such that this condition is met. The value of this voltage is precisely the value of $\Delta\Phi_{B.}$ By using this technique, VerilogA and HSPICE can be used to quickly and accurately compute the channel surface potential change [Deng and Wong 2007a].

Next, the model takes into account two scattering mechanisms when computing the transmission probabilities: (1) acoustic phonon scattering (near-elastic scattering [Mann et al. 2003]), and (2) optical phonon scattering (nonelastic scattering [Yao 2000]). Elastic scattering is also considered, but is handled in the next level, CNFET_L2. By incorporating these scattering mechanisms (versus assuming ideal, ballistic transport), the model produces more realistic results for evaluating performance. Detailed equations and derivations are presented in Deng and Wong [2007a]. Having found $\Delta\Phi_B$ and the transmission probabilities, I_{semi} can be calculated. I_{semi} is implemented as a dependent current source shown in Figure 3.

The other two current components, I_{BTBT} and I_{metal}, can be found much more easily. Modeling band-to-band tunneling current is important because it significantly affects the subthreshold slope and leakage current. From Deng and Wong [2007a], I_{BTBT} is modeled using

$$I_{BTBT} = \frac{4qkT}{h} \sum_{\substack{k_m \\ m=1}}^{M} \left[T_{BTBT} \cdot \ln \left(\frac{1 + e^{\frac{qV_{ch,DS} - E_{m,0} - E_f}{kt}}}{1 + e^{\frac{E_{m,0} - E_f}{kT}}} \right) \cdot i_m \right], \tag{6}$$

where E_f is the Fermi level of the doped source/drain region. i_m is an "accounting dummy parameter" whose value is 1 only if there is band-to-band tunneling in the mth subband ($V_{ch,DS} > 2E_{m,0}$); thus, only those subbands with band-to-band tunneling are actually summed. T_{BTBT} is the band-to-band tunneling probability and can be found using the WKB method shown in Kane [1959, 1961] while noting that the carriers are confined to only the axial direction (1D problem). Full derivations of I_{BTBT} and T_{BTBT} are in Deng and Wong [2007a].

The current contributed by the metallic subband (I_{metal}) can be found using an equation similar to that of I_{semi}, Equation (2), but both electron and hole current must be summed. Since only 1 subband is considered (the metallic subband, $m = 0$), the summation over k_m can be reduced. Once again, approximating the summation over k_l as an integral and evaluating the integral, the expression for I_{metal} simplifies to

$$I_{metal} = \frac{4q^2}{h} T_{metal} V_{ch,DS}. \tag{7}$$

The corresponding transmission probability can be calculated as in Deng and Wong [2007a]. As expected, the metallic current is independent of the channel surface potential change (and the gate potential) because the density of states of a metallic CNT is independent of the carrier energy. This current source is

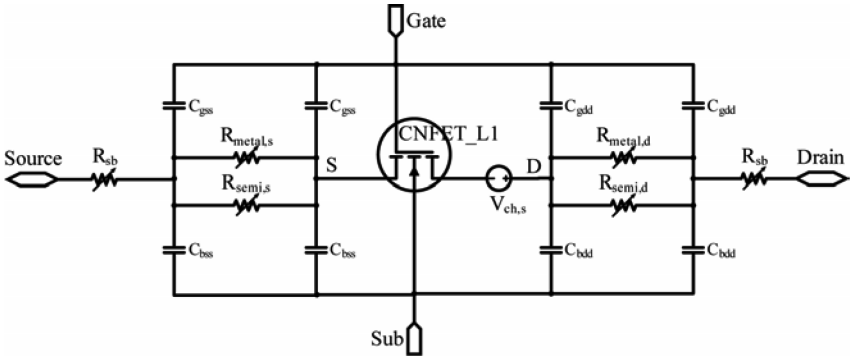

Fig. 6. Equivalent circuit for the level 2 model (CNFET_L2).

implemented as a dependent conductance from drain to source (Figure 3) with resistance $(4q^2/h)T_{metal}$.

For a semiconducting CNT, there is no metallic subband, so the total drain current is $I_{semi} + I_{BTBT}$. For a metallic CNT, I_{metal} dominates the drain current. So the total drain current can be approximated as simply I_{metal}.

The other part of the CNFET_L1 model is the transcapacitance network. To accurately model the dynamic performance of the CNFET, 5 coupling capacitances are included (gate/substrate to source/drain + gate to substrate capacitance) as shown in Figure 3. The complete equations and derivations can be found in Deng and Wong [2007a].

In summary, to model the intrinsic channel region of the CNFET, three current contributions have been included (Figure 3) to accurately describe the CNFET drive current, dynamic performance, subthreshold slope, and leakage. In addition, a full transcapacitance network (Figure 3) is also modeled to accurately predict the transient response and AC performance. To model a complete CNFET device for circuit-level simulations, additional levels (CNFET_L2 and CNFET_L3) must be included to model various other non-idealities and effects, such as those due to the source/drain extension region and contacts as well as the inter-CNT charge screening.

2.3 CNFET Model Level 2 (CNFET_L2)

The second level of the model (CNFET_L2) builds on top of the first level (CNFET_L1). The first level accurately models the intrinsic channel region; and the second level takes into account the effects of the heavily doped source/drain extension region (Figure 2) beyond the intrinsic channel region. Specifically, CNFET_L2 mainly accounts for the following 4 effects (among others): (1) elastic scattering effects; (2) parasitic resistances of the source/drain extension region; (3) parasitic capacitances of the source/drain extension region; and (4) the Schottky Barrier (SB) resistance of the source/drain metal contacts, if any. The circuit schematic of CNFET_L2 is shown in Figure 6.

Elastic scattering is primarily due to scattering sites cause by imperfect CNT fabrication and Coulomb centers. This elastic scattering effect is modeled in CNFET_L2, while the near-elastic (acoustic) and inelastic (phonon) scattering

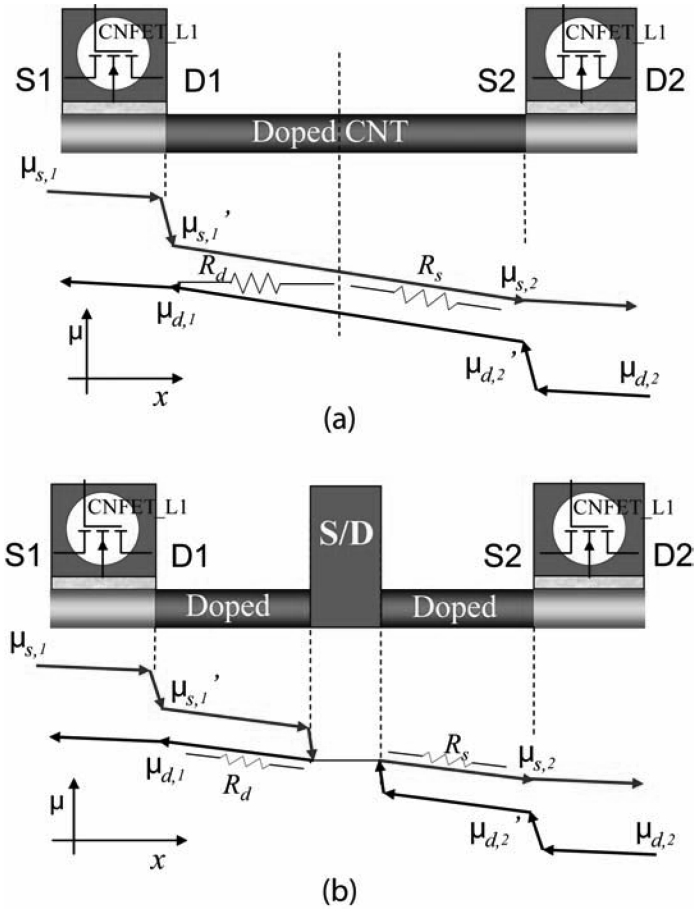

Fig. 7. Fermi Level Profiles. Case (a): the heavily doped source/drain extension region is used as local interconnect, and Case (b): the source/drain region is connected to a metal contact. There is an additional potential drop in Case (b) at the source(drain)-to-contact interface.

effects are modeled in CNFET_L1. The elastic scattering effects are modeled as a series resistance to the intrinsic channel and implemented as an effective potential drop $V_{ch,series}$.

The parasitic resistances of the source/drain extension region must be accurately modeled since they can play a significant role in determining the overall CNFET drain current. The parasitic resistance contributions due to the semiconducting and metallic sub-bands are modeled separately as dependent resistors $R_{semi,s}$ and $R_{metal,s}$ ($R_{semi,d}$ and $R_{metal,d}$). In addition, there are two cases to consider when evaluating these resistance values. The two cases are illustrated in Figure 7. Case (a): the source (or drain) is not connected to a metal contact; that is, the source (drain) extension region is connected directly to another CNFET's drain (source) extension region as local interconnect. Case (b): the source (or drain) is connected to a metal contact. These cases must be handled differently because the effective parasitic resistances are not the same. In Case

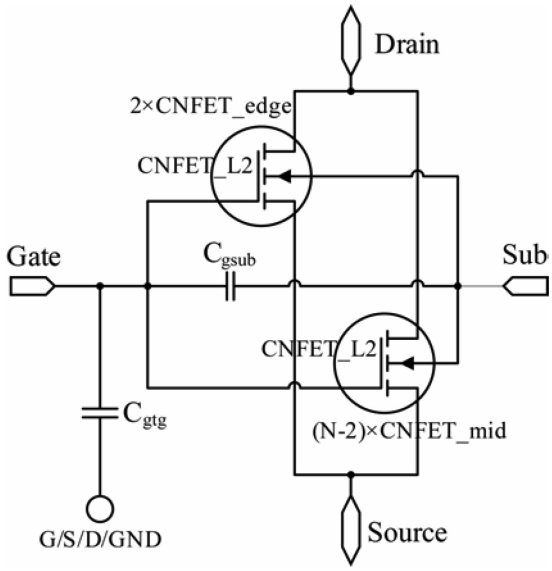

Fig. 8. Equivalent circuit for the level 3 model (CNFET_L3).

B, there is an additional potential drop (an effective series resistance) across the source(drain)-to-contact interface due to mode-mismatch. The model correctly handles both of these cases.

Parasitic capacitances of the source/drain extension region are modeled using the 8 capacitances shown in Figure 6. The fringing fields from the side of the gate metal to the doped source/drain extension region of the CNT(s) are considered here. The parasitic capacitances and parasitic resistances together form a π-model for the heavily doped source/drain extension regions.

Lastly, in the case where the source (or drain) is connected to a metal contact, CNFET_L2 also models the Schottky Barrier (SB) resistance as a dependent resistor R_{sb}. The following simplifying assumptions are made when calculating the SB resistance: (1) the doped CNT region is long enough such that there is no surface potential modulation due to the quantum confinement effects; (2) the dipole effects are neglected; (3) there are no pinning effects; and (4) the depletion region is approximated as a step function. This allows the computation of the SB resistance to be greatly simplified.

Detailed derivations of the model equations and parameters for CNFET_L2 are presented in Deng and Wong [2007b].

2.4 CNFET Model Level 3 (CNFET_L3)

CNFET_L3 completes the model by addressing two important effects: (1) the CNT-to-CNT charge screening effects, and (2) the gate-to-neighboring-contacts parasitic capacitances. The circuit schematic is shown in Figure 8.

Practical CNFETs must contain multiple CNTs per device in order to achieve sufficient drive currents for reasonable speed. Thus the model allows multiple-nanotube CNFETs and accounts for the CNT-to-CNT charge screening effects

present in these devices. The model assumes that, for a typical device geometry with a wide gate and thin dielectric, CNTs far apart have negligible charge screening effects on each other [Deng and Wong 2007c]. In other words, CNTs only experience charge screening from their immediate neighbors. Thus, the model considers two groups of CNTs within the multiple-nanotube CNFET. There are "edge CNFETs," which are CNTs at the edge of the device so that they only experience charge screening from one neighboring CNT; there can be only a maximum of 2 "edge CNTs." The remaining $(N-2)$ CNTs (assuming there are at least 2 CNTs) are "middle CNTs," which are CNTs that experience charge screening from both sides. The model accounts for charge screening effects by determining the effective gate-to-channel coupling capacitance depending on the charge screening effects. As shown in Deng and Wong [2007c], this approximation of categorizing the CNTs into edge and middle groups where only immediate neighboring charge-screening effects are considered is accurate to within 10% (and in many cases much better) compared to a full 3D field solver; thus validating these approximations. Following Deng and Wong [2007c],

$$C_{edge} = \frac{C_{scr} \cdot C_{inf}}{C_{scr} + C_{inf}} \tag{8a}$$

and

$$C_{middle} = 2C_{edge} - C_{inf} = \frac{C_{scr} \cdot C_{inf} - C_{inf}^2}{C_{scr} + C_{inf}} \tag{8b}$$

describe the effective edge and middle CNT gate-channel capacitance, which is passed to CNFET_L1 to determine the effect on channel current. C_{scr} is the effective screening capacitance and C_{inf} is the effective gate-to-channel capacitance assuming no charge screening effects. Thus, for a CNFET with only 1 CNT, the effective gate-to-channel coupling capacitance is C_{inf}. This is approximated by the model as $C_{inf} \approx C_{edge}$ evaluated at a large enough inter-CNT pitch ($\sim$40nm) such that C_{scr} becomes very large (the screening effect becomes negligibly small). For N CNTs per CNFET, the model calculates 2 edge CNTs with C_{edge} and $(N-2)$ CNTs with C_{middle}, as in Figure 8. Both single-nanotube and multiple-nanotube CNFETs are handled by the model.

CNFET_L3 also includes two more capacitances to model the parasitic gate capacitances. C_{sub} models the gate metal contact to substrate capacitance. In addition, the adjacent metal contacts shown in Figure 2 can be source/drain contacts or gate contacts if the CNFET is directly connected to other CNFETs in series. Since typical device aspect ratios and geometries have relatively tall and wide gates and short source/drain extensions, the gate-to-adjacent-contact parasitic capacitance can be quite significant when evaluating AC performance. C_{gtg} is a lumped capacitance that models these parasitic coupling capacitances to the nearby metal contacts.

Detailed derivations of the gate-to-channel capacitances for charge screening and the gate parasitic capacitances are presented in Deng and Wong [2007c].

With all three levels, the Stanford CNFET Model is now complete. In summary, the Stanford CNFET Model includes many practical nonidealities from scattering to Schottky Barrier resistances to charge screening effects. A

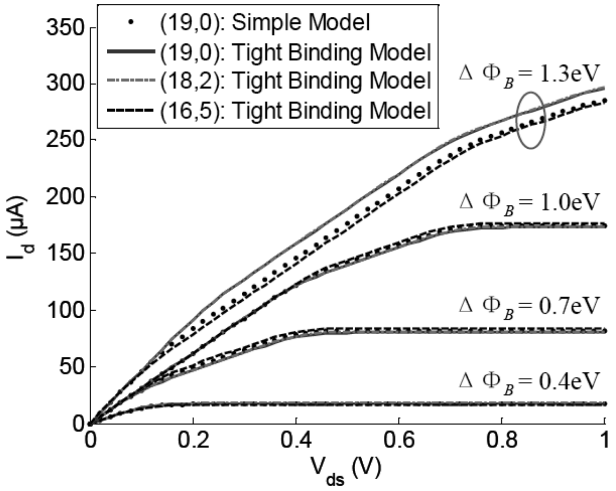

Fig. 9. Comparison of the CNFET compact model and the tight-binding model for the intrinsic CNT channel region. The CNT diameter was fixed at ∼1.5nm.

complete transcapacitance model is also included. The CNFET model can used in a variety of applications, including exploration and optimization on the device level to performance analyses on the circuit level. The most up-to-date version of the model can be found on the Stanford Nano Website (http://nano.stanford.edu) [Stanford 2007].

3. VALIDATION OF THE MODEL

The CNFET Model results are compared against other device-level models as well as measurements to validate the model.

Since there are currently no other comparable full CNFET models (including source/drain extension regions and multiple nanotube effects) available, only the first level (intrinsic CNT channel region) model is compared against another model (Figure 9) [Deng and Wong 2007a]. A (19,0) chirality CNFET is simulated using CNFET_L1 and is compared against numerical results obtained using the tight-binding model to calculate the (19,0) CNFET intrinsic channel current. CNFET_L1 assumes all chiralities of the same diameter have the same current. Thus, also shown for comparison are the results of the tight binding model using other chiralities of similar diameter (1.5nm). For the first 3 sub-bands ($\Delta\Phi_B < 1.0$eV), the results match quite well; for the fourth subband, some difference is observed.

In addition, the model results were also compared against both DC and AC experimental results [Amlani et al. 2006], as shown in Figure 10 and Figure 11. For the DC results, the drain current as a function of drain voltage matches to within 10% between a simulated CNFET and a fabricated CNFET. Similarly, for the AC experiment, the results match to within 10% (if the simulated data is shifted up by 1dB, a really good match is obtained).

Furthermore, a series of simulations was also performed using the model with varying parameters, such as channel length, CNT diameter, CNT pitch,

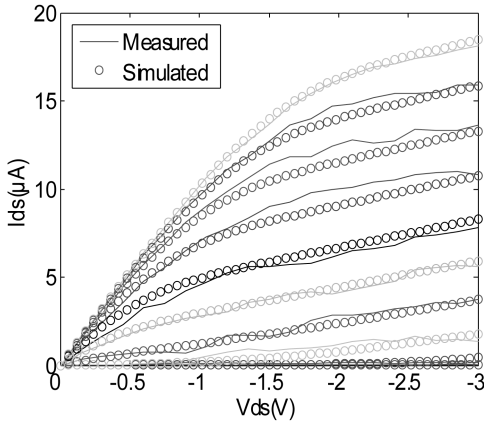

Fig. 10. Comparison of DC simulated results (CNFET Compact Model) and measured results. V_G is swept from 1.7V to −1.3V in steps of 300mV. Results match to within about 10% [Amlani et al. 2006].

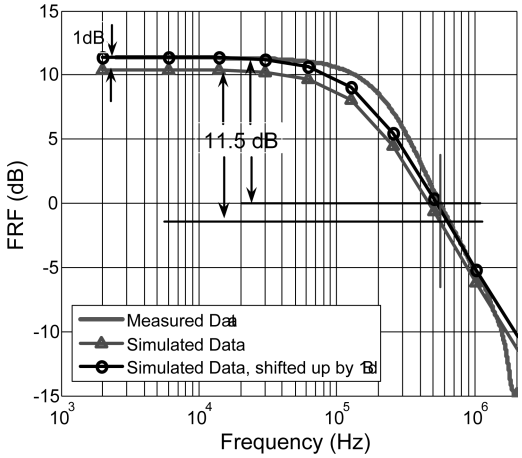

Fig. 11. Comparison of AC simulated results (CNFET Compact Model) and measured results. Results match reasonably well (∼10%), though a better match is achieved if the simulated data is shifted up by 1dB [Amlani et al. 2006].

. . . etc. All of the simulation results exhibited trends consistent with the underlying device physics.

Overall, for typical device geometries and dimensions, the Stanford CNFET Compact Models is accurate to within 10% of the tight-binding model and experimental measurements.

4. BENCHMARKING THE VERILOG-A IMPLEMENTATION

The Stanford CNFET Compact Model was implemented in both HSPICE and VerilogA. There are many advantages to VerilogA over HSPICE. Perhaps the two most important ones are portability and speed. VerilogA has been implemented in many simulators (including HSPICE), allowing the same model to

Table I. Comparison of VerilogA versus HSPICE Simulations Times and Speedup

Benchmark	VerilogA runtime (s)	HSPICE (s) runtime (s)	Speedup VerilogA/HSPICE
1 (CNFET static)	0.35	2.00	5.71x
2 (CNFET static)	0.40	2.10	5.25x
3 (CNFET trans.)	2.80	20.50	7.32x
4 (CNFET trans.)	2.70	20.70	7.67x
5 (CNFET trans.)	5.30	41.00	7.74x
6 (CNFET trans.)	7.90	60.90	7.71x
7 (Inverter DC)	0.40	3.30	8.25x
8 (Inverter trans.)	5.20	41.00	7.88x
9 (NAND2 trans.)	9.60	83.00	8.65x

be easily shared and distributed to users investigating different applications with different simulators. VerilogA is also significantly faster than HSPICE, most likely due to the many constructs uniquely available in VerilogA and its highly efficient iterative solvers. VerilogA can typically simulate a circuit (after compiling) within a fraction of the time for HSPICE. Here, we present some benchmarking data.

Several benchmark circuits were created to compare the simulation performance of the VerilogA versus HSPICE implementation [Wan 2007]. Both single CNFETs as well as simple logic gates were simulated. DC and transient simulations were also performed. The simulation times are shown in Table I.

The general trend, as expected, is that as the circuit becomes larger, the greater the speed advantage of VerilogA over HSPICE. This is because with increasing complexity, the advantages of VerilogA's highly efficient iterative solver become more apparent while any overhead is proportionally less significant. Overall, VerilogA exhibits speedups of 5x–8x over HSPICE for simulating simple devices and logic gates. This speedup advantage is expected to further increase for large-scale CNFET circuits (speedups of up $>$11x have been observed).

5. APPLICATIONS OF THE MODEL

The Stanford CNFET Model can be used both for device-level performance simulation as well as gate/circuit level performance simulation. An example application is projecting the performance advantage of n-type and p-type CNFETs over Si CMOS n-FETs and p-FETs at the 32nm technology node. Table II compares the gate capacitance, on current, and off current between CNFETs and Si MOSFETs [Deng and Wong 2007b].

Table II presents the performance advantage of CNFETs over Si MOSFETs based on CV/I. I_{on} and I_{off} are in units of current per capacitance, while I_{off} is set to the same value. CNFETs have a 6x and 13x CV/I improvement over the respective n-type and p-type Si MOSFET. Similar results with 2$\sim$10x delay improvement, 2$\sim$7x energy improvement, and 14$\sim$20x energy-delay-product improvement over Si CMOS is also reported by Deng et al. [2007d] using the CNFET Model.

Table II. Comparison of CNFET and MOSFET Performance at the 32nm Node. The on currents are units of current per capacitance. The off currents for CNFET and MOSFET have been set to the same value. The last column shows the (CNFET I_{on})/(MOSFET I_{on}) ratio (i.e. the performance advantage of CNFET over MOSFET based on CV/I).

$L_{channel}$ = 18mm	Gate C_{eff}	$I_{off(nA/fF)}$	$I_{on(mA/fF)}$	I_{on}/I_{off}	CNFET/MOS
nMOS	1.1 fF/μn	383	1.198	3128	N/A
nCNFET	3.6 aF/FET	383	7.236	18863	6.03
pMOS	1.1 fF/μm	253	0.5229	2066	N/A
pCNFET	3.6 aF/FET	253	7.172	28389	13.74

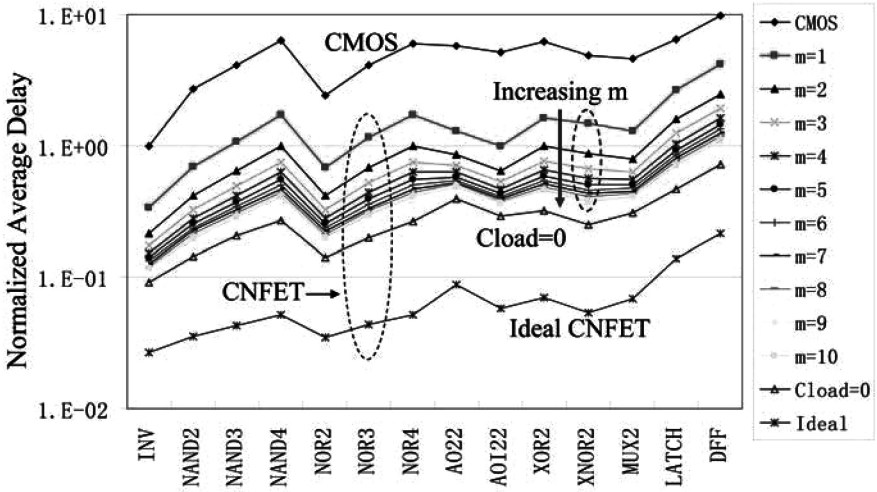

Fig. 12. Comparison of Circuit Speeds for CNFET and CMOS Circuits at the 32nm Node with Realistic Layouts and Interconnects. Delay is normalized to that of an FO1 CMOS inverter. The number of nanotubes (m) per CNFET gate is also varied from 1 to 10. The "C_{load}=0" curve assumes no interconnect capacitanc.

A similar comparison of CNFET and Si CMOS was also performed with logic gates in Deng [2007b] (Figure 12). Several different logic gates ranging from inverters to multiplexers were simulated. The results show that ideal CNFET devices give a theoretical upper bound speed improvement of 25∼50x over CMOS. However, taking into account practical non-idealities such as the parasitics of the highly-doped source/drain extension region, the speedup is reduced by about a factor of 2x to 10x∼20x. Lastly, including practical layout and interconnect capacitance, the speed improvement decreases significantly down to 2∼10x. The study suggestions that CNFET technology does have a reasonable advantage over Si CMOS at the 32nm node, however the advantage is significantly less than what may have been previously suggested by other theoretical studies.

Other applications include using the model to investigate the effects of device variations on performance, as reported by Deng et al. [2007d]. Diameter and doping were varied to study the impact of these variations on energy and delay. The results are summarized in Figure 13. Deng et al. [2007d] also looked

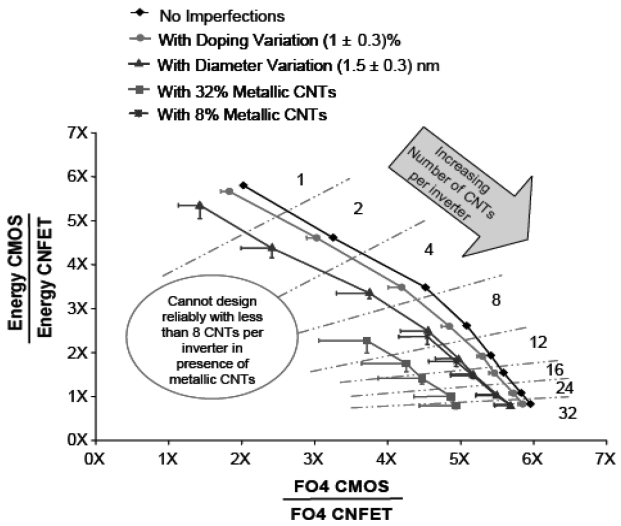

Fig. 13. Energy per cycle and FO4 delay advantage for a CNFET Inverter at 3σ points over a Si CMOS Inverter at the 32nm Node. Error bars indicate 6σ variation.

at the variation introduced by metallic CNTs. Roughly one-third of all CNTs are metallic (assuming uniform distribution of chiralities). Thus, a multiple-nanotube CNFET will contain a random mix of metallic CNTs and semiconducting CNTs. Metallic CNTs can short the source and drain of the CNFET and render the device useless. Even assuming metallic CNTs can be perfectly removed (that is, all metallic CNTs are removed, while all semiconducting CNTs are preserved), the remaining number of semiconducting CNTs can vary significantly. This metallic-CNT-induced variation was found to be the most problematic of the three variations. Both the CNFET energy and delay advantage over CMOS diminished greatly when in the presence of metallic CNT variations. Furthermore, due to the high probability of metallic CNTs, there can be a non-negligible probability of a CNFET with no semiconducting CNTs at all. Thus, this device simply becomes an open circuit after metallic CNT removal. Deng et al. [2007d] suggest that CNFETs should be designed with no fewer than 8 CNTs per CNFET given a 33% probability of metallic CNTs for functional reliability.

In the same study [Deng et al. 2007d], the model was used for inverter design optimization. The FO4 of a complimentary CNFET inverter was compared to that of a CMOS inverter at various CNT densities (Figure 14). The inverter width is fixed at 32nm while the number of CNTs per inverter is increased from 1 to 16 (CNT density of 30 CNTs/um to 500 CNTs/um; or equivalently, a CNT pitch of 32nm to 2nm). The optimal performance occurs at 8 CNTs/32nm (or 250 CNTs/um), which yields a 5x performance advantage of CNFET over CMOS. Fewer than this optimal CNT density results in better current per CNT (less charge screening) but less total current (fewer total CNTs); while greater than 250 CNTs/um results in more total CNTs, but less total current due to much less current per CNT. This serves as a device design guideline that roughly ~250 CNTs/um density is required for optimal performance.

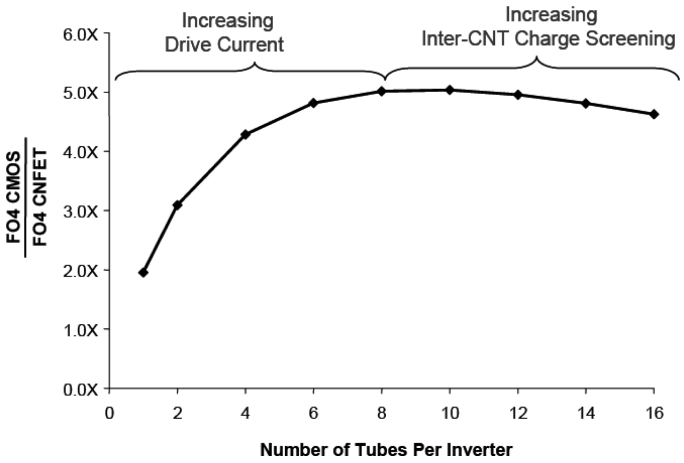

Fig. 14. Tradeoff between Increasing Drive Current and Increasing CNT Density. The inverter has a fixed width of 32nm. The optimal CNT density is ∼250 CNTs/um (8 CNTs/32nm, equivalent CNT pitch of 4nm).

Lastly, other applications of the CNFET Compact Model include the study of biomimetic CNT synapse circuits [Friesz et al. 2007] and CNT chemical/biological sensor design [Deng et al. 2007e].

In this section, we presented several different applications of the CNFET Compact Model, from device simulation to circuit performance analysis to device exploration and optimization. The versatility and applicability of the model will aid and expedite all aspects of design.

6. CONCLUSION

CNFETs are promising extensions to Si CMOS beyond the ITRS roadmap. To harness this potential, CNFET technology must move forward from the "scientific discovery" phase into the "engineering design" phase. Appropriate models and tools for CNFET design are essential to the engineering, design, and realization of any large-scale CNFET circuit. To address this need, the Stanford University CNFET Compact Model was developed and implemented in VerilogA. The model includes practical nonidealities and a complete transcapacitance network to achieve both accurate DC and AC simulation results (accurate within 10%). The model is derived from device and quantum physics to ensure accurate results and employs approximations and implementation techniques to improve runtime.

The model was subsequently validated against the tight-binding model as well as experimental device data. In addition, the speed of the VerilogA implementation of the compact model was compared against an HSPICE implementation using several different device and logic gate benchmarks. The VerilogA implementation showed speedups of 5x-8x, with an speedup of >11x expected for large-scale circuits with tens or hundreds of CNFETs. Lastly, applications of the model were presented, suggesting that n- and p-CNFETs will have 6x and 13x speed advantage over Si n- and p-MOSFETs respectively at the 32nm

node and that a CNT density of 250 CNTs/um is ideal for multiple-nanotube gates. Several other applications were presented as well, illustrating the power of tools like this in revealing important design considerations for the future. Certainly, if CNFET technology is to become a widely adopted IC technology, the supporting device and circuit design models and tools must be developed.

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