Reliability Analysis for Flexible Electronics: Case Study of Integrated a-Si:H TFT Scan Driver

TSUNG-CHING HUANG, KWANG-TING (TIM) CHENG
University of California, Santa Barbara
and
HUAI-YUAN TSENG and CHEN-PANG KUNG
EOL/ITRI

Flexible electronics fabricated on thin-film, lightweight, and bendable substrates (e.g., plastic) have great potential for novel applications in consumer electronics such as flexible displays, e-paper, and smart labels; however, the key elements, namely thin-film transistors (TFTs), for implementing flexible circuits often suffer from electrical instability. Therefore, thorough reliability analysis is critical for flexible circuit design to ensure that the circuit will operate reliably throughout its lifetime. In this article we propose a methodology for reliability simulation of hydrogenated amorphous silicon (a-Si:H) TFT circuits. We show that: (1) the threshold voltage (V_{TH}) shift of a single TFT can be estimated by analyzing its operating conditions; and (2) the circuit lifetime can be predicted accordingly by using SPICE-like simulators with proper modeling. We also propose an algorithm to reduce the simulation time by orders of magnitude, with good prediction accuracy. To validate our analytical model and simulation methodology, we compare simulation results with the actual circuit measurements of an integrated a-Si:H TFT scan driver fabricated on a glass substrate and we demonstrate very good consistency.

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General Terms: Experimentation

Additional Key Words and Phrases: Reliability, flexible electronics, threshold voltage, amorphous hydrogenated silicon (a-Si:H), thin-film transistor, scan driver

Authors' addresses: T.-C. Huang (corresponding author), K.-T. (T.) Cheng, Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106; email: Ettrick@ece.ucsb.edu; H.-Y. Tseng, C.-P. Kung, Flexible Electronics Technology Division, EOL/ITRI, Taiwan-R.O.C.

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1. INTRODUCTION

To meet the great demand for lightweight, portable, and low-cost consumer electronic products, revolutionary manufacturing processes such as ink-jet printing and reel-to-reel imprinting are now emerging as alternatives to billion-dollar conventional fabrication foundries [Boehm et al. 2006; Burns et al. 2005]. Flexible electronics, which have emerged from these low-cost and high-volume manufacturing methods, recently have attracted much attention because of their great potential to provide the foundation for novel consumer electronics applications such as flexible displays, e-paper, and RFIDs [Burns et al. 2005; Cantatore et al. 2006]. Compared to their MOSFET counterparts, the cost-to-area ratio of flexible electronics can be reduced by several orders. According to IDTechEx [2007], the number of low-cost RFIDs for item-level merchandise tracking is expected to grow explosively, as these devices can potentially replace the current, ubiquitous barcode system. On the other hand, rollable displays for portable devices are now also reaching the commercialization stage. More exciting applications of flexible electronics, such as wearable electronics, implantable IDs, and biosensors, will soon become pervasive in our daily lives.

TFTs are considered to comprise an ideal candidate on which to implement flexible circuits because of their compatibility with flexible substrates and their relatively simple and low-cost manufacturing process. According to their differing atomic structures and manufacturing processes, TFTs can be generally categorized into three types: amorphous hydrogenated silicon (a-Si:H) TFTs, polycrystalline silicon (poly-Si) TFTs, and organic TFTs (OTFTs). Among these candidates, a-Si:H TFT is our chosen experimental target for this study, based on the following observations: (1) It has good uniformity for large-area fabrication with relatively low cost; (2) it is mature, commercially available, and also compatible with the low-temperature process (e.g., 200°C) used on flexible substrates such as polyimide [Yeh et al. 2007]; (3) it shares many common features with the emerging ink-jetted OTFT and exhibits no significantly different characteristics on glass or flexible substrates [Yeh et al. 2007]; and (4) it is air stable (i.e., stable under ambient O_2 and H_2O), whereas ink-jetted OTFT is not. A-Si:H TFT allows us to focus on the electrical degradation that is the main scope of this work.

There has been extensive study on the electrical instability of a-Si:H TFTs [Chaji et al. 2006; Chiang et al. 1998; Huang et al. 2000; Libsch and Kanicki 1993; Powell 1983; Powell et al. 1989; 1987]. Two major mechanisms, carrier trapping and point defect creation, can explain the phenomenon of a-Si:H TFTs'

electrical instability. Carrier trapping usually occurs in the gate insulator due to material defects, while point defect creation typically occurs at or near the interface between the gate insulator and semiconductor. More details will be discussed in Section 2.

As a result, these material defects cause reliability problems in the operation of flexible circuits using a-Si:H TFTs, and therefore require careful analysis for designing more reliable flexible circuits. Particularly, the transistor degradation of a-Si:H TFTs is strongly affected by the bias-stress (i.e., switching activity) of an individual transistor. Different transistors can be exposed to different degrees of degradation. Therefore, the input/output characteristics of a degraded transistor could force it to deviate from its expected behavior and further influence its neighboring transistors. This problem makes a-Si:H circuits less stable than crystalline-Si circuits and also imposes great design burdens on circuit designers to ensure reliable operation throughout the expected lifetime. In this article, in order to systematically address this problem, we propose a methodology of reliability simulation for flexible circuits with TFTs such as a-Si:H TFTs. With this methodology, we can analyze the degradation profile for each TFT, perform reliability simulation, and predict the circuit lifetime accordingly by incorporating transient simulators such as SPICE. To validate our analytical model and simulation methodology, we designed and fabricated a scan-driver circuit using a-Si:H TFTs. This scan-driver circuit is used both to drive the active-matrix LCD (AMLCD), and also as our test circuit to assess the accuracy of the simulation results. The comparison shows high consistency between the measurement and simulation results. On the other hand, to assess the effectiveness of this methodology as a design aid, we analyze the published works regarding a-Si:H TFTs scan drivers' [Chen et al. 2007; Edo et al. 2006; Jang et al. 2006; Jang 2006] circuit reliability and lifetime as our case studies.

To reduce simulation time without sacrificing simulation accuracy, we introduce an algorithm that incorporates statistical methods, such as autoregressive integrated moving-average (ARIMA) models, to estimate the statistical features of bias-temperature-stress (BTS) information. With this algorithm, we can predict future values for circuit reliability and lifetime simulation with negligible loss of accuracy, while a simulation-time reduction of up to several orders of magnitude can be achieved.

The rest of this article is organized as follows. Section 2 describes the physical mechanism of transistor degradation and its analytical model. In Section 3, we review two commercial reliability tools for nanoscale CMOS [Karam et al. 2000; Cadence 2003] and explain why these tools are not adequate for simulating a-Si:H TFT circuit reliability. We then illustrate our methodology for reliability simulation and its applicability to an integrated a-Si:H TFT scan driver. We describe the algorithm for adaptively determining the step size for simulation-time reduction in Section 4. Extensive case studies on circuit reliability of a-Si:H TFT scan drivers are shown in Section 5. The simulation and measurement results are compared in Section 6, followed by the conclusion in Section 7.

2. TRANSISTOR DEGRADATION

In this section, we will briefly explain the physical mechanism of transistor degradation and then show the analytical model for estimating the transistor property (e.g., V_{TH}) shifts under different BTS conditions.

2.1 Electrical Degradation

The a-Si:H structure exists in a state of metastable equilibrium among weak Si-Si bonds, Si dangling bonds, and hydrogen passivated bonds. This equilibrium could be broken by applying external energy such as prolonged gate bias and result in more dangling bonds. This degradation process, fortunately, is reversible by annealing and the dangling bonds can be passivated by hydrogen mediation [Kuo 2003]. For a-Si:H TFTs, the mechanisms responsible for electrical instability are: (1) carrier trapping under the higher positive-bias and negative-bias regimes; and (2) point defect creation under the lower positive-bias regime. Carrier trapping occurs in the gate insulator and the a-SiNx:H layer, and arises from the high density of material defects generated during the deposition process, such as plasma-enhanced chemical vapor deposition (PECVD). The magnitude of ΔV_{TH} due to this carrier-trapping mechanism has a strong dependence on the nitrogen composition of the a-SiNx:H thin-film layer. On the other hand, point defect creation occurs in the semiconductor a-Si:H layer, at or near the interface, between the gate insulator and the semiconductor layers. These defects are bias-induced dangling bonds and the ΔV_{TH} attributed to this mechanism has dependence on the defect density. Higher defect density causes V_{TH} to shift toward the more positive direction, while an opposite effect on V_{TH} can be observed if the defect density is reduced in the a-Si:H layer.

By contrast, the annealing process of an a-Si:H TFT, which takes place during the off-state of the TFT operation, helps recover the degraded TFT characteristics (e.g., V_{TH} and V_{FB}) to a certain extent. This also explains why TFTs in the pixel circuits of AMLCD have a much longer lifetime than those TFTs used in functional circuits, such as scan drivers, since the fraction of active time of a pixel TFT is normally less than 1%. Therefore, TFTs in the AMLCD have much better chances to recover from bias-induced degradation. In addition, TFTs in AMLCD act as independent switches, controlling the transmissive light intensity from the backlight modules to human eyes. This implies that degraded TFTs have negligible influence on neighboring TFTs and also ensures their reliable operation throughout the circuit's expected lifetime.

2.2 Analytical Model of ΔV_{TH}

Empirically, the magnitude of ΔV_{TH} can be estimated by a stretched-exponential function [Chiang et al. 1998], shown in Eq. (1).

$$|\Delta V_{TH}| = |\Delta V_{eff}| \cdot \left\{1 - \exp\left[-\left(\frac{t_{ST}}{\tau}\right)^{\beta}\right]\right\} \tag{1}$$

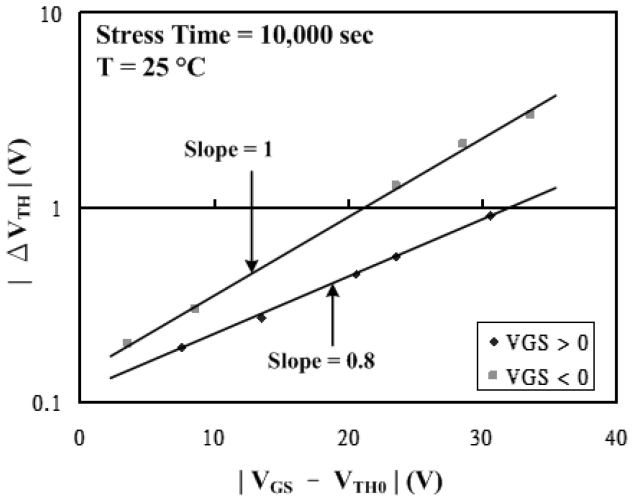

Fig. 1. ΔV_{TH} as a function of stress voltage $|V_{GS} - V_{TH0}|$.

Here, ΔV_{eff} is approximately the effective voltage drop across the gate insulator, t_{ST} is the effective stress time, τ is a temperature-dependent time constant, and β is a stretched-exponential exponent.

From our measurement results, shown in Figure 1, we observe ΔV_{TH}'s power-law dependence on $\Delta V_{eff}(=V_{GS} - V_{TH0})$, which can be described in Eq. (2) as

$$|\Delta V_{TH}| \propto |V_{GS} - V_{TH0}|^{\alpha}, \tag{2}$$

where V_{TH0} is the initial threshold voltage and α is a process-dependent exponent. This observation is also consistent with the results reported in Chiang et al. [1998], Huang et al. [2000], and Powell [1983]. For negatively pulsed V_{GS}, we observe that ΔV_{TH} exhibits pulse-width dependence that can be explained by the effective carrier concentration at the interface between the insulator and semiconductor layers [Chiang et al. 1998]. By considering this pulse-width dependence in a negative V_{GS} scheme, Eqs. (1) and (2) can be further combined to generate a more comprehensive model, as

$$\begin{aligned}\Delta V_{TH}(t) &= \Delta V_{TH}^{+}(t) - \Delta V_{TH}^{-}(t) \\ &= |V_{GS+} - V_{TH0}|^{\alpha+} \cdot \left\{1 - \exp\left[-\left(\frac{t \cdot D_c}{\tau^{+}}\right)^{\beta+}\right]\right\} \\ &\quad -|V_{GS-} - V_{TH0}|^{\alpha-} \cdot \left\{1 - \exp\left[-\left(\frac{t \cdot (1 - D_c)}{\tau^{-}}\right)^{\beta-}\right]\right\} \cdot f(PW), \end{aligned} \tag{3}$$

where t is the total operation time, D_c is the duty ratio of the bias pulses, $t \cdot D_C$ represents the effective bias-stress time for the positively pulsed bias-stress, $t \cdot (1 - D_C)$ represents the effective bias-stress time for the negatively pulsed bias-stress, the minus sign between positive and negative $\Delta V_{TH}(t)$ reflects the fact that V_{TH} shifts in opposite directions for positively and negatively pulsed bias-stress, and $f(PW)$ is a function characterizing the pulse-width dependence

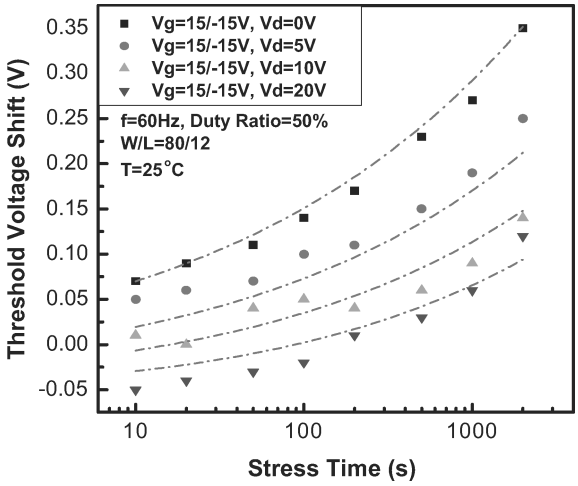

Fig. 2. ΔV_{TH} as a function of drain voltage V_{DS} and stress time.

under negatively pulsed bias. The techniques of calculating the effective bias-stress in the irregular waveforms from SPICE simulation will be discussed in Section 3.

In Eq. (3), we notice that only V_{GS} dependence is described and characterized. This characterization is adequate for the TFT operation in pixel circuits of the AMLCD, since V_{DS} is kept at fixed value for most of the AMLCD operational time [Chiang et al. 1998; Libsch and Kanicki 1993; Powell 1983]. To further characterize ΔV_{TH} for typical circuit operation (e.g., scan driver), therefore, we should extend this model to include the dependence on V_{DS}. Based on the transistor measurement results in Figure 2, we attempted to derive a formula to fit the measurement data and found that under positive V_{GS}, we can express $\Delta V_{TH}^{+}(t)$ as

$$\Delta V_{TH}^{+}(V_{GS+}, V_{DS}, t) = \Delta V_{TH}^{+}(V_{GS+}, t) \cdot f^{+}(V_{DS}) \tag{4}$$

$$f^{+}(V_{DS}) = \frac{2}{3} \cdot \frac{(V_{GS+} - V_{TH0})^3 - (V_{GS+} - V_{DS} - V_{TH0})^3}{(V_{GS+} - V_{TH0})^2 - (V_{GS+} - V_{DS} - V_{TH0})^2} \cdot (V_{GS+} - V_{TH0})^{-1}, \tag{5}$$

where $f^{+}(V_{DS})$ represents dependence on V_{DS} under the positive V_{GS} regime. On the other hand, for the negative V_{GS} regime, $\Delta V_{TH}^{-}(t)$ can also be expanded from Eq. (3) by incorporating the dependence on V_{DS} and the pulse width, as

$$\Delta V_{TH}^{-}(V_{GS-}, V_{DS}, PW, t) = \Delta V_{TH}^{-}(V_{GS-}, PW, t) \cdot f^{-}(V_{DS}) \tag{6}$$

$$f^{-}(V_{DS}) = 1 + \frac{V_{DS}}{2 \cdot (V_{TH0} - V_{GS-})}, \tag{7}$$

where PW describes the dependence on pulse width under the negative V_{GS} regime.

Based on Eqs. (1) through (7), the comprehensive analytical model can then be expressed as

$$\begin{aligned}\Delta V_{TH}(V_{GS}, V_{DS}, PW, t) &= |V_{GS+} - V_{TH0}|^{\alpha+} \cdot \left\{1 - \exp\left[-\left(\frac{t \cdot D_c}{\tau^+}\right)^{\beta^+}\right]\right\} \cdot f^+(V_{DS}) \\ &\quad -|V_{GS-} - V_{TH0}|^{\alpha-} \cdot \left\{1 - \exp\left[-\left(\frac{t \cdot (1 - D_c)}{\tau^-}\right)^{\beta^-}\right]\right\} \cdot f(PW) \cdot f^-(V_{DS}),\end{aligned} \tag{8}$$

where temperature-dependent terms are involved in τ^+ and τ^-. All curve-fitting parameters ($=\alpha, \beta, \tau$) are process dependent and should be characterized accordingly for different manufacturing processes.

3. RELIABILITY SIMULATION

Due to the electrical instability of flexible circuits, their reliability issues pose challenges to circuit designers, consequently hindering their development. To address this problem, we propose a methodology for reliability simulation of flexible circuits with TFTs. This methodology can help designers to identify the most degraded transistors and to predict performance of these degraded circuits. Based on the analytical model in Section 2, we can calculate the degradation profile of each individual TFT and also perform iterative SPICE simulation for mimicking the physical degradation mechanisms. Therefore, the designer is able to get a fast assessment of circuit reliability in the early design stages.

In order to validate this methodology, we designed an integrated TFT scan driver fabricated on the same glass substrate with the AMLCD. Comparison results will be discussed in Section 6.

3.1 Previous Work

Reliability simulation tools such as the Cadence Virtuoso UltraSim [Cadence 2007] and Mentor Graphics Eldo [Karam et al. 2000] are now widely available for simulating circuit reliability of nanoscale CMOS due to HCI/NBTI degradation. These tools originate from the BERT (Berkeley reliability tool) [Huang et al. 2000], which uses the *Age* parameter-modeling concept. The model parameters for both fresh and prestressed devices can be extracted from device characterization using parameter analyzers. The *Age* parameter can be calculated using interpolation and extrapolation from a table of prestressed device parameters. With the aged model parameters given for all devices in a circuit, SPICE-like circuit simulators can predict the circuit lifetime with high accuracy and compare the waveforms of fresh and degraded circuits accordingly.

The $\Delta I_{SAT}/\Delta V_{TH}$ due to HCI/NBTI for CMOS, however, does not have the same strong dependence on operational conditions as do a-Si:H TFTs. In addition, the correlation of $\Delta I_{SAT}/\Delta V_{TH}$ between neighboring transistors is negligible. For these reasons, the reliability simulation tools designed for nano-CMOS are not considered suitable for our purpose. Regardless, in order to reduce the long simulation time due to the multistep iterative nature of BERT-like

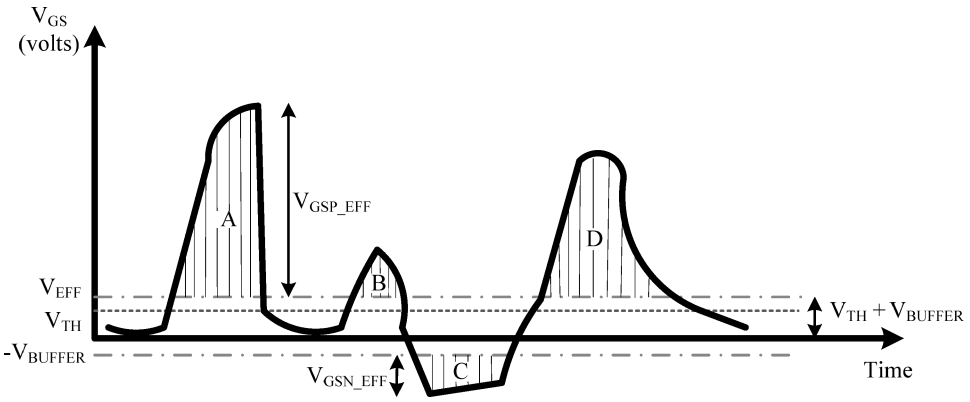

Fig. 3. Example voltage waveform of calculating effective bias-stress for each TFT.

reliability simulators, an integrated environment using AHDL for a-Si:H TFT is proposed [Gadelrab et al. 1995; Gadelrab and Barby 1998]. However, this environment is not SPICE-compatible and the accuracy of this method is still a matter of concern. Therefore, neither of these reliability simulators meets our needs. In this article, the proposed methodology for simulating circuit reliability takes advantage of the high accuracy of BERT-like tools. We also reduce the total simulation time by performing time-series analysis on SPICE transient simulation results such that we can use adaptive simulation time-steps in the Age domain between two consecutive SPICE runs. More details will be discussed.

3.2 Effective Pulse Formulation

For the transistor measurement environment, we can apply ideal pulses to transistor terminals and extract the required parameters accordingly; however, in the real circuit operation, the bias-stress waveforms applied to each transistor terminal are often irregular. Therefore, how to calculate and convert these irregular waveforms into effective pulse widths and pulse voltages for Eq. (8) becomes an important factor that can significantly affect the accuracy of ΔV_{TH} calculation.

The charge-trapping mechanism that causes TFT degradation (e.g., ΔV_{TH}), depends on the energy levels and quantities of electron charges transported in the channel layer. Therefore, a simple yet effective way to estimate this effect is to calculate the total effective area under the bias-voltage waveforms derived by SPICE transient simulation. In Figure 3, areas A, B, and D are considered effectively positive-bias areas, while area C is considered an effectively negative-bias area for estimating the charge-trapping and detrapping phenomena. Here, $V_{\text{GSP-EFF}}$ and $V_{\text{GSN-EFF}}$ represent the effective peak voltages for positive and negative bias-stress, respectively. V_{BUFFER} represents the regime in which the TFT just starts to conduct current with low-energy electrons, and its voltage level depends on the magnitude of $V_{\text{GSP-EFF}}$ and $V_{\text{GSN-EFF}}$. The total effective pulse-widths and average pulse-voltages that will be used in Eq. (8) can then be derived; an example is shown in Figure 3.

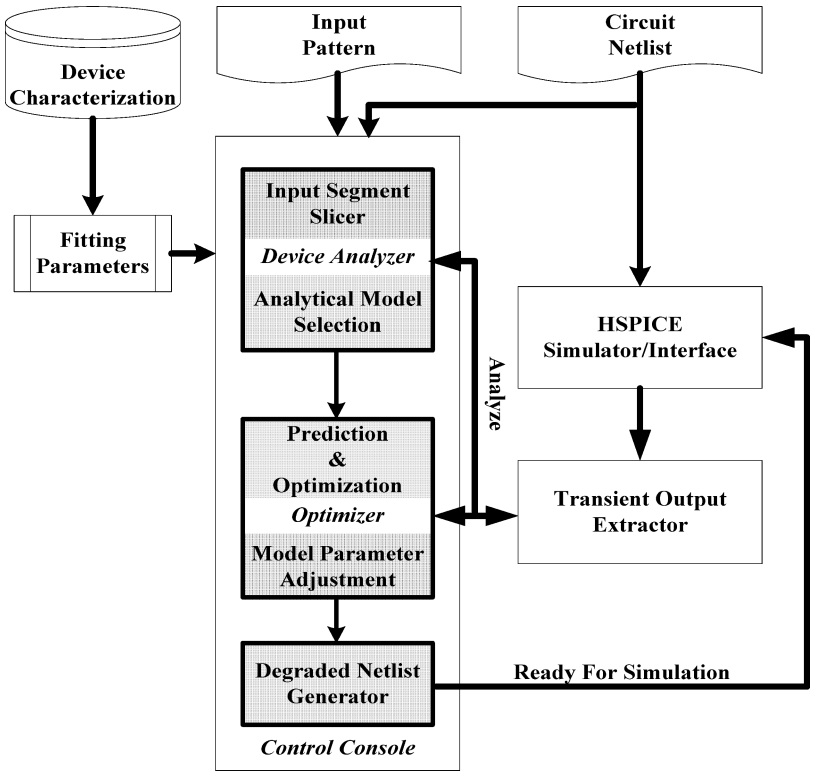

Fig. 4. Methodology of reliability simulation.

3.3 Simulation Flow

We show the methodology for the reliability simulation of TFT circuits in Figure 4. The *control console* acts as an external pre- and postprocessor for the SPICE-like simulator (e.g., HSPICE). The internal component *device analyzer* in the control console selects an appropriate analytical model for ΔV_{TH} and its fitting parameters for each transistor based on the prestressed device characterization and its input patterns. It also collects data from the *transient output extractor* for calculating effective bias-stress time (e.g., total pulse widths) and bias voltages (e.g., V_{GS}, V_{DS}) for each transistor and then computes ΔV_{TH} degradation accordingly. The component *optimizer*, which plays the central role in data-processing flow, is designed for performing time-series analysis of V_{GS} and V_{DS} in Eq. (8) for each transistor and, based on this analysis, for predicting future values accordingly for the next SPICE run. The time-step between two consecutive SPICE runs can be determined adaptively and increasing the time-step can reduce the total simulation time. More importantly, the prediction error can be well controlled under predefined error boundaries. Finally, the optimizer can collect the complete information of each transistor degradation profile and then the component *degraded netlist generator* can generate a degraded circuit netlist, including degraded model parameters for each transistor. The degraded netlist is then used in the next run of the SPICE transient simulation in the

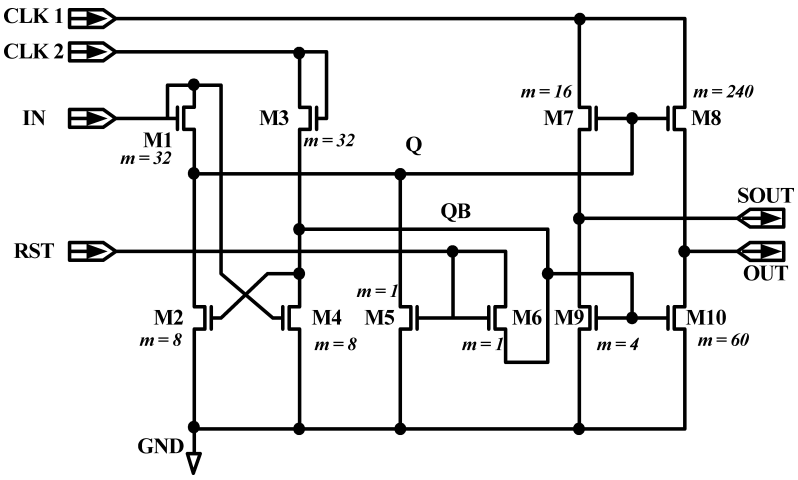

Fig. 5. One of eight modules in the scan driver (test chip).

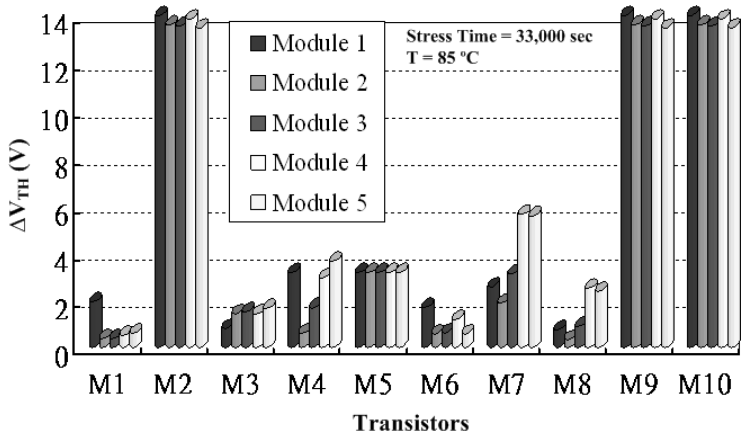

Fig. 6. ΔV_{TH} profiles of individual transistors in the first five modules.

Age domain. This process repeats until the specified time-stamp is reached. One should note that the operational condition for each transistor here is assumed unchanged during each SPICE run of short-period (e.g., 5 ms) transient simulation.

3.4 Test Chip: Scan-Driver Circuit

We show a single module of the scan driver for the AMLCD in Figure 5. In our experimental circuit, eight such modules are serially connected. A scan driver is typically designed with a 60 Hz scanning signal, which scans the TFT pixel array of AMLCD one-line-at-a-time to sequentially turn on each horizontal scan line.

Based on the aforementioned methodology, the BTS information for each transistor is used for calculating ΔV_{TH} profiles. The derived ΔV_{TH} profiles from modules 1 to 5 are shown in Figure 6. We find that M2, M9, and M10 are the

most degraded TFTs. The reason is straightforward: These transistors are directly connected to *CLK-2* and continuously operated under pulsed bias-stress. From Figure 6, we can observe that the ΔV_{TH} of the most degraded transistors exceeds nine times their initial value (in this case ($V_{TH0} = 1.41$ V)) and can significantly deteriorate the functionality of the scan driver. Through this reliability simulation and analysis, we can realize that the scan-driver circuit as shown in Figure 5 requires a certain amount of modification in order to ensure reliable operation throughout the desired lifetime.

4. SIMULATION-TIME REDUCTION

The methodology proposed in Section 3 attempts to mimic the physical degradation process of bias-stressed TFTs; however, due to the strong correlation of ΔV_{TH} between neighboring transistors, the degradation simulation of the circuit inevitably requires a circuit simulator such as SPICE to run iteratively. The long SPICE simulation time makes this method impractical. Hence, to resolve this problem, we propose to minimize the number of required SPICE runs by performing time-series analysis.

4.1 Problem Formulation

Our main objective is to minimize the total number of required SPICE runs. This goal can be accomplished by maximizing the time-step used in the Age domain between two consecutive SPICE runs. This time-step can be adaptive and the total simulation time can be greatly reduced if the SPICE transient simulation results from different (but consecutive) runs are auto-correlated.

For a given input pattern, the effective bias-stress time of each individual transistor is approximately proportional to the total bias-stress time. The magnitude of the bias-stress voltages, on the other hand, is affected by neighboring transistors. Without loss of generality, we can assume that the magnitude of the bias-stress applied to the same transistor terminals is a continuous-time function, that is, there are no sudden changes between two consecutive SPICE runs. Linear extrapolation techniques can generally provide good prediction accuracy in this case for simulation-time reduction.

To further cover such cases for a wide range of input patterns, we need a more compressive time-series analysis to reduce the prediction error caused by simple linear extrapolation techniques. The auto-regressive integrated moving-average (ARIMA) model is widely used in economics and weather forecasting, for predicting future time-series values in more complex circumstances than in a linear circuit [Wei 2006]. To use this model in our case, we can treat the average magnitude of V_{GS} and V_{DS} (as shown in Eq. (8) and Figure 3) in each short-period SPICE transient simulation as random variables in a nonstationary time-series process. Here we assume that for each given input pattern, the accumulated pulse widths of V_{GS} and V_{DS} for each SPICE run are identical, and proportional to the total stress time under the given input pattern. Assuming the variables (i.e., $Z_1, Z_2, \ldots Z_n$, representing average V_{GS} and V_{DS} magnitudes for each of the n previous SPICE runs), we can get the l-step-ahead prediction by expressing the time-series variables. This is shown in Wei [2006]

as

$$e_n(l) = Z_{n+1} - \hat{Z}_n(l) = \sum_{j=0}^{l-1} \psi_j \varepsilon_{n+l-j} \tag{9}$$

$$\hat{Z}_n(l) = E(Z_{n+l} \mid Z_t, t \le n) = \sum_{j=1}^{p} \pi_j^{(l)} Z_{n-j+1} \tag{10}$$

$$\pi_j^{(l)} = \sum_{i=0}^{l-1} \pi_{l-1+j-1} \psi_i, \tag{11}$$

where $\hat{Z}_n(l)$ is the l-step-ahead prediction of Z_{n+l} at the prediction origin n, $e_n(l)$ is the prediction error, Ψ and π are weighting coefficients, p is the order of the AR process, and ε is a random variable from a normal process with zero mean. Thus, the $(1-\alpha)\cdot 100\%$ prediction limits [Wei 2006] are

$$\hat{Z}_n(l) \pm N_{\alpha/2} \left[1 + \sum_{j=1}^{l-1} \psi_j^2 \right]^{1/2} \cdot \sigma_\varepsilon, \tag{12}$$

where $N_{\alpha/2}$ is the standard normal deviation such that $P(N > N_{\alpha/2}) = \alpha/2$. Hence, the time-step problem can be formulated as

$$\text{subject to} \quad \sum W_i \cdot e_{n,i}(l) \le Eo, \qquad \text{maximize } \textit{time-step } l \qquad i = 1, \ldots, N, \tag{13}$$

where Eo is a user-defined error boundary, N is the total transistor count of the circuit, W_i is the weight of transistor i's influence on the circuit output, and $e_{n,i}(l)$ represents the l-step-ahead prediction error of the ith transistor after the nth SPICE run. The higher the Eo is set, the fewer SPICE runs needed by the process. Tradeoffs can be made between prediction accuracy and simulation time, based on the designer's needs.

4.2 Step-Size Algorithm

To get the maximum time-step l at the prediction origin n, first we need to build the appropriate ARIMA model from previous simulation results $Z_1 \sim Z_n$ [Wei 2006]. The initial ARIMA model for given data can be obtained using software such as EVIEWS [2008] and SAS [2008]. The next step is to calculate the prediction error based on the time-series model to see whether it exceeds the predefined error boundary. If not, we can proceed to increase the time-step l and to compute the l-step-ahead prediction values $Z_n(l)$ and prediction error $e_n(l)$ accordingly, where n represents the current simulation instant. Once the prediction error reaches the error boundary, we can run SPICE with the most current l-step-ahead prediction value that was used to generate the degraded circuit netlist and model card parameters. We can repeat this process by iteratively including the most current SPICE simulation result and calculating the new l-step-ahead prediction value for each simulation instant. This process repeats until the final time-stamp for simulation is reached. The pseudocode is described in Figure 7.

```
Find Maximum Time-Step l for simulation instant n
Build initial time-series model for Z_l ~ Z_n
Begin
        Compute error boundary Eo
        Set l to be one
        Compute aggregate error Σ e_n(l)
    While Σ e_n(l) ≤ error boundary Eo Then
        Increase time-step l
        Compute l-step ahead prediction Z_n(l)
        Compute aggregate error Σ e_n(l)
    End while
        Call SPICE using Z_n(l)
        Update time-series model for Z_l ~ Z_n+l
End
```

Fig. 7. Pseudocode of step-size algorithm.

4.3 Accuracy Validation

To validate the accuracy of our analytical model and step-size algorithm, a trustworthy reference source is required and plays an essential role. Two sources can be considered as good references: (1) the SPICE transient simulation results in a small-step and iterative manner in the Age domain, and (2) the real working circuit under the same settings (e.g., stress time and temperature), as in the SPICE simulations. For the case of iterative small-step SPICE simulations, the analytical model in Eq. (8) will be applied after each short-period (e.g., 1 ms) SPICE run and used to generate degraded model parameters for the next SPICE run. The limitation of this method is that the analytical model in Eq. (8) is generally not optimized for short periods. Usually, the reliability model is derived by applying different bias-stress amounts to the transistors for long periods (e.g., 10,000s). Applying this long-period analytical model to a short-period SPICE simulation will inevitably result in errors in ΔV_{TH} calculation. Thus, running SPICE iteratively (e.g., 10,000 SPICE runs) in this manner for monitoring ΔV_{TH} with respect to stress time will accumulate such small modeling and calculation errors, make the result untrustworthy, and take a long simulation time. Therefore, we still cannot tell whether a real fabricated circuit will work as predicted by iterative SPICE simulations.

By contrast, the results of direct measurement of a fabricated circuit will be more trustworthy. However, one has to note that, although ΔV_{TH} is the most significant and observable phenomenon on a degraded transistor, other parameters such as flat-band voltage V_{FB} and carrier mobility μ will also degrade with time and change its electrical behavior. Therefore, monitoring ΔV_{TH} with stress time cannot fully reflect the degraded circuit performance. For the aforementioned reasons, we decided to use the output waveforms of a fabricated circuit as our reference source. Our simulation methodology uses the previously mentioned step-size algorithm to predict the future values of average V_{GS} and V_{DS} in a SPICE run. The long-period analytical model is then applied to get the

final ΔV_{TH} when the time-stamp is reached. Longer-period SPICE results (e.g., V_{GS}/V_{DS} and stress time) are used in this case. Comparison results will be shown in Section 6.

5. CASE STUDY OF A-SI:H TFT SCAN DRIVER

In order to verify the effectiveness of our reliability simulation methodology and tool as a design aid, we will go over the typical designs of reliable a-Si:H TFT scan drivers from published work. Reliable designs of the a-Si:H TFT scan driver include many varieties, and can be categorized into several types: (1) redundancy-based [Edo et al. 2006], (2) AC-bias-based [Jang et al. 2006; Jang 2006], and (3) compensation-based [Chen et al. 2007] scan-driver designs. The detailed analysis and comparison of circuit reliability will be discussed in this section.

5.1 Redundancy-Based Reliable Scan-Driver Design

A unit stage of the reliable a-Si:H TFT scan-driver design is shown in Figure 8(a). As for the case of a QVGA-size scan-driver design [Edo et al. 2006], 320 such stages are connected serially to generate the scan signals and turn on the scan lines one-line-at-a-time. In the figure, G(n − 1), G(n), and G(n + 1) represent the output signals of each unit stage from the previous stage, current stage, and next stage, respectively. Nodes A, B, and C are controlling signals for T4, T6, and T2, as shown in Figure 8(a), and the timing diagram of these controlling signals is shown in Figure 8(b). Since a-Si:H TFTs have both stress and recovery cycles, ΔV_{TH} due to the stress cycles can be relieved to some extent during the recovery cycles. The key to ensuring reliable operation for redundancy-based design, therefore, is to have dual pull-down TFTs that are responsible for discharging the pixel TFTs of the AMLCD. In such a design, one TFT is stressed/controlled using low duty-ratio control signals (e.g., G(n + 1) to T5) to ensure negligible ΔV_{TH}, while the other TFT is stressed/controlled using near-DC bias-stress (e.g., node B to T6) to ensure fully discharged pixel TFTs. From Figure 9(a), it can be seen that the degraded profile for each TFT matches the signal duty-ratios as shown in Figure 8(b), and that the most degraded TFTs are under near-DC bias-stress.

Those TFTs under low duty-ratio bias-stress (e.g., *T3* and *T5*) have only one-third ΔV_{TH} compared to TFTs under near-DC bias-stress (e.g., *T2* and *T6*). Figures 9(b) and 9(c) show simulated output waveforms of the first two modules of the scan driver under no bias-stress and under accelerated stress (i.e., 33,000s at 85°C), respectively. We notice that the scanning signal outputs have only negligible variation (e.g., 22V → 21.9V). More importantly, the pull-down TFT pairs keep working properly in discharging redundant charges, which results in negligible expanded signal-spikes, as the arrows indicate in those figures. From this waveform comparison, we may not only preview the degraded signal outputs of the scan driver, but may also realize that lowering the duty ratio of controlling signals is an effective way of improving the reliability of a-Si:H TFT circuits.

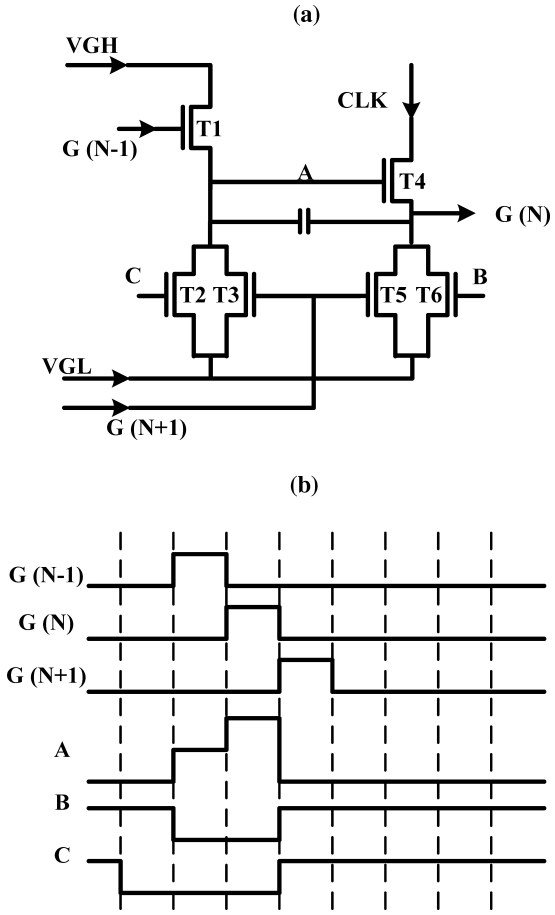

Fig. 8. Redundancy-based reliable scan-driver design and its signal waveforms [Edo et al. 2006].

5.2 AC-Bias-Based Reliable Scan-Driver Design

Unlike the redundancy-based design, the AC-bias-based design shown in Figure 10 [Jang et al. 2006] does not require additional TFTs to ensure both reliability and functionality. The ΔV_{TH} of the pull-down TFT (e.g., *Td* in Figure 10(a)) is mitigated by using low duty-ratio (e.g., 50%) AC controlling signals, as shown in Figure 10(b). In this case, pull-down TFTs have better chances to recover from charge-trapping-induced degradation, while for half of the time these TFTs are biased under negative voltage (e.g., V_L in Figure 10(b)). On the other hand, the functionality of pull-down TFTs can also be ensured by fully discharging the pixel TFTs of AMLCD for half of the time using 50% duty-ratio AC controlling signals. From Figure 11(a), it can be seen that the degradation profiles of T_U and T_D in Figure 10(a) show a much smaller ΔV_{TH} compared to those TFTs under near-DC bias-stress in Figure 9(a) (e.g., *T2* and *T6*). Note that the signal feed-through problems of T_D are resolved in this case by providing a low-resistance path from the gate lines to ground when the *Qb* node is high.

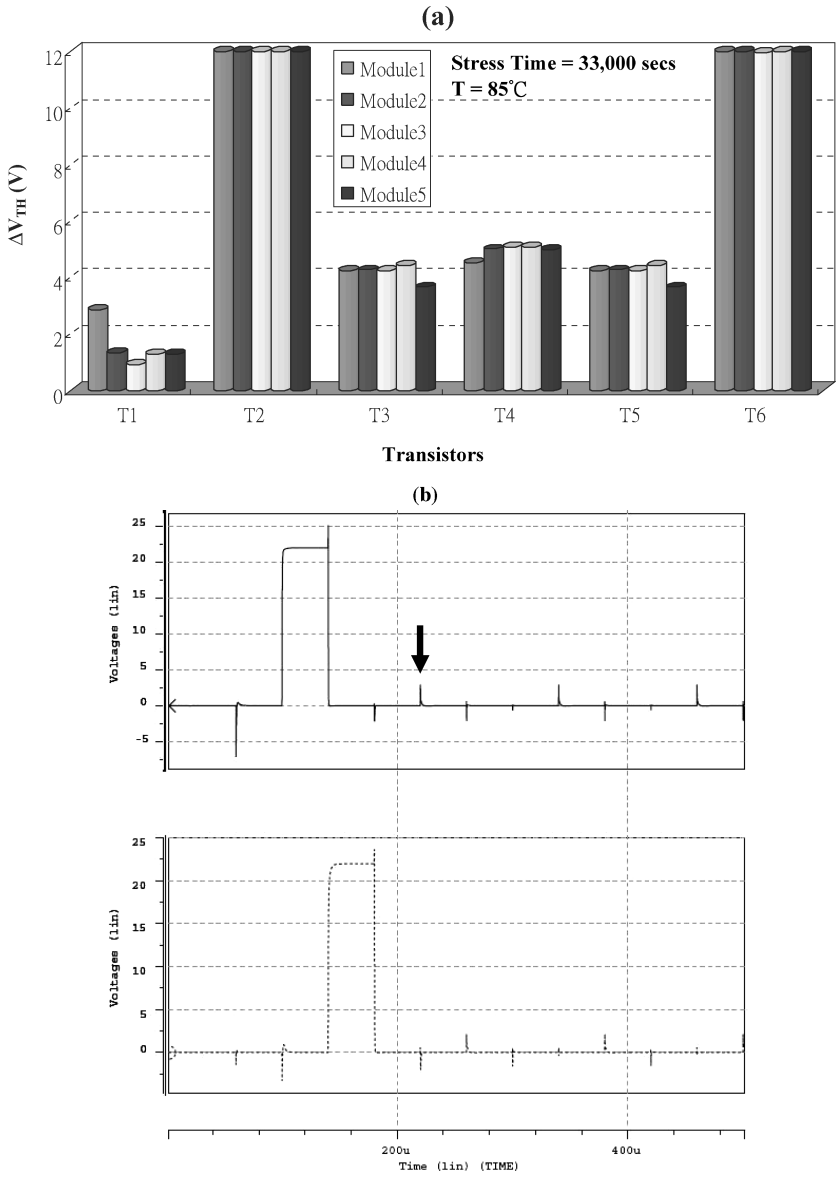

Fig. 9. Degradation profile for TFTs in Figure 8 and degraded waveform comparisons.

On the other hand, the clock feed-through of T_U is relieved by providing the opposite controlling signals for T_U and T_D, as seen in Figure 10.

Figures 11(b) and 11(c) show the output waveform comparisons for fresh and degraded scan drivers under the same stress conditions as in Figure 6 and Figure 9 (i.e., 33,000s at 85°C). We can observe that the signal spikes appearing in Figure 11(b) become significant in Figure 11(c) after circuit degradation. The output-signal level is pulled into negative due to the signal feed-through of T_U and T_D. On the other hand, due to the increased on-resistance after the

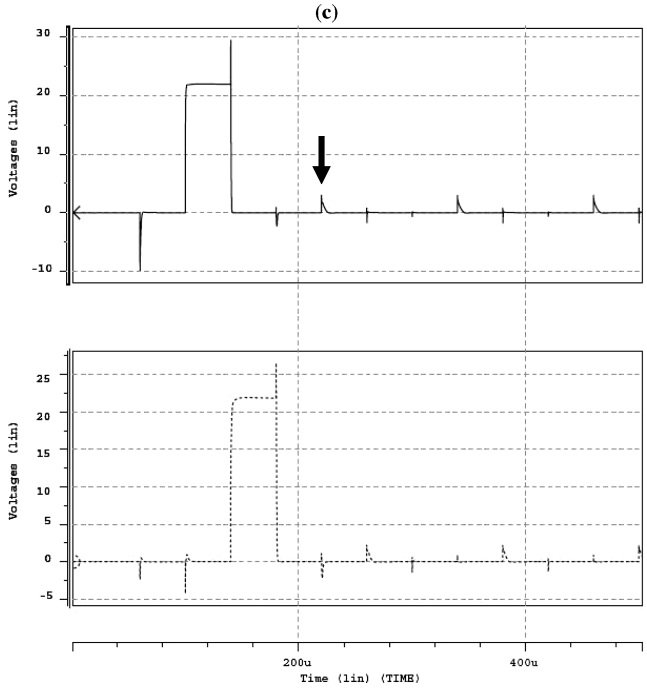

Fig. 9. (*Continued*).

electrical degradation, the output signal level cannot be easily pulled to ground, particularly when V_{DS} is small. Fortunately, this degradation pattern will not cause error functions of the pixel TFTs of AMLCD, since the output levels remain low. Therefore, T_U, T_D, and the gate lines will remain off and function correctly, even under continuous AC-bias stress, as shown in Figure 10(b).

6. EXPERIMENTAL RESULTS

Due to the limited availability of flexible circuits, to assess the accuracy of our methodology and analytical models, we use comparisons between the output waveforms of SPICE simulation and actual stressed circuit measurements. On the other hand, simply comparing the ΔV_{TH} with stress time can reflect the real case, since ΔV_{TH} is not the only degraded transistor parameter. To assess the simulation-time reduction, we compared the required number of SPICE runs both with and without proper prediction techniques. The experimental circuit is the scan driver with eight such modules, as shown in Figure 5.

6.1 Waveform Comparison

6.1.1 *Unstressed Circuit.* Based on our analytical model, we analyzed ΔV_{TH} profiles for the scan-driver circuit and simulated degraded circuit accordingly. To get a fast assessment of circuit degradation, the simulation was performed without the extraction of layout-related parasitics and thus the layout-related noise/crosstalk was neglected. We first evaluate the circuit that

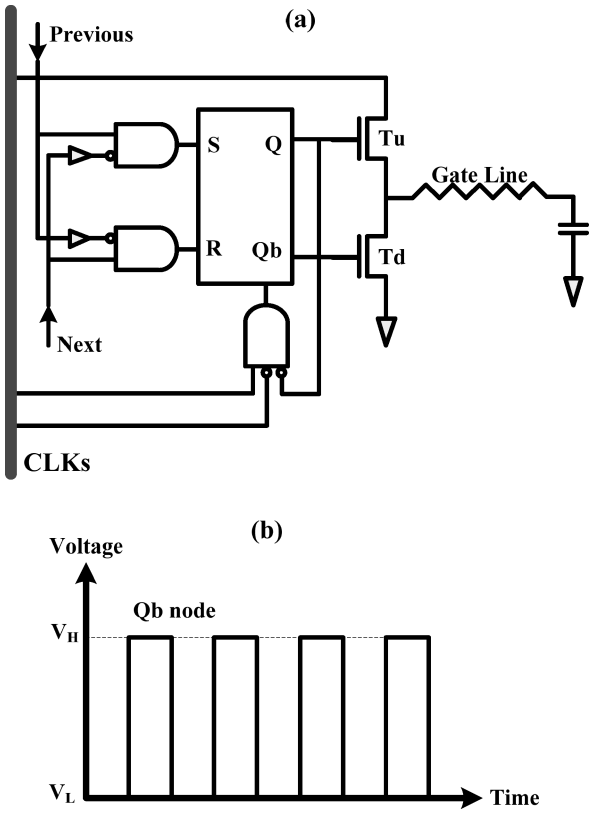

Fig. 10. AC-bias-based reliable scan-driver design and its signal waveforms [Jang et al. 2006].

has never been stressed before (i.e., in the very beginning of its life-cycle). The comparison of the simulation and actual measurement results is shown in Figure 12. We observe in Figure 12(a) that the simulation successfully identifies some unwanted signal spikes in the simulation waveforms, which also appeared at the same locations in the measurement waveforms of Figure 12(b). These unwanted spikes identified by the simulation, shown in Figure 12(a), are due to the signal currents from *CLK-1* through M8 (Figure 5), which have larger size. Other signal spikes in Figure 12(b) which do not appear in Figure 12(a) are mainly due to certain layout-related parasitics that were not accurately considered in our prelayout SPICE simulation.

6.1.2 *Stressed Circuit.* With continuous bias-stress on the test circuit, we observe in Figure 13 that the signal spikes that also appeared in Figure 12 become more significant both in amplitude and width. These expanded spikes could cause malfunction of the AMLCD and are mainly due to a large ΔV_{TH} increment of M2 (Figure 5) under the considerable bias-stress. In normal circuit operation, *CLK-2,* which is activated right after *CLK-1*, should be able to switch on M2 and pull the voltage level of Q to low; however, with the significant ΔV_{TH} of M2, the voltage level of Q sticks at high and cannot be pulled to low. This

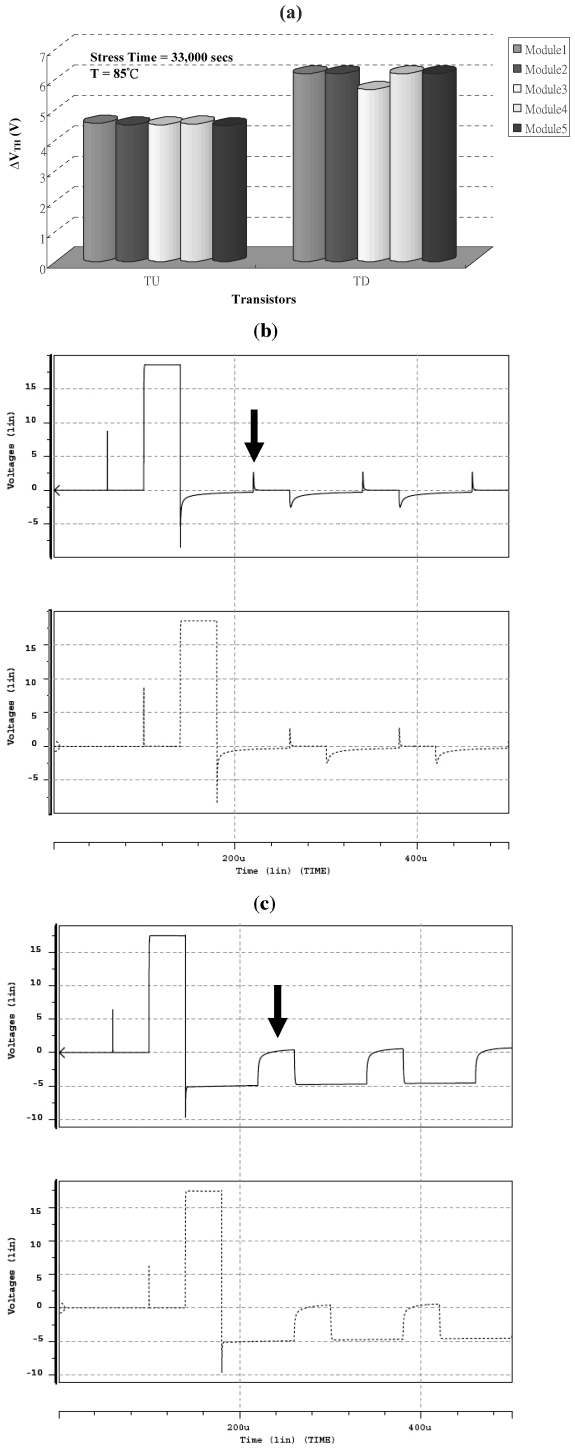

Fig. 11. Degradation profile for TFTs in Figure 10 and degraded waveform comparisons.

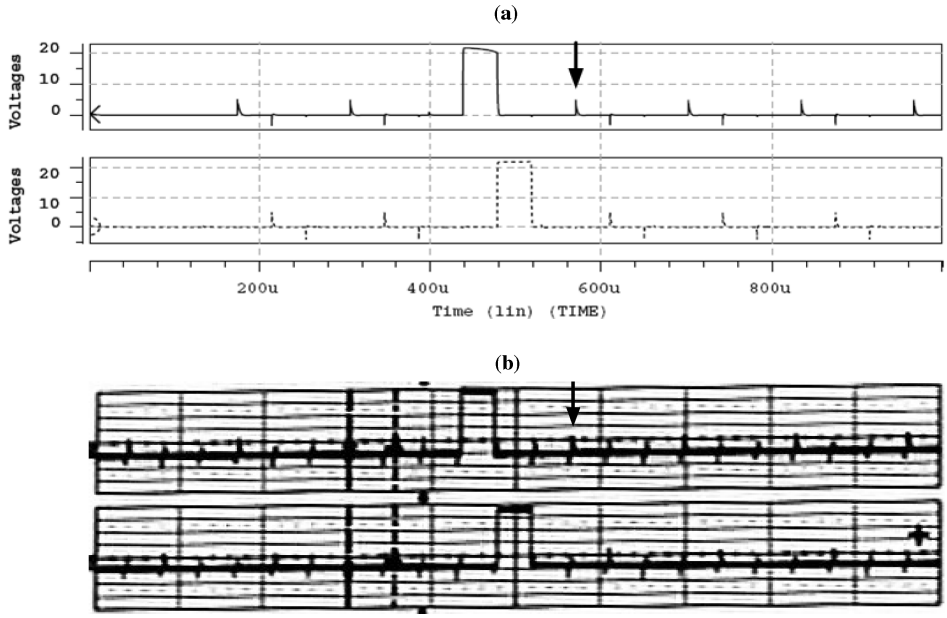

Fig. 12. Comparison of output waveforms from the first two modules of the unstressed circuit: (a) SPICE simulation; (b) actual measurement (the scale is 5v/div (vertical) and 100μs/div (horizontal)).

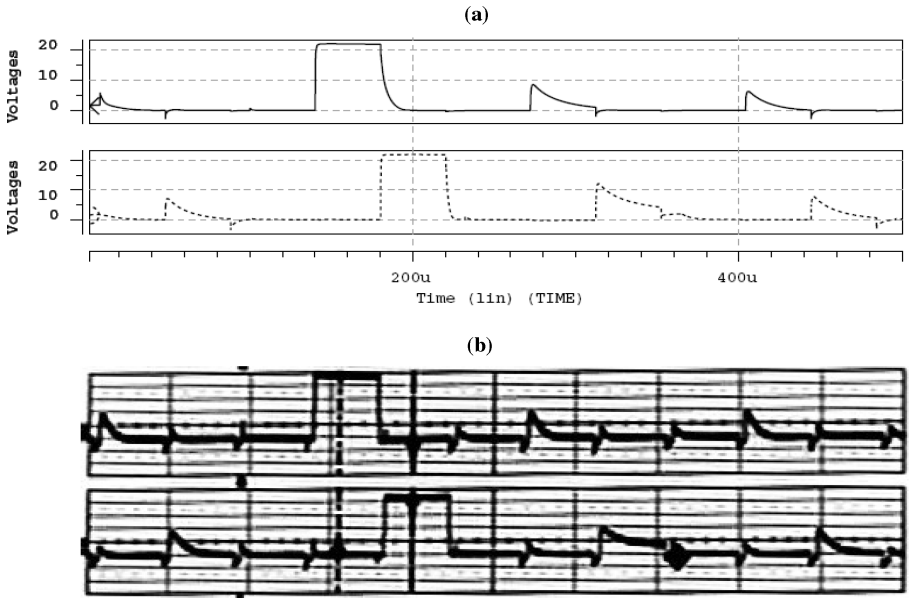

Fig. 13. Comparison of output waveforms from the first two modules of the stressed circuit for 33,000s: (a) SPICE simulation; (b) actual measurement (the scale is 5v/div (vertical) and 50 μs/div (horizontal)).

Table I. Comparison of SPICE Iterations and Simulation Time

Prediction Techniques	Number of SPICE Iterations	Simulation Time (sec)
Not Applied	3.30×10^7	2.60×10^8 (*est.*)
Time-Series Analysis		
10% Error	1.42×10^3	1.56×10^4
20% Error	4.83×10^2	5.41×10^3

results in the malfunction of M8, which relies on the voltage level of Q to switch on/off the signal current from *CLK-1*. This phenomenon was successfully predicted using SPICE simulation, as shown in Figure 13(a). We can observe highly consistent results between the simulation and actual measurement results, as depicted in Figure 13(a) and Figure 13(b). In the case of Figure 13, the stress time (=33,000s) is the point at which the circuit might accidentally turn on the pixel circuit of the AMLCD, due to excessively expanded output signal spikes. In the simulation results shown in Figure 13(a), the extrapolation techniques have been applied for predicting the BTS conditions of individual transistors. This predicted BTS information (e.g., average V_{GS}) for each SPICE run is then used to generate ΔV_{TH} accordingly.

6.2 Simulation-Time Reduction

In Table I, we can see that without using any prediction techniques, the required number of SPICE iterations for total stress-time 33,000s is prohibitively long; however, after applying prediction techniques to the SPICE results, the number of required SPICE iterations has been significantly reduced while maintaining negligible loss of prediction accuracy, as shown in Table I. Note that "*est*." represents the estimated simulation time.

7. CONCLUSION

In this article, we discuss reliability issues for emerging flexible electronics technology. As the first work analyzing the electrical instability of flexible circuits, we chose a-Si:H TFTs for this study. We derive an analytical model of ΔV_{TH} from actual measurement data to analyze the transistor degradation. We then use a scan-driver circuit, which is used to drive the AMLCD, as our test case for validating our analytical model and simulation methodology. The analytical model of ΔV_{TH} has been verified with a number of measurements under various conditions. The reliability simulation methodology, which is developed based on the Age parameter concept in BERT, is more comprehensive and suitable for use with flexible circuits than BERT-like tools for nanoscale CMOS. This is because our method takes into account the input pattern and the operational conditions of individual transistors in the flexible circuit, while maintaining BERT's high accuracy. The key drawback of BERT-like tools, which need small-step iterative simulation, is alleviated by dynamically adjusting the step size using time-series analysis techniques based on preceding SPICE transient simulation results. On the other hand, extensive case study of major design types of a-Si:H TFT scan drivers are also analyzed and simulated based on our methodology. This study gives us a good assessment of the effectiveness of

our methodology and reliability tool as a design aid. By performing reliability simulation, designers can preview the circuit reliability under designated operating conditions, without need for actual fabrication and lifetime/reliability testing. This can greatly reduce the design time and effort.

We designed and fabricated a test chip, an integrated scan-driver circuit, on the same glass substrate as the pixel circuits of the AMLCD using a-Si:H TFTs. The comparisons between SPICE simulation results and actual measurements show very high consistency. To our knowledge, this is the first work addressing reliability simulation methodology and design analysis of flexible circuits with TFTs, which is a key step toward developing an effective methodology for designing robust flexible circuits.

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