Organizing Wires for Reliability in Magnetic QCA

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This article investigates, via analytic modeling, how a magnetic QCA wire should be organized to provide the highest reliability. We compare a nonredundant wire and two redundant wire organizations. For all three organizations, a fault rate per unit length is used for comparison; additionally, since extra components are necessary to implement the redundant organizations, these components are faulty as well. We show that the difference between these two fault rates is the main driver for selecting a wire organization. Lastly, we develop a guideline for selecting the most reliable wire organization during the circuit design process.

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1. INTRODUCTION

Three components are required when building a processor: memory, logic, and interconnect. This is true for the silicon technology of today and will be true with the various nanoelectronic devices and architectures that will be used to augment or replace silicon technology. An important aspect of building these systems, particularly at the nanoscale, is that each of these system components must be reliable.

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Frequently, reliability modeling in CMOS has centered on when a wire will break and no longer pass current. However, for a technology like Magnetic QCA[1] (MQCA), the traditional idea of a broken wire is unsuitable since the devices interact through near-neighbor interactions rather than current. As such, we need to use a modeling technique capable of treating the devices as individual logic devices. The technique used here, probabilistic transfer matrices, is capable of doing this.

In this work, we investigate three wire organizations to determine which has the highest reliability. The first organization is a regular, nonredundant wire. The second and third utilize Triple Modular Redundancy (TMR) with a single voter and with redundant voters. In all three configurations, a fault rate per unit length is the basis for faulty wire segments. In the TMR configurations, the components needed to implement the redundancy (i.e., voters) are faulty as well. We demonstrate that it is the relationship between these fault rates that will determine which wire organization ensures the highest reliability for a variety of wire lengths and number of voting stages (for the TMR organizations). This leads to a set of guidelines that can be followed by circuit designers to maximize circuit reliability.

The next section provides background information. Section 3 introduces the wire models used in this work. Single segment results are presented in Section 5 and the multisegment results are presented in Section 6. Section 7 presents organizational guidelines and outlines future research directions.

2. BACKGROUND INFORMATION

2.1 Magnetic QCA

The Quantum-dot Cellular Automata (QCA) architecture is built upon a foundation of simple, identical, bistable devices that interact with one another via electromagnetic forces. The initial devices for QCA were charge based (electrostatic) and utilized Coulombic interactions for transmitting information [Lent et al. 1993]. MQCA, rather than using Coulombic interactions, uses magnetization vectors to store and transmit information. Experimental work on MQCA is described in Imre [2005], Imre et al. [2006], and Varga et al. [2009].

MQCA utilizes rectangularly shaped nanomagnets since they are in their lowest energy state when the magnetization vector is aligned along the long axis of the nanomagnet. Since, depending upon the external magnetization forces, this vector will point straight up or down for vertical nanomagnets, the magnets can provide stable binary values.

Figure 1(a) shows two vertical nanomagnets with opposing magnetizations. The fundamental logic gate, the majority gate, is shown in Figure 1(b). A horizontal wire segment is an ordered line of nanomagnets which utilizes antiferromagnetic coupling to transmit data and is shown with the wire organizations in Figure 2(a). Other components, such as fanouts, can be constructed by the

[1]QCA has generally been referred to as quantum-dot cellular automata, but for magnetic implementations the quantum-dot component of the QCA term can cause confusion. As a result, we use QCA to describe the architecture based on these devices.

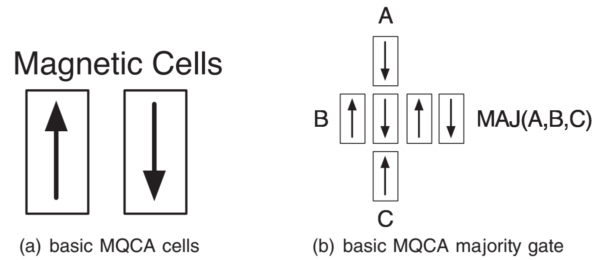


Fig. 1. Sample MQCA cells and majority gate.

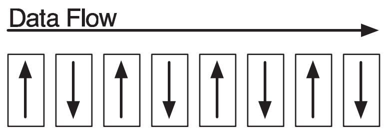
proper arrangement of nanomagnets. Since the basic device is used to implement both logic and interconnect, they must be treated equally from a reliability perspective. This is why faults in both the wire and logic components are considered.

We assume MQCA to be a planar technology that utilizes crossover components to swap the arrangement of signals [Niemier et al. 2007, 2008]. As will be shown, this assumption increases the routing complexity of the TMR organization when redundant voters are used. We also assume that a fixed clocking field is used to move data as required by the QCA paradigm [Lent and Tougaw 1997; Niemier et al. 2007]. As discussed in Niemier et al. [2008], it may be possible to improve the reliability of the nanomagnets by using a stronger clock, but we do not explore that possibility here. Additionally, we assume that the clocking structure does not introduce any errors since they can be eliminated by strengthening the clock signal or tested separately (a circuit with defective clock signals will be unusable independent of the nanomagnets).

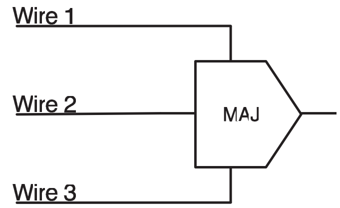
2.2 Probabilistic Transfer Matrices Framework

In this work, Probabilistic Transfer Matrices (PTMs) [Krishnaswamy et al. 2005, 2008] are used to compute the fault rates of the wire organizations. The PTM for a component/circuit/system with m inputs and n outputs is a $2^m \times 2^n$ matrix that shows the relationship for all combinations of inputs and outputs. At location (i, j) in the matrix, the specific relationship between input set i and output set j is defined. If the component produces an incorrect output with probability p (fault rate), regardless of input values, correct relationships between i and j are represented by $1 - p$ and erroneous relationships are represented by $p/(2^n - 1)$ in the PTM.

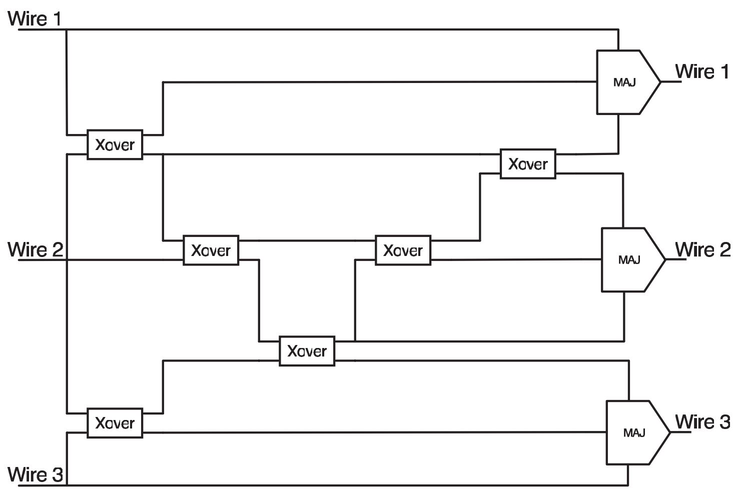
By following a simple set of construction rules, a PTM for a larger structure can be formed from the PTMs of its constituent structures. Once the PTM for a structure is obtained, its reliability can be found by following a simple procedure. For this work, the fault rate for a wire organization is then just $1 - r$, where r is the reliability of the wire organization. See the previously cited references and Dysart and Kogge [2009a] for more detailed examples and discussion on using PTMs to calculate reliability.



(a) straight wire slice



(b) single voter slice (TMR-NR)



(c) replicated voters slice (TMR-Rep). Each wire crossing component is marked with an Xover box.

Fig. 2. Wire slice models.

3. WIRE MODELS

This work considers three general types of wire slices as shown in Figure 2. The first slice type is that of a single wire segment without redundancy as shown in Figure 2(a). The second slice type (identified as TMR-NR), shown in Figure 2(b), is a single wire segment that has been replicated and uses a voter (majority gate) to select the output of the wire. When slices of this type are chained together, a fanout component (one in, three out) is needed in each slice to ensure that the output of the voter from the previous slice is replicated to each of the three wires in this slice. The third wire slice type (identified as TMR-Rep), shown in Figure 2(c), is similar to the previous type, but replicates the voters as well as the wires. This causes an increase in the amount of signal routing required to implement this technique. For reference, the *XOver* boxes in this figure show where a crossover component is utilized. Since three outputs result from the voters in this approach, when several of these slices are chained together a fanout component is needed only in the initial slice rather than in each slice and a final voter is also needed to have a single output from a chain of these slices.

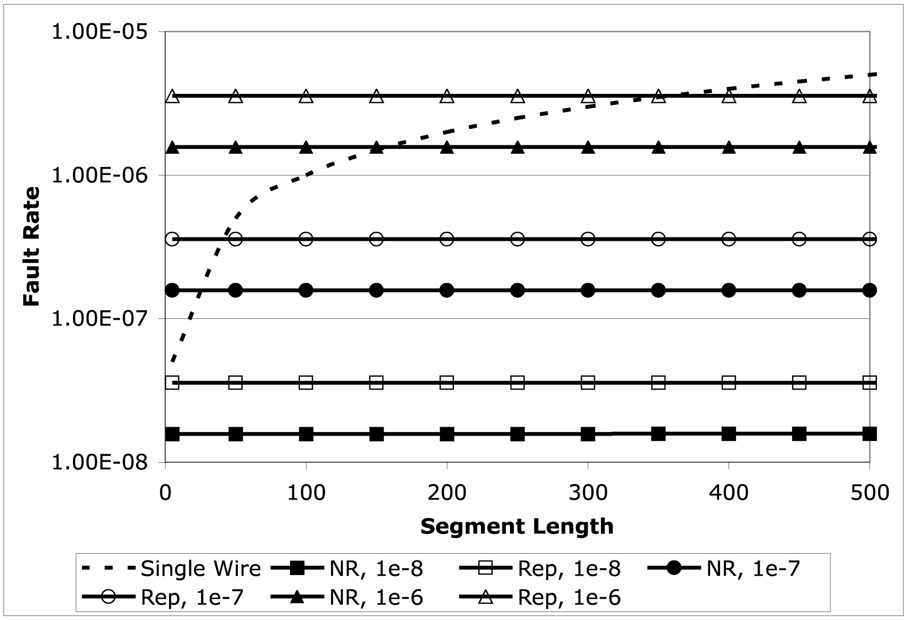


Fig. 3. Fault rates for single slices as the wire segment length increases.

4. EXPERIMENTAL SETUP

In this work, we assume that a unit length of a wire segment is a single nanomagnet. A wire segment is then a series of l nanomagnets. The PTM for a wire segment (PTM_{WS}) is PTM_{UL}^{l}, where PTM_{UL} is the PTM for a unit length. The notation F_{ul} is used to identify the fault rate per unit length of wire. In this work, l is in increments of five.

In addition to having fault-prone wire segments, the components required to implement the redundant wire organizations (e.g., voters) are faulty as well. The fault rate for these TMR-required components is identified as F_{ec}. Rather than do a complete cell-by-cell layout for the wires between the TMR-required components, it is assumed that F_{ec} encompasses any potential faults in the wires used to connect these components to one another. This is a slight simplification from the methodology used in Dysart and Kogge [2008, 2009b].

Throughout this article, $F_{ul} = 1 \times 10^{-8}$ and F_{ec} is varied along with the segment length and number of slices. This value of F_{ul} is arbitrary, but its value is insignificant because the guidelines for organizing wires is based on the relationship between F_{ul} and F_{ec}. This relationship has been observed by testing multiple values of F_{ul}, but these results are not shown due to space restrictions.

5. SINGLE SLICE FAULT RATES

Figure 3 presents the main result for this section. In this figure, *Single Wire* refers to a single wire with no replication, *NR*, F_{ec} refers to a triplicated wire with a single voter, and *Rep,* F_{ec} refers to a triplicated wire with triplicated voters.

There are several trends in Figure 3 that can be observed. First, when F_{ec} is the same for the TMR-based configurations, the TMR-NR configuration has the lower fault rate. Second, as the segment length increases, the fault rates for the TMR-based configurations have an indistinguishable increase while the fault rate for the single wire configuration has a noticeable increase. This indistinguishable increase is a result of the fault rate for the TMR-based configurations being significantly more dependent upon F_{ec} rather than F_{ul}. This result was also observed in Dysart and Kogge [2008].

TMR-Rep shows a higher fault rate than TMR-NR in this case since a final voter has not been used to generate a single output. If a final voter is used to generate a single output for the TMR-Rep configuration, then the fault rates for TMR-NR and TMR-Rep at a given F_{ec} are virtually identical.

For the results in Figure 3, if $F_{ec} = F_{ul}$, then the replicated wire configurations have a lower fault rate. However, this scenario is unlikely to occur as this would mean that the fault rate for a multidevice component (i.e., majority gate) is equivalent to a single device. If $F_{ec} = 10 * F_{ul} = 1 \times 10^{-7}$, then the single wire slice configuration is better (lower fault rate) than TMR-NR until the segment length is between 15 and 20 and is better than TMR-Rep until the segment length is between 35 and 40. If $F_{ec} = 100 * F_{ul}$, then the segment lengths at which the nonreplicated and replicated voter slice configurations are better than the single wire slice are 155–160 and 355–360, respectively. In essence, as F_{ec} increases by an order of magnitude in relation to F_{ul}, then the segment length needed for the TMR slice configurations to have a lower fault rate than the single wire slice configuration increases by approximately an order of magnitude.

6. MULTISLICE WIRE FAULT RATES

Having determined how a single wire slice should be configured to ensure reliable operation, we explore how wires should be configured if multiple slices are chained together. Two main scenarios will be considered: (1) a fixed number of slices are chained together (variable wire length) and (2) a total fixed wire length is divided into a variable number of slices.

6.1 Fixed Number of Slices

Figure 4 displays the system fault rates for a chain of 5 slices. We observe that for a given F_{ec} that TMR-Rep has a lower fault rate than TMR-NR which is different than the single slice case where they were equivalent (assuming a final output voter for TMR-Rep). For this chain, if $F_{ec} \geq 10{*}F_{ul}$ than TMR-Rep is the most reliable. TMR-NR is an improvement on the single wire configuration after the segment length is beyond 15–20. When $F_{ec} = 100{*}F_{ul}$, then TMR-Rep and TMR-NR are better than the single wire once the segment length is 30–35 and 155–160, respectively. Increasing F_{ec} by another order of magnitude adds roughly another order of magnitude in the segment length needed for either TMR version to be an improvement on the single wire.

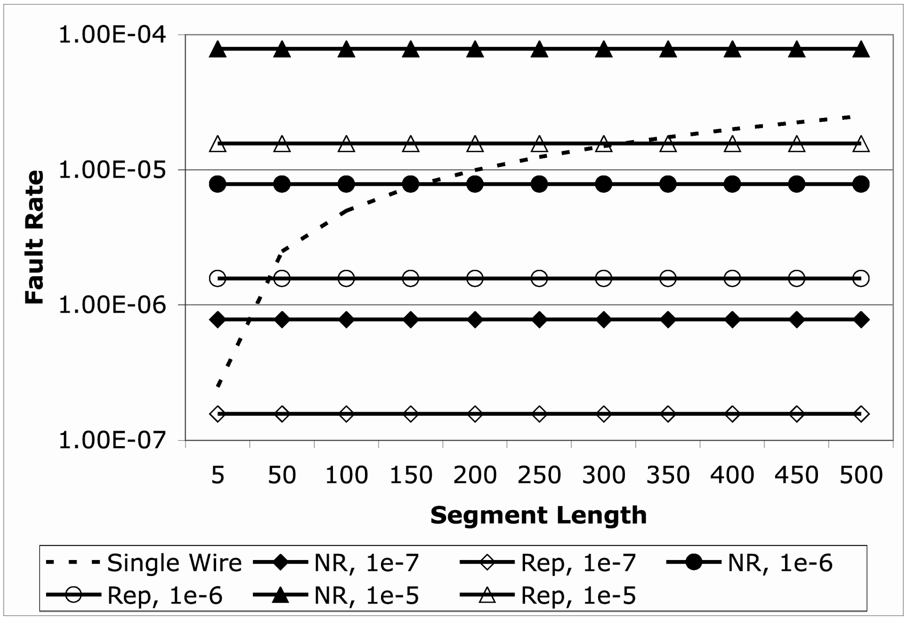


Fig. 4. Fault rates for 5 slice chains (total wire length is $5 * segment\_length$).

If a 50 slice chain is considered, then the fault rates for the single wire and TMR-NR configurations increase by an order of magnitude. Thus, the regions (in terms of F_{ec}, F_{ul}, and the segment length) where TMR-NR should be favored over the single wire configuration remain the same here as they are for the 5 slice chain case. For the TMR-Rep case, the fault rate for the 50 slice chain is only slightly higher than for the 5 slice chain at a given value of F_{ec}. As a result, instead of having the single wire configuration be better than TMR-Rep for segment lengths of 30–35 at $F_{ec} = 100 * F_{ul}$, F_{ec} can increase by another order of magnitude to reach the same point. In other words, if $F_{ec} \leq 100 * F_{ul}$ then TMR-Rep, rather than the single wire configuration, should be utilized for any segment length.

6.2 Fixed Total Wire Length

Having considered wires using a fixed number of slices (1, 5, 50), we now consider a fixed length wire with a variable number of slices. Figure 5 shows the system fault rates for wire lengths of 600 (marked in legend) and 1200 (unmarked in legend) unit lengths. Assuming that a unit length is a single nanomagnet in today's technology, a nonreplicated wire of this length would then be approximately 45μm and 90μm long if the nanomagnets have a pitch of 75nm (Niemier et al. [2007] assumes 60nm wide nanomagnets with 15nm between them). Since the TMR slice configurations add extra components, these wires would be longer.

From Figure 5, we observe that TMR-Rep can offer significant improvements in the fault rate provided that the wire is long enough. We also observe that

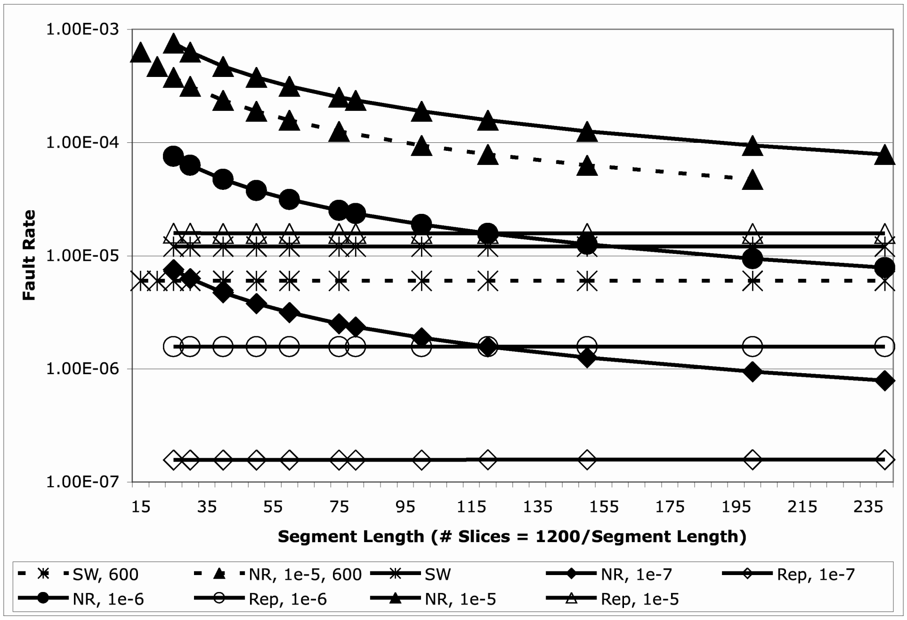


Fig. 5. Fault rates for wires of 1200 unit lengths except for those marked with a 600 which are 600 unit lengths.

the fault rate for the TMR-NR improves as the number of slices is reduced. This result is expected since earlier work has demonstrated that the fault rate of the voters in TMR-NR has a strong effect on the system fault rate [Dysart and Kogge 2008]. As in the previous results, the relationship between F_{ec} and F_{ul} will have the largest impact on which wire organization should be favored.

7. DISCUSSION AND FUTURE WORK

We have investigated a variety of wire organizations to determine how magnetic QCA wires, particularly long wires, should be organized within a circuit. The main driver for determining which organization should be favored is the difference between the fault rate per unit length of wire (F_{ul}) and the fault rate for the components, for example, voters, required to implement the redundant organizations (F_{ec}). The major contribution of this work is the guideline that follows describing which wire organization should be favored for the highest reliability (lowest fault rate).

When comparing the redundant organizations, TMR-NR should be utilized if a single slice is desired due to its lower cost and slightly lower fault rate while TMR-Rep is preferred for multislice organizations. In the list that follows, we identify the shortest wire where redundancy (using the favored technique as listed earlier) offers a higher reliability than the single-wire configuration for both single and multislice organizations. For reference, if using a single nanomagnet as a unit length, a 100 cell long wire is $\sim 7.5\mu$m.

—Case 1, $F_{ec} \geq 1000 * F_{ul}$: Single slice $\sim$ 1600; multislice $\sim$ 1500.
—Case 2, $F_{ec} \approx 100 * F_{ul}$: Single slice $\sim$ 160; multislice $\sim$ 150.
—Case 3, $F_{ec} \approx 10 * F_{ul}$: Single slice $\sim$ 16; multislice any length.
—Case 4, $F_{ec} \approx F_{ul}$: This case was not studied in detail since it is unlikely to occur because the extra components use multiple unit lengths. If it does occur, redundancy should be utilized.

Having identified how wires should be organized from an analytical perspective, physical modeling is necessary to determine the actual relationship between F_{ec} and F_{ul}. Additionally, should it turn out that cells near clock boundaries have higher fault rates than other cells, this modeling will need to be enhanced. This enhancement can be done in a straightforward manner by using a unique PTM for the boundary cells. Finally, a close analysis of the cost of redundancy needs to be completed. The challenge in doing this analysis at the present time is that it is not yet known how much logic/routing can be contained in a single clocking zone. This challenge strongly influences the cost of redundancy and is discussed in more depth in Dysart and Kogge [2009b] and Dysart [2009].

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