

A Simulator for Ballistic Nanostructures in a 2-D Electron Gas

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A multipurpose simulator for ballistic nanostructures, based on classical mechanics of electrons at the Fermi level, has been successfully implemented. Despite the simplicity of the model, the simulator successfully reproduces a number of experimental results, and is shown to consistently match observed current-voltage characteristics and magnetoresistance phenomena. The simulator results provide design guidelines for devices which operate on ballistic transport principles. Using the simulator, preliminary logic structures have been designed based on the ballistic deflection transistor.

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1. INTRODUCTION

As modern nanofabrication advances, semiconductor device dimensions now approach the electron mean free path, defined by the average distance traveled between scattering events due to material impurities or phonon interactions [Hess and Iafrate 1988]. Although quantum-mechanical in nature, electrons in this ballistic regime can be modeled as dynamical billiards, characterized by

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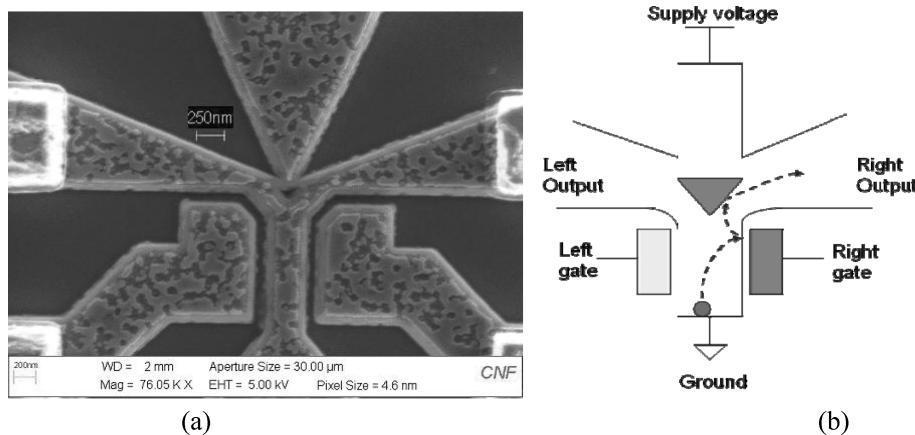


Fig. 1. (a) Scanning electron micrograph (SEM) of a fabricated BDT [Diduck 2006] and (b) its corresponding schematic.

elastic boundary collisions and specular reflection [Beenakker and van Houten 1989]. These behaviors present unique opportunities for defining high-level device functionality based on the shape of physical boundary structures in the plane of a 2-dimensional electron gas (2DEG). Although ballistic effects become more prevalent at very low temperatures (~ 4 K [Song 2004]), ballistic transport has also been observed at room temperature [Hirayama and Tarucha 1993]. Many room temperature devices, such as the ballistic rectifier [Song 2004], T-branch junction with Schottky gate [Galoo et al. 2004], and the Y-branch nanojunction rectifier [Bednarz et al. 2005], exhibit ballistic behavior.

Recently a new transistor prototype operating on the ballistic transport principle has been demonstrated [Diduck et al. 2006]. Termed the Ballistic Deflection Transistor (BDT), this device is expected to achieve terahertz performance. Shown in Figure 1, the BDT is a 6-terminal 2DEG device which uses a triangular deflector and lateral gate voltage to “steer” electrons to the left or right output leads. By guiding the electrical current in this way, a potential difference is produced across the left and right output contacts; this potential difference can then be used to represent logic states.

Nonlinearities and boundary discontinuities in ballistic transport make the derivation of general closed-form analytic expressions impractical. To the best of our knowledge, no commercial tools capable of modeling the overall behavior of ballistic devices such as the BDT are currently available. Within the research community, however, varying levels of success have been achieved for many specific devices by combining the dynamical billiard model described in Section 2 of this article with device-specific semi-classical effects. Beenakker and van Houten [1989] have successfully used a deterministic billiard model to explain anomalous magnetoresistance effects such as “negative Hall resistance” and the “quenching of the Hall effect” in ballistic nanostructures. Mateos et al. [2003] have further applied Monte Carlo methods along with select quantum effects to create models of mesoscopic HEMTs, T-Junctions, and Ballistic Rectifiers.

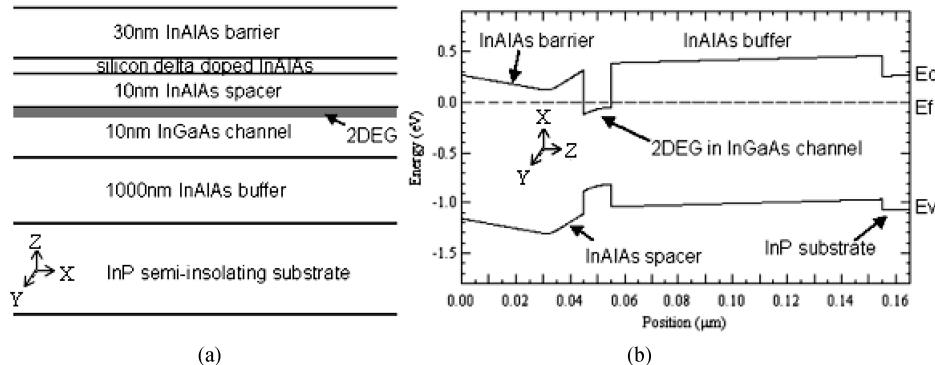


Fig. 2. (a) Multiple layer structure and (b) corresponding energy band for the InAlAs-InGaAs heterojunction [Diduck 2006].

Whereas these previous works have focused on extensive modeling of various physical phenomena, the purpose of our work is to create a low-complexity analysis tool to identify the effects of modifications to the BDT as well as the feasibility of new device structures, which can then be verified through fabrication. In this article, we present a custom Monte Carlo simulator built on a simplified semi-classical ballistic transport model. Section 2 provides an overview of the physical model on which the simulator is based, and describes the mathematical framework behind that model. Section 3 describes the simulator's capabilities, implementation details, and usage in the design and verification of ballistic devices. Section 4 compares simulator results to experimental laboratory results in order to evaluate the accuracy of the model. This section further describes behavioral prediction of the BDT for various geometries. Section 5 provides simulator results for preliminary BDT logic while addressing some of the important future challenges faced in BDT system design and integration. Conclusions are discussed in Section 6.

2. MATHEMATICAL MODELS AND MATERIAL PROPERTIES

2.1 Material Properties and the Billiard Model with Coulombic Interactions

A 2DEG is present in many semiconductor devices wherein the intrinsic energy level dips below the Fermi energy across a thin surface layer, resulting from an applied potential or heterojunction effects. For the purposes of ballistic 2DEG devices utilizing boundary structures, III-V semiconductor heterostructures such as GaAs-AlGaAs and InAlAs-InGaAs have been examined. These materials have been shown to exhibit high mobility with mean free paths in excess of 100 nm at room temperature [Song 2004]. The use of a spacer, shown in Figure 2, physically separates the 2DEG from donor ions, protecting against donor impurity scattering, which is the predominant coherent scattering mechanism [Davies 1998].

Since the conduction band drops below the Fermi level in the channel, the 2DEG does not require any external energy potential, and the majority carriers are electrons with the Fermi energy. In our simulator, we use a single layer

of electrons at the Fermi energy as the representative energy level. The heterostructure is therefore treated as a degenerate conductor [Datta 1995], which is a valid approximation for the low-temperature simulations described in this paper. Future extensions to model room-temperature operation will require a more thorough treatment of energy distributions.

Experiments by Beenakker and van Houten [1989] have shown that geometry-dependent effects in ballistic nanojunctions can be accurately characterized by a billiard treatment of electrons at the Fermi level. In an isolated dynamical billiard system, particles are treated as idealized “billiards,” traveling in straight lines and reflecting off boundaries specularly and with perfect elasticity. Our simulator combines this model with an electrostatic approximation of Coulombic interactions and electromagnetic field forces, using hard-walled boundaries to model an infinite potential well. Applying a first-order Euler approximation, the nonrelativistic position and velocity vectors and for each electron are computed as follows:

$$\vec{r}(x, y, t + \Delta t) = \vec{r}(x, y, t) + [\vec{V}(x, y, t)] \cdot \Delta t \quad (1)$$

$$\vec{V}(x, y, t + \Delta t) = \vec{V}(x, y, t) + [\vec{F}(x, y, t)/m_e] \cdot \Delta t. \quad (2)$$

Here, m_e is the rest mass of the electron, and \vec{F} is the vector sum of the Coulomb forces from neighboring electrons and the Lorentz force from applied electromagnetic fields. The simpler forward Euler method was favored over higher-order approximation methods such as 4th order Runge-Kutta because device behavior was found to be largely insensitive to minor imprecision in individual trajectories; the details of this analysis are described in Section 3 of this article.

In our model, Coulombic interactions between electrons are simplified by imposing a finite range which can be adjusted as desired. For the devices described in this article, a limit of up to 35 nm was found to achieve results comparable with experimental data. Gate contacts (approximated as parallel plate capacitors) capable of significant long-range effects are modeled separately from the mobile current carriers. The main contribution of short-range interactions has been to address transient, localized regions of high electron density, such as those in the immediate vicinity of the applied potentials. The shortcomings of this approach are described in Section 2.3.

2.2 Landauer-Büttiker Formalism

In mesoscopic systems where electron transport is not diffusive, the Landauer-Büttiker formalism describes channel conductance as an electron transmission problem in terms of transmission probabilities:

$$G = \frac{2e^2}{h}MT. \quad (3)$$

This Landauer formula expresses the conductance G of a ballistic channel as a function of M , the number of transverse modes; the fundamental charge e ; Planck’s constant h ; and T , the transmission probability between two leads contacting the ballistic conductor [Landauer 1957, 1970]. Büttiker extends the two-terminal Landauer formula to multiprobe conductors in terms of the current,

I , and the chemical potential μ at each lead [Datta 1995]:

$$I_\alpha = \frac{2e}{h} \sum_\beta (\overline{T}_{\beta \leftarrow \alpha} \mu_\alpha - \overline{T}_{\alpha \leftarrow \beta} \mu_\beta) = \frac{2e^2}{h} \sum_\beta (\overline{T}_{\beta \leftarrow \alpha} V_\alpha - \overline{T}_{\alpha \leftarrow \beta} V_\beta). \quad (4)$$

In this formula, $\overline{T}_{\beta \leftarrow \alpha} = M_{\beta \leftarrow \alpha} T_{\beta \leftarrow \alpha}$ is the total transmission probability from terminal α to terminal β over all available transverse modes $\overline{T}_{\beta \leftarrow \alpha}$ and V is the voltage.

For simple ballistic conductors, the Landauer-Büttiker formula is linear since $\overline{T}_{\beta \leftarrow \alpha}$ is constant. However, to characterize the nonlinear behavior of ballistic devices with complicated geometrical structures within the channel (e.g., the Ballistic Rectifier [Song 2004] or the BDT), the transmission probability is treated as a nonlinear function of device geometry, applied electromagnetic fields, intrinsic energy levels, and material properties.

To obtain the current-voltage (I-V) characteristics of such nonlinear ballistic devices, our simulator employs Monte Carlo methods to compute the transmission probabilities for combinations of parameters such as triangle placement (for the BDT), channel length, channel width, channel intersection angle, carrier density, external fields, gate voltage magnitude, etc. Using the Landauer-Büttiker formula, each set of transmission probabilities completely characterizes a device for its corresponding set of nonlinear parameters.

2.3 Limitations and Future Improvements

Our simulations to date have focused on ballistic properties in cryogenic (~ 4 K) environments, but temperature-dependent effects such as phonon scattering [Hess and Iafrate 1988] and variable energy distributions [Landauer 1957, 1970] will be incorporated in the future. Despite these apparent shortcomings, it has been shown that higher temperatures tend to mask quantum effects such as phase coherence and quantized energy band effects [Hirayama and Tarucha 1993; Mateos et al. 2003; Beenakker and van Houten 1991], which should further reduce currently existing model inaccuracies.

Although stationary impurity and lattice defect scatterers are not expected to have a large contribution at the dimensions investigated by the simulator, the smooth, hard-walled representation of boundaries may introduce nonnegligible errors. Particularly for the III-V heterostructures used, large depletion regions (ranging from about 30 nm in InGaAs-InAlAs to 100 nm in GaAs-AlGaAs) may be present near the etched boundaries from the fabrication process [Song 2004]. This limitation will be addressed in the future by representing boundaries as soft walls with built-in potentials, and treating boundary reflections quasi-specularly, with a probability distribution of reflection angles about the specular path [Hess and Iafrate 1988; Roukes and Alerhand 1990]. Currently, the simulator is designed for steady-state analysis of ballistic devices, but high-frequency simulations in the future will incorporate a complete treatment of Poisson's equation to model the time-varying space charge effects which define boundary depletion regions.

As mentioned before, the current use of a finite electron interaction range to simplify the model has demonstrated experimentally consistent results; gate

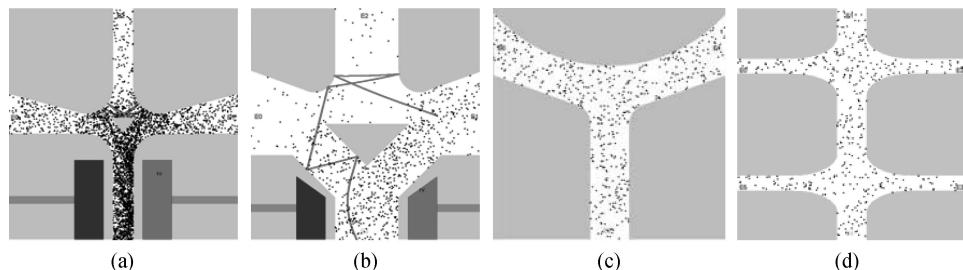


Fig. 3. Ballistic devices: (a and b) BDTs, (c) Y-branch junction and (d) six-terminal Hall junction.

contacts leading to significant long-range effects are modeled separately as parallel-plate capacitors, and the nanostructures presented in this paper appear insensitive to cross-channel gating by mobile carriers. However, future investigations will certainly involve a more thorough treatment of long-range Coulomb effects. This would also require an explicit treatment of donor ions. Such donor charges are currently ignored because the 10 nm “spacer” layer in our InAlAs-InGaAs heterostructure shields the 2DEG somewhat, and we assume minimal gradients in ion distribution density since no gate contacts are layered parallel to the 2DEG. Nonetheless, the donor ions will play an important role in the electrostatic screening of long-range effects, and will be incorporated in a future Poisson solver.

Preliminary investigations using a semi-classical combination of particle and wave interactions have shown that the devices described in this paper are largely insensitive to phase-coherent interference effects. Nonetheless, future work will certainly include these effects to allow simulation of sensitive geometries such as the Aharanov-Bohm interferometer [Datta 1995].

3. SIMULATOR CAPABILITIES AND USAGE

3.1 Design of Ballistic Nanoelectronic Devices

Since the goal of the simulator is to aid in large-scale circuit design, a high degree of flexibility has been maintained both in terms of material/device parameters and the user interface. A large variety of ballistic functionality can be described using the same ballistic transport principle; the ballistic rectifier [Song 2004], Y-branch nanojunction rectifier [Bednarz 2005], and BDT [Diduck et al. 2006], are all defined by the physical structure of boundaries etched into the semiconductor wafer. Since the same physical model applies to all ballistic nanostructures, the simulator provides a design interface for creating completely novel ballistic architectures, as shown in Figure 3. Devices of arbitrary complexity can thus be modeled by beginning with a blank 2DEG “wafer”, and “etching” features into the wafer to define device geometries. Using the simulator to investigate the electrical properties of each device, pitfalls in novel device designs can be found and avoided before costly fabrication takes place.

As will be shown in the following sections, the implemented model is consistent with experimental data for several devices. Nonetheless, the simulator

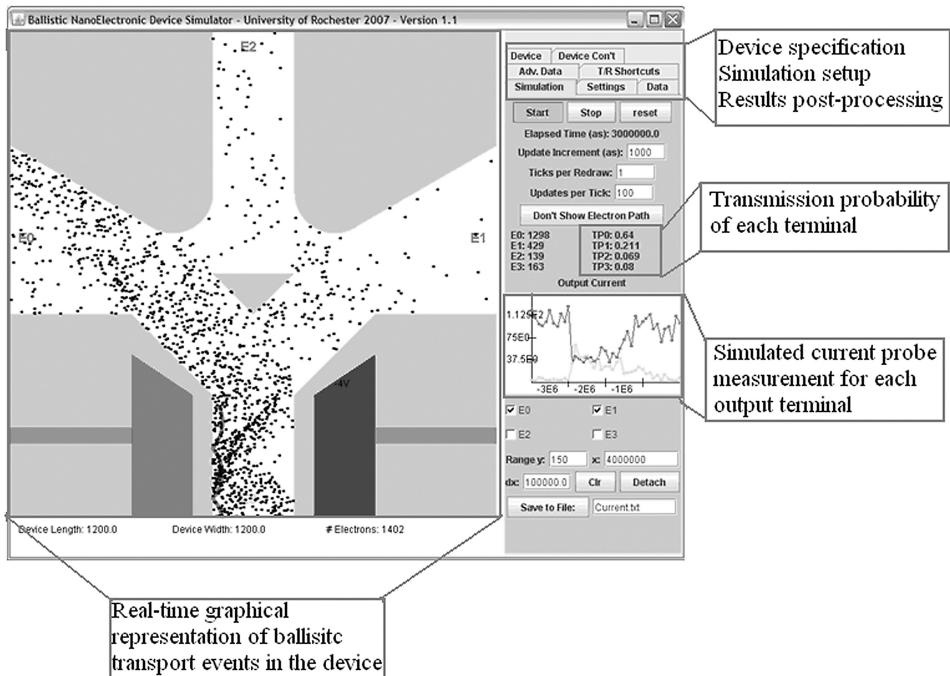


Fig. 4. Overview of simulator interface.

is continuously being improved; in addition to exploring novel ballistic architectures, experimental measurements of fabricated devices will be used to further improve simulator accuracy.

3.2 Analytical Tools for Evaluating Designs

Our simulator provides a diverse set of tools to analyze and characterize ballistic device behaviors. A screenshot of the simulator interface is shown in Figure 4. The panel on the left side is a continuously updated graphical depiction of electron transport within the device, providing the user with visual feedback on the underlying causes of device properties arising from the billiard model. Electron paths through the device are drawn to the screen, giving an intuitive feel for the relative strengths of the various electromagnetic forces present in the device.

The transmission probabilities that characterize the device are dynamically updated while the simulation runs. Thus, it is possible to see the transmission probabilities stochastically converge in real time for any particular set of parameters. The probe measurement graph in Figure 4 permits real-time monitoring of the output currents through any of the output terminals. Of course, all real-time analysis capabilities are strictly supplementary to the basic data output and post-processing tools needed to quantify device behavior; the main motivation behind using real-time analysis is to identify ways the device could be optimized before it is fully characterized. The tabs on the upper right side

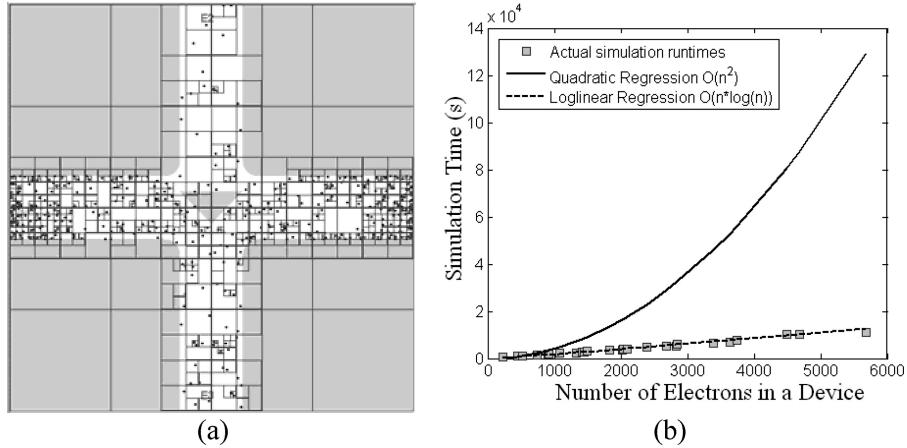


Fig. 5. (a) Graphical depiction of the Barnes-Hut quad-tree data structure. (b) Simulation times versus the number of electrons in a device, following a loglinear regression.

provide access to the simulator functions, in which geometric, material and electromagnetic parameters can be specified.

3.3 Implementation Details and Algorithmic Verification

For the reasons discussed in Section 2, we assume perfect confinement in the z-direction so that the entire simulation occurs in only two dimensions and current flow results from a single, degenerate energy level. Device parameters such as permittivity, Fermi energy or carrier density, etc. are taken from physical measurements.¹ The simulations described in this paper use a relative permittivity of 6.0 and a typical carrier density of $5 \times 10^{11} \text{ cm}^{-2}$.

To determine the rate of electron injection into each channel, we enforce conservation of current at every time-step. The injection angles and initial positions of electrons at each input terminal are used as our Monte Carlo variables. The simulations we present use a Gaussian distribution of injection angles limited to the range $[-\pi/2, \pi/2]$, and a uniform distribution of initial positions over the entrance to each terminal. We also investigated the usage of a cosine distribution of initial angles, but no noticeable differences in device behavior were found. Corner boundaries occurring in channel junctions are represented as circles; such a treatment of junction corners has been shown to induce a non-negligible collimation effect on the angle of electron trajectories [Beenakker and van Houten 1989].

Rather than using the naïve $O(n^2)$ direct implementation, a simplified version of the $O(n \log n)$ Barnes-Hut quad-tree method is used to calculate electron-electron interactions [Barnes and Hut 1986]. This loglinear time complexity of the simulator is shown in Figure 5(b). The electrostatic force vectors are approximated using Coulomb's law. The screenshot in Figure 5(a) depicts the quad-tree structure used in the Barnes-Hut algorithm. The region of the device

¹Special thanks to Quentin Diduck and Hiroshi Irie of our BDT group at the University of Rochester for contributing lab measurements of specific material properties.

is recursively divided into quadrants, and the maximum size of the tree can be defined by setting a maximum recursion depth or a maximum number of electrons per quadrant. In our implementation, any quadrant with two or more electrons is always further divided; at the deepest level, each “leaf” of the tree has only one electron. Such a method determines a tree of neighboring electrons very quickly, since each recursion requires only two atomic comparisons of each electron’s position to place an electron in the correct quadrant. By dynamically “trimming” empty regions from the tree, resources are efficiently allocated. In the conventional Barnes-Hut method, there is no limit on the range of interactions, but for the reasons described in Section 2, we impose a maximum electron interaction range.

Our choice of using the simple “forward Euler” method instead of the more conventional 4th-order Runge-Kutta² method was made based on several different factors. In a pure dynamical billiard model without electron interactions, the Runge-Kutta method is usually a good trade-off, since a larger time step can be used to achieve the same accuracy as a much smaller time step with the forward Euler method. However, our simulator was designed with scalable parallel processing in mind to make use of multi-core, multithreaded hardware, and the Runge-Kutta method introduces extra synchronization bottlenecks that slow down the multi-threaded approach. This is because the Runge-Kutta method requires “hypothetically” stepping forwards in half-step increments, recalculating force vectors, and iteratively redoing the “hypothetical” step to achieve better approximations. Currently, our simulator is unable to use persistent threads between calculating electron movement and calculating Coulomb force vectors, so the Runge-Kutta method introduces additional overhead by having to recreate processing threads after each iteration.

To test the stability of Euler and Runge-Kutta methods for various time steps, we simulate an ideal one-electron cyclotron orbit in a perpendicular magnetic field; in this setup, without loss of momentum, the magnetic flux density required to induce a cyclotron orbit of radius R is given by [Beenakker and van Houten 1989]:

$$B_0 = \frac{mv_f}{eR}. \quad (5)$$

B_0 is expressed in units of Tesla, for an electron of charge e , mass m , and velocity v_f . In general, Runge-Kutta errors result in loss of momentum, while forward Euler errors increase momentum. Thus, a signature of the Euler method is that electrons spiral out of the device, while the Runge-Kutta method results in the electron’s orbit decreasing until it is stationary.

Figure 6 shows the deviation from the constant orbit as a function of time. For a 1 μm^2 device and a Fermi velocity of 5×10^5 m/s, a typical electron will travel through the entire device within 2 ps. From the graph, this translates to about 1% error for the Euler method with a time step of 1 fs, and less than 0.5% error for a time step of 0.5 fs. For the simulations in this paper, a 0.5 fs time step was used. Thus, for our constant-current electric-field devices, the

²Note that the 1st order Runge-Kutta is equivalent to the forward Euler method; from here on, “Runge-Kutta” is used synonymously with “4th order Runge-Kutta.”

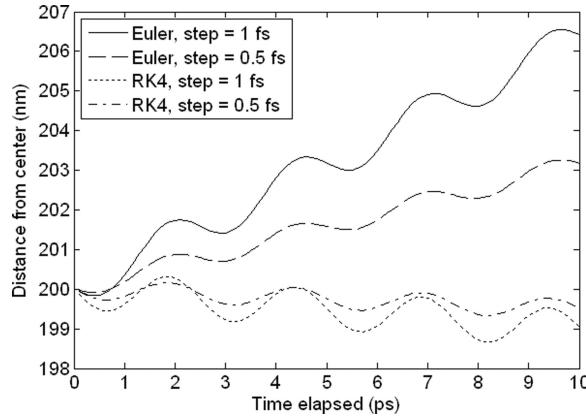


Fig. 6. Radius of electron cyclotron orbit as a function of time. The sinusoidal oscillations represent slight offsets of each orbit from the ideal “center”. The ideal method would consist of a straight horizontal line at 200 nm.

forward Euler method is a reasonable approximation. However, simulation of long-lifetime apparatuses such as particle accelerators would certainly require higher-order methods.

In general, the graphical interface has been invaluable in verifying that algorithms have been correctly implemented. For example, the aforementioned signature behaviors of the Euler and Runge-Kutta methods can be used to detect any significant implementation errors. The interface provides a “click-to-place” feature, allowing electrons to be placed in arbitrary positions within a device by clicking; one can additionally click and drag to define the direction of the electron’s velocity. This allows the direction of electric or magnetic fields to be verified, as well as the vector rotation operations for boundary collisions. The quad-tree depiction can be drawn in real-time, showing that the tree is correctly drawn at each time step.

4. EXPERIMENTAL RESULTS

4.1 Experimental Verification of Physical Model

As mentioned earlier, one of the main goals of the simulator is to unify a large variety of ballistic devices under the same physical model. Simulations have been performed to compare predicted device behaviors with published experimental results. In this section, we present simulator results which have been verified for the ballistic rectifier, multi-probe Hall resistance, and four-terminal cross-junction Hall resistance.

4.1.1 Ballistic Rectifier. The ballistic rectifier is similar to the BDT, and consists simply of a four-terminal cross junction with a triangle in the center. The asymmetry across the y -axis due to the triangle induces a negative net voltage between the bottom and top terminals when an AC current is applied across the left and right terminals. Song [2004] describes the *collimation* of electron angular distribution due to the applied voltage contributing to the net

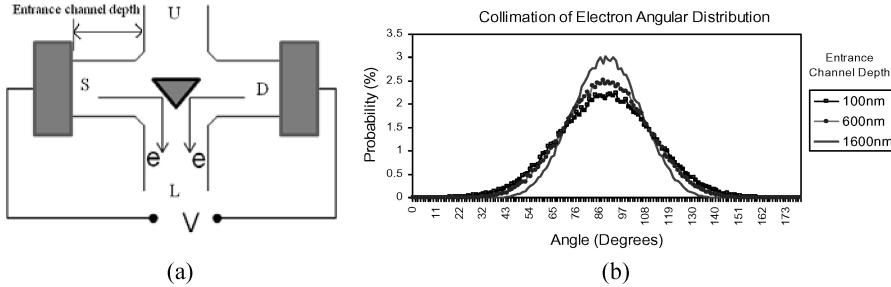


Fig. 7. Collimation effects in entrance channel. (a) Rectifier schematic (b) Collimation of electron angular distribution.

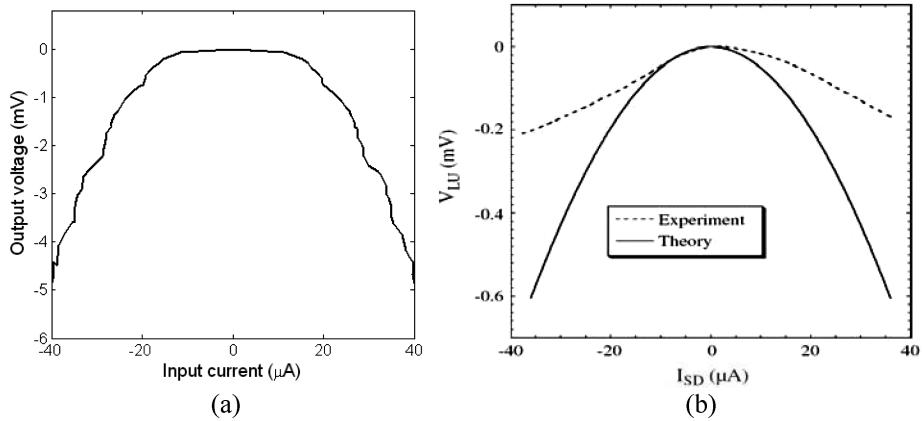


Fig. 8. I-V characteristics of ballistic rectifier. (a) Simulation results from our simulator (b) published theoretical and experimental results in [Song 2004].

negative voltage and rectification in the device. This same collimation has been observed in the simulator, verifying the ballistic mechanism through which electron angular distribution responds to the applied electric field. As shown in Figure 7, the simulator shows that a longer entrance channel translates to a narrower angular distribution of electrons entering the central junction, due to the longer duration of acceleration from the applied electric field.

Simulation results for the ballistic rectifier, shown in Figure 8(a), agree with original theory predicting a quadratic relationship between input current and output voltage, shown in Figure 8(b) [Song 2004]. Although some numerical error is expected since no precise device dimensions were given for the rectifier device, the overall data trend predicted by the simulator is comparable to the published theoretical and experimental results.

4.1.2 Low-Field Hall Resistance. Simulations by Beenakker and van Houten [1989] have successfully applied the billiard model to explain certain magnetoresistance phenomena such as the “quenching of the Hall effect,” “negative Hall resistance,” the “last Hall plateau,” and “bend resistances”. Our simulator was used to reproduce some of these effects, particularly the “quenching

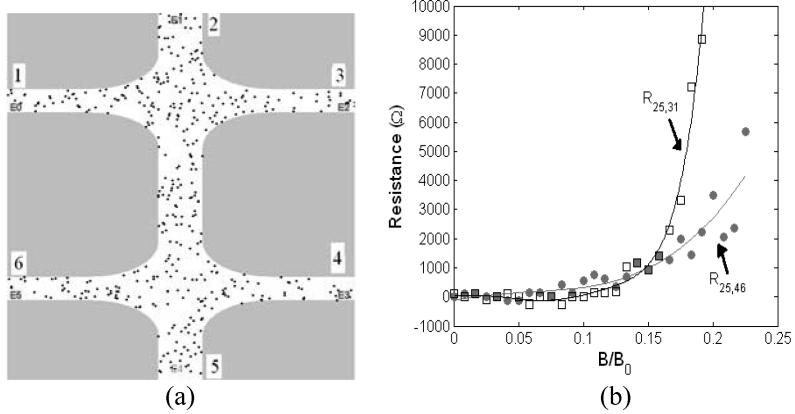


Fig. 9. Hall resistances (a) Simulated device (b) Hall resistance predicted by our simulator.

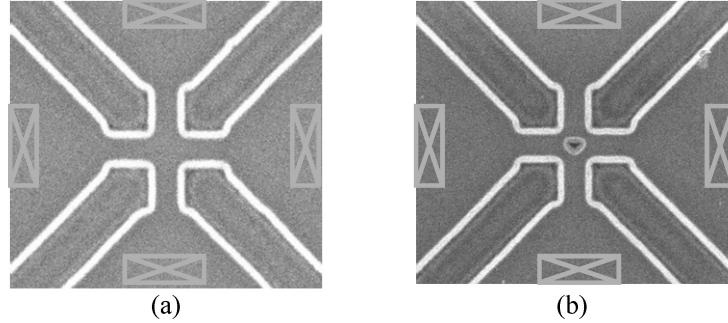


Fig. 10. SEM images of fabricated cross junction devices (a) without (b) with triangle.

effect” and the “negative Hall resistances,” to help verify consistency of the model. For this simulation, we used the six-terminal structure shown in Figure 9(a). Electrons are injected at the bottom lead with a voltage potential at the top lead, and a perpendicular magnetic field is applied ranging from 0 to $0.3B_0$, where $2B_0 = B_{\text{crit}}$, and B_{crit} is the field which confines an electron to a cyclotron orbit of diameter equal to the width of its ballistic channel. As shown in Figure 9(b), our simulator results demonstrate the same quenching of the Hall effect and negative Hall resistances described by Beenakker and van Houten [1989]. In particular, the “quenching of the Hall effect” can be seen at $B/B_0 \approx 0.15$, with an accompanying “threshold value” at which increasing Hall resistance is observed. Negative values of low-field Hall resistances were also obtained, as shown between $B/B_0 \approx 0.05$ and $B/B_0 \approx 0.12$.

4.1.3 Four-Terminal Cross Junction Hall Effects. Our research group has recently quantified the contribution of a triangle in the center of a four-terminal cross junction, shown in Figure 10, to the measured Hall resistance [Irie 2007]. These measurements have been reproduced by our simulator, also providing additional insight into the nature of fabricated “triangle” structures.

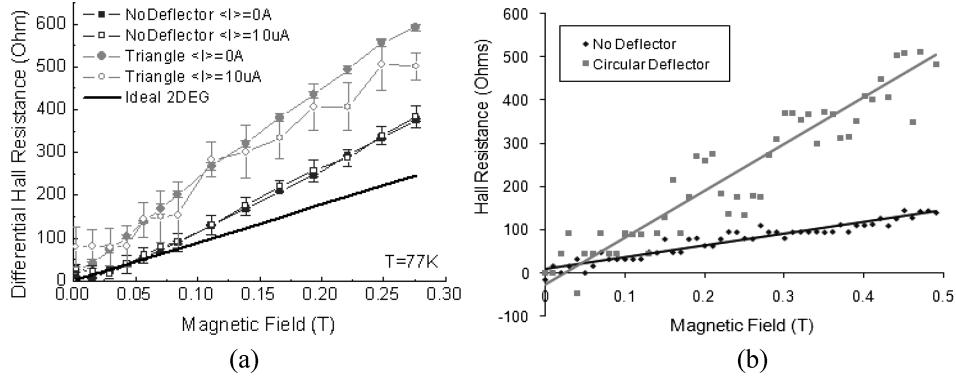


Fig. 11. Hall resistances for cross-junctions. (a) Measured resistances [Irie 2007] (b) Simulated resistances.

In general, experimental measurements (Figure 11(a)) have shown that the triangle in the center increases Hall resistance, as expected in the ballistic transport model. This is due to an enhancement of the “guiding” effect of the magnetic field, which deflects electrons towards the side exit leads. Because fabrication limitations resulted in severe rounding of the triangle corners, the simulated results in Figure 11(b) were generated using a circular deflector. Although the simulation temperature was significantly lower than the experimental temperature, the simulated Hall resistances in the cross junctions followed the same trend as the experimental values, and increased when a deflector was inserted. The error bars in the experimental results indicated greater noise for the junction with a deflector, and this response was also observed by the simulator.

4.2 General BDT Characterizations and Design Guidelines

4.2.1 General I-V Characteristics with Experimental Support. Simulations have been performed to determine I-V characteristics of the BDT. For some BDT designs, the I-V curve exhibits a non-monotonic behavior, shown in Figure 12(a), indicated by a peak in the current as voltage changes. Under certain combinations of geometry, voltage, initial carrier injection angles, and positions at the entry channel, a decrease in current with increasing gate voltage is observed. Figure 12(b) depicts this situation with no electron-electron scattering, a limited range of initial carrier states, and a relatively high gate voltage to make the mechanism of negative gain more obvious. In general, particle interactions randomize and smooth the underlying, discontinuous, single-electron billiard characteristics [Roukes and Alerhand 1990].

In addition to the twin-peak behavior shown in Figure 12(a), simulations have produced BDT designs with current-voltage characteristics closer to conventional voltage transfer functions, with a linear transition region between two saturation regions, as shown in Figure 13. By identifying the billiard trajectories which resulted in negative current slopes, it was possible to optimize for desired characteristics to obtain the broadened saturation region. From a

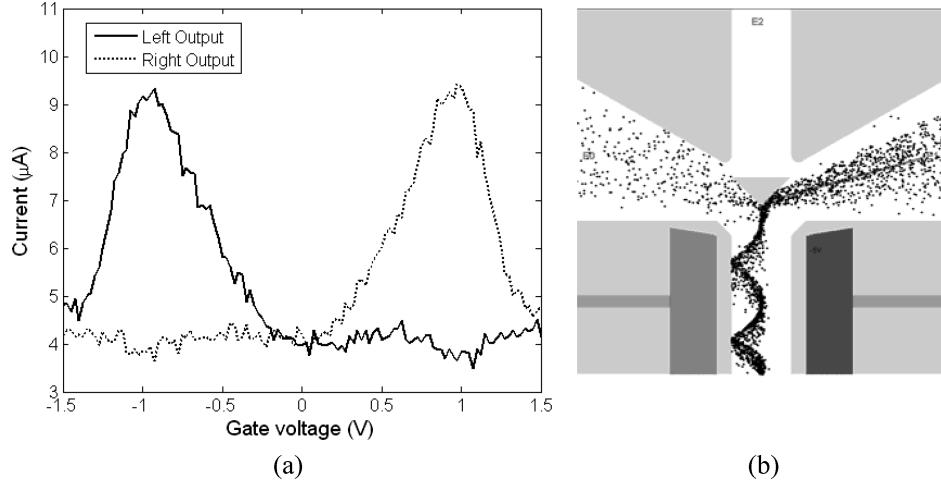


Fig. 12. (a) Current-voltage characteristics of BDT (b) Simulated view of current in opposite direction of steering voltage.

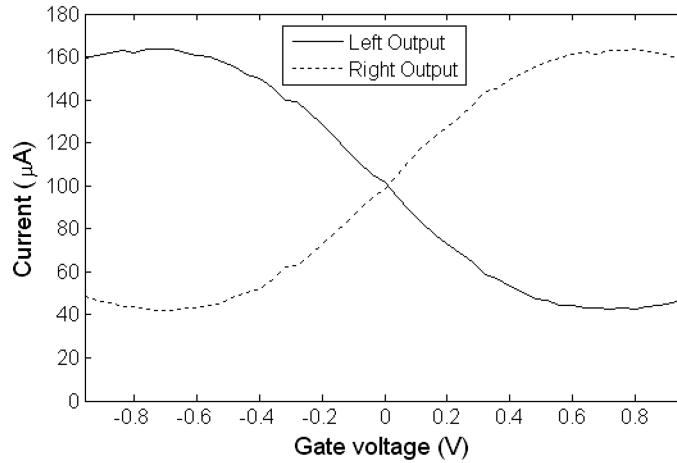


Fig. 13. BDT I-V characteristic exhibiting nearly monotonic behavior.

logic design standpoint, having both possible classes of behavior available could be quite useful. As fabrication techniques improve, this type of control will allow for more advanced geometrical optimization, enabling new types of device behaviors.

4.2.2 Triangle Position Effect on Leakage Current. Ideally, all the current flowing into the device should contribute to the gain, and no current should flow out the top terminal; however, in reality, there is leakage current. One factor that was found to have an important effect on this leakage current was the vertical position of the triangle island within the device. An “offset” value defines the vertical position, denoted as a percentage of the triangle’s vertical length that the triangle’s center deviates from the exact center of the entire

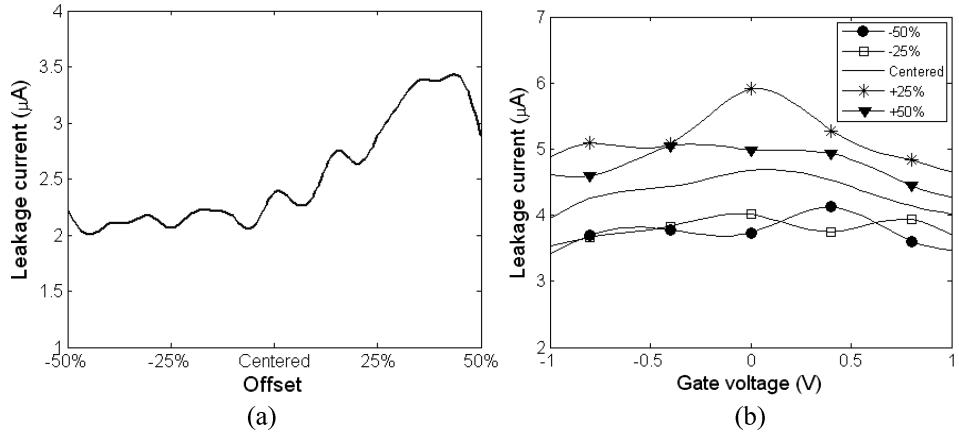


Fig. 14. Leakage current as a function of (a) triangle position and (b) gate voltage.

device. As shown in Figure 14, the triangle should be placed between 10% and 25% of its own length lower than the exact center of the device to minimize leakage current. Although placing it lower than 25% does not appear to further reduce leakage current, placing it above the center of the junction can result in more than 50% increased leakage (depending on the gate voltage).

4.2.3 Corner Sharpness Effect on Gain. One of the most pronounced results of BDT simulations came from representing imperfections in fabrication using rounded corner edges in the central junction. The dullness of these corners is defined by a “radius of curvature,” representing the radius of a circle inscribed in the wall between two intersecting channels. This effect is important to consider, since Beenakker and van Houten’s [1989] experiments described in Section 4.1.2 explained previously inexplicable magnetoresistance anomalies precisely through this “dull junction corner” effect, with the same definition of dullness as a circle radius [Roukes and Alerhand 1990]. When all other parameters were kept the same but this radius of curvature was changed, there was a strong effect on device performance.

As shown in Figure 15(a), the output current is heavily dependent upon the radius of curvature. One potential reason for this is shown in Figure 15(b), where the large radius is responsible for scattering the electron to the opposing output lead. The randomness in electron trajectory as corner radii increase has been thoroughly examined by Roukes and Alerhand [1990].

4.2.4 Timing Simulations. Simulations have been performed comparing net output current against time for changing gate voltages. The time from the rising edge of the input voltage to the rising edge of the net output current was determined for different device geometries, indicating some of the factors affecting device response time and revealing typical operational frequencies. In general, response times fall into a range between 0.3 and 2 ps suggesting operational frequencies for the BDT from 0.5 THz to about 3.3 THz. As expected, smaller devices tend to have faster response times, but lower output currents

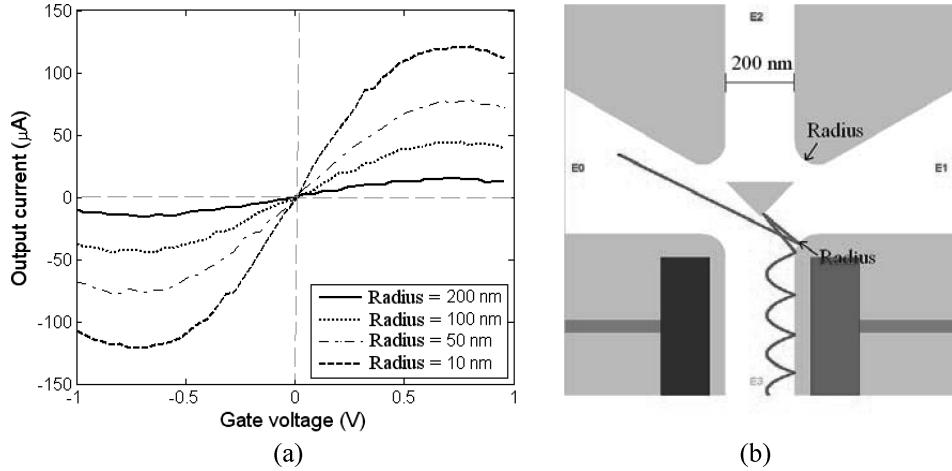


Fig. 15. Output current dependence on the increasing radius (a) Simulated results (b) Schematic with radius of interest labeled.

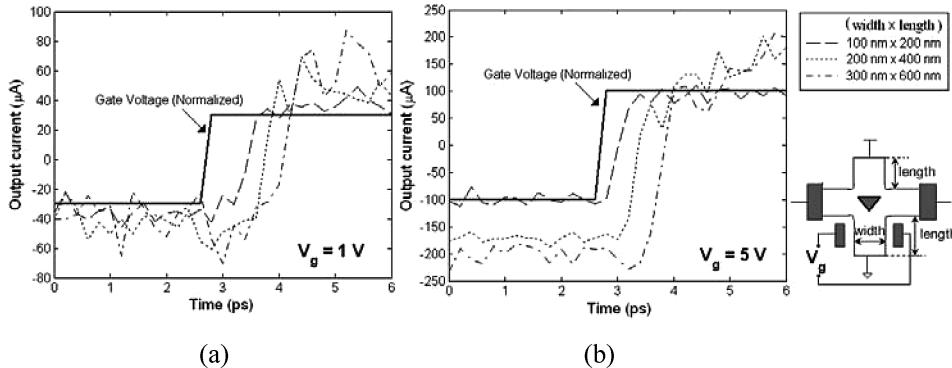


Fig. 16. Timing simulations of the BDT for multiple geometries with (a) 1 V input and (b) 5 V input.

than larger devices; a larger gate voltage decreases response time, as shown in Figure 16.

5. NEW BALLISTIC DEVICE STRUCTURES

5.1 BDT NAND Gate

Logic design and integration of the BDT will certainly be an important and challenging endeavor. To maintain high operational frequencies in devices, it is good to consider using integrated devices made of multiple BDTs. Rather than having diffusive interconnects between every BDT unit, higher level functionality could be implemented on a contiguous section of 2DEG in order to avoid contact impedances. In fact, some researchers have expanded upon this idea of high-level single-unit functionality, incorporating an entire half-adder in a single unit [Reitzenstein et al. 2003], while sacrificing ease of fabrication and

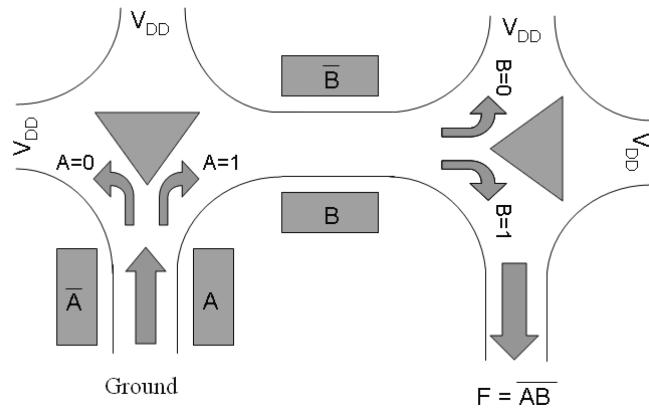


Fig. 17. Schematic of a BDT NAND gate.

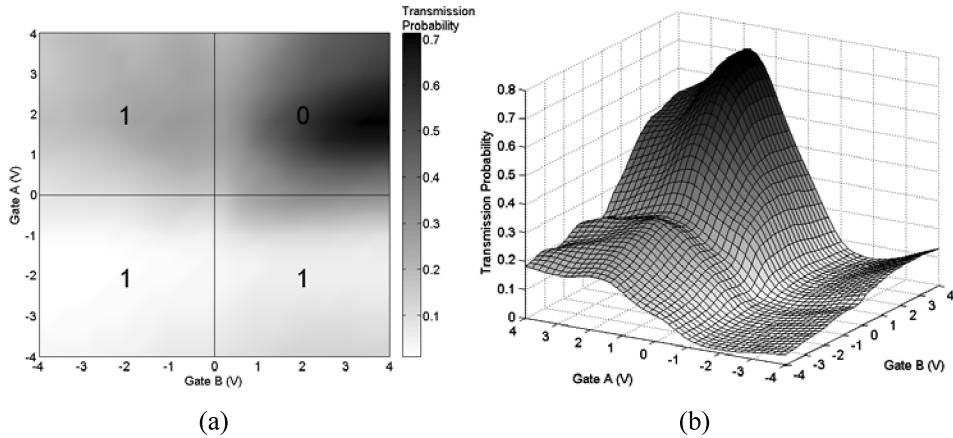


Fig. 18. BDT NAND gate (a) contour map and (b) corresponding surface.

increasing device complexity. One somewhat simpler BDT-based device recently investigated with the simulator is the BDT NAND gate, shown in Figure 17. The large gray arrows in Figure 17 represent the gate input and output, while the smaller gray arrows represent the possible electron paths depending upon the input state. As shown, electrons would only travel from the input to the output when inputs A and B are both high (set to logic 1).

Since the majority carriers are electrons, the output F in the diagram would provide negative current when A and B are both high. The output lead would consequently be pulled to a negative voltage, representing a “0” logic state. Being logically complete, the NAND gate alone theoretically enables general BDT logic design. Simulations have been performed to find transmission probabilities at the output lead for a range of input voltages. The transmission probabilities are also provided as an output current in our simulator. The NAND gate behavior shown in Figure 18 was achieved through geometric optimization of the structure in Figure 17, and shows that the design concept appears promising.

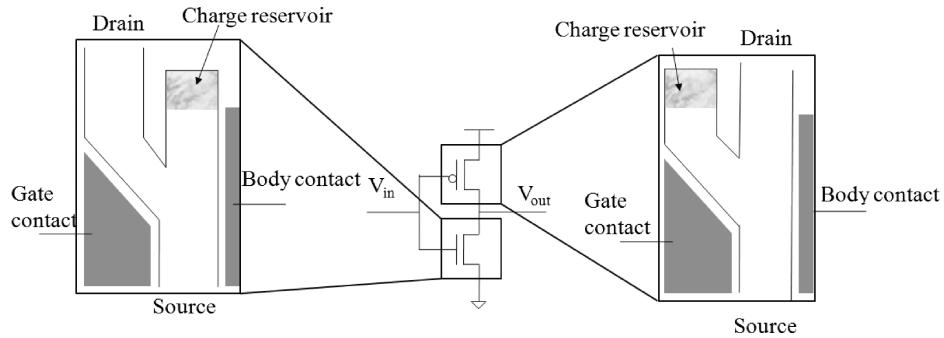


Fig. 19. Schematics for non-inverting (left) and inverting (right) BRT. Analogous to the NMOS and PMOS transistors, respectively, an inverter can be achieved in the fashion of the CMOS inverter (center).

5.2 Alternative Ballistic Transistor Design

Based on simulator indications, another possible transistor design based on ballistic nanostructures has been conceived. Similar in concept to the HEMT, the conductivity through a ballistic channel is changed in response to a gate voltage. However, rather than placing the gate parallel to the 2DEG, a skew Y-branch structure is used, incorporating a gating structure similar to that used in the BDT such that the gate is coplanar with the 2DEG. Termed the Ballistic Redirection Transistor (BRT), these devices shown in Figure 19 were designed with digital logic and integration in mind.

Since the x-component of the velocity only needs to be altered slightly to transition from one branch to the other, there is a sharp transfer function between the ratios of the transmission probabilities through the two branches. For the noninverting design (shown in Figure 19(left)), the ballistic transport ensures a probability bias for the straight branch into the reservoir region. As charge accumulates in this branch the incidence of backscattering increases, causing the source-drain impedance to be high. As a gate bias is applied, the transmission probability favors the left side, permitting high source-drain current. For the inverting design, shown in Figure 19(right), the opposite is true in both cases. Since the gate contact is coplanar with the 2DEG, compared to the parallel-plate gating structure in the HEMT, the operational frequency determined by the RC time constant is expected to be significantly higher.

Another important characteristic of the BRT is that the geometry is relatively simple and robust, since the channel width can be the smallest feature size in the device. Furthermore, the inverting and non-inverting designs are schematically equivalent to PMOS and NMOS transistors, respectively, and thus CMOS design paradigms are directly applicable to BRT devices. Using complementary BRT (CBRT) designs, rail-to-rail output voltage swings can be achieved. Figure 20 shows the voltage transfer characteristic (VTC) of a CBRT inverter made following a schematic design analogous to the CMOS inverter. A bias for the “0” output state was initially observed, but can be corrected by adding a static 1.5 V bias potential uniformly to the “body” of the BRT to make

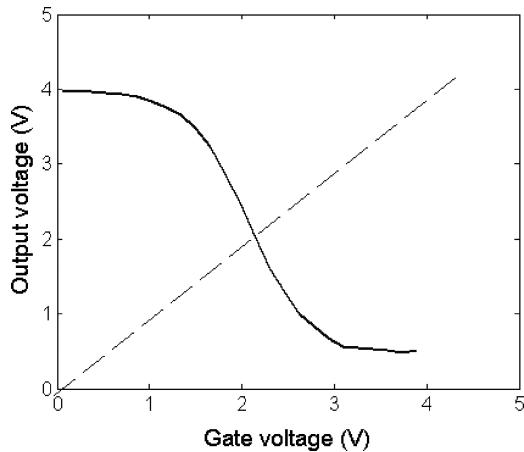


Fig. 20. Simulated VTC of a CBRT inverter.

it easier to steer the electrons between the branches. As a static potential this bias is not expected to hinder the performance of CBRT logic.

5.3 Future Challenges and Considerations in Ballistic Logic

Although there are still a great many challenges to be resolved before BDT and general ballistic logic become commercially feasible, the future of ballistic electronics appears promising. Many issues, such as limiting contact impedance, reducing edge effects, and improving transconductance are ongoing concerns in the semiconductor industry.

For ballistic nanostructures in particular, key considerations today include characterizing simple structures that will be the primitive building blocks of ballistic nanostructure devices in general, such as Y-branch junctions, multi-terminal junctions, and 2DEG interconnects. For logic design and device integration, precise timing and delay characterizations will require creative measurement techniques to address the predicted terahertz frequency ranges. Also, in order to create robust integrated circuits, amplification methods are needed to ensure that signal strengths are sufficient to drive large loads (e.g., I/O pads).

Fortunately, these challenges represent more of a road map for future work rather than being insurmountable hurdles. Much literature exists detailing laboratory characterizations of simple ballistic nanojunctions. The voltage transfer function of the proposed CBRT inverter shows a transition region sufficiently steep to correctly interpret intermediate voltages and amplify them by pulling up to the source voltage or down to ground. Given the rail-to-rail design of the CBRT, higher-level functions such as NAND or NOR are expected to achieve a similar amplification effect. Ultimately, as smaller and smaller feature sizes are used in nanofabrication, ballistic transport behavior should continue to improve, and enormous returns can be expected as the basic challenges are eventually resolved.

6. CONCLUSIONS

A multipurpose ballistic nanoelectronic device simulator has been created successfully. Since ballistic nanodevices operate on the same transport principle, their behaviors can be predicted using our simulator's generic framework. Various published experimental and theoretical results on ballistic devices have been replicated in the simulator, confirming that the semi-classical billiard model of ballistic electron transport, despite its simplicity and limitations, is effective in describing 2DEG nanoelectronic devices.

As part of our ongoing research at the University of Rochester, the simulator has been used to investigate properties of the Ballistic Deflection Transistor (BDT). Several design guidelines are presented based on simulation results. In particular, we show that leakage can be reduced by a lower position triangle island and corner defects may limit the ballistic steering effects of the applied gate voltage. Comparing the I-V characteristics of different BDT designs in the simulator showed that different types of BDT functionality can be designed by varying the geometry of the device. Timing simulations of the BDT have indicated operational frequencies in the terahertz range.

The progression of nanoelectronic devices into the ballistic regime marks the dawn of a new generation of electronics. Novel designs, such as the ballistic half-adder or the BDT gates described in this paper, show that ballistic logic circuits will soon open the door to entire new worlds of electronics.

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