

123456

Project:

DM1097

Current Revision:

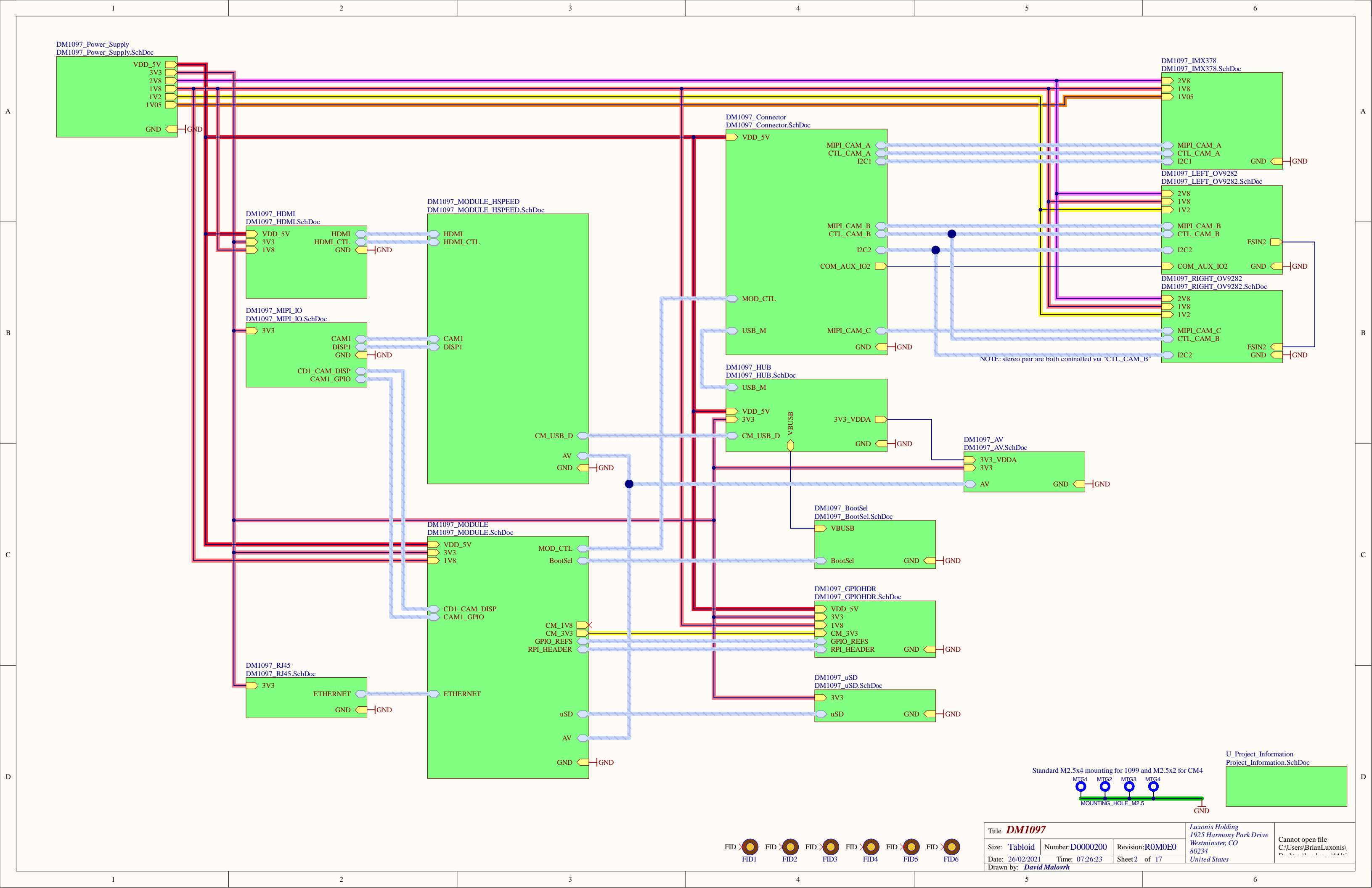
R0M0E0

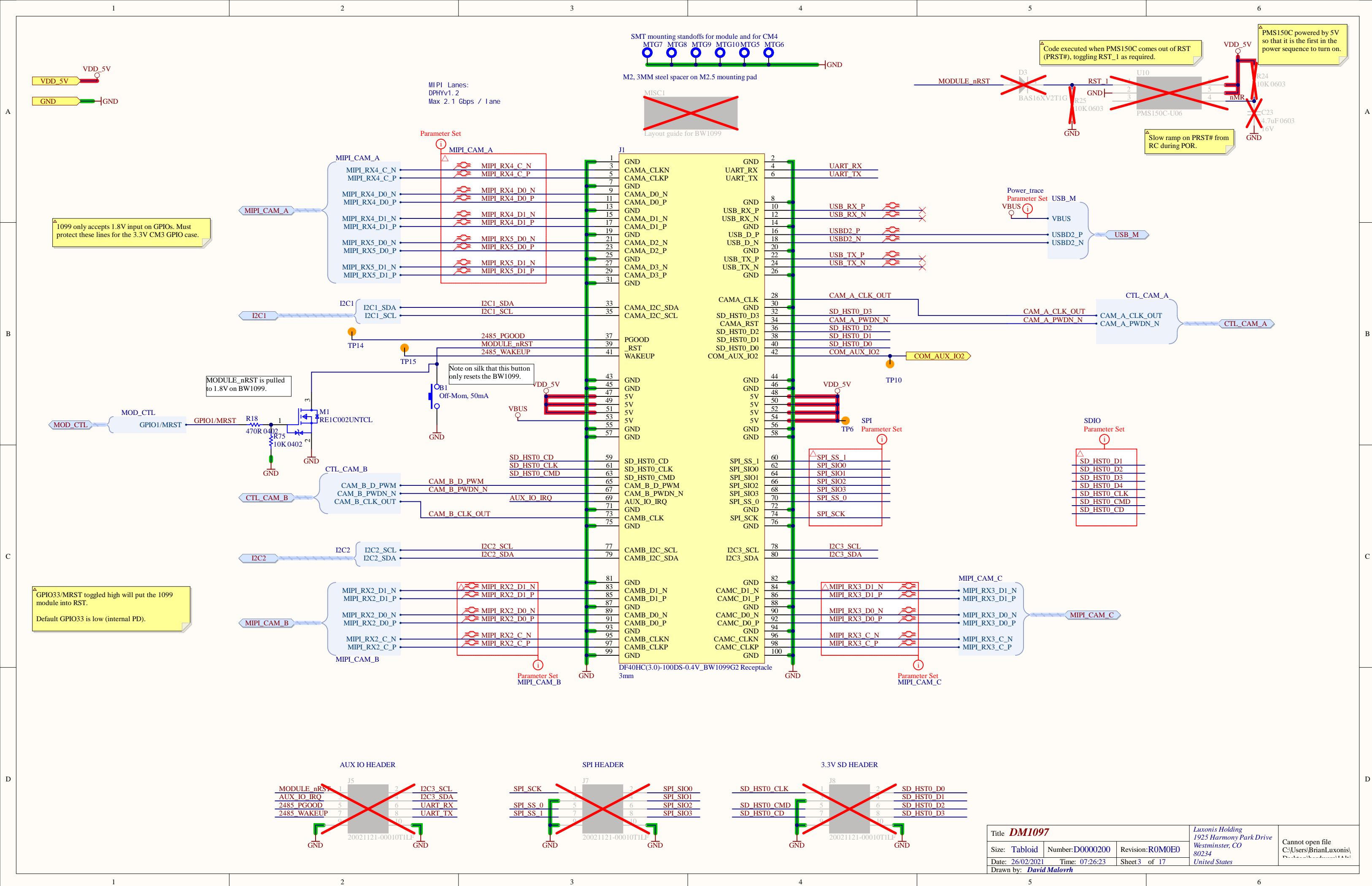
BW1097 Revision History:

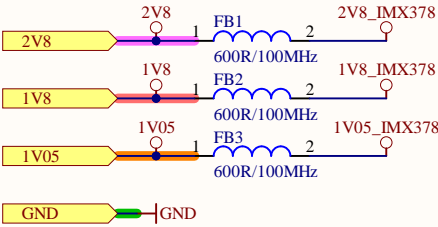
Date	Revision	Reason for Change	Changes Implemented
11/29/2019	R1M1E2 -> R2M2E3	1) Updating board to be aligned with Gen2 1099 boards, with SPI and uSD 2) Header jumpers are unnecessary and expensive, and can be repalced with a simpler solution 3) Existing design was not standardized on LuxonisMaster library format 4) Series input power resistor is a sense resistor, but should be 0 ohm 5) The OV9282 LDOs have unnecessary components compared to the most recent baseboards 6) Depopped R26 had no set component value. 7) HDMI connector footprint was found to be slightly crooked 8) PGOOD LED driver did not match other boards 9) DMG1012 FETs were automotive qualified, changed to non-automotive for entry into LuxonisMaster 10) Passive component equivalent part substitutions as library was built up	1) Leveraged 1098OBC connector schematic. Updated J1 Hirose connector to be the Gen2 version with proper pin names, Added three 10-pin headers (not populated) to break out AUX io, SPI io, and uSD io, same as on 1098OBC. Updated schematic net names, harnesses and connections to accommodate the Gen2 changes. 2) Removed header jumpers and exchanged with resistor jumper networks 3) Updated schematic and component information to align with LuxonisMaster library system. 4) Changed input series resistor to 0603 0ohm to match 1098OBC, 1098FFC, and 1094. 5) Removed RC circuit on OV9282 LDOs to match 1098OBC 6) Added 47K as default, but R26 remains depopulated 7) Corrected HDMI footprint to match recommended PCB layout from Wurth 685119134923 8) Changed transistor on PGOOD LED to be RE1C002UNTCL, to match other boards (Q5) 9) Changed from DMG1012TG-7 to DMG1012T-7 (Q1, Q2, Q3, Q4, Q6) 10) Many passive components did not exist in LuxonisMaster, so in some cases, equivalent from a different manufacturer are used. For 332R and 100K resistors, all were standardized to 0402, rather than a mix of sizes

DM1097 Revision History:

	R0M0E0 -> R0M0E1		
	R0M0E1 -> R1M1E2		
	R1M1E2 -> R2M2E3		







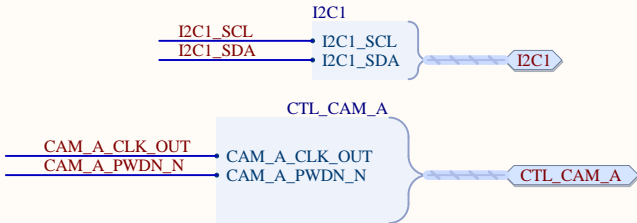
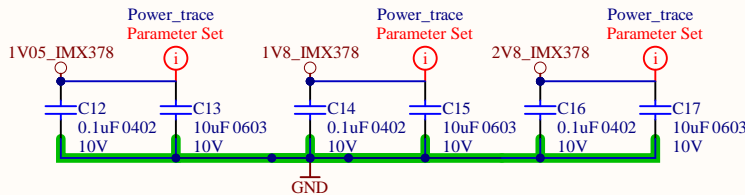
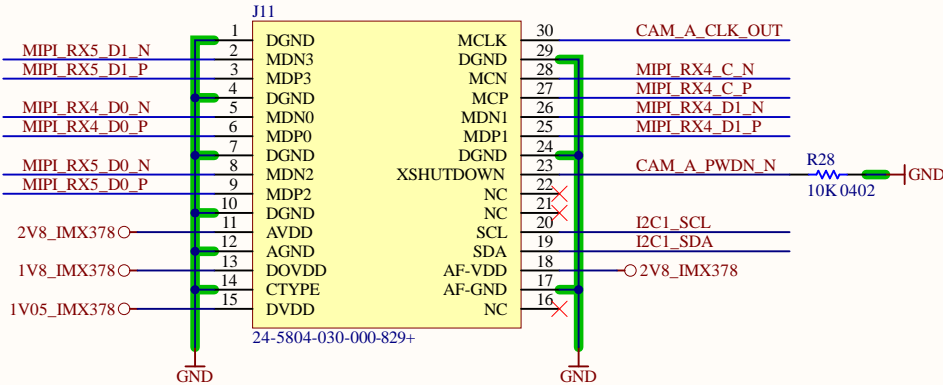
Place FBs and caps close to their associated camera connector.

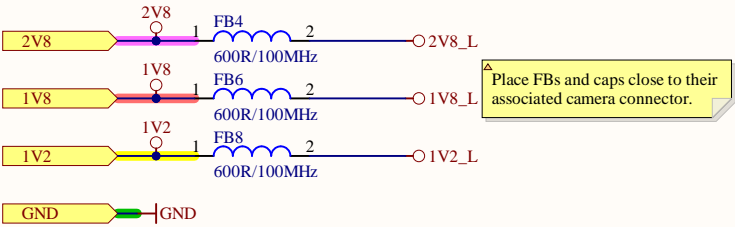
On the BW1097, the IMX378 camera module is hardwired into the "Cam-A" logical position. This means the logic which used to be required to support the module being plugged into different physical connectors (and different logical positions) is no longer needed and can be removed.

Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.

### IMX378 MODULE CONNECTOR

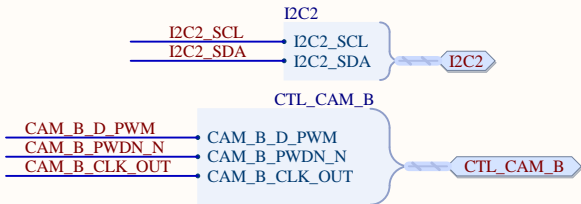
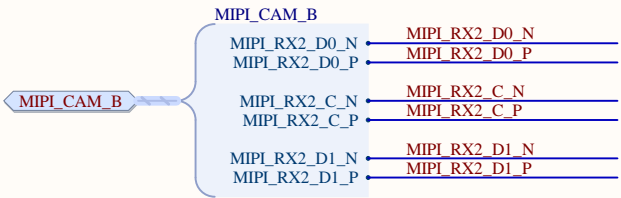
MODULE & SENSOR INFORMATION			
MODULE	A12N02A-201	I2C Clock Rate	1000 kHz Max
SENSOR	IMX378-AAQH5-C 12.3 Mega pixel CMOS 1/2.3 inch	I2C Address (8 bits)	0x34 (Sensor)
			0x18 (VCM driver)
			0xA0 (EEPROM driver)
MAX RESOLUTION	4056x3040	Sensor Clock Input	6 - 27 MHz





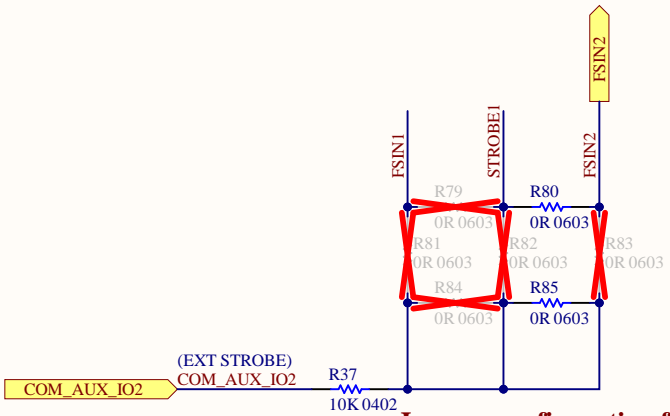
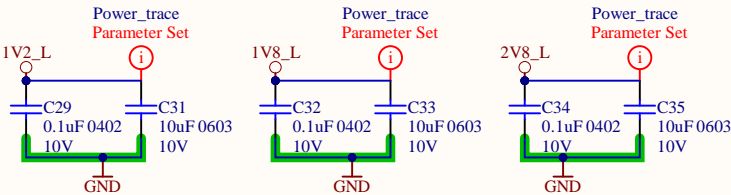
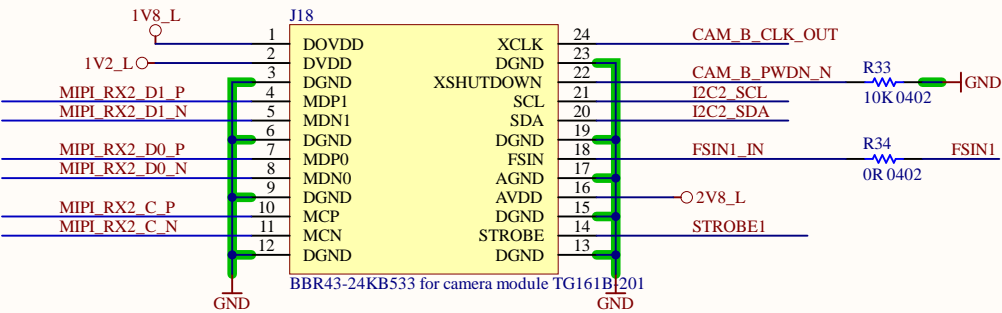
MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-0JG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

Supply Information			
Supply Name	Module	Sensor	Vol tage
DOVDD	VDD-I0	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA



Mark "LEFT" on PCB

Place so that is the module's left camera.



### Jumper configuration for FSIN and STROBE pins

PCB NOTE: Add below diagram to the PCB

#### Supported Modes of Operation

- NO SYNC
- NORMAL
- TIMING MASTER
- TIMING SLAVE

This header is used for configuring the STROBE signal direction between the camera boards by using jumpers. A strobe signal may drive FSIN signal for waking up a sensor from its low power mode. See the "Supported Modes of Operation" note for supported jumper settings.

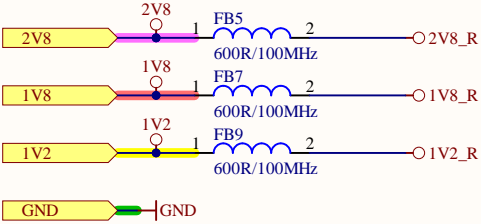
- "NO SYNC" is the mode in which none of the camera modules is excited by any strobe signal.
- "NORMAL" mode means STROBE mechanism works only among the stereo cameras themselves. In this mode, CAM1 strobe is connected to the CAM2 FSIN input.
- "TIMING MASTER" mode means CAM1 STROBE signal drives the EXT\_STROBE signal as well as the CAM2 FSIN input. EXT\_STROBE signal circulates among the other camera ports so that one camera module can manage the timing of all cameras within the system.
- "TIMING SLAVE" mode uses external strobe signal which is driven externally by another camera. In this mode, CAM1 and CAM2 are excited by the EXT\_STROBE signal.

Note that, at most only one camera can be in the "TIMING MASTER" mode at a time. STROBE generation and FSIN reception should be configured via software.

Because the stereo pair of OV9282 modules hard wired to CAM\_B no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM\_PWDN, and "CAM2" (Right), is reset via CAM\_PWM. This also means that the signal CAM\_AUX\_I01 is no longer required here, as that was only possible if the stereo pair were connected to CAM\_C or CAM\_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

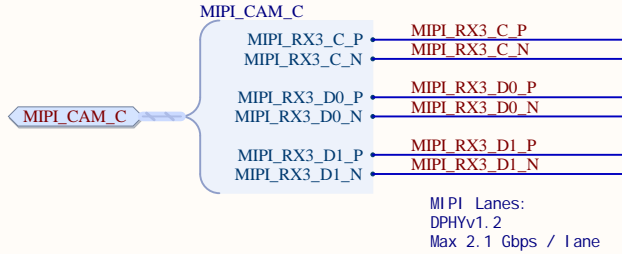
CAMERA CONNECTOR RESET CONNECTION TABLE				
CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM 1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_I01	CAM_AUX_I01



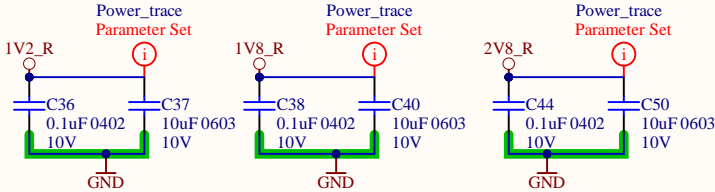
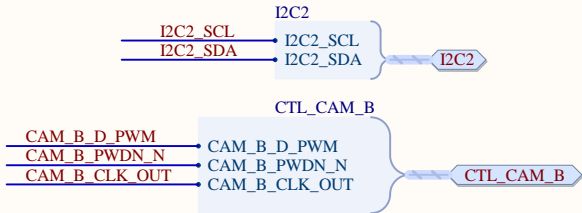
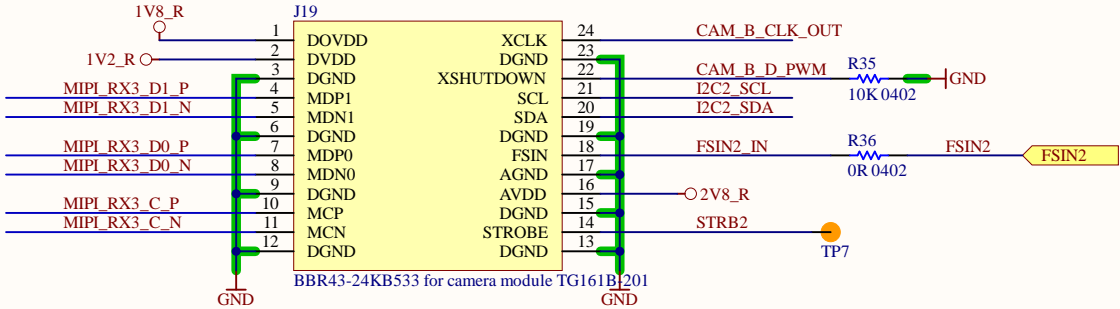
Place FBs and caps close to their associated camera connector.

MODULE & SENSOR INFORMATION			
MODULE	TG161B-201 OR AN01V32-QJG	I2C Clock Rate	400 kHz Max
SENSOR	OV09282-GA4A B&W 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	0xC0(W) 0xC1(R)
MAX RESOLUTION	1280X800	Sensor Clock Input	6 - 64 MHz (24 MHz typ.)

Supply Information		Voltage	Max Current
Supply Name	Module Sensor		
DOVDD	VDD-I/O	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA



Mark "RIGHT" on PCB  
Place so that is the module's right camera.

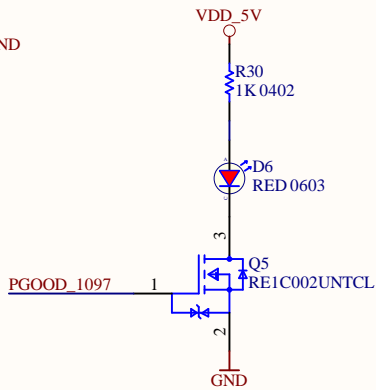
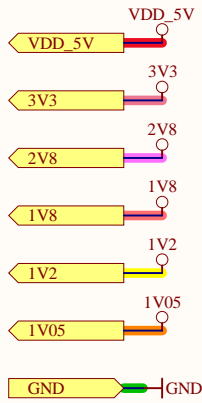


Because the stereo pair of OV9282 modules hard wired to CAM\_B (below) no additional reset circuitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM\_PWDN, and "CAM2" (Right), is reset via CAM\_PWM. This also means that the signal CAM\_AUX101 is no longer required here, as that was only possible if the stereo pair were connected to CAM\_C or CAM\_D

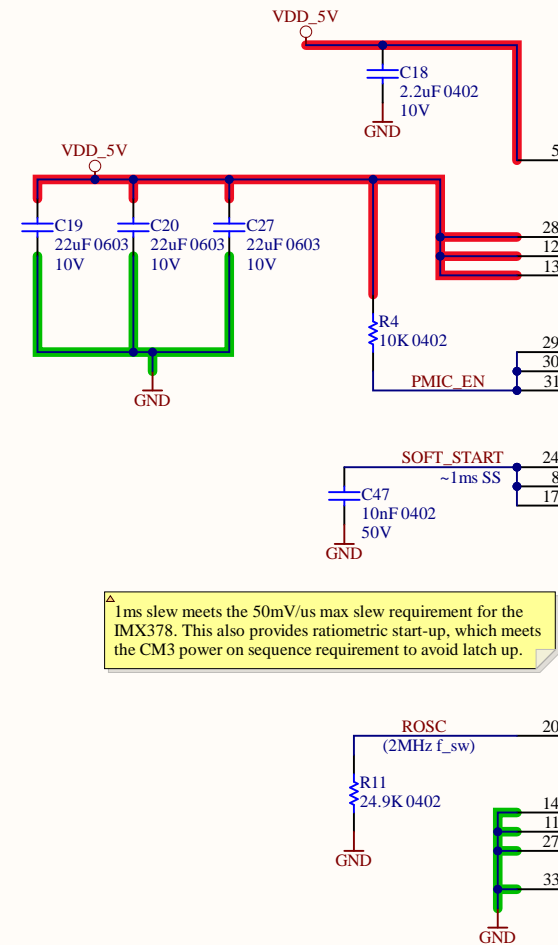
OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAM NO	CAMERA CONNECTOR RESET CONNECTION TABLE			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM 1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX_101	CAM_AUX_101

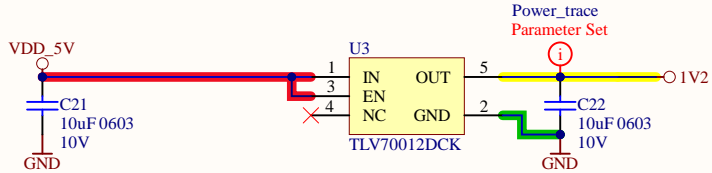
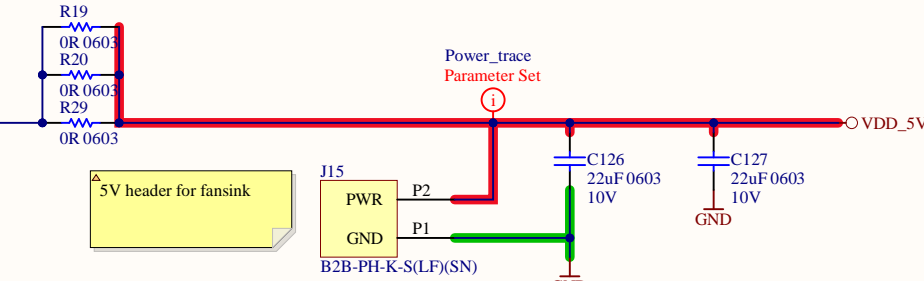




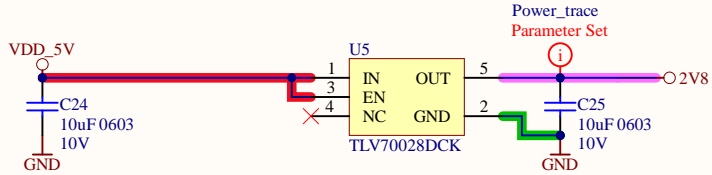
Mark "PWR" on PCB



1ms slew meets the 50mV/us max slew requirement for the IMX378. This also provides ratiometric start-up, which meets the CM3 power on sequence requirement to avoid latch-up.



Loading: OV9282 - 52mA max, each.

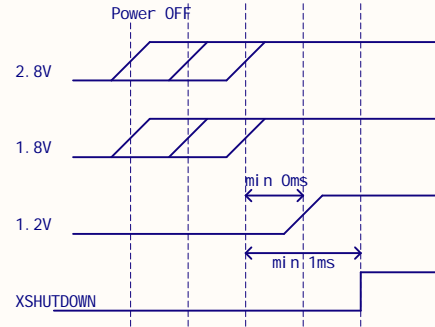


Loading: OV9282 - 24mA max, each  
IMX378 - 55mA max  
CM\_VDAC - 25mA, if active for A/V output

Placed RC timing circuit for EN pins in order to obtain the appropriate power supply sequencing if necessary

## OV9282 POWER REQUIREMENTS

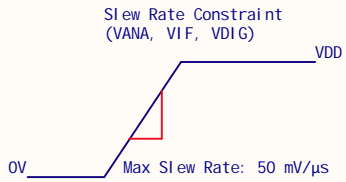
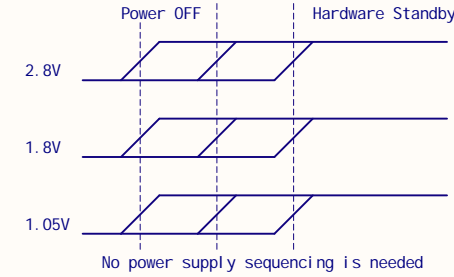
Supply Information			
Supply Name	Sensor	Voltage	Max Current
DOVDD	VDD-I/O	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA



1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

## IMX378 POWER REQUIREMENTS

Supply Information		
Supply Name	Sensor	Voltage
AVDD	VANA	2.8V ± 0.1
DOVDD	VIF	1.8V ± 0.1
DVDD	VDIG	1.05V ± 0.1



### POWER SEQUENCING REQUIREMENTS:

The CM3 requests a power sequence such that, "supplies should be staggered so that the highest voltage comes up first, then the remaining voltages in descending order. this is to avoid forward biasing internal (on-chip) diodes between supplies, and causing latch-up. Alternatively supplies can be synchronised to come up at exactly the same time as long as at no point a lower voltages supply rail exceeds a higher voltage supply rail."

The BW1099 module handles it's own power sequencing on-board.

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.

Effective capacitance targets for each rail, taking into account DC bias and other effects:  
3.3V C<sub>eff</sub> = 24uF  
1.8V C<sub>eff</sub> = 26uF  
1.05V C<sub>eff</sub> = 70uF

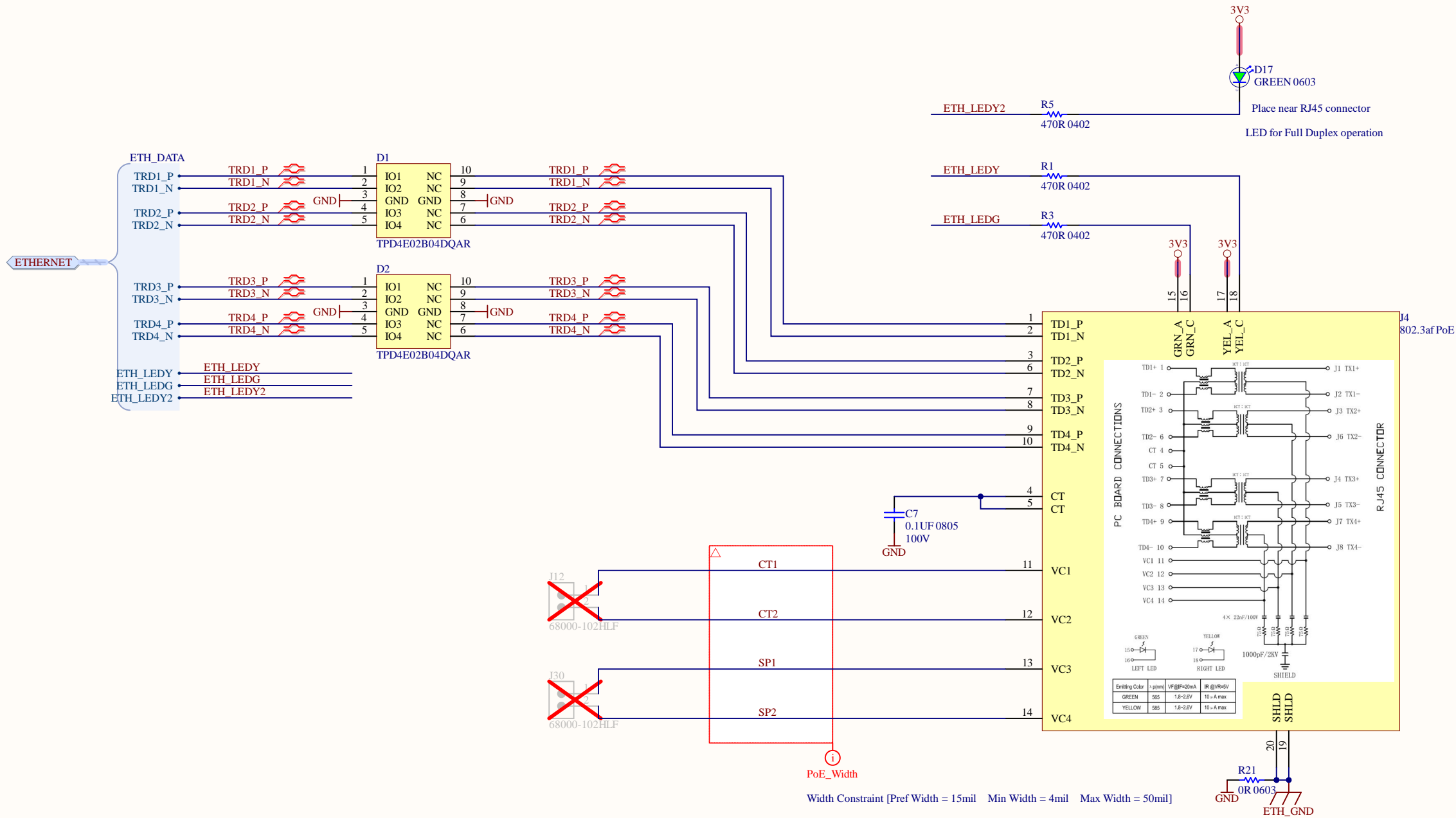
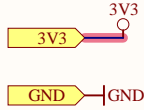
Voltage ripple and allowed voltage tolerance on all rails is +/-5%

Load step design assumptions, based on worst case rail loading:  
3.3V - 2.5A step  
1.8V - 1A step  
1.05 - 0.5A step

SET POINT EQN FOR ALL REG OUTPUTS:  
 $R2 = R1 \times (0.6V / (Vout - 0.6V))$

Compensation adjusted to set Fc 1/10th Fsw (200kHz) for all three outputs. The compensation circuitry has not been fully tuned.

Title <b>DM1097</b>			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States	
Size: Tabloid	Number: D0000200	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\Documents\dm1097.dwg	
Date: 26/02/2021	Time: 07:26:24	Sheet 7 of 17		
Drawn by: David Malovrh				

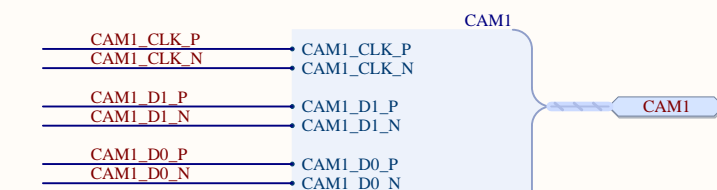
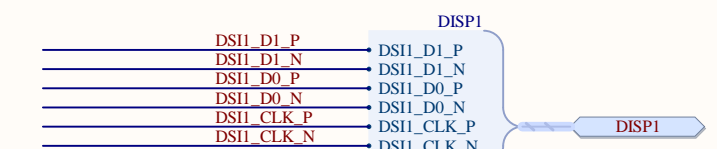
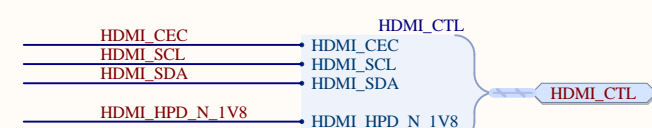
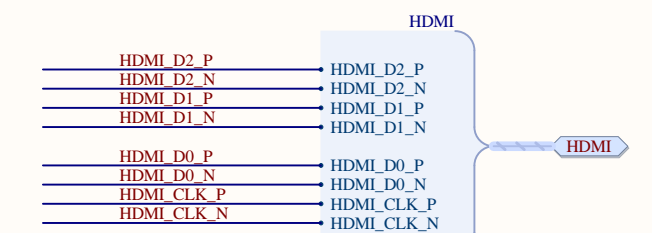
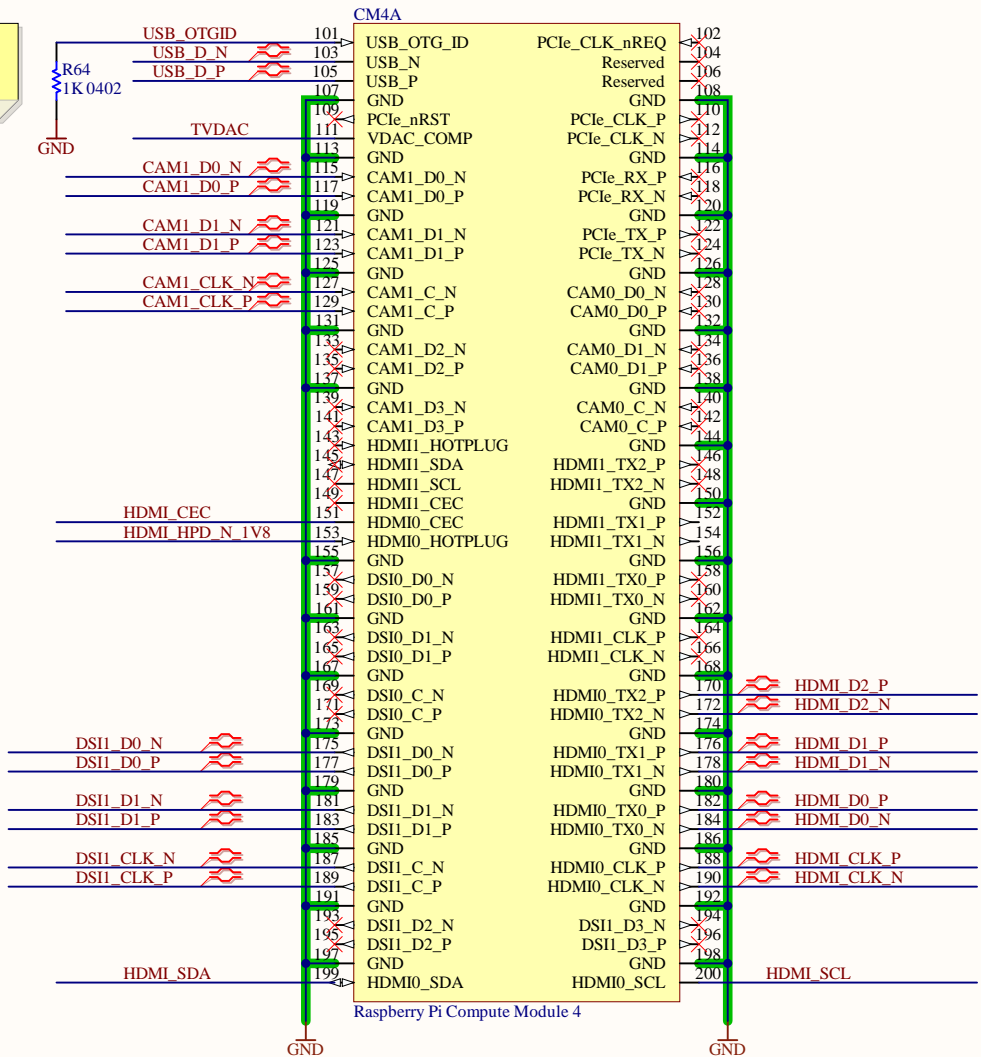


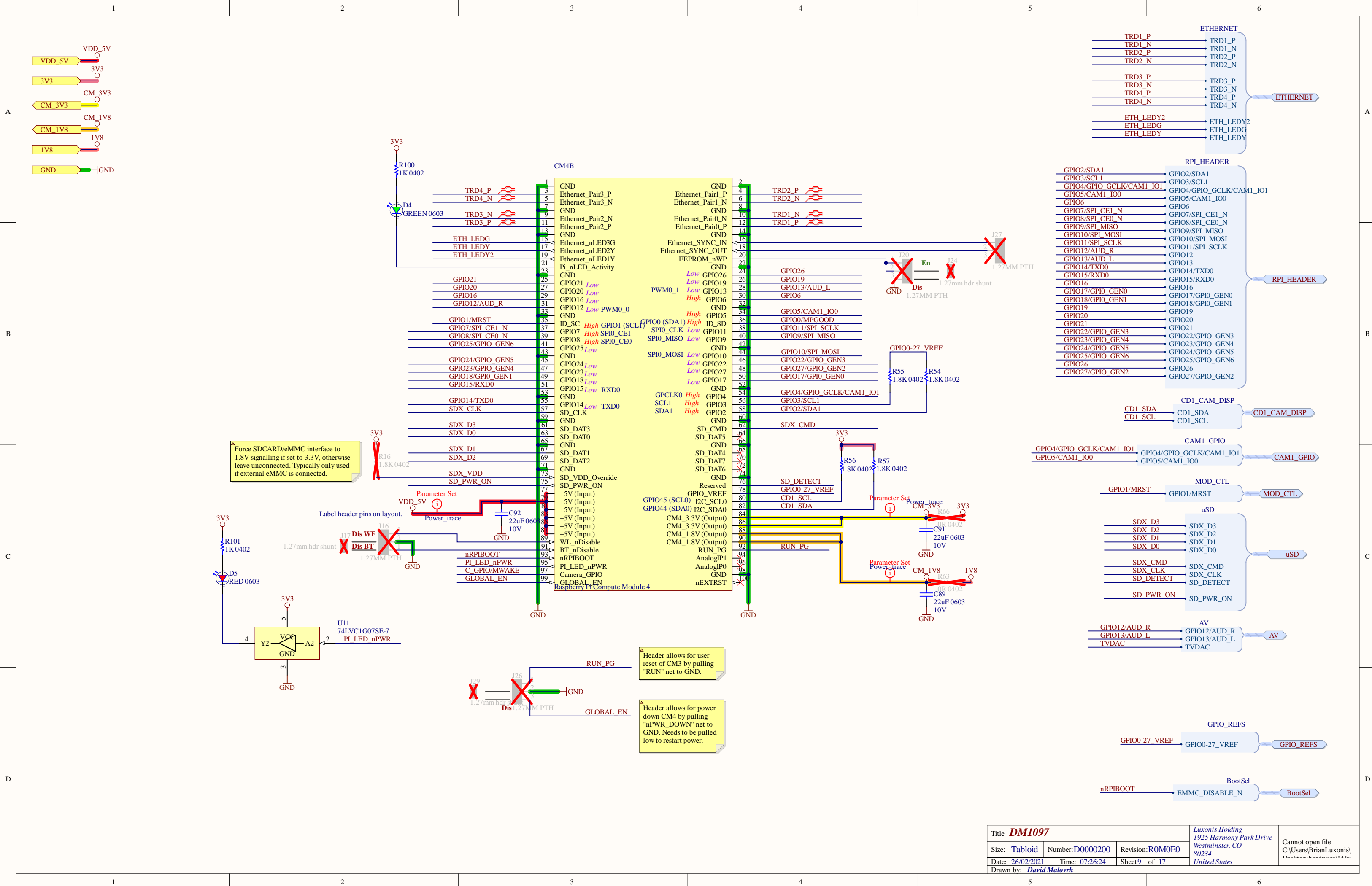


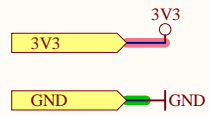


GND

USB\_D diff pair: 90ohms +/-10%  
All other diff pairs: 100ohms +/-10

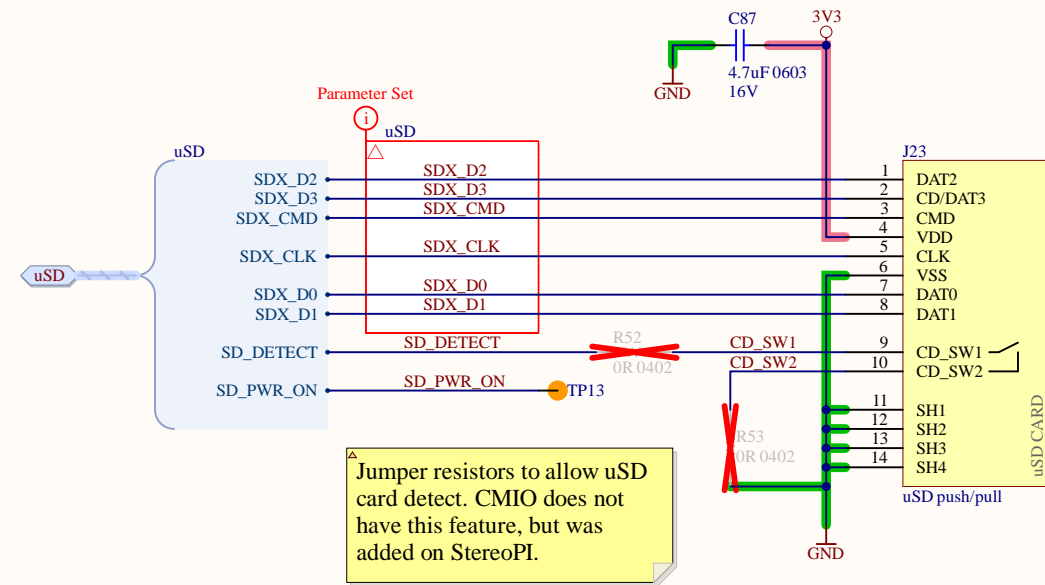




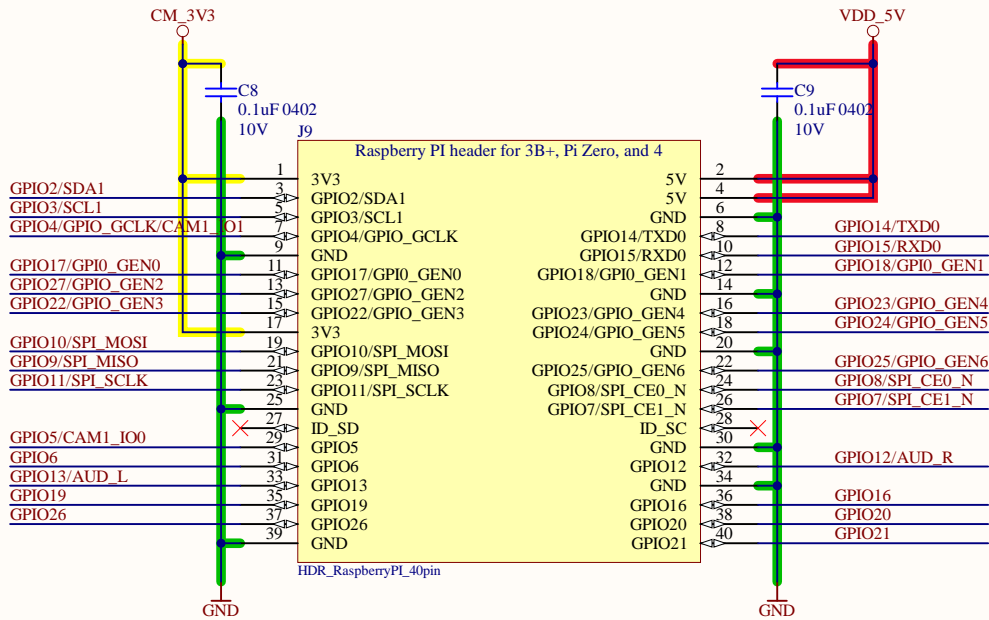
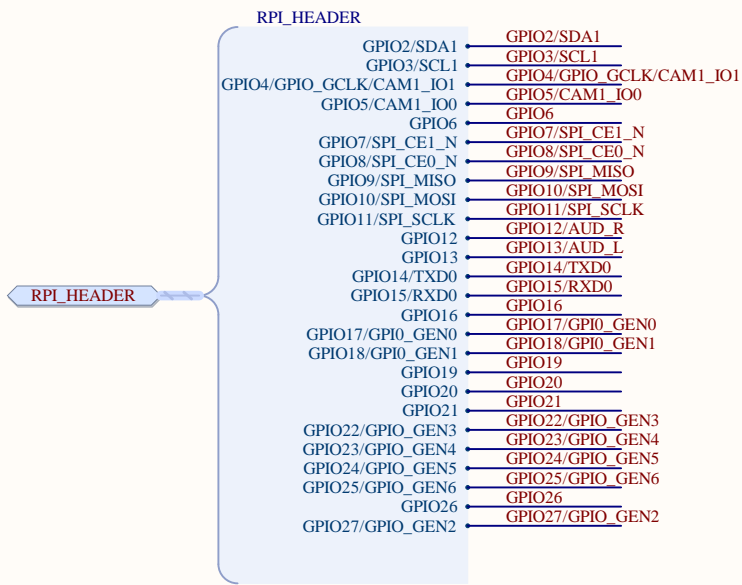
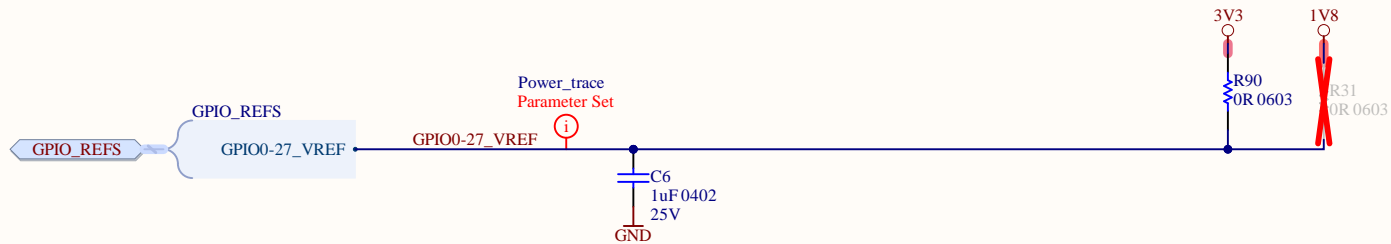
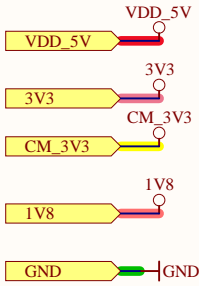


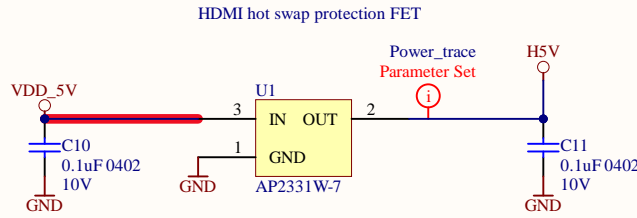
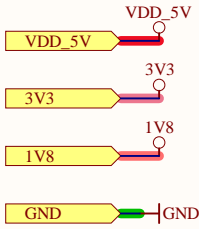
CMIO Note:

uSD is only used for modules with no on-board Flash (eMMC)

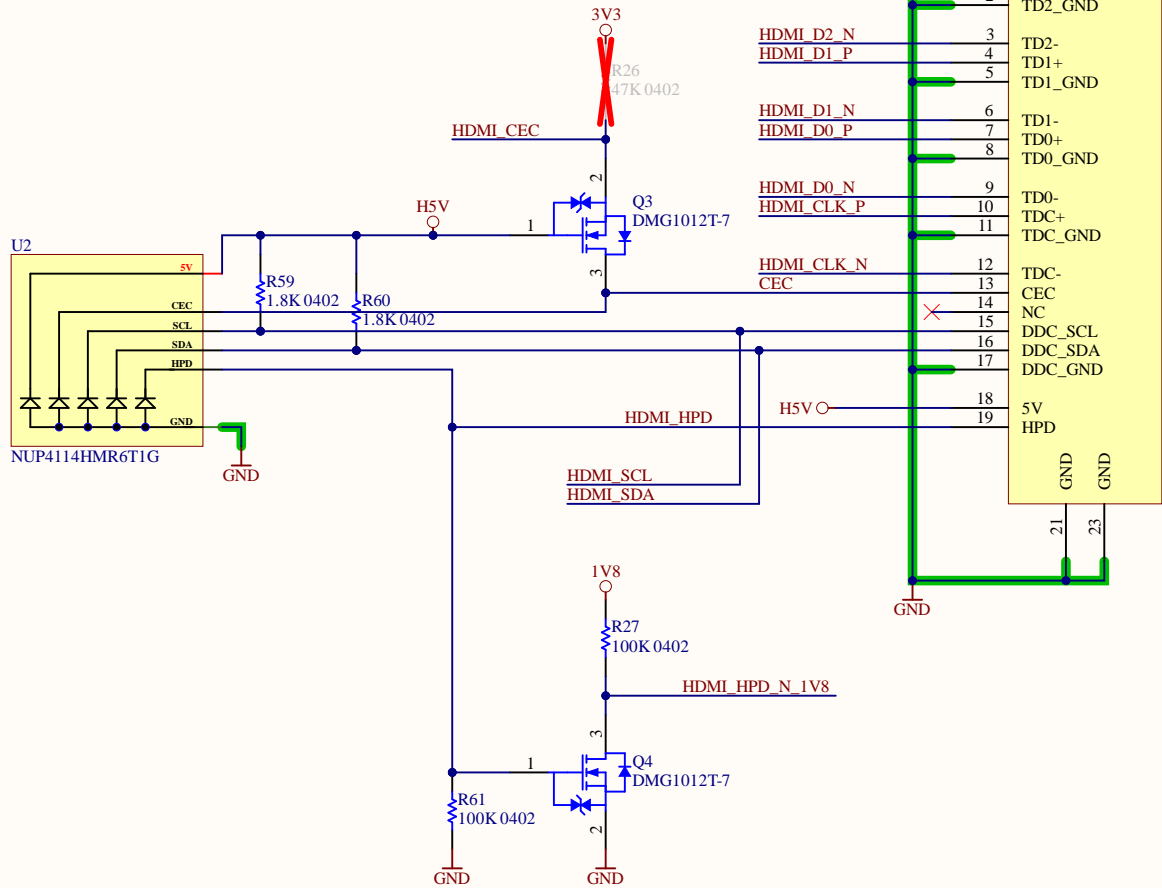
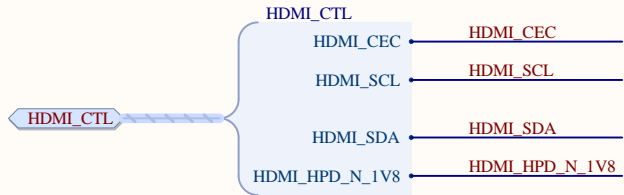
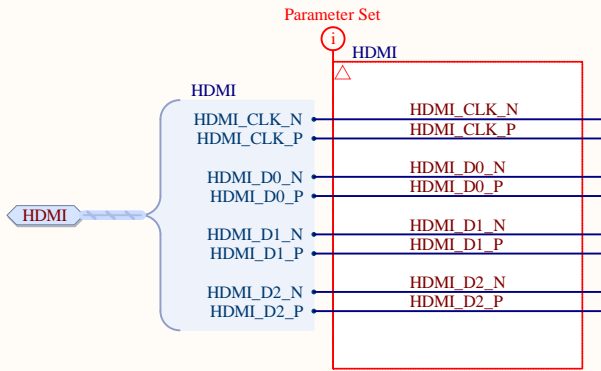


Title <b><i>DM1097</i></b>			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 <i>United States</i>	Cannot open file C:\Users\BrianLuxonis\
Size: <b>Tabloid</b>	Number: <b>D0000200</b>	Revision: <b>R0M0E0</b>		
Date: <b>26/02/2021</b>	Time: <b>07:26:24</b>	Sheet <b>10</b> of <b>17</b>		
Drawn by: <b><i>David Malovrh</i></b>				

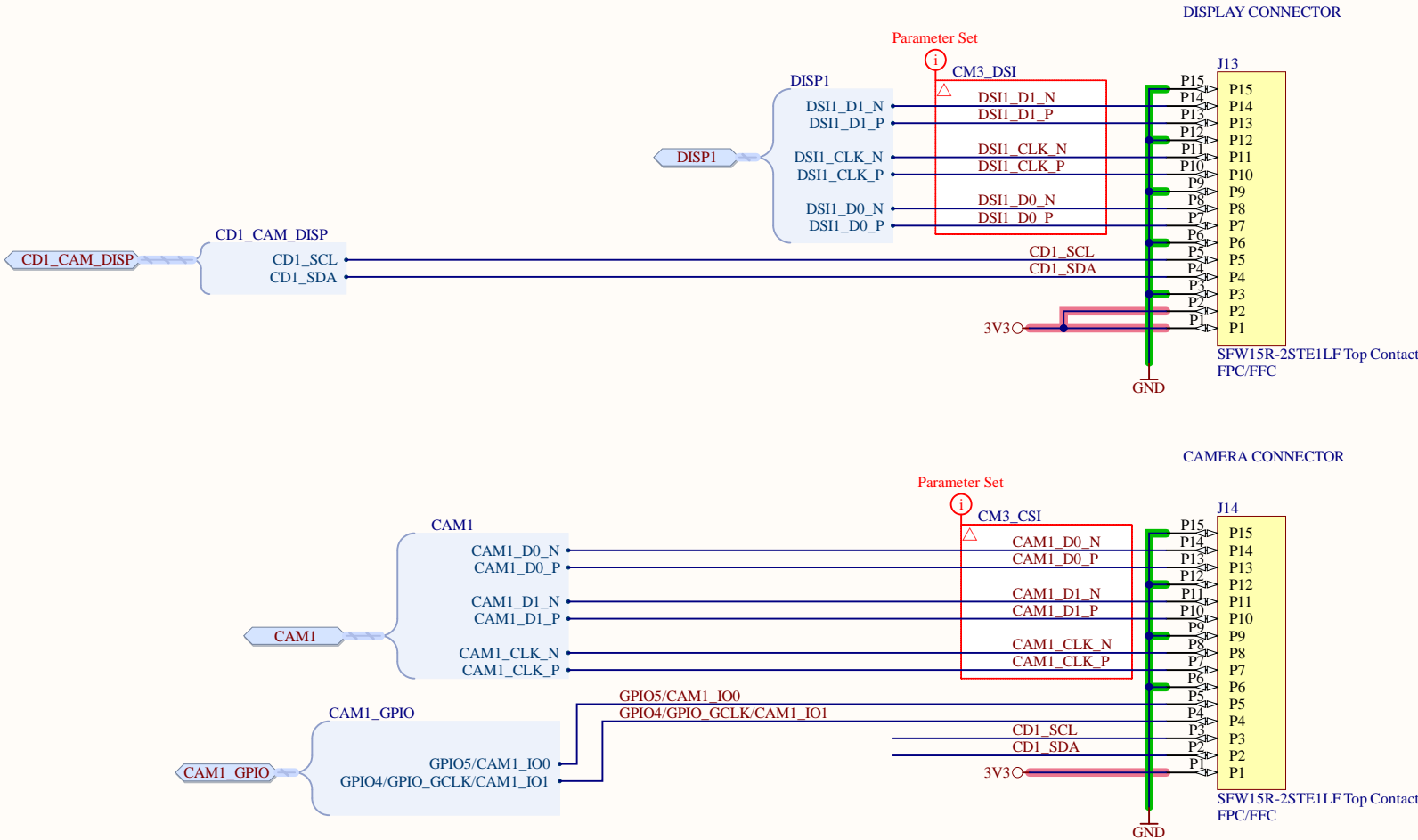
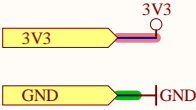




Basic onboard ESD protection is provided for the I2C EDID signals and the CEC signals, internal pullup and down resistors are also provided. On the {rpi4} the HDMI signals don't have any extra ESD protection, depending on the application extra ESD protection maybe required.







CMIO/CM3 guide for attaching display + camera  
(<https://www.raspberrypi.org/documentation/hardware/computemodule/cmio-display.md>) uses:

GPIO0 - CD1\_SDA  
GPIO1 - CD1\_SCL  
GPIO4 - CAM1\_IO1  
GPIO5 - CAM1\_IO0

.dts file provided on that guide for this configuration.

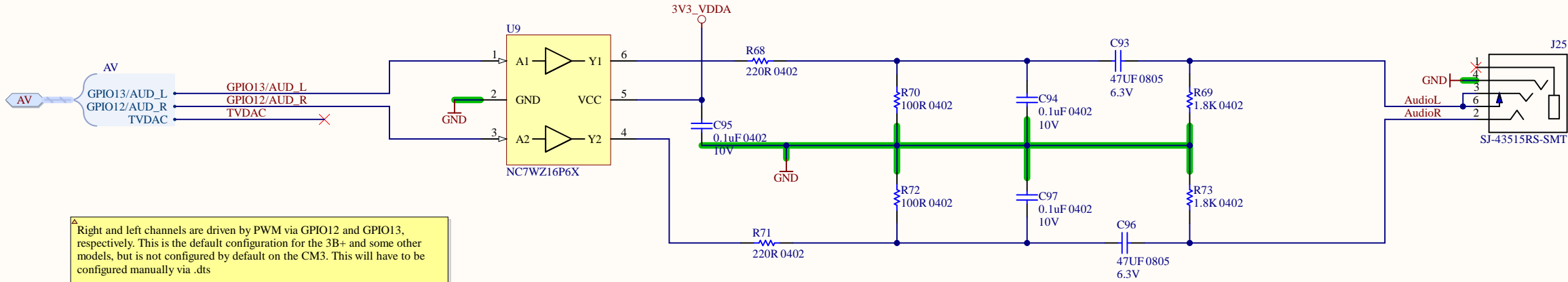
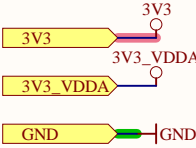
NOTES:  
(1) GPIO4/GPIO\_GCLK and GPIO5 are also broken out to the standard 40-pin, 3B+-style header on this board.  
(2) CAM1 and DISP1 are both 4-lane MIPI busses, but the 15-pin connectors only support 2-lane.

The PiCam V2.1 uses only the camera connector Pin 11 (CAM1\_IO0) as an Enable pin, so this pin needs to be pulled high by default to enable camera usage, regardless of what GPIO it is connected to.

Both GPIO4 and GPIO5 are weakly pulled up by default in the BCM (see pg. 102 <https://www.raspberrypi.org/app/uploads/2012/02/BCM2835-ARM-Peripherals.pdf>)

FFC uses top-contact, so pin numbers are flipped relative to net names. This maintains correct connections when flex cable is inserted in top-contact position.





Right and left channels are driven by PWM via GPIO12 and GPIO13, respectively. This is the default configuration for the 3B+ and some other models, but is not configured by default on the CM3. This will have to be configured manually via .dts

TVDAC requires a 75ohm route, and is susceptible to coupled noise. (Not used in this design)