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Sec - 04

Lab Experiment 02

18101530_circuit1 - Proteus 8 Professional - Schematic Capture

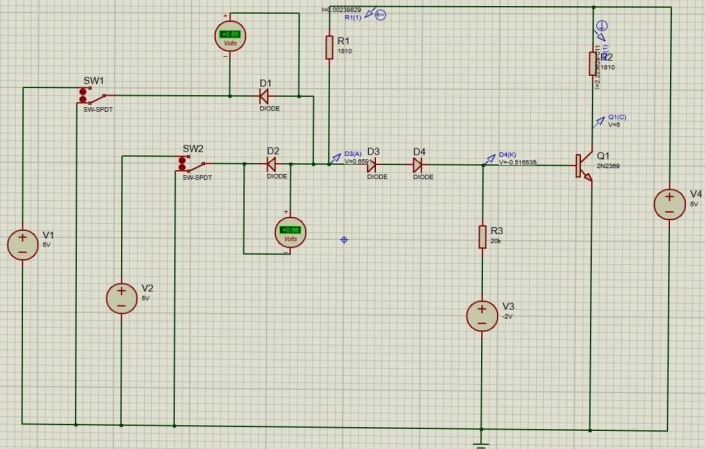
File Edit View Tool Design Graph Debug Library Template System Help

Base Design

Schematic Capture

P L DEVICES

2N2369
DIODE
RES
SW-SPDT
VSOURCE



2 Message(s)

ANIMATING: 00:57:54.700000 (CPU load 4%)

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18101530_circuit2 - Proteus 8 Professional - Schematic Capture

File Edit View Tool Design Graph Debug Library Template System Help

Base Design

Schematic Capture

P L DEVICES

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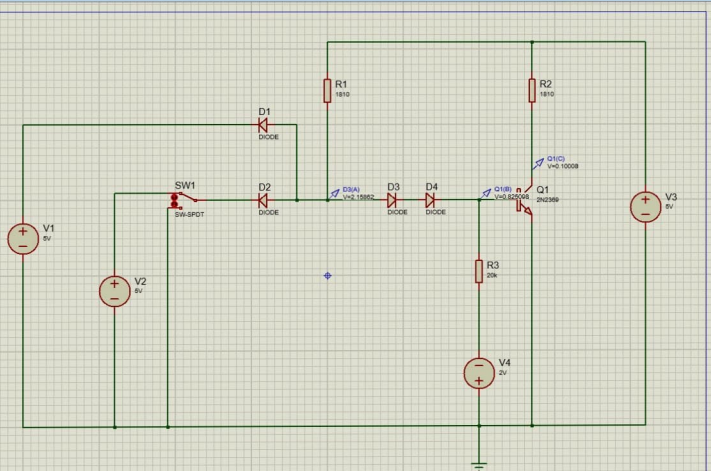
DIODE
RES
SW-SPDT
VSOURCE



2 Message(s)

ANIMATING: 00:41:07.300000 (CPU load 7%)

-6800.0

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Table 1:

Input A	Input B	V_{DA}	V_{DB}	V_p	I_R	I_{R_2}	V_b	Output y
0	0	0.66	0.66	0.6591	0.00233 98	2.22 e^{-11}	-0.516	5
0	1	0.68	-4.32	0.677	0.00233 88	2.22 e^{-11}	-0.499	5
1	0	-4.32	0.68	0.67	0.00233 88	2.22 e^{-11}	-0499	5
1	1	-2.84	-2.84	2.15	0.00156	0.00270714	0.825	0.10008

Table 2:

Input A	Input B	V_p	V_b	Output y
1	0	0.677	-0.499	5
1	1	2.158	0.825	0.10008

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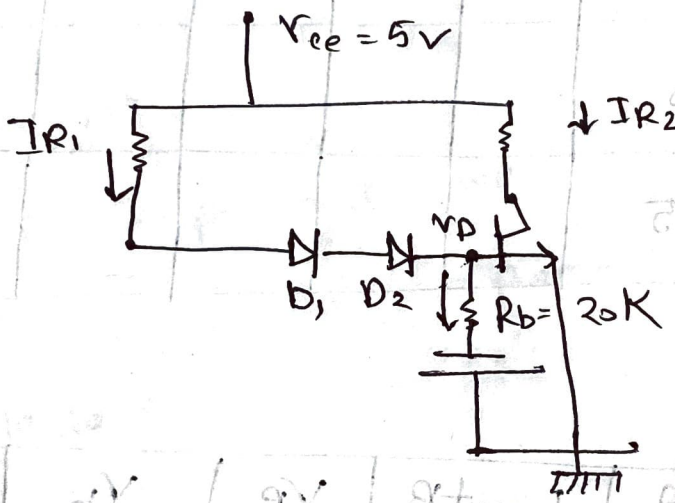
Report:

1. If we assume that logic is high that applied to both inputs of the circuit then partial circuit which remain active is drawn below-



2. Table 2 is work as Inverter.

By fixing V_A as High, I can change the value of V_B to High and Low.

If, V_B = High = 5V, then output = 0.1000 gr = Low

If, V_B = Low, or, then output = 5 V = High

So, NAND gate is work as Not gate

3. The brief explanation of the NAND operation:

In the NAND gate, if we input high voltage in every input the output will be low. Here the diodes will be turned off and the transistors will get turned on and for this reason the output will tend to be zero or low.

Then, on the other hand, when we will put all the inputs are low or a particular input is low, then the transistor will be in cut off mode and the output will be high which is 5V. The reason is that the transistor will be turned off and this will make the input high.

4. By using the proteus data, I can find that if the one of the pin inputs is High = 5V and other is Low = 0V, then the operation mode of Q1 is in cut off. That means the transistor is off in this situation.

5. By using simulation Data, I find that, the maximum value of inputs A and B to keep the Output High is 1.1

V_A	V_B	Output
5	0.8	5 V
5	0.9	4.99V
5	1.1	4.942V
5	1.2	2.87V