Palash Ranjan Roy

ID - 18101530

Sec - 04

Lab Experiment 03

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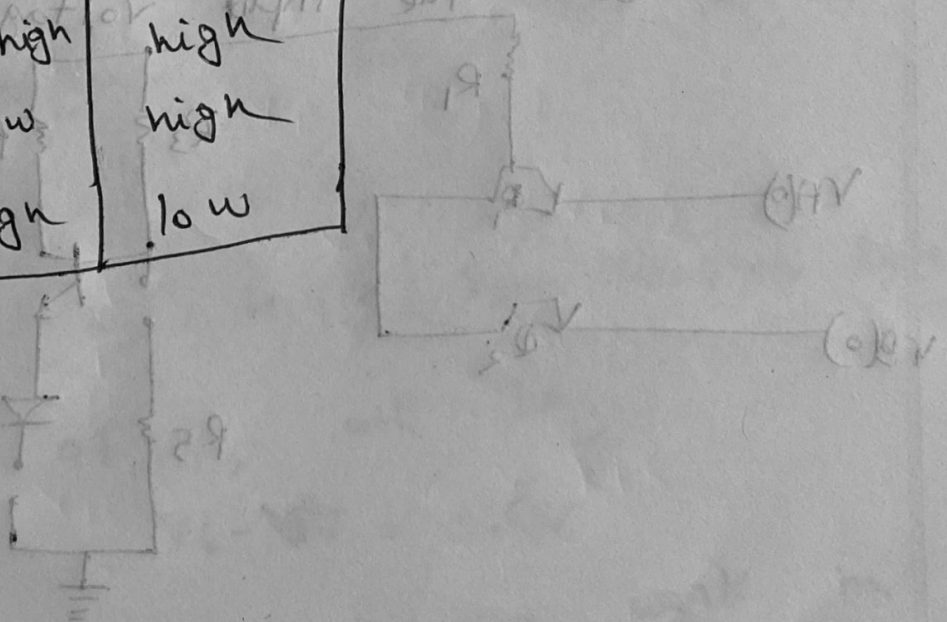
Table 1:

Input A	Input B	Input VA(V)	Input VB(V)	V_0	V_1	V_2	V_3	V_4	V_5	V_6
0	0	0	0	4.613	0.717	0.0076	1.057 e-8	5	4.80314	5
0	1	0	5	4.613	0.755	0.049	1.068 e-8	5	4.80314	5
1	0	5	0	4.613	0.755	0.0494	1.066 e-8	5	4.803	5
1	1	5	5	0.0097	2.676	1.968	1.0625	1.154	0.582	4.99

Report: 1. NAND GATE: Truth table

x	y	Output
low	low	high
low	high	high
high	low	high
high	high	low



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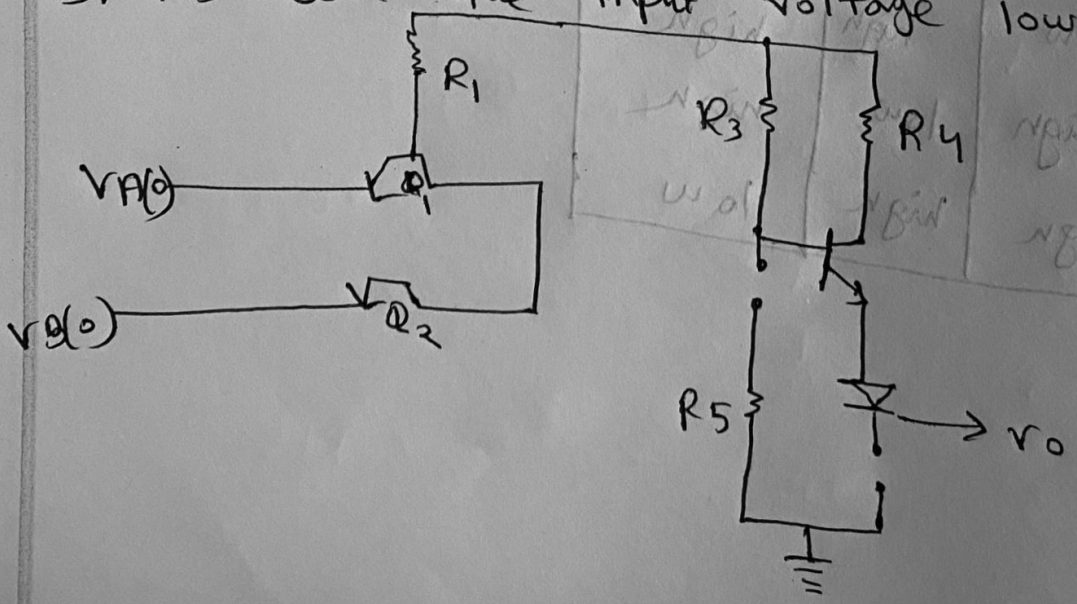
The table from the circuit:

Input A	Input B	output, v_o
0	0	4.613
0	5	4.613
5	0	4.613
5	5	0.009

It can be said that the circuit is working like a NAND gate.

2. When we use two transistors following a push-pull ~~cong~~ configuration we call that totem-pole stage

3. As both the input voltage low,



4. Here, T_3 is acting as a switch and belongs to the splitter phase. It helps to turn ON and OFF T_4 and T_5. If one of them is ON, the other will be off.

5. If diode D_1 is absent in the circuit, the V_{cc} will be divided among T_3, T_4 and R_4. As a result, it may cause indefined logic state for output section with reduced noise margin.

6. Here, T_5 "Transistor" will be work in forward Active ~~mode~~ node when at least one input is low.

Test: $V_{CE} \geq 0.2$

$V_6 = 5\,V$, $V_5 = 4.8\,V$ (From Previous Data)

So, V_{CE} of T_5 will be,

$V_6 - V_5 = 0.2V$

So, "T_5" Transistor will be work in forward Active node.

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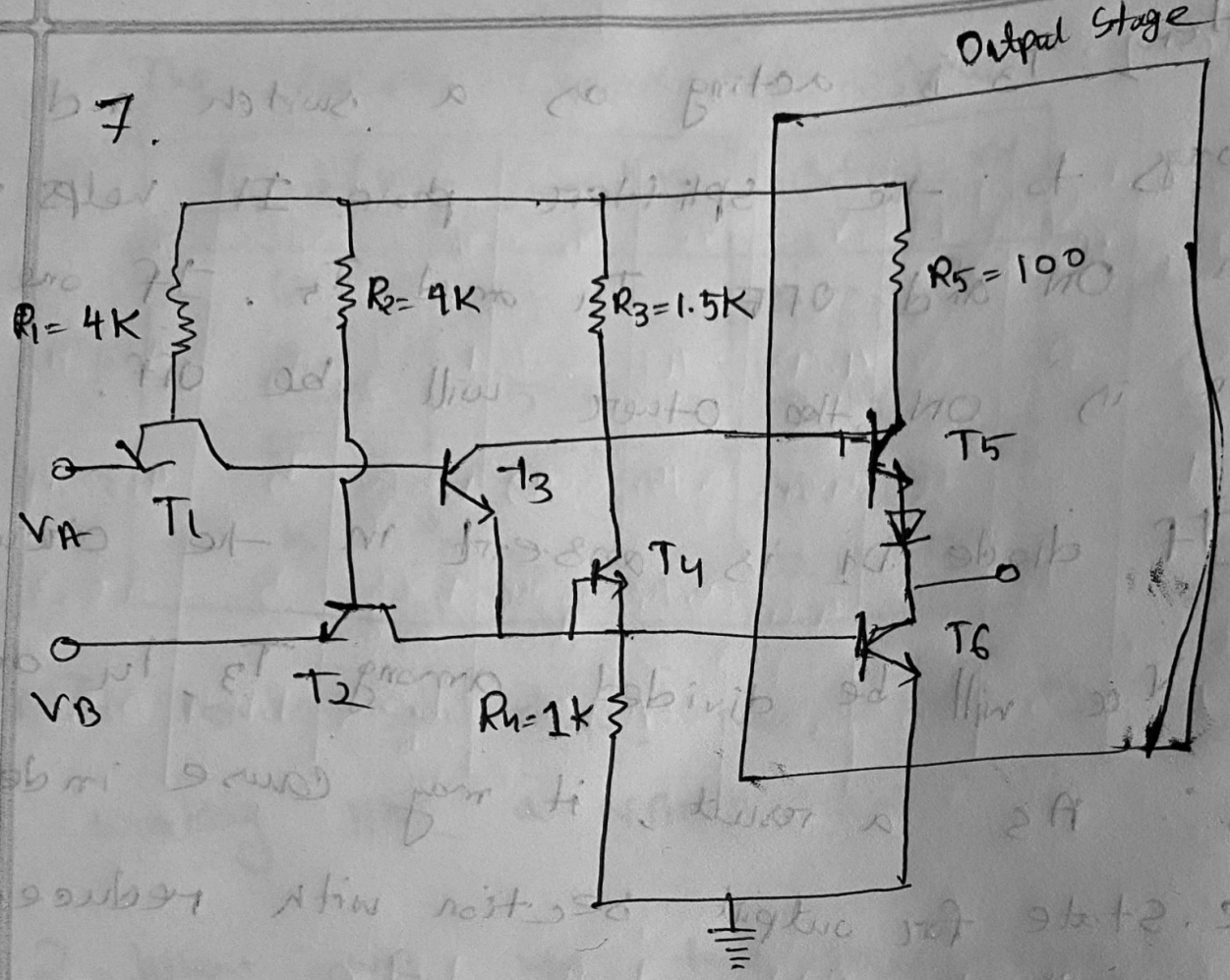
7.



This is the TTL "NOR" gate circuit with totem pole output stage