ANALOGUE DEVICES AND THEIR CHARACTERISTICS, SPECIFICATIONS AND APPLICATIONS

1. INTRODUCTION TO OPERATIONAL AMPLIFIERS

With the advances in electronics and integrated circuits (ICs), the requirement to implement designs from discrete components has given way to easier and more reliable methods of signal conditioning. Many special circuits and general purpose amplifiers are now contained in IC packages producing a quick solution to signal conditioning problems together with small size, low power consumption and low cost.

In general, the application of ICs requires familiarity with an available line of such device, their specifications and limitations before they can be applied to a specific problem. Apart from these specialized ICs, the Operational Amplifier (Op Amp.) finds wide application as the building block of signal conditioning applications.

The op-amp is a direct coupled high-gain amplifier to which feedback is added to control its overall response characteristics. It is used to perform a wide variety of linear functions (and also some nonlinear operations) and is often referred to as the basic linear (or more accurately, analog) IC.

There are two types of linear ICs, namely, monolithic-and hybrid-ICs. Monolithic ICs are manufactured along with some resistors and capacitors. Hybrid ICs are those achieved by connection of discrete component, passive elements, and monolithic ICs.

Integrated op-amp is being widely used because if offers all the advantages of monolithic ICs, namely, small size, high reliability, reduced cost, temperature tracting and low offset voltage and current.

1.2 Birth And Growth of the IC Op.Amp

Fairchild brought out the 702, 709, and 741 IC Op.amps between 1964 and 1968, while National semiconductor introduced the 101/301. These IC op-amps revolutionized certain areas of electronics because of their small size and low cost, and even more importantly, reduced drastically the task of circuit design. With advances in semiconductor fabrication technology, major improvements were made in op-amps. First, field-effect transistors were substituted for certain BJTs within the op-amp. JFETs, at the op amp's input draw very small currents and allow the input voltages to be varied between the power supply limits. MOS transistors in the output circuitry allow the output terminal to go within millivolts of the power supply limits. The second major improvement was the introduction of dual and quad op.amp packages. In the same 14-pin package occupied by a single op-amp, designers fabricated four separate op-amps. All four Op. Amps in the package share the same power supply. The LM 324 is popular example of the quad Op. Amp and the LM 358 is a popular dual op-amp.

Inevitably, general purpose op-amps were redesigned to optimize or add certain features. Special function ICs that contain more than a single op-amp were then developed to perform complex functions. General purpose op-amps will be around for quite some time, however, more complex ICs will be developed on a single chip that combine many op-amps with digital circuitry. With improved very large scale integrated (VLSI) technology, it is inevitable that entire systems will be fabricated on a single large chip. A single chip computer is today's really, a single-chip TV set will happen eventually. Before learning how to use op-amps, we will first learn how they look like and how to buy them. The op. amps' greatest use will be as a part in a system that interfaces the real world of analog voltage with the digital world of the computer.

1.3 Schematic-Symbol-Package

In the schematic internal circuitry of a 741 op-amp, there are about 17 BJTs, 12 resistors, one capacitor and 4 diodes 9 BJTs connected as diodes). It is not necessary to learn about the internal workings of this complex circuit. The circuit symbol is as shown in figure 3.1. The basic part of the symbol is a triangle that signified amplification, pointing in the direction of signal flow. There are five basic terminals, as shown in Figure 3.1: two for power supply, two for input signals, and one for the output.

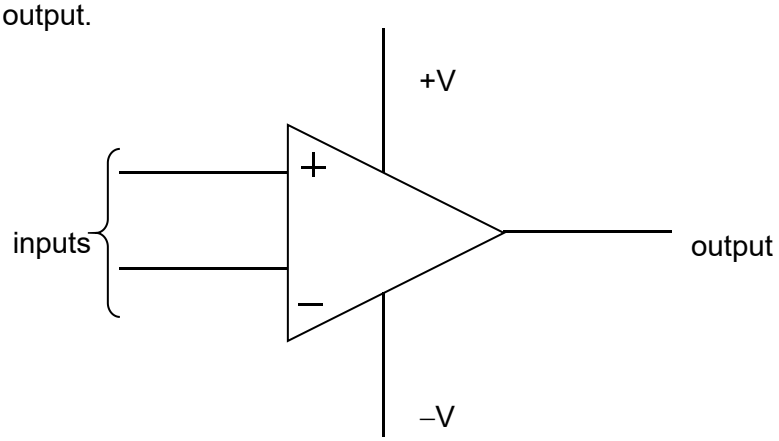


Fig 3.1: Basic Circuit Symbol of an Op-amp.

The two most common types of op amps packages encountered are the round metal can (TO-) and dual-in-line (DIP). The TO-style metal package can have 8. 10, or 12 leads. DIP packages have, 8, 14,16,18,20,24,28, 40 and even 64 terminals. Usually, an 8-pin DIP for single op-amps, and a 14 pin DIP for dual and quad op. Amp packages, are encountered. The most common types of packages that house an op-amp are shown in figure 3.2. From figures 3.2 (a) and (b), the numbering schemes are identical for 8-pin can and 8-pin DIP. A notch or dot identifies pin 1 on the Dips, and a tab identifies pin 8 on the TO-package. From a top view, the pin count proceeds counter clockwise. Thus, it could be said that manufacturers are now combining the circuit symbol for an op-amp together with the package view into a single drawing.

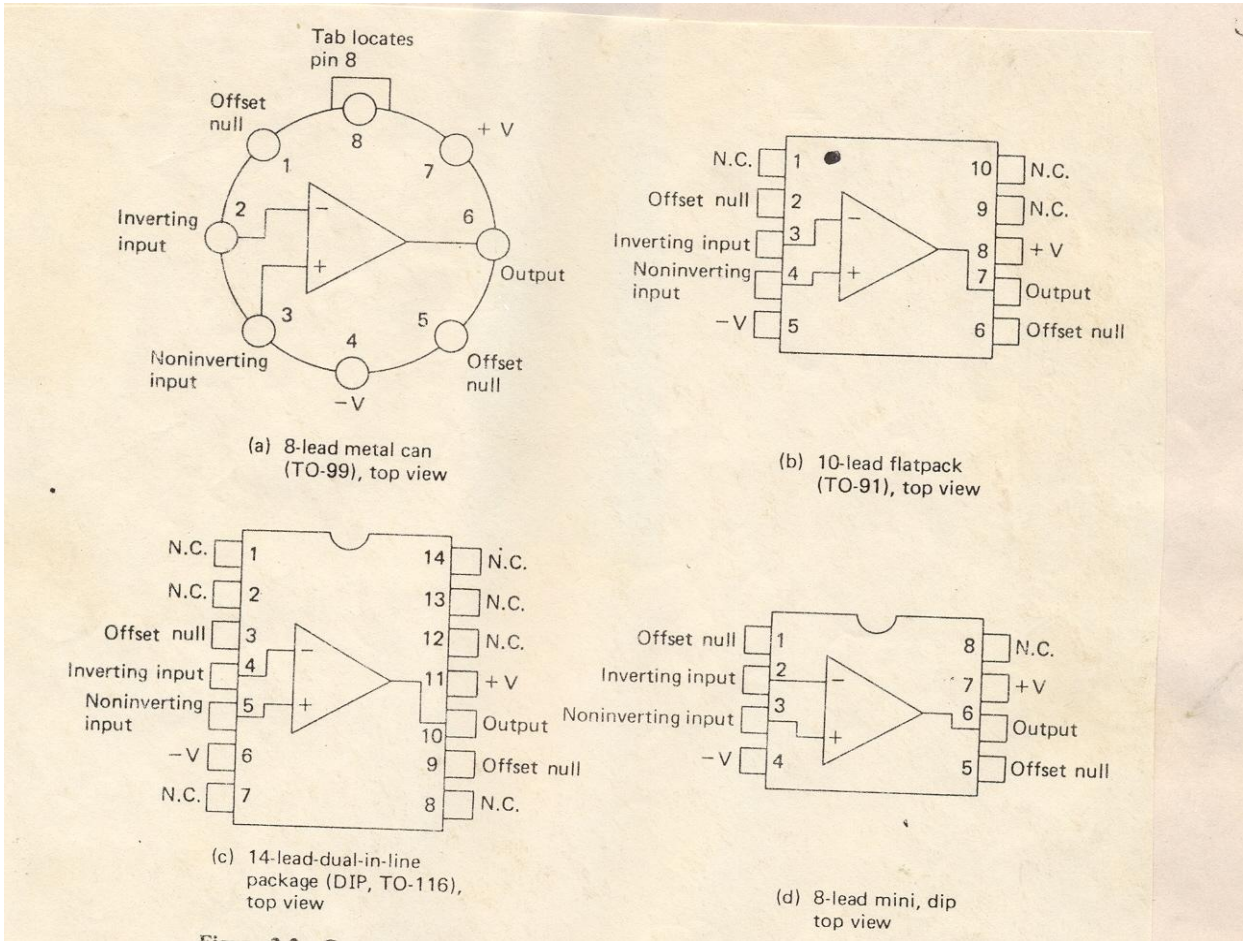


Fig. 3.2: Op Amp Packages

To wire an op. amp into a circuit, first, dimensions of the package must be known (usually for printed circuit board, PCB layout), and these are found in the data section called “Mechanical Data’, Physical Dimension”, or “Dimensional outlines”, depending on the manufacturer’s choice. Secondly, the package “pinout” (how to count the pins, and the function of each pin) must be known. This information is usually given on the data sheet and is usually titled “Functional Diagram” or “Connection Diagram”.

1.4 How To Identify or Order An Op. Amp

1.4.1 The Identification Code

Each type of op amp has a letter-number identification code, that answers four questions:

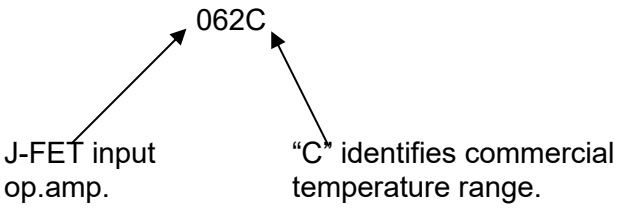
1. What type of op. amp is it? (Example: 741)
2. Who made it? (Example: Analog Devices)
3. How good is it? (Example: the guaranteed temperature range of operation).
4. What kind of package houses the op. amp chip? (Example: plastic DIP).

Not all manufacturers use precisely the same code. But most use an identification code that consists of four parts written in the following order: (1) letter prefix, (2) circuit designator, (3) letter prefix, and (4) military specification code.

Letter Prefix: It usually consists of two or three letters that identify the manufacturer, listed as in the following examples.

Letter Prefix	Manufacturer
AD	Analog Devices
CA	RCA
LM	National Semiconductor Corp.
MC	Motorola
NE/SE	Signetics
OP	Precision Monolithics
RC/RM	Raytheon
SG	Silicon General
TI	Texas Instruments
µA	Fairchild

Circuit Designation: It consists of three to seven numbers and letters, identifying the type of op. amp and its temperature range. For example:



The temperature-range codes are:

C Commercial, 0 to 70°C
I: Industrial, - 25 to 85°C
M: Military, - 55 to 125°C

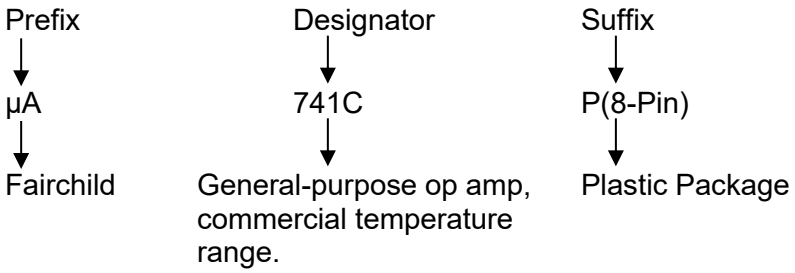
Letter suffix: A one-or two-letter suffix identifies the package style that houses the op. amp chip. Three of the most common package suffix codes are:

Package Code	Description
D	Plastic dual-in-line for surface mounting on a PC board
J	Ceramic dual-in-line
N.P	Plastic dual-in-line for insertion into sockets. Leads extend through the top surface of a PC board and are soldered to the bottom surface.

Military Specification Code: This code is used only when the part is for high-reliability application.

1.4.2 Order Number Example:

A 741 general – purpose op. amp. Would be completely identified as follows:



1.5 Breadboarding: Of Op. Amp. Circuits.

The requirements for breadboarding are:

(i) to set up a circuit in a minimum amount of time.

(ii) Change external elements easily for any design modification

(iii) Replace the IC without having to unsolder it (i.e. use an IC socket).

(iv) Connect leads from audio oscillators, function generators, volunters, and oscilloscopes

(v) Have a + ve and –ve power supply.

There are different types of IC breadboard, and the one used is mainly a matter of availability.

After having designed and analyzed a circuit with an IC, and the components obtained, the next stage is the building (fixing of components) of the circuit, and finally testing the design.

Note that all grounded leads should be connected to a common ground

Testing an IC Circuit

Before testing, the connections have to be checked and then proceed as follows:

(i) Connect the ±V or 2V (V = 6,9,12,15,18) to the ± or + and ground terminals respectively.

(ii) With a CRO, or with a dc voltmeter, check to be sure that the appropriate voltages are being supplied to the right terminals.

(iii) Connect the input signal and measure it.

(iv) Measure the output voltage to be sure the output is neither in saturation nor slew rate limited.

(v) All measurements should be taken with respect to ground

(vi) Unless otherwise instructed, avoid using ammeters.

(vii) There is an minimum value of 2kΩ placed on load resistors

(viii) Disconnect the input signal before the dc power is removed, otherwise, the IC may be destroyed.

(ix) (a) Never reverse polarity of the power supplies

(b) Never drive the op amp's input pins above or below the potentials at the + V and – V terminal.

(c) Never leave an output signal connected with no power on the IC

(x) If unwanted oscillations appear at the output and the circuit connections seem correct

(a) Connect a 0. 1μF capacitor between the op amp's +V pin and ground, and another 0.1μF capacitor between the op-amp's –V pin and ground.

(b) Shorten your leads and

(c) Check the test instrument, signal generator, load, and power supply ground leads. They should be connected to a common ground.

2. OP. AMP CHARACTERISTICS AND SPECIFICATIONS

Although many type of Op. amps with diverse specifications exist from many manufacturers, they all have common characteristics of operation that can be employed in basic designs relating to any general op. amp.

2.1 Op. Amp Terminals

2.1.1 Power Supply Terminals

The power supply terminals are labelled +V and –V. The power supply usually has three terminals: Positive, Negative, and Common ground.

The power supply could either be a bipolar or split supply with typical values of ±15V, ±12V and ±6V, or non-symmetrical supplies (as required in special-purpose op amps) such as ±12V and –6V or even a single polarity supply such as ±30V and ground. A load resistor, RL has to be connected to provide a path for currents returning to the supply from the op amp.

The maximum supply voltage that can be applied between +V and –V is typically 36V or ±18V.

2.1.2 Output Terminal:

The output terminal is connected to one side of the load resistor R_L. Since there is only one output terminal in an op amp. It is called a single ended output. There is a limit to the current that can be drawn from the out put terminal of an op amp. Usually on the order of 5 to 10mA. There are also limits on the output terminal's voltage levels, with an uper limit of V_o =+ V_{sat} (positive saturation voltage) and the lower limit is caled the negative saturation voltage, -$V_{sat.}$ Typically, V_{sat} = V_{supply} -2, and V_o is restricted to a peak-to-peak swing of ±$V_{sat.}$ some op. amps such as the 741 have internal circuitry that automatically limits current drawn from the output terminal. Even with a short circuit for R_L output current is limited to about 25mA.

2.1.3 Input Terminals

The two input terminals, -&+(Fig. 3.1) are called differential input terminals because output voltage, V_o, depends on the difference in voltage between them, V_d, and the gain of the amplifier, A_{OL}.

2.2 Ideal Op Amp:

The ideal op amp has the following characteristics:

Input impedance $R_I = \infty$, Output impedance $R_o = 0$, Open-loop Voltage gain, $A_{OL} = -\infty$, Band width = ∞, output voltage is zero for zero differential input voltage (V_d), Characteristics do not drift with temperature.

In a practical op. amp. $A_v \neq \infty$ but is extremely large, often 2 x 10^5 or more, $R_i \neq \infty$ and $R_o \neq 0$, Bandwidth $\neq \infty$ and there is an internal drift in the op amp as a result of which $V_o \neq$ o when $V_d = 0$.

Since V_o oscillates between $\pm V_{sat}$ (such that for a ± 15V supply $-13V < V_o < 13V$). Thus V_d is limited to a maximum voltage of ±65 μV. This value is difficult to measure because the voltage of noise generated by the mains frequency and that of leakage currents on the typical test set-up, could be around 1m V. Thus if V_d is small that is not measurable, then for all practical purposes V_d = 0V.

2.3 Op. Amp. Specification

Design applications are always directed toward the ideal properties, but these properties are never realized in practice, or course, but the assumption of such ideal allow rapid preliminary analysis of feedback circuits involving these amplifiers. Although these characteristics are extreme specifications, commercially available units approach the ideal so closely that many practical circuits can be designed on the basis of these characteristics.

Thus, there are characteristics of op. amps other than the ideal that enter into design applications. These characteristics, together with the open loop gain input and output. Impedance's are given in the specifications for particular op. amp. Several of these specifications are in relation to do and ac performances.

2.3.1 DC Performance: Bias, Offsets and Drift

2.3.1.1 Input Bias Currents

Transistors within the op amp must be biased correctly (correct values of 1_{b2} 1_c & V_{ce}) before any signal voltage is applied. In an ideal op amp. It is assumed that the input terminals conduct no current. In practice, however, the input terminals do conduct a small value of dc current to bias the op amps transistor. A simplified diagram of an op amp is shown in Figure 3.3a, with an accompanied model for bias currents shown in Figure 3.3 (b).

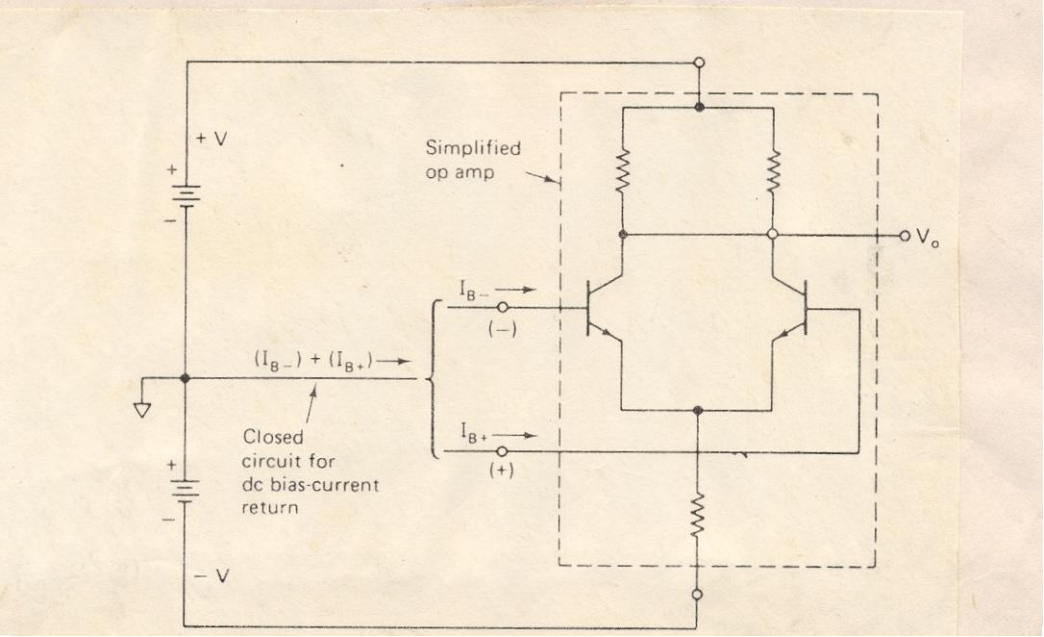


Fig. 3.3a: Typical Schematic representations for supplying power to an op amp.

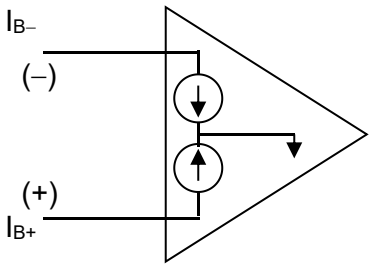


Fig. 3.3b: Model for bias currents

I_{B-} is usually not equal to I_{B+}. Manufacturers specify an average (I_B) of the magnitude of both input bias current.

$$I_B = \frac{|I_{B+}| + |I_{B-}|}{2}$$

I_B is in the range of 1μA or more for general-purpose op amps, and around 1pA or less for op amp with FETs at the input.

2.3.1.3 Input Offset Current

I_{os} is given by, $I_{OS} = |I_{B+}| - |I_{B-}|$

Values of 1_{os} specified by manufacturers are for circuits' condition where the output is at 0V and the temp is 25°C. Typical values of I_{os} is less than 25% of I_B. I_{os} is a net current required between the inputs of zero the output voltage.

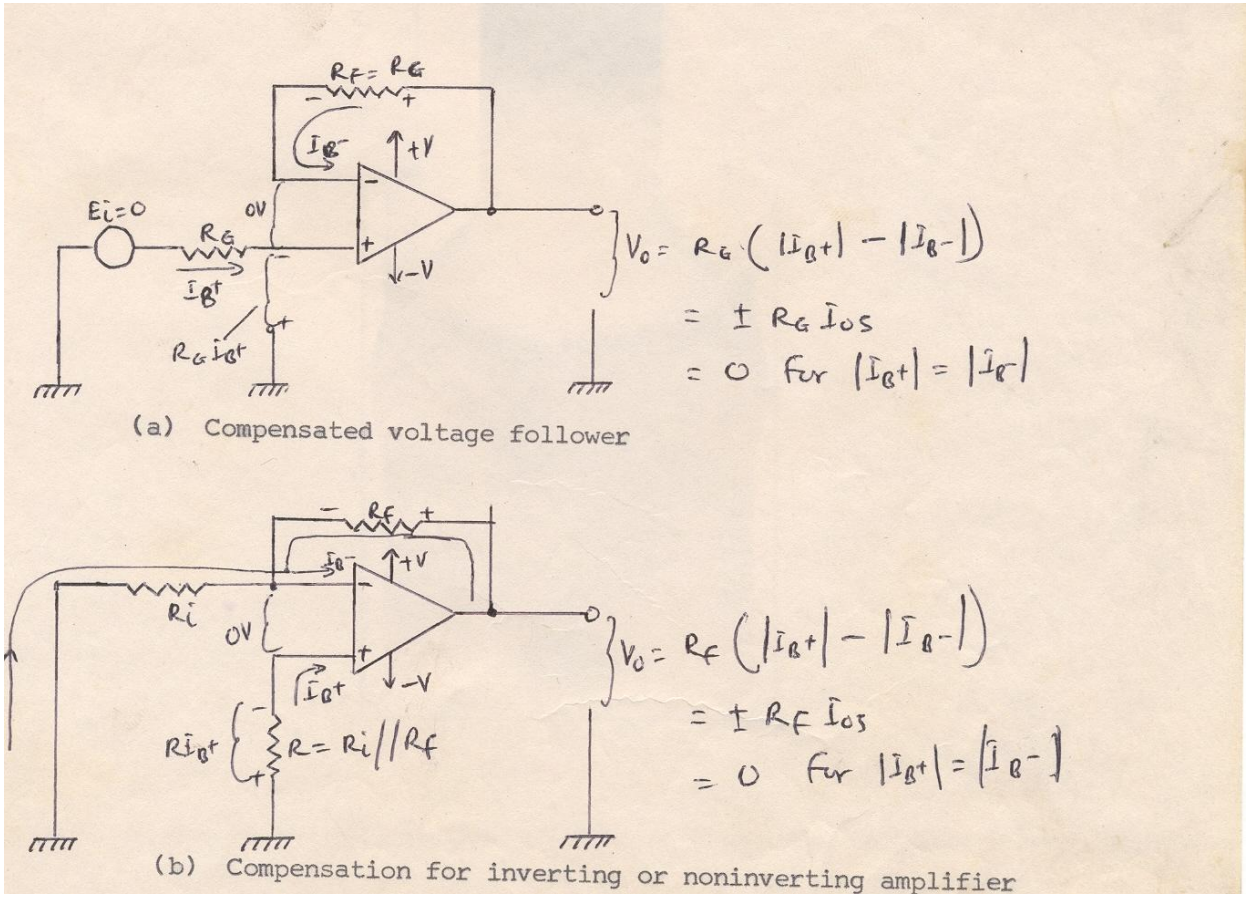


Fig. 3.4: Balancing out effects of bias current in V_o

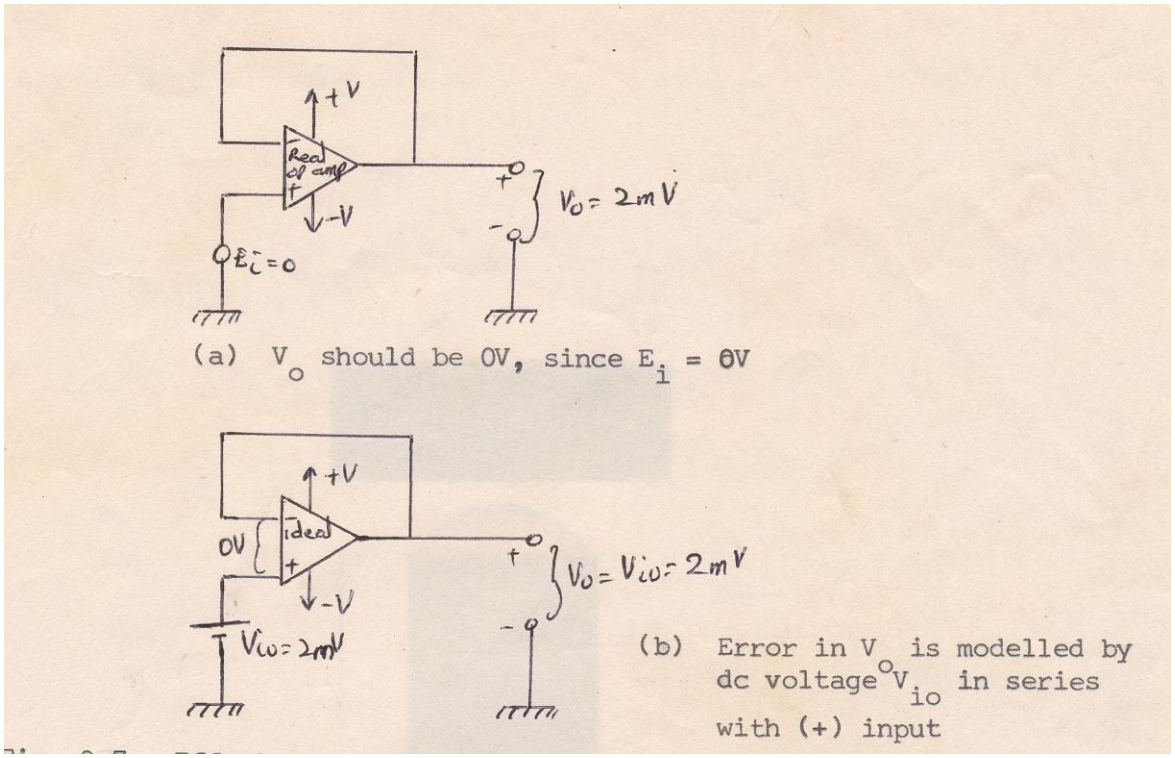


Figure 3.5: Effect of input offset voltage in the real op. am of (a) is modeled by an ideal op. am plus battery V_{io} in (b).

In Figure 3.4 (a), if $I_{B+} = I_{B=,}$ then $V_o = 0$ when $E_i = 0$. But seldom do $I_{B+} = I_B$. By making $R_f = R_G$, error in V_o is reduced.

In Figure 3.4 (b), with no input signal, V_o depends on R_f times I_{os}. Resistor R is called the current-compensating resistor and is equal to the parallel combination of R_I and R_f. This is included in the act to minimise errors in V_o due to I_B & $I_{B+.}$ Note: Always add a bias-current compensating resistor R in series with the (+) input terminal (except for FET input op. amps). The value of R should equal the parallel combination of all resistance branches connected to the (-) terminal. In circuits where more than a single resistor is connected to the (+) input to ground should equal the dc resistance seen from the (-) input to ground.

In applying this principle, signal sources are replaced by their internal dc resistance and the op amp output terminal is considered to be at ground potential.

2.3.1.3 Input Offset Voltage

In the Circuit of Fig, 3.5 (a) $V_o \neq 0$ but ranges between μVs to mVs. This small error-voltage component, is caused by very small but unavoidable unbalances inside the op.amp. A model of the net offset is shown in Fig. 3.5 (b). This dc voltage is called input offset voltage $V_{io,}$ and is shown to be a series with the (+) input terminal of the op. amp. It makes no difference whether V_{io} is modeled in series with the (-) input or the (+) input.

Thus the voltage that must be applied across the input terminals to drive the output to zero is the input offset voltage, $V_{io.}$ The magnitude and polarity of V_{io} varies from op. amp. to op. amp.

A fairly complex resistor – divider network that would inject a small variable voltage into the (+) or (-) input terminal, could be constructed – to compensate for the effects of both V_{io} and $I_{os.}$ But this would be more costly and bulky than necessary. Therefore, it is for better to go to op. amp. Will have a V_{io} circuit recommended by the manufacturer. Some typical output-voltage null circuit are shown in Figure 3.6.

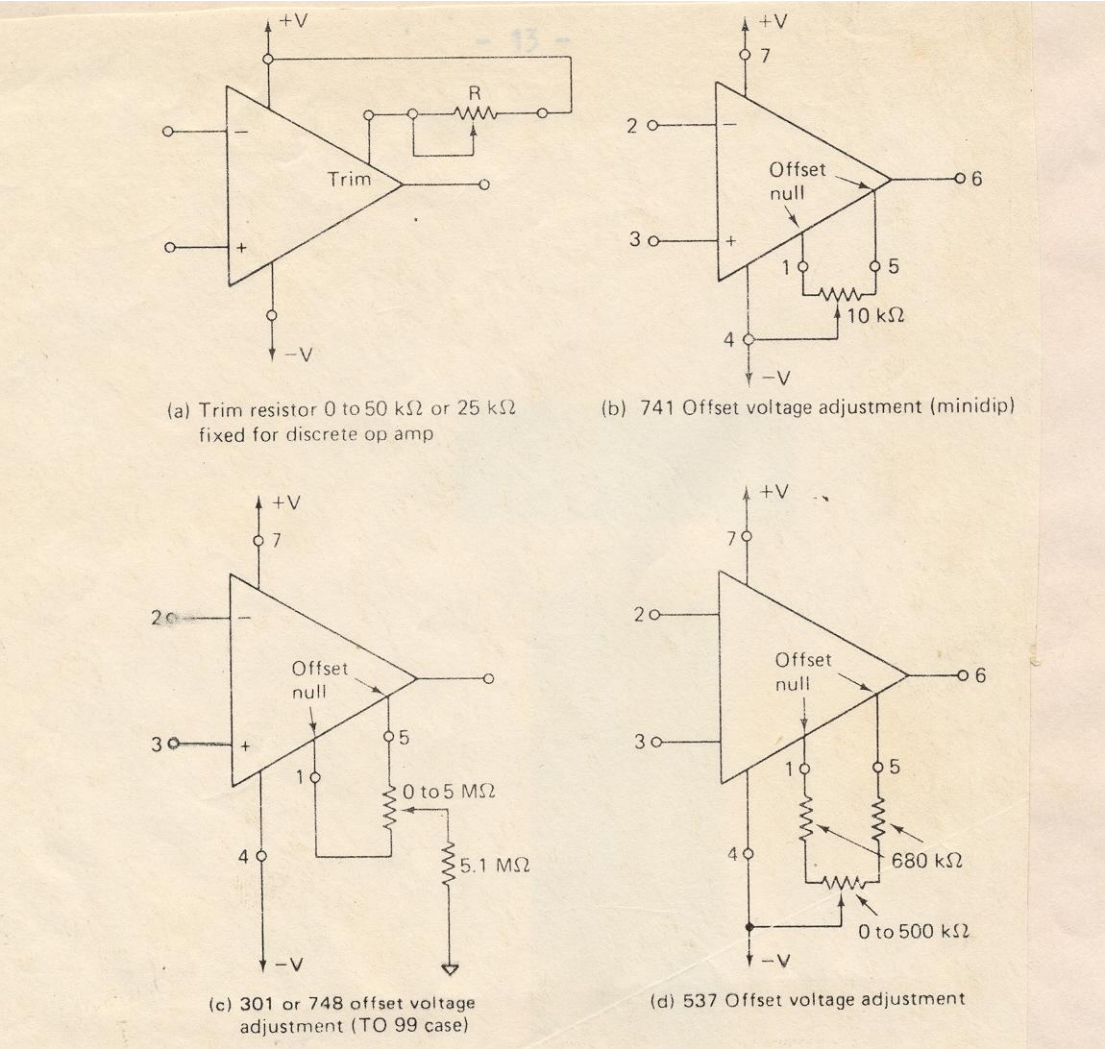


Fig. 3.6: Typical Circuits to minimize error in output voltage due to input offset voltage & offset current.

2.3.1.4 Nulling Procedure For Output Voltage

1. Build the circuit & include (a) the CCR
   (b) Voltage offset null circuit
2. Reduce all generator signals to O. If their output cannot be set to O, replace them with resistors equal to their internal resistance.
3. Connect the loan to the output terminal
4. Turn on the power & wait a few minutes for things to settle down
5. Connect a dc voltmeter or a CRO (dc coupled) across the load to measure V_o.
6. Vary the offset voltage adjustment resistor until V_o reads Ov. Note that output voltage errors due to both V_{io} & I_{os} are now minimized.
7. Install the signal sources and do not touch the offset – voltage adjustment resistor again.

2.3.1.5 Drift

The zeroing procedure of section 2.3.1.4 holds at one temperature and at a given time. I_{os} and V_{io} change with time because of aging of component. Also, if the supply voltage changes, bias

current and consequently the offset current, will change. Changes in supply voltage can be eliminated by use of a well-regulated power supply. However, the offset changes with temp. can only be minimized by:

(1) holding the temp. surrounding the circuit constant

(2) selecting op amps with offset current & offset voltage rating that change very little with temperature changes.

Changes in offset current and offset voltage due to temperature are described by the term drift, and are specified in mA/^{o}C and ^{o}C respectively. Drift an average or maximum drift between two temperature limits.

2.3.2 AC Performance: Band-Width, Slew Rate, Noise & Frequency Compensation

In the application of op. amp in ac. Circuits, output signals less than IV peak are considered as being small and the op. amp performance is affected by noise and frequency response. For large ac output signals (greater than IV peak), the op. amp characteristic known as slew rate limiting determines whether the output signal will be distorted or not.

2.3.2.1 Frequency Response of the Op. Amp.

(a) Internal Frequency Compensation

Many op. amps (whether general or special purpose) have internal compensation, through the installation of a small capacitor, usually 30pF. This prevents the op.amp from oscillating at high frequencies. Oscillations are prevented by decreasing the op.amp's gain as frequency increases. It is known that

$X_C = 1/(2 \pi fC)$, i.e. $X_C \propto 1/f$

Therefore, for increasing f, X_C decreases, thus the voltage gain decreases. A curve of how the open-loop gain of the op. amp is related to the frequency of the differential input signal is always given by manufacturers in the data sheet. This curve is called the open-loop voltage gain versus frequency, or the small-signal response.

(b) Frequency Response Curve

This is shown in Figure 3.7, for internally compensated op. amps such as the 741 and 747. At frequencies below 1Hz, the gain is very high (typically$\geq$200,000 $\equiv$ 106dB).

Point A is called the –3dB point, and the frequency at this point is known as the break frequency. Changing the frequency by a factor of 10 (1 decade) decreases the gain by a factor of 10, or by 20dB. Therefore the frequency response curve of figure 3.7 is said to roll-off at 20dB/decade. Alternative description is xdB/octave roll-off ("octave" signified a frequency change of factor of 2). Therefore each time the frequency doubles, the voltage gain decreases by 6dB.

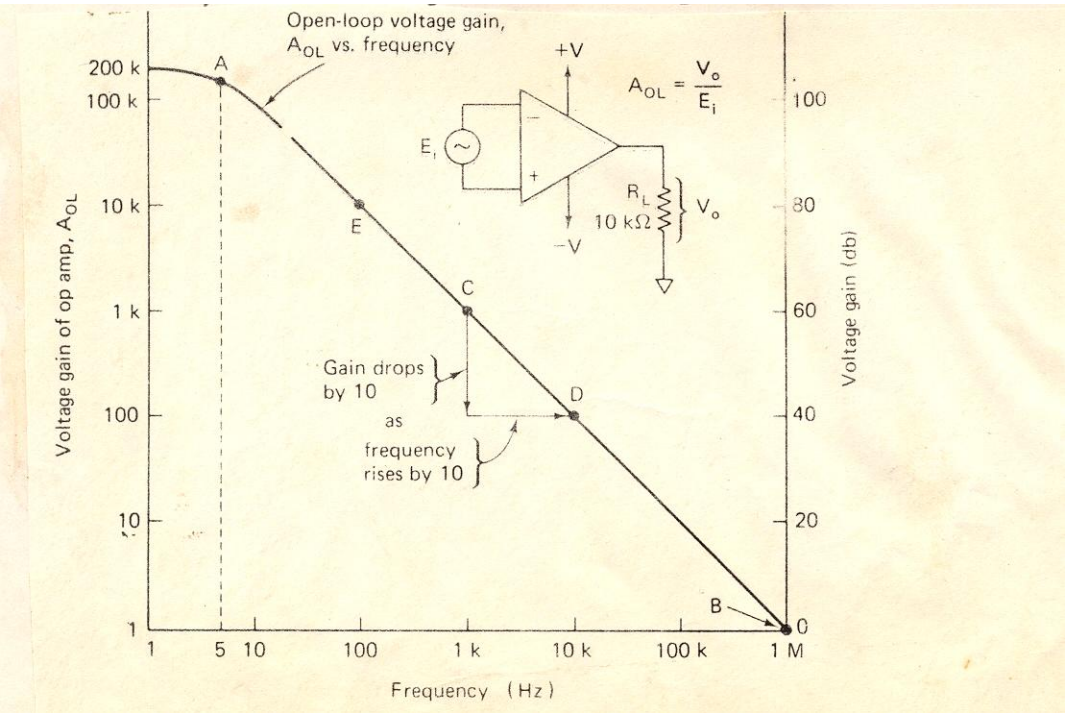


Fig. 3.7: Open-loop voltage gain of a 741 op amp versus frequency

(c) Unity-Gain Band Width

The unity-gain bandwidth corresponds to the frequency at which $A_{OL} = 1$, i.e. point B in Figure 3.7.

In some data sheets, the unity gain bandwidth or the frequency response curve is not given, but the "Transient Response Rise Time (Unit gain)" specification is given. From this quantity, the unity gain bandwidth, B, is calculated from the equation,

$$B = \frac{0.35}{risetime}$$

where B is in Hz and rise time in seconds.

Also, $A_{OL,}$ at a given frequency, F, = (Bandwidth at Unity Gain)/F

2.3.2.2 Amplifier Gain and Frequency Response

(a) Effect of Open-loop Gain On Closed-Loop Gain Of An Amplifier, DC Operation

For both inverting and non-inverting amplifier, the actual dc closed-loop gain is obtained by dividing the ideal A_{CL} by a factor A, given by,

$$A = 1 + \frac{1}{A_{OL}}\left(\frac{R_F + R_i}{R_i}\right)$$

If A_{OL} is large, then A approaches unity, and the amplifier gain will not depend on A_{OL}

(b) Small-Signal Bandwidth, Low-and High-Frequency Limits

A sketch of the general frequency-response curve is as shown in Figure 3.8

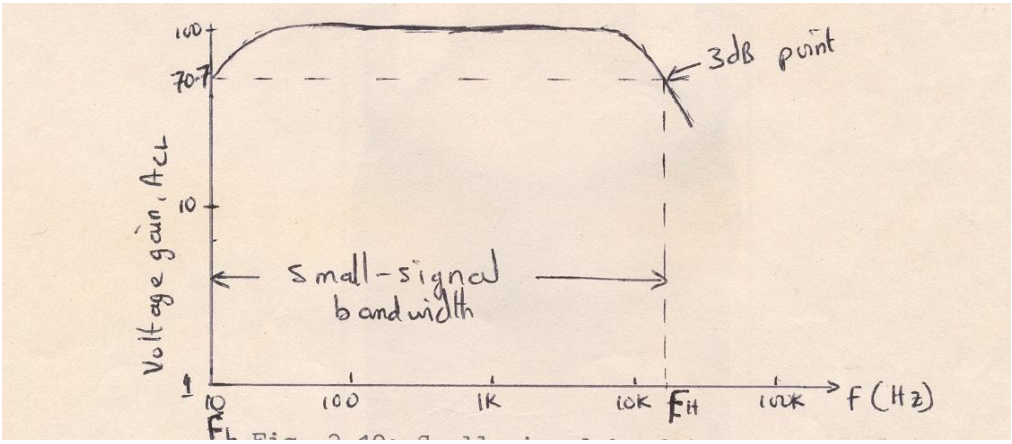


Fig 3.8: small signal bandwidth

The small signal bandwidth, BW = $F_H - F_L$, where F_H and F_L are the high frequency limit and low frequency limit, respectively. At F_H and F_L, the voltage gain is 0.707 of the maximum value in the middle of the useful frequency range.

Often, $F_L << F_H$, or $F_L = 0$ (for dc amplifier), hence BW ≡ F_H

The relationship between BW & B is given by, $BW = \frac{B}{A_{CL}}$

This implies that the gain-bandwidth product is equal to B of the op. amp. There is a direct trade-off, in that bandwidth is sacrificed for more gain and vice-versa.

(c) Finding Bandwidth by a Graphical Method

Given the amplifier gain (say) 1000) at low and mid-frequencies, then the bandwidth (or rather F) is ≡ 1kHz The amplifier gain is approximately 700 at f_H. For all frequencies above f_H, in fig. 3.9, the frequency response of the amplifier and op. amp coincide (i.e. A_{CL} & A_{OL} responses coincide).

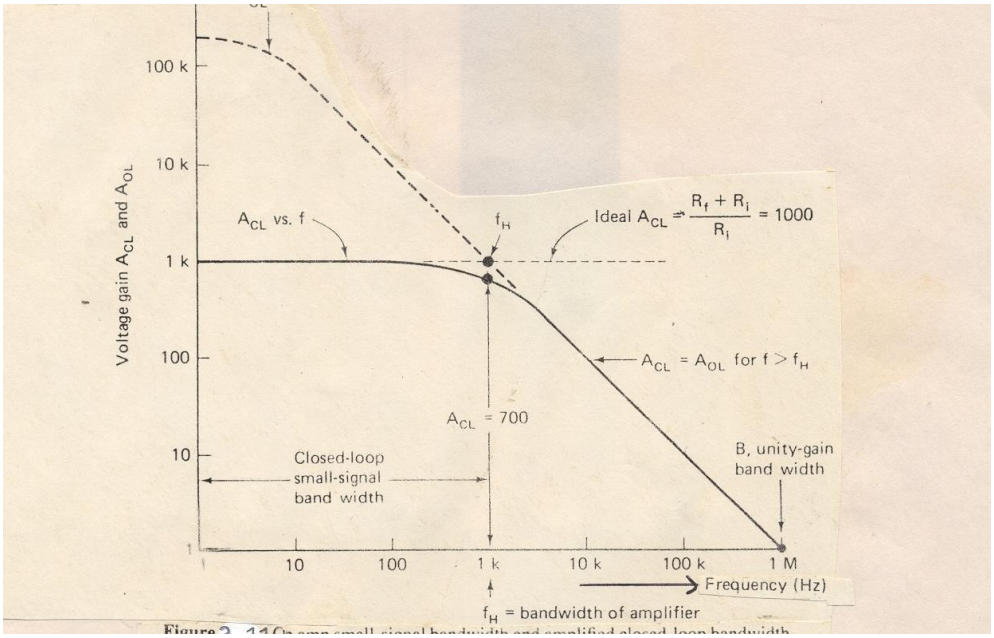


Fig. 3.9: Op amp small-signal bandwidth and amplified closed-loop bandwidth.

2.3.2.3 Slew Rate & Output Voltage

Slew rate of an op. amp is how fast the output voltage can change, and is usually given in V/μs. There are several factors that determine the slew rate; such as amplifier gain, compensating capacitors, and even whether the output voltage is going positive or negative. The slowest slew rate occurs at unity gain, and as such, slew rate is usually specified at unity gain.

Cause of Slew-Rate Limiting

At least a capacitor is usually connected within or outside the op.amp circuitry to prevent oscillation: The part of the op.amp connected to this capacitor is capable of supply a maximum current I, limited by the op.amp design. Then slew rate can be defined by,

$$Slew\ Rate = \frac{Output\ voltage\ change}{time} = \frac{1}{C} \quad V/\mu s$$

From this equation, a faster slew rate requires the op amp to have either a higher maximum current or a smaller compensating capacitor.

2.3.2.4 Noise in the output Voltage

Undesired electrical signals in the output voltage are classified as noise, which is generated by all electrical devices and their controls. Noise could be generated internally by the op-amp or externally to the op.amp. External noise can be minimized by proper construction techniques and circuit selection.

(a) Noise in Op. Amp Circuits

Assuming there were no external noise, then the noise in the output voltage caused by the op.amp. could be modeled by a noise voltage V_n, as shown in Figure 3.10.

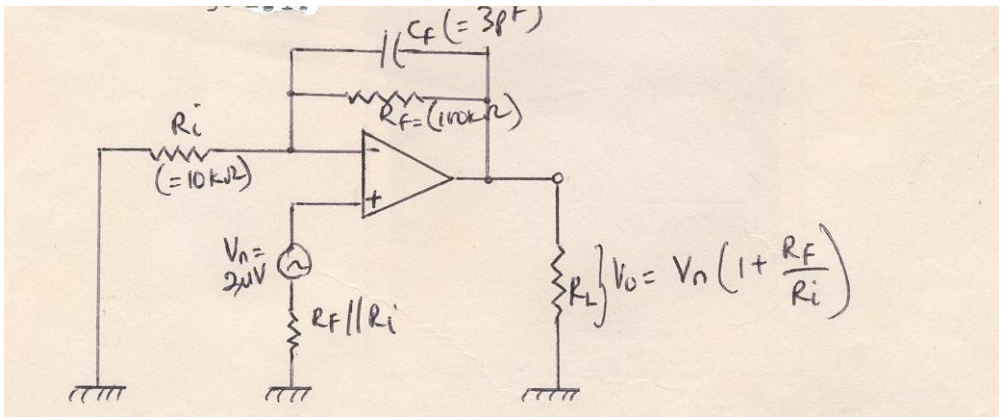


Fig. 3.10: Op amp noise is modeled by a noise voltage in series with the non-inverting input.

V_n is usually specified in μV (rms value). For different values of source resistance, R_i over a particular frequency range. For example, the 741 op. amp has 2μV of total noise over a frequency range of 10Hz – 10kHz and for R_1 between 100 Ω and 20k Ω. Thus R_1 should be kept below

$20k\Omega$ to minimize noise in the output, otherwise, V_n increases directly with R_1, once R_1 exceeds $20k\Omega$.

(b) Noise Gain

The noise gain = $1 + R_F/R_i$

To reduce the effects of op. amp noise:

1. If possible, avoid large values of resistors (R_i and R_F in particular), so as to have R_i within the range of frequency and resistance, and also low values of R_F minimizes the effects of noise currents.
2. Always connect a small capacitor (3pF) across R_F. This reduces the noise gain at high frequencies.
3. Never shunt R_i with a capacitor, otherwise, at higher frequencies the R_iC combination will have a smaller impedance than R_i alone, and gain will increase with frequency thereby aggravating the situation.
4. Finally, $R_i \leq 10k\Omega$.

For example, in an inverting adder, the noise gain is (1 + no of inputs). Thus to reduce the noise voltage being excessively amplified for inputs more than one, low amplitude signals should be pre-amplified before connecting to an adder circuit.

2.3.2.5. External Frequency Compensation

For an internally frequency compensated op.amps, there are prices to be paid for achieved stability. These are, limited small-signal bandwidth, slow slew rate and reduced power bandwidth. Internally compensated op. amps. are useful at audio frequencies but not at higher frequencies.

In order for designers to play-around with these trade offs, manufacturers of op. amps. bring out, up to 3 frequency compensating terminals. Thus the op. amp is classified as externally frequency – compensated.

(a) Single Capacitor Compensation

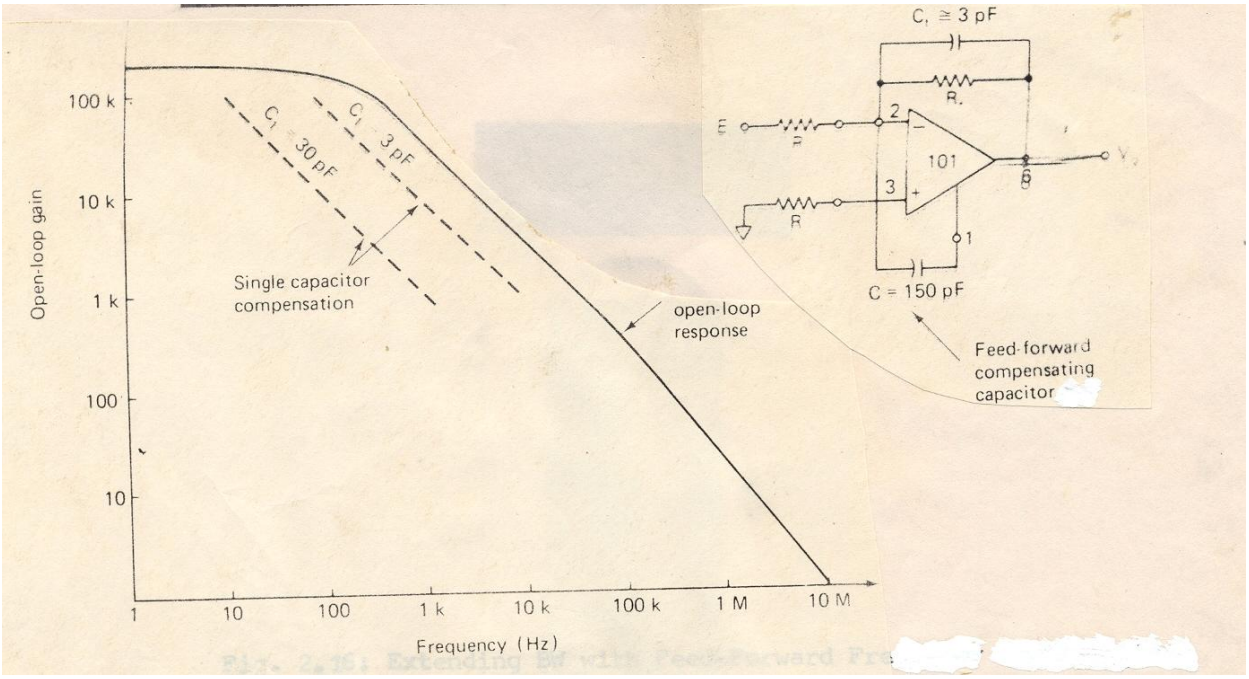


Fig. 3.11. Extending frequency response with an external compensating capacitor.

The effect of varying the frequency compensating capacitor, C, is shown in Figure 3.11.

b) Feed-Forward Frequency Compensation.

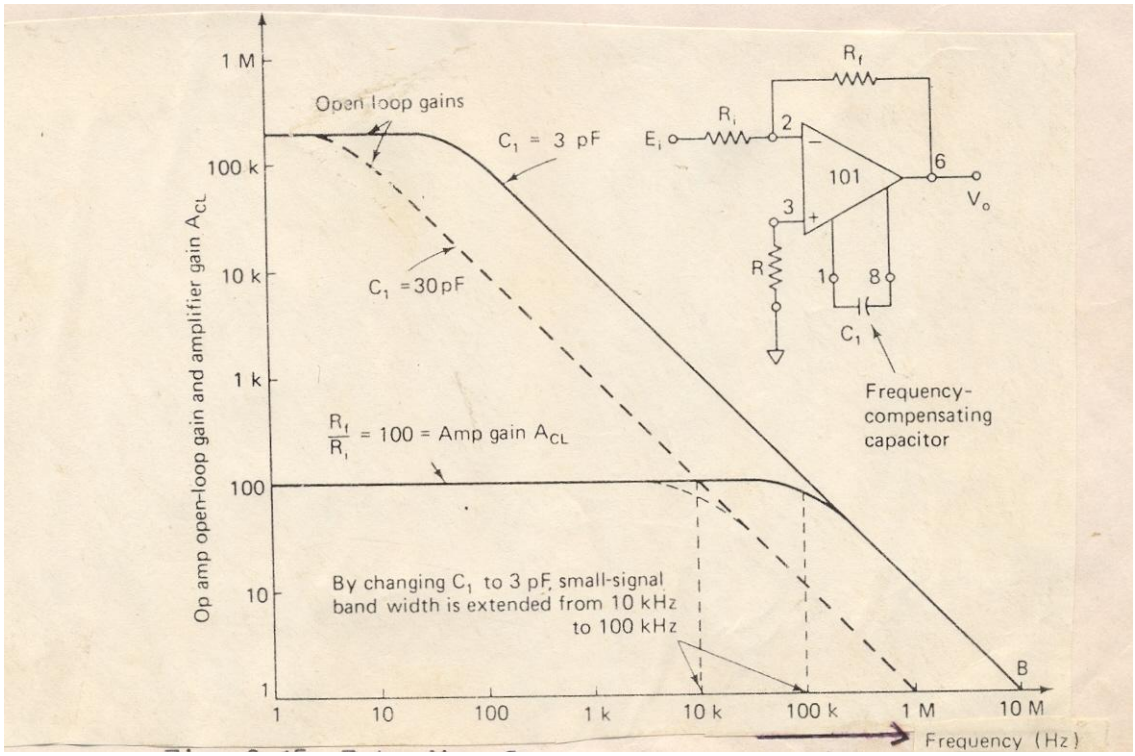


Fig. 3.12: Extending bandwidth with feed-forward compensation.

There are other types of frequency compensation, such as the two-capacitor (or two-pole) compensation, and feed forward compensation. The type best suited for a desired application would be given in the manufacturer's data sheets. Figure 3.12 shows a feed-forward compensation for the 101, which is compared to single capacitor compensation. The capacitor C_F

across R_F is for stability purpose. The full-power bandwidth and the slew-rate are increased, so also is the high-frequency gain and hence the high-frequency noise. As a result, frequency compensation techniques must be applied only to extend required for a circuit, otherwise there will be unwanted amount of high frequency noise in the output.

3. APPLICATIONS

As the op. amp has become familiar to the individual working in process control and instrumentation technology a large variety of circuits have been developed with direct application. In general, it is much easier to develop a circuit for a specific service using op. amps than discrete component, and with the development of low cost, IC op.amps., it is also a practical design. Op. amp applications could be classified into linear and non-linear, and it would be impossible to mention all of them in this write-up.

3.1. Basic Applications

3.1.1 Inverting and Non-Inverting Amplifiers.

An external feedback resistor, connected between the output terminal and (-) input terminal is used to control the gain of the amplifier.

The resulting circuit now has a closed-loop gain or amplifier gain, $A_{CL,}$ which is independent of A_{OL}.

(a) Inverting Amplifier

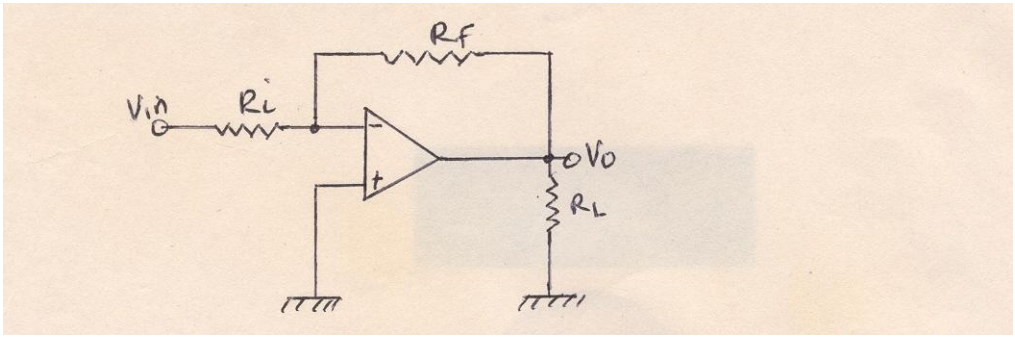


Fig 3.13: Inverting Amplifier

The closed-loop gain, A_{CL} is $A_{CL} = V_0/V_{in} = -R_F/R_I$

Therefore, depending on the ratio of R_F and R_i, the circuit either attenuate or amplify. V_0 is inverted with respect to $V_{in,}$ and V_{in} could either be dc or ac signal. The input impedance is essentially equal to R_i and since R_i is not large, then the input impedance is not large.

(b) Non-inverting Amplifier

The general non-inverting amplifier is shown in figure 3.14.

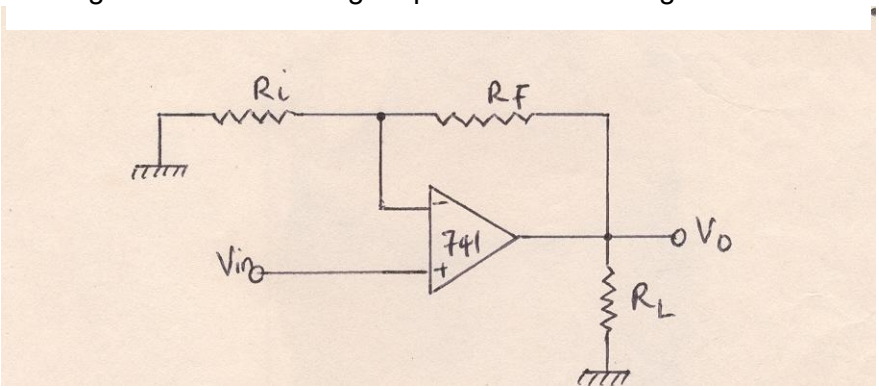


Fig. 3.14: Non-inverting Feedback Amplifier.

The amplifier gain is given as,

$A_{CL} = V_0/V_{in} = 1 + R_F/R_I$

Thus the gain is always greater than, or equal to, unity. If $R_F = 0$ and $R_I = \infty$, the gain is exactly 1 and the amplifier acts as a voltage follower; the output voltage follows the input voltage exactly. The advantage of such a voltage follower, and of non-inverting circuits in general, is the impedance buffering property, i.e.,

$R_i \longrightarrow \infty$ (typically exceeding 100MΩ)

$R_0 \longrightarrow 0$ (typically less than 100Ω)

3.1.2 Voltage-to-Current Converter

Figure 3.15. is a voltage-to-current converter. The circuit is often required in process control (or when driving a deflection coil in a television tube) where signals are often transmitted as a current.

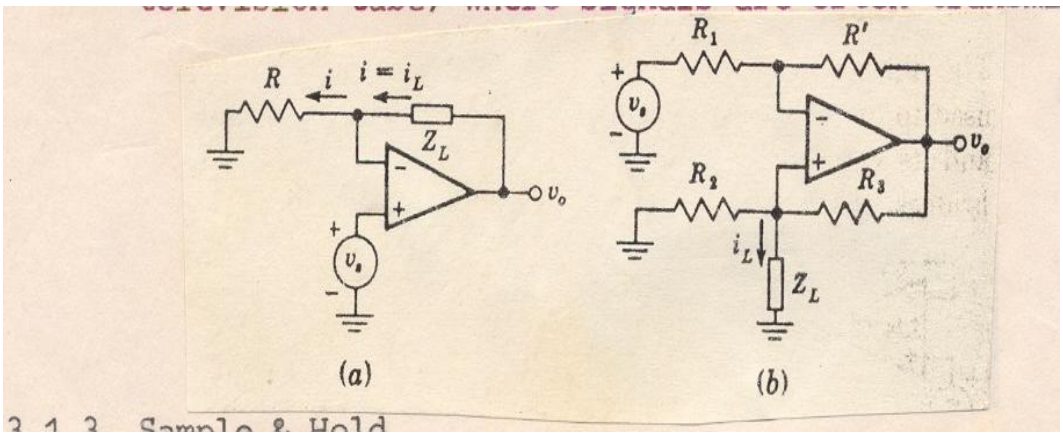


Fig 3.15: Voltage-to-current converter for (a) a floating load and (b) a grounded load Z_L

3.1.3 Sample and Hold

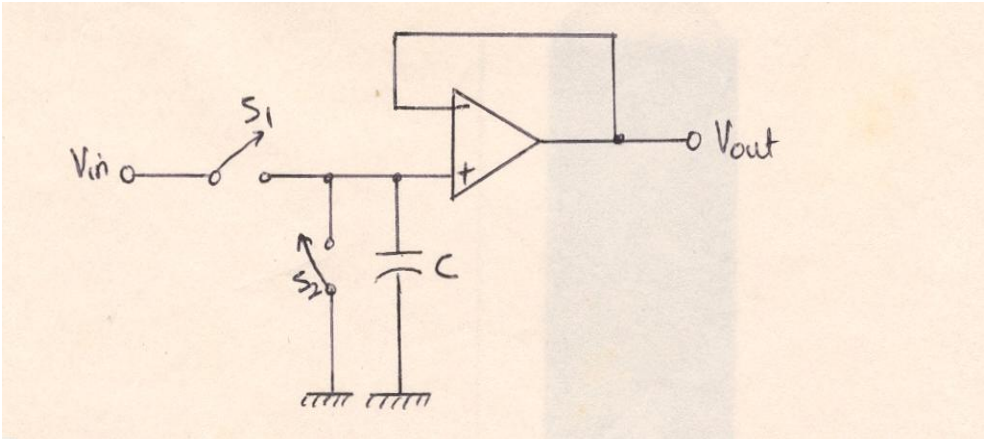


Figure 3.16: Sample & Hold circuit, S_I is closed to take a sample and open to hold the sample. S_2 is closed to reset.

The circuit of Figure 3.16 is used when measurement must interface with a digital process in a control or measurement situation, it is often necessary to provide a fixed value to an analog-to-digital converter (ADC) Switches S_1 and S_2 are usually electronic switches activated by digital logic levels.

3.1.4 Integrator

The integrator, shown in Figure 3.17, consists of an input resistor and feedback capacitor.

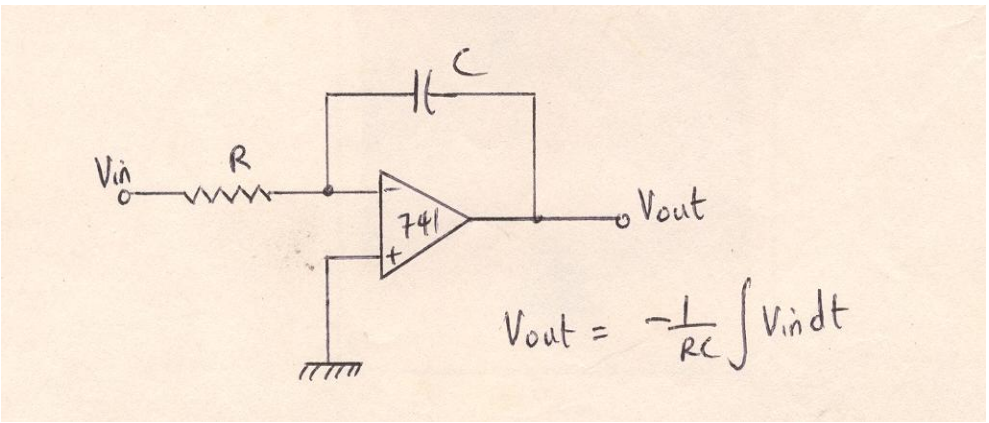


Fig 3.17: Integrator circuit. A switch is placed across the capacitor to reset the integral.

One typical application of the integrator is illustrated in Figure 3.18, where it is used in conjunction with a comparator to form a sawtooth-wave generator circuit. Other applications include among others adjustable timer circuit and triangular-wave generator.

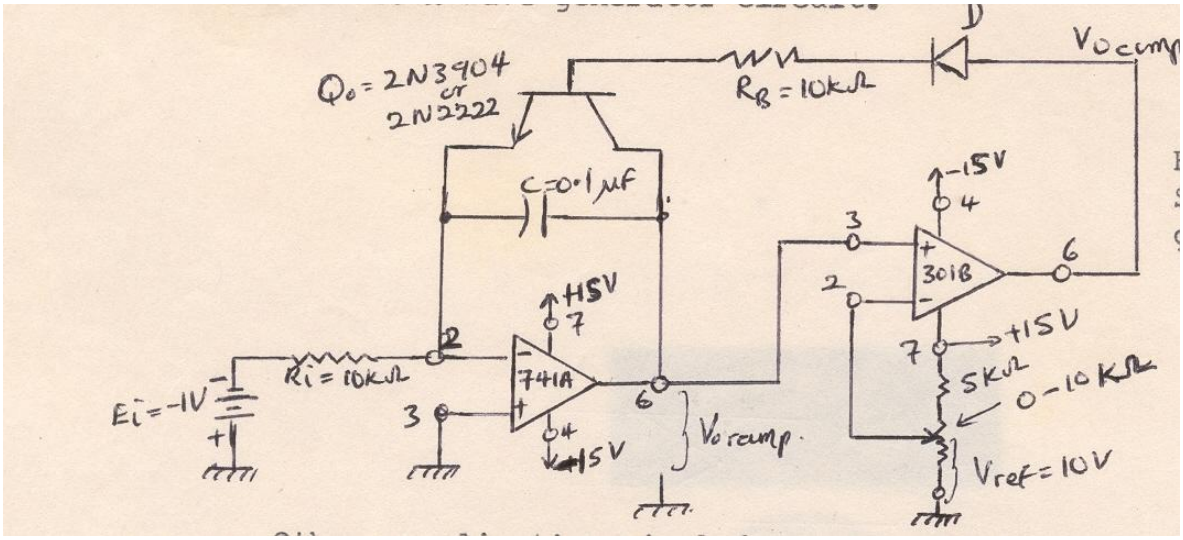
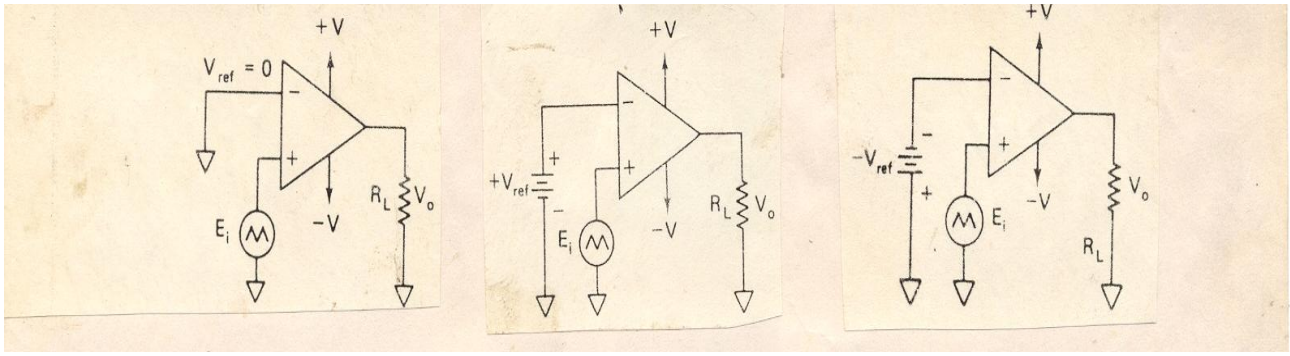


Figure 3.18 Sawtooth-wave generator circuit.

3.2 Voltage-Level Detectors

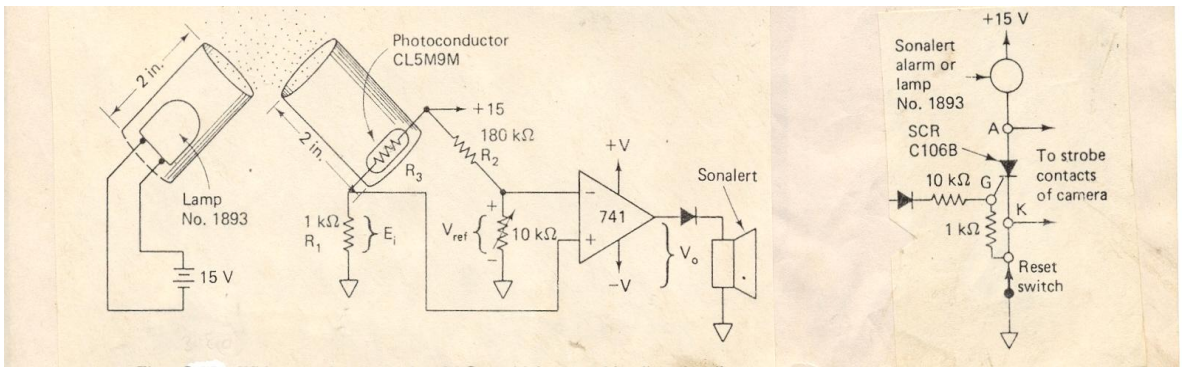
There are three types of level detector viz; zero-crossing-, positive – and negative level detectors, as shown in figure 3.19 for non-inverting voltage level detectors. Similar circuits also exist for inverting voltage level detectors.



(a) zero crossing (b) Positive level crossing (c) Negative level crossing

Fig 3.19: Level detectors.

3.2.1 Typical Applications of Voltage-level Detectors.



(a) (b)

Fig. 3.20 (a): With no smoke present the 10-kΩ sensitivity control is adjusted until the alarm stops. Light reflected off any smoke particles causes the alarm to sound.

(b) SCR Alarm circuit

Typical application is the smoke detector, of Figure 3.20a. In the absence of smoke, very little light strikes the photo-conductor and its resistance stays at some high value, typically several hundred kilo-ohms. The 10-k Ω sensitivity is adjusted until the alarm turns off. Any smoke entering the chamber causes light to reflect off the smoke particles and strike the photo conductor. The photo-conductor's resistance decreases and the voltage, E_1, across R_1 increases. As E_1 increases above V_{ref}, V_n switches from – V_{sat} to + V_{sat}, causing the alarm to sound. When the smoke particles leave the chamber, the alarm turns off.

For the alarm to stay on, the SCR alarm circuit of Figure 3.20b is used. Lamp and photo-resistor must be mounted in a flat back, light proof box that admits smoke. Ambient (room) light prevents proper operation.

Other applications include sound-activated switch and light column voltmeter.

These voltage-level detector circuits are generally known as comparator, and there exist specifically designed ICs to act as a comparator. These ICs (such as the 311 comparator) eliminate the disadvantages of using the general-purpose op. amp. The disadvantages are, slow response and the fixed saturation voltage, $-V_{sat}$ and + V_{sat} between which the output switches, thus not compatible with TTL digital logic IC's.

Neither the general-purpose op. amp not the comparator can operate properly if noise is present at either input. This problem is solved by having positive feedback.

ELEMENTS OF DIGITAL ELECTRONICS

1 INTRODUCTION

Electronic signals (current and voltages) are grouped into two categories – continuous and discrete. Continuous signals vary over a range of values with time. Examples are audio signals, temperature reading or light-detecting devices. These continuous signals are also referred to as analog signals. Discrete (Countable) signals are signals, which assumes discrete logic values 0, and 1, which actually represent low and high voltage levels respectively. Examples of devices using discrete signals are computers, calculators, and in fact the digital line used in the manufacturing of products in the NBL.

Discrete signals are the basis of digital electronics. Digital electronics is concerned with these two-state switching circuits i.e. they are designed to operate on voltage pulses which exist in one of two levels, 'high' and 'low' (1, 0). Digital devices are now commonplace at homes e.g. Digital audio, (CD player), offices, and industries.

Exercise : List 10 electronic devices each, which use Analog and digital signals.

In digital circuits, the voltage levels 1 and 0 correspond to High and low. These voltage levels are allowed to fall in some range. For example, with high – speed Transistor-Transistor Logic (TTL);

0 - 2.0 V = Low

2.1 – 5V = High.

The voltage levels high and low are given as logic 1 and 0 respectively and are used in Boolean logic to mean True and False respectively.

Rationale for digital circuits

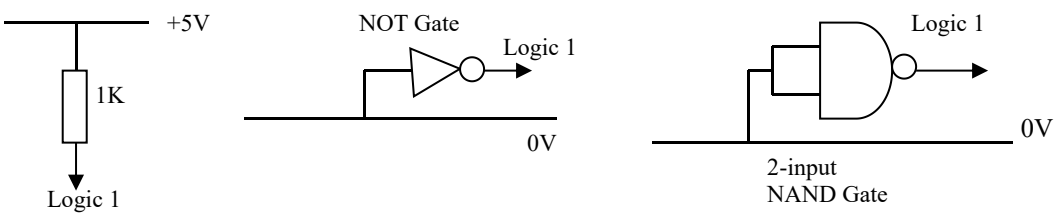
Many of the today's electronic devices and equipment come as digital devices. Why ?

1. Continuous signals are often accompanied with different kinds of noise in the circuits that transports them. The noise could come from capacitive coupling, external interferences, electrons movements, etc. These noises are often minimized in digital signals. Digital electronics is noiseless and perfect.
2. Digital devices have become so powerful that tasks that seem well suited to analog techniques are often better solved with digital methods. For example an analog temperature meter might incorporate a microprocessor and memory in order to improve accuracy by compensating the instrument's departure from perfect linearity. Because of the wide availability of microprocessors, such applications are becoming commonplace.

Creating Digital Signals

Providing logic 1, or logic 0 is simply a matter of connecting the appropriate input(s) to the positive supply rail or to the zero volt rail. E.g for logic 1, we could use any of the following connections:

Fig.1.1



On connecting to zero volt rail, we have logic 0, or using a pull-up resistor with gates as shown in fig.1.2 :

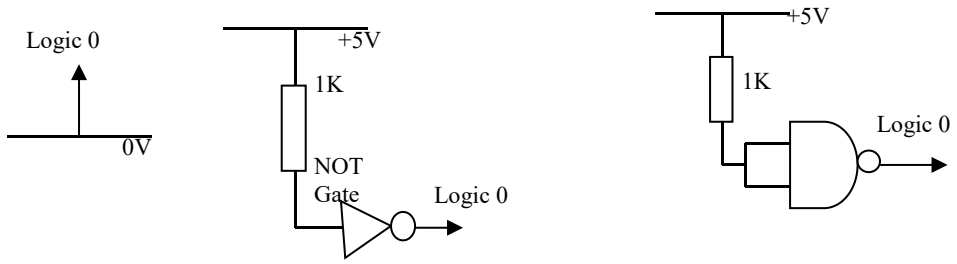


Fig.1.2

Numbers We Use in Digital Electronics

We can count ordinarily in base 10. A decimal (base –10) number is simply a string of integers that are understood to multiply successive powers of 10, the individual products then being added together. For instance;

$137.06 = 1 \times 10^2 + 3 \times 10^1 + 7 \times 10^0 + 0 \times 10^{-1} + 6 \times 10^{-2}$

However, the logic levels 0 and 1 which are used in digital electronics are in fact representations of binary numbers – base –2

The individual 1's and 0's are called bits (coined from binary digits). A number in base two can be converted to base 10 e.g. $1101_2 = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 13_{10}$. Also, base 10 numbers can be converted to base 2 ; thus

13/2 = 6 r 1
6/2 = 3 r 0
3/2 = 1 r 1
½ = 0 r 1

Answer = 1101_2
MSB LSB

LSB = Least Significant Bit
MSB = Most Significant Bit

Hexadecimal (hex) Representation

The binary number representation is the natural choice for two-state systems. But since the numbers tend to get rather long, hexadecimal (Base-16) representation is adopted. Each position represents successive powers of 16; with each hex symbol having a value from 0 to 15. The symbols A – F are assigned to the values 10 – 15 since we want a single symbol for each hex position. To write a binary number in hexadecimal, we just group it in 4-bit groups, beginning with the LSB, and write the hexadecimal equivalent of each group. For instance,

$707_{10} = 1011000011_2 = 10 \leftarrow 1100 \leftarrow 0011_2$
$(2_{10}) \quad (12_{10} = C) \quad (3_{10})$
$= 2C3_{16} = 2C3_H$

2 BASIC ELECTRONIC GATES

A gate is an electronic circuit having one or more inputs but only one output. An output signal occurs only for certain combinations of input signals; i.e. the combination arrangement of inputs determines the output.

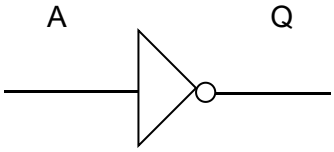
The various kinds of logic gates are switching circuits that 'open' and give a high output depending on the combination of signals at their inputs of which there is usually more than one. The behaviour of each type is summed-up in a "truth table" showing in terms of 1s (high) and 0s (Low) what the output is for all possible inputs

COMMON GATES ARE:

(1) NOT GATE (INVERTER)

- Simplest of the gates
- Only one input and one output
- The is an inverted version of the input

Symbol



Truth Table: The table that depicts the outputs given some inputs to the gate

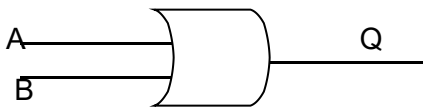
Input A	Output
0	1
1	0

Logical function $Q = \overline{A}$

2 OR GATE

The output is at high level (2.4 - 5v) only when at least one of the inputs to the gate is low (0 to 0.4v)

Symbol



Logical function Q = A + B

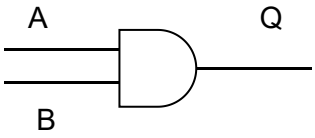
Truth table:

INPUTS		OUTPUT
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

3. AND GATE

The output is high only when both the inputs are high.

Symbol



Logic function Q = AB

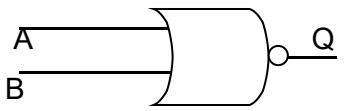
Truth table:

INPUTS		OUTPUT
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTE: if we have n inputs, then the number of possible combinations is 2^n

4 NOR GATE:

This is the inversion of an OR Gate (Not- OR)



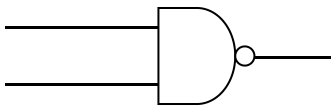
Logical function: $Q = \overline{A + B}$

Truth table:

INPUTS		OUTPUT
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

5. NAND GATE (NOT AND)

This is a complement of AND GATE



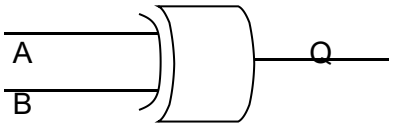
$Q = \overline{AB}$

Truth table:

INPUTS		OUTPUT
A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

6. EXCLUSIVE OR GATE (EX-OR)

There is output if both the inputs are different.

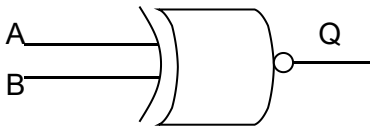


Truth table:

INPUTS		OUTPUT
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

7. EXCLUSIVE NOR GATE (EX-NOR)

There is output if the inputs are the same.



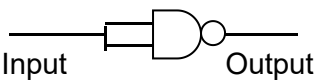
Truth table:

INPUTS		OUTPUT
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

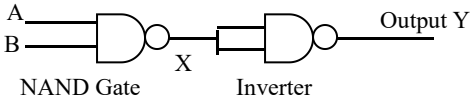
The NAND Gate as a Universal gate

NAND gates can be combined to produce other gates. Consider the following combinations

(i) NOT from NAND

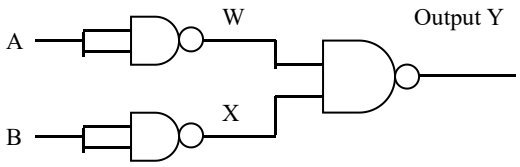


(ii) AND from two NAND Gates



Inputs			Output
A	B	X	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

(iii) OR from three NAND Gates



Exercise: Work out the Truth Table for this circuit

3 BOOLEAN ALGEBRA, KARNAUGH MAPS, COMBINATION AND SEQUENTIAL CIRCUITS

Boolean Algebra and Karnaugh Maps are used to simplify digital electronic logic functions and to minimize space for construction of the electronic components on the circuit board as well as to minimize the number of components to be used in the construction.

Boolean Algebra

Basic laws

1. Commutative Law A + B = B + A; A.B = BA
2. Associative Law (A + B) + C = A + (B + C)
   (AB)C = A(BC)
3. Distributive Law A (B+C) = A.B + A.C
   A + BC = (A+ B) (A+C)
4. Idempotence Laws
   A + A = A A.0 = 0
   AA = A AA = A
   A + 0 = A A.1 = A
   A + $\overline{A}$ = 1 A$\overline{A}$ = 0

Simplify
1. A + AB
2. (A + B)(A + $\overline{B}$)
3. A(A + B)
4. AB + A$\overline{B}$
5. Show that $A + \overline{A}B = A + B$
6. Show that $A\left(\overline{A} + B\right) = AB$

7. Simplify $\overline{A}B\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + AB\overline{C} + ABC$
8. Simplify $\overline{A}B\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + + ABC + \overline{A}BC + A\overline{B}C + A\overline{B}\,\overline{C}$
9. Simplify $\overline{A}B\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + + ABC + \overline{A}BC + A\overline{B}C + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + AB\overline{C}$
10. Simplify (AB + AB + AC)(AB + AB + AC)
11. Show that (AB + BC + ABC + ABCD) = AB + BC
12. Show that A + B + (A + CD)(A + BC) = A + B
13. Simplify ($\overline{A}$ + B)($\overline{A}$ + $\overline{B}$ + $\overline{C}$)($\overline{A}$ + $\overline{B}$ + C)(A + $\overline{B}$ + $\overline{C}$)(A + B + C)

DE MORGAN'S THEOREM

1. $\overline{ABC} = \overline{A} + \overline{B} + \overline{C}$

2. $\overline{A + B + C} = \overline{A}\,\overline{B}\,\overline{C}$

LOGICAL FUNCTIONS

1. MINTERMS (SUM OF PRODUCTS)

E.g. V = wx + xy + yz + xz

Each term must have the same number of variables for a standard minterm. These can also be represented on truth tables. A normal variable would stand for logic 1 while the complement of it would be logic 0.

Given the following table of function:

A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

The function can be expressed as a sum of products (Minterm) thus:

f(A,B,C) = Q = $\overline{A}B\overline{C} + A\overline{B}\,\overline{C} + AB\overline{C}$. I.e. the outputs at the Q column with 1 values are reckoned with.

Therefore, Q = M2 + M4 + M6 = Σm(2,4,6)

2. MAXTERMS (PRODUCT OF SUMS)

E.g. ($\overline{A}$ + $\overline{B}$ + $\overline{C}$)(A + $\overline{B}$ + C)(A + B + C)

For maxterms, the complimented variable takes logic 1 while the normal variable takes logic 0.

E.g.

A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

To get the maxterms, take all the cases of Q = 0

Q = (0,0,0)(001)(011)(101)(111)

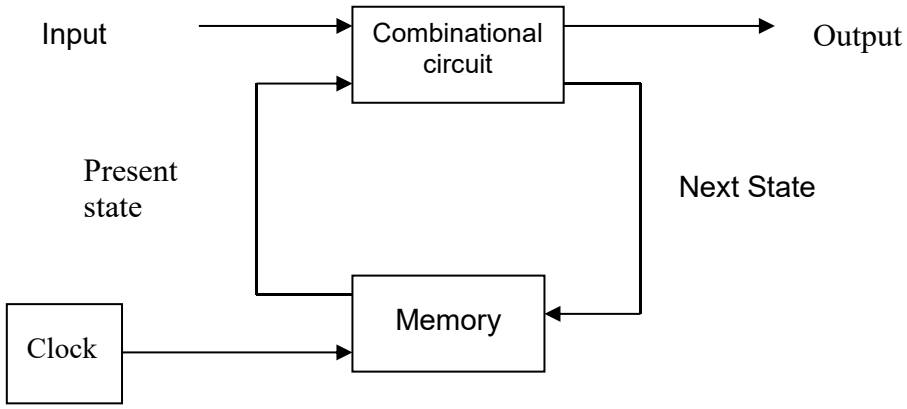
= ($\overline{A}$ + $\overline{B}$ + $\overline{C}$)($\overline{A}$ + $\overline{B}$ + C)(A + $\overline{B}$ + $\overline{C}$)($\overline{A}$ +B+ $\overline{C}$)(A + B + C)

= $\prod$M(0,1,3,5,7)

= $\prod$(0,1,3,5,7)

SEQUENTIAL LOGIC

All along, we have been considering combinational circuit in which case outputs depend on the inputs. With sequential logic, the output depends on the inputs as well as the past history (previous output). This is why sequential logic is used in memory design and construction.

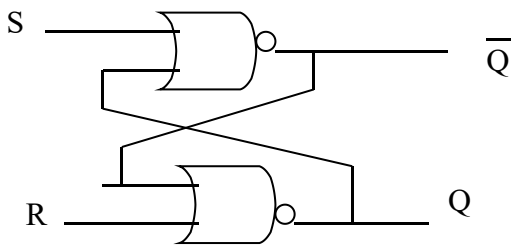


The basic essentials of a sequential logic design are:

1. combinational circuits (array of gates)
2. memory elements (array of flip flops)
3. clock signal (for synchronization)
4. Some means of presetting an input state.

BASIC FLIP FLOPS

RS – LATCH



NOR
GATES

S	R	Qt	Qt+1	
0 0	0 0	0 1	0 1	No Change
0 0	1 1	1 0	0 0	Resets
1 1	0 0	0 1	1 1	Sets
1 1	1 1	0 1	X X	Ambiguous

$Q+ = S+ \overline{R}\, Q$

A simple RS latch is a simple memory circuit. When R = S = 0; there is no change in the outputs. This is when the memory element stores data. The ambiguous case when S = R = 1 is an invalid conditions which should not be allowed to occur.

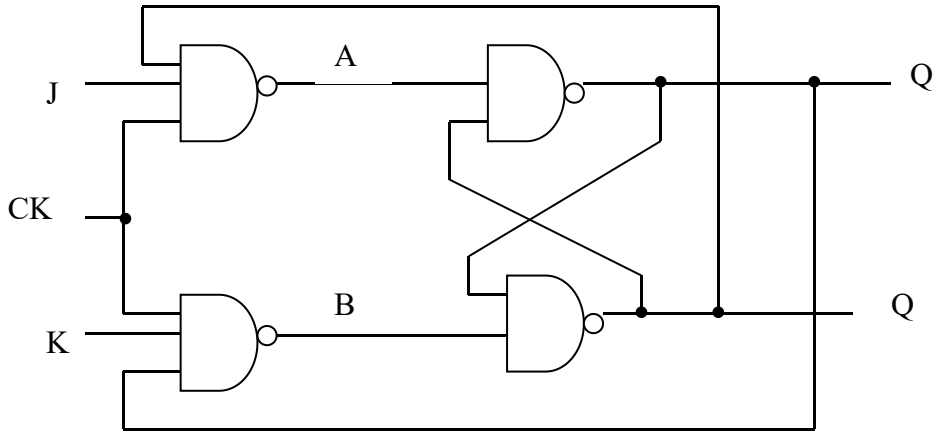
The circuit becomes stable when R = 1, Q = 0, $\overline{Q}$ =1 (i.e. when the memory is reset) or S = 1, Q = 1, $\overline{Q}$ = 0 (setting the memory).

In computers, when we reset, it means we are putting 0s into the memory locations (i.e. Q = 0 when R = 1). This is in contrary with when we set the computer (S = 1, Q = 1). The logical formula for the next state Q^+ is $Q^+ = S + \overline{R}\, Q$

Note: (1) The memory or ability of the flip flop to remember the past output to be used as input is achieved by feedback connections which ensure that when the input changes, the effect of the previous input is not lost.

(2) Basically a flip-flop is a bistable multivibrator whose output is either a low voltage or a high voltage, i.e. a 0 or a 1. The output stays low or high until the circuit is driven by an input called a “trigger”.

J – K FLIP FLOP



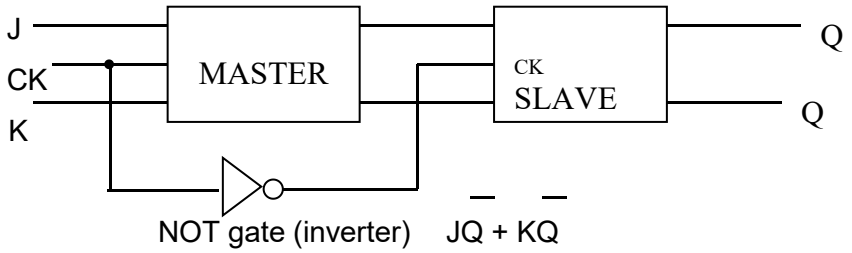
Inputs		Outputs Before Clock Pulse		During Clock Pulse		Outputs After Clock Pulse		Comments
J	K	Q	$\overline{Q}$	A	B	Q	$\overline{Q}$	
0 0	0 0	1 0	0 1	1 1	1 1	1 0	0 1	no change in outputs
1 1	0 0	1 0	0 1	1 0	1 1	1 1	0 0	Stays at or sets to Q = 1 and Q = 0
0 0	1 1	1 0	0 1	1 1	0 1	0 0	1 1	Stays at or resets to Q = 0 and Q = 1
1 1	1 1	1 0	0 1	1 0	0 1	0 1	1 0	Toggles

The J – K flip flop has a truth table which differs from that of the SR flip flop in that the unwanted indeterminate state (S =R = 1) does not exist. From the truth table it can be shown that when J =K =1 (equivalent to S=R=I in an SR flip-flop) this condition is allowed and causes “toggling” i.e. the circuit changes state.

Note: J is equivalent to S in SR flip flop and K = R.

The logic equation for determining the next state is $Q^+ = J\overline{Q} + \overline{K}Q$

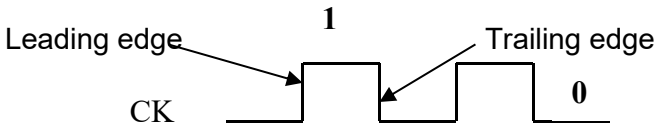
Most of the integrated J-K flip flops are either master-slave or edge triggered devices, if the duration of a clock pulse is greater than the switching time of a flip-flop outputs can “race” round to inputs, because of the feedback connections causing uncontrolled switching and unreliable. This problem can be overcome. If we use circuits using two flip flops with one called the “master” and the other “slave”



JK	00	01	11	10
0	0	1	1
1	0	0	1

When the clock is 'high' the inverted clock is 'Low' and isolates the slave from the master i.e. the slave is 'disabled'. The master responds to the data present at its J and K inputs and 'stores' the resultant state temporarily. At the end of the clock pulse, the inverted clock goes high, and then the data stored by the master is transferred to the slave and appears at the output terminals. This means that the output sate of a master-slave J-K flip-flop changes at the trailing edge of the clock pulse.

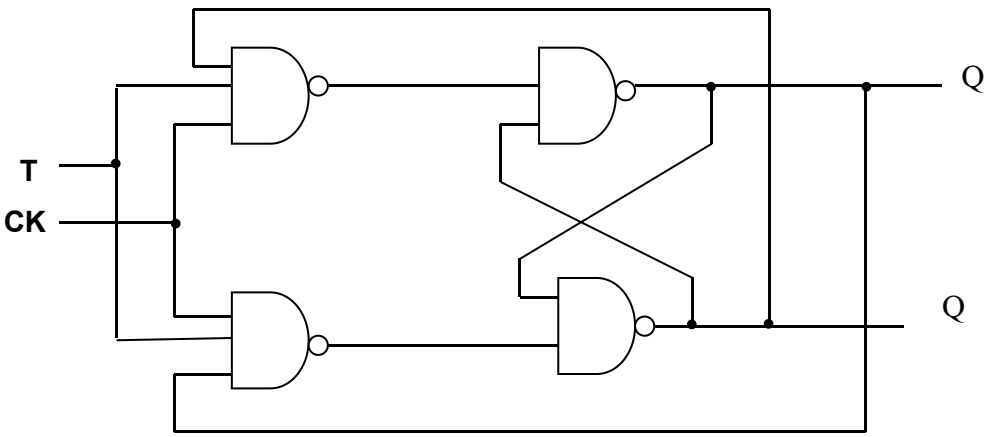
In the edge-triggered IC J-K flip flops, they change state as determined by the J and K inputs either as the clock changed from 1 to 0- a trailing-edge triggered device,- or as the clock changes from 0 to 1- a leading edge triggered device



One problem apart from the 'race' condition, with master-slave JK flip-flop is a slight delay in the circuit's operation. Why??

T-flip flop [Ex-OR function]

T stands for Toggle.



Note: Both J and K are joined together in the T- flip to form the input signal T.

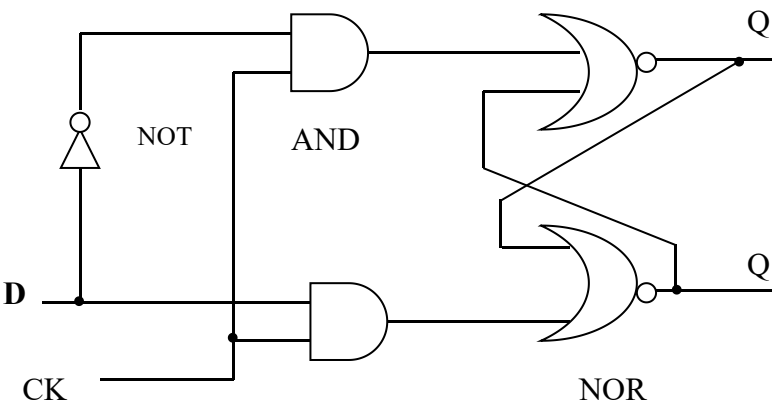
T	Q	Q^+	
0	0	0	
0	1	1	NOTE:
1	0	1	EX – OR operation
1	1	0	

The logical function is $Q^+ = \overline{T}\,Q + T\overline{Q}$

Or $Q^+ = T \oplus Q$

A T-flip flop is a controllable Toggle flip-flop. Depending on T, the toggling would either be stopped (T= 0, $Q^+ = 0 + Q = Q$, The flip flop is in the inhibit /stop mode), or initiated (T=1, $Q^+ = 1 + Q = Q$, the flip flop Toggles). With T-flip flop, the next state for memory Q+ always depend on Q. The set or reset input cannot be effected without applying information about Q.

D-flip-flop



CK	D	Q	Q^+	
0	0	0	0	No change
0	0	1	0	
0	1	0	1	
0	1	1	1	
1	0	0	0	$Q^+ \rightarrow D$
1	0	1	0	
1	1	0	1	
1	1	1	1	

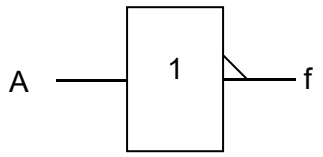
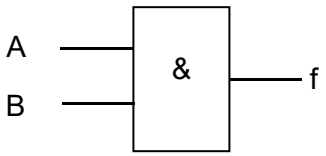
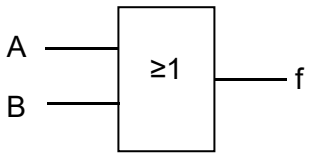
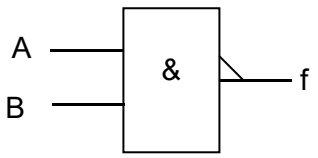
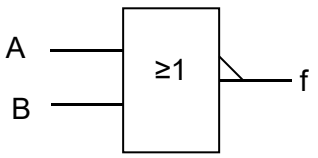
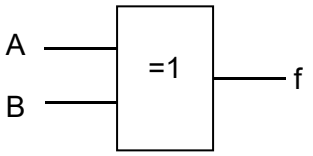
Q+ = Next state

Q = present state.

D actually stands for Data. D-flip-flop is mostly used in Buffer in connection with the line printer. The data input is the Data output. It has 2 control inputs, D and CK, D is the Data input, and CK is the clock input. Whenever the D flip-flop is clocked, the value of the data (D-input) is transferred to the output and then remains the same until the next time. As long as CK input to the AND gates is low, R and S are clamped at zero and Q cannot change. When CK is active (at logic 1) D is connected to S and D is connected to R.

The logic behaviour function is $Q^+ = D$

IEEE LOGIC SYMBOLS

S/N	LOGIC GATE	SYMBOL
1	NOT	
2	AND	
3	OR	
4	NAND	
5	NOR	
6	EXOR	
7	EXNOR