

2025 Chipathon 13th Weekly Layout Review

**IEEE Solid-State Circuits Society
Technical Committee on the Open Source Ecosystem (TC-OSE)
September 5th, 2025**



2025 Chipathon: Blocks & Bots: An Open Chip Playground augmented with LLMs



- ▶ **Phase 1 :** Setup and Introduction (June 13 - July 4 , 2025)
- ▶ **Phase 2 :** Team Formation and Project Planning (July 11 - July 25 , 2025)
- ▶ **Phase 3 :** Design and Simulation (Aug 1 - Aug 16 , 2025)
- ▶ **Phase 4 :** Layout and Verification (Aug 22 - September 26 , 2025)
- ▶ **Phase 5 :** Tapeout and Testing

2025 Chipathon: Schedule

Phase 3: Design and Simulation

Week	Date	Event	Review Focus	Recording	Slides	Report
Week 31	Aug 01, 2025	Schematic Review 	Analog/Digital	Watch	View	Submit
Week 32	Aug 08, 2025	Schematic Review 	MOSbius/Digital	Watch	View	Submit
Week 33	Aug 15, 2025	Dry Run Integration 	-	Watch	View	Submit
	Aug 16, 2025	READiness Check & Go/No-go Decision				



Phase 4: Layout and Verification

Week	Date	Event	Details	Recording	Slides	Report
Week 34	Aug 22, 2025	Layout Tutorial 	DRC, LVS, PEX (Mitch, Juan)	Watch	View	Submit
	Aug 22, 2025	DRC Dry-run	GDS to Channel Partner			
Week 35	Aug 29, 2025	Integration Tutorial 	Layout, Top level, ESD, padframe, packaging (Tim, Juan, Akira)	TBA	TBA	TBA
Week 36	Sept 05, 2025	Layout Review (blocks) 	-	TBA	TBA	TBA
Week 37	Sept 12, 2025	Layout Review (top level) 	-	TBA	TBA	TBA

Goals for Week 13

- ▶ Each team **must** nominate a members who will lead the top integration
 - POC: Juan Moya Baquero, Mitch
- ▶ Crunch time! Layout, verification, repeat
- ▶ Update your Github issues!

M13: SpikCore

Team members:

- Royce Richmond
- Rosendo valdes
- Oscar Islas
- Abraham alejandro

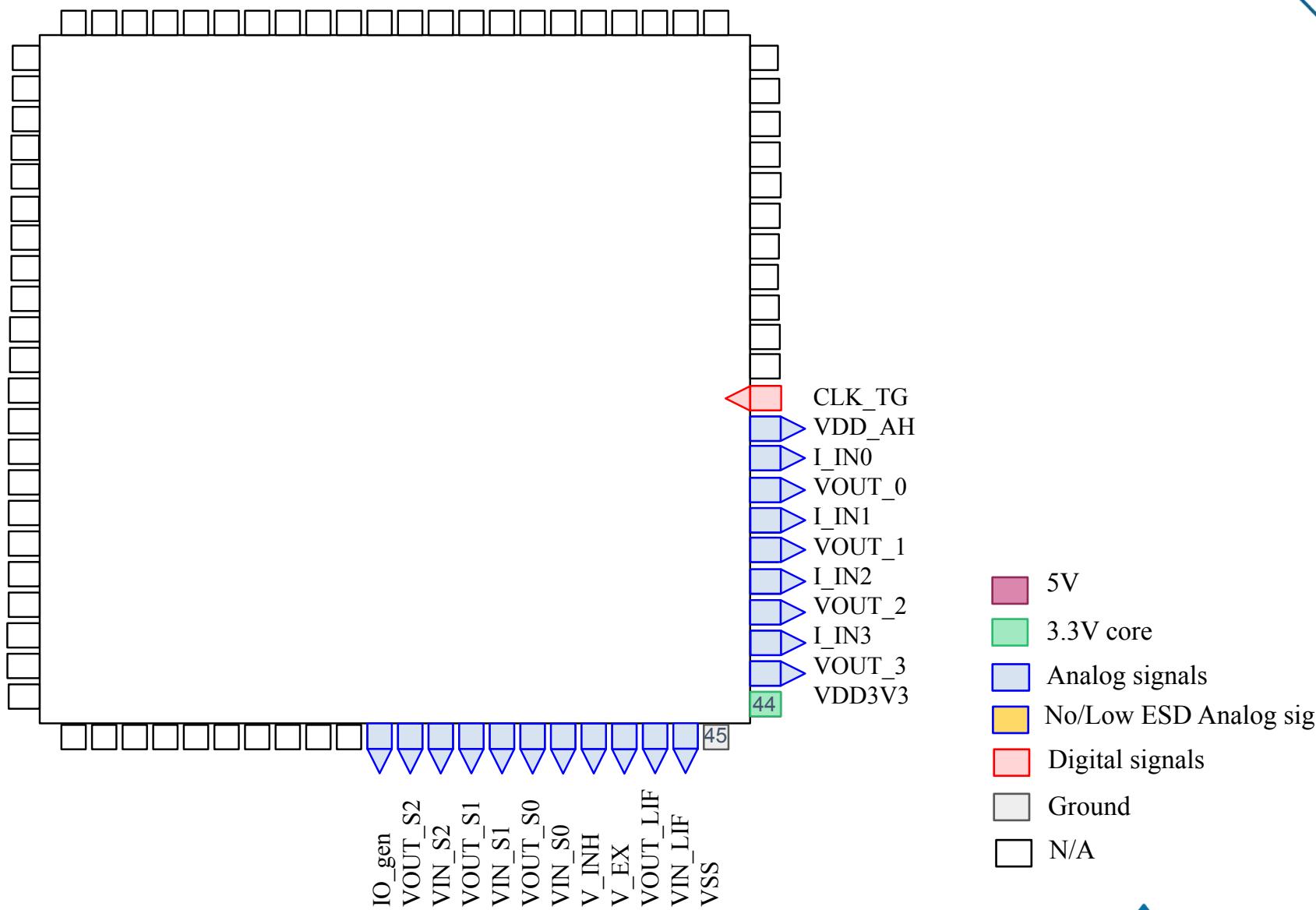
Contact email:

rramirezm2021@cic.ipn.mx

Total number of pins: 88
Total number of pins used: 22

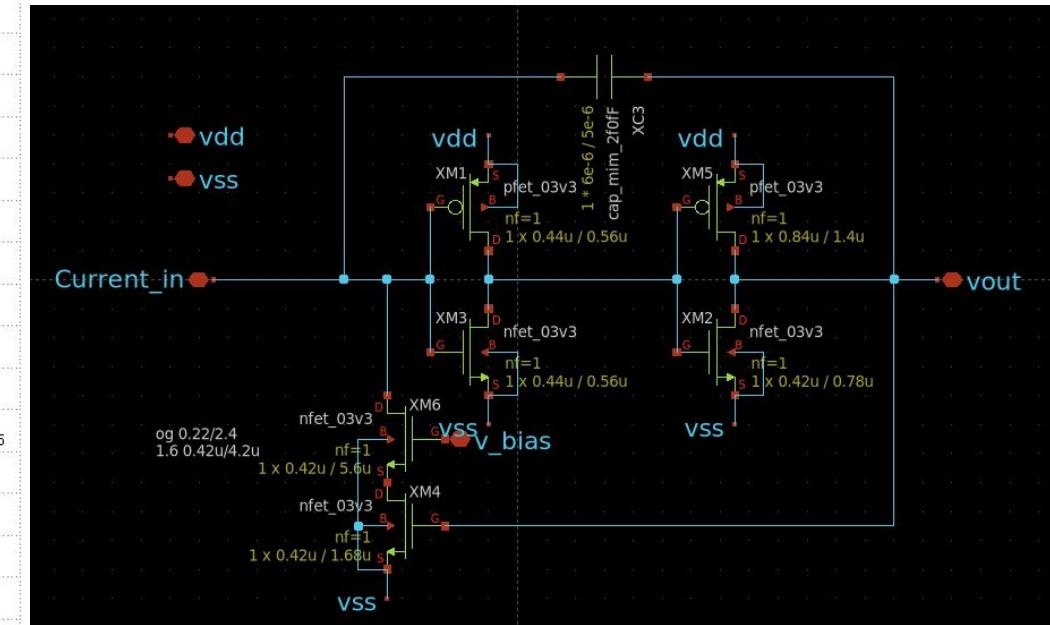
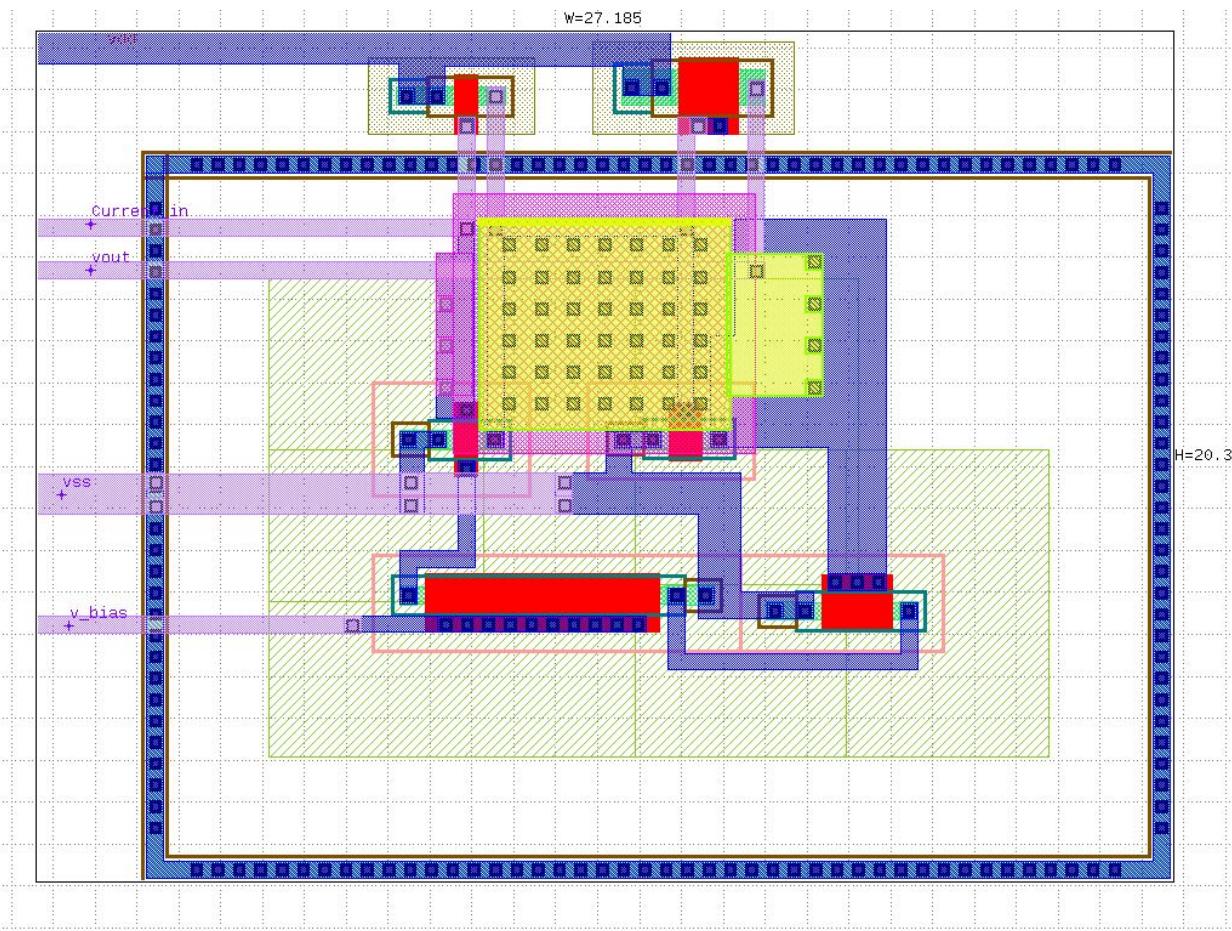
Chip area:

- AH neuron: 27.185um x 20.325um
- Synapse: 20.905um x 26.825um
- LIF neuron (ring oscillator): 35.215um x 14.975um
- LIF neuron (comparator): 60.725 um x 67.565 um
- TG bootstrapped: pending
- Schmitt trigger: 21.495 um x 9.315 um



M13: SpikCore

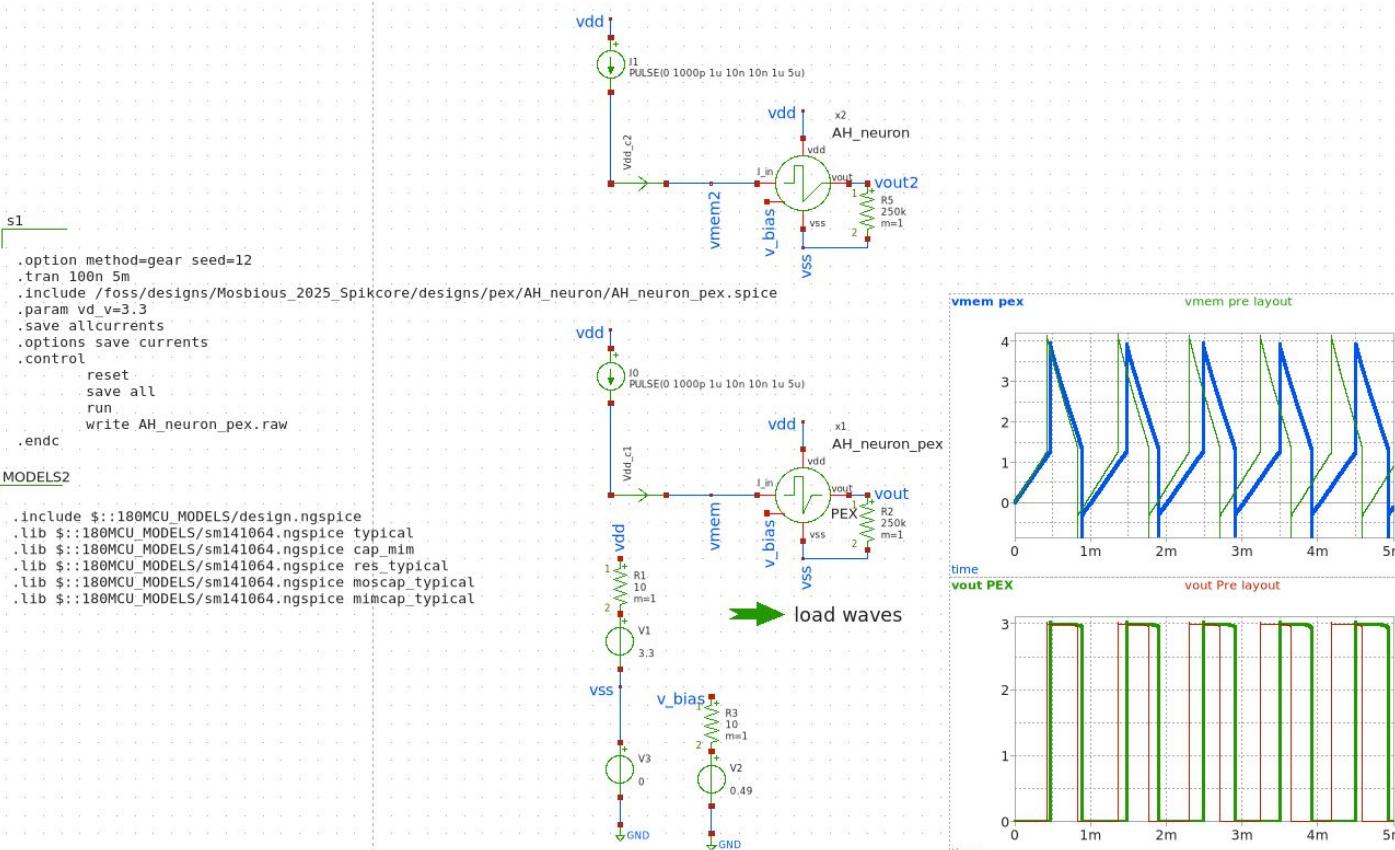
Axon Hillock (AH) Neuron



DRC and LVS clean
Layout size: 27.185um x 20.325um

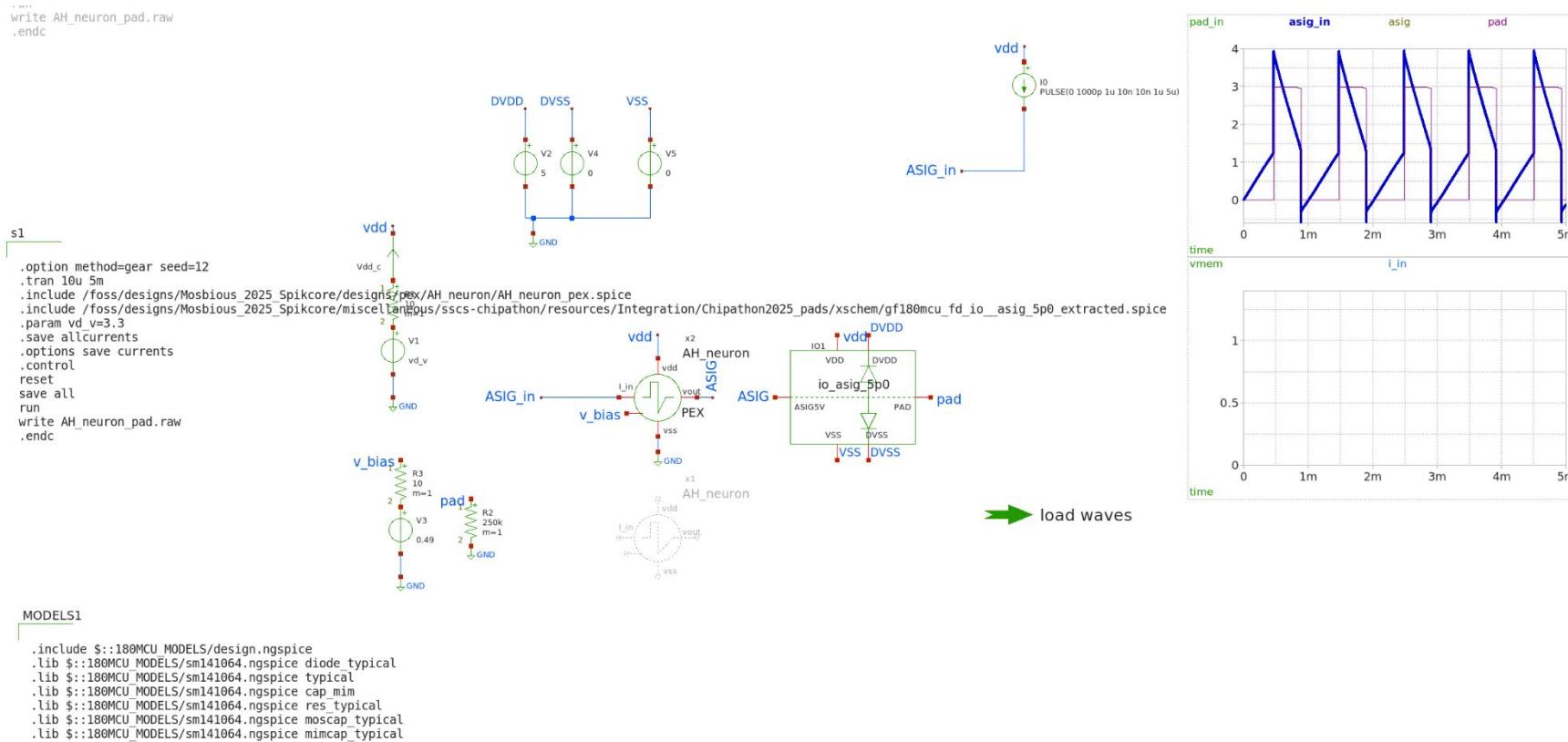
M13: SpikCore

PEX vs Schematic simulation Axon Hillock (AH) Neuron



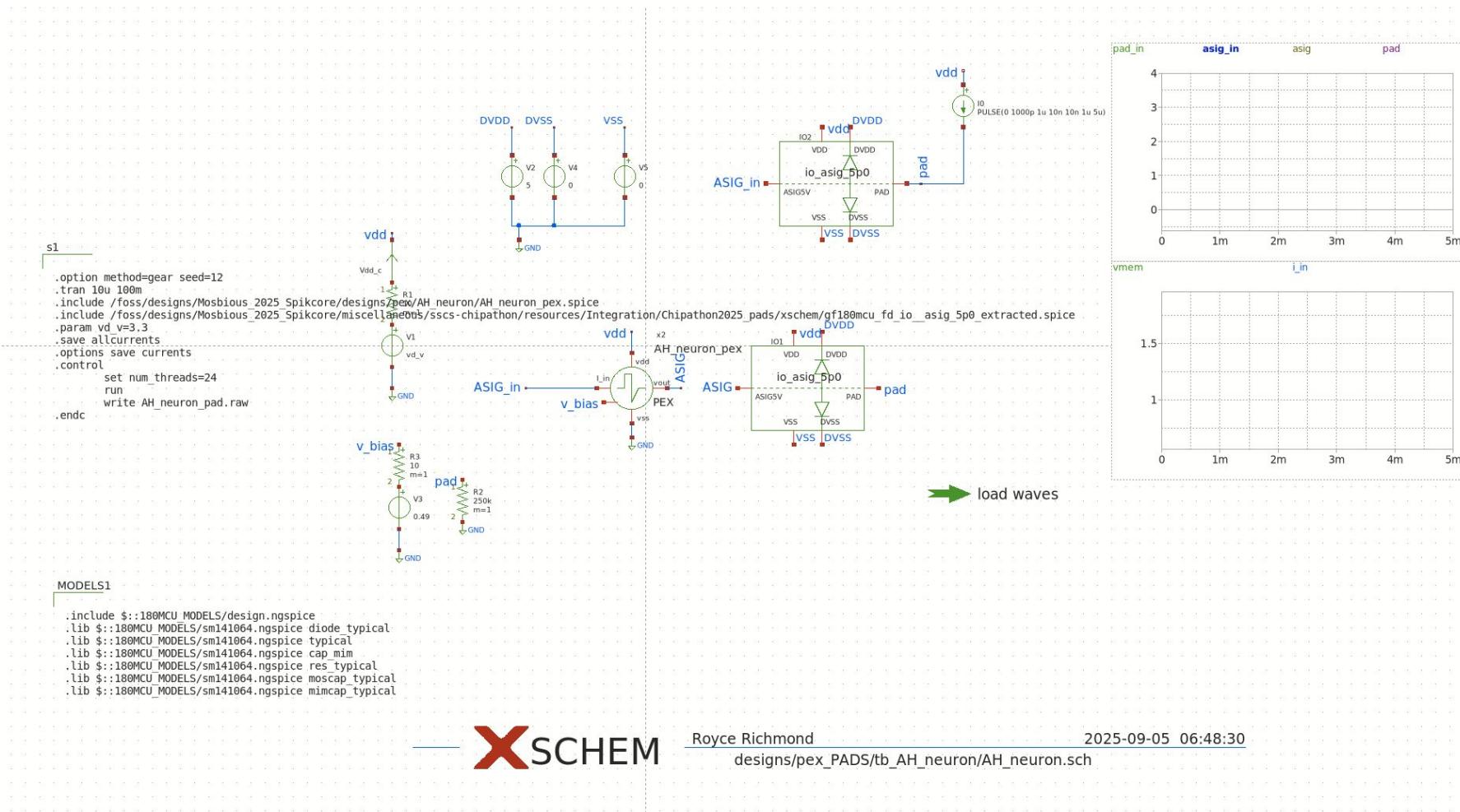
M13: SpikCore

PEX simulation + PAD (output) Axon Hillock (AH) Neuron



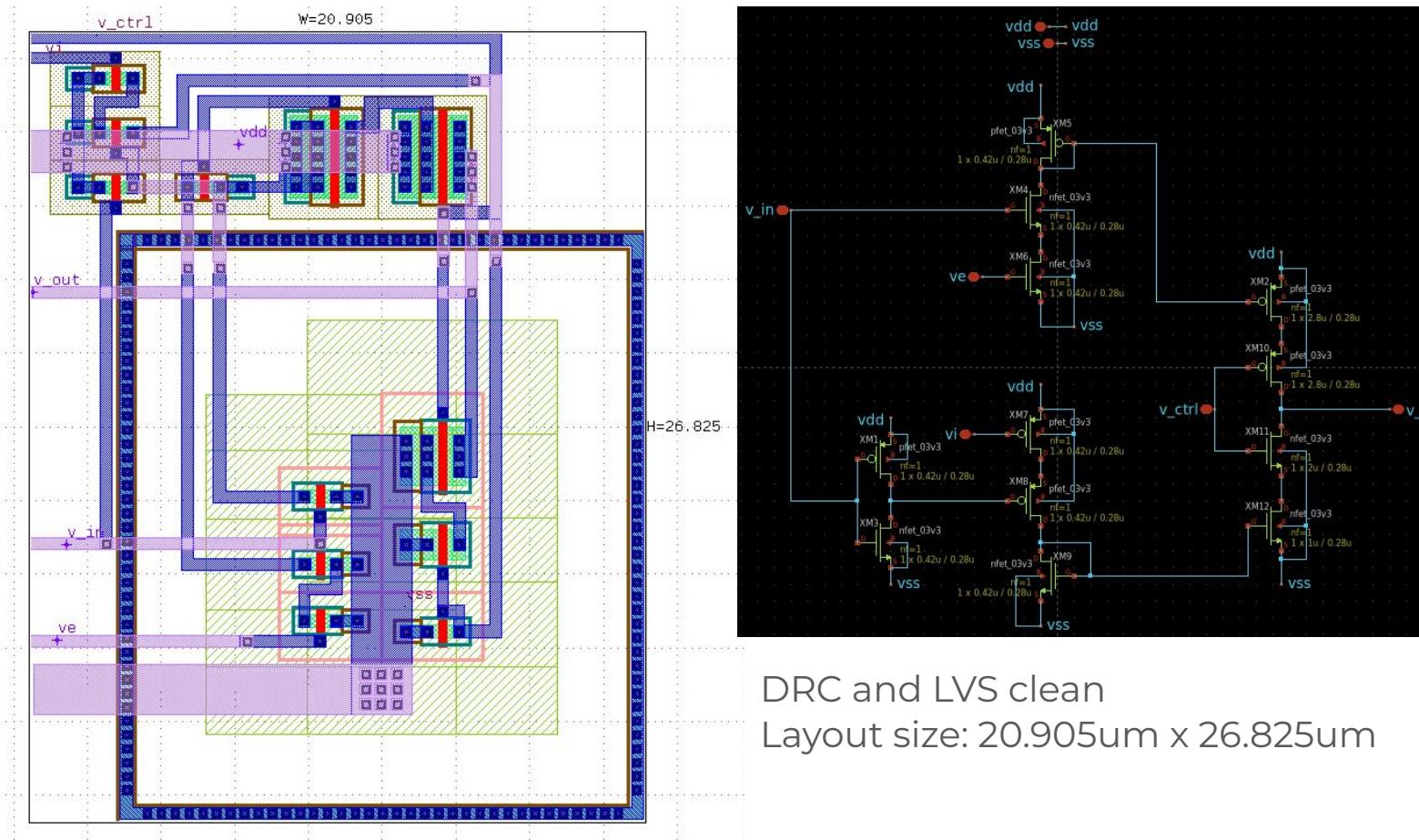
M13: SpikCore

PEX simulation + PAD (input and output) Axon Hillock (AH) Neuron



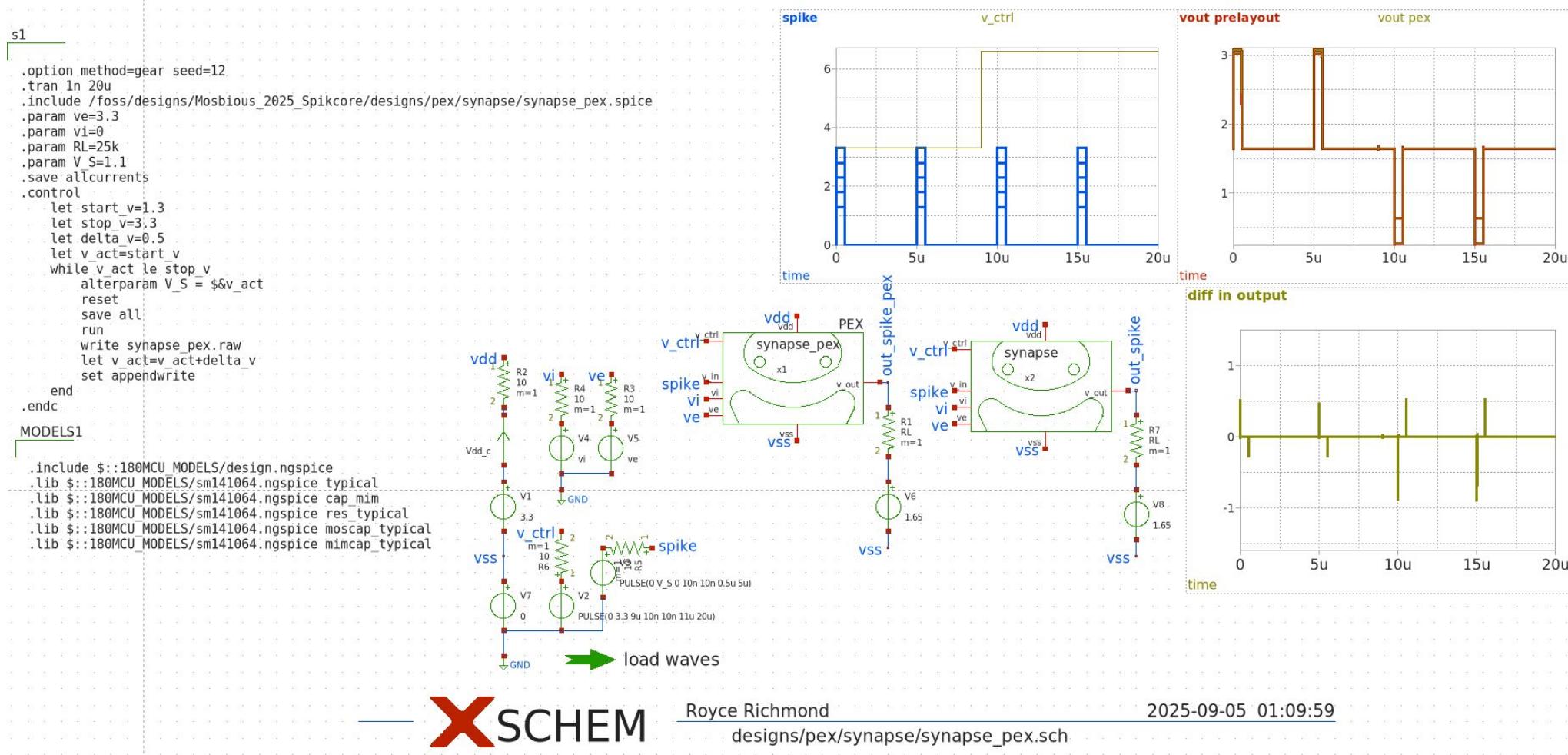
M13: SpikCore

Inhibitory / Excitatory synapse



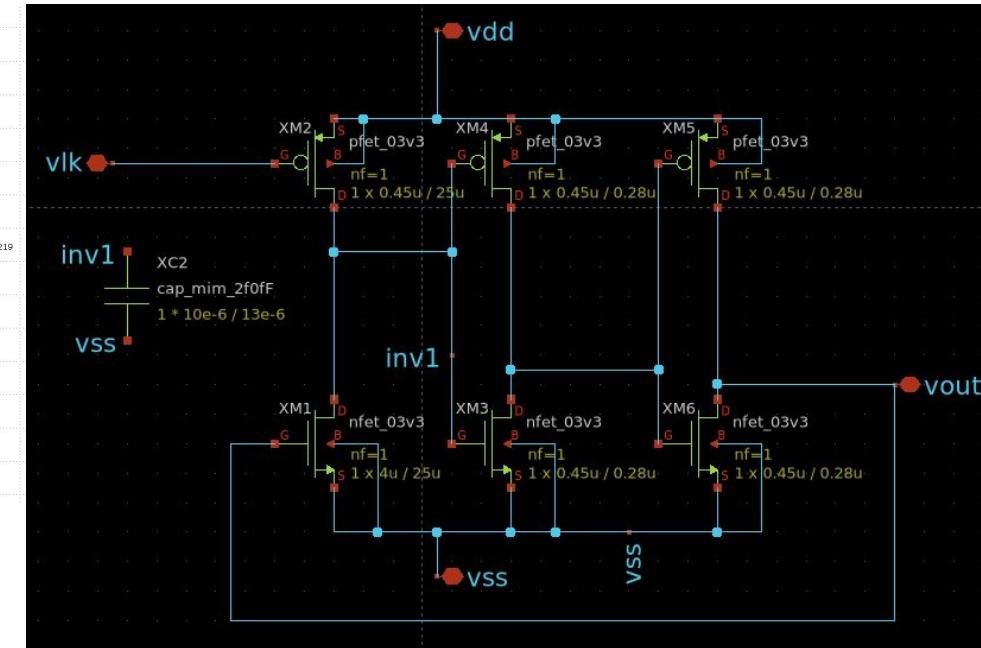
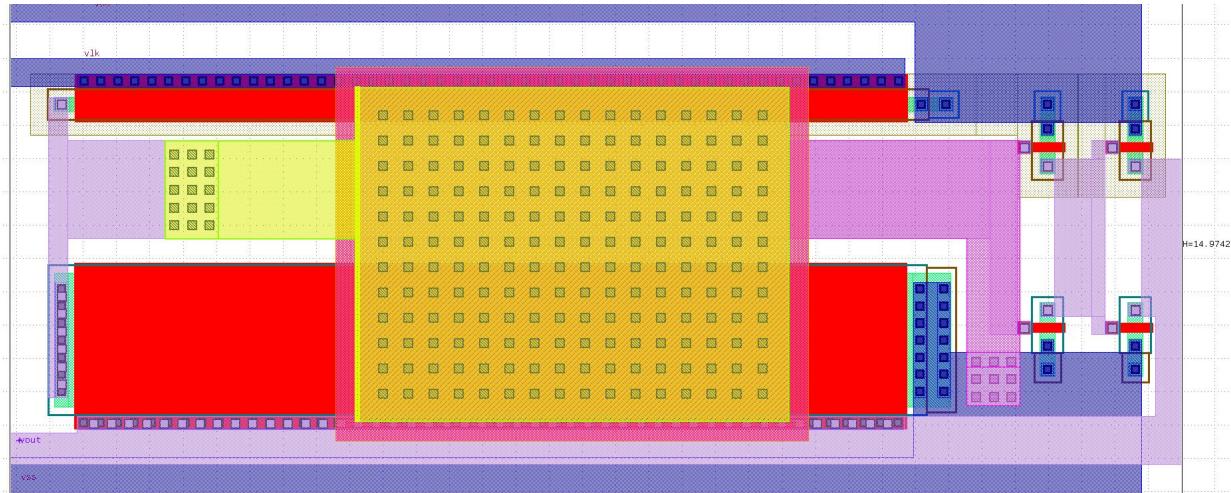
M13: SpikCore

PEX vs Schematic simulation Inhibitory / Excitatory synapse



M13: SpikCore

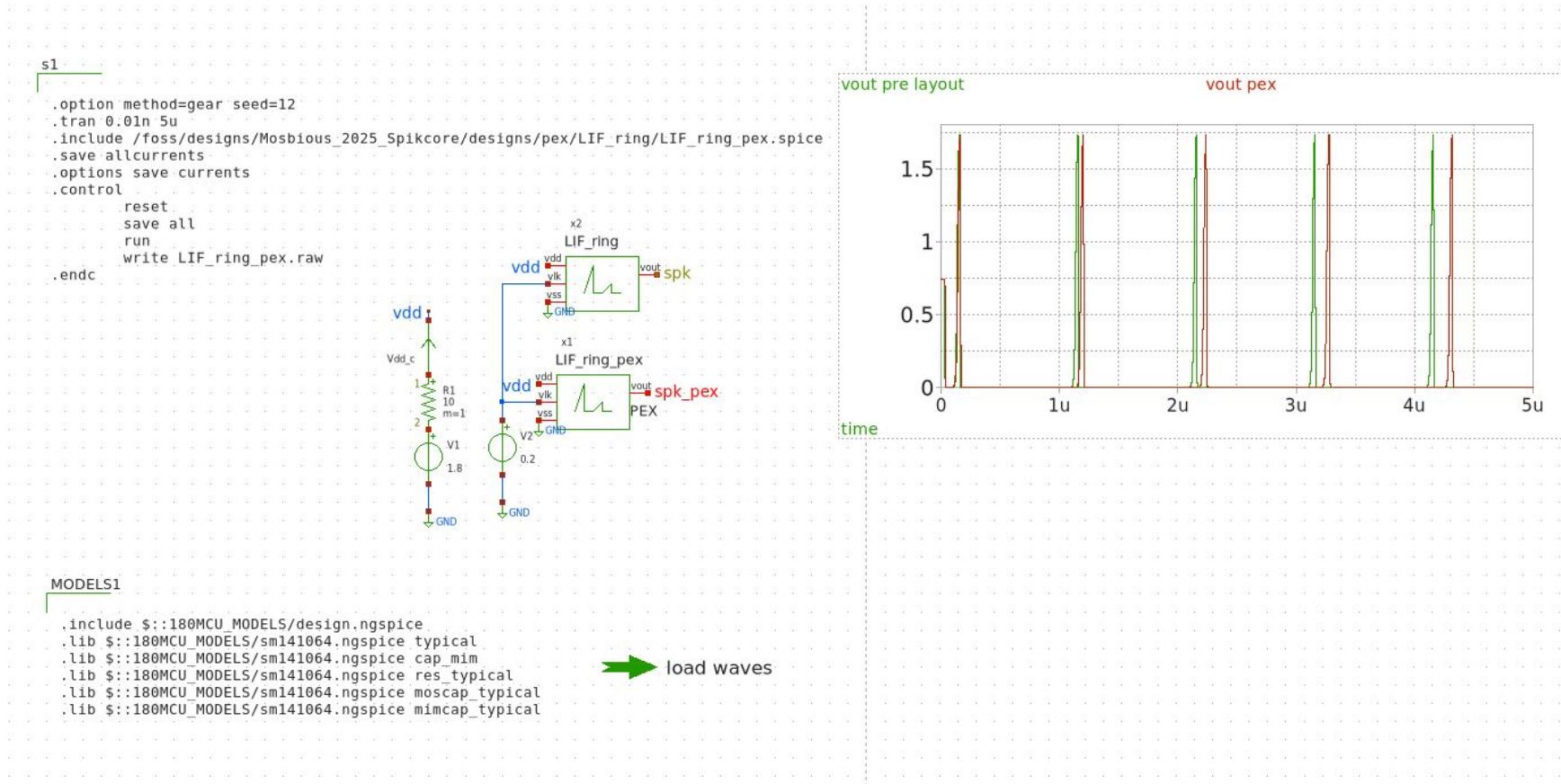
LIF neuron (ring oscillator)



DRC and LVS clean
Layout size: 35.215um x 14.975um

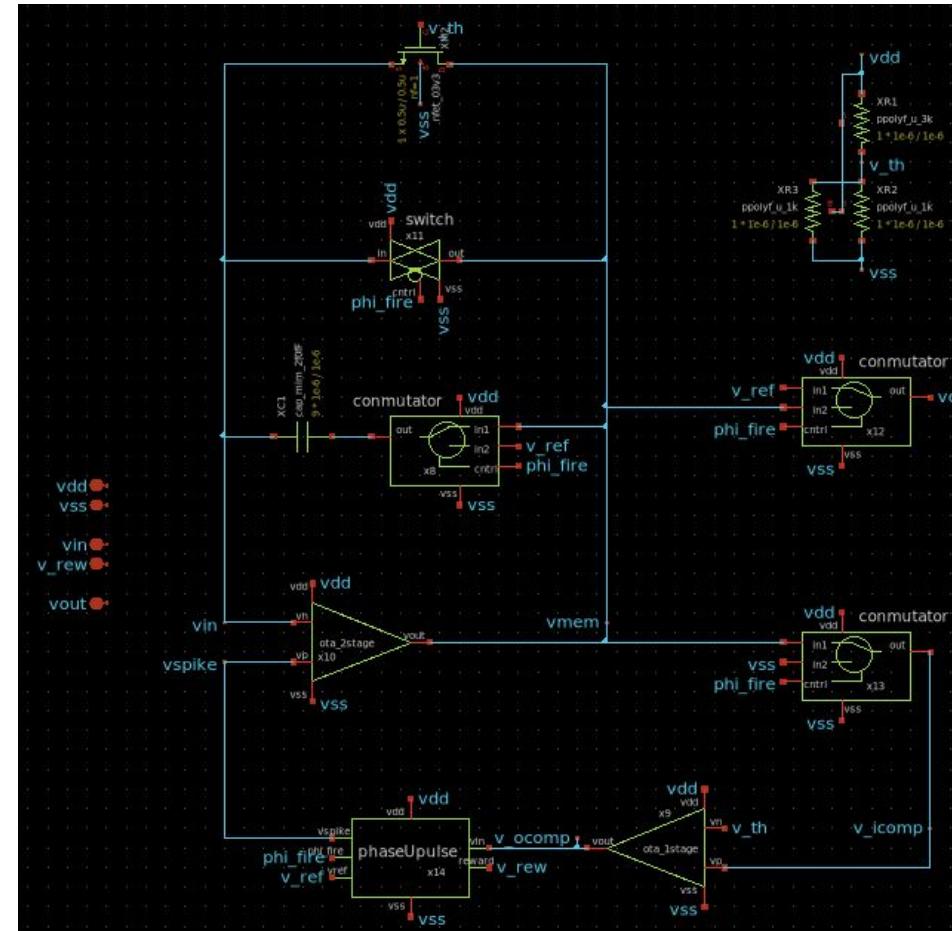
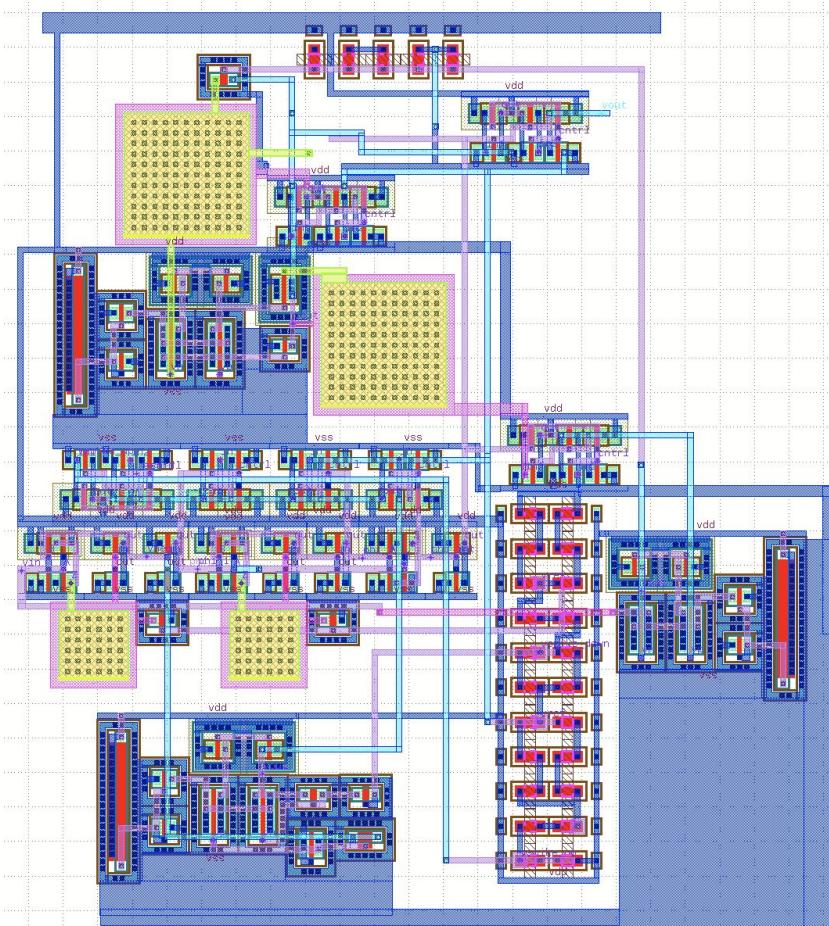
M13: SpikCore

PEX vs Schematic simulation LIF neuron (ring oscillator)



M13: SpikCore

LIF neuron (comparator)



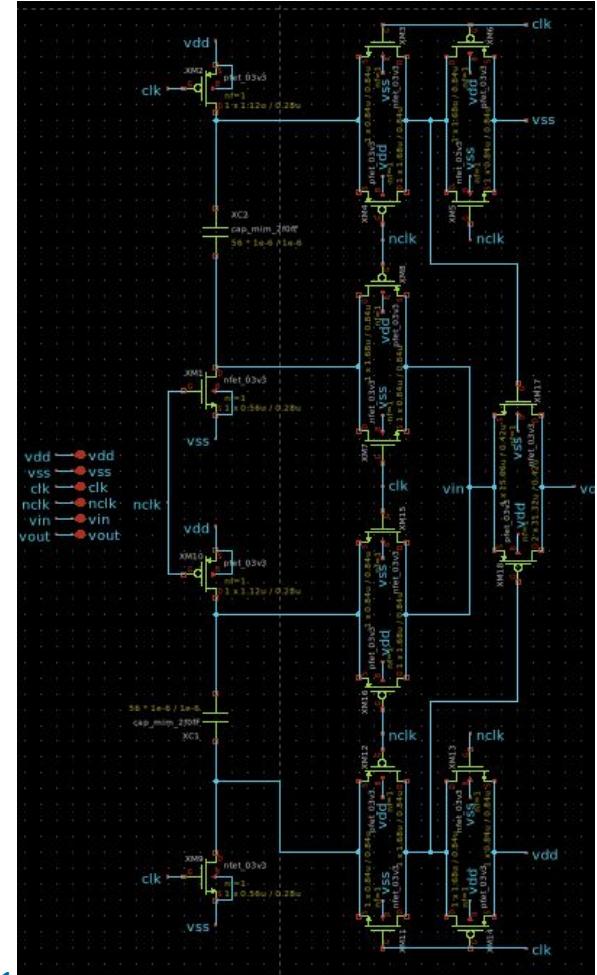
DRC clean, LVS shows a mismatch between schematic and layout even on single elements that were already verified

example not gate with 4 vs 3 netlist

Layout size: 60.725 um x 67.565 um

M13: SpikCore

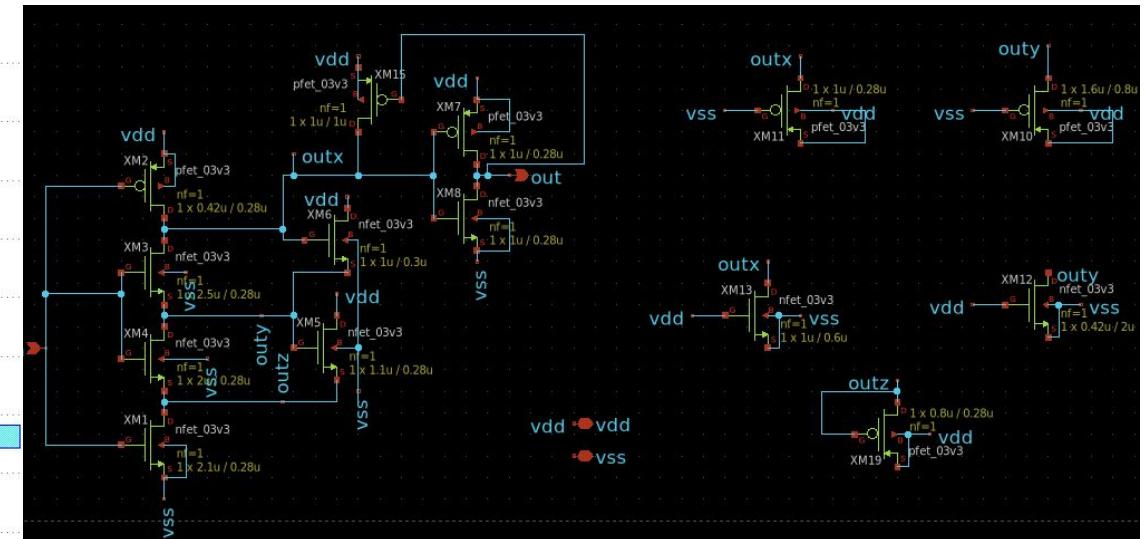
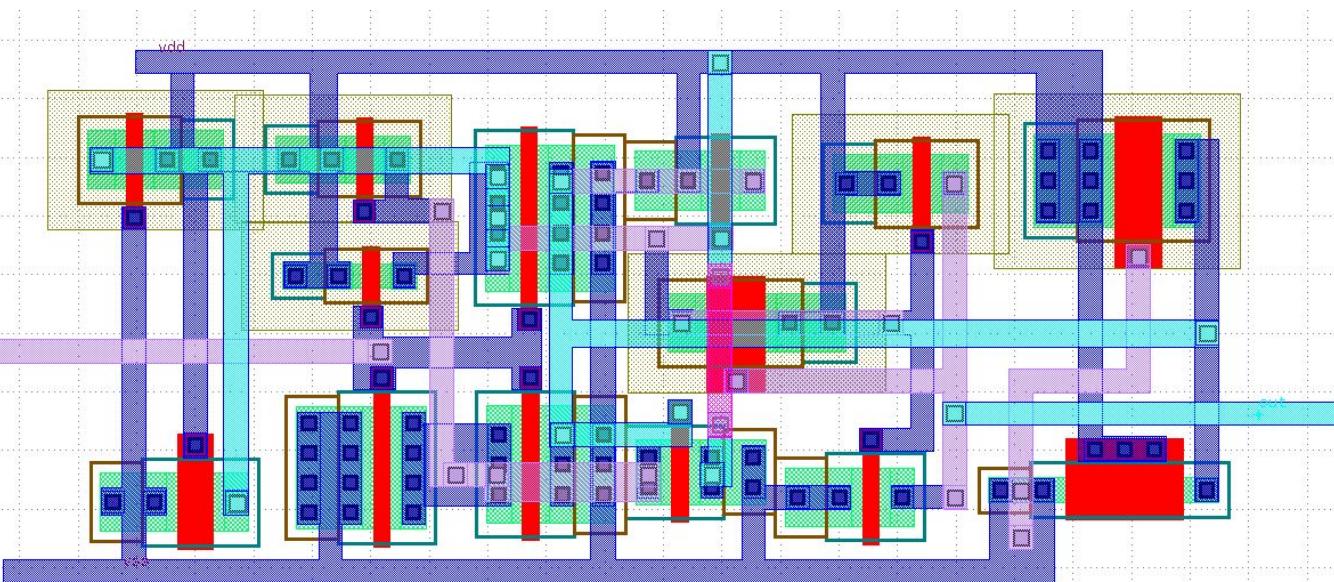
Bootstrapped transmission gate



Layout size: pending

M13: SpikCore

Schmitt Trigger

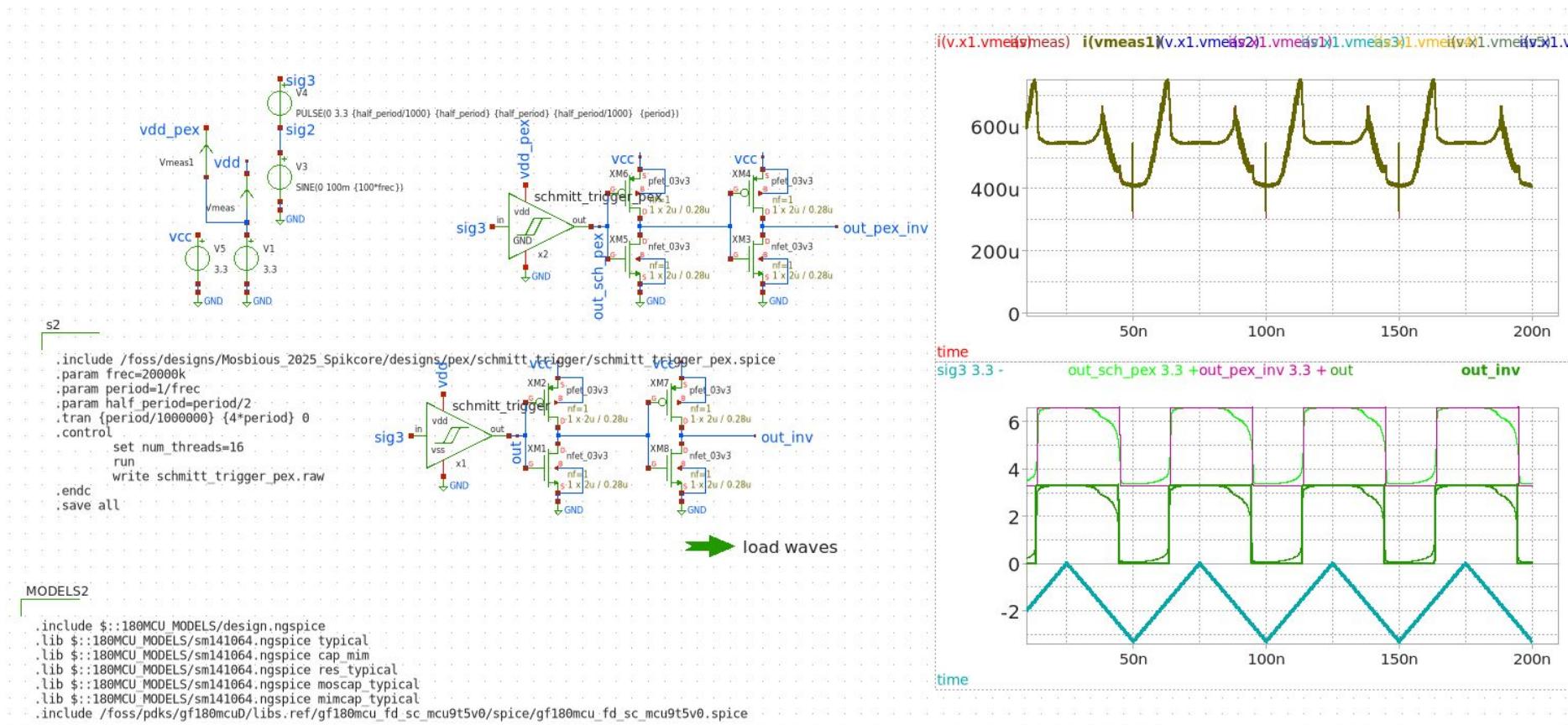


DRC and LVS clean

Layout size: 21.495 um x 9.315 um

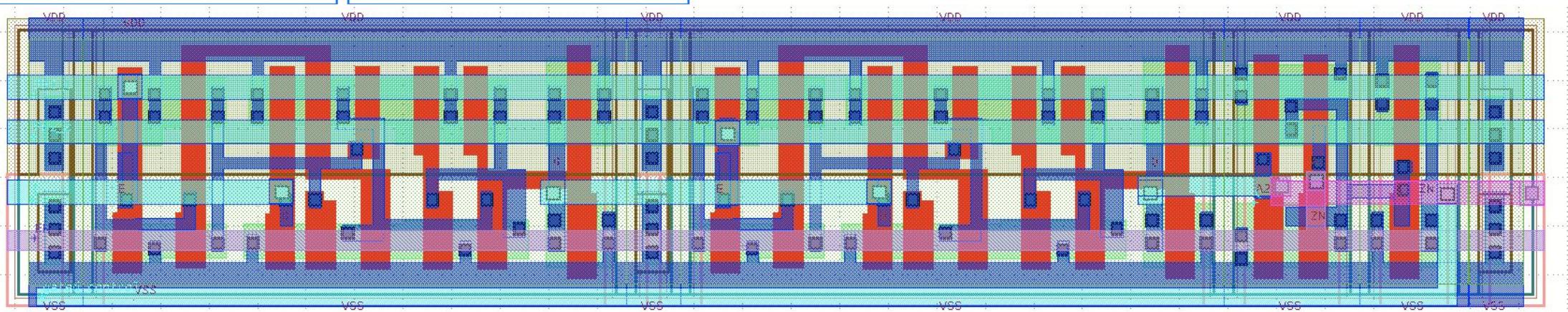
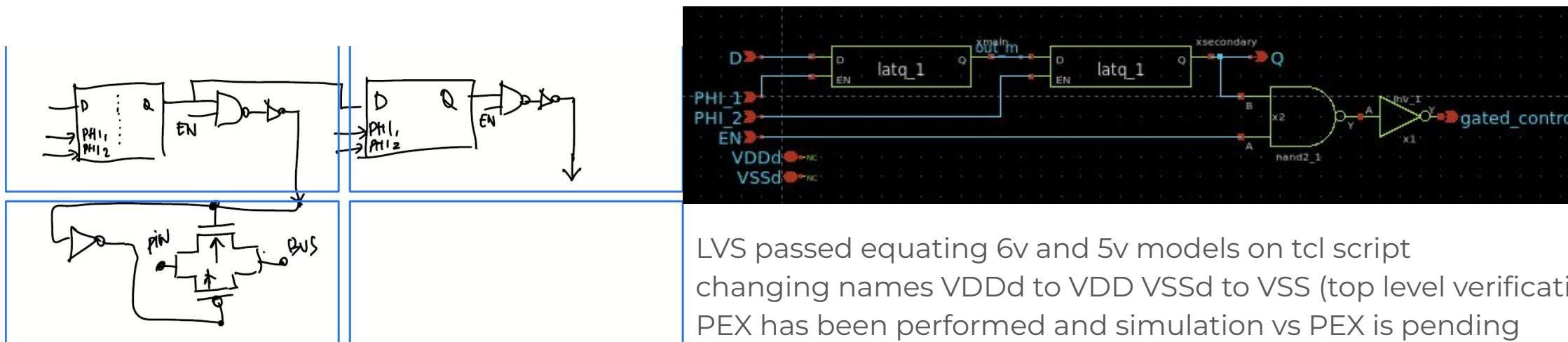
M13: SpikCore

PEX vs Schematic simulation Schmitt Trigger



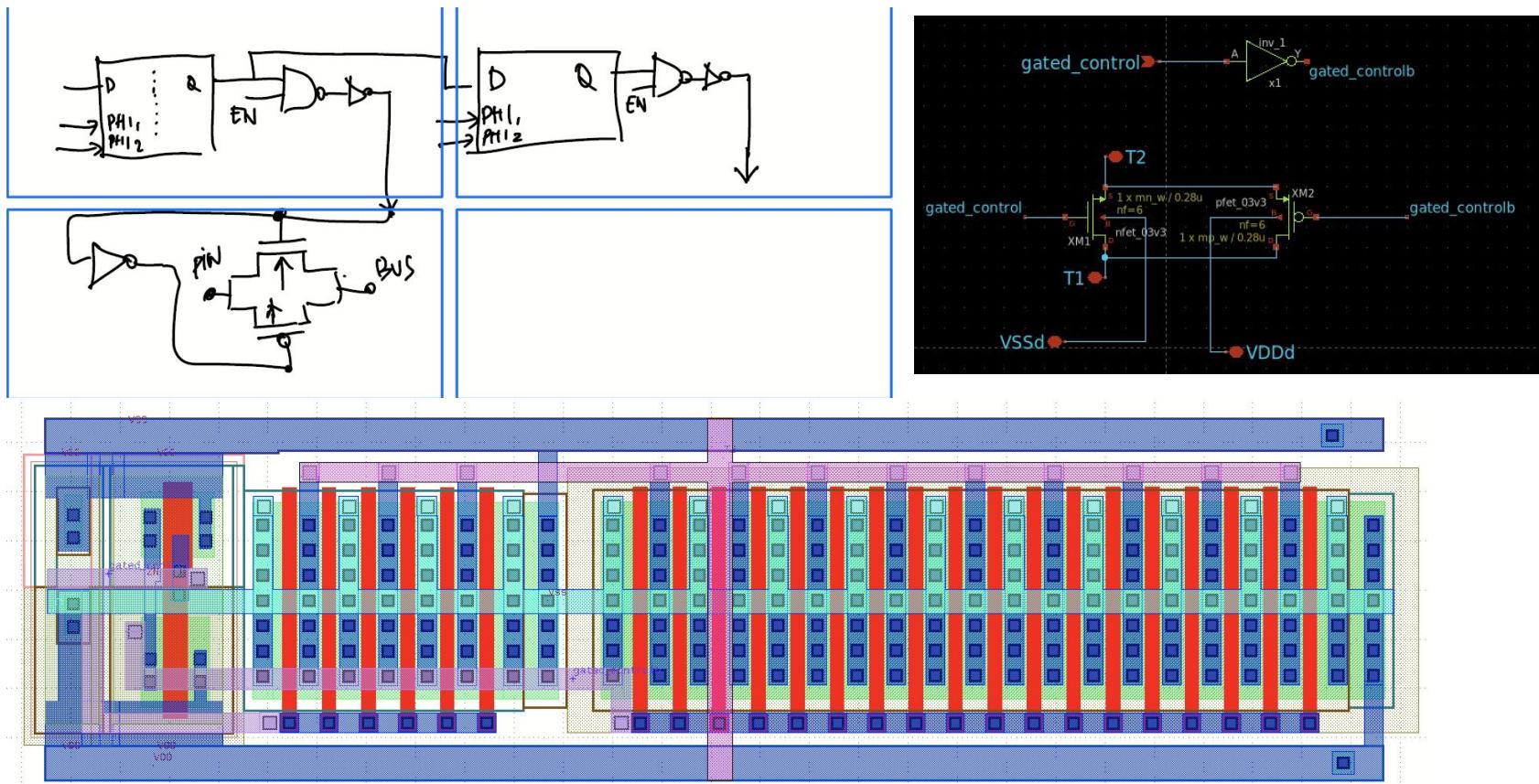
M13: SpikCore

D type Flip Flop and TG for switch matrix



M13: SpikCore

D type Flip Flop and TG for switch matrix



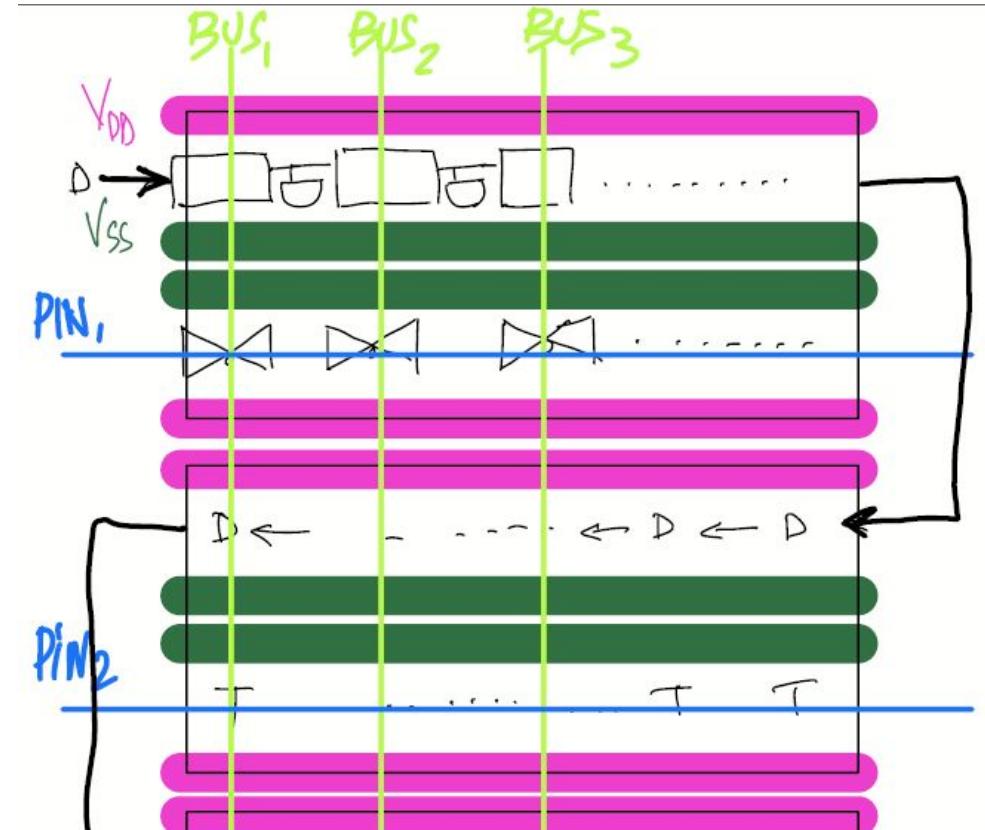
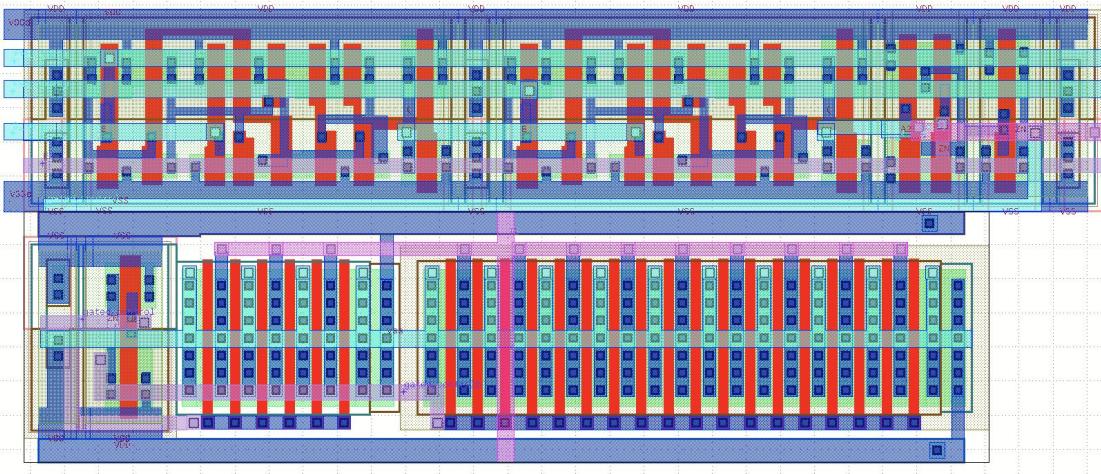
Changing names VDDd to VDD
VSSd to VSS (top level verification)

The LVS check failed when using the parameter .param mn_w=24u. However, the LVS passed after this value was hard-coded directly on the device.

PEX has been performed and simulation vs PEX is pending

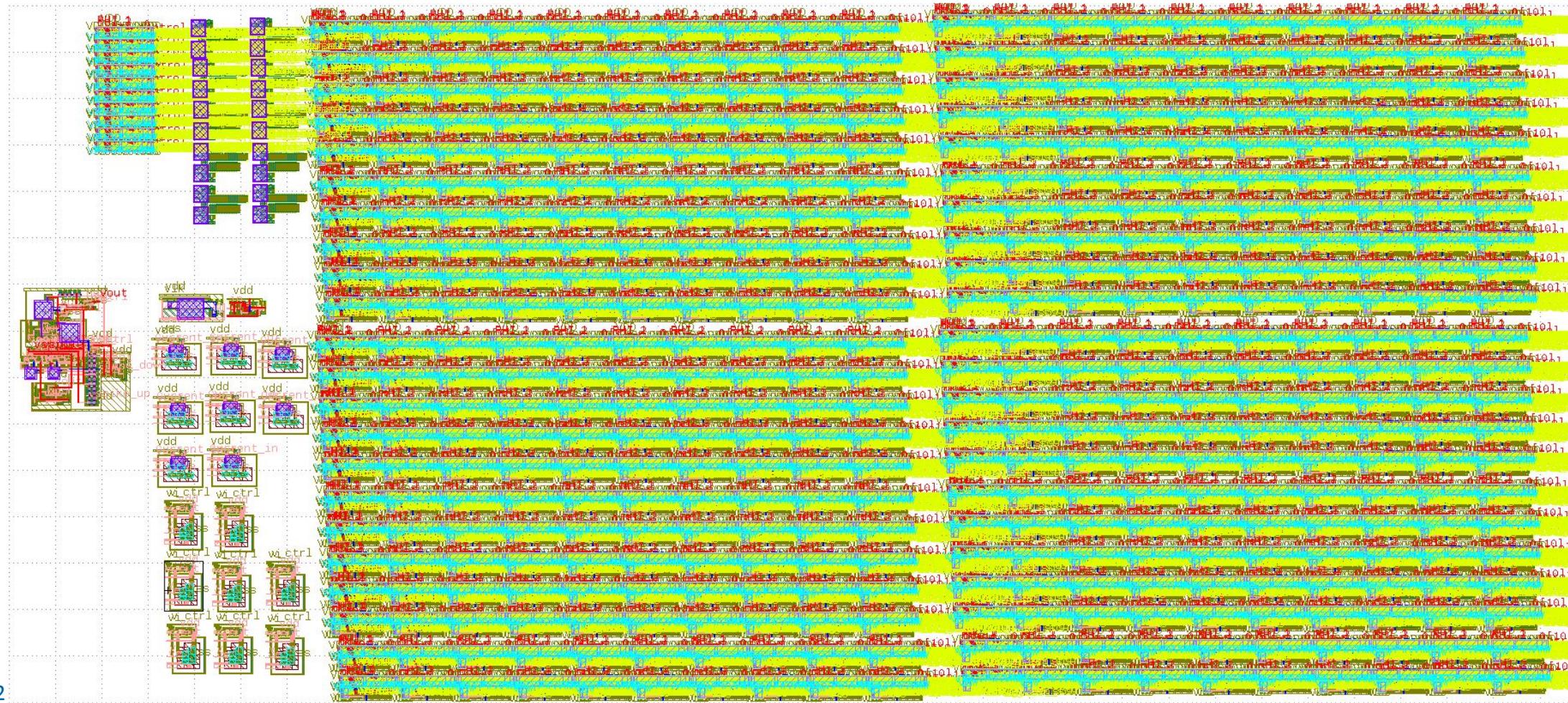
M13: SpikCore

Switch matrix



M13: SpikCore

Top level



M13: SpikCore

Open issues

Final switch matrix layout is pending.

The building blocks for the switch matrix are available, using “equate” on models

The new update from Tim edwards for the 3.3V Standard cells could help us to unify the design layout (3.3V and 5v/6v well can't be connected together) and reduce the size [missing latq_1 std 3.3v cell]

PAD simulations are performed one at a time, due to RAM consumption and a bottleneck in multithreading, as only 8 or 2 threads are used at a time, despite having 24 threads available.

Depending on the simulation ngspice utilized all available threads or down to 1 possibly memory bottleneck ?

PEX model -> output PAD ✓
(similar performance to PEX simulation)

input PAD -> PEX model ->
output PAD ✗
(number of threads decreases and simulation time and response changes)