Make a chip proposal

June de 2025

Functionality

The chip proposal will contain the building blocks for spiking neurons and analog synapses, a reconfiguration on the hardware side will allow to test different neurons behaviour (and possibly different neuron models like LIF, AH, etc.) and the modification of this neurons with excitatory and inhibitory synapses (rather than designing different neurons for excitatory and inhibitory behaviour the synapses modify the beheviour of said neurons simplifying the testing and reconfiguration).

Specs

1. 6 inverters, 3 pairs with 2 and 4 sizes
2. one-stage, nMOS-input, load-compensated OTA
3. one-stage, pMOS-input, load-compensated OTA
4. current mirrors (pMOS and nMOS) with 1, 2, 4, 8 designs
5. 4 synapses (inhibitory or excitatory with the use of differential pairs)

Block diagram

Figure 1 presents a flow diagram outlining the proposed configuration process for analog neurons. The process begins with the definition of a coding architecture, similar to frameworks like Keras or TensorFlow. This architecture specifies the connections between neurons, the active states of neurons, and the behavior of the synapses (excitatory or inhibitory).

Next, this coding architecture is translated into a register-based format that can be uploaded to the registers (flip-flops) via serial communication, using the Raspberry Pi Pico. These registers are responsible for configuring the active states of the neurons and the synaptic behavior.

Finally, data from the crossbar array of the mosbiou chip is transmitted. This data establishes the internal connections between neurons and synapses. The final step in the process involves running inference tasks on the configured network.

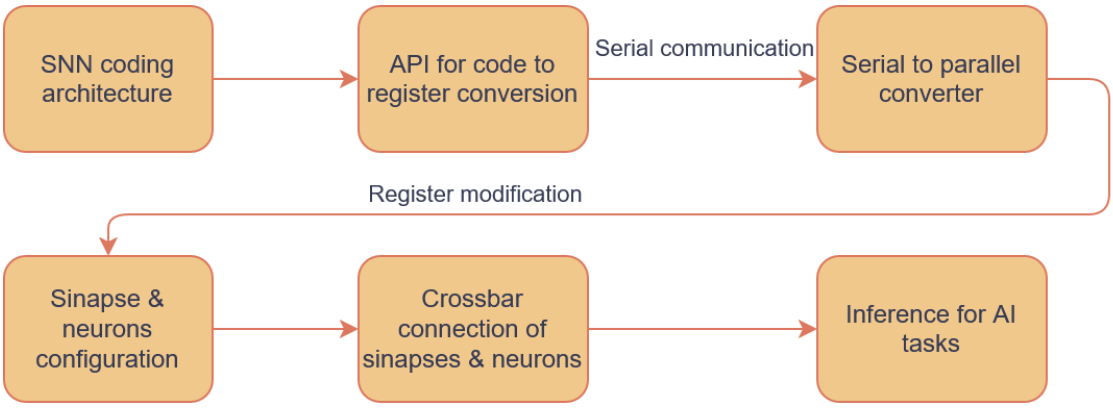

Figure 1. Block diagram of the flow process from coding the structure of neural networks to the inference stage.

Figure 2. Shows the use of registers to configure the state of the neurons and synapses.

- Neurons have one register responsible for the active state of the neurons.
- Synapses take two registers, the ASR (Active State Register) determines if the synapse is active or not; the EISR (Excitatory Inhibitory State Register) determines whether the synapse will source current, acting as an excitatory path, or sink current, acting as an inhibitory path.

Figure 3. shows the schematic for the axon-hillock artificial neuron on cmos technology, a working simulation with variable pulse width is already working on SKY130 PDK. This same architecture is expected to work on GF180 on the subthrehold region. The choice of the subthreshold region is intentional, as it improves power efficiency and allows for a smaller capacitor size relative to the overall design.

Figure 4. shows the schematic for the inhibitory/excitatory synapses, the building block for this synapse are a pMOS and nMOS current mirror, 2 inverters, and pMOS and nMOS voltage followers

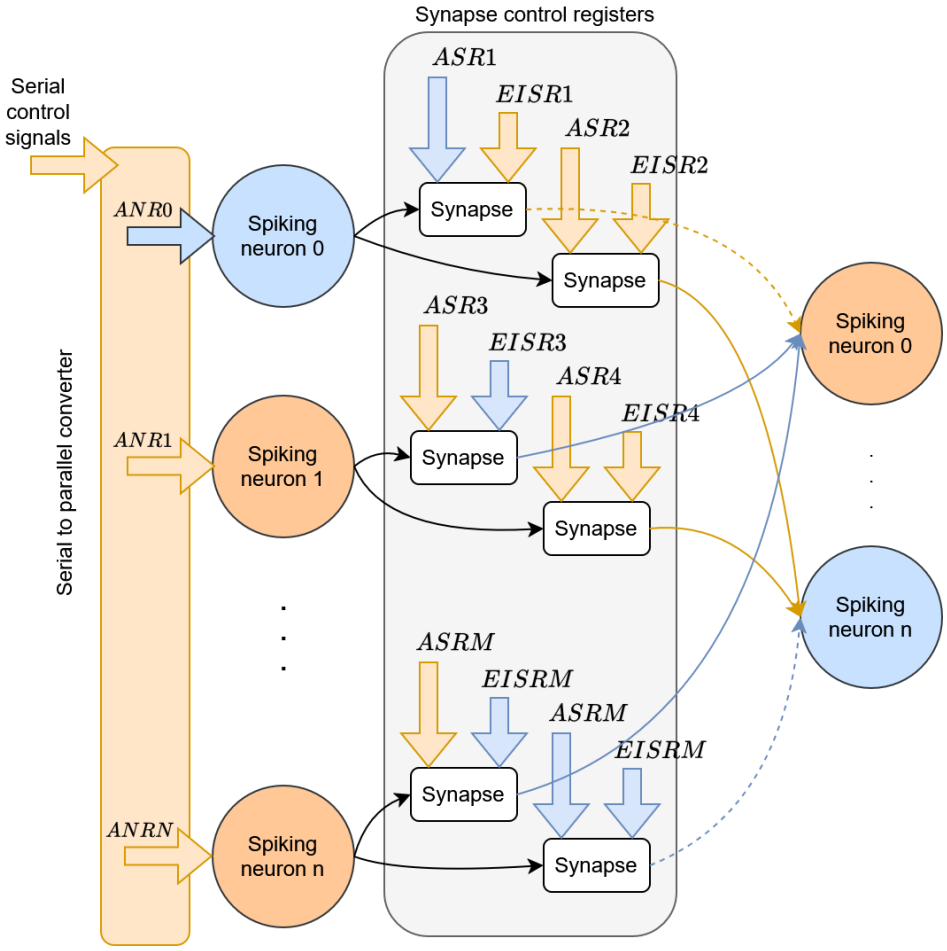

Figure 2. Use of registers for configurations of the behaviour of the synapses and neurons.

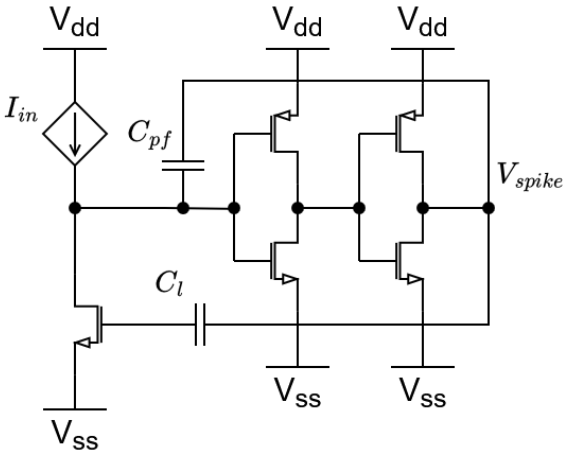

Figure 3. Schematic for the AH neuron model.

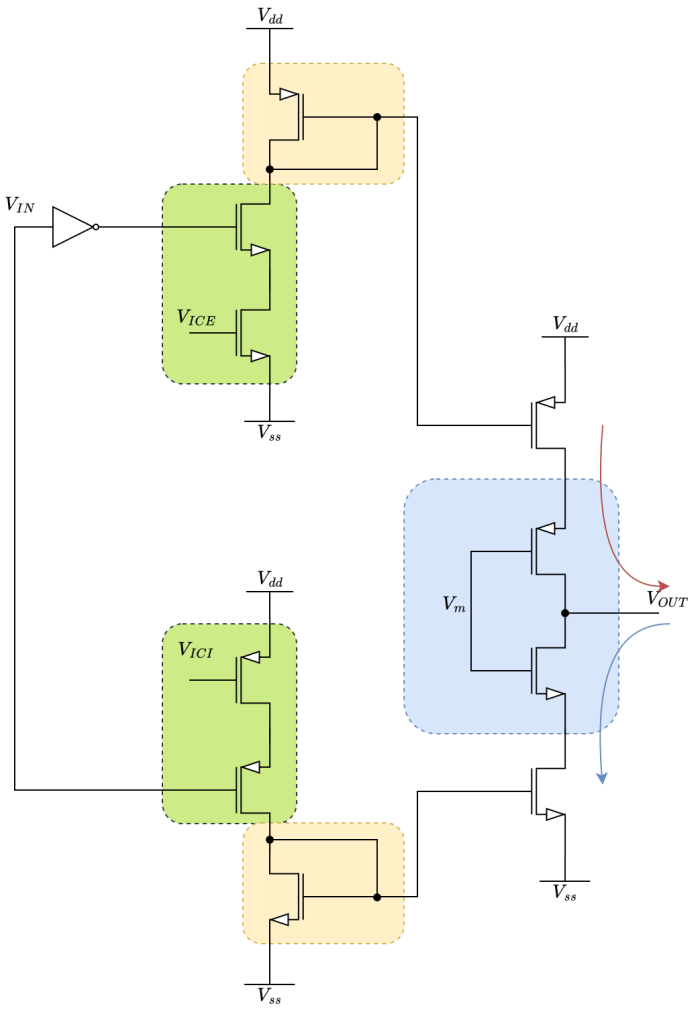

Figure 4. Schematic for the excitatory and inhibitory synapses

Pin-out

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Team members

- Royce Richmond
- asdasd
- asdasd

Schedule

Week 28

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Week 29

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Week 30

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Week 31

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Week 32

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Week 40

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