Team SpikCore

Chipathon 2025

Spiking Mosbius

Team members

- Royce Richmond
- Rosendo Valdés
- Oscar Islas

What is a spiking mosbius ? and why ?

What's the goal ?

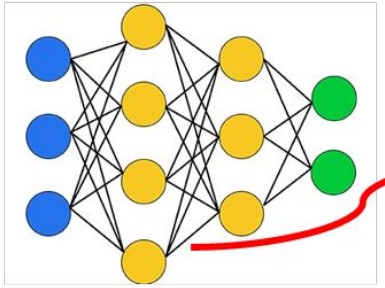
Develop a reconfigurable neuronal architecture leveraging a crossbar array topology, enabling experimentation with different neural networks configurations, input/output patterns, and domain-specific problem-solving.

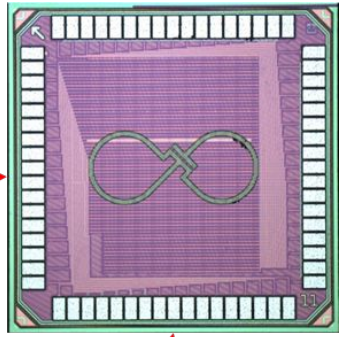
Why does it matters ?

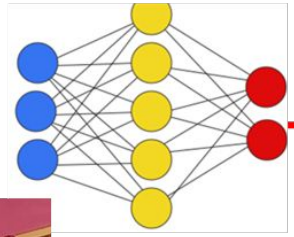
Neuromorphic hardware has the potential to solve computing problems with a fraction of the power consumption compared to digital counterparts. Being able to reconfigure a chip for different tasks, datasets, and outputs can help us develop specialized chips

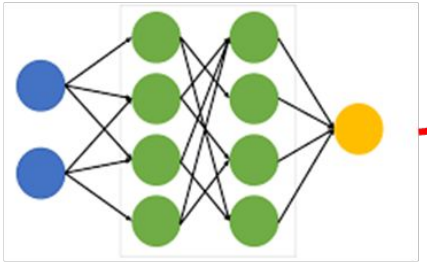
What is a spiking mosbius ? and why ?

We have unlimited power!! (kind of)



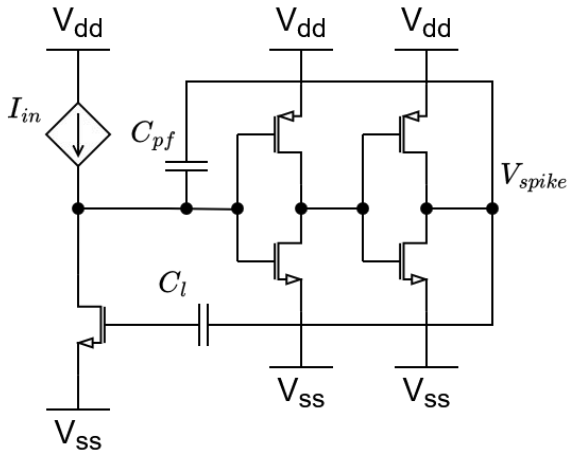






One neuron to rule them all - Axon Hillock neuron

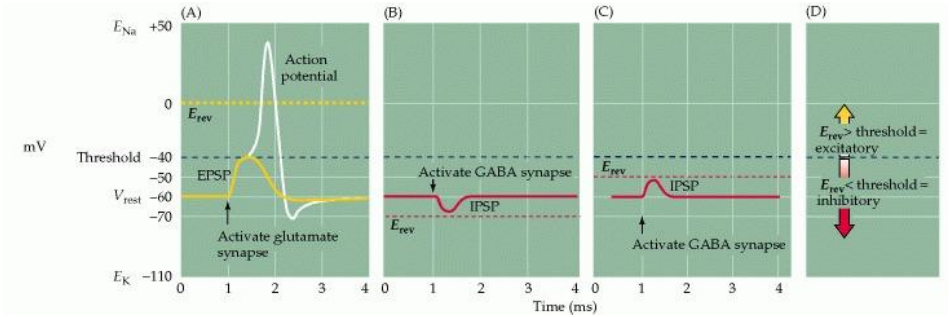
One of the very first VLSI implementations of neurons is the Axon Hillock neuron [1]. We propose a modification that emulates a floating gate and eliminates the membrane capacitance (reducing the layout size)



[1] Indiveri, G., Linares-Barranco, B., Hamilton, T. J., Schaik, A. van, Etienne-Cummings, R., Delbruck, T., Liu, S.-C., Dudek, P., Häfliger, P., Renaud, S., Schemmel, J., Cauwenberghs, G., Arthur, J., Hynna, K., Folowosele, F., Saighi, S., Serrano-Gotarredona, T., Wijekoon, J., Wang, Y., & Boahen, K. (2011). Neuromorphic Silicon Neuron Circuits. Frontiers in Neuroscience, 5. https://doi.org/10.3389/fnins.2011.00073

Excitatory inhibitory activity on the brain

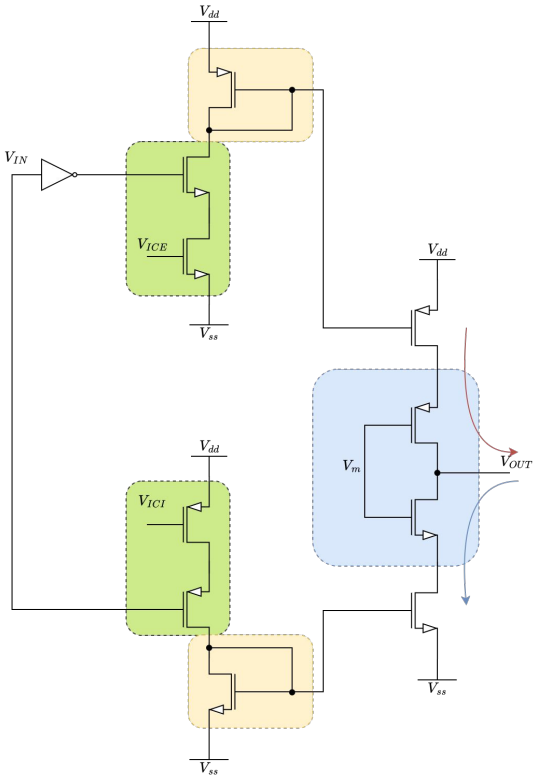
Neurons communicate through electrical currents called action potentials, which are either excitatory or inhibitory, the different input of the neurons allows the brain to learn different patterns [1].



[1] Purves D, Augustine GJ, Fitzpatrick D, et al., editors. Neuroscience. 2nd edition. Sunderland (MA): Sinauer Associates; 2001. Excitatory and Inhibitory Postsynaptic Potentials. Available from: https://www.ncbi.nlm.nih.gov/books/NBK11117/

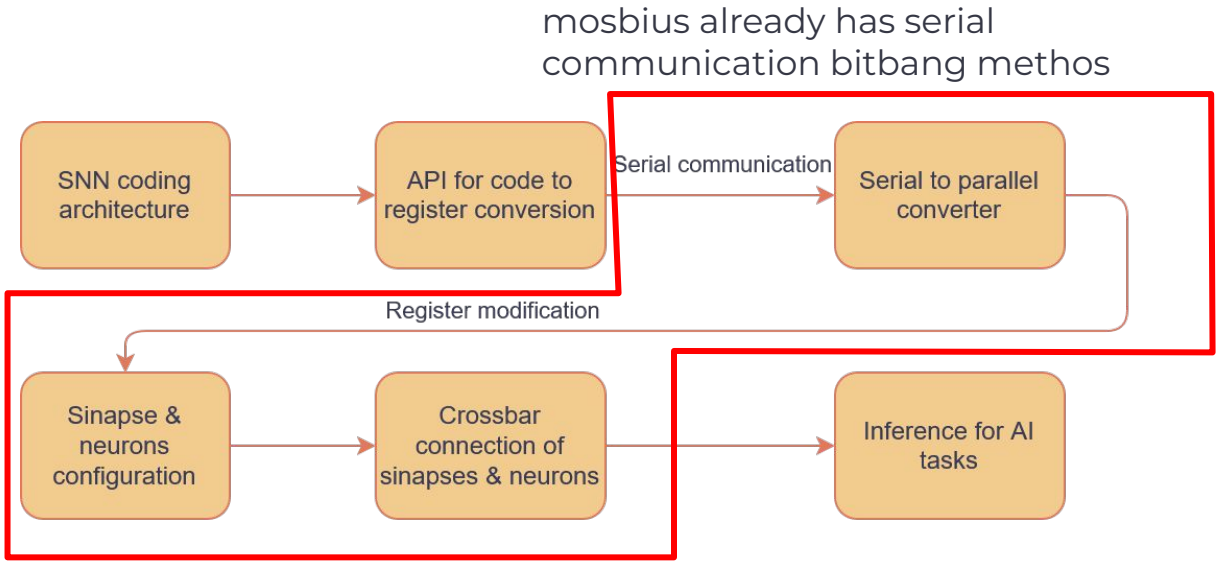
Excitatory inhibitory synapses

The goal is to simplify the building blocks by utilizing synapses that can function as either excitatory or inhibitory. This approach allows us to create diverse types of neurons without requiring distinct designs or specifications for each type.



from paper down to bitstream

We need a way to convert the idea (neural architecture to bitstream), we plan on a python script that will generate said bitstream



Optimizing the static power consumption

An important part of the power consumption on a chip is the static power, we can improve on this if we turn on the hardware necessary [2].

VDD is not static, utilizing inverters as demonstrated in [2] we have reduced static power consumption from 2.4e-8W to 1.8e-10W on the SKY130 pdk, we expect similar results on GF180 pdk

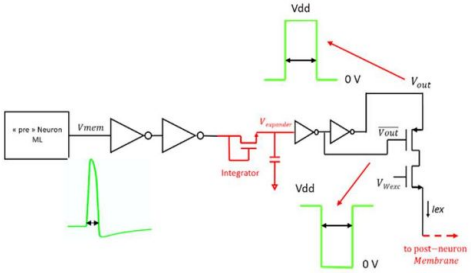


Fig. 7. Ultra low power synapses.

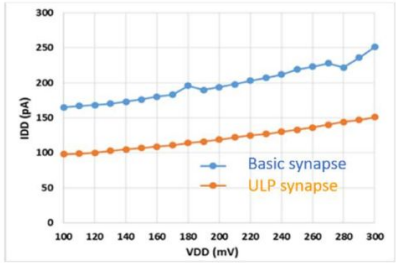


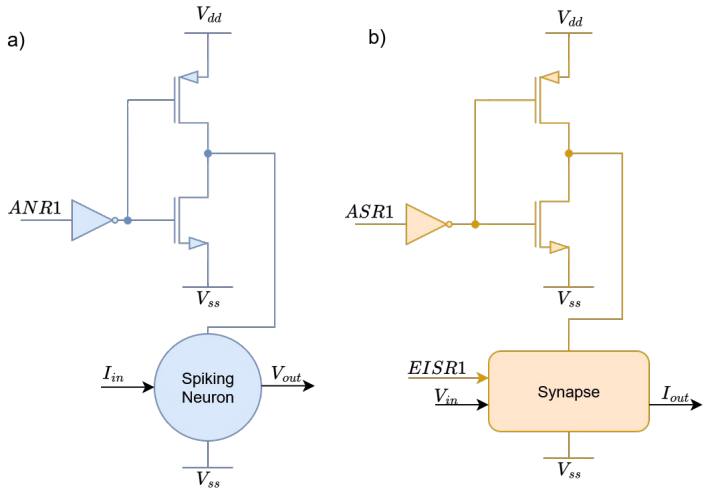
Fig. 8. Variations of the total current consumed by the SNN

[2] C. Loyez, K. Carpentier, I. Sourikopoulos and F. Danneville, "Subthreshold neuromorphic devices for Spiking Neural Networks applied to embedded A.I," 2021 19th IEEE International New Circuits and Systems Conference (NEWCAS), Toulon, France, 2021, pp. 1-4, doi: 10.1109/NEWCAS50681.2021.9462779. keywords: {MOSFET;Neuromorphics;Network topology;Neurons;Threshold voltage;Energy efficiency;Topology;Spiking Neural Network;subthreshold;energy efficiency},

Optimizing the static power consumption

Originally, a zig-zag configuration was considered; however, it is only feasible with deep-well technologies.

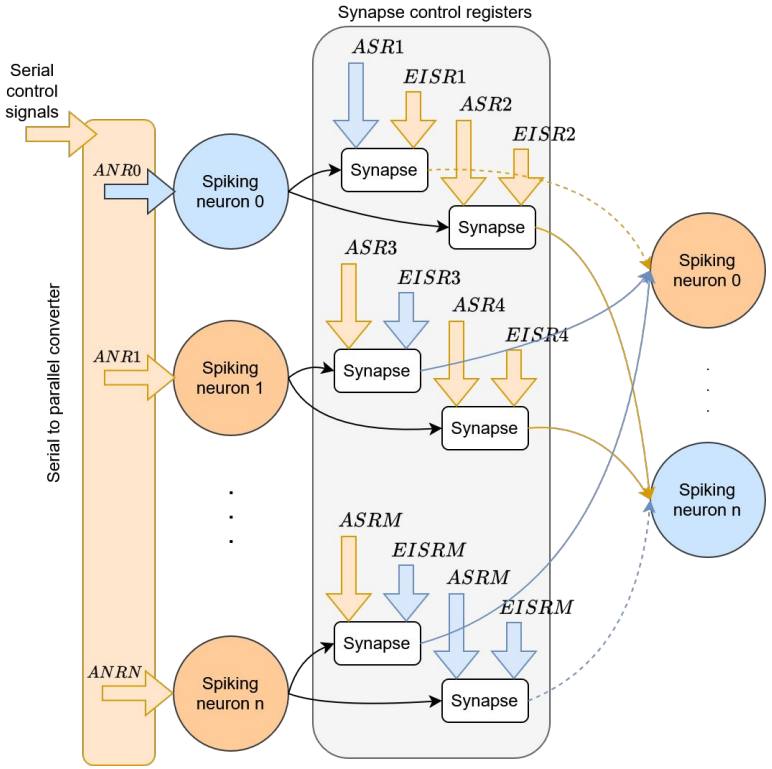
Alternatively, the use of inverters is a viable option on GF180, where a control signal will activate the cells.



Turn on only what you use

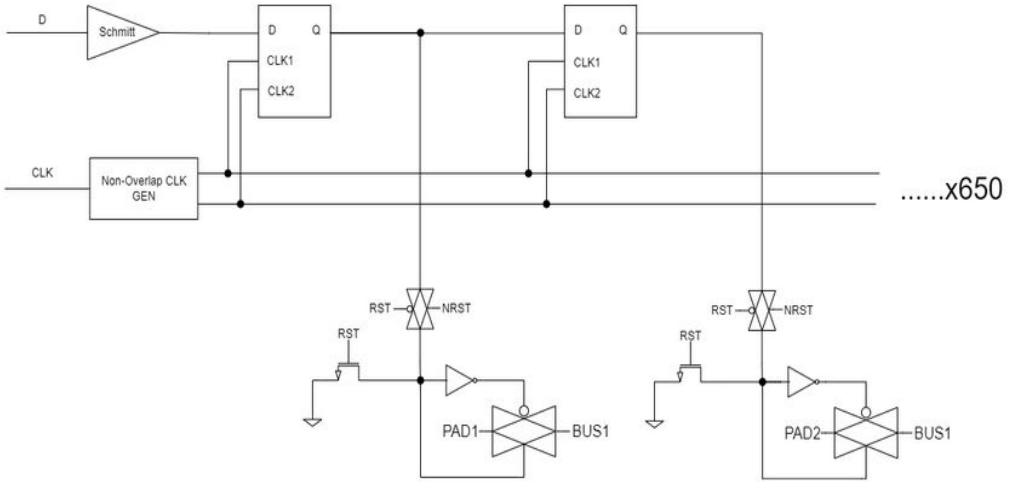
We can use a serial to parallel register to activate cells, this will give us control over active neurons and synapses.

The mosbius platform already requires said serial to parallel register

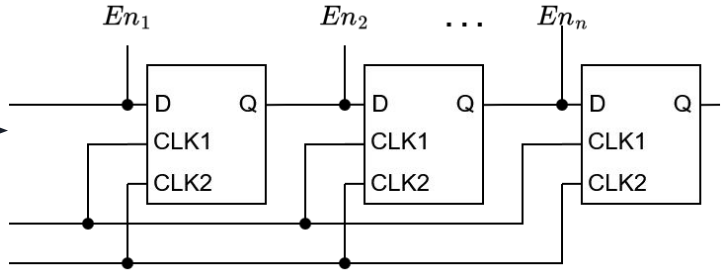


Expand the hardware and reutilize cells

Existing control path for mosbius



additional control path using an overflow



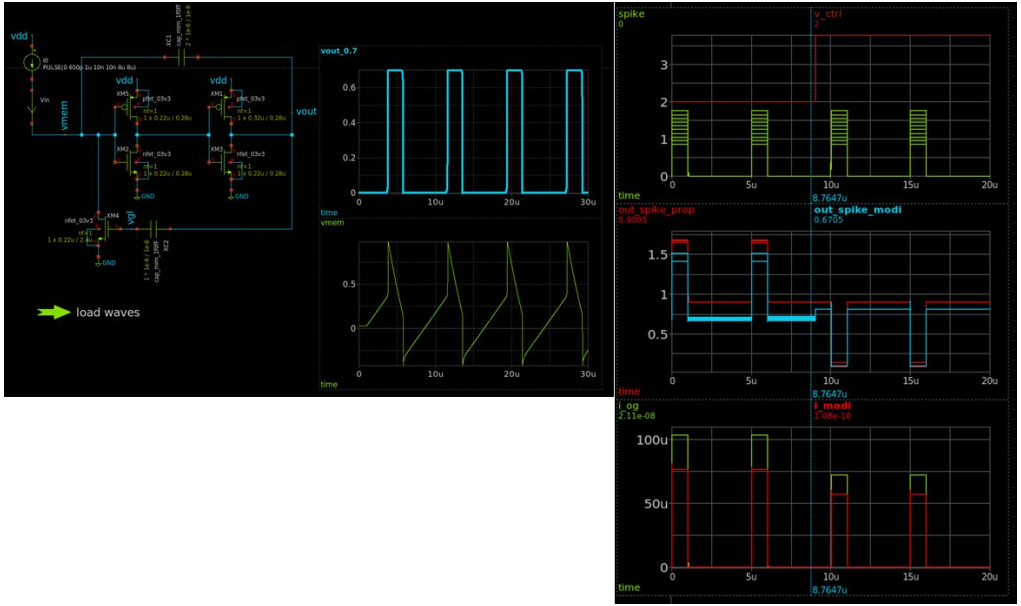
Expand the existing hardware

The current hardware for controlling the switch matrix already has D-type flip flops, non-overlapping clocks and a platform to upload the Bitstream File into the MOSbius Chip

Why create new hardware ? when we can expand the existing one and use the same programming platform (plus some tweaks) to turn on and off elements of our chip

What has been done ?

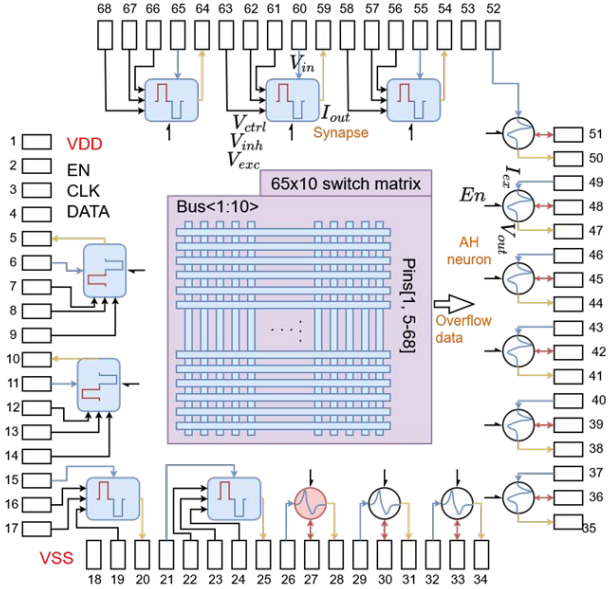
Simulation results on neurons, synapses and transmission gates



Mosbius Pinout

Pinout and characteristics:

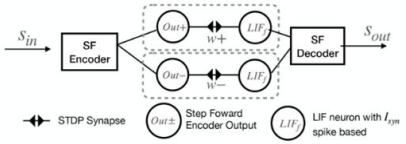
- 7 inhibitory/excitatory synapses
- 8 AH neuron subthreshold
- 1 LIF neuron
- 1 LIF neuron subthreshold

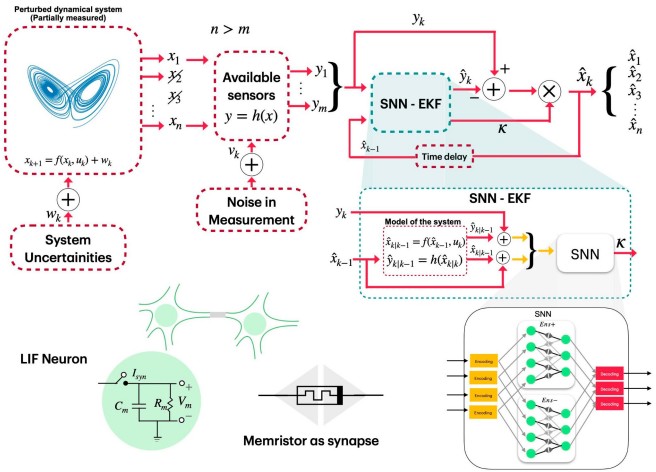


What are the potential applications of this technology?

We can utilize it for robotic applications as demonstrated in [3] it only requires 2 LIF neurons and 2 synapses in order to create a “PID control”

Filtering system could also be constructed, as demonstrated in [4]





[3] Juarez-Lora, A., Ponce-Ponce, V. H., Sossa, H., & Rubio-Espino, E. (2022). R-STDP Spiking Neural Network Architecture for Motion Control on a Changing Friction Joint Robotic Arm. Frontiers in Neurorobotics, 16. https://doi.org/10.3389/fnbot.2022.904017

[4] Juárez-Lora, A., García-Sebastián, L. M., Ponce-Ponce, V. H., Rubio-Espino, E., Molina-Lozano, H., & Sossa, H. (2022). Implementation of Kalman Filtering with Spiking Neural Networks. Sensors, 22(22), 8845. https://doi.org/10.3390/s22228845

Timeline

Week	Task	Responsable	Expected product
28	Project proposal review	All team members	Review proposal with posible updates and tweaks
29	Update and modification to proposal	All team members	Updated project proposal with observations
30	Schematic and symbol creation of neuron, synapse, TG, and read/write subsystem.	Royce Richmond Oscar Islas	Symbol and schematics of building blocks of the peripheral components of spiking mosbius
31	Simulation of TG and characterization	Rosendo Valdés Oscar Islas	Simulation and characteristics of TG
32	Simulation of neuron and synapse with TG (pending FF)	Royce Richmond	Simulation and characteristics of neurons and synapses
33	Top cell simulation	All team members	Top cell integration and simulation

Timeline

Week	Task	Responsable	Expected product
34	Layout of individual cells and post layout simulation	Rosendo Valdes Royce richmond	GDS and spice files
35	Layout of Cross-bar array and interconnects	Royce Richmond Oscar Islas	GDS and spice files
36	Integration of layouts (top cell) and post layout simulation	All team members	Final GDS file of the top cell
37	Layout review	All team members	Reviewed layout and possible annotations
38	Verification of top cell comparison pre vs post layout	Royce Richmond Rosendo valdes	Final layout ready for submission
39	Review process of submission and repository	Royce Richmond Rosendo valdes	Submission for manufacturing
40	Review of submitted file, simulations and data analysis	Oscar Islas	Report with incidents, improvements and results