2025 Chipathon 9th Weekly

Schematic Review

IEEE Solid-State Circuits Society

Technical Committee on the Open Source Ecosystem (TC-OSE)

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SSCS

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Advancing Technology for Humanity

M13: SpikCore

Team members:

- Royce Richmond
- Rosendo valdes
- Oscar Islas

What is SpikCore?

SpikCore is a MOSbius-style chip to demonstrate reconfigurable spiking neural networks with in-situ learning (external memristors from knowm)

Dimensions

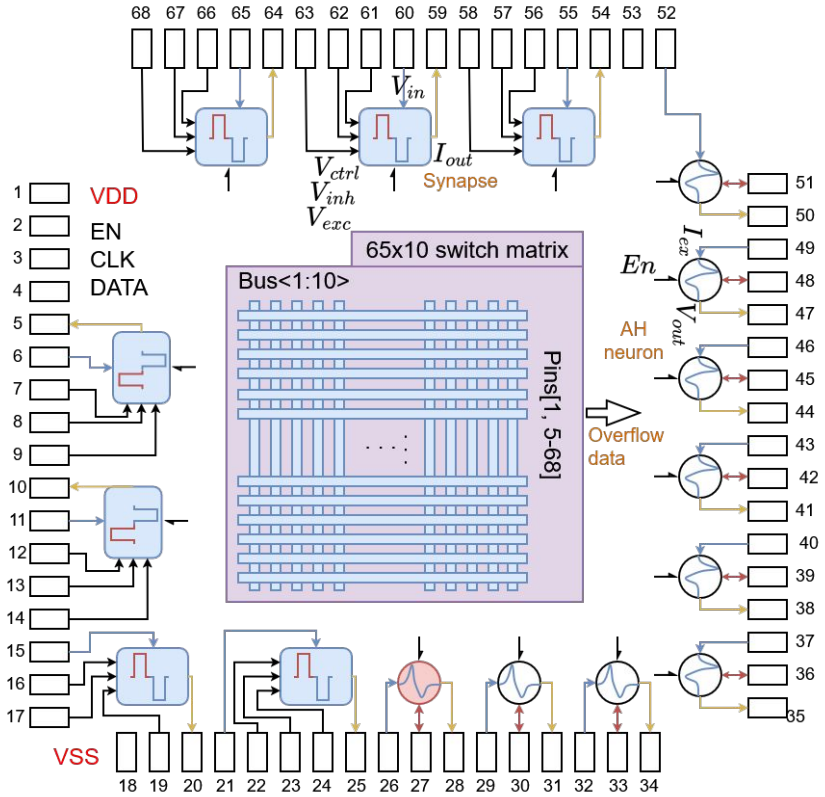
93.786um^2 + capacitor sizing

Pinout

63 pins: VDD,VSS, 7 digital inputs, 56 analog pins[16 analog outputs, 16 analog VDD (it can be reduces by sharing between similar cells), 24 analog inputs]

What do we have ?

- Inhibitory/excitatory synapse (sch, sym and tb)
- AH neuron subthreshold (sch, sym and tb)
- LIF neuron (ring oscillator) (sch, sym and tb)
- LIF neuron (comparator) (sch, sym and tb) missing one block
- TG bootstrap needs optimization for GF180



https://github.com/RoyceRichmond/Mosbious_2025_Spikcore

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Progress Summary

Progress summary — 0/13 completadas

Design	Schematic design Status	Schematic simulation Status	Layout Status	Post-layout simulation Status
AH neuron (subthreshold)	100%	100%	0%	0%
LIF neuron (ring oscillator)	100%	100%	0%	0%
LIF neuron (comparator)	75%	50%	0%	0%
Synapse	100%	100%	0%	0%
Transmission Gate synchronous	0%	0%	0%	0%
Transmission Gate asynchronous	75%	75%	0%	0%
D type Flip Flop (DFF)	100%	100%	50%	0%
DFF & transmission Gates	0%	0%	0%	0%
Crossbar array	0%	0%	0%	0%
	0%	0%	0%	0%
	0%	0%	0%	0%
	0%	0%	0%	0%
	0%	0%	0%	0%

Week-by-week schedule

Tasks — 2/13 completadas

Week	Task	Status	Responsable	Expected product
~~28~~	~~Project proposal review~~	~~Complete~~	~~All team members~~	~~Review proposal with posible updates and tweaks~~
~~29~~	~~Update and modification to proposal~~	~~Complete~~	~~All team members~~	~~Updated project proposal with observations~~
30	Schematic and symbol creation of neuron, synapse, and TG	Work in progress	Royce Richmond Oscar Islas	Symbol and schematics of building blocks of the peripheral components of spiking mosbius
31	Simulation of TG and characterization	Work in progress	Rosendo Valdés Oscar Islas	Simulation and characteristics of TG
32	DFF layout	Work in progress	Royce Richmond	Simulation and characteristics of neurons and synapses
33	Simulation of neuron and synapse	Not started	All team members	Top cell integration and simulation
34	Top cell simulation	Not started	Rosendo Valdes Royce richmond	GDS and spice files
35	Layout of individual cells and post layout simulation	Not started	Royce Richmond Oscar Islas	GDS and spice files
36	Layout of Cross-bar array and interconnects	Not started	All team members	Final GDS file of the top cell
37	Integration of layouts (top cell) and post layout simulation	Not started	All team members	Reviewed layout and possible annotations
38	Layout review	Not started	Royce Richmond Rosendo valdes	Final layout ready for submission
39	Verification of top cell comparison pre vs post layout	Not started	Royce Richmond Rosendo valdes	Submission for manufacturing
40	Review process of submission and repository	Not started	Oscar Islas	Report with incidents, improvements and results
	Review of submitted file, simulations and data analysis			

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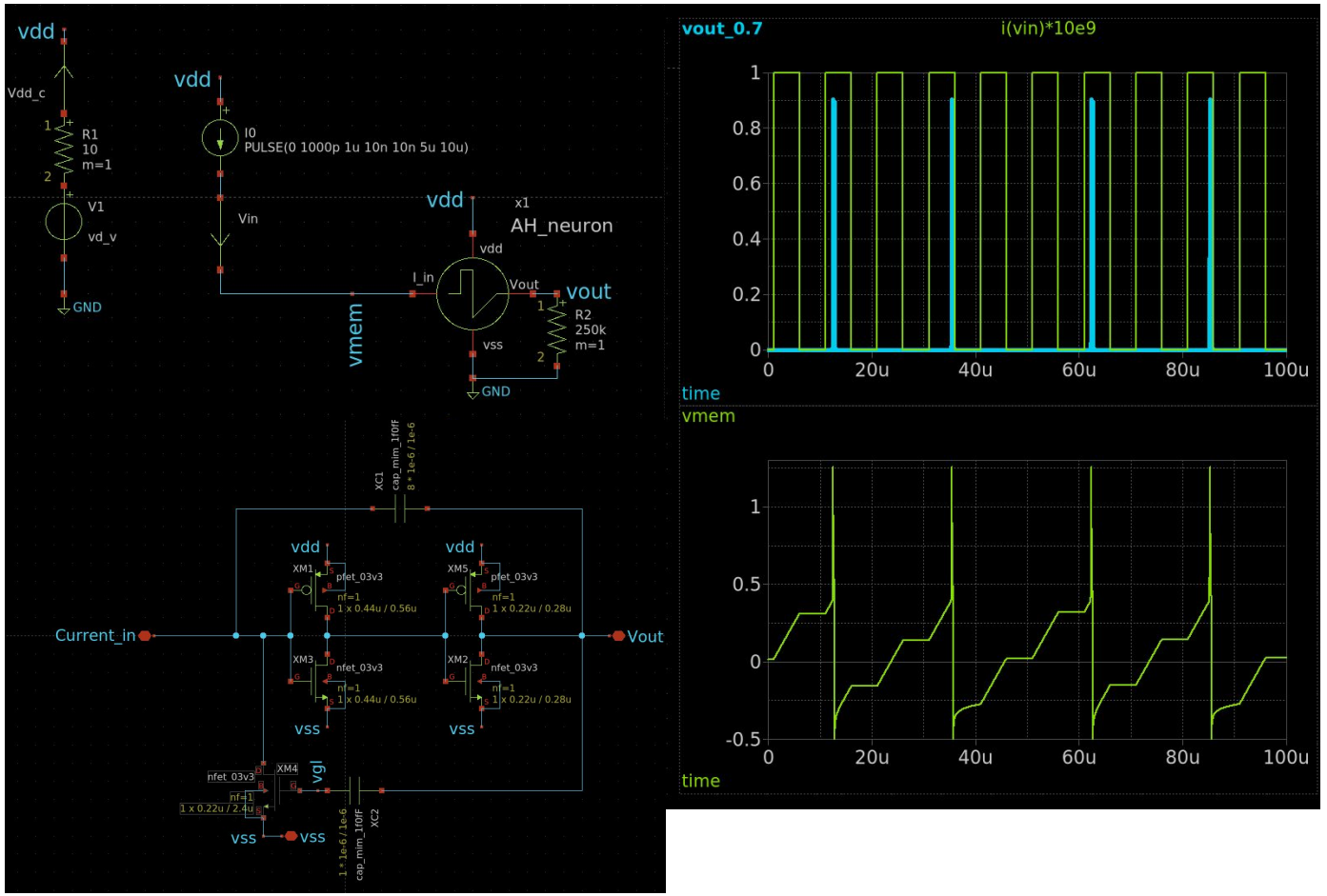
Axon Hillock (AH) Neuron



The Axon Hillock neuron was one of the first VLSI implementations for discrete events (spiking neurons) this neuron requires a relatively small footprint to operate and a small membrane capacitance.
The addition of a series capacitor to the reset/leakage NMOS reduces the firing frequency by dividing the charge of the output

approx size: 1.144 um^2 + 16um^2 capacitor

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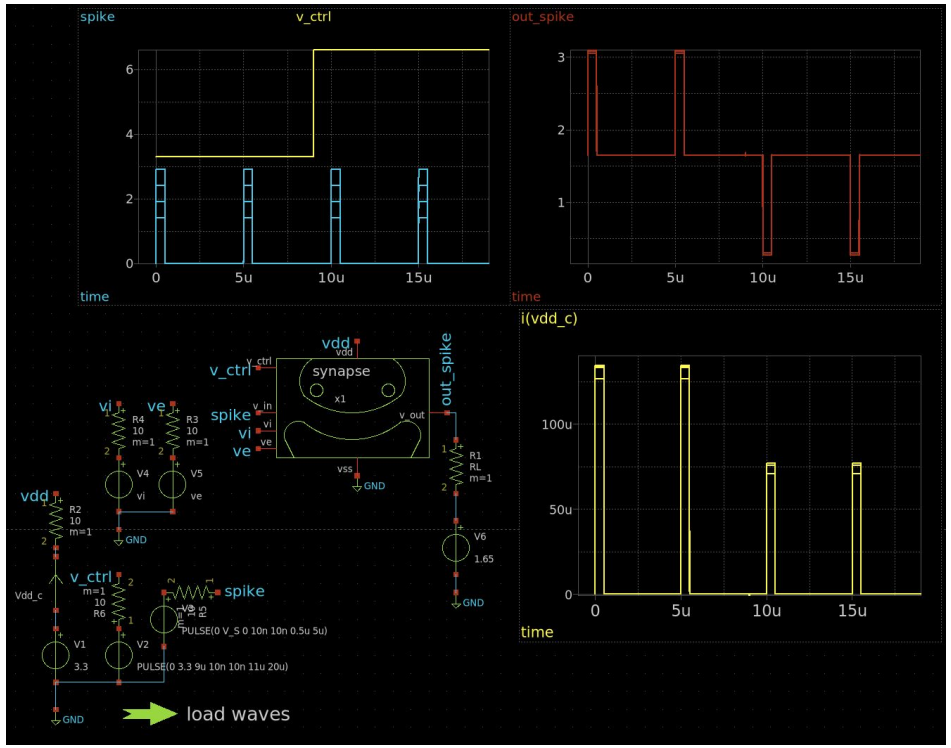
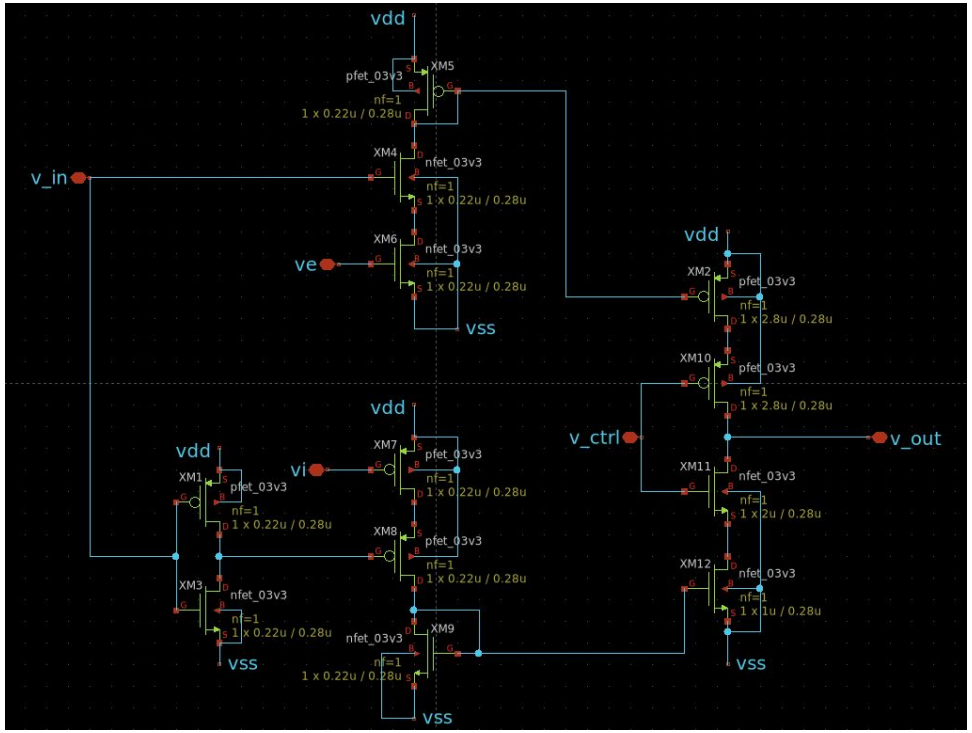
Inhibitory / Excitatory synapse



The synapse is capable of sourcing or sinking current to the next stage (neuron), thereby functioning as either an excitatory or inhibitory connection modifying the neuron's behaviour.

It can accept a wide input voltage range for incoming spikes (1.3 V to 3.3 V) and reshape them into a 3.3 V output.

approx size: 2.9 um^2



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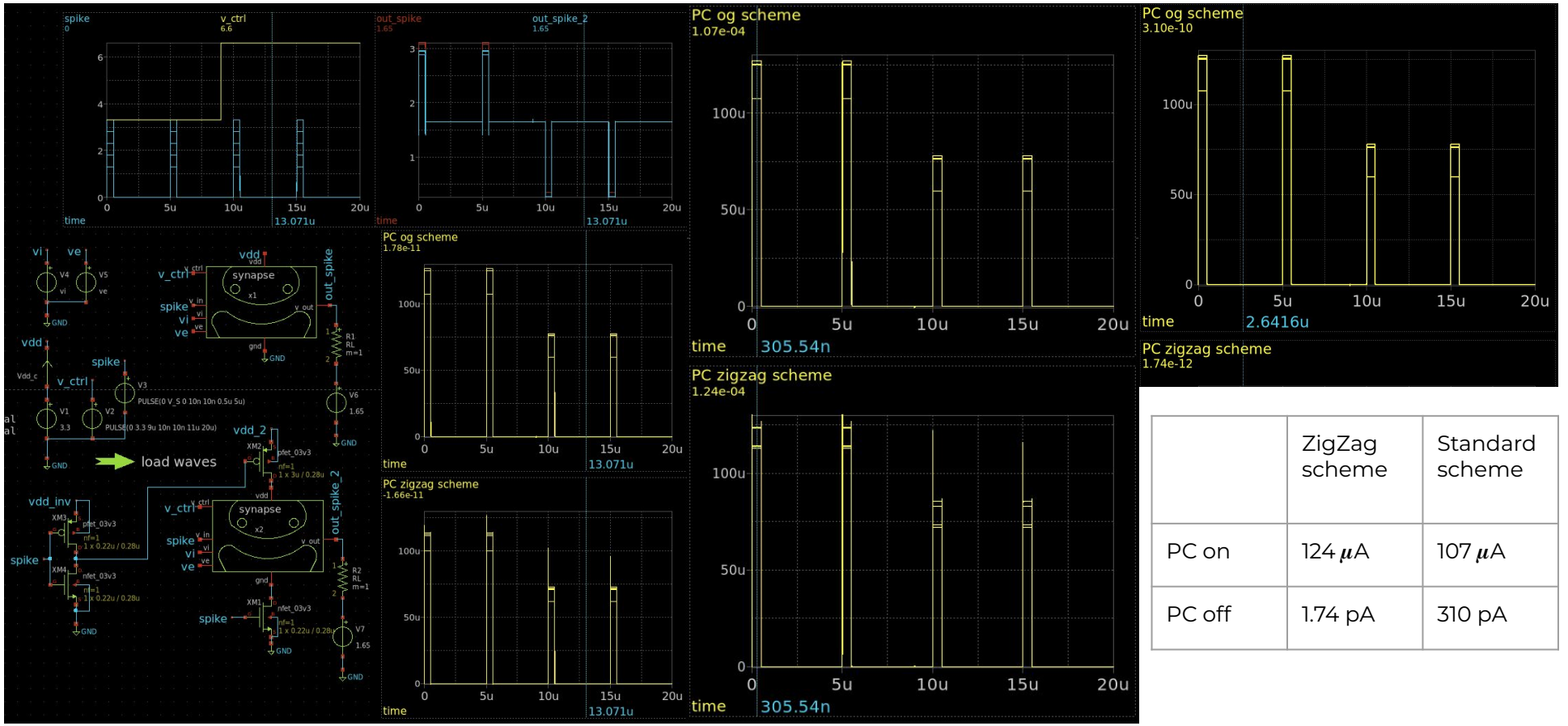
Inhibitory / Excitatory synapse with ZigZag power scheme



	ZigZag scheme	Standard scheme
PC on	124 μA	107 μA
PC off	1.74 pA	310 pA

The power consumption (PC) during operation increases by 15%, due to the addition of the inverter and control MOS.

In standby mode, the power consumption is reduced 178 times. This is particularly important for neuromorphic hardware, where neurons spend most of their time in standby mode. Therefore, implementing methods to minimize power consumption in standby is crucial for developing power-efficient platforms.

approx size ZigZag: 1.0248 um^2

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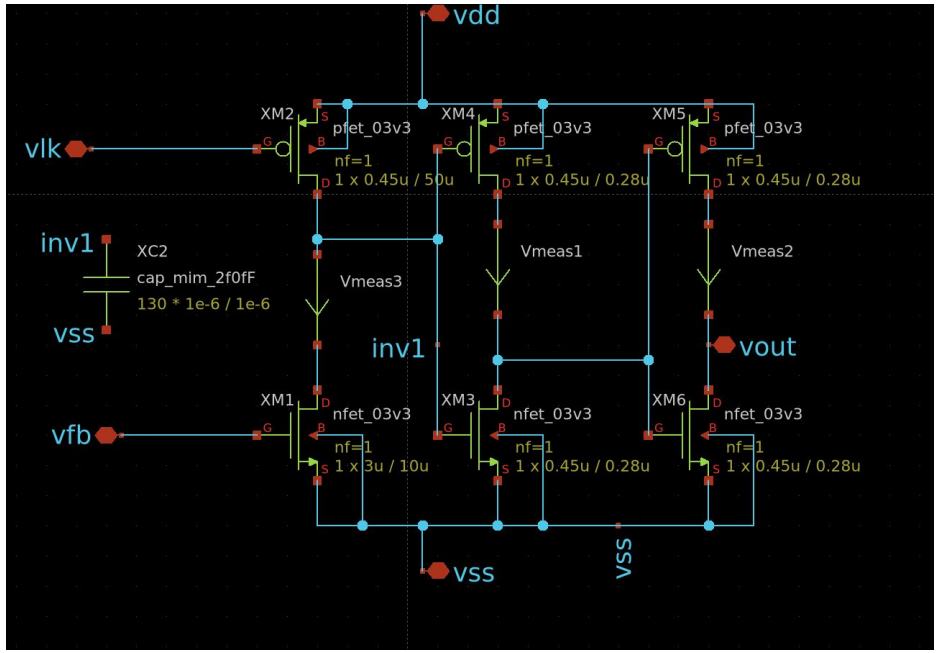
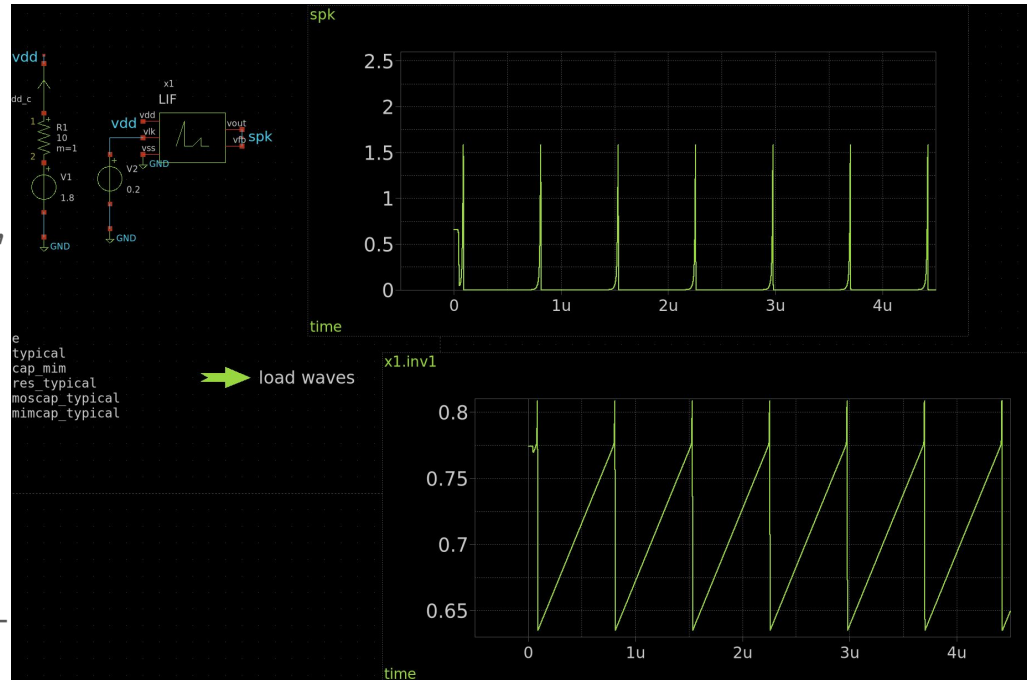
LIF neuron (ring oscillator)



The LIF neuron has the characteristic to backpropagate the spiking from other neurons on the network, and a controllable frequency via the XM2 PMOS which acts as the “leakage” current (if no current flows the neurons does not start spiking)

approx size: 65.478 um^2 + 130um^2 capacitor



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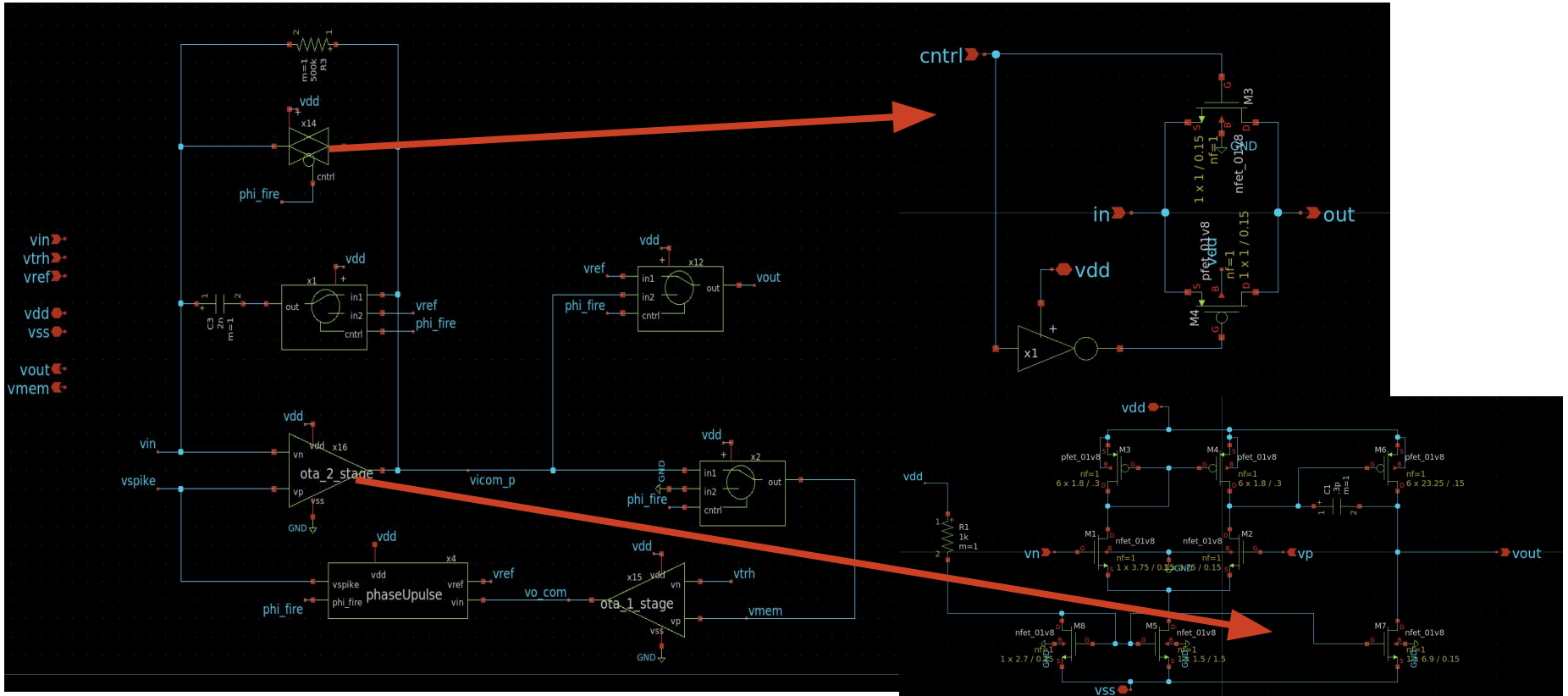
LIF neuron (comparator)



The LIF neuron (comparator) is an asynchronous neuron that can generate its own control signals, which are also tunable.

Additionally, this neuron includes a module called “PhaseUPulse” which generates output signals capable of driving memristors and enabling the network to learn using the STDP learning algorithm.

A CMOS Spiking Neuron for Brain-Inspired Neural Networks With Resistive Synapses and *In Situ* Learning

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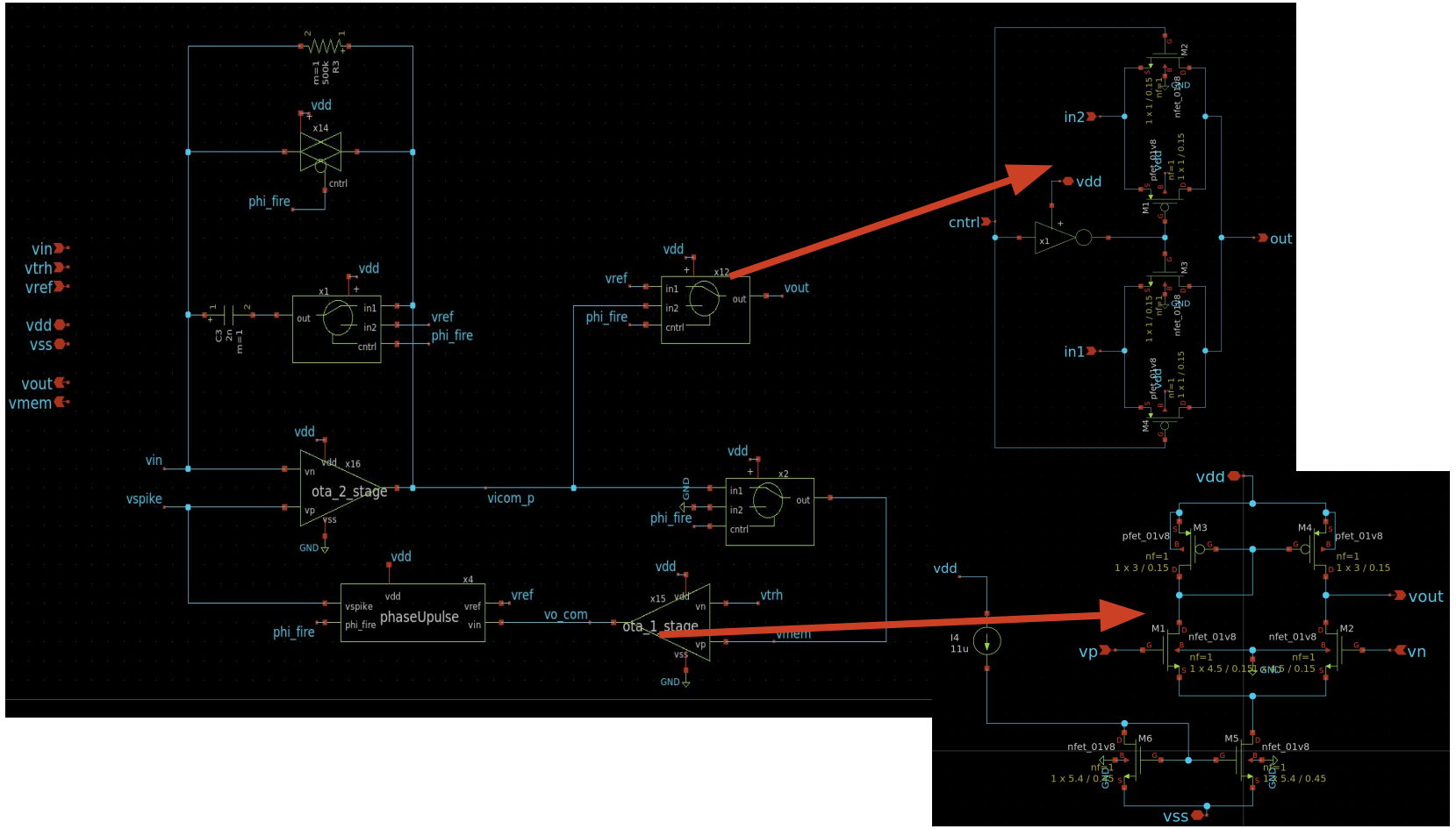
LIF neuron (comparator)



The design includes transmission gates (TGs), which can be repurposed for use in the switch matrix.

This design was developed with the intention of enabling its application in large-scale spiking neural networks, based on a previously validated implementation

https://www.mdpi.com/2227-7390/12/13/2025

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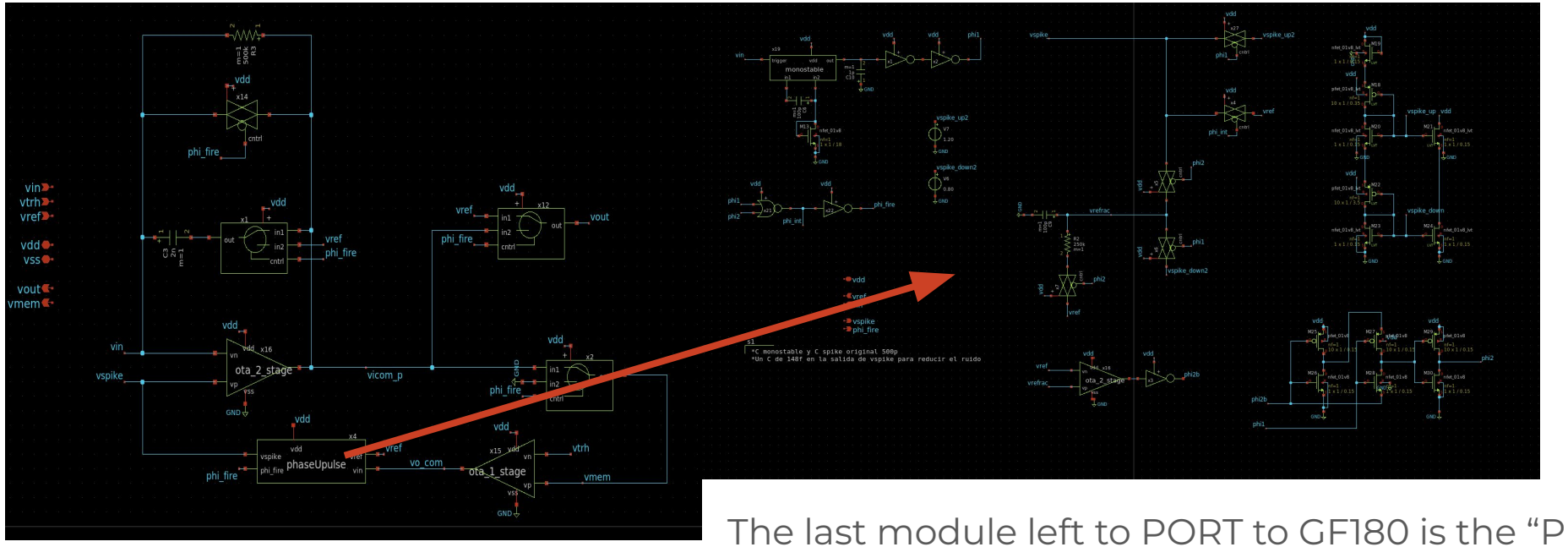
LIF neuron phaseUpulse needs port to GF180



The last module left to PORT to GF180 is the “PhaseUPulse” which controls the firing frequency, the output waveform.

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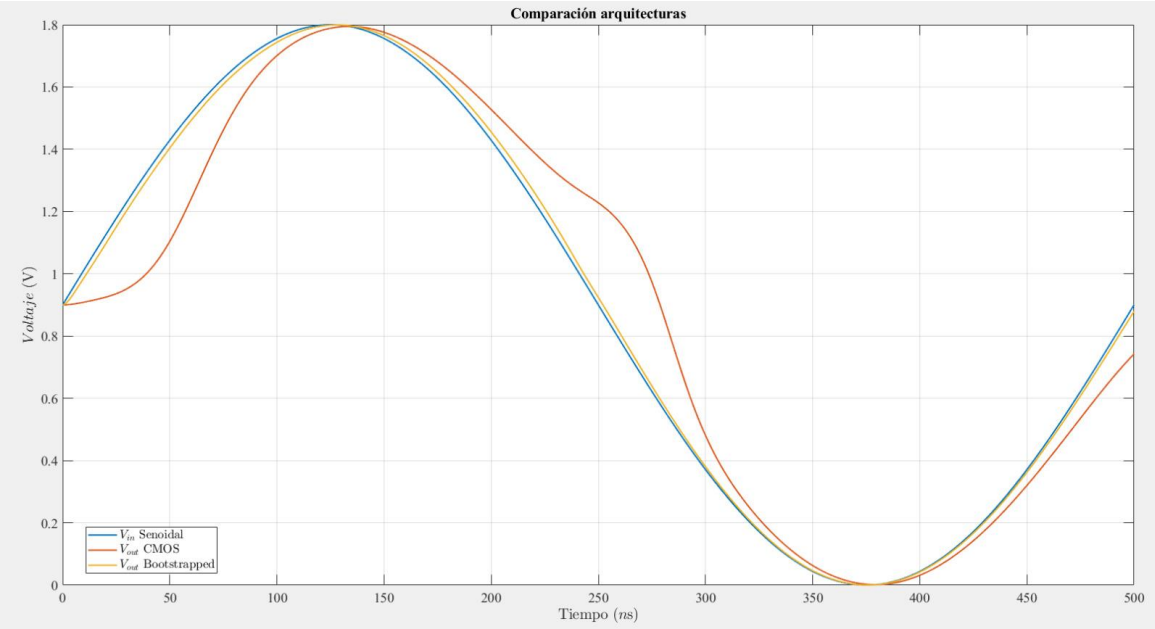
Bootstrapped transmission gate

Transmission gates exhibit an input-dependent on-resistance, this behaviour interfere with the ability to reach the full range of supply voltage, a method to mitigate this is with a bootstrapped TG which increases the gate voltage. A bootstrapped transmission gate has been characterized on SKY130, TB needs minor updates (some geometries were not fully optimized on time for the presentation)

Transmission Gate	Sampling Frequency (MHz)	THD (%)	Comment
CMOS	-	7.779	Significant distortion
Bootstrapped	-	0.153	Excellent linearity
Bootstrapped	200	0.087	Excellent linearity
Bootstrapped	400	0.533	No noticeable distortion
Bootstrapped	450	0.941	Onset of distortion
Bootstrapped	500	1.794	Significant distortion



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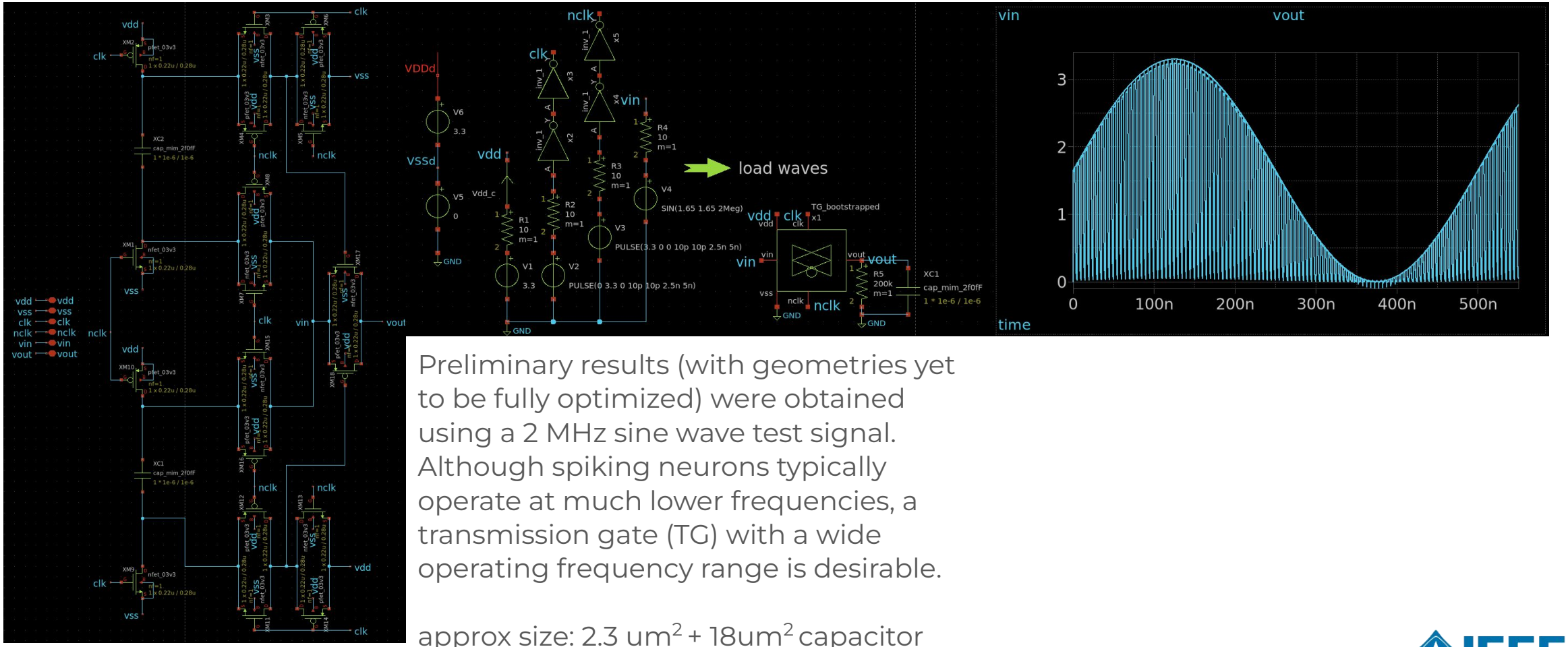
Bootstrapped transmission gate



Preliminary results (with geometries yet to be fully optimized) were obtained using a 2 MHz sine wave test signal. Although spiking neurons typically operate at much lower frequencies, a transmission gate (TG) with a wide operating frequency range is desirable.

approx size: 2.3 um^2 + 18um^2 capacitor

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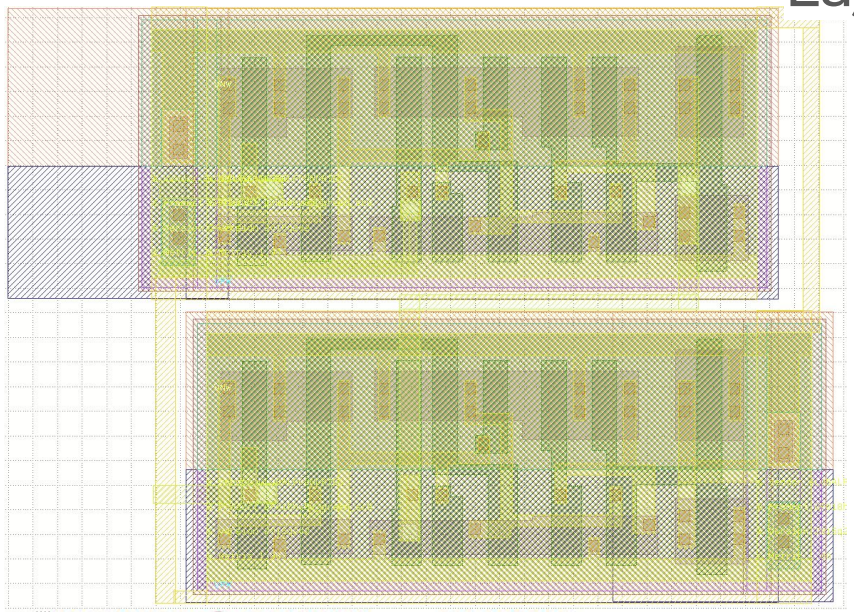
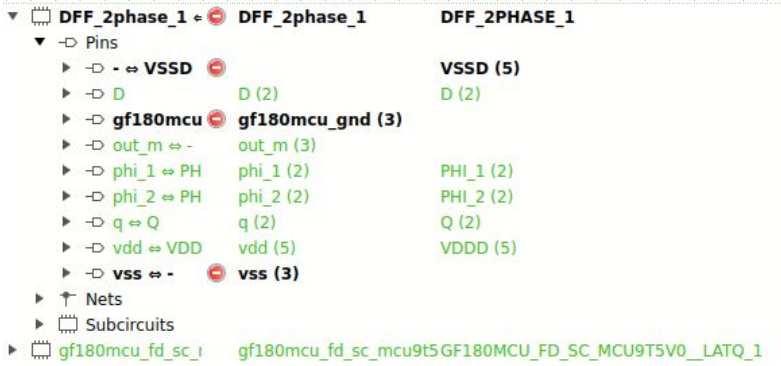
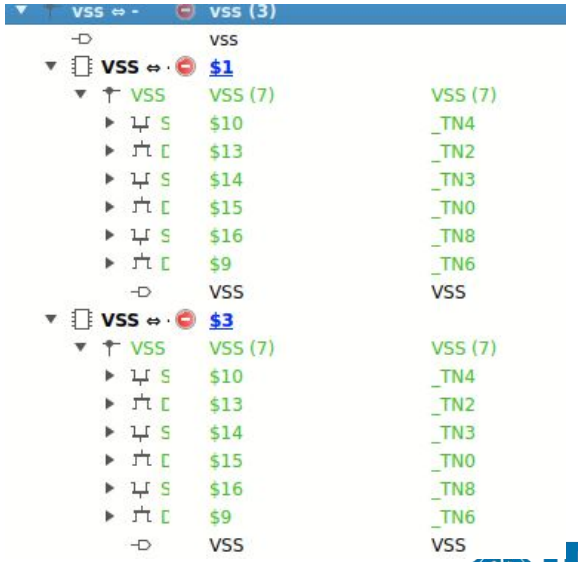
Layout of the D type Flip Flop



Individual elements from the standard cells are correctly mapped out (the subckt definition need to be added to the spice file)
Mismatch between layout & schematic where nets from standard cell netlist are not connected in the top view, resulting in an error



layout	schematic
	VSSD
	VPW
	VSS
gf180mcu_gnd	VPW



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Open issues

Layout and testing of the D flip-flop (DFF) are currently in progress. There are still some issues with LVS, primarily the recognition of the netlists for VPW, VNW, VSS, and gf180mcu_gnd. Other LVS issues have been resolved, thanks to David Mitchell Bailey, particularly those involving endcaps and subcircuits (.subckt) in the SPICE netlist used for LVS in KLayout.

Comparison between different team designs for TGs. This approach would allow us to integrate various TG implementations on the same chip.

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