2025 Chipathon 5th Weekly Project Proposals 1/2

IEEE Solid-State Circuits Society
Technical Committee on the Open Source Ecosystem (TC-OSE)
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Team members: Royce Richmond [Team Leader] (RR)

Rosendo Valdés (RV)

Athesh

Venkadesh

Team background:

- Academic Experience:
 - o RR Third-year Phd student at CIC IPN
 - o RV Final-year Master's student at CIC IPN
- Work Experience:
 - o RV Signal integrity engineer @ Intel



Project goal:

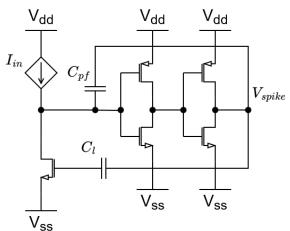
Develop a reconfigurable neuronal architecture leveraging a crossbar array topology, enabling experimentation with different neural networks configurations, input/output patterns, and domain-specific problemsolving.

We have unlimited power!! (kind of)



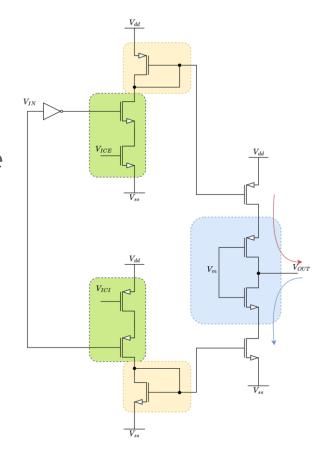
AH (Axon Hillock)[1] neuron

 Small footprint, low power consumption, and high density!!



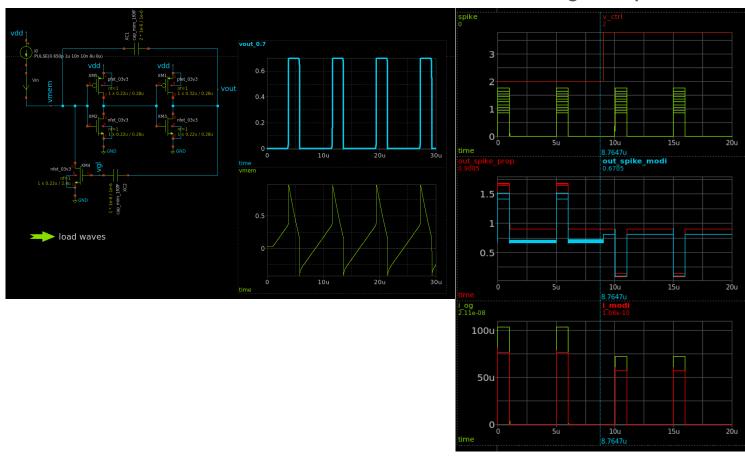
Synapses

- Pattern recognition relies on excitatory and inhibitory connections, we can replicate this functionality with synapses that can do both.
- Keeping each block simple





Simulation results on neurons, synapses and transmission gates

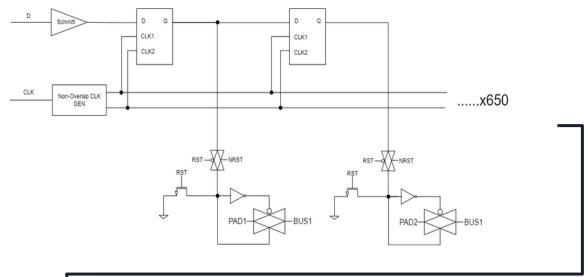


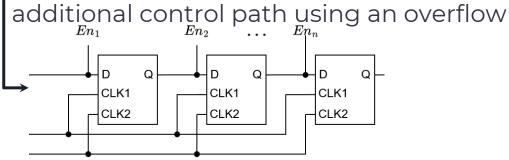


Expand the hardware and software

- expand the flip flops to act as enable signals for subcomponents
- develop (mostly) transparent reconfigurable interconnects between neurons
- extend the bitbang upload method (raspberry pico) to configure the analog architecture

Existing control path for mosbius



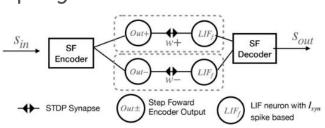


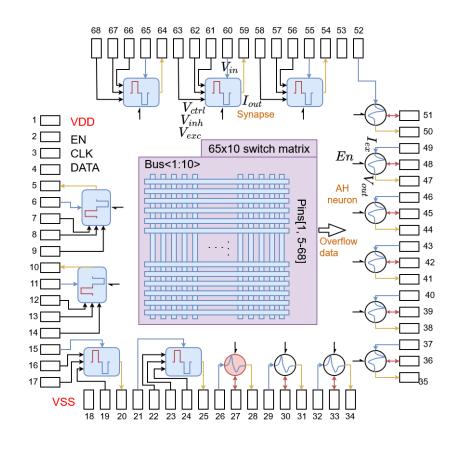


Pinout and characteristics:

- 7 inhibitory/excitatory synapses
- 8 AH neuron subthreshold
- 1 LIF neuron
- 1 LIF neuron subthreshold

The chip can interface with event camera, robotics [2], biophysical signal, etc







Timeline

Week	Task	Responsable	Expected product
28	Project proposal review	All team members	Review proposal with posible updates and tweaks
29	Update and modification to proposal	All team members	Updated project proposal with observations
30	Schematic and symbol creation of neuron, synapse, TG, and read/write subsystem.	Royce Richmond Venkadesh Athesh	Symbol and schematics of building blocks of the peripheral components of spiking mosbius
31	Simulation of TG and characterization	Rosendo Valdés Venkadesh	Simulation and characteristics of TG
32	Simulation of neuron and synapse with TG (pending FF)	Royce Richmond	Simulation and characteristics of neurons and synapses
33	Top cell simulation	All team members	Top cell integration and simulation



Timeline

Week	Task	Responsable	Expected product
34	Layout of individual cells and post layout simulation	Rosendo Valdes Royce richmond	GDS and spice files
35	Layout of Cross-bar array and interconnects	Royce Richmond Venkadesh	GDS and spice files
36	Integration of layouts (top cell) and post layout simulation	All team members	Final GDS file of the top cell
37	Layout review	All team members	Reviewed layout and possible annotations
38	Verification of top cell comparison pre vs post layout	Royce Richmond Rosendo valdes	Final layout ready for submission
39	Review process of submission and repository	Royce Richmond Rosendo valdes	Submission for manufacturing
40	Review of submitted file, simulations and data analysis	Royce Richmond	Report with incidents, improvements and results