ELECTRONIC DEVICES AND CIRCUITS

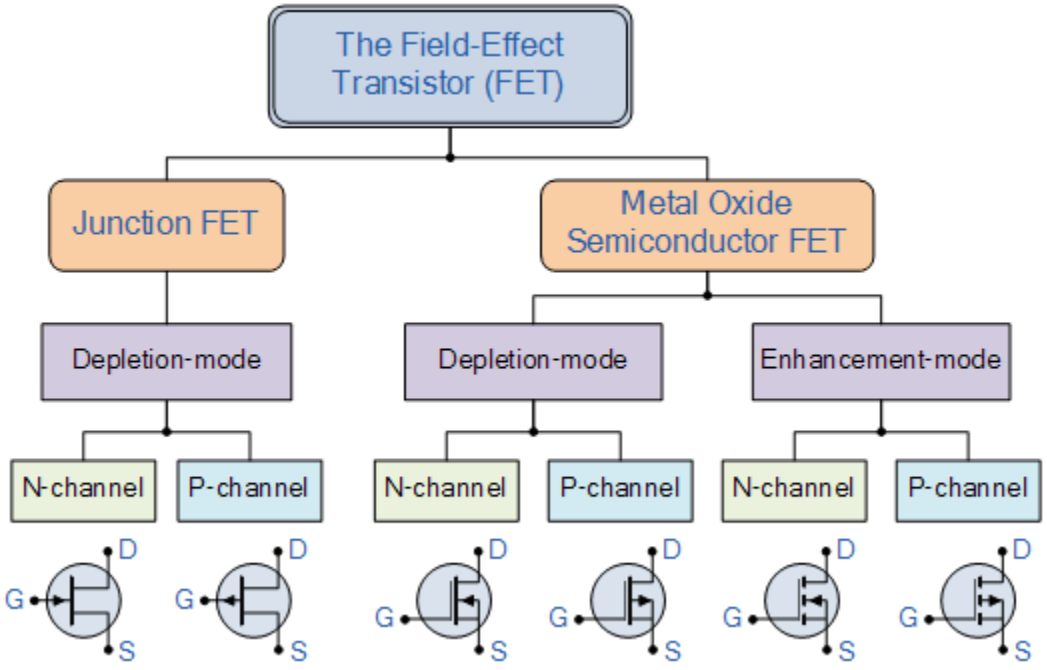
UNIT IV Junction Field Effect Transistor and MOSFET:

Construction, Principle of Operation, Pinch-Off voltage, Volt-Ampere characteristic, comparison of BJT and FET, Biasing of FET, FET as voltage variable resistor, MOSFET construction and its characteristics in enhancement and depletion modes.

4.1 Introduction to Field Effect Transistor

A field effect transistor is a voltage controlled device i.e. the output characteristics of the device are controlled by input voltage. There are two basic types of field effect transistors:

- Junction field effect transistor (JFET)
- Metal oxide semiconductor field effect transistor (MOSFET)



4.2 Junction Field Effect Transistor (JFET)

- A JFET is a three terminal semiconductor device in which current conduction is by one type of carrier i.e. electrons or holes.
- It has three terminals namely Source (S), Drain (D) and Gate (G).
- The current conduction is controlled by means of an electric field between the gate and the conducting channel of the device.
- The JFET has high input impedance and low noise level.
- There are two types of JFET's namely N-channel JFET's and P-channel JFET's.
- Generally N-channel JFETs are more preferred than P-channel.

4.2.1 Symbols of JFET

- The symbol of N-channel and P-channel JFETs are shown in the figure 4.1.

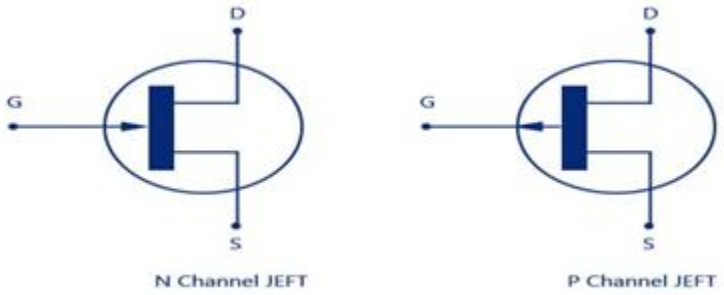


Fig. 4.1 Symbols of N - channel and P- channel JFET

- The vertical line in the symbol may be thought as channel and source S and drain D connected to the line.
- Note that the direction of the arrow at the gate indicates the direction in which the gate current flows.

4.2.2 Construction of JFET

- In an N-channel JFET an N-type silicon bar, referred to as the channel, has two smaller pieces of P-type silicon material diffused on the opposite sides of its middle part, forming P-N junctions, as illustrated in figure 4.2.

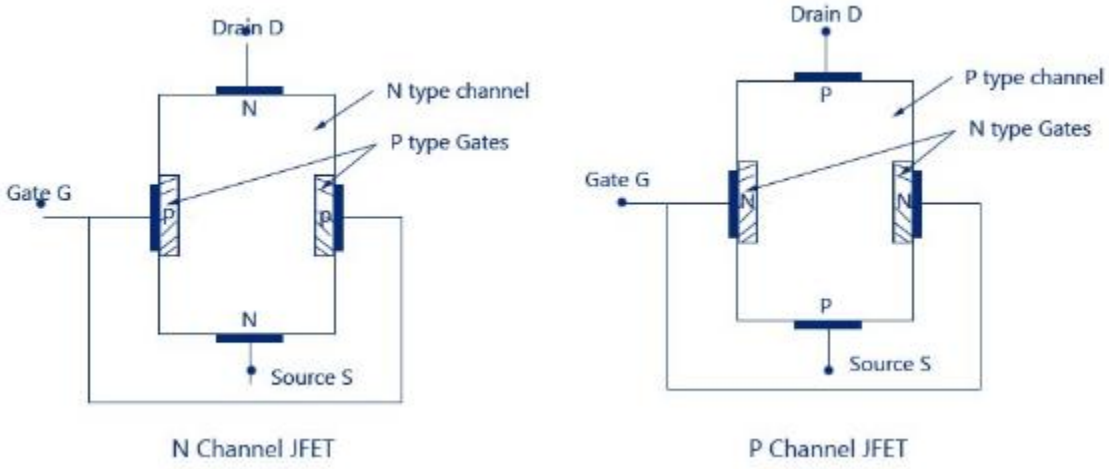


Fig. 4.2 Construction of JFET

- The two P-N junctions forming diodes or gates are connected internally and a common terminal, called the gate terminal, is brought out.
- Ohmic contacts (direct electrical connections) are made at the two ends of the channel—one lead is called the Source terminal S and the other Drain terminal D.
- **Source** – The terminal through which the majority carriers enter the channel, is called the source terminal S
- **Drain** – The terminal, through which the majority carriers leave the channel, is called the drain terminal D

- **Channel** – The region between the source and drain, sandwiched between the two gates is called the channel and the majority carriers move from source to drain through this channel.
- The silicon bar behaves like a resistor between its two terminals D and S.
- The gate terminal is used to control the flow of current from source to drain.
- In the figure above, the gate is P-region, while the source and the drain are N-regions.
- Because of this, a JFET is similar to two diodes.
- The gate and the source form one of the diodes, and the drain form the other diode.
- These two diodes are usually referred as the gate-source diode and the gate-drain diode.
- Since JFET is a silicon device, it takes only 0.7 volts for forward bias to get significant current in either diode.

4.2.3 Polarities of JFET

- Fig.4.3 shows the n-channel JFET polarities and the p-channel JFET polarities.
- In each case, the voltage between the gate and source is such that the gate is reverse biased.
- The source and the drain terminals are interchangeable.

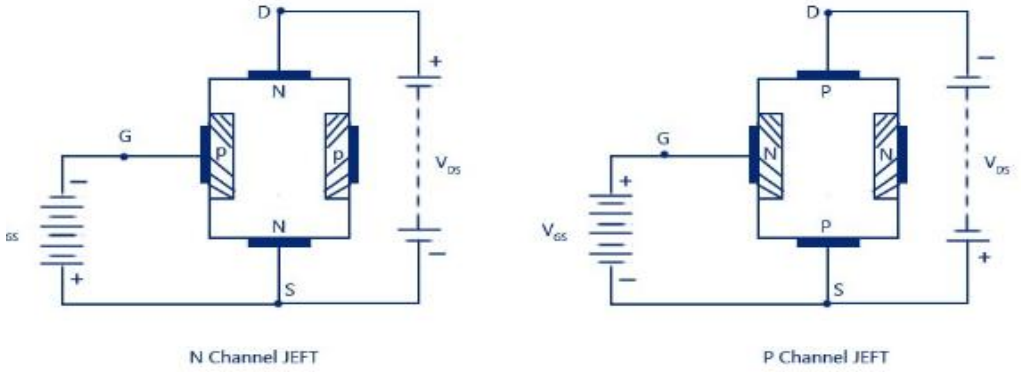


Fig. 4.3 Polarities of JFET

4.2.4 Principle of operation n channel JFET

- The working of JFET can be explained as follows.

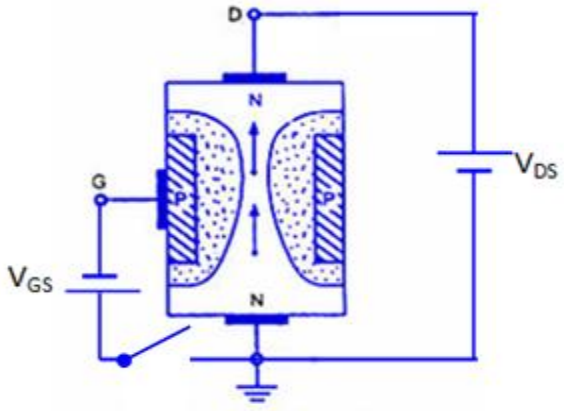


Fig. 4.4 Operation of JFET when V_{GS}=0

Case-i:

- When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero as shown in fig.4.4, then two pn junctions at the sides of the bar establish depletion layers.
- The electrons will flow from source to drain through a channel between the depletion layers.
- The size of the depletion layers determines the width of the channel and hence current conduction through the bar.

Case-ii:

- When a reverse voltage V_{GS} is applied between gate and source terminals, then width of depletion layer is increased which is shown in fig. 4.5.
- This reduces the width of conducting channel, thereby increasing the resistance of n-type bar.
- Consequently, the current from source to drain is decreased.
- On the other hand, when the reverse bias on the gate is decreased, the width of the depletion layer also decreases.
- This increases the width of the conducting channel and hence source to drain current

4.2.5 Principle of operation p channel JFET

- A p channel JFET operates in the same manner as an n-channel JFET except that channel current carries will be the holes instead of electrons and polarities of V_{GS} and V_{DS} are reversed.

4.3 Volt-Ampere characteristics of JFET

- There are two types of static characteristics viz.
    - Output or drain characteristics
    - Transfer characteristics

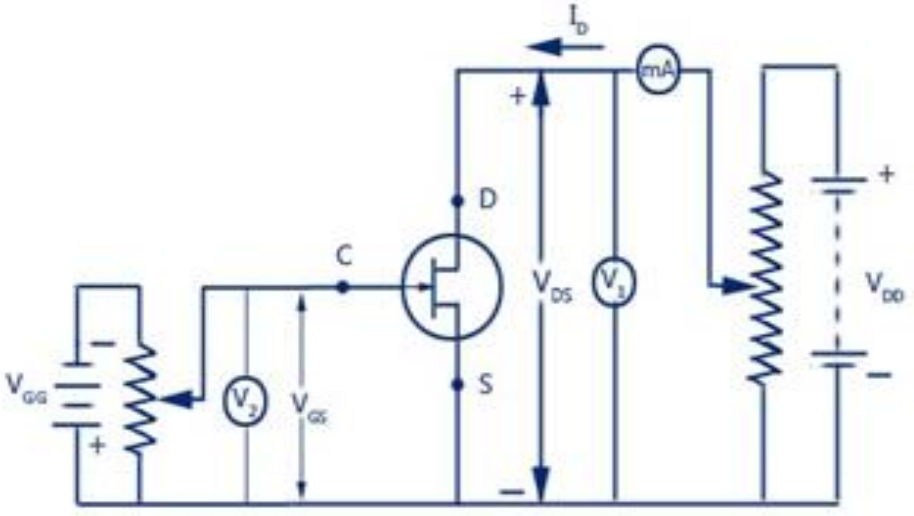


Fig. 4.5 Drain characteristics of JFET

4.3.1 Output or Drain Characteristics

- The curve drawn between drain current I_D and drain-source voltage V_{DS} by keeping gate-to source voltage V_{GS} as constant parameter.

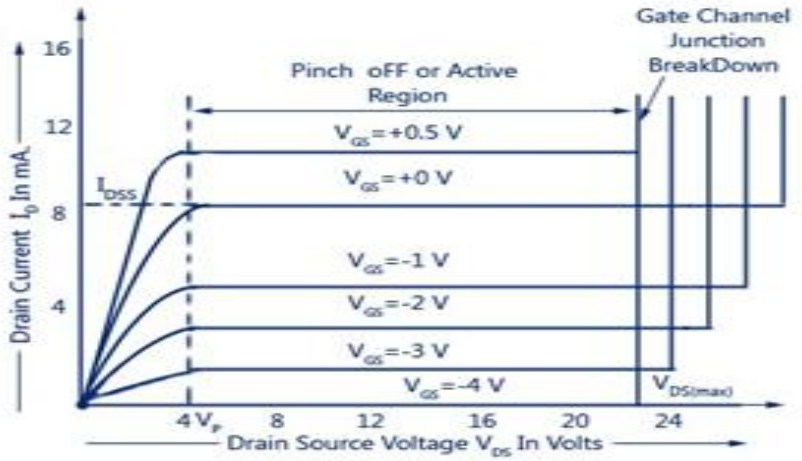


Fig. 4.6 Waveforms of Drain characteristics of JFET

Pinch-off voltage

The value of voltage V_{DS} at which the channel is pinched off (i.e. all the free charges from the channel get removed) and the drain current I_D attains a constant value is called as pinch-off voltage Vp.

- For small applied voltage VDS, the n-type bar acts as a simple semiconductor resistor and the drain current increases linearly with the increase in VDS, upto the knee point.
- So with the increase in V_{DS}, the conducting portion of the channel begins to constrict more at the drain end. Eventually a voltage V_{DS} is reached at which the channel is pinched off.
- The drain current I_D no longer increases with the increase in V_{DS}. It approaches a constant saturation value.
- The drain current in the pinch-off region with V_{GS} = 0 is referred to the drain-source saturation current (I_{DSS}).
- Drain current in the pinch-of region is given by Shockley's equation

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{\mathrm{Vp}}\right]^2$$

Where

I_D = Drain current at given VGS
I_{DSS} = Drain-source saturation current
V_{GS} = Gate-source Voltage
$V_{GS(off)}$ = Gate-source cut off voltage
V_P = Pinch off voltage

4.3.2 Transfer characteristics

- The transfer characteristics for a JFET can be determined experimentally, keeping drain-source voltage V_{DS} as constant and determining drain current I_D for various values of gate-source voltage, V_{GS}.
- The circuit diagram is shown in fig. 4.5.

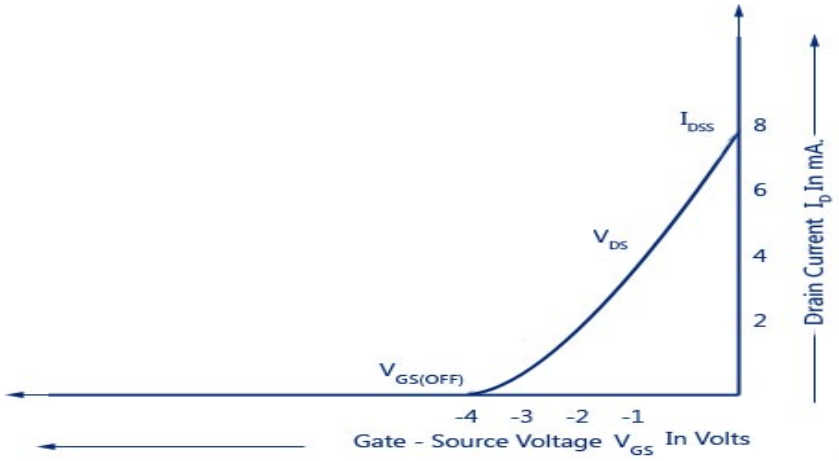


Fig. 4.7 Transfer characteristics

- The curve is plotted between gate-source voltage, V_{GS} and drain current, I_D, as illustrated in fig. 4.7.
- It is observed that
    - Drain current decreases with the increase in negative gate-source bias
    - Drain current, $I_D = I_{DSS}$ when $V_{GS} = 0$
    - Drain current, $I_D = 0$ when $V_{GS} = V_D$

4.5 JFET parameters

- The JFET parameters are the major components of low frequency small signal model for JFET.
- We know that, drain to source current of JFET is controlled by gate to source voltage.
- The change in the drain current due to change in gate to source voltage can be determined using the transconductance factor g_m. It is given as

$$g_m = \frac{\Delta I_d}{\Delta V_{GS}}$$

- The another important parameter of JFET is drain resistance r_d. It is given by

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}= \text{constant}}$$

It determines the output impedance Z_o of the JFET amplifier.

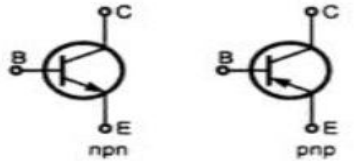
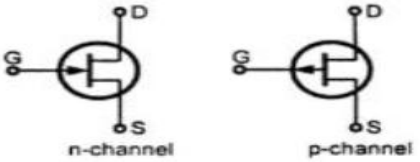
- The amplification factor μ of an FET is defined as

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{gS}}\right|_{I_D=\text{const}}$$

- The parameters g_m, r_d and μ are related by,

$$\mu = r_d\, g_m$$

4.6 Comparison BJT and FET

Sr. No.	Parameter	BJT	FET
1	**Control element**	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2	**Device type**	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3	**Types**	npn and pnp	n-channel and p-channel.
4	**Symbols**		
5	**Configurations**	CE, CB, CC	CS, CG, CD
6	**Input resistance**	Less compare to JFET.	High compare to BJT.
7	**Size**	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in integrated - circuits (IC).
8	**Sensitivity**	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9	**Thermal stability**	Less	More
10	**Thermal runaway**	Exists in BJT, because of cummulative effect of increase in I_C with temperature, resulting increase in temeperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.
11	**Relation between input and output**	Linear	Non-linear
12	**Ratio of o/p to i/p**	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13	**Thermal noise**	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14	**Gain bandwidth product**	High	Low

4.7 Biasing FET

- Like BJT, the parameters of FET are also temperature dependent.
- In FET, as temperature increases drain resistance also increases, reducing the drain current.
- Thus unlike BJT, thermal runaway does not occur with FET.
- However, the wide differences in maximum and minimum transfer characteristics make it necessary to keep drain current I_D stable at its quiescent value.
- The general relationships that can be applied to the d.c analysis of all FET amplifiers are:

$$I_G = 0\ A$$

$$I_D = I_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

4.7.1 Types of FET biasing circuits

- Fixed Bias Circuit
- Voltage Divider Bias Circuit
- Self Bias Circuit

4.7.2 Fixed Bias Circuit

- Fig. 4.8 shows the fixed bias circuit for the n-channel JFET.
- This is the simplest biasing arrangement.
- To make gate-source junction reverse-biased, a separate supply V_{GG} is connected such that gate is more negative than the source.

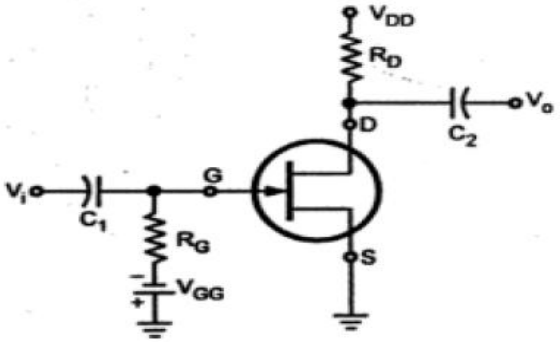


Fig. 4.8 Fixed Bias Circuit for the n-channel JFET

4.7.2.1 DC Analysis

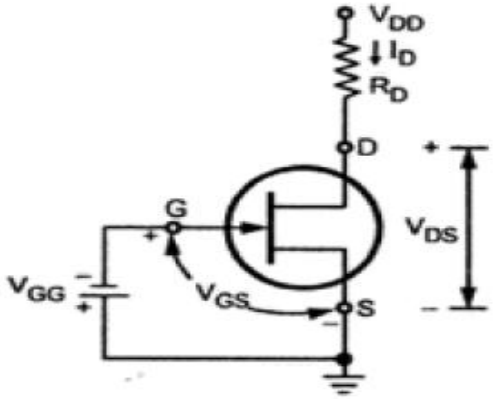


Fig. 4.9 Simplified Fixed bias Circuit

- For the d.c analysis coupling capacitors are open circuits.
- The current through R_G is I_G which is zero.
- This permits R_G to replace by short circuit equivalent.
- Simplified the fixed bias circuit as shown in the Fig. 4.9.

We know for d.c. analysis

$$I_G = 0 \text{ A}$$

And applying KVL to the input circuit we get,

$$V_{GS} + V_{GG} = 0$$

$$\therefore \boxed{V_{GS} = -V_{GG}}$$

Since V_{GG} is a fixed d.c. supply, the voltage V_{GS} is fixed in magnitude, and hence the name fixed bias circuit.

For fixed bias circuit the drain current I_D can be calculated using equation

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$

The drain to source voltage of output circuit can be determined by applying KVL.

$$+ V_{DS} + I_D R_D - V_{DD} = 0$$

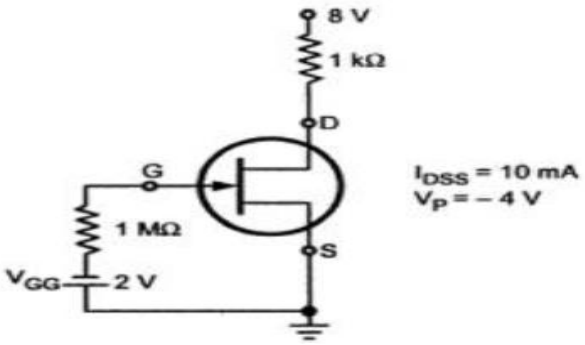
$$\therefore \boxed{V_{DS} = V_{DD} - I_D R_D}$$

The Q point of the JFET amplifier with fixed bias circuit is given by :

$$\boxed{I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

$$\boxed{V_{DSQ} = V_{DD} - I_{DQ} R_D}$$

Example : *For the circuit shown in the Fig. Calculate :*
a) V_{GSQ}, b) I_{DQ}, c) V_{DSQ}, d) V_D



Solution :

a) $V_{GSQ} = -V_{GG} = -2\ V$

b) $I_{DQ} = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2 = 10\times10^{-3}\left(1-\frac{-2\ V}{-4\ V}\right)^2$

$= 10\times10^{-3}\ (1-0.5)^2 = 10\times10^{-3}\ (0.25) = 2.5\ mA$

c) $V_{DSQ} = V_{DD} - I_{DQ}R_D = 8\ V - 2.5\times10^{-3}\ (1\times10^{3}) = 5.5\ V$

d) $V_D = V_{DS} + V_S = 5.5 + 0 = 5.5\ V$

4.7.3 Voltage Divider Bias Circuit

- The Fig. 4.10 shows n-channel JFET with voltage divider bias.
- The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased.

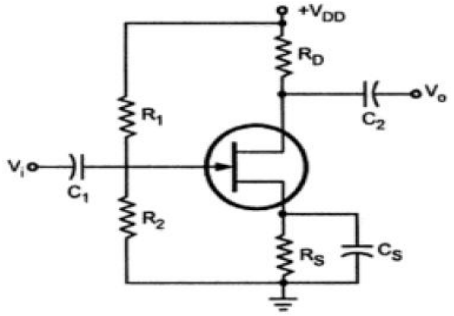


Fig. 4.10 Voltage Divider Bias Circuit

- The source voltage is,

$$V_S = I_D R_S$$

- The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage divider formula

$$V_G = \left(\frac{R_2}{R_1+R_2}\right)V_{DD} \qquad \because I_G = 0$$

4.7.3.1 DC Analysis

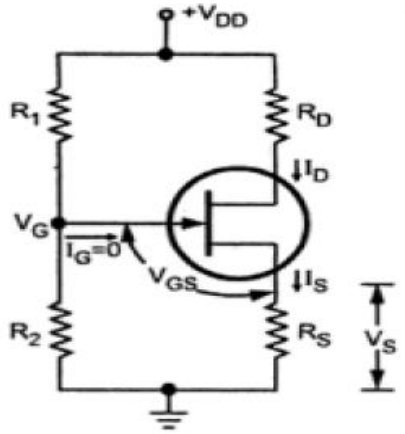


Fig. 4.11 Simplified Voltage Divider Bias Circuit

Applying KVL to the input circuit we get,

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$$

$$= V_G - I_D R_S \qquad \because I_D = I_S$$

$$\therefore \boxed{V_{GS} = V_G - I_D R_S}$$

Applying KVL to the output circuit we get,

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

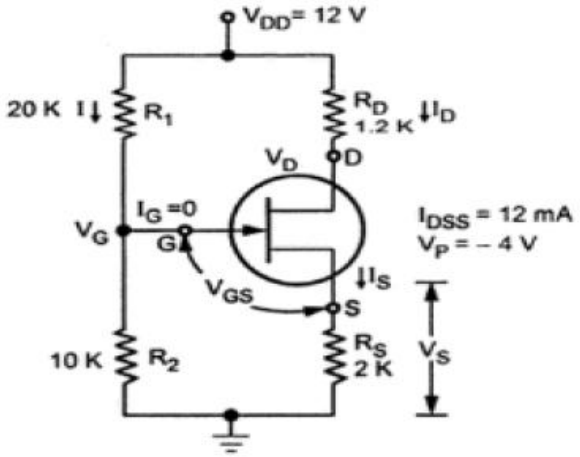
$$\boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$$

The Q point of a JFET amplifier using the voltage divider bias is given by :

$$\boxed{I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

$$\boxed{V_{DSQ} = V_{DD} - I_D (R_D + R_S)}$$

Example : *For circuit shown in Fig. Calculate* I_D , V_{GS} , V_G, V_{DS} *and* V_S.



Solution : We have,

$$V_{GS} = V_G - I_D R_S$$

where $$V_G = \frac{V_{DD} R_2}{R_1 + R_2} = \frac{12 \times 10K}{10K + 20K} = 4 \text{ V}$$

$$\therefore V_{GS} = 4 - I_D R_S$$

We have, $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} we get,

$$I_D = I_{DSS}\left(1-\frac{(4-I_D R_S)}{V_p}\right)^2 = 12\times10^{-3}\left(1-\frac{(4-I_D\times2\times10^3)}{-4}\right)^2$$

$$= 12\times10^{-3}\,(1-[(-1)+500\,I_D])^2 = 12\times10^{-3}\,(2-500\,I_D)^2$$

$$= 12\times10^{-3}(4-2000\,I_D+250000\,I_D^2)$$

$$I_D = (0.048-24\,I_D+3000\,I_D^2)$$

$$\therefore\ 3000\,I_D^2-25\,I_D+0.048=0$$

Solving quadratic equation using formula $\frac{-b\pm\sqrt{b^2-4ac}}{2a}$ we get,

$$= \frac{-(25)\pm\sqrt{(-25)^2-4(3000)(0.048)}}{2(3000)}$$

$$= \frac{25\pm\sqrt{625-576}}{6000} = \frac{25\pm\sqrt{49}}{6000} = \frac{25\pm7}{6000} = 5.33\text{ mA or }3\text{ mA}$$

If we calculate value of V_{DS} taking $I_D = 5.33$ mA we get,

$$V_{DS} = V_{DD}-I_D(R_D+R_S)$$

$$= 12-5.33\times10^{-3}(1.2K+2K) = 12-17.07 = -5.07$$

Practically, the value of V_{DS} must be positive, hence $I_D = 5.33$ mA is invalid.

$$\therefore I_D = 3\text{ mA},$$

$$V_{DS} = 12-3\times10^{-3}\,(1.2\times10^3+2\times10^3) = 12-9.6 \doteq 2.4\text{ V}$$

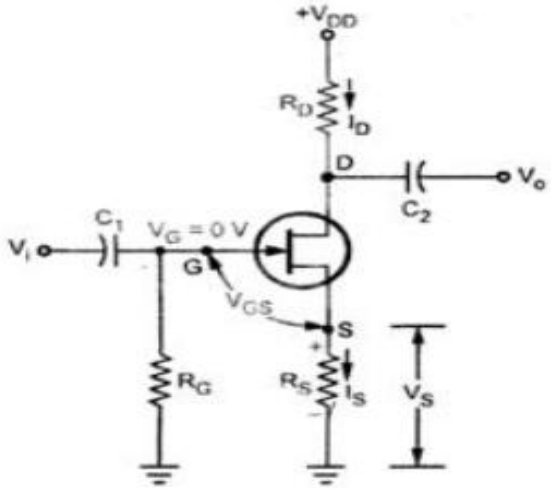
$$\therefore V_{DS} = 2.4\text{ V}$$

$$V_{GS} = 4-I_D R_S = 4-3\times10^{-3}\times2\times10^3 = 4-6 = -2\text{ V}$$

$$V_S = I_D R_S = 3\times10^{-3}\times2\times10^3 = 6\text{ V}$$

4.7.4 Self Bias Circuit

- Self bias is the most common type of JFET bias.
- Recall that a JFET must be operated such that the gate source junction is always reverse-biased.
- This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET.
- This can be achieved using the self bias arrangement shown in Fig. 4.12.
- The gate resistor, R_G does not affect the bias because it has essentially no voltage drop across it and therefore the gate remains at 0 V.
- R_G is necessary only to isolate an a.c signal from ground in amplifier applications.



(a) n-channel

Note : $I_S = I_D$ in all JFETs

Fig. 4.12 Self Bias Circuit using n channel JFET

- The voltage drop across resistor, R_S makes gate source junction reverse biased.
- For the n-channel FET in Fig. 4.12, I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = I_S R_S = I_D R_S$. The gate to source voltage is,

$$V_{GS} = V_G - V_S = 0 - I_D R_S = - I_D R_S$$

$$\boxed{V_{GS} = - I_D R_S}$$

4.7.4.1 DC Analysis

- For D.C. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$.
- This is illustrated in Fig. 4.13.

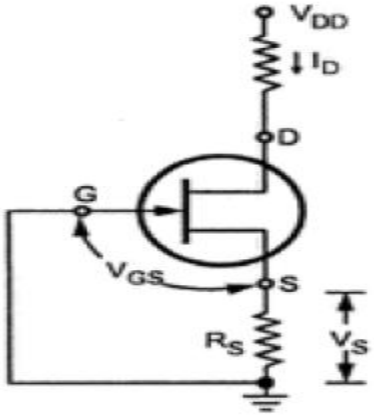


Fig. 4.13 DC equivalent circuit of self bias circuit

- We know that, the relation between I_D and V_{GS}.

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$

- Substituting value of V_{GS} in above equation we get,

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_p}\right)^2$$

$$\boxed{I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2}$$

Applying KVL to the output circuit we get,

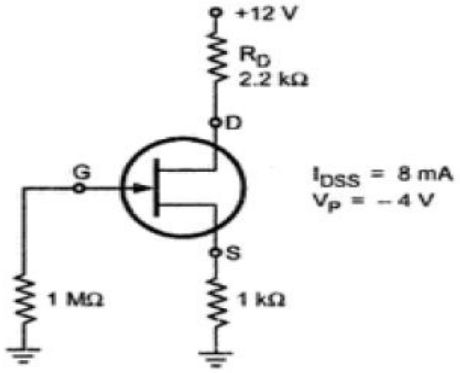
$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D$$

$$= V_{DD} - I_D (R_S + R_D)$$

$$\boxed{V_{DS} = V_{DD} - I_D (R_S + R_D)}$$

Example : *For the circuit shown in Fig. 3.27. Calculate* V_{GSQ} , I_{DQ} , V_{DS} , V_S *and* V_D



Solution : i) I_D : we have,

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2$$

$$\therefore \quad I_D = 8 \times 10^{-3}\left(1 + \frac{I_D \times 1 \times 10^3}{-4}\right)^2$$

$$= 8 \times 10^{-3} (1 - 250 I_D)^2$$

$$= 8 \times 10^{-3} (1 - 500 I_D + 62500 I_D^2)$$

$$I_D = 8 \times 10^{-3} - 4 I_D + 500 I_D^2$$

$$\therefore \quad 500 I_D^2 - 5 I_D + 8 \times 10^{-3} = 0$$

Solving quadratic equating using formula $\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ we have,

$$= \frac{+5 \pm \sqrt{(-5^2) - 4(500)(8\times10^{-3})}}{2\times(500)}$$

$$= \frac{+5 \pm \sqrt{25-16}}{1000} = \frac{+5 \pm \sqrt{9}}{1000}$$

$$= \frac{+5 \pm 3}{1000} = 8 \text{ mA or } 2 \text{ mA}$$

I_{DQ} cannot have value 8 mA because maximum value of I_D, I_{DSS} is given as 8 mA at $V_{GS} = 0$ and hence I_{DQ} is taken as 2 mA.

ii) $V_{GS(Q)}$: we have,

$$V_{GS_Q} = -I_D R_S = -2\times10^{-3}\times1\times10^{3}$$

$$= -2 \text{ V}$$

iii) $V_{GS} : V_S = I_D R_S = -2\times10^{3}\times1\times10^{3}$

$$= 2 \text{ V}$$

iv) $V_{DS} : V_{DS} = V_{DD} - I_D(R_D + R_S) = 12 - 2\times10^{-3}(2.2\times10^{3} + 1\times10^{3}) = 12 - 6.4$

$$= 5.6 \text{ V}$$

v) $V_D = V_{DS} + V_S = 5.6 + 2 = 7.6 \text{ V}$

4.8 FET as Voltage Variable Resistor

- Let us consider the drain characteristics of FET as shown in the Fig. 4.14.

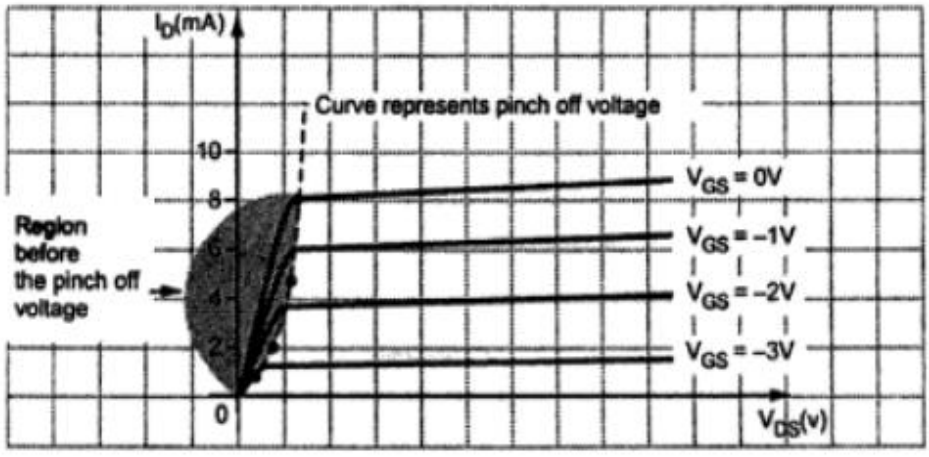


Fig. 4.14 Drain characteristics of FET

- In this characteristic we can see that in the region before pinch off voltage, drain characteristics is Linear, i.e., FET operation is linear.
- In this region the FET is useful as a voltage-controlled resistor, i.e., the drain to source resistance is controlled by the bias voltage V_{GS}.
- The operation of FET in this region is useful in most Linear applications of FET.
- In such an application the FET is also referred to as a Voltage Variable Resistor (VVR) or Voltage Dependent Resistor (VDR).

In JFET, the drain-to-source conductance $g_d = \frac{I_D}{V_{DS}}$ for small values of V_{DS}, which may also be expressed as,

$$g_d = g_{do}\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]$$

where g_{do} is the value of drain conductance when the bias voltage V_{GS} is zero.

The variation of the r_d with V_{GS} can be closely approximated by the empirical expression,

$$r_d = \frac{r_0}{1 - KV_{GS}}$$

where r_0 = drain resistance at zero gate bias, and K = a constant, dependent upon FET type.

Thus, small signal FET drain resistance r_d varies with applied gate voltage V_{GS} and FET acts like a variable passive resistor.

- FET finds wide applications where VVR property is useful.
- For example, the VVR can be used in Automatic Gain Control (AGC) circuit of a multistage amplifier.

4.9 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

- The field effect transistor that can be operated to enhance the width of the channel. Such a FET is called MOSFET.
- The MOSFET differs from the JFET in that it has no p-n junction structure.
- Instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer.
- Due to this the input resistance of MOSFET is greater than JFET.
- Because of the insulated gate, MOSFETs are also called as Insulate Gate FET (IGFET)

4.9.1 Types of MOSFETs

- There are two basic types of MOSFETs such as:
- **Depletion-type MOSFET or D-MOSFET:** The D-MOSFET can be operated in both depletion mode and the enhancement mode.
- **Enhancement-type MOSFET or E-MOSFET:** The E-MOSFET can be operated only in enhancement mode.

4.10 D-MOSFET

- There are two types of D-MOSFETs such as:
    - n-channel D-MOSFET
    - p-channel D-MOSFET

4.10.1 Construction of n-channel D-MOSFET

- A thin layer of metal oxide, usually silicon dioxide (SiO2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer.
- As SiO2 is an insulator, therefore, gate is insulated from the channel.
- The substrate is connected to the source internally so that a MOSFET has three terminals such as Source (S), Gate (G) and Drain (D).

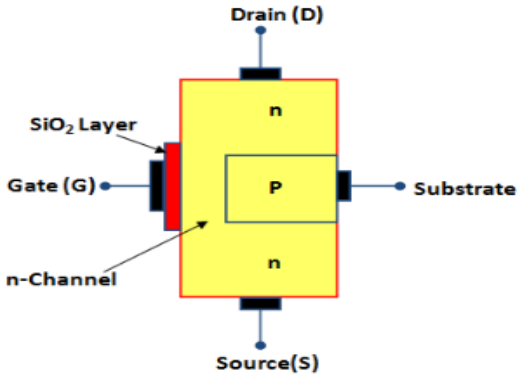


Fig. 4.15 construction of n-channel D-MOSFET

- Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate.
- Therefore, D-MOSFET can be operated in both depletion-mode and enhancement-mode.
- The p-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side.
- Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel.

4.10.2 Symbol for n-channel D-MOSFET

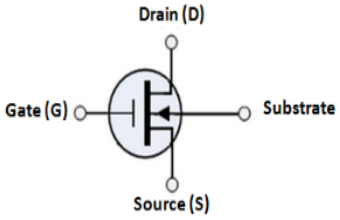


Fig. 4.16 Symbol for n-channel D-MOSFET

- The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel.

- The drain lead comes out of the top of the channel and the source lead connects to the bottom.
- The arrow is on the substrate and points to the n-material, therefore we have n-channel D-MOSFET.
- The substrate is connected to the source as shown in fig.4.17. This gives rise to a three terminal device.

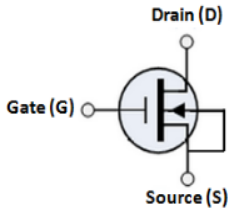


Fig. 4.17 Symbol for n-channel D-MOSFET

4.10.3 Operation of n-channel D- MOSFET

- Fig.4.18 (a) shows the circuit for operation of n-channel D-MOSFET.
- The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric.
- When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the n-channel.
- Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate.
- The negative gate operation is called depletion mode and positive gate operation is called enhancement mode.

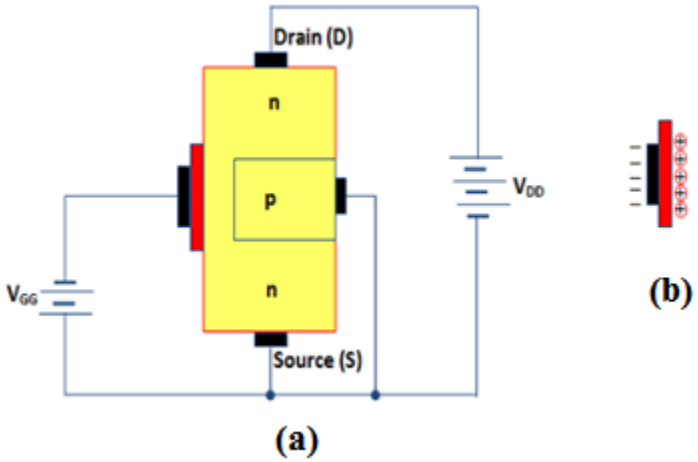


Fig. 4.18 Operation of D- MOSFET

- Since gate is negative, it means electrons are on the gate as shown in fig. 4.18 (b).
- These electrons repel the free electrons in the n-channel, leaving a layer of positive ions in a part of the channel as shown in fig. 4.18 (b).
- In other words, the n-channel is depleted of some of its free electrons.

- Therefore, lesser number of free electrons are available for current conduction through the n-channel. This is same as increasing the channel resistance.
- The greater the negative voltage on the gate, the lesser is the current from source to drain.
- Thus by changing the negative voltage on the gate, we can vary the resistance of the n-channel and hence the current from source to drain.
- As the action with negative gate depends upon depleting the channel of free electrons, the negative-gate operation is called depletion mode.
- In a D-MOSFET, the source to drain current is controlled by the electric field of capacitor formed at the gate.
- D-MOSFET has very low input capacitance, which makes the D-MOSFET useful in high frequency applications.

4.10.4 Construction of p-channel D-MOSFET

- Fig.4.19 shows the various parts of p-channel D-MOSFET.
- The n-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side.
- The conduction takes place by the flow of holes from source to drain through this narrow channel.

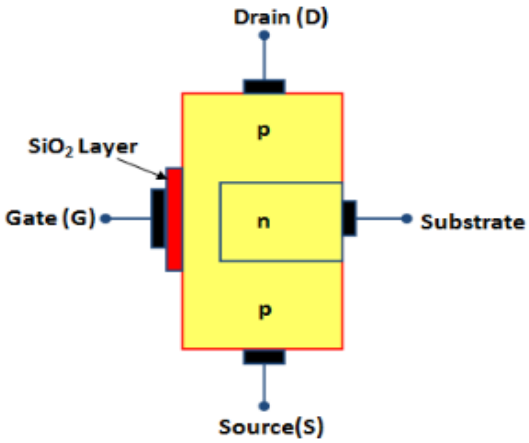


Fig. 4.19 Construction of p-channel D-MOSFET

4.10.5 Symbol for p-channel D-MOSFET

- The symbol for p-channel D-MOSFET is shown in Fig.4.20.

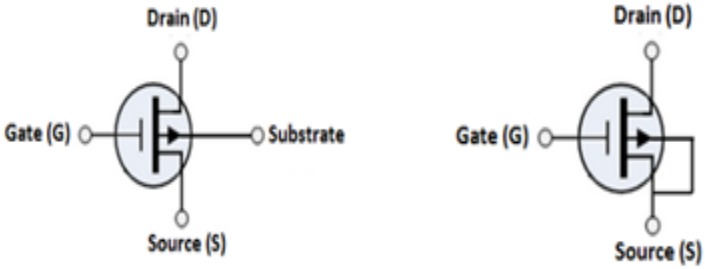


Fig. 4.20 Symbol for p-channel D-MOSFET

4.11 E-MOSFET

- There are two types of D-MOSFETs such as:
    - n-channel D-MOSFET
    - p-channel D-MOSFET

4.11.1 Construction of n-channel D-MOSFET

- Fig.4.21 shows the constructional details of n-channel E-MOSFET.
- Its gate construction is similar to that of D-MOSFET.
- The E-MOSFET has no channel between source and drain. The substrate extends completely to the SiO_2 layer so that no channel exists.

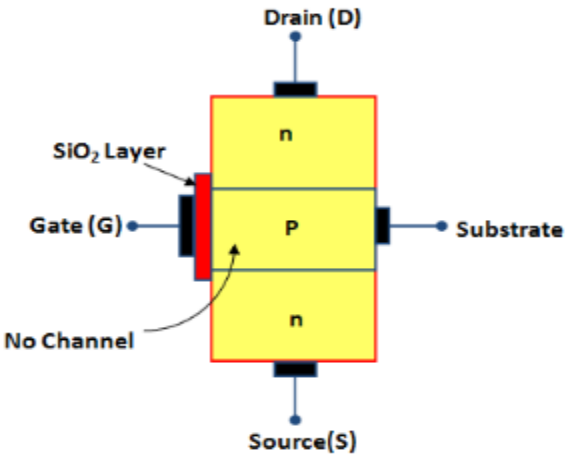


Fig. 4.21 Construction of n-channel D-MOSFET

- The E-MOSFET requires a proper gate voltage to form a channel, called induced channel between the source and the drain.
- It operates only in the enhancement mode and has no depletion mode.
- Only by applying VGS of proper magnitude and polarity, the device starts conducting.
- The minimum value of V_{GS} of proper polarity that turns on the E-MOSFET is called threshold voltage [$V_{GS(th)}$].
- The n-channel device requires positive V_{GS} ($\geq V_{GS(th)}$) and the p-channel device requires negative V_{GS} ($\geq V_{GS(th)}$).

4.11.2 Symbol of n-channel D-MOSFET

- Fig. 4.22 (a) shows the schematic symbols for n-channel E-MOSFET and Fig. 4.22 (b) shows the schematic symbol for p-channel E-MOSFET.

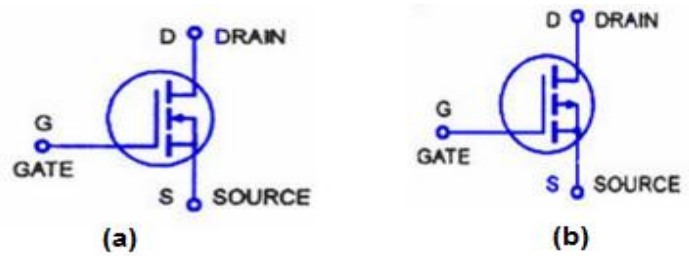


Fig. 4.22 Symbol of n-channel D-MOSFET

4.11.3 Operation of n-channel E-MOSFET

- Fig. 4.23 (a) shows the circuit of operation of n-channel E-MOSFET.
- Again the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the n-channel as shown in fig. 4.23 (b).
- These negative charges are the free electrons drawn into the channel.
- Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased.

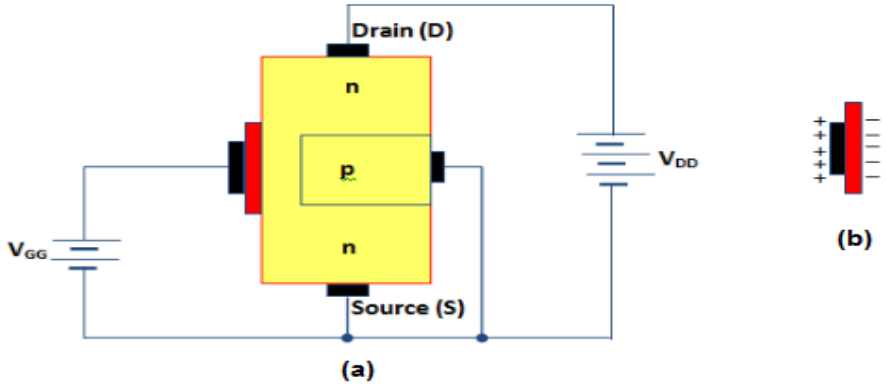


Fig. 4.23 Operation of n-channel E-MOSFET

- Thus a positive gate voltage enhances or increases the conductivity of the channel.
- The greater the positive voltage on the gate, greater the conduction from source to drain.
- Thus by changing the positive voltage on the gate, we can change the conductivity of the channel.
- Because the action with a positive gate depends upon enhancing the conductivity of the channel, the positive gate operation is called enhancement mode.
- When V_{GS}= 0V, as shown in fig. 4.23 (a), there is no channel connecting source and drain.
- The p-substrate has only a few thermally produced free electrons (minority carriers) so that drain current is almost zero. For this reason, E-MOSFET is normally OFF when V_{GS} = 0V.
- When VGS is positive, i.e gate is made positive as shown in fig. 4.23 (b), it attracts free electrons into the p region. The free electrons combine with the holes next to the SiO_2 layer.
- If V_{GS} is positive enough, all the holes touching the SiO_2 layer are filled and free electrons begin to flow from the source to drain.
- The effect is same as creating a thin layer of n-type material i.e. inducing a thin n-layer adjacent to the SiO_2 layer.

- Thus the E-MOSFET is turned ON and drain current I_D starts flowing from the source to the drain.
- The minimum value of VGS that turns the E-MOSFET ON is called threshold voltage [$V_{GS(th)}$].
- When V_{GS} is less than $V_{GS(th)}$, there is no induced channel and the drain current I_D is zero.
- When V_{GS} is equal to $V_{GS(th)}$, the E-MOSFET is turned ON and the induced channel conducts drain current from the source to the drain.
- Beyond $V_{GS(th)}$, if the value of V_{GS} is increased, the newly formed channel becomes wider, causing to I_D to increase.
- If the value of V_{GS} decreases not less than $V_{GS(th)}$, the channel becomes narrower and I_D will decrease.

4.12 MOSFET Characteristics in Enhancement and Depletion modes

- In general, any MOSFET is seen to exhibit three operating regions viz.,
- **Cut-Off Region:** Cut-off region is a region in which the MOSFET will be OFF as there will be no current flow through it.
- In this region, MOSFET behaves like an open switch and is thus used when they are required to function as electronic switches.
- **Ohmic or Linear Region:** Ohmic or linear region is a region where in the current I_{DS} increases with an increase in the value of V_{DS}.
- When MOSFETs are made to operate in this region, they can be used as amplifiers.
- **Saturation Region:** In saturation region, the MOSFETs have their I_{DS} constant inspite of an increase in V_{DS} and occur once when V_{DS} exceeds the value of pinch-off voltage V_P.
- Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows.
- As a result, this operating region is chosen whenever MOSFETs are required to perform switching operations.

4.12.1 n-channel Depletion-type MOSFET

- The transfer characteristics of n-channel depletion MOSFET shown by Figure 4.24 (a) indicate that the device has a current flowing through it even when V_{GS} is 0V.
- This indicates that these devices conduct even when the gate terminal is left unbiased, which is further emphasized by the V_{GS0} curve of Figure 4.24 (b).
- Under this condition, the current through the MOSFET is seen to increase with an increase in the value of V_{DS} (Ohmic region) until V_{DS} becomes equal to pinch-off voltage V_P.
- After this, I_{DS} will get saturated to a particular level I_{DSS} (saturation region of operation) which increases with an increase in V_{GS} i.e. $I_{DSS3} > I_{DSS2} > I_{DSS1}$, as $V_{GS3} > V_{GS2} > V_{GS1}$.
- Further, the locus of the pinch-off voltage also shows that V_P increases with an increase in V_{GS}.

- However it is to be noted that, if one needs to operate these devices in cut-off state, then it is required to make V_{GS} negative and once it becomes equal to $-V_T$, the conduction through the device stops ($I_{DS} = 0$) as it gets derived of its n-type channel (Figure 4.24 a).

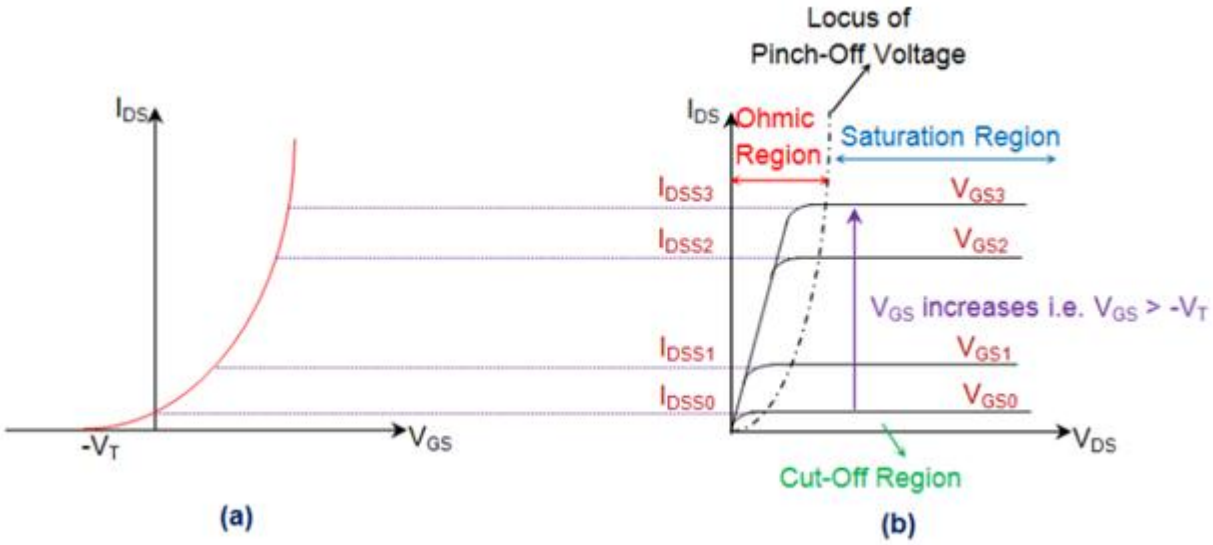


Fig. 4.24 n-channel Depletion-type MOSFET a) transfer characteristics b) output characteristics

4.12.2 n-channel Enhancement-type MOSFET

- Figure 4.25 (a) shows the transfer characteristics (drain-to-source current I_{DS} versus gate-to-source voltage V_{GS}) of n-channel Enhancement-type MOSFETs.
- From this, it is evident that the current through the device will be zero until the V_{GS} exceeds the value of threshold voltage V_T.
- This is because under this state, the device will be void of channel which will be connecting the drain and the source terminals.
- Under this condition, even an increase in V_{DS} will result in no current flow as indicated by the corresponding output characteristics (I_{DS} versus V_{DS}) shown by Figure 4.25 (b).
- As a result this state represents nothing but the cut-off region of MOSFET's operation.
- Next, once V_{GS} crosses V_T, the current through the device increases with an increase in I_{DS} initially (Ohmic region) and then saturates to a value as determined by the VGS (saturation region of operation) i.e. as VGS increases, even the saturation current flowing through the device also increases.
- This is evident by Figure 4.25 (b) where I_{DSS2} is greater than I_{DSS1} as $V_{GS2} > V_{GS1}$, I_{DSS3} is greater than I_{DSS2} as $V_{GS3} > V_{GS2}$, so on and so forth.
- Further, Figure 4.25 (b) also shows the locus of pinch-off voltage (black discontinuous curve), from which V_P is seen to increase with an increase in V_{GS}.

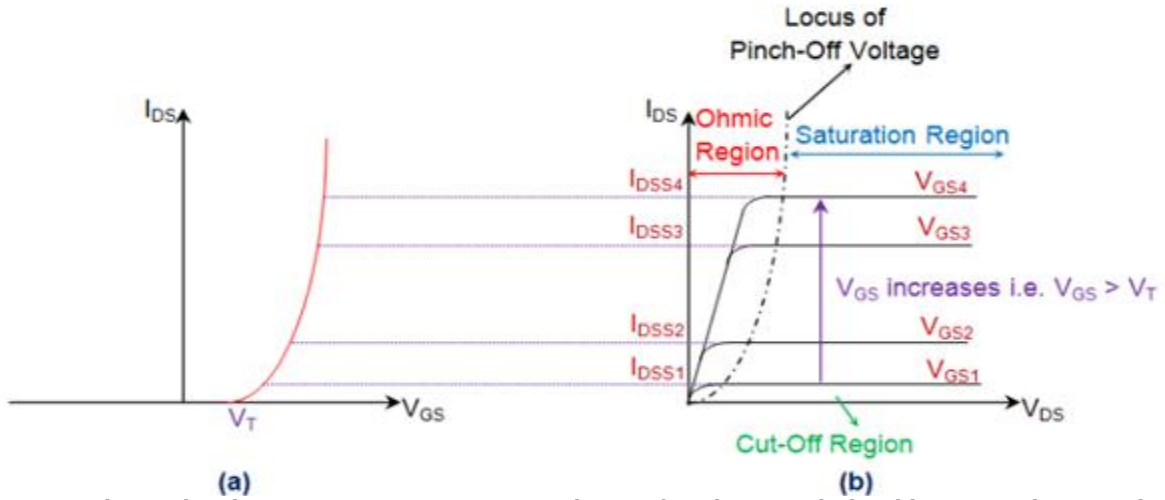


Fig. 4.25 n-channel Enhancement type MOSFET a) transfer characteristics b) output characteristics

The explanation provided above can be summarized in the form of a following table

Kind of MOSFET	Region of Operation		
	Cut-Off	Ohmic/Linear	Saturation
n-channel Enhancement-type	$V_{GS} < V_T$	$V_{GS} > V_T$ and $V_{DS} < V_P$	$V_{GS} > V_T$ and $V_{DS} > V_P$
p-channel Enhancement-type	$V_{GS} > -V_T$	$V_{GS} < -V_T$ and $V_{DS} > -V_P$	$V_{GS} < -V_T$ and $V_{DS} < -V_P$
n-channel Depletion-type	$V_{GS} < -V_T$	$V_{GS} > -V_T$ and $V_{DS} < V_P$	$V_{GS} > -V_T$ and $V_{DS} > V_P$
p-channel Depletion-type	$V_{GS} > V_T$	$V_{GS} < V_T$ and $V_{DS} > -V_P$	$V_{GS} < V_T$ and $V_{DS} < -V_P$