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Homework #4

1. a) I/O-MEM-CPU
2. b) CPU
3. (a)

$$256kB = 256 * 1024 \; bytes$$
$$lg(256 * 1024) = 18 \; address \; lines.$$

(b)

$$2MB = 2 * 1048576 \; bytes$$
$$lg(2 * 1048576) = 21 \; address \; lines.$$

(c)

$$4GB = 4 * 1024MB = 4 * 1024 * 1048576 \; bytes$$
$$lg(4 * 1024 * 1048576) = 32 \; address \; lines.$$

4. (a) Data is stored in the MEMORY.
   (b) Programs are stored in the MEMORY.
   (c) To be executed, an instruction is loaded into the IR.
   (d) The address of an instruction to be executed is held in PC.
   (e) Instructions are retried during the FETCH PHASE.
   (f) Instructions are interpreted during the EXECUTE PHASE.
   (g) Arithmetic operations occur in the ALU.
   (h) Temporary intermediate results are held in the ACC.
5. The fetch phase is preceded by the EXECUTE phase.
6. The fetch phase is followed by the EXECUTE phase.
7. The instruction register (IR) is loaded during the FETCH phase.
8. Computation performed by an instruction occurs during the EXECUTE phase.
9. In the ARM architecture, there are:
   (a) 2 bytes in a half word.
   (b) 8 bytes in a double word.

12. (a)

Address 111	Address 110	Address 109	Address 108
Address 107	Address 106	Address 105	Address 104
Address 103	Address 102	Address 101	Address 100
Address 99	Address 98	Address 97	Address 96

    (b) Address 105.

    (c) 2 memory cycles.

    (d) 1 memory cycle.

13. b) The most significant byte.

14. Address 100.

15. (a) Address N + 3.

    (b) Address N + 2.

16. b) Big-endian numbering.

17. a) From least to most significant bit, starting at 0.

18. (a) 101.

    (b) 102.

    (c) 104.

    (d) 108.

19. b)PC, c)LR, and d)PSW.