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Homework #5

6. (a)
```
long purple;
short blue[10];
short red;
blue[purple] = red;
```

(b)
```
long green;
green++;
long long violet = green;
```

(c)
```
char black;
char white;
white = black - (5 * (black/5));
```

(d)
```
long long orange;
long long yellow;
yellow = orange << 1;
```

7. (a)
```
LDR R0, =100
STR R0, u32
```

(b)
```
LDR R0, u32
STRB R0, u8
```

(c)
```
LDR R0, =100
STRH R0, u16
```

(d)
```
LDRSB R0, s8
STRH R0, s16
```

(e)
```
LDR R0, =100
STRB R0, u8
```

(f)
```
LDRSH R0, s16
STR R0, s32
```

(g)
```
LDR R0, =100
LDR R1, =0
STRD R0, R1, u64
```

(h)
```
LDRSB R0, s8
STR R0, s32
```

(i)
```
LDRB R0, u8
STRH R0, u16
```

(j)
```
LDR R0, s32
ASR R1, R0, #31
LDRD R0, R1, s64
```

(k)
```
LDRH R0, u16
STR R0, u32
```

(l)
```
LDR R0, =-1
LDR R1, =-1
STRD R0, R1, s64
```

(m)
```
LRDB R0, u8
STR R0, u32
```

(n)
```
ADR R0, u32
STR R0, pu32
```

(o)
```
LDR R0, u32
LDR R1, =0
STRD R0, R1, u64
```

(p)
```
ADR R0, u8
```

```
STRB R0, pu8
```

(q)
```
LDRH R0, u16
STRB R0, u8
```

(r)
```
LDRB R0, u8
STRB R0, u32
```

(s)
```
LDR R0, u32
STRH R0, u16
```

(t)
```
LDR R0, pu32
LDR R1, =1
LDR R1, [R0]
```

(u)
```
LDRB R0, u8
ADD R0, R0, #1
```

8. (a)
```
LDRSB R0, s8
LDRD R1, R2, s64
ADDS R0, R0, R1
STR R0, s32
```

(b)
```
ADR R0, a32
LDR R1, p32
SUB R0, R1, R0
ASR R0, R0, #2
ADD R0, R0, #5
STR R0, k32
```

(c)
```
ADR R0, a64
LDR R1, k32
ADD R0, R0, R1 LSL #3
ADD R0, R0, #1
LDR R1, p32
STR R0, [R1]
```

(d)
```
LDR R0, u32
MUL R0, R0, #10
STR R0, s32
```

(e)
```
LDR R0, pp16
LDR R0, [R0]
LDR R1, #0
STR R1, [R0, #1]
```

(f)
```
LDR R0, p32
ADR R1, a32
LDR R2, k32
ADD R1, R1, R2 LSL #2
SUB R1, R1, R0
ASR R1, R1, #2
```

```
STRH R0, u16
```

(v)
```
LDRD R0, R1, u64
ADDS R0, R0, #1
ADC R1, R1, #0
STRD R0, R1, u64
```

(w)
```
ADR R0, u16
ADD R0, R0, #1
STR R0, p16
```

(x)
```
LDR R0, p16
LDRH R1, [R0]
ADD R1, R1, #1
STRH R1, [R0]
```

```
STR R1, k32
```

(g)
```
LDR R0, k32
SUB R0, R0, #1
ADR R1, a16
ADD R1, R1, R0 LSL #1
LDRH R0, [R1]
ADD R0, R0, #1
STRH R0, [R1]
```

(h)
```
LDR R0, u32
LDR R1, =0
STRD R0, R1, u64
```

(i)
```
LDRSB R0, s8
ASR R1, R0, #31
STRD R0, R1, s64
```

(j)
```
LDR R0, s32
ASR R1, R0, #31
STRD R0, R1, s64
```

(k)
```
LDR R0, s32
LDR R1, =10
SDIV R2, R0, R1
MUL R1, R2, R1
SUB R0, R0, R1
STR R0, s32
```

(l)
```
LDR R0, u16
LDR R1, =10
UDIV R0, R0, R1
STRH R0, u16
```