A diagram of a software design flow

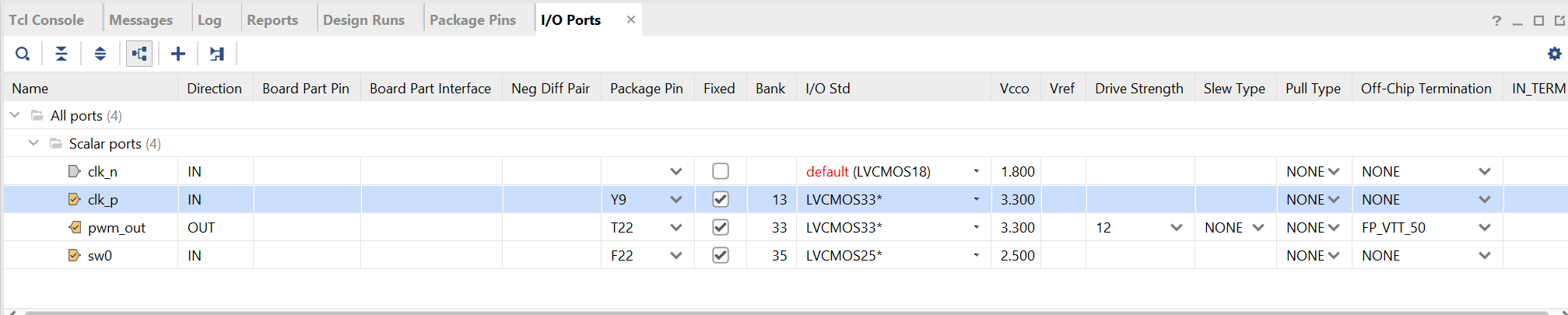
AI-generated content may be incorrect.

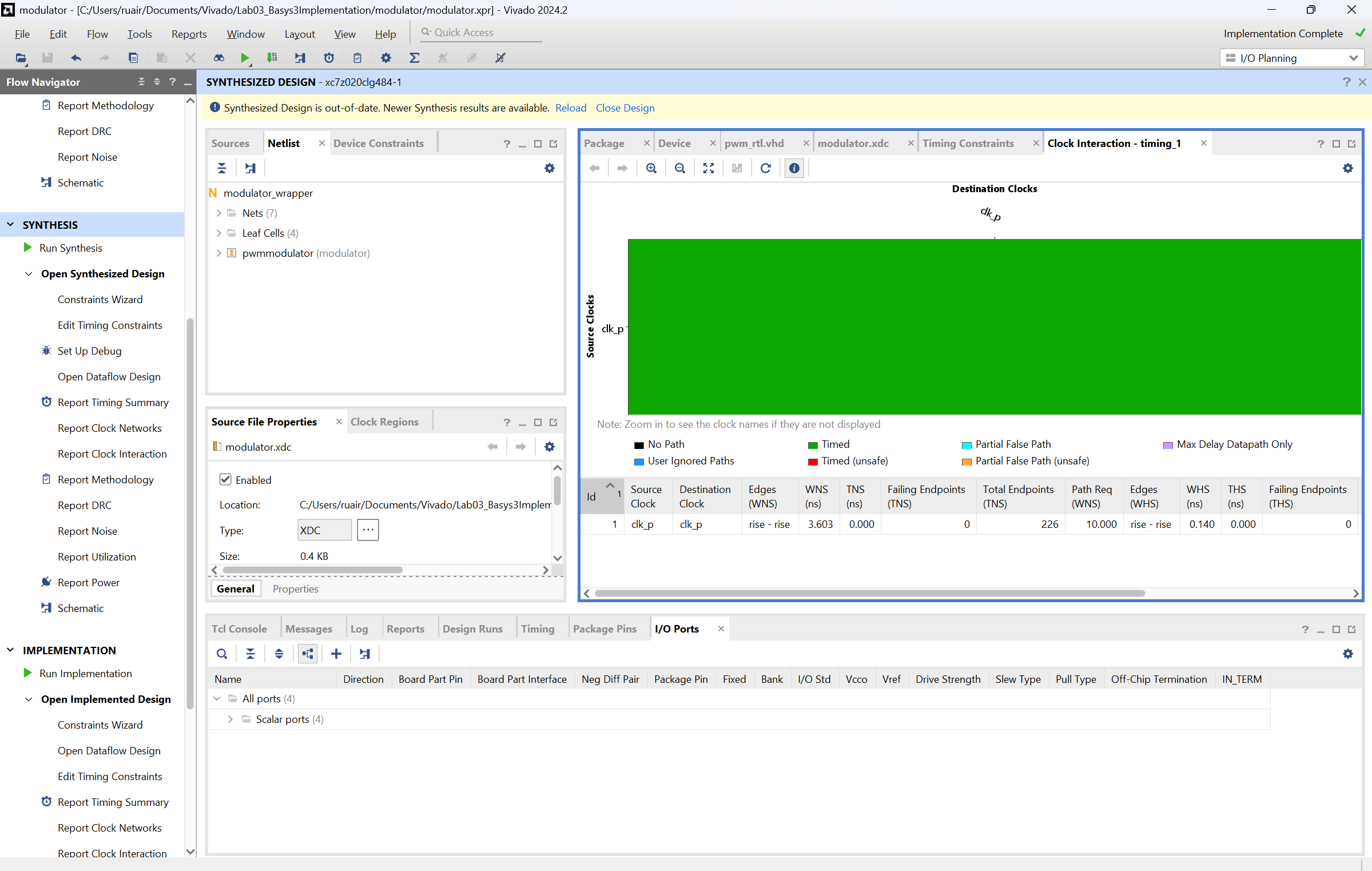
Problems:

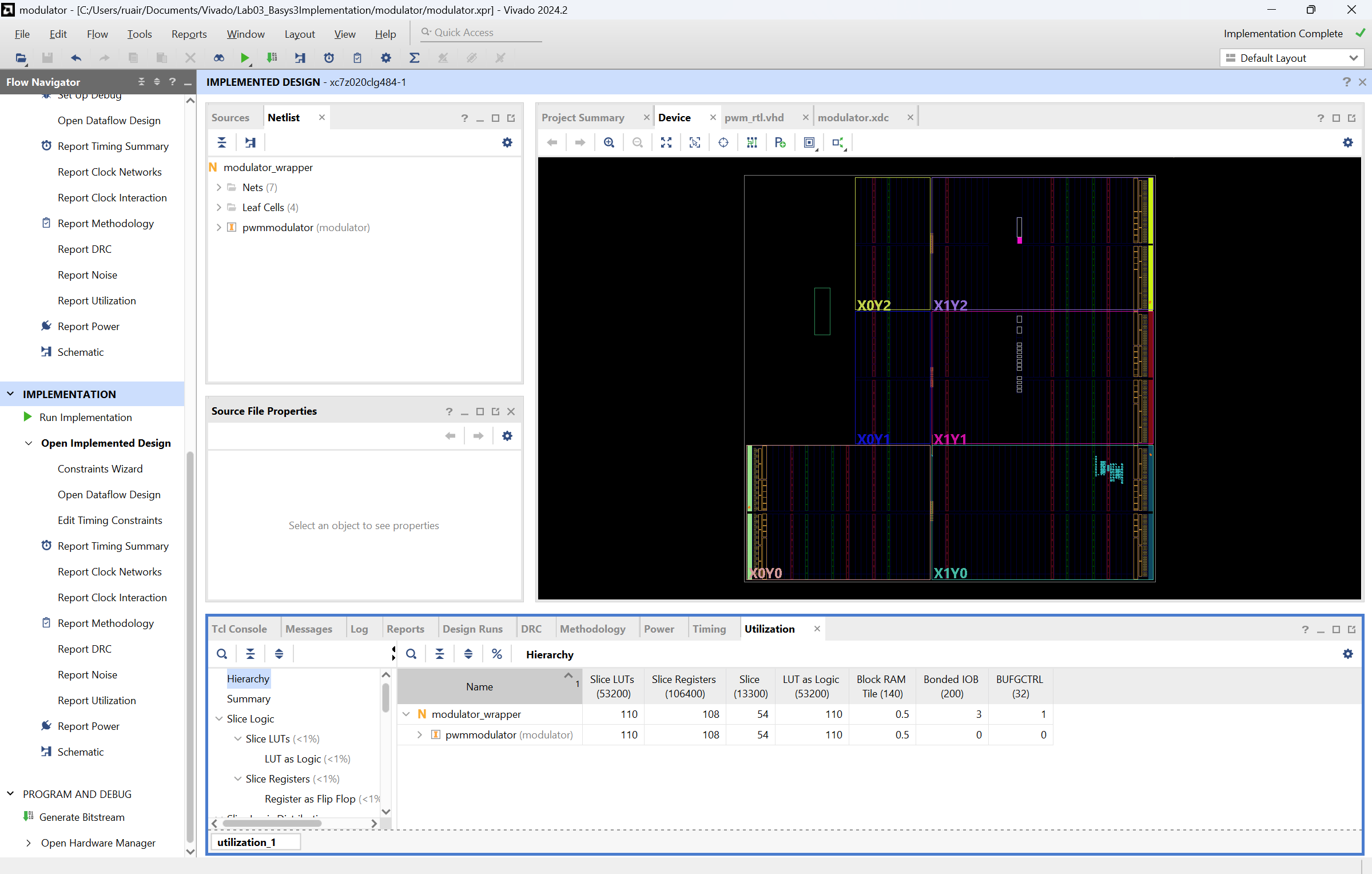
7000 series board support,

Board install from DIGILENT website

Syntax error in VDHL for running synthesis







The first 4 LEDs flash on almost instantly, the 5th LED flashes midway through ‘mississippi’ at about .5s, the 6th at 1 seconds, and the 7th at 1 seconds. Almost like the time taken to initialize is doubling every time.

0.03125(2^n) is the formula

LD1 is 0.03125s after LD0.

LD2 is 0.0625s after LD0.

LD3 is 0.125s after LD0.

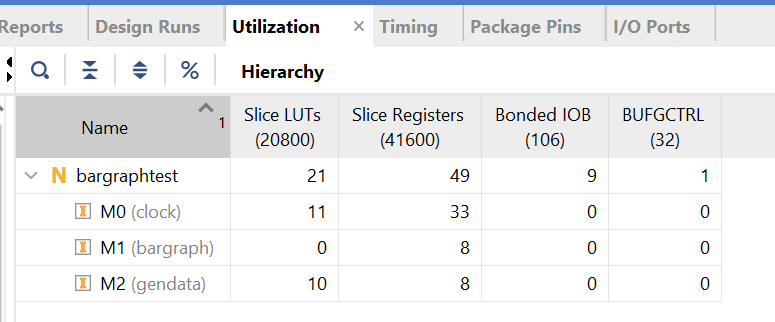
LD4 is 0.25s after LD0.

LD5 is 0.5s after LD0.

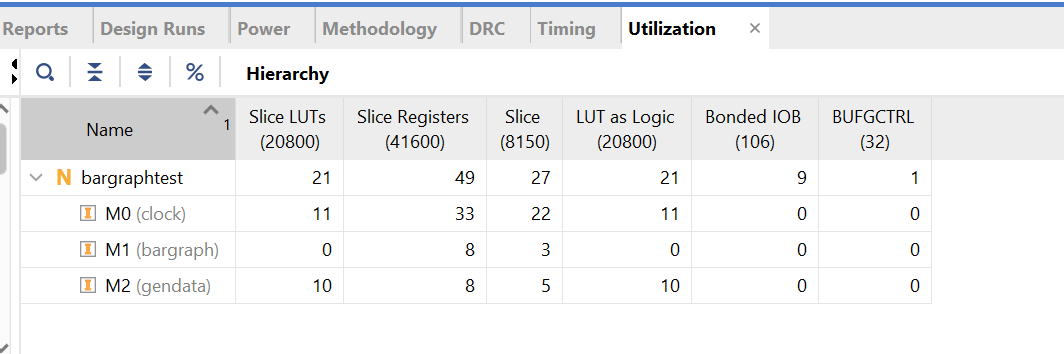
LD5 is 1s after LD0.

LD6 is 2s after LD0.

Synthesis Utilization:



Implementation Utilization:



56 in binary: 0000000000111000