SYSC4001

Lab1 Report

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When we do all the test for changing the save/restore context, with trace_5.txt as the input, the percentage of time it took between save/restore context and the total time increases. The higher the switching frequency or the cost per switch, the greater the system performance loss

$$t_1 = \frac{144 \cdot 10}{32738 + 52} \cdot 100 = 4.3915828$$

$$t_2 = \frac{144 \cdot 20}{34178 + 52} \cdot 100 = 8.413672217$$

$$t_3 = \frac{144 \cdot 30}{35618 + 52} \cdot 100 = 12.11101766$$

We vary the ISR activity time from between 40 and 200 (40,100,200). As ISR execution time increases, the system spends more time processing interrupts, while the execution time of ordinary CPU tasks is significantly compressed. Interrupt latency rises sharply, and user programs only get a very short execution time between interrupts.

$$t_1 = \frac{216 \cdot 40}{12978 + 52} \cdot 100 = 66.3085188$$

$$t_2 = \frac{216 \cdot 100}{25938 + 52} \cdot 100 = 83.10888803$$

$$t_3 = \frac{216 \cdot 200}{47538 + 52} \cdot 100 = 90.77537298$$

We varied the CPU burst time from between 100 and 1000 (100 400 1000), and from the output we observed that increasing the CPU burst time can improve CPU utilization, reduce switching and management overhead, and improve overall system efficiency.

$$t_1 = \frac{73 \cdot 100}{34736 + 100} \cdot 100 = 20.95533356$$

$$t_2 = \frac{73 \cdot 400}{56336 + 400} \cdot 100 = 51.46644106$$

$$t_3 = \frac{73 \cdot 1000}{99536 + 1000} \cdot 100 = 72.61080608$$

GitHub Link: ***https://github.com/Ruangfafa/SYSC4001_A1***