# Low Power Scheduling For High-Level Synthesis

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*Abstract*—Low power design has become a critical factor in the technical and commercial success of modern hardware systems. High Level Synthesis (HLS) involves transforming a behavioral description into a structural RTL-level netlist through scheduling, allocation, and binding [1] [2].The aim of this paper is to discuss integrated low power methods within the scheduling process of the HLS performed in [3]. The goal is to minimize switching activity and utilize low-power modules while meeting performance constraints, ultimately achieving a balance between size, performance, and energy efficiency. The scheduler discussed is known as the Power Scheduler [1] which identifies mutually exclusive operation paths, analyzes their activity profiles, and partitions them using a compatibility graph and clique search algorithm. Each resulting partition has a controlled activation or deactivation mechanism meaning they can be switched off when not used.

*Index Terms*—high level synthesis, scheduling, dynamic and static power, clique search algorithm.

## I. Introduction

This document is a model and instructions for LaTeX. Please observe the conference page limits.

## II. Related Work

## III. Fundamentals

### A. Conclusion

## Acknowledgment

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## References

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For papers published in translation journals, please give the English citation first, followed by the original foreign-language citation [?].

## References

[1] A. Rettberg, "Low Power Driven High-Level Synthesis for Dedicated Architectures," Phd Thesis, University of Paderborn, Paderborn, North-Rhein Westphalia, December 2006.

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[3] A. Rettberg and F. J. Rammig, "Integration of Energy Reduction into High-Level Synthesis by Partitioning," in IFIP International Federation for Information Processing, 2006, pp. 225-234.