

# Md Rubel Ahmed

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## SUMMARY

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- Developed frameworks for SoC trace mining
- Working knowledge of MIPS, RISC-V, x86 architectures
- Computer Architecture and FPGA design teaching experience

## EDUCATION

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<b>Ph.D. in Computer Science and Engineering</b> University of South Florida, Tampa, FL	<i>July 2023 (Exp.)</i> CGPA: 3.81/4.00
<b>M.S. in Computer Engineering</b> University of South Florida, Tampa, FL	<i>May 2022</i> CGPA: 3.91/4.00
<b>B.S. in Computer Science and Engineering</b> Khulna University of Engineering and Technology, Bangladesh	<i>March 2017</i> CGPA: 3.23/4.00

## TECHNICAL STRENGTHS

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<b>Programming Languages</b>	C/C++, Python
<b>EDA Tools</b>	Vitis HLS, Modelsim, Xilinx ISE Webpack, Vivado HLx
<b>Architectural Simulator</b>	Simplescalar, and gem5
<b>Miscellaneous</b>	Data Mining, Deep Learning, VHDL, Verilog, Z3 solver, Make, Git, Vim, Linux

## EXPERIENCE

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<b>Research Intern</b> Mitsubishi Electric Research Laboratories, Cambridge, MA	<i>Sept. 2022 - Present</i>
<ul style="list-style-type: none"><li>• Developed ML model for a target application</li><li>• High-Level Synthesis for ML models</li><li>• FPGA Development</li></ul>	
<b>Research Assistant</b> The SEES Lab, U. of South Florida, Tampa, FL	<i>August 2019 - August 2022</i>
<ul style="list-style-type: none"><li>• Instrumented and generated traces from SoCs modeled in VHDL, gem5, Rocket Chip Generator</li><li>• Developed an algorithm for automatic specification generation using data mining techniques</li><li>• Mentored Research Experience for Undergrad (REU) students</li></ul>	
<b>Course Instructor</b> University of South Florida, Tampa, FL	<i>May 2019 - July 2022</i>
<ul style="list-style-type: none"><li>• Computer Architecture (Summer 2022, 2019)</li><li>• Computer Architecture Lab (Summer 2022)</li></ul>	
<b>Teaching Assistant</b> University of South Florida, Tampa, FL	<i>August 2018 - July 2022</i>
<ul style="list-style-type: none"><li>• FPGA Design (Spring 2020)</li><li>• Computer Architecture (Fall 2019)</li><li>• System Integration and Architecture (Spring 2019)</li></ul>	
<b>Software Engineer</b> Synchronous ICT, Dhaka, Bangladesh	<i>Nov 2017 - July 2018</i>
<ul style="list-style-type: none"><li>• Worked on multimedia processing using FFMPEG.</li><li>• Developed data-driven cross-platform mobile app using React Native.</li></ul>	

## ACADEMIC/SIGNIFICANT PROJECTS

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- **>128 bit prime factorizer** : Designed FPGA implementation of prime factorizer for larger numbers >128 bit using VHDL and implemented on Zedboard.
- **Single Cycle Processor**: Designed a single cycle processor consisting of ALU, and multibank main memory in logisim.
- **Memory system performance analysis**: Analyzed memory system performance using gem5 simulator and 4 SPEC-CPU2000 benchmarks.
- **Addition and Multiplication matrix operations**: Designed an FSM controller to implement the multiplication and addition logic using Vivado and prototyped on Zed board.

## PUBLICATIONS

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**J2** Shuvo, Salman Sadiq; Symum, Hasan; **Ahmed, Md Rubel**; Yilmaz, Yasin; Zayas-Castro, Jose L, “Multi-Objective Reinforcement Learning Based Healthcare Expansion Planning Considering Pandemic Events”, IEEE Journal of Biomedical and Health Informatics (J-BHI, IF 7.021).

**J1 Md Rubel Ahmed**, Hao Zheng, Parijat Mukherjee, Mahesh C. Ketkar, Jin Yang, “Mining Patterns From Concurrent Execution Traces”, IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems (TCAD, h5 53).

**C6** Hao Zheng, **Md Rubel Ahmed**, Parijat Mukherjee, Mahesh C. Ketkar, Jin Yang, “Model Synthesis for Communication Traces of System Designs”, The 39<sup>th</sup> IEEE International Conference on Computer Design (ICCD’21).

**C5 Md Rubel Ahmed**, Hao Zheng, Parijat Mukherjee, Mahesh C. Ketkar, Jin Yang, “A Comparative Study of Specification Mining Methods for SoC Communication Traces” (ISVLSI’21).

**C4** Salman Sadiq Shuvo , **Md Rubel Ahmed**, Hasan Symum, Yasin Yilmaz, “Deep Reinforcement Learning Based Cost-Benefit Analysis for Hospital Capacity Planning”, International Joint Conference on Neural Networks (IJCNN’21).

**C3 Md Rubel Ahmed**, Hao Zheng, Parijat Mukherjee, Mahesh C. Ketkar, Jin Yang, “Mining Message Flows from System-on-Chip Execution Traces”, The 22<sup>nd</sup> International Symposium on Quality Electronic Design (ISQED’21).

**C2** Salman Sadiq Shuvo, **Md Rubel Ahmed**, Sadia Binta Kabir, Shaila Akter Shetu, “Application of Machine Learning Based Hospital Up-gradation Policy for Bangladesh”, 7<sup>th</sup> Int’l Conf. on Networking, Systems and Security (NSysS’20).

**C1** Amit Sutradhar, Md. Samiul Haque Sunny, Manash Mandal, **Rubel Ahmed**, “Design and construction of an automatic electric wheelchair: An economic approach for Bangladesh”, 2017 3<sup>rd</sup> International Conference on Electrical Information and Communication Technology (EICT’17).

## PREPRINTS

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**C2** Ahmed, Md Rubel and Zheng, Hao, “Deep Bidirectional Transformers for SoC Flow Specification Mining”, publisher: arXiv, 2022, doi:[10.48550/ARXIV.2203.13182](https://doi.org/10.48550/ARXIV.2203.13182)

**C1** Ahmed, Md Rubel and Nadimi, Bardia and Zheng, Hao, “Mining SoC Message Flows with Attention Model”, publisher: arXiv, 2022, doi:[10.48550/ARXIV.2209.07929](https://doi.org/10.48550/ARXIV.2209.07929).

## POSTERS/PRESENTATION

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**P7** Md Rubel Ahmed, Hao Zheng, “Model Synthesis for Communication Traces of Systems Designs”, WIP paper at 58<sup>th</sup> Design and Automation Conference (DAC), Dec. 2021.

**P6** Md Rubel Ahmed, Hao Zheng, “Model Synthesis for Communication Traces of System-on-Chip Designs”, USF Annual Graduate Research Symposium. Sept. 2021

**P5** Md Rubel Ahmed, Hao Zheng, “Mining Message Flows from SoC Execution Traces”, 57<sup>th</sup> Design and Automation Conference (DAC), Jun 2020.

**P4** Md Rubel Ahmed, Yuting Cao, Hao Zheng, “Specification Mining for SoC Validation using Data Mining Techniques”, 56<sup>th</sup> Design and Automation Conference (DAC), Jun 2019.

**P3** Md Rubel Ahmed, Yuting Cao, Hao Zheng, “Message Flow Mining for SoC Validation for Safe and Secure IoT Edge Node Design”, Warren B. Nelms Annual IoT Conference, Dec 2019.

**P2** Md Rubel Ahmed, Yuting Cao, Hao Zheng, “Execution Trace Mining for SoC Validation for Safe and Secure IoT Edge Node Design”, IFIP International Internet of Things Conference, Oct 2019.

**P1** Md Rubel Ahmed, Yuting Cao, Hao Zheng, “Specification Mining from Message Flows for SoC Validation”, 2019 FICS Research Conference on Cybersecurity, Mar 2019. doi: 10.1109/MDAT.2015.2499272

## PROFESSIONAL ACTIVITIES

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- Reviewed article for IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- Treasurer for IEEE-CS USF Student Chapter (2020 - 2022)
- Judge for 2021 USF Undergraduate Research Conference
- Registered volunteer for Meals on Wheels of Tampa
- Volunteer of IFIP IoT Annual Conference 2019

## AWARDS

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- USF Engineering Alumni Society Scholarship’22
- NSF travel grant for ISVLSI’21
- USF Student Govt. travel grant for ISQED’21
- Young Fellow (58<sup>th</sup> DAC, 2021)
- A. Richard Newton Young Student Fellowship award: 56<sup>th</sup>(2019) and 57<sup>th</sup>(2020) Design Automation Conference