PBL#17 Report: Sequence Detector (101)

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1. Introduction

In this report, we will explore the creation of a quad core pipelined design of a floating-point adder/multiplier/subtractor. The design uses submodules that incorporate a counter as a control flow for the pipelined adder, multiplier and subtractor. The design will take in 16 inputs at a time and process the data through the pipelined floating point operation submodules. Each group of inputs take 34 clock cycles to compute and produce a valid output.

2. Verilog HDL Design Code

Please see attached files for Verilog code.

3. Simulation Waveform

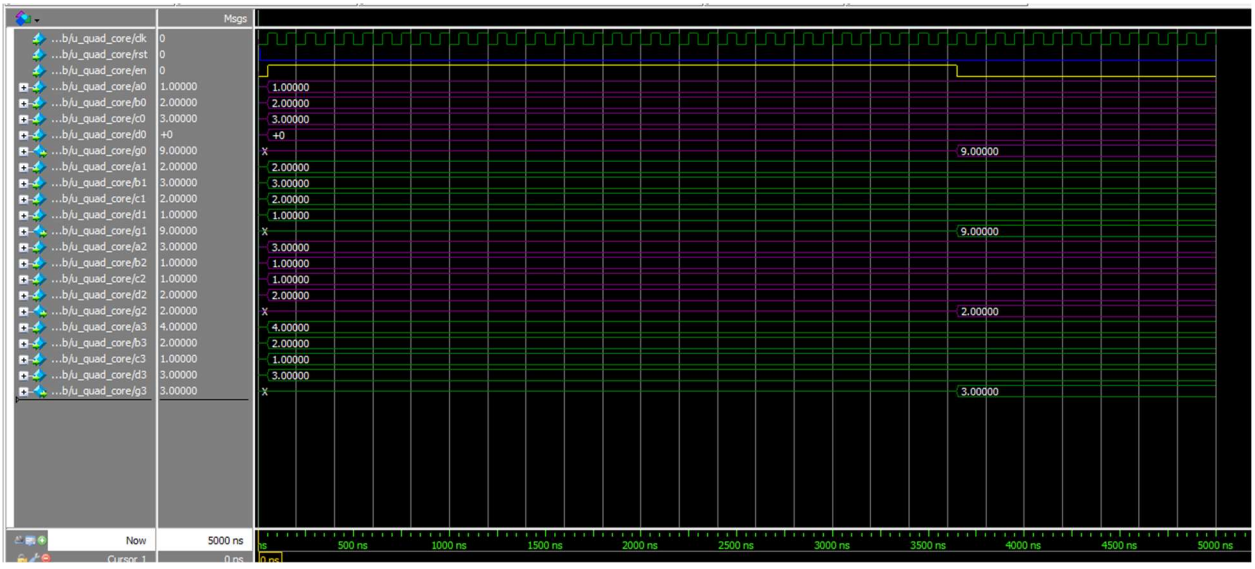

Figure 1: Waveform of quadcore pipeline design

4. Comments

The design functioned as intended from the description of a quadcore pipeline design. Each core handles the computation of a set of 4 inputs at a time and yields and output 34 clock cycles later.