PBL# 5 Report: SEQUENTIAL CIRCUIT DESIGN AND SIMULATION

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1. Introduction

In this report, we will explore the creation of a sequential circuit according to the design in figure 1. Our design incorporates two submodules of an and or gate design, an adder, and three Flip-Flop register with a falling edge reset and rising edge clock signal. The circuit will be designed to feature single-bit input ports denoted as a, b, c, d,e,f, g an asynchronous reset signal rst, a clock signal clk, and an output f.

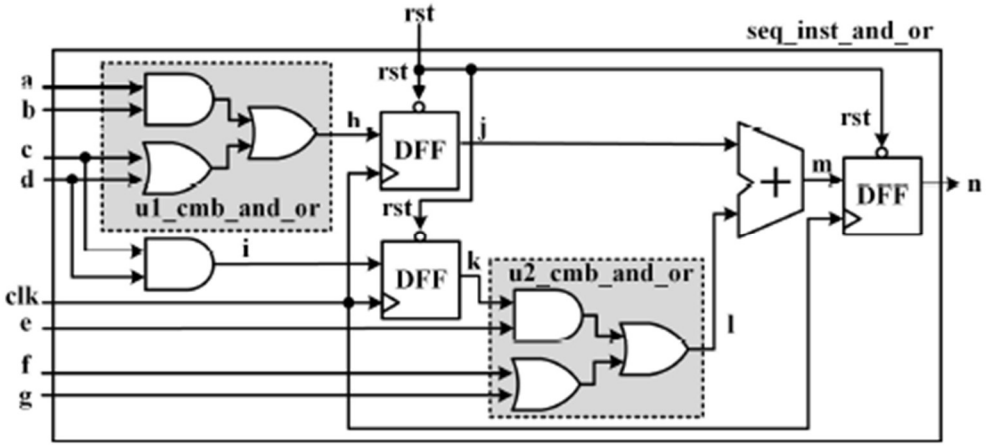

Figure 1: Sequential Circuit Instantiation

2. Verilog HDL Design Code

See attached files for verilog

3. Simulation Waveform

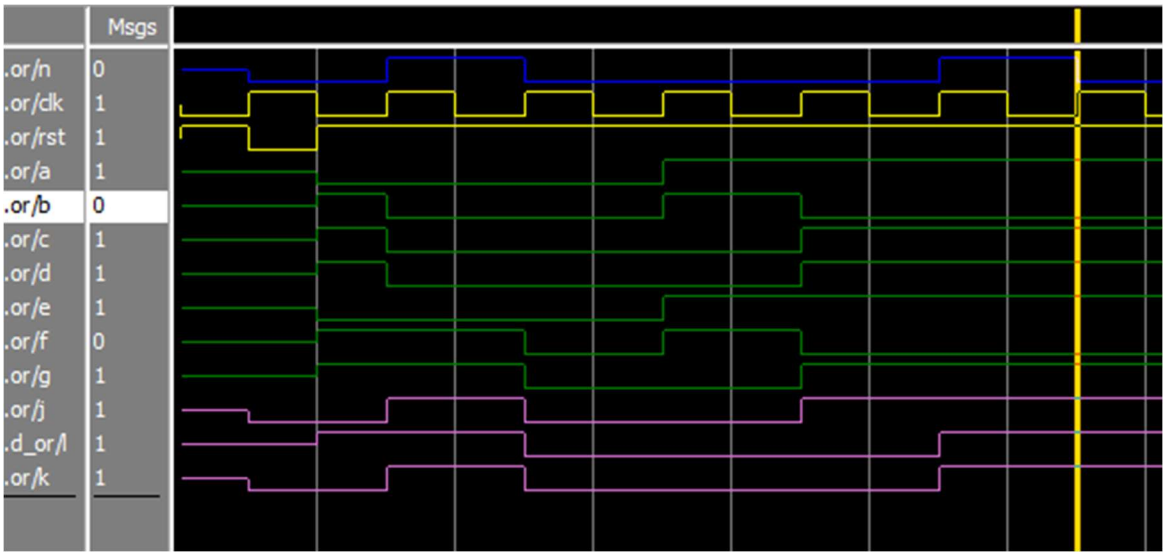

Figure 2: Waveform of Design testbench

4. Comments

This circuit behaved as expected with regards to the sequential circuit design in figure 1.