Circuit Theory and Electronics Fundamentals

MEAer (Integrated Master In Aerospace Engineering), Técnico, University of Lisbon

Laboratory 5: OP-AMP bandpass filter

Group 3

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1 Introduction

The objective of this laboratory assignment is to build a BandPass Filter (BPF) circuit whose specifications are: a central frequency at 1000Hz and a gain at central frequency of 40dB.

In order to achieve this, we used a selected number of components whose properties were predefined.

Our circuit is comprised of a μA741 OPAMP connected to two resistors, creating a non-inverting amplifier, and a combination of resistors and capacitors to take care of the filtering. These components are arranged according to figure 1 and their values shown in table 1.

The signal goes through a first stage where we have a capacitor whose function is to block unwanted DC current and to filter out lower frequencies, since the rest of the circuit is connected to the terminals of the resistor. Now the signal goes through a combination of resistors and a μ741 OPAMP. This arrangement creates a non-inverting amplifier. In this configuration, the output signal is "in-phase" with the input signal. Feedback control of the non-inverting OPAMP is achieved by applying a small part of the output voltage back to the inverting (-) terminal via Rx-Ry voltage divider network. And finally, the signal is subjected to a voltage divider network comprised of resistor Rz and capacitor C-ona. The desired voltage corresponds to the voltage drop at the terminals of the capacitor which, as a result, is subjected to a low pass filtering. For this to run, we need two supply DC voltage sources overlapped with our main circuit in order to power the transistors inside the OPAMP.

For this laboratory assignment there is a figure of merit, depending on the results obtained in the NGSpice simulation. This figure takes into account the cost of the components used, and the results they provide - a desirably low gain deviation and low central frequency deviation. The figure is calculated using the formula given by equation 1. The cost englobes the cost of transistors (0.1 units per transistor), resistors (1 unit per KOhm) and capacitors (1 unit per uF). The objective is to achieve the highest merit, so we tried different configurations of components data until we achieved our greatest figure of merit.

$$M = \frac{1}{Cost * (GainDeviation + CentralFrequencyDeviation + 10^{-6})} \tag{1}$$

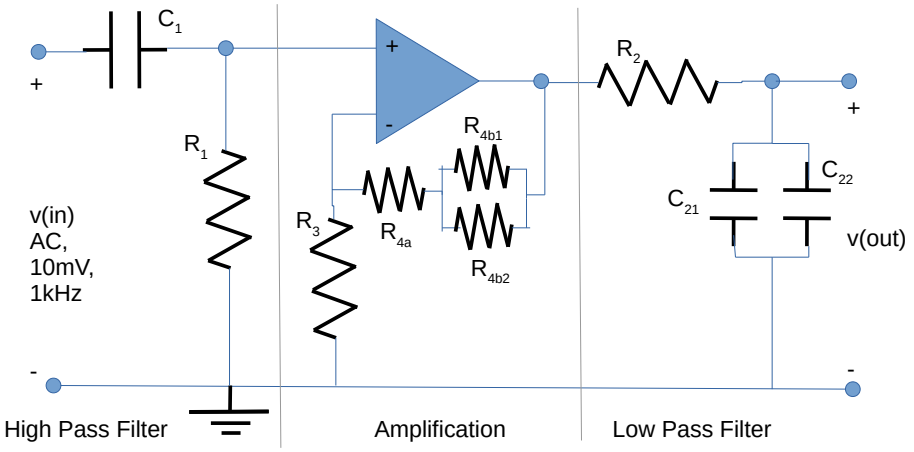

Figure 1: Geometry of our Audio Amplifier circuit.

To analyse this circuit theoretically we computed the transfer function for each stage in order to obtain the overall transfer function.

Name	Values
R_1	1.000000 kOhm
C_1	0.220000 uFarad
R_2	1.000000 kOhm
C_{21}	0.220000 uFarad
C_{22}	0.220000 uFarad
R_3	1.000000 kOhm
R_{4a}	100.000000 kOhm
R_{4b1}	100.000000 kOhm
R_{4b2}	100.000000 kOhm

Table 1: Values of the components used.

That being said, in Section 2 we present the theoretical models and calculations used to determine the transfer function and, therefore, the frequency response of the circuit, in Section 3 we introduce the results obtained in the simulation. Finally, in Section 4 we compare the two set of results, looking for possible discrepancies and we lay out our conclusions.

2 Theoretical Analysis

2.1 Circuit frequency response

With the following equations we determined both cutoff frequencies for the band pass circuit.

$$w_L = \frac{1}{R_1 C_1} \tag{2}$$

$$w_H = \frac{1}{R_2 C_2} \tag{3}$$

This was the definition used to determine the central frequency, which is meant to be 1KHz.

$$w_O = \sqrt{w_H w_L} \tag{4}$$

Name	Values
Lower Cut-Off Frequency	723.431560 Hz
Upper Cut-Off Frequency	1446.863119 Hz
Central Frequency	1023.086723 Hz

Table 2: Cut off frequencies and central frequency

The gain value peaks around the central frequency, at which point the output voltage is in phase with the input voltage.

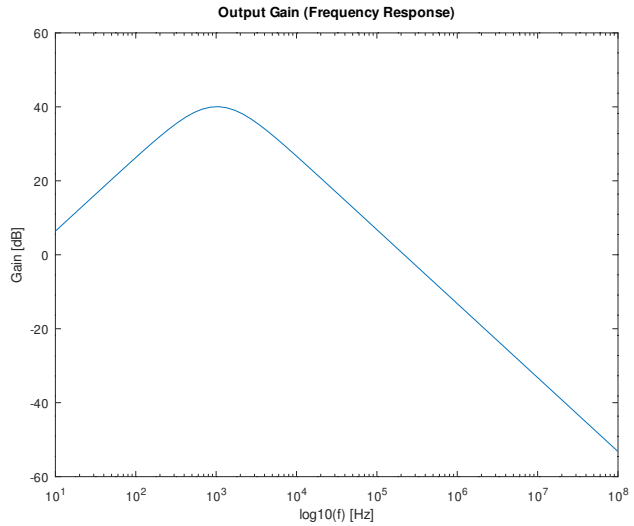

Figure 2: Voltage gain frequency response.

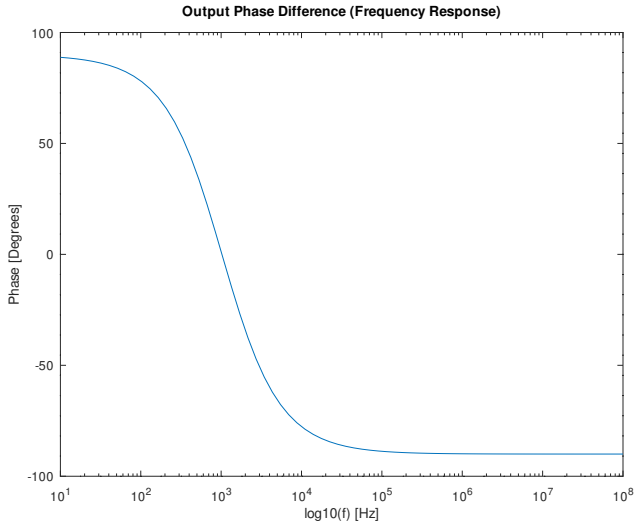

Figure 3: Voltage phase frequency response.

2.2 Central frequency results

For the mentioned central frequency we computed the circuit gain and input and output impedances for the amplifier. Also, we determined a theoretical figure of merit based on the predicted results with the set of values we chose. The gain value for the entire circuit is obtained by summing the individual gains (in decibels) of each of the three subcircuits. This is an ideal situation, where we don't take into account the loss of signal between stages. These are the equations for the gain values:

$$HighPassGain = \frac{R_1 C_1 j w_O}{1 + R_1 C_1 j w_O} \tag{5}$$

$$AmplifierGain = 1 + \frac{R_4}{R_3} \tag{6}$$

$$LowPassGain = \frac{1}{1 + R_2 C_2 j w_O} \tag{7}$$

Name	Values
Gain	100.666667
Gain (dB)	40.057714 dB
Z_{in}	1000.000000 -707.106781j Ohm
Z_{in} modulus	1224.744871 Ohm
Z_{in} phase	-35.264390 Degrees
Z_{out}	666.666667 -471.404521j Ohm
Z_{out} modulus	816.496581 Ohm
Z_{out} phase	-35.264390 Degrees
Cost	13626.952040MU
Merit	$3.089411*10^{-6}$

Table 3: Voltage gain of the different stages and input/output impedances of the amplifier.

3 Simulation Analysis

Since the input voltage source in this circuit is sinusoidal, the voltage and current values of the various components vary in time, and we are interested therefore in analysing how they evolve in time and obviously we want to picture the transformation of our AC input voltage source throughout the multiple stages of the circuit. We will run an operating point analysis in order to confirm the forward-active region of the two transisters, a transient analysis which will help us measuring the input and output impedances. We will also run a frequency response analysis in order to determine the gain and bandwidth of our output amplified sinusoidal signal. The transistors used were the Philips BJT's.

3.1 Operating point

We start with the operating point analysis. Given that the output signal will be solely sinusoidal, there isn't much relevance to this set of data. Its main goal is to confirm the forward-active region of both the npn and pnp transistors. In table **??** we present the operating point node voltages of the circuit. As expected, the voltage in nodes in e $in2$ since our source doesn't have a DC component. Our output signal doesn't have a linear voltage component, since the voltage in node out is zero, because the output coupling capacitor blocks the coming DC voltage. Regarding the npn transistor, the voltage drop must occur from the collector to the base, and from the base to the emitter - since $V_{coll} > V_{base} > V_{emit}$, this is confirmed. Looking to the pnp transistor, our collector node is ground, our base node is $coll$ and our emitter node is $emit2$. The voltage drop in this case must happen from the emitter to the collector. Since $V_{emit2} > V_{coll} > GND$, this is confirmed - both our transistors work in the pretended forward-active region.

3.2 Frequency response and impedances

We measured the input impedance of the circuit, seen through the perspective of the source, and the output impedance, seen through the perspective of our output (using a dummy test source). With the frequency response, we measured the voltage gain in our output. As we will see in figure **??**, the gain graph has the traits of a band-pass filter, letting pass medium frequencies (our source operates at a medium frequency), so we measure the in that zone. We also measured then the lower and upper cut-off frequencies of such graph, in order to determine the bandwidth of our amplifier. In table **??**, we present the results of our calculations. In figures **??**and **??** we can see the evolution of the gain throughout the circuit, first the gain

out of the gain stage - node $coll$ - and then the final gain, the gain out of the output stage - node out. With this figures we can confirm the band-pass filter trait of our circuit.

Analysing both the input and output impedances of the circuit, the input impedance is pretty satisfactory as it allows the vast majority of input voltage to go through the transistors, which means a low voltage loss. However, comparing the value of the output impedance with the load resistor, they are very much comparable. This means that part of the gain coming from the transistors will be consumed by some of our resistors in the circuit, hence losing a considerable part of the possible output gain. However, given the gain value we obtained, the overall result is very satisfying.

3.3 Final product and merit

In figure **??**, we can see the evolution of our AC signal from stage to stage until its final form. The output voltage has a null DC component as pretended, a symmetric phase in comparison to the input source (it's inverted) and a clear greater amplitude of approximately 0.55V, in comparison to the input's 10mV. We can say then that we have achieved the goal of amplifying our input signal, in this case, by 50-60 times! In table **??**, we present the cost and merit of our circuit. When looking to the parameters judged by the merit formula, we achieved an amazing bandwidth that clearly operates in the 20Hz-20kHz frequency band pretended, since we have an upper cut-off frequency in the zone of MHz, and a lower cut-off frequency inferior to 20Hz - $\approx$16Hz. The voltage gain could always be a bit higher, but without a defined pretended output amplitude, we can't really evaluate our achieved gain. Since we achieved a merit similar to 2326, the high cost seems like a reasonable price to pay for a circuit with these results. We were able however to achieve greater values of gain, but the output sinusoidal wave would be distorted, almost "cut-off" in its positive voltage periods, which was clearly not desirable, so we escaped from such happening, no matter the increase of gain it delivered.

4 Conclusion

Theoretical	**Value**	**Simulation**	**Value**
Operating point			
V_{vcc}	12 V	vcc[0]	1.200000e+01 V
V_{in}	0 V	in[0]	0.000000e+00 V
V_{in2}	0 V	in2[0]	0.000000e+00 V
V_{base}	1.876319 V	base[0]	1.878920e+00 V
V_{coll}	6.736022 V	coll[0]	7.214695e+00 V
V_{emit}	1.176319 V	emit[0]	1.184175e+00 V
V_{emit2}	7.436022 V	emit2[0]	8.033675e+00 V
V_{out}	0 V	out[0]	0.000000e+00 V
Frequency response and impedances			
$Gain$	158.174605	Gain	65.5843
$Gain(dB)$	43.982735 dB	Gain(dB)	36.336 dB
$LowerCut-offFreq$	20.432601 Hz	Lower cut-off freq	16.6025 Hz
$UpperCut-offFreq$	-	Upper cut-off freq	2.47423E+06 Hz
$Bandwidth$	-	Bandwidth	2.47421E+06 Hz
$InputImpedance$	729.020826 Ohm	Input impedance	0.856866 kOhm
$OutputImpedance$	3.619271 Ohm	Output impedance	8.18142 Ohm

Table 4: Comparison of the theoretical and simulated data results, regarding the operating point, frequency response and impedances.

In this laboratory assignment, we managed to build a BandPass Filter (BPF) circuit which is represented in Figure 1. The first step of our analysis was to determine the frequency response by computing the transfer function of the whole circuit.

The results from the theoretical and simulation analysis confirm that the transistors were operating in this region for each case. It should be noted that there is a small difference in the node voltages between the two analysis. For the theoretical analysis, we used the ideal transistor model, which is based on the ideal p-n diode model. In this model, we assumed the voltage drop happening on the base-emitter junction of the npn and pnp transistors while it is forwardly biased to be constant, VBEON=0.7. However, in reality, this value oscillates which is taken into account in NGspice. These errors can also be further enhanced by greater values of resistances, like the case of RC1.

In the second part of our analysis, we set off to determine the incremental values of the circuit in order to compute its frequency response, as well as its output gain and input/output impedances. According to Table 11, the discrepancy between the simulation and theoretical values is more significant, particularly in the gain . According to the small signal models, the incremental variables of the transistors depend upon its operating point. Therefore, we can assume the errors committed in the operating point analysis to have been carried to the computation of the Gain and frequency response. These calculations were derived from the Ebers-Moll model which does not consider non-ideal effects such as the base-width modulation and recombination in the depletion region. These effects break the linear relationship between the transistor values assumed in the theoretical analysis. Another very important cause is the approximation for high frequencies that we used for the capacitors, which neglets their effect (they become short-circuits). Given that we are studying medium frequencies, this a major source of error in our theoretical analysis, since it disregards the capacitors' impedances, in order to simplify calculations. The exception to this was the frequency response analysis, which did produce more accurate results, even though they were still visually different from the simulated ones, due to other factors.

Despite the discrepancies that have been exposed, it should be noted that both analyses yielded satisfactory results for the input and output impedances. The values for the input impedance are approximately 729 Ohm (theoretical) and 857 Ohm (simulation). Despite the error of 18 percent, the value obtained for the real input impedance is still acceptable given the fact that the typical range for professional microphone output impedances is 50-500 Ohms. Therefore, our circuit would be suitable as a microphone amplifier. This same comment can be applied to the output impedance of our circuit. Both theoretical and simulation values land within the typical range for speaker impedance. In the case of this assignment, our circuit is perfectly suitable for the 8 Ohm speaker. Furthermore, when it comes to the frequency response of the circuit, as for the lower cut-off frequency, the values obtained matched perfectly. However, we didn't manage to obtain a value for the higher cut-off frequency within the selected spectrum in the theoretical analysis. This can be explained by the fact that we disregarded the transistor's internal capacitances in the calculations. That is not the case in the simulation. NGspice accounts for all the variables of the transistor and, therefore, we obtained an upper cut-off frequency of 2.47423+06 Hz. With this, we managed to obtain a circuit that can clearly operate in the 20Hz-20kHz frequency band, making it perfect as an amplifier.