TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

MEAer (Integrated Master In Aerospace Engineering), Técnico, University of Lisbon

Laboratory 3: AC/DC Converter Circuit

Group 3

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May 8, 2021

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1 Introduction

The objective of this laboratory assignment is to build an AC/DC converter. The architecture we implemented was a full bridge rectifier for the Envelope Detector and a limiter with a resistor in the regulator circuit. Below we will compare the theoretical and simulation data of the following circuit.

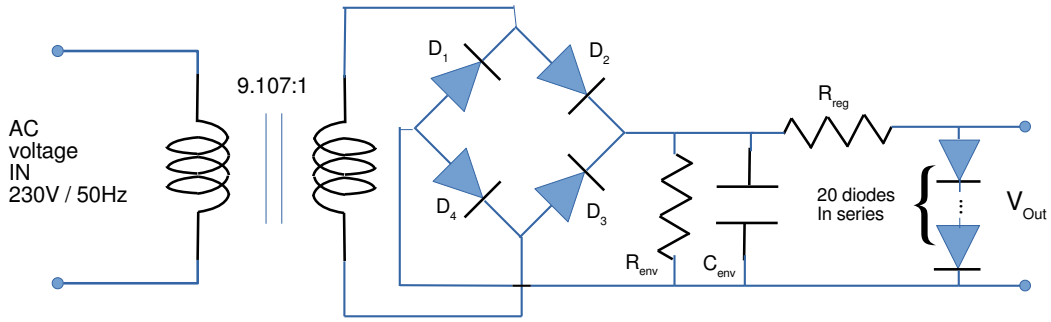

Figure 1: ACDC converter circuit.

2 Theoretical Analysis

In this section we analyse the architecture chosen for the ACDC converter circuit using an Octave theoretical model. Using the ideal diode model we were able to predict the output of the Envelope Detector and Voltage Regulator circuits.

2.1 Envelope Detector

Below are the values we chose for the number of coils in the transformer and for the components of the envelope detector circuit. Due to the transition regime, that turned out to be quite

Name	Value
R	900000.000000 Ohm
C	0.000900 Farad
Number of Coils	9.107000

Table 1: Initial values for the input voltage and circuit components.

lengthy, we opted to start the study of the circuit after a period of 3.8 seconds in order to have a stabilized response The voltage at the output of the envelope detector circuit was then plotted

as follows. As expected, we see a positive voltage oscillating up to a maximum voltage equal

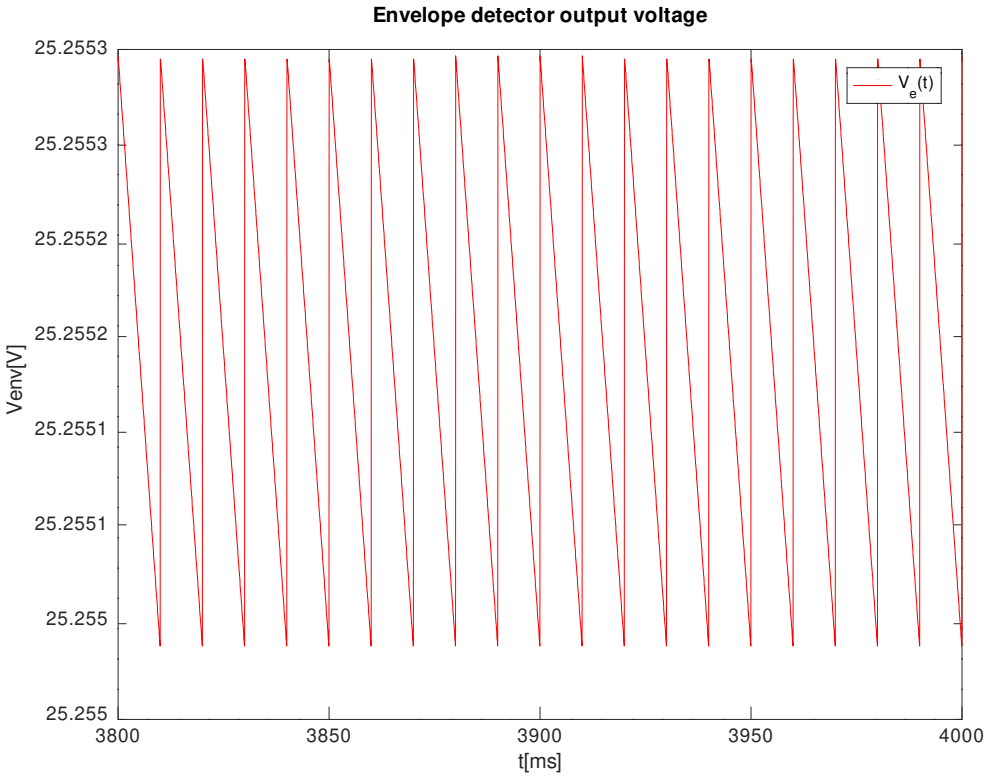

Figure 2: Voltage envelope detector circuit output.

to the initial 230V divided by the number of coils: 25.2553V. Already we are close to a direct current regime, but the voltage level and the magnitude of the ripple still need to be addressed and adjusted.

2.2 Voltage Regulator

We used incremental analysis in order to determine the equivalent diode resistance, using the following formula.

$$R_d = \frac{\eta * V_T}{I_s * e^{(\frac{V_d}{\eta * V_T})}} = 247.05; \tag{1}$$

This way we knew we needed a resistance value much greater than the diode incremental resistance. Below are the values we chose for the resistor and diode layout.

Name	**Value**
Rreg	100000.000000 Ohm
Number of Diodes	20.000000

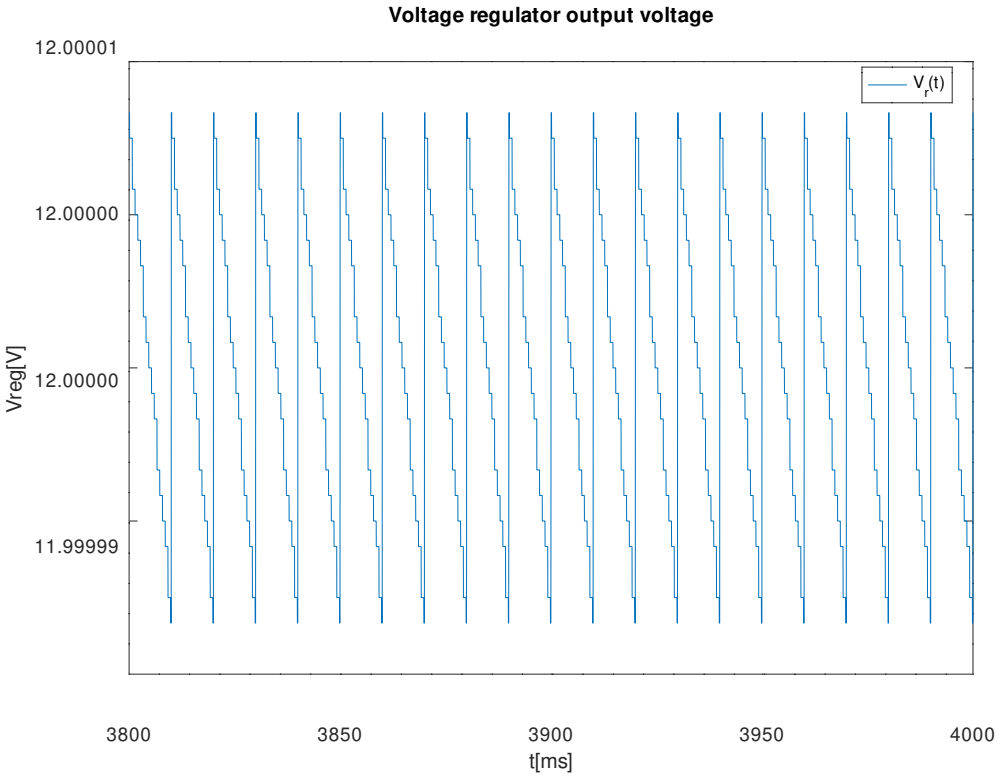

Figure 3: Voltage regulator circuit output.

3 Simulation Analysis

Since this circuit has a sinusoidal voltage source, the voltage and current values of the various components vary in time. Therefore, we must perform a transient analysis to simulate the circuit's total response. We also ran operating point analysis for both $t < 0$ and $t = 0$ to determine what the initial conditions were and establish the boundary conditions. Finally, we ran a frequency response analysis of the capacitor voltage and node 6 voltage.

3.1 Operating Point Analysis

The tables below show the simulated operating point results for both $t < 0$ (where we assume no current is flowing through the capacitor) and t=0 where we shut down the voltage source V_s and we replace the capacitor with a voltage source V_x, in order to determine the equivalent resistor seen through the capacitor.

Table shows the simulated node voltages and branch currents for $t < 0$. Table **??** gives us the current flowing through our voltage source, V_x. With the voltage source value calculated in the previous operating poing simulation, we can now calculate the equivalent resistance, R_{eq}, and characteristic time, τ:

$$R_{eq} = \frac{V_x}{@V_c[i]} \Leftrightarrow R_{eq} = \frac{8.548722}{2.80822e-03} \Leftrightarrow R_{eq} = 3044.178163Ohm$$

$$\tau = R_{eq} \times C \Leftrightarrow \tau = (3044.178163 * C)s$$

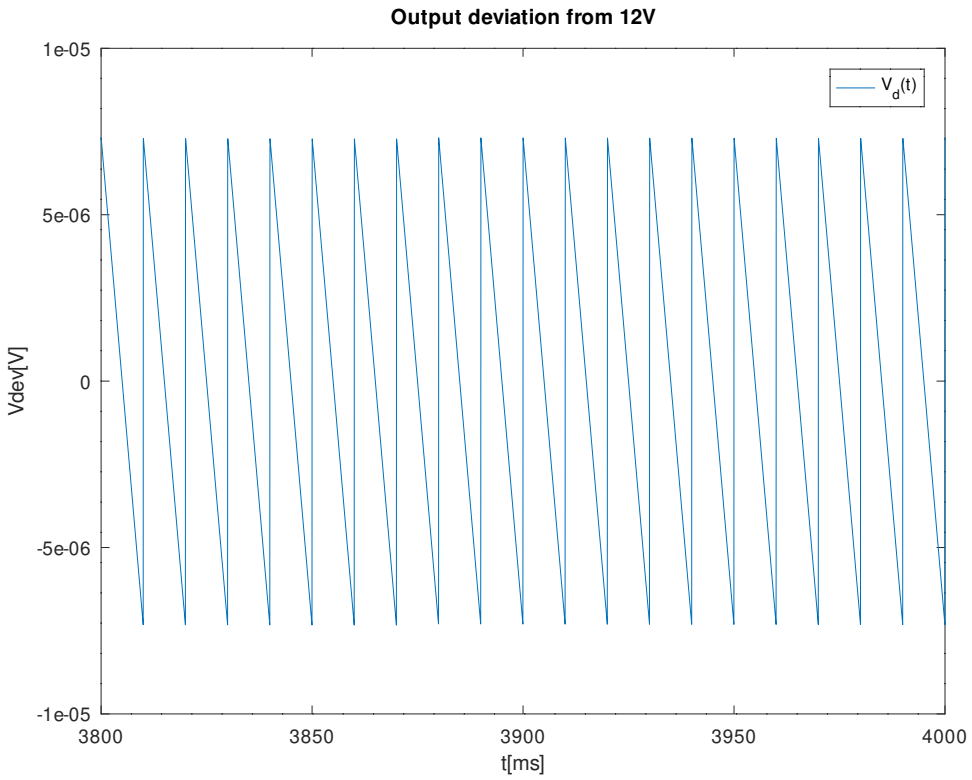

Figure 4: Circuit output without the DC component.

3.2 Natural response

In this section we simulate the natural response of the circuit in the [0,20] ms time interval using the transient analysis simulation in NGSpice and the computations from the previous section.

3.3 Natural and forced response

We repeat the previous step now with the sinusoidal voltage source $V_s(t)$ considering a frequency of 1kHz. Below is the plot for both the stimulus and the response:

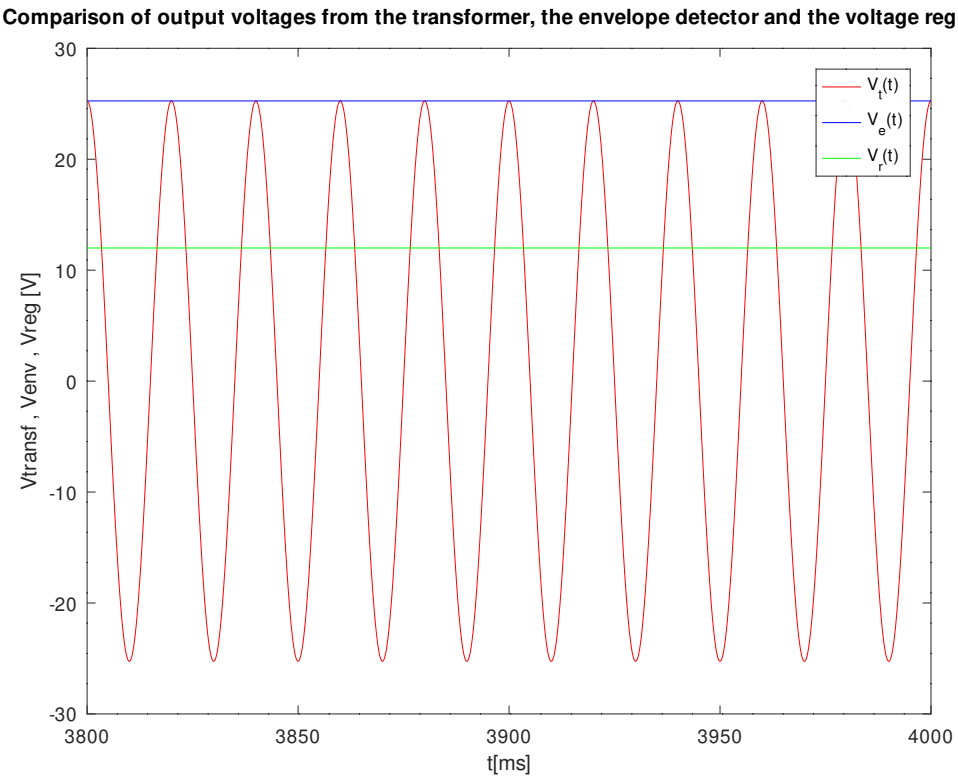

Figure 5: Comparison between the different voltage outputs.

3.4 Frequency response

We simulated the frequency response to the voltage source V_s, both in node 6 and in the capacitor itself, in NGSpice, and we plotted the magnitude, in dB, and phase, in degrees, of the three voltages in relation of course to a variation of frequency. The frequency varies from 0.1 Hz to 1MHz. Analysing figures **??** and **??**, they confirm what we foresaw in the theoretical analysis. The various reasons on why certain voltage parameters vary or are equivalent are laid out and explained in the $Frequency\ Response$ subsection of the theoretical analysis.

4 Conclusion

Now, we proceed to compare our theoretical and simulation results. Looking at all plots generated either by GNU Octave or NGSpice, the theoretical plots are checked out by NGspice with very high precision (plots relative to the natural solution, the complete solution and the frequency responses). When it comes to the tables generated by the operating point analysis regarding $t < 0$ and $t = 0$, we have assembled a table comparing the theoretical analysis run by Octave and the simulated data from NGSpice (Table **??**).

All compared figures are equal, if we discard effectuated roundings, mostly operated by Octave, and if we disregard differences in the number of significant algharisms presented by both softwares. In the final case of the equivalent resistance, R_{eq}, the error is bigger because we calculated it not using either of the softwares (we took the V_x and I_x data from NGspice and operated the division ourselves). All comparisons made, all results predicted in the theoretical section were matched by the simulations executed.

All things taken into account, in this laboratory assignment, we were successful in producing coherent calculations using the Octave Maths tool and the circuit simulation, done using the Ngspice tool. Static and transient analysis were performed both theoretically and using a circuit simulation. Some results in the simulation that were predicted to yield zero current or voltage were actually very slightly off - in the magnitude of 1e-15, a similar magnitude to the floating number precision used in the software we utilised, which shows these errors are most likely due to roundings effectuated either by GNU Octave or NGSpice in their calculations, most specifically in linear systems. This could also be do to the writing and reading of the different text files truncating the numbers at specific decimal places. The whole report has been automatised and we're confident that it would yield consistent results with a new set of data.