Circuit Theory and Electronics Fundamentals

MEAer (Integrated Master In Aerospace Engineering), Técnico, University of Lisbon

Laboratory 3: AC/DC Converter Circuit

Group 3

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Contents

1 Introduction

The objective of this laboratory assignment is to build an AC/DC converter. The AC voltage goes through a transformer in order to reduce its amplitude. The AC voltage is then processed by an envelope detector composed of a full bridge wave rectifier and a capacitor. The full wave rectifier is composed by 4 diodes and a resistor (the load): the diodes allow the AC voltage to always pass to the resistor, no matter the direction of the current. Combining this with a capacitor will allow the sinusoidal character of the input voltage to be diminuished, oscilating then around its amplitude value. After this, the new input voltage goes through a voltage regulator, which is composed by a resistor and a limiter - a series of diodes. The resistor will decrease the voltage ripple (oscilation) and the limiter will make sure the DC component of our voltage is the pretended one - 12V - allowing us a pretty much linear output voltage of 12V, ready to be used by many of our home electronical gadgets. For this laboratory assignment there is a figure of merit, depending on the results obtained in the NGSpice simulation. This figure takes into account the cost of the components used, and the results they provide - a desirable low voltage ripple and an ideal average for the DC component of 12V. The figure is calculated using the formula given by equation 1. The cost englobes the cost of diodes (0.1 units per diode), resistors (1 unit per KOhm) and capacitors (1 unit per uF). The objective is to achieve the highest merit, so we tried different configurations of components data until we achieved our greatest figure of merit.

$$M = \frac{1}{cost * [ripple(V_O) + |average(V_O - 12)| + 10^{-6}]} \tag{1}$$

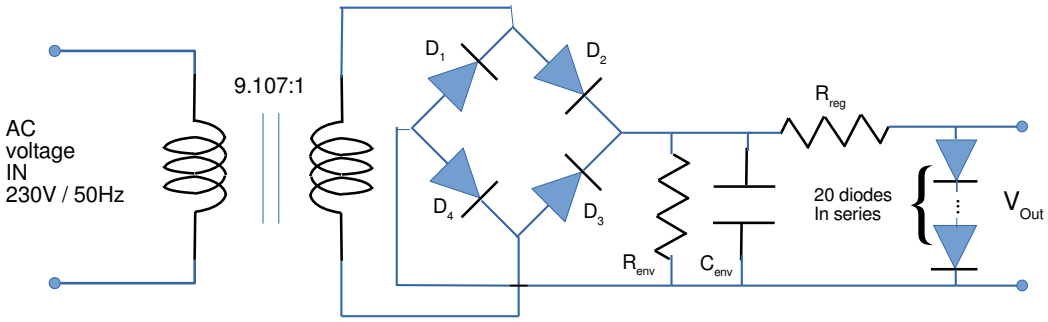

Figure 1: Geometry of our AC/DC converter circuit.

To analyse this circuit theoretically we will use the ideal diode model for the full wave bridge rectifier and the incremental diode model in the voltage regulator. We will compare this results with the ones obtained in the NGSpice simulation. That being said, in Section 2 we present the various theoretical models and calculations used to determine the output voltage, in Section 3

we introduce the results obtained in the simulation. Finally, in Section 4 we compare the two set of results, looking for possible discrepancies and we lay out our conclusions.

In Table 1, we list the numeric values of the components used.

Name	**Values**
Number of Coils	9.107000
R_{env}	900.000000 KOhm
C_{env}	900.000000 uFarad
R_{reg}	100.000000 KOhm
Number of Diodes in Limiter	20.000000

Table 1: Components numeric values used in our analysis and simulation.

2 Theoretical Analysis

In this section we analyse the architecture chosen for the ACDC converter circuit using an Octave theoretical model. Using the ideal diode model we were able to predict the output of the Envelope Detector and Voltage Regulator circuits.

2.1 Envelope Detector

Below are the values we chose for the number of coils in the transformer and for the components of the envelope detector circuit. Due to the transition regime, that turned out to be quite

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C_{env}	900.000000 uFarad
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Table 2: Initial values for the input voltage and circuit components.

lengthy, we opted to start the study of the circuit after a period of 3.8 seconds in order to have a stabilized response The voltage at the output of the envelope detector circuit was then plotted as follows. As expected, we see a positive voltage oscillating up to a maximum voltage equal to the initial 230V divided by the number of coils: 25.2553V. Already we are close to a direct current regime, but the voltage level and the magnitude of the ripple still need to be addressed and adjusted.

2.2 Voltage Regulator

We used incremental analysis in order to determine the equivalent diode resistance, using the following formula.

$$R_d = \frac{\eta * V_T}{I_s * e^{(\frac{V_d}{\eta * V_T})}} = 247.05; \tag{2}$$

This way we knew we needed a resistance value much greater than the diode incremental resistance. Below are the values we chose for the resistor and diode layout.

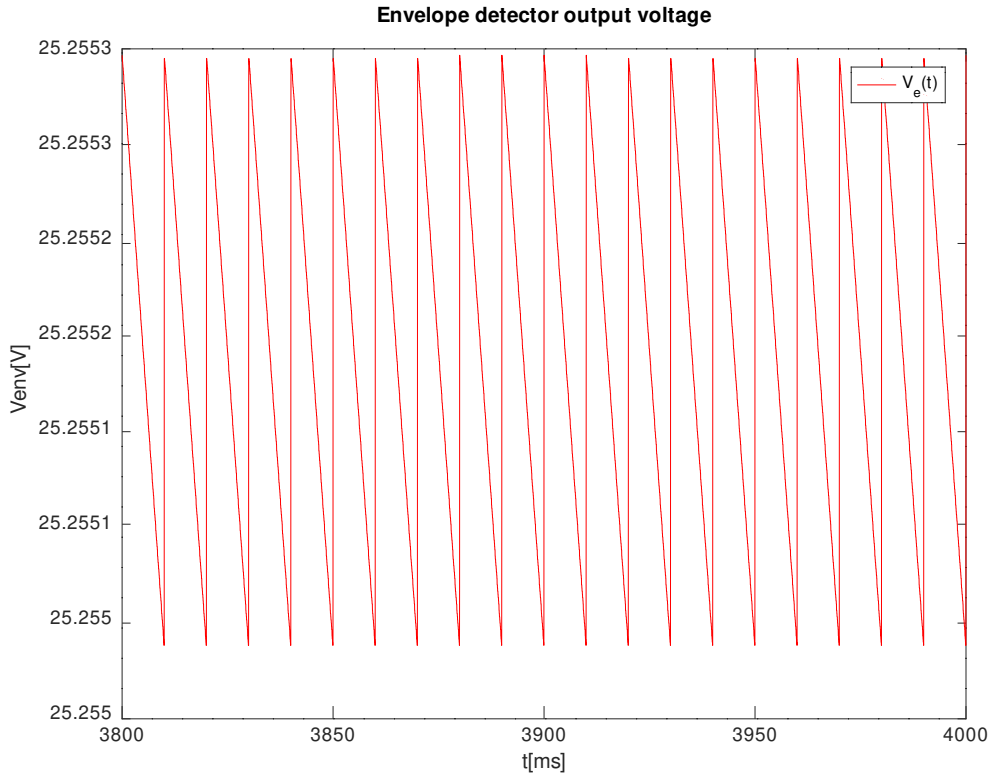

Figure 2: Voltage envelope detector circuit output.

Name	Value

3 Simulation Analysis

Since the input voltage source in this circuit is sinusoidal, the voltage and current values of the various components vary in time, and we are interested therefore in analysing how they evolve in time and obviously we want to picture the transformation of our AC input voltage source throughout the multiple stages of the circuit. Therefore, we will run a single transient analysis for this circuit, lasting 10 periods of the voltage source. For this simulation we are not taking the natural solution into account, only the forced one. In our simulation we came across a large transitional period of roughly 4 seconds, until the output voltage source stabilized enough in the envelope detector, so we only account for data after this period, [3.8 ; 4.0]. This is due to the natural solution of the voltage and its downfall effects will be aproached in our conclusions. We used the default diode model of NGSpice in this simulation and we saw no need of introducing a transformer since it only reduces the amplitude of the voltage source, so we applied the AC voltage output of the transformer as our input voltage source of the circuit.

3.1 Envelope Detector Output Voltage

In figure 6 we present the plot of the envelope detector output voltage throughout 10 periods, and in table 3 we introduce the average voltage (approximate DC component) and the voltage ripple of such voltage. Since the objective lies in the output of the regulator, this set of data isn't of much relevance.

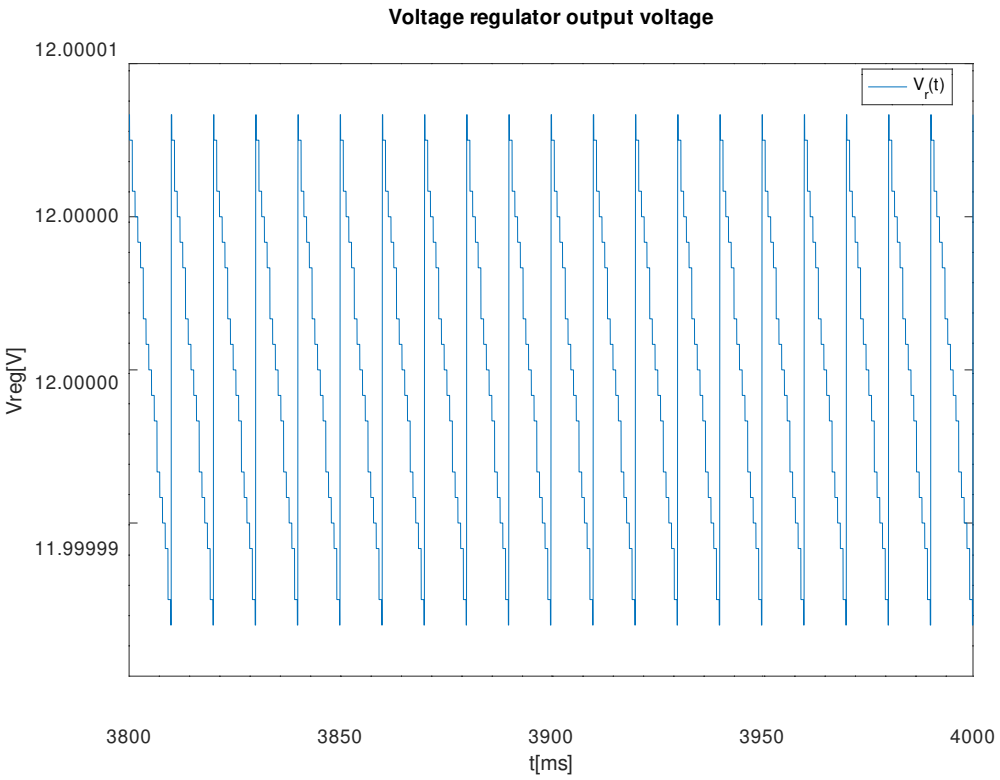

Figure 3: Voltage regulator circuit output.

Name	Values [V]
envelopeaverage	2.387308e+01
enveloperipple	1.480000e-03

Table 3: Envelope Detector Output Voltage characteristics.

3.2 Voltage Regulator Output Voltage - The output of the circuit

Now, in figure 7 we present the plot of the voltage regulator output voltage throughout the same 10 periods, and in table 4 we introduce the average voltage (approximate DC component) and the voltage ripple of such voltage. This is indeed our desired output voltage for the circuit, so its average and ripple are very important data. In this case, we managed a average output voltage that only differs from 12V in its last significant algharism, and a voltage ripple in the order of the uV, which seems to us a pretty satisfactory result.

Name	Values [V]
outputaverage	1.200005e+01
outputripple	6.000000e-05
merit	4.735602e+00

Table 4: Voltage Regulator Output Voltage characteristics, and figure of merit.

In figure 8 we are able to get a closer look to the slight deviations from the desired linear 12V in our output, and in figure 9 we compare the input voltage source post-transformer, the output of the envelope detector, and our final output - the voltage regulator output voltage. In this figure we can see the linear character of the voltage post-envelope detector, opposed to its sinusoidal form after the transformer, so the envelope did its job in annihilating the sinusoidal wave form. Then, we can see that our final output voltage maintains this linear (DC) trait, even

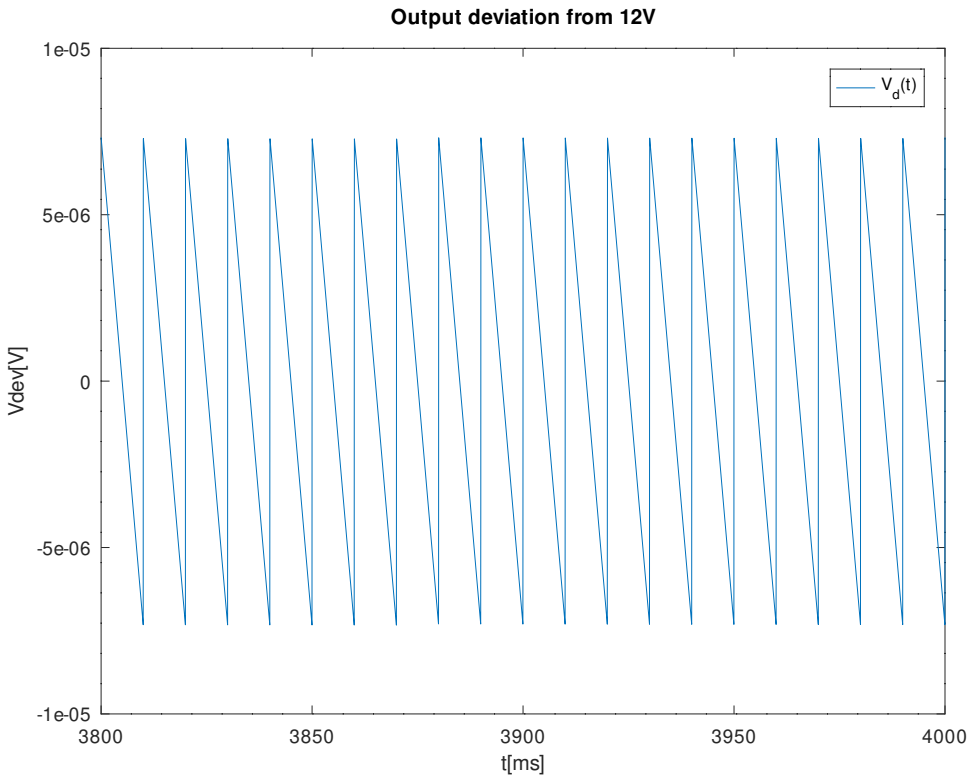

Figure 4: Circuit output without the DC component.

improving on it thanks to the resistor, and it is now at the desired 12V fruit of the action of our limiter, the 20 diodes in series.

Going back to table 4, we calculated the figure of merit for this configuration, and obtained a value close to 5. The value could have been higher if the average of the output voltage were a straight 12V, which is not the case. Another way to increase the merit would have been to diminuish our ripple by increasing our resistors and capacitor values. Even though we would be increasing our cost, the decrease of the ripple would have an even bigger effect than that of the cost, increasing our merit. However, we noticed this could come at the cost of a even bigger transitional period, which is not a good model for an AC/DC converter, since it is impractical to wait more than 5 seconds for the conversion to take place in an effective manner. A way to decrease this transitional period could come in the form of increasing the input voltage source coming from the transformer, but that would require an even bigger resistance in the regulator to help bring that value down (we're using the default diode model, not the theoretical ideal one)... Final notes on the figure of merit topic will be approached in our conclusions.

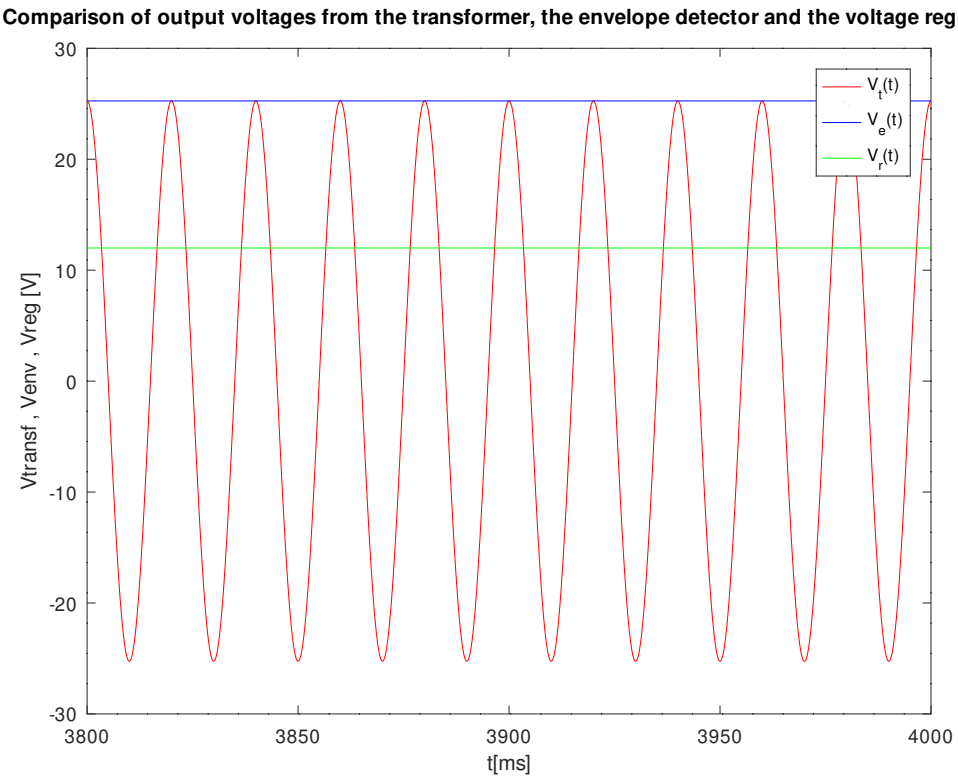

Figure 5: Comparison between the different voltage outputs.

4 Conclusion

Now, we proceed to compare our theoretical and simulation results. Looking at all plots generated either by GNU Octave or NGSpice, the theoretical plots are checked out by NGspice with very high precision (plots relative to the natural solution, the complete solution and the frequency responses). When it comes to the tables generated by the operating point analysis regarding $t < 0$ and $t = 0$, we have assembled a table comparing the theoretical analysis run by Octave and the simulated data from NGSpice (Table **??**).

All compared figures are equal, if we discard effectuated roundings, mostly operated by Octave, and if we disregard differences in the number of significant algharisms presented by both softwares. In the final case of the equivalent resistance, R_{eq}, the error is bigger because we calculated it not using either of the softwares (we took the V_x and I_x data from NGspice and operated the division ourselves). All comparisons made, all results predicted in the theoretical section were matched by the simulations executed.

All things taken into account, in this laboratory assignment, we were successful in producing coherent calculations using the Octave Maths tool and the circuit simulation, done using the Ngspice tool. Static and transient analysis were performed both theoretically and using a circuit simulation. Some results in the simulation that were predicted to yield zero current or voltage were actually very slightly off - in the magnitude of 1e-15, a similar magnitude to the floating number precision used in the software we utilised, which shows these errors are most likely due to roundings effectuated either by GNU Octave or NGSpice in their calculations, most specifically in linear systems. This could also be do to the writing and reading of the different text files truncating the numbers at specific decimal places. The whole report has been automatised and we're confident that it would yield consistent results with a new set of data.

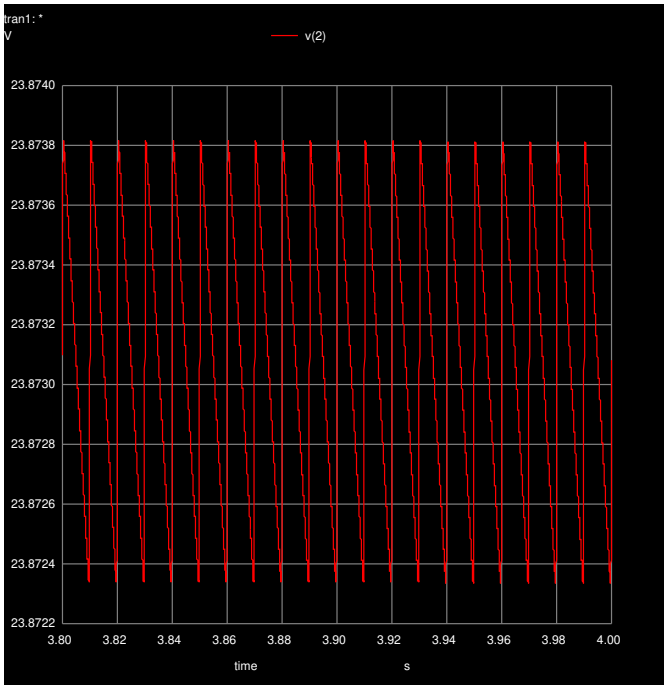

Figure 6: Simulated output voltage in the envelope detector.

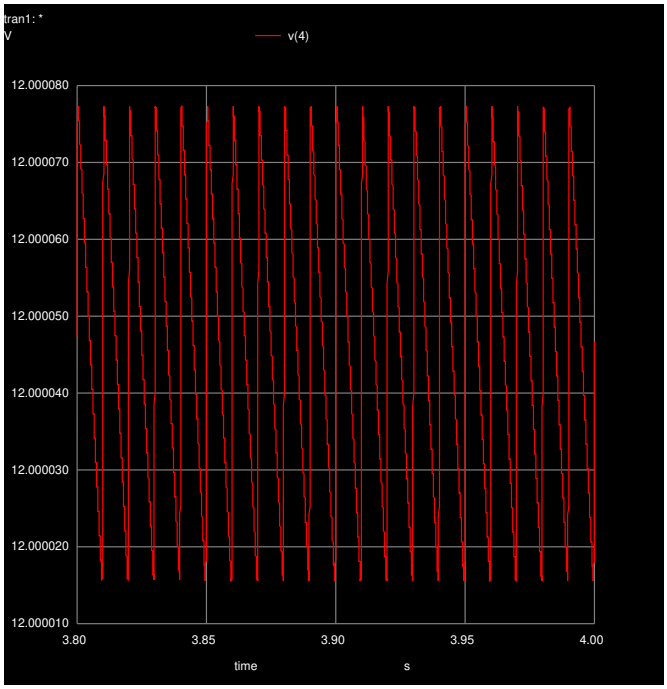

Figure 7: Simulated output voltage in the voltage regulator.

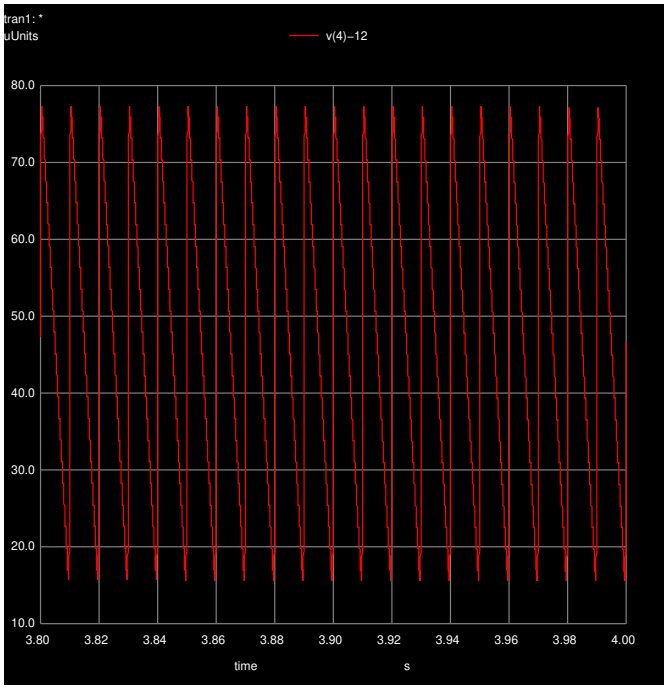

Figure 8: Deviation from 12V of the output voltage in the voltage regulator.

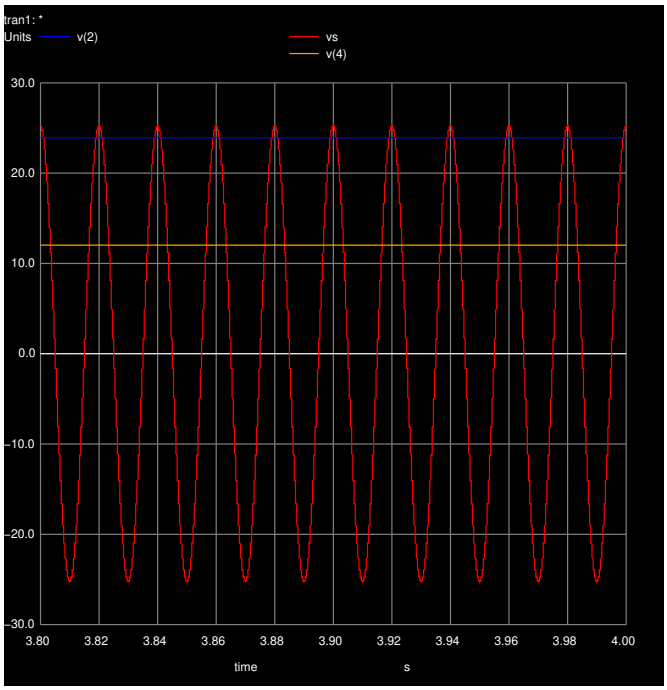

Figure 9: Comparison of the simulated input voltage source (after transformer), the envelope detector voltage and, finally, the voltage regulator voltage, our output.