Circuit Theory and Electronics Fundamentals

MEAer (Integrated Master In Aerospace Engineering), Técnico, University of Lisbon

Laboratory 3: AC/DC Converter Circuit

Group 3

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1 Introduction

The objective of this laboratory assignment is to build an AC/DC converter. The AC voltage goes through a transformer in order to reduce its amplitude. The AC voltage is then processed by an envelope detector composed of a full bridge wave rectifier and a capacitor. The full wave rectifier is composed by 4 diodes and a resistor (the load): the diodes allow the AC voltage to always pass to the resistor, no matter the direction of the current. Combining this with a capacitor will allow the sinusoidal character of the input voltage to be diminuished, oscilating then around its amplitude value. After this, the new input voltage goes through a voltage regulator, which is composed by a resistor and a limiter - a series of diodes. The resistor will decrease the voltage ripple (oscilation) and the limiter will make sure the DC component of our voltage is the pretended one - 12V - allowing us a pretty much linear output voltage of 12V, ready to be used by many of our home electronical gadgets. For this laboratory assignment there is a figure of merit, depending on the results obtained in the NGSpice simulation. This figure takes into account the cost of the components used, and the results they provide - a desirable low voltage ripple and an ideal average for the DC component of 12V. The figure is calculated using the formula given by equation 1. The cost englobes the cost of diodes (0.1 units per diode), resistors (1 unit per KOhm) and capacitors (1 unit per uF). The objective is to achieve the highest merit, so we tried different configurations of components data until we achieved our greatest figure of merit.

$$M = \frac{1}{cost * [ripple(V_O) + |average(V_O - 12)| + 10^{-6}]} \tag{1}$$

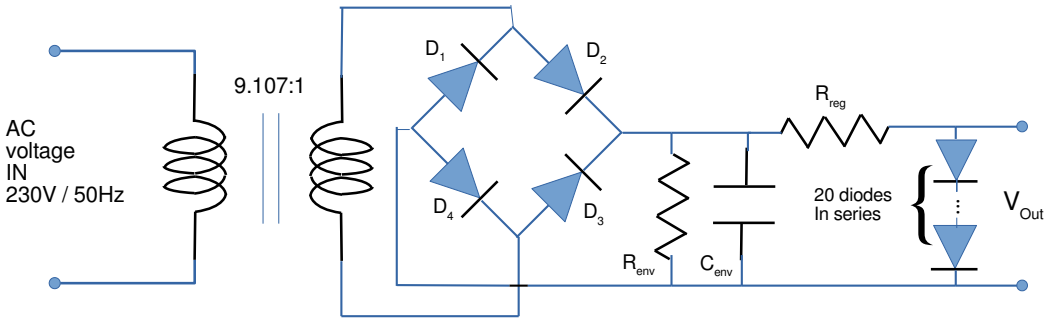

Figure 1: Geometry of our AC/DC converter circuit.

To analyse this circuit theoretically we will use the ideal diode model for the full wave bridge rectifier and the incremental diode model in the voltage regulator. We will compare this results with the ones obtained in the NGSpice simulation. That being said, in Section 2 we present the various theoretical models and calculations used to determine the output voltage, in Section 3

we introduce the results obtained in the simulation. Finally, in Section 4 we compare the two set of results, looking for possible discrepancies and we lay out our conclusions.

In Table 1, we list the numeric values of the components used.

Name	**Values**
Number of Coils	9.107000
R_{env}	900.000000 KOhm
C_{env}	900.000000 uFarad
R_{reg}	100.000000 KOhm
Number of Diodes in Limiter	20.000000

Table 1: Components numeric values used in our analysis and simulation.

2 Theoretical Analysis

In this section we analyse the architecture chosen for the ACDC converter circuit using an Octave theoretical model. Using the ideal diode model we were able to predict the output of the Envelope Detector and using the incremental diode model we predicted the output of the Voltage Regulator.

2.1 Envelope Detector

Our input for the envelope detector is the AC voltage source with its amplitude reduced by the transformer. This voltage is processed by the full-wave bridge rectifier, which allows current to flow in both directions, unlike the half-wave rectifier, which only allows current to pass when our voltage source is at a positive state (otherwise the diode would be shut-off). The full-wave rectifier allows two possible paths for the current to flow, one for positive voltage, the other for negative voltage. This way, in R_{env} the voltage will always be positive or nule, obviously mantaining its amplitude and frequency traits, since we are using the ideal diode model - no voltage is consummed by the diodes. The junction of the capacitor will annihilate the wave status of the voltage. When the voltage is at its peak, it will then start its periodic decrease, and the current in the capacitor will grow more and more negative until it reaches the point where its simmetric to the current flowing in the resistor! It's simple to see, using the nodal method, that the current flowing from the diode path is now null, and those diodes will shut-off. This happens, as stated, when i_R = i_C, and the equation for the instant is given by:

$$t_{off} = \frac{1}{w} * arctan(\frac{1}{wRC}); \tag{2}$$

Now the capacitor will discharge through the resistor, and our output for the envelope detector will decay (remember that until t_{off} our output voltage was equal to the one that comes out of the full-wave rectifier, the output voltage in the load (the resistor), which is the same voltage of the capacitor (since they're in paralell), which is then finally our envelope detector output voltage). The decay of our output voltage is expressed by the following equation, where A is the amplitude of the input voltage, $\frac{230}{N_{coils}}$:

$$V_{env} = A|cos(wt_{off})|e^{\frac{-(t-t_{off})}{RC}}; \tag{3}$$

When the full-wave voltage becomes once again greater than our decay voltage (which is due to happen since it will reach the amplitude peak again and the voltage in the RC circuit is ever diminuishing). There, our envelope detector output voltage returns to being the one that comes

out of the rectifier. Eventually, the rectifier voltage reaches its peak again (which happens a half of a period after - we're considering the negative peaks as well, which are now positive fruit of the rectifier's action) and the cycle repeats

Due to the transition regime we found in the NGSpice simulation, as you will see, that turned out to be quite lengthy, we opted to start the study of the circuit after a period of 3.8 seconds in order to have a stabilized response. The voltage at the output of the envelope detector circuit is now plotted as follows in figure 2.

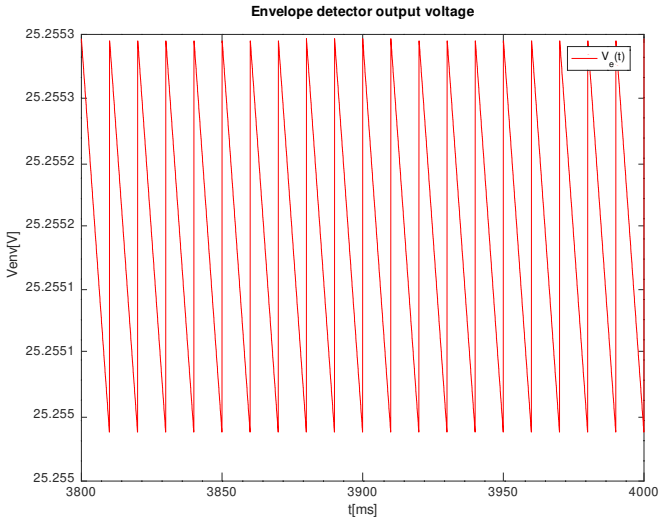

Figure 2: Voltage envelope detector circuit output.

As expected, we see a positive voltage oscillating up to a maximum voltage equal to the initial 230V divided by the number of coils ≅ 25.2553V. Already we are close to a direct current regime, but the voltage level and the magnitude of the ripple still need to be addressed and adjusted. In table 2, we present the average (DC component) and the ripple (the oscillation, the AC character) of the output from the envelope detector, which will now be our input voltage for our next step - the voltage regulator.

Name	Values [V]
@V_{DC}	25.255143
@$V_{ACripple}$	0.000311

Table 2: Envelope Detector Output Voltage traits.

2.2 Voltage Regulator

For the voltage regulator, we used the incremental model. In the previous subsection, we divided our new input voltage in its DC and AC component, and we will now treat them separately. Starting with the DC component, for this step the ideal model with a voltage source V_{ON} is used. We chose $V_{ON} = 0.6$, in accordance to our number of diodes, 20, so that our final output voltage, the output in the series of diodes, is the desired 12V. So, if our input DC voltage is greater than 12V, the current will flow and our DC output voltage will be 12V - since our input DC component is purposely greater than 12V, then our DC component for the voltage regulator is guaranteed to be 12V. For the AC component, every diode is represented by a resistor, r_d, whose resistance can be calculated according to the following formula:

$$r_d = \frac{\eta * V_T}{I_S * e^{\frac{V_D}{\eta * V_T}}} = 247.05; \tag{4}$$

I_S is the reverse saturation current, with a value of 10^{-14}, η is the material constant, valued 1, and V_T is the thermal voltage, with a value of $26mV$ - all this values are the default values used by NGSpice for the default diode model. V_D is the DC voltage in each diode - V_{ON}. This being said, our circuit is now equivalent to a voltage divider circuit, with the greater resistante, R_{reg} and the sum of the diode resistances r_d making up our output, so our AC output voltage can then be calculated in each time instance by the this next formula:

$$v_o = \frac{20r_d}{R + 20r_d} v_{env}; \tag{5}$$

This way, we needed a resistance value much greater than the diode incremental resistance (we chose 100kOhm) in order to diminuish our AC output voltage. This AC component is the inevitable variation of our output voltage around the 12V - the ripple - fruit of the sinusoidal character of our input voltage that can never be trully extinguished. Finally, our voltage regulator output and so our final output voltage consists of the adding effect of both the DC and AC components. The output of the regulator circuit is plotted in figures 3 to 5. In table 3 we can see the DC component and ripple of our final output, as well as the figure of merit such results would give us. However, the figure of merit desired is the one obtained in the simulation.

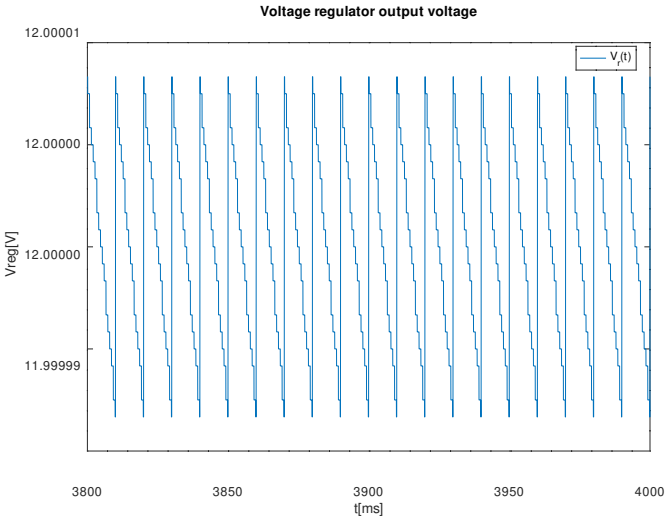

Figure 3: Voltage regulator circuit output.

Name	Values [V]
@V_{DC}	12.000000
@$V_{ACripple}$	0.000015
Cost	1902.400000
Merit	33.573648

Table 3: Voltage Regulator Output Voltage traits, and theoretical figure of merit.

As we can see in this table, the ripple is very low, in an order of greatness of the uV (15 uV), which is a very much pleasing result to be replicated in the simulation.

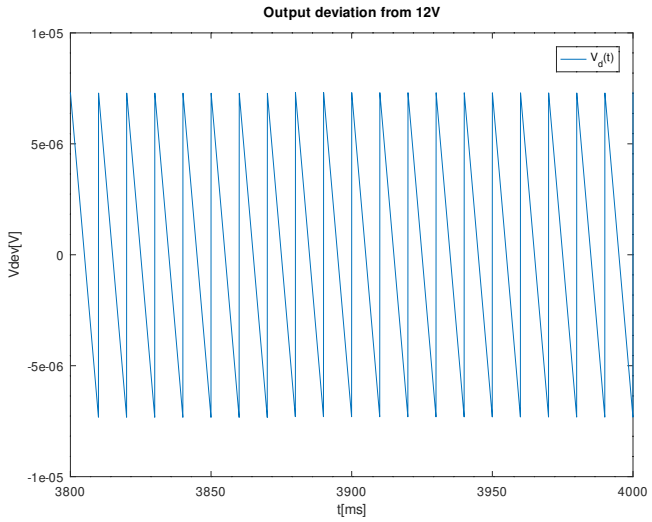

Figure 4: Circuit output subtracted of the desired 12V.

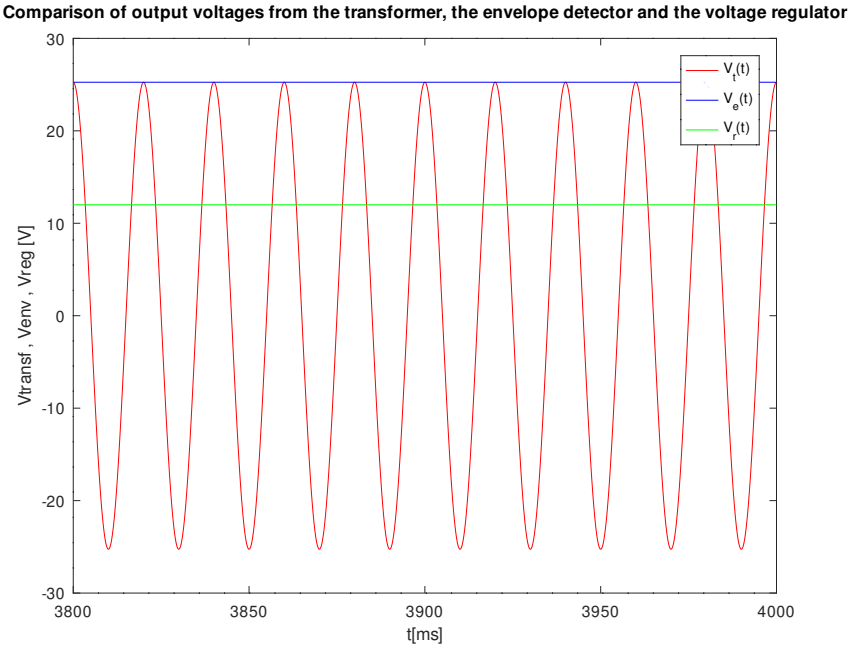

Figure 5: Comparison between the different voltage outputs.

3 Simulation Analysis

Since the input voltage source in this circuit is sinusoidal, the voltage and current values of the various components vary in time, and we are interested therefore in analysing how they evolve in time and obviously we want to picture the transformation of our AC input voltage source throughout the multiple stages of the circuit. Therefore, we will run a single transient analysis for this circuit, lasting 10 periods of the voltage source. For this simulation we are not taking the natural solution into account, only the forced one. In our simulation we came across a large transitional period of roughly 4 seconds, until the output voltage source stabilized enough in the envelope detector, so we only account for data after this period, [3.8 ; 4.0]. This is due to the natural solution of the voltage and its downfall effects will be aproached in our conclusions. We used the default diode model of NGSpice in this simulation and we saw no need of introducing

a transformer since it only reduces the amplitude of the voltage source, so we applied the AC voltage output of the transformer as our input voltage source of the circuit.

3.1 Envelope Detector Output Voltage

In figure 6 we present the plot of the envelope detector output voltage throughout 10 periods, and in table 4 we introduce the average voltage (approximate DC component) and the voltage ripple of such voltage. Since the objective lies in the output of the regulator, this set of data isn't of much relevance.

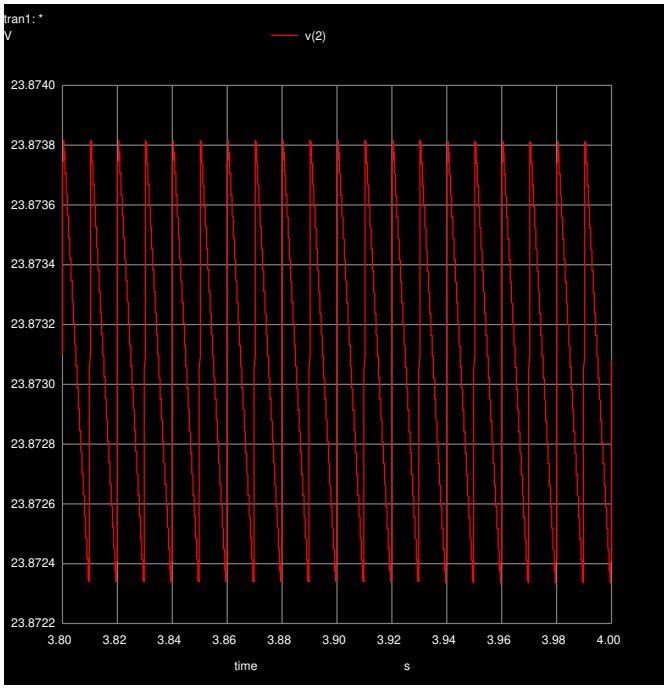

Figure 6: Simulated output voltage in the envelope detector.

Name	Values [V]
envelopeaverage	2.387308e+01
enveloperipple	1.480000e-03

Table 4: Envelope Detector Output Voltage characteristics.

3.2 Voltage Regulator Output Voltage - The output of the circuit

Now, in figure 7 we present the plot of the voltage regulator output voltage throughout the same 10 periods, and in table 5 we introduce the average voltage (approximate DC component) and

the voltage ripple of such voltage. This is indeed our desired output voltage for the circuit, so its average and ripple are very important data. In this case, we managed a average output voltage that only differs from 12V in its last significant algharism, and a voltage ripple in the order of the uV, which seems to us a pretty satisfactory result.

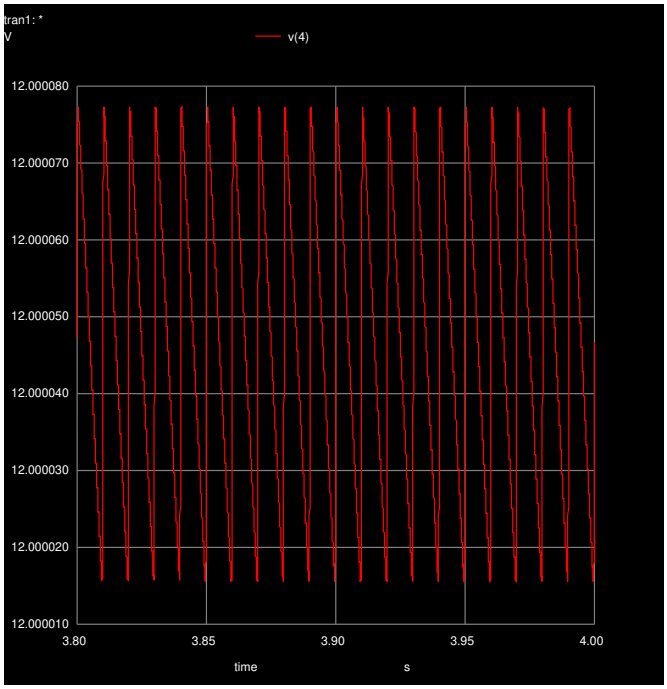

Figure 7: Simulated output voltage in the voltage regulator.

Name	**Values [V]**
outputaverage	1.200005e+01
outputripple	6.000000e-05
merit	4.735602e+00

Table 5: Voltage Regulator Output Voltage characteristics, and figure of merit.

In figure 8 we are able to get a closer look to the slight deviations from the desired linear 12V in our output, and in figure 9 we compare the input voltage source post-transformer, the output of the envelope detector, and our final output - the voltage regulator output voltage. In this figure we can see the linear character of the voltage post-envelope detector, opposed to its sinusoidal form after the transformer, so the envelope did its job in annihilating the sinusoidal wave form. Then, we can see that our final output voltage maintains this linear (DC) trait, even improving on it thanks to the resistor, and it is now at the desired 12V fruit of the action of our limiter, the 20 diodes in series.

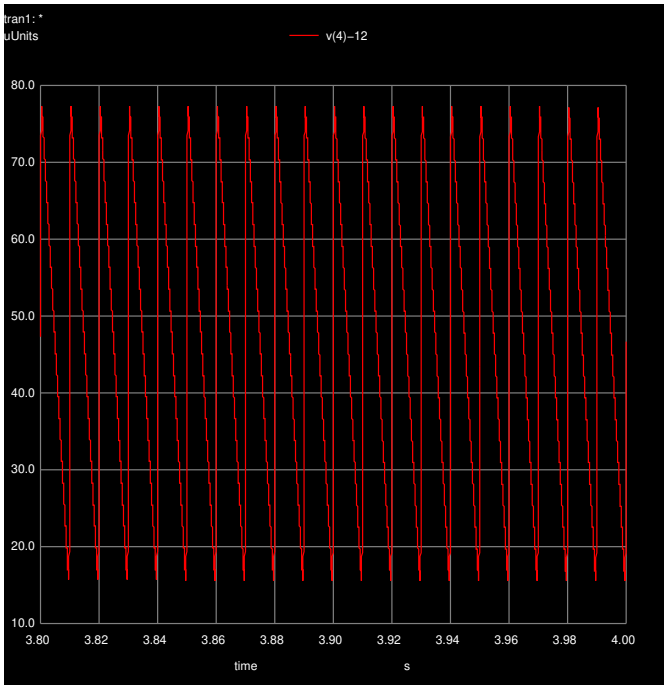

Figure 8: Deviation from 12V of the output voltage in the voltage regulator.

Going back to table 5, we calculated the figure of merit for this configuration, and obtained a value close to 5. The value could have been higher if the average of the output voltage were a straight 12V, which is not the case. Another way to increase the merit would have been to diminuish our ripple by increasing our resistors and capacitor values. Even though we would be increasing our cost, the decrease of the ripple would have an even bigger effect than that of the cost, increasing our merit. However, we noticed this could come at the cost of a even bigger transitional period, which is not a good model for an AC/DC converter, since it is impractical to wait more than 5 seconds for the conversion to take place in an effective manner. A way to decrease this transitional period could come in the form of increasing the input voltage source coming from the transformer, but that would require an even bigger resistance in the regulator to help bring that value down (we're using the default diode model, not the theoretical ideal one)... Final notes on the figure of merit topic will be approached in our conclusions.

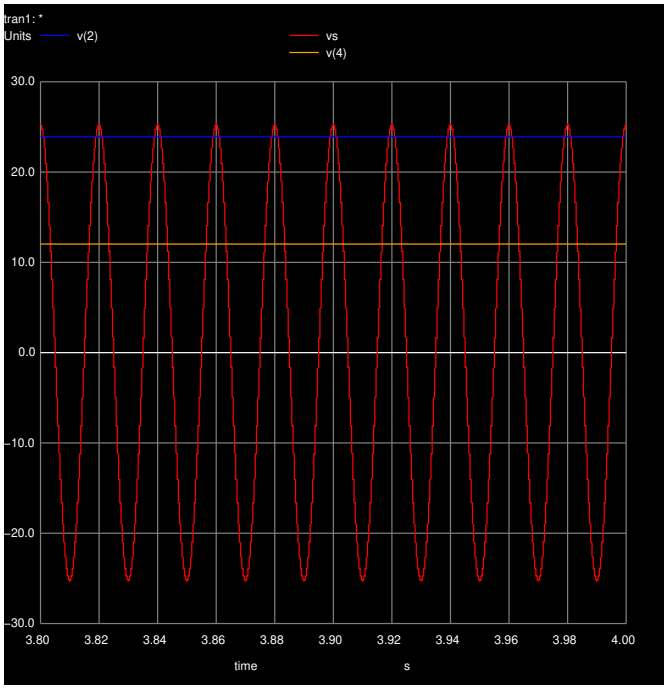

Figure 9: Comparison of the simulated input voltage source (after transformer), the envelope detector voltage and, finally, the voltage regulator voltage, our output.

4 Conclusion

Theoretical	**Value**	**Simulation**	**Value**
$V_{DCenvelope}$	25.255143 V	$V_{DCenvelope}$	2.387308e+01 V
$V_{ACenvelope}$	0.000311 V	$V_{ACenvelope}$	1.480000e-03 V
$V_{DCregulator}$	12.000000 V	$V_{DCregulator}$	1.200005e+01 V
$V_{ACregulator}$	15 uV	$V_{ACregulator}$	60 uV
$Merit$	33.573648	$Merit$	4.735602e+00

Table 6: Comparison of the theoretical and simulated data results, regarding the DC and AC components.

The main difference between simulation and the theoretical predictions was the transition regime, which was not considered for our calculations: we assumed the circuit was in equilibrium from the beginning. However, due to the relatively high resistance and capacitance of the components in the circuit, this regime became apparent in the simulation. A permanent regime should be established within 5 time periods, however, each time period (calculated from equivalent RC) took almost a second long. This is obviously not desirable in real world applications but we optimized the circuit to obtain a solid merit figure and nothing else. We tried to

mitigate this effect by starting our study of the circuit after roughly 4 seconds of the beginning of the simulation. Still, the results didn't match perfectly, and the final merit figure was quite different from the predicted. This mostly has to do with the difference in diode model, since the calculations were performed with an ideal diode and that wasn't the case for the simulation. All things taken into account, in this laboratory assignment we were able to reproduce a working, despite rudimentary, ACDC converter.