TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

MEAer (Integrated Master In Aerospace Engineering), Técnico, University of Lisbon

Laboratory 4: Audio Amplifier Circuit

Group 3

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1 Introduction

The objective of this laboratory assignment is to build an audio amplifier circuit. For this laboratory assignment there is a figure of merit, depending on the results obtained in the NGSpice simulation. This figure takes into account the cost of the components used, and the results they provide - a desirably low cut off frequency, the voltage gain and usable bandwidth. The figure is calculated using the formula given by equation 1. The cost englobes the cost of transistors (0.1 units per transistor), resistors (1 unit per KOhm) and capacitors (1 unit per uF). The objective is to achieve the highest merit, so we tried different configurations of components data until we achieved our greatest figure of merit. Since the human ear can perceive frequencies between 20 Hz to 20 kHz, the circuit was designed to amplify that frequency band.

$$M = \frac{Gain * bandwidth}{cost * CutOffFrequency} \tag{1}$$

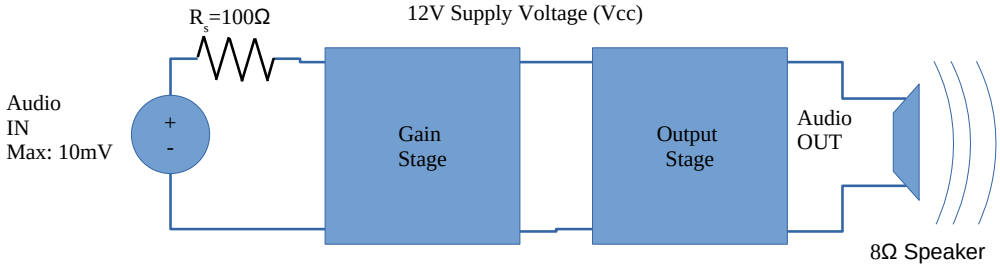

Figure 1: Geometry of our Audio Amplifier circuit.

To analyse this circuit theoretically we will separate the circuit in two stages: the gain and output stage. We will compare these results with the ones obtained in the NGSpice simulation. That being said, in Section 2 we present the theoretical models and calculations used to determine the operating point, gain, impedances and frequency response, in Section 3 we introduce the results obtained in the simulation. Finally, in Section 4 we compare the two set of results, looking for possible discrepancies and we lay out our conclusions.

In Table 2, we list the numeric values of the components used (nomenclatures consistent with the theoretical lecture).

Name	Values
VT	0.025000 V
BFN	178.700000
VAFN	69.700000 V
VBEON	0.700000 V
BFP	227.300000
VAFP	37.200000 V
VEBON	0.700000 V
VCC	12.000000 V
RB1	80.000000 kOhm
RB2	20.000000 kOhm
RE1	200.000000 Ohm
RC1	900.000000 Ohm
RE2	50.000000 Ohm
C_{input}	0.100000 mF
C_{bypass}	2.500000 mF
C_{output}	1.500000 mF

Table 1: Values of components used in our analysis and simulation.

2 Theoretical Analysis

First of all, we performed an operating point analysis in order to check if the transistor was operating in the forward active region.

Name	Values
IB1	0.000033 A
IC1	0.005849 A
IE1	0.005882 A
VE1	1.176319 V
VO1	6.736022 V
VCE	5.559704 V

Table 2: Operating point analysis results.

As we can see, VCE is greater than VBEON (0.7V), so we're good to go.

2.1 Gain Stage

For the gain stage, the analysis of the incremental circuit yielded the following results:

We can clearly see the need for an output stage, given the magnitude of the output impedance. The gain is also significant, and we'll strive for a unitary gain in the output stage in order not to sacrifice this.

2.2 Output Stage

As desired, the input impedance of this stage is much bigger than the output impedance of the gain stage. This means that the circuit experiences very little signal loss. As well, the output impedance of this stage is desirably low when compared to the 8 Ohm of the speakers. At last, the total circuit gain results.

Name	Values [V]
Gm	0.233955 S
Rpi	763.823529 Ohm
Ro	11916.843872 OHM
Input impedance	729.020826 Ohm
Output impedance	836.801914 Ohm
Gain	-172.158583
Gain(dB)	44.718574 dB

Table 3: Gain stage theoretical results

Name	Values [V]
Gm	3.635189
gpi	0.015993
go	0.002443
Input impedance	10234.962944
Output impedance	0.272211
Gain	0.993891
Gain	-0.053227dB

Table 4: Output stage theoretical results

3 Simulation Analysis

Since the input voltage source in this circuit is sinusoidal, the voltage and current values of the various components vary in time, and we are interested therefore in analysing how they evolve in time and obviously we want to picture the transformation of our AC input voltage source throughout the multiple stages of the circuit. Therefore, we will run a single transient analysis for this circuit, lasting 10 periods of the voltage source. For this simulation we are not taking the natural solution into account, only the forced one. In our simulation we came across a large transitional period of roughly 4 seconds, until the output voltage source stabilized enough in the envelope detector, so we only account for data after this period, [3.8 ; 4.0]. This is due to the natural solution of the voltage and its downfall effects will be aproached in our conclusions. We used the default diode model of NGSpice in this simulation and we saw no need of introducing a transformer since it only reduces the amplitude of the voltage source, so we applied the AC voltage output of the transformer as our input voltage source of the circuit.

3.1 Envelope Detector Output Voltage

In figure we present the plot of the envelope detector output voltage throughout 10 periods, and in table we introduce the average voltage (approximate DC component) and the voltage ripple of such voltage. Since the objective lies in the output of the regulator, this set of data isn't of much relevance.

3.2 Voltage Regulator Output Voltage - The output of the circuit

Now, in figure we present the plot of the voltage regulator output voltage throughout the same 10 periods, and in table we introduce the average voltage (approximate DC component) and the voltage ripple of such voltage. This is indeed our desired output voltage for the circuit, so its average and ripple are very important data. In this case, we managed a average output voltage that only differs from 12V in its last significant algharism, and a voltage ripple in the order of the uV, which seems to us a pretty satisfactory result.

Name	Values [V]
Gain	-158.174605
Gain	43.982735dB

Table 5: Total circuit theoretical gain results

Name	Values [V]
vcc[0]	1.200000e+01
in[0]	0.000000e+00
in2[0]	0.000000e+00
base[0]	1.878920e+00
coll[0]	7.214695e+00
emit[0]	1.184175e+00
emit2[0]	8.033675e+00
out[0]	0.000000e+00

Table 6: Operating point node voltage values of the amplifier circuit.

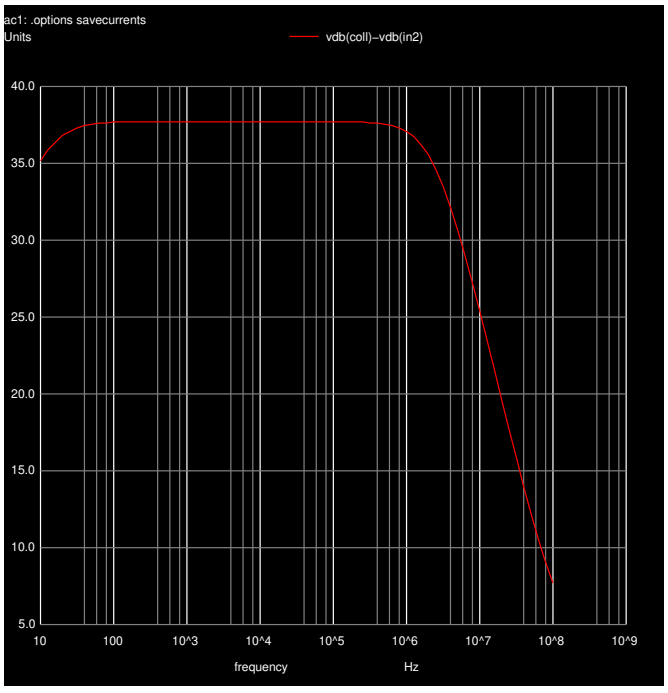

Figure 2: Gain Stage output voltage gain (frequency response).

In figure we are able to get a closer look to the slight deviations from the desired linear 12V in our output, and in figure we compare the input voltage source post-transformer, the output of the envelope detector, and our final output - the voltage regulator output voltage. In this figure

Name	Values
Gain	65.5843
Gain(dB)	36.336
Lower cut-off frequency	16.6025 Hz
Upper cut-off frequency	2.47423E+06 Hz
Bandwidth	2.47421E+06 Hz
Input impedance	0.856866 kOhm
Output impedance	8.18142 Ohm

Table 7: Output gain, bandwidth, and input and output impedances of the audio amplifier circuit (as a whole).

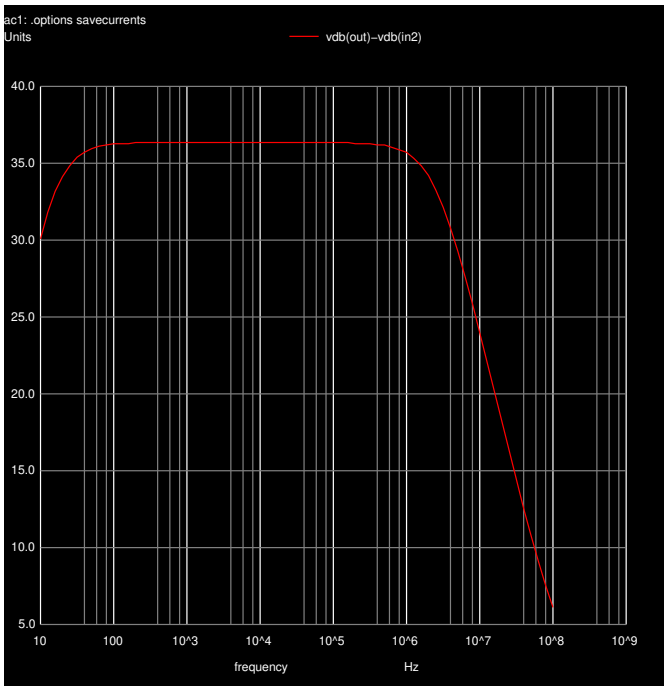

Figure 3: Load output voltage gain (frequency response).

we can see the linear character of the voltage post-envelope detector, opposed to its sinusoidal form after the transformer, so the envelope did its job in annihilating the sinusoidal wave form. Then, we can see that our final output voltage maintains this linear (DC) trait, even improving on it thanks to the resistor, and it is now at the desired 12V fruit of the action of our limiter, the 20 diodes in series.

Going back to table, we calculated the figure of merit for this configuration, and obtained a value close to 5. The value could have been higher if the average of the output voltage were a straight 12V, which is not the case. Another way to increase the merit would have been to

Name	Values
cost	4.201458e+03
merit	2.326284e+03

Table 8: Cost and merit of the audio amplifier circuit.

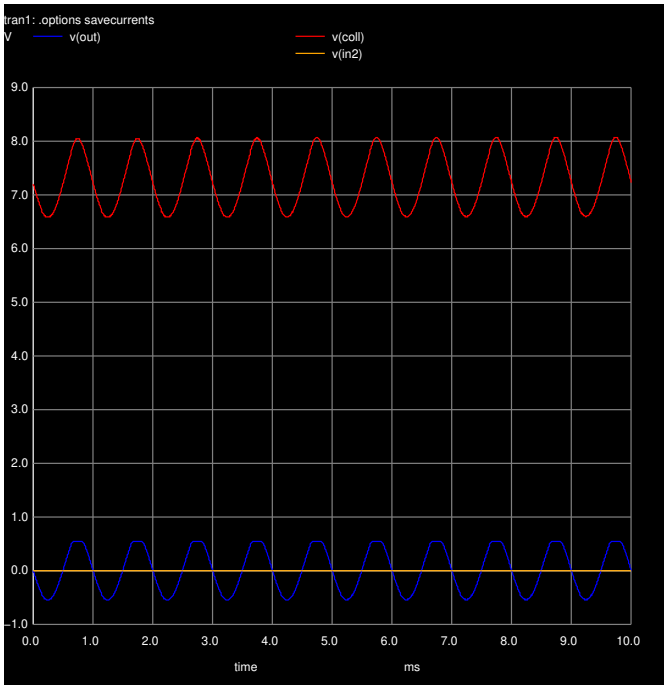

Figure 4: Evolution of the AC signal from input to output.

diminuish our ripple by increasing our resistors and capacitor values. Even though we would be increasing our cost, the decrease of the ripple would have an even bigger effect than that of the cost, increasing our merit. However, we noticed this could come at the cost of a even bigger transitional period, which is not a good model for an AC/DC converter, since it is impractical to wait more than 5 seconds for the conversion to take place in an effective manner. A way to decrease this transitional period could come in the form of increasing the input voltage source coming from the transformer, but that would require an even bigger resistance in the regulator to help bring that value down (we're using the default diode model, not the theoretical ideal one)... Final notes on the figure of merit topic will be approached in our conclusions.

As we can see in the table, regarding the envelope detector DC component, its value is lower in the simulation, which is due to the use of a real diode model in NGSpice, and the ideal diode model always produces a higher output voltage than a real diode. Both the ripples are higher in the simulation, cause of the same situation. For the DC component of the regulator output voltage, we were unable to fully hit the 12V. The merit is then obviously higher theoretically,

fruit of lower ripples and a certain DC 12V. We noticed during our trials and errors that higher resistances and capacitances lowered the ripples and increased our merit, despite the greater cost, so we went for it. The main difference between simulation and the theoretical predictions was the transition regime, which was not considered for our calculations: we assumed the circuit was in equilibrium from the beginning. However, due to the relatively high resistance and capacitance of the components in the circuit, this regime became apparent in the simulation. A permanent regime should be established within 5 time periods, however, each time period (calculated from equivalent RC) took almost a second long. This is obviously not desirable in real world applications but we optimized the circuit to obtain a solid merit figure and nothing else. We tried to mitigate this effect by starting our study of the circuit after roughly 4 seconds of the beginning of the simulation. Still, the results didn't match perfectly, and the final merit figure was quite different from the predicted. This mostly has to do with the difference in diode model, since the calculations were performed with an ideal diode and that wasn't the case for the simulation. All things taken into account, in this laboratory assignment we were able to reproduce a working, despite rudimentary, ACDC converter.