TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

MEAer (Integrated Master In Aerospace Engineering), Técnico, University of Lisbon

Laboratory 4: Audio Amplifier Circuit

Group 3

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Contents

1 Introduction

The objective of this laboratory assignment is to build an audio amplifier circuit. Our circuit input consists of a 10 mV sinusoidal signal and its inevitable resistance. This signal goes through a first stage - the gain stage - whose principal component is the NPN transistor. This stage will amplify our signal drastically, but it will be not suited to be connected to our load due to its high output impedance (which would consume a great part of its own voltage). At the entrance of this stage we have an input coupling capacitor to block unwanted DC current. Now the signal goes through our second stage - the output stage - primarily composed of a PNP transistor. This stage will approximately mantain our amplitude, but due to the stage's very low output impedance, the signal will now be suitable to be linked to our resistor load without considerable gain lost. Before the load we have an output coupling capacitor, which will block the coming DC voltage, allowing a solely sinusoidal output signal. For this to run, we need a bias circuit powered by a supply DC voltage of 12V overlapped with our main circuit. For this laboratory assignment there is a figure of merit, depending on the results obtained in the NGSpice simulation. This figure takes into account the cost of the components used, and the results they provide - a desirably low cut off frequency, the voltage gain and usable bandwidth. The figure is calculated using the formula given by equation 1. The cost englobes the cost of transistors (0.1 units per transistor), resistors (1 unit per KOhm) and capacitors (1 unit per uF). The objective is to achieve the highest merit, so we tried different configurations of components data until we achieved our greatest figure of merit. Since the human ear can perceive frequencies between 20 Hz to 20 kHz, the circuit was designed to amplify that frequency band.

$$M = \frac{Gain * Bandwidth}{Cost * LowerCutOffFrequency} \tag{1}$$

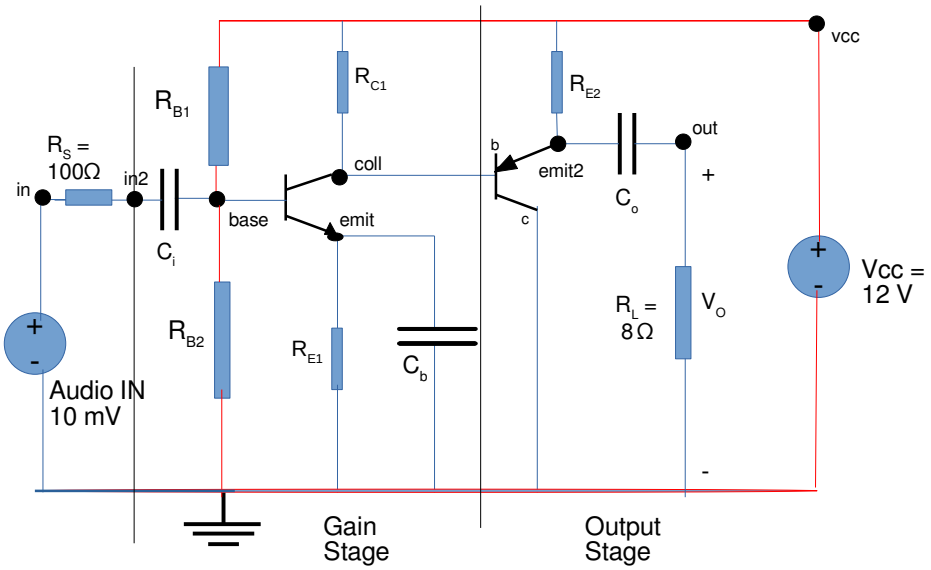

Figure 1: Geometry of our Audio Amplifier circuit.

To analyse this circuit theoretically we will separate the circuit in two stages: the gain and output stage. We will determine the operating point values of the circuit, with the help of a Thévenin equivalent of the bias circuit, in order to confirm the forward-active region of the transistors, and we will use the transistor incremental model to base in our calculations for the AC component of our circuit. We will compare these results with the ones obtained in

the NGSpice simulation. That being said, in Section 2 we present the theoretical models and calculations used to determine the operating point, gain, impedances and frequency response, in Section 3 we introduce the results obtained in the simulation. Finally, in Section 4 we compare the two set of results, looking for possible discrepancies and we lay out our conclusions. In Table 2, we list the numeric values of the components used (nomenclatures consistent with the theoretical lecture), and some important parameters of the Philips BJT transistors used which will come in handy in our theoretical calculations.

Name	**Values**
VT	0.025000 V
BFN	178.700000
VAFN	69.700000 V
VBEON	0.700000 V
BFP	227.300000
VAFP	37.200000 V
VEBON	0.700000 V
VCC	12.000000 V
RB1	80.000000 kOhm
RB2	20.000000 kOhm
RE1	200.000000 Ohm
RC1	900.000000 Ohm
RE2	50.000000 Ohm
C_{input}	0.100000 mF
C_{bypass}	2.500000 mF
C_{output}	1.500000 mF

Table 1: Values of components used in our analysis and simulation.

2 Theoretical Analysis

First of all, we performed an operating point analysis in order to check if the transistor was operating in the forward active region.

Name	**Values**
RB	16000.000000 Ohm
VEQ	2.400000 V
IB1	0.000033 A
IC1	0.005849 A
IE1	0.005882 A
VE1	1.176319 V
VO1	6.736022 V
VCE	5.559704 V
V_{in}	0 V
V_{in2}	0 V
V_{vcc}	12 V
V_{base}	1.876319 V
V_{coll}	6.736022 V
V_{emit}	1.176319 V

Table 2: Operating point analysis results.

As we can see, VCE is greater than VBEON (0.7V), so we're good to go.

2.1 Gain Stage

For the gain stage, the analysis of the incremental circuit yielded the following results:

Name	Values
gm	0.233955 S
rpi	763.823529 Ohm
ro	11916.843872 Ohm
Input impedance	729.020826 Ohm
Output impedance	836.801914 Ohm
Gain	-172.158583
Gain(dB)	44.718574 dB

Table 3: Gain stage theoretical results

We can clearly see the need for an output stage, given the magnitude of the output impedance. The gain is also significant, and we'll strive for a unitary gain in the output stage in order not to sacrifice this.

2.2 Output Stage

As before, we perform a DC operating point analysis: From both the table and the following

Name	Values
IB2	0.000400 A
IC2	0.090880 A
IE2	0.091280 A
VO2	7.436022 V
V_{vcc}	12 V
V_{coll}	6.736022 V
V_{emit2}	7.436022 V
V_{out}	0 V

Table 4: Operating point analysis results.

equation we can understand that the voltage drop in this transistor is greater than 0.7V and so it is operating in the forward active region.

$$V_{emit2} = V_{coll} + V_{EBON}; \tag{2}$$

Next, we present the results of the output stage theoretical model.

Name	Values
gm2	3.635189 S
rpi2	62.527694 Ohm
ro2	409.332200 Ohm
Input impedance	10234.962944 Ohm
Output impedance	0.272211 Ohm
Gain	0.993891
Gain(dB)	-0.053227 dB

Table 5: Output stage theoretical results

As desired, the input impedance of this stage is more than 10 times greater than the output impedance of the gain stage. This means that the circuit experiences little signal loss. As well, the output impedance of this stage is desirably low when compared to the 8 Ohm of the speakers. At last, the total circuit gain results.

Name	Values
Input impedance	729.020826 Ohm
Output impedance	3.619271 Ohm
Gain	-158.174605
Gain(dB)	43.982735 dB

Table 6: Total circuit theoretical gain results

The gain is slightly lower than the product of the two previous gains, likely due to some signal loss in the interface between stages. Besides this approach, we plotted the frequency response of the circuit for the output voltage of the circuit, in terms of gain and phase difference:

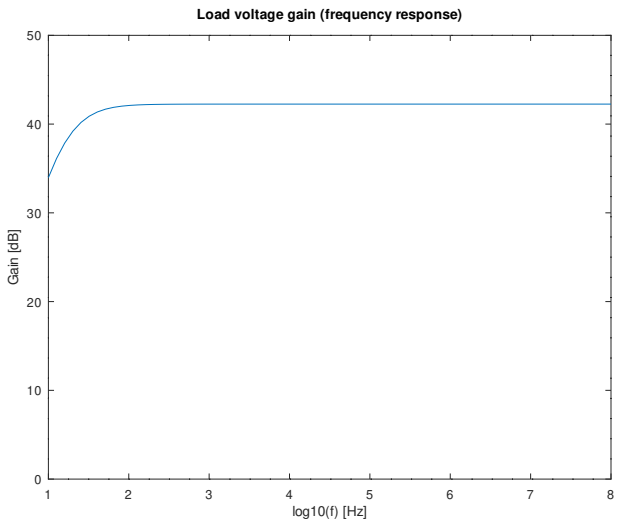

Figure 2: Load output voltage gain (frequency response).

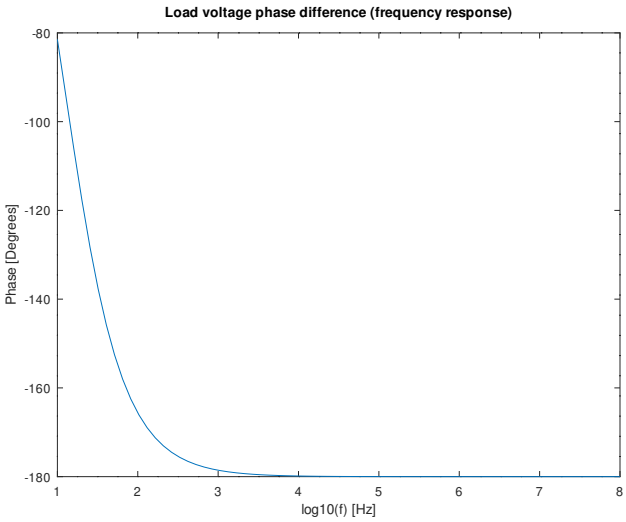

Figure 3: Load output voltage phase difference (frequency response).

For the medium frequencies (within the bandwidth) we obtained the following gain figure.

We also determined the lower cut-off frequency, which yielded close to 20 Hz, the lowest frequency the human ear can perceive as a musical note. This was achieved by finding the point on the gain frequency response plot that had a 3 decibel drop relative to the maximum gain.

Name	**Values**
Gain	129.600426
Gain(dB)	42.252129 dB
Lower cut-off frequency	20.432601 Hz

Table 7: Gain for medium frequencies and lower cut-off frequency of the output voltage signal.

3 Simulation Analysis

Since the input voltage source in this circuit is sinusoidal, the voltage and current values of the various components vary in time, and we are interested therefore in analysing how they evolve in time and obviously we want to picture the transformation of our AC input voltage source throughout the multiple stages of the circuit. We will run an operating point analysis in order to confirm the forward-active region of the two transisters, a transient analysis which will help us measuring the input and output impedances. We will also run a frequency response analysis in order to determine the gain and bandwidth of our output amplified sinusoidal signal. The transistors used were the Philips BJT's.

3.1 Operating point

We start with the operating point analysis. Given that the output signal will be solely sinusoidal, there isn't much relevance to this set of data. Its main goal is to confirm the forward-active region of both the npn and pnp transistors. In table 8 we present the operating point node voltages of the circuit. As expected, the voltage in nodes in e $in2$ since our source doesn't have a DC component. Our output signal doesn't have a linear voltage component, since the voltage in node out is zero, because the output coupling capacitor blocks the coming DC voltage. Regarding the npn transistor, the voltage drop must occur from the collector to the base, and from the base to the emitter - since $V_{coll} > V_{base} > V_{emit}$, this is confirmed. Looking to the pnp transistor, our collector node is ground, our base node is $coll$ and our emitter node is $emit2$. The voltage drop in this case must happen from the emitter to the collector. Since $V_{emit2} > V_{coll} > GND$, this is confirmed - both our transistors work in the pretended forward-active region.

Name	Values [V]
vcc[0]	1.200000e+01
in[0]	0.000000e+00
in2[0]	0.000000e+00
base[0]	1.878920e+00
coll[0]	7.214695e+00
emit[0]	1.184175e+00
emit2[0]	8.033675e+00
out[0]	0.000000e+00

Table 8: Operating point node voltage values of the amplifier circuit.

3.2 Frequency response and impedances

We measured the input impedance of the circuit, seen through the perspective of the source, and the output impedance, seen through the perspective of our output (using a dummy test source). With the frequency response, we measured the voltage gain in our output. As we will see in figure 5, the gain graph has the traits of a band-pass filter, letting pass medium frequencies (our source operates at a medium frequency), so we measure the in that zone. We also measured then the lower and upper cut-off frequencies of such graph, in order to determine the bandwidth of our amplifier. In table 9, we present the results of our calculations. In figures 4and 5 we can see the evolution of the gain throughout the circuit, first the gain out of the gain stage - node $coll$ - and then the final gain, the gain out of the output stage - node out. With this figures we can confirm the band-pass filter trait of our circuit.

Name	Values
Gain	65.5843
Gain(dB)	36.336
Lower cut-off frequency	16.6025 Hz
Upper cut-off frequency	2.47423E+06 Hz
Bandwidth	2.47421E+06 Hz
Input impedance	0.856866 kOhm
Output impedance	8.18142 Ohm

Table 9: Output gain, bandwidth, and input and output impedances of the audio amplifier circuit (as a whole).

Analysing both the input and output impedances of the circuit, the input impedance is pretty satisfactory as it allows the vast majority of input voltage to go through the transistors, which means a low voltage loss. However, comparing the value of the output impedance with the load resistor, they are very much comparable. This means that part of the gain coming from the transistors will be consumed by some of our resistors in the circuit, hence losing a considerable part of the possible output gain. However, given the gain value we obtained, the overall result is very satisfying.

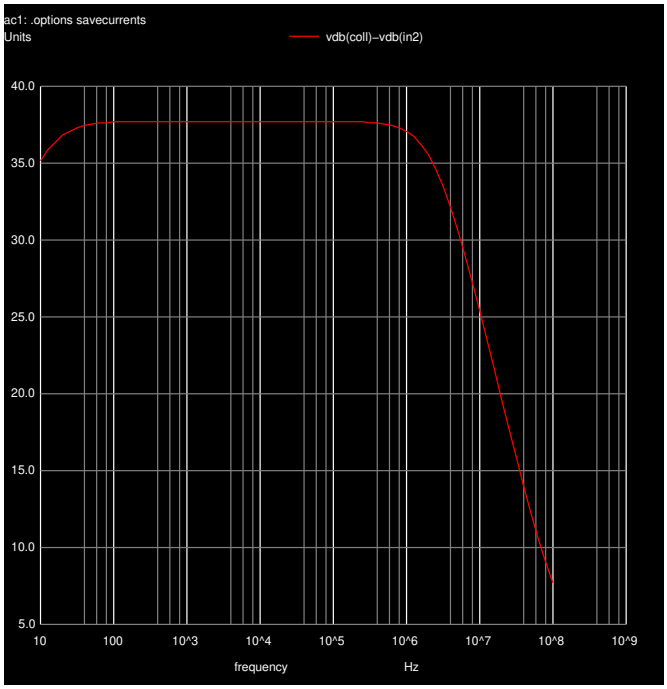

Figure 4: Gain Stage output voltage gain (frequency response).

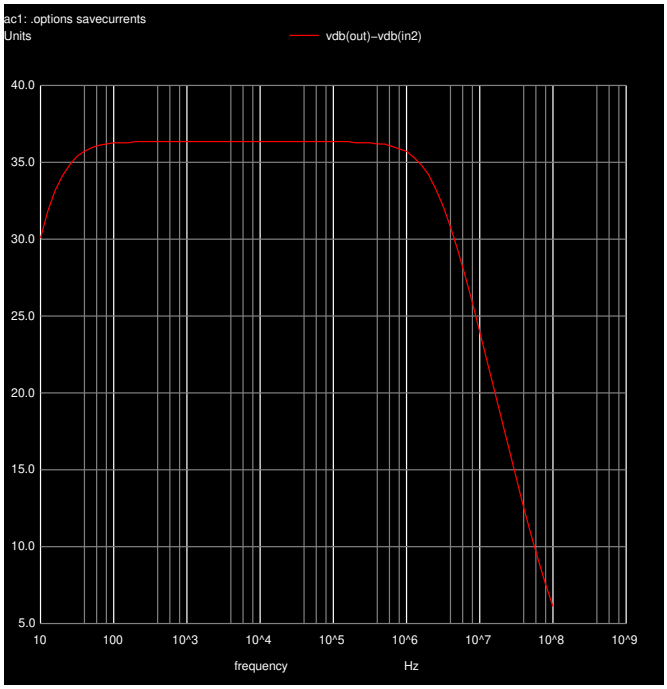

Figure 5: Load output voltage gain (frequency response).

3.3 Final product and merit

In figure 6, we can see the evolution of our AC signal from stage to stage until its final form. The output voltage has a null DC component as pretended, a symmetric phase in comparison to the input source (it's inverted) and a clear greater amplitude of approximately 0.55V, in comparison to the input's 10mV. We can say then that we have achieved the goal of amplifying our input signal, in this case, by 50-60 times! In table 10, we present the cost and merit of our circuit. When looking to the parameters judged by the merit formula, we achieved an amazing bandwidth that clearly operates in the 20Hz-20kHz frequency band pretended, since we have an upper cut-off frequency in the zone of MHz, and a lower cut-off frequency inferior to 20Hz - $\approx$16Hz. The voltage gain could always be a bit higher, but without a defined pretended output amplitude, we can't really evaluate our achieved gain. Since we achieved a merit similar to 2326, the high cost seems like a reasonable price to pay for a circuit with these results. We were able however to achieve greater values of gain, but the output sinusoidal wave would be distorted, almost "cut-off" in its positive voltage periods, which was clearly not desirable, so we escaped from such happening, no matter the increase of gain it delivered.

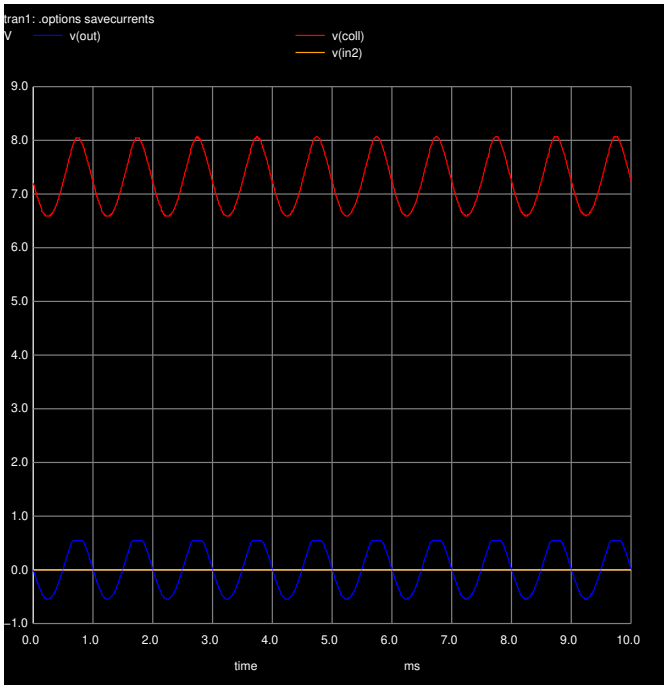

Figure 6: Evolution of the AC signal from input to output.

Name	Values
cost	4.201458e+03
merit	2.326284e+03

Table 10: Cost and merit of the audio amplifier circuit.

4 Conclusion

As we can see in the table, regarding the envelope detector DC component, its value is lower in the simulation, which is due to the use of a real diode model in NGSpice, and the ideal diode model always produces a higher output voltage than a real diode. Both the ripples are higher in the simulation, cause of the same situation. For the DC component of the regulator output voltage, we were unable to fully hit the 12V. The merit is then obviously higher theoretically, fruit of lower ripples and a certain DC 12V. We noticed during our trials and errors that higher resistances and capacitances lowered the ripples and increased our merit, despite the greater cost, so we went for it. The main difference between simulation and the theoretical predictions was the transition regime, which was not considered for our calculations: we assumed the circuit was in equilibrium from the beginning. However, due to the relatively high resistance and capacitance of the components in the circuit, this regime became apparent in the simulation. A permanent regime should be established within 5 time periods, however, each time period (calculated from equivalent RC) took almost a second long. This is obviously not desirable in

Theoretical	Value	Simulation	Value
Operating point			
V_{vcc}	12 V	vcc[0]	1.200000e+01 V
V_{in}	0 V	in[0]	0.000000e+00 V
V_{in2}	0 V	in2[0]	0.000000e+00 V
V_{base}	1.876319 V	base[0]	1.878920e+00 V
V_{coll}	6.736022 V	coll[0]	7.214695e+00 V
V_{emit}	1.176319 V	emit[0]	1.184175e+00 V
V_{emit2}	7.436022 V	emit2[0]	8.033675e+00 V
V_{out}	0 V	out[0]	0.000000e+00 V
Frequency response and impedances			
$Gain$	158.174605	Gain	65.5843
$Gain(dB)$	43.982735 dB	Gain(dB)	36.336 dB
$LowerCut-offFreq$	20.432601 Hz	Lower cut-off freq	16.6025 Hz
$UpperCut-offFreq$	-	Upper cut-off freq	2.47423E+06 Hz
$Bandwidth$	-	Bandwidth	2.47421E+06 Hz
$InputImpedance$	729.020826 Ohm	Input impedance	0.856866 kOhm
$OutputImpedance$	3.619271 Ohm	Output impedance	8.18142 Ohm

Table 11: Comparison of the theoretical and simulated data results, regarding the operating point, frequency response and impedances.

real world applications but we optimized the circuit to obtain a solid merit figure and nothing else. We tried to mitigate this effect by starting our study of the circuit after roughly 4 seconds of the beginning of the simulation. Still, the results didn't match perfectly, and the final merit figure was quite different from the predicted. This mostly has to do with the difference in diode model, since the calculations were performed with an ideal diode and that wasn't the case for the simulation. All things taken into account, in this laboratory assignment we were able to reproduce a working, despite rudimentary, ACDC converter.