TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

MEAer (Integrated Master In Aerospace Engineering), Técnico, University of Lisbon

Laboratory 4: Audio Amplifier Circuit

Group 3

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1 Introduction

The objective of this laboratory assignment is to build an audio amplifier circuit. Our circuit input consists of a 10 mV sinusoidal signal and its inevitable resistance. This signal goes through a first stage - the gain stage - whose principal component is the NPN transistor. This stage will amplify our signal drastically, but it will be not suited to be connected to our load due to its high output impedance (which would consume a great part of its own voltage). At the entrance of this stage we have an input coupling capacitor to block unwanted DC current. Now the signal goes through our second stage - the output stage - primarily composed of a PNP transistor. This stage will approximately mantain our amplitude, but due to the stage's very low output impedance, the signal will now be suitable to be linked to our resistor load without considerable gain lost. Before the load we have an output coupling capacitor, which will block the coming DC voltage, allowing a solely sinusoidal output signal. For this to run, we need a bias circuit powered by a supply DC voltage of 12V overlapped with our main circuit. For this laboratory assignment there is a figure of merit, depending on the results obtained in the NGSpice simulation. This figure takes into account the cost of the components used, and the results they provide - a desirably low cut off frequency, the voltage gain and usable bandwidth. The figure is calculated using the formula given by equation 1. The cost englobes the cost of transistors (0.1 units per transistor), resistors (1 unit per KOhm) and capacitors (1 unit per uF). The objective is to achieve the highest merit, so we tried different configurations of components data until we achieved our greatest figure of merit. Since the human ear can perceive frequencies between 20 Hz to 20 kHz, the circuit was designed to amplify that frequency band.

$$M = \frac{Gain * Bandwidth}{Cost * LowerCutOffFrequency} \tag{1}$$

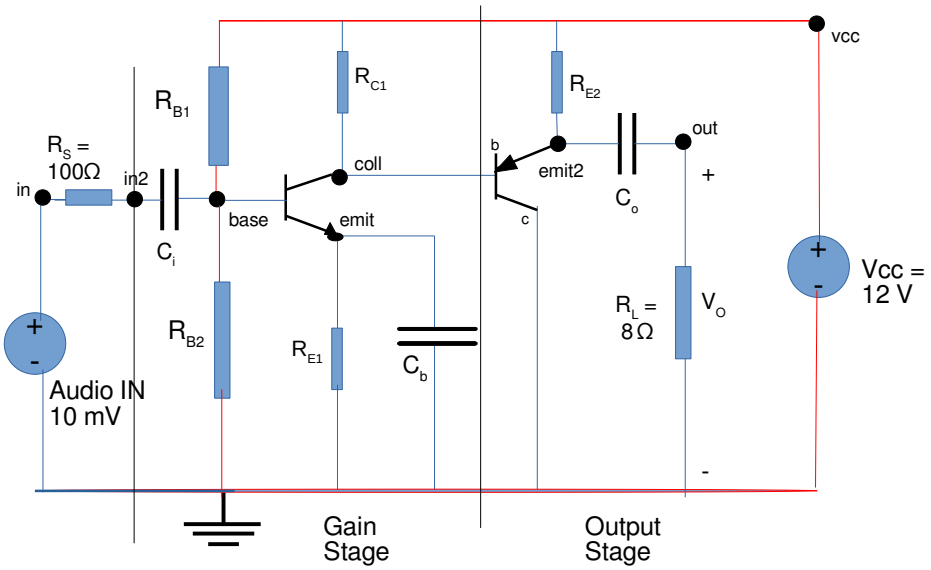

Figure 1: Geometry of our Audio Amplifier circuit.

To analyse this circuit theoretically we will separate the circuit in two stages: the gain and output stage. We will determine the operating point values of the circuit, with the help of a Thévenin equivalent of the bias circuit, in order to confirm the forward-active region of the transistors, and we will use the transistor incremental model to base in our calculations for the AC component of our circuit. We will compare these results with the ones obtained in

the NGSpice simulation. That being said, in Section 2 we present the theoretical models and calculations used to determine the operating point, gain, impedances and frequency response, in Section 3 we introduce the results obtained in the simulation. Finally, in Section 4 we compare the two set of results, looking for possible discrepancies and we lay out our conclusions. In Table 2, we list the numeric values of the components used (nomenclatures consistent with the theoretical lecture), and some important parameters of the Philips BJT transistors used which will come in handy in our theoretical calculations.

Name	**Values**
VT	0.025000 V
BFN	178.700000
VAFN	69.700000 V
VBEON	0.700000 V
BFP	227.300000
VAFP	37.200000 V
VEBON	0.700000 V
VCC	12.000000 V
RB1	80.000000 kOhm
RB2	20.000000 kOhm
RE1	200.000000 Ohm
RC1	900.000000 Ohm
RE2	50.000000 Ohm
C_{input}	0.100000 mF
C_{bypass}	2.500000 mF
C_{output}	1.500000 mF

Table 1: Values of components used in our analysis and simulation.

2 Theoretical Analysis

2.1 DC components

First of all, we performed an operating point analysis in order to check if the transistors were operating in the forward active region, both in the gain stage and in the output stage (since the output signal will not have a DC component, there isn't much more purpose to this part of the analysis). For DC analysis, we consider the capacitors to perform as open-circuits (low frequency approximation) - this way, no current flows through the input source and the load, so the DC voltage in both is null. The bias circuit was substituted by its Thévenin equivalent in order to make calculations more simple. The input source is purely sinusoidal, so both V_S and R_S don't come into play here. For the transistors we used a simplification of the Ebbers-Moll model for forward-active regions. With this, for npn transistors, the voltage drop must occur from the collector to base and from base to emitter - this last voltage drop is approximated with the ideal diode model voltage (0.7V). The current coming out of the emitter must be the sum of the base and collector currents. The same process happens with the pnp transistor, but in a symmetrical fashion. In table 2 we present the DC voltage data for the gain stage, and in table 3 we present the equivalent for the output stage We assumed the predicted current direction for I_C, I_B, and I_E, and all these currents are positive - so far so good. Since VCE is greater than VBEON, VCB is also positive, which means the voltage drop occurs from the collecter, to the base, to the emitter - the transistor does operate in the forward-active region

Again the transistor currents are all positive. The collecter is the ground in this case, and since VO2 (which is the same as VEC in this case) is greater than VEBON, VBC is also positive

Name	Values
RB	16000.000000 Ohm
VEQ	2.400000 V
IB1	0.000033 A
IC1	0.005849 A
IE1	0.005882 A
VE1	1.176319 V
VO1	6.736022 V
VCE	5.559704 V
V_{in}	0 V
V_{in2}	0 V
V_{vcc}	12 V
V_{base}	1.876319 V
V_{coll}	6.736022 V
V_{emit}	1.176319 V

Table 2: Operating point analysis results (gain stage).

Name	Values
IB2	0.000400 A
IC2	0.090880 A
IE2	0.091280 A
VO2	7.436022 V
V_{vcc}	12 V
V_{coll}	6.736022 V
V_{emit2}	7.436022 V
V_{out}	0 V

Table 3: Operating point analysis results (output stage).

- the voltage drop goes from the emitter all the way to the collector (ground in this case) and this transistor also operates in the forward-active region. We're good to go!

2.2 Gain Stage

Now, we move on to analyse the AC components. Recurring to the incremental model for a transistor, we were able to derive equations for the input and output impedances of the gain stage, as well as the voltage gain obtained for the output signal of this stage:

$$Z_i = R_B||r_\pi; \tag{2}$$

$$Z_o = R_{C1}||r_o; \tag{3}$$

$$A_V = -g_m * Z_o * \frac{Z_i}{Z_i + R_S}; \tag{4}$$

The constants used, r_π, r_o and g_m, are the input resistance, output resistance and transconductance of the incremental transistor model. In table 4 we present the results obtained (the negative gain only symbolizes the inversion of the voltage signal direction, and the gain is also calculated solely in relation to the voltage source, without the effect of its resistance):

The input impedance we obtained is considerably larger than R_S, which means we will not lose much voltage amplitude in the input part of this stage, which is appropriate. We can clearly

Name	Values
gm	0.233955 S
rpi	763.823529 Ohm
ro	11916.843872 Ohm
Input impedance	729.020826 Ohm
Output impedance	836.801914 Ohm
Gain	-172.158583
Gain(dB)	44.718574 dB

Table 4: Gain stage theoretical results.

see the need for an output stage though, given the magnitude of the output impedance - since it is so much greater than the load resistance, it would consume almost all voltage amplitude, leaving us with a very small voltage amplitude in the load, the exact opposite of our goal. The gain is also significant, and we'll strive for a unitary gain in the output stage in order not to sacrifice this.

2.3 Output Stage

Again, using the incremental model, we derived equations for the input and output impedances, and the gain of the output stage of the circuit:

$$A_V = \frac{g_\pi + g_m}{g_\pi + g_m + g_o + (\frac{1}{R_{E2}})}; \tag{5}$$

$$Z_i = \frac{r_\pi}{1 - A_V}; \tag{6}$$

$$Z_o = \frac{1}{\frac{1}{g_m}||r_\pi||r_o||R_{E2}}; \tag{7}$$

In table 5 we present the results obtained:

Name	Values
gm2	3.635189 S
rpi2	62.527694 Ohm
ro2	409.332200 Ohm
Input impedance	10234.962944 Ohm
Output impedance	0.272211 Ohm
Gain	0.993891
Gain(dB)	-0.053227 dB

Table 5: Output stage theoretical results.

As desired, the input impedance of this stage is more than 10 times greater than the output impedance of the gain stage. This is important because the output impedance of the gain stage and the input impedance of the output stage form a voltage divider, and the voltage in the output stage's input impedance is the one that follows through. Having a much greater impedance in this last impedance guarantees then a very small amplitude loss, which allows us to preserve the incoming gain. As well, the output impedance of this stage is desirably low when compared to the 8 Ohm of the speakers resistance, which allows the vast majority of the final gain to flow through the load, thus allowing us to truly have an amplified voltage in our output. The gain for this stage is almost unitary, which means the first stage gain is preserved, as hoped. At last, the total circuit gain results.

2.4 Global circuit

With the same model, we derived similar equations for the circuit as a whole, which will always to directly compare results with the NGSpice simulation (the input impedance is independent from the load, so it will be the same as the input impedance from the gain stage):

$$Z_o = \frac{1}{\frac{1}{r_{(\pi)2}+Z_{O1}}||g_{o2}||g_{m2}\frac{r_{(\pi)2}}{r_{(\pi)2}+Z_{O1}}||\frac{1}{R_{E2}}}; \tag{8}$$

$$A_V = \frac{\frac{1}{r_{(\pi)2}+Z_{O1}} + \frac{g_{m2}r_{(\pi)2}}{r_{(\pi)2}+Z_{O1}}}{\frac{1}{r_{(\pi)2}+Z_{O1}} + \frac{g_{m2}r_{(\pi)2}}{r_{(\pi)2}+Z_{O1}} + \frac{1}{R_{E2}} + \frac{1}{r_{o2}}}A_{V1}; \tag{9}$$

In table 6 we present the results obtained:

Name	**Values**
Input impedance	729.020826 Ohm
Output impedance	3.619271 Ohm
Gain	-158.174605
Gain(dB)	43.982735 dB

Table 6: Total circuit theoretical gain results.

The gain is slightly lower than the product of the two previous gains, likely due to some signal loss in the interface between stages. The output impedance is now clearly bigger, but still smaller than the load resistance. Even though we experience a greater loss of amplitude, we can still consider this set of data a good result depending on how big the gain is to compensate this increase in the output impedance.

2.5 Frequency response

Using the incremental model once again, but this time considering the capacitors' impedances, we ran a frequency response analysis for the gain and the phase difference of the output signal (on the load) in relation to the input signal (voltage source plus its resistance). We did this running a nodal method analysis of the incremental circuit for a vaste branch of frequencies. Figures 2 and 3 expose the results obtained:

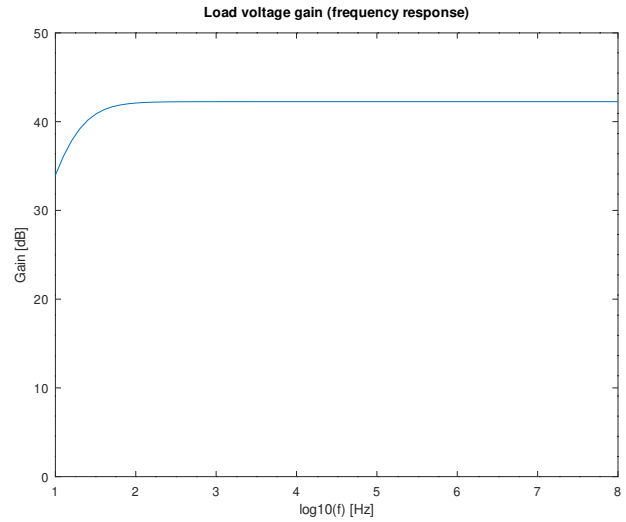

Figure 2: Load output voltage gain (frequency response).

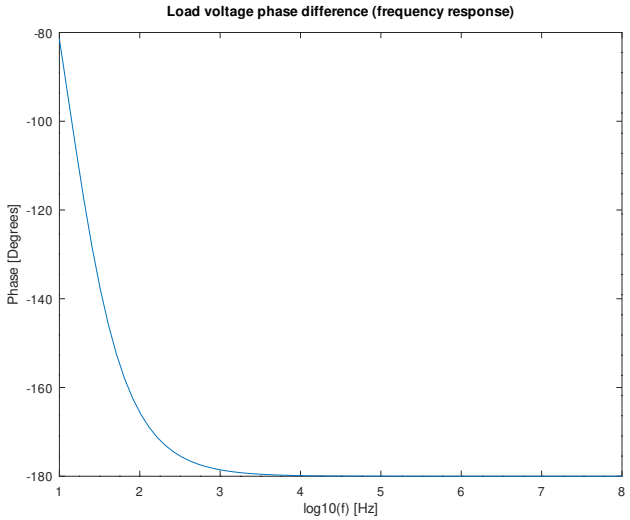

Figure 3: Load output voltage phase difference (frequency response).

Looking to the gain plot, we would be hoping to achieve the likes of a band-pass filter (as it will be obtained in simulation). However, we only achieved a high-pass filter. This is due to the fact that we didn't consider the capacitors of the transistors themselves, which would cause the gain to fall for high frequencies. With our plot, the gain stabilizes for medium frequencies, and keeps its momentum for high frequencies - the upper cut-off frequency is then something always tending to infinity with this model. We did manage to measure the lower cut-off frequency and a more accurate measure of gain for each frequency (since we considered the capacitors in this analyse). Regarding the phase plot, we notice that the phase difference stabilizes in the 180º degrees for medium frequencies, thus confirming the inversion of the signal voltage direction in the output. In table 7 we present the results:

The lower cut-off frequency yielded close to 20 Hz, the lowest frequency the human ear can perceive as a musical note, and the lower limit pretended for this amplifier - this is a very suitable result. This was achieved by finding the point on the gain frequency response plot that had a 3 decibel drop relative to the maximum gain.

Name	Values
Gain	129.600426
Gain(dB)	42.252129 dB
Lower cut-off frequency	20.432601 Hz

Table 7: Gain for medium frequencies and lower cut-off frequency of the output voltage signal.

3 Simulation Analysis

Since the input voltage source in this circuit is sinusoidal, the voltage and current values of the various components vary in time, and we are interested therefore in analysing how they evolve in time and obviously we want to picture the transformation of our AC input voltage source throughout the multiple stages of the circuit. We will run an operating point analysis in order to confirm the forward-active region of the two transisters, a transient analysis which will help us measuring the input and output impedances. We will also run a frequency response analysis in order to determine the gain and bandwidth of our output amplified sinusoidal signal. The transistors used were the Philips BJT's.

3.1 Operating point

We start with the operating point analysis. Given that the output signal will be solely sinusoidal, there isn't much relevance to this set of data. Its main goal is to confirm the forward-active region of both the npn and pnp transistors. In table 8 we present the operating point node voltages of the circuit. As expected, the voltage in nodes in e $in2$ since our source doesn't have a DC component. Our output signal doesn't have a linear voltage component, since the voltage in node out is zero, because the output coupling capacitor blocks the coming DC voltage. Regarding the npn transistor, the voltage drop must occur from the collector to the base, and from the base to the emitter - since $V_{coll} > V_{base} > V_{emit}$, this is confirmed. Looking to the pnp transistor, our collector node is ground, our base node is $coll$ and our emitter node is $emit2$. The voltage drop in this case must happen from the emitter to the collector. Since $V_{emit2} > V_{coll} > GND$, this is confirmed - both our transistors work in the pretended forward-active region.

Name	Values [V]
vcc[0]	1.200000e+01
in[0]	0.000000e+00
in2[0]	0.000000e+00
base[0]	1.878920e+00
coll[0]	7.214695e+00
emit[0]	1.184175e+00
emit2[0]	8.033675e+00
out[0]	0.000000e+00

Table 8: Operating point node voltage values of the amplifier circuit.

3.2 Frequency response and impedances

We measured the input impedance of the circuit, seen through the perspective of the source, and the output impedance, seen through the perspective of our output (using a dummy test source). With the frequency response, we measured the voltage gain in our output. As we will see in figure 5, the gain graph has the traits of a band-pass filter, letting pass medium

frequencies (our source operates at a medium frequency), so we measure the in that zone. We also measured then the lower and upper cut-off frequencies of such graph, in order to determine the bandwidth of our amplifier. In table 9, we present the results of our calculations. In figures 4and 5 we can see the evolution of the gain throughout the circuit, first the gain out of the gain stage - node $coll$ - and then the final gain, the gain out of the output stage - node out. With this figures we can confirm the band-pass filter trait of our circuit.

Name	**Values**
Gain	65.5843
Gain(dB)	36.336
Lower cut-off frequency	16.6025 Hz
Upper cut-off frequency	2.47423E+06 Hz
Bandwidth	2.47421E+06 Hz
Input impedance	0.856866 kOhm
Output impedance	8.18142 Ohm

Table 9: Output gain, bandwidth, and input and output impedances of the audio amplifier circuit (as a whole).

Analysing both the input and output impedances of the circuit, the input impedance is pretty satisfactory as it allows the vast majority of input voltage to go through the transistors, which means a low voltage loss. However, comparing the value of the output impedance with the load resistor, they are very much comparable. This means that part of the gain coming from the transistors will be consumed by some of our resistors in the circuit, hence losing a considerable part of the possible output gain. However, given the gain value we obtained, the overall result is very satisfying.

3.3 Final product and merit

In figure 6, we can see the evolution of our AC signal from stage to stage until its final form. The output voltage has a null DC component as pretended, a symmetric phase in comparison to the input source (it's inverted) and a clear greater amplitude of approximately 0.55V, in comparison to the input's 10mV. We can say then that we have achieved the goal of amplifying our input signal, in this case, by 50-60 times! In table 10, we present the cost and merit of our circuit. When looking to the parameters judged by the merit formula, we achieved an amazing bandwidth that clearly operates in the 20Hz-20kHz frequency band pretended, since we have an upper cut-off frequency in the zone of MHz, and a lower cut-off frequency inferior to 20Hz - $\approx$16Hz. The voltage gain could always be a bit higher, but without a defined pretended output amplitude, we can't really evaluate our achieved gain. Since we achieved a merit similar to 2326, the high cost seems like a reasonable price to pay for a circuit with these results. We were able however to achieve greater values of gain, but the output sinusoidal wave would be distorted, almost "cut-off" in its positive voltage periods, which was clearly not desirable, so we escaped from such happening, no matter the increase of gain it delivered.

Name	**Values**
cost	4.201458e+03
merit	2.326284e+03

Table 10: Cost and merit of the audio amplifier circuit.

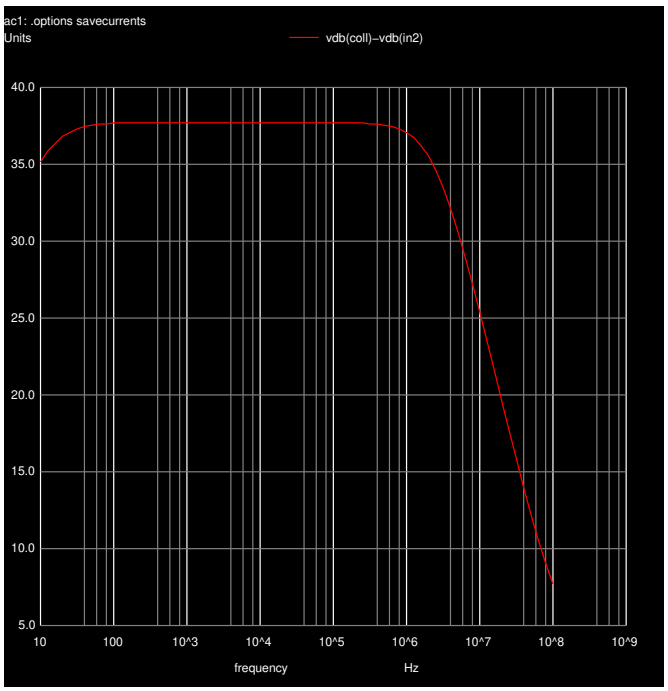

Figure 4: Gain Stage output voltage gain (frequency response).

4 Conclusion

In this laboratory assignment, we managed to build an audio amplifier circuit which is represented in Figure 1. The first step of our analysis was to determine the operating point values of the circuit to ensure the transistors were working in the forward active region. The results from the theoretical and simulation analysis confirm that the transistors were operating in this region for each case. It should be noted that there is a small difference in the node voltages between the two analysis. For the theoretical analysis, we used the ideal transistor model, which is based on the ideal p-n diode model. In this model, we assumed the voltage drop happening on the base-emitter junction of the npn and pnp transistors while it is forwardly biased to be constant, VBEON=0.7. However, in reality, this value oscillates which is taken into account in NGspice. These errors can also be further enhanced by greater values of resistances, like the case of RC1.

In the second part of our analysis, we set off to determine the incremental values of the circuit in order to compute its frequency response, as well as its output gain and input/output impedances. According to Table 11, the discrepancy between the simulation and theoretical values is more significant, particularly in the gain . According to the small signal models, the incremental variables of the transistors depend upon its operating point. Therefore, we can assume the errors committed in the operating point analysis to have been carried to the computation of the Gain and frequency response. These calculations were derived from the

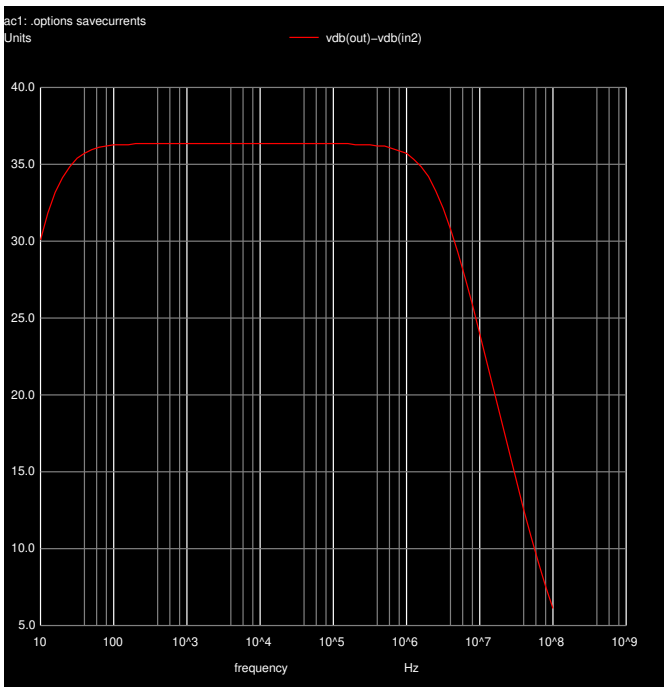

Figure 5: Load output voltage gain (frequency response).

Ebers-Moll model which does not consider non-ideal effects such as the base-width modulation and recombination in the depletion region. These effects break the linear relationship between the transistor values assumed in the theoretical analysis. Another very important cause is the approximation for high frequencies that we used for the capacitors, which neglets their effect (they become short-circuits). Given that we are studying medium frequencies, this a major source of error in our theoretical analysis, since it disregards the capacitors' impedances, in order to simplify calculations. The exception to this was the frequency response analysis, which did produce more accurate results, even though they were still visually different from the simulated ones, due to other factors.

Despite the discrepancies that have been exposed, it should be noted that both analyses yielded satisfactory results for the input and output impedances. The values for the input impedance are approximately 729 Ohm (theoretical) and 857 Ohm (simulation). Despite the error of 18 percent, the value obtained for the real input impedance is still acceptable given the fact that the typical range for professional microphone output impedances is 50-500 Ohms. Therefore, our circuit would be suitable as a microphone amplifier. This same comment can be applied to the output impedance of our circuit. Both theoretical and simulation values land within the typical range for speaker impedance. In the case of this assignment, our circuit is perfectly suitable for the 8 Ohm speaker. Furthermore, when it comes to the frequency response of the circuit, as for the lower cut-off frequency, the values obtained matched perfectly. However, we didn't manage to obtain a value for the higher cut-off frequency within the selected

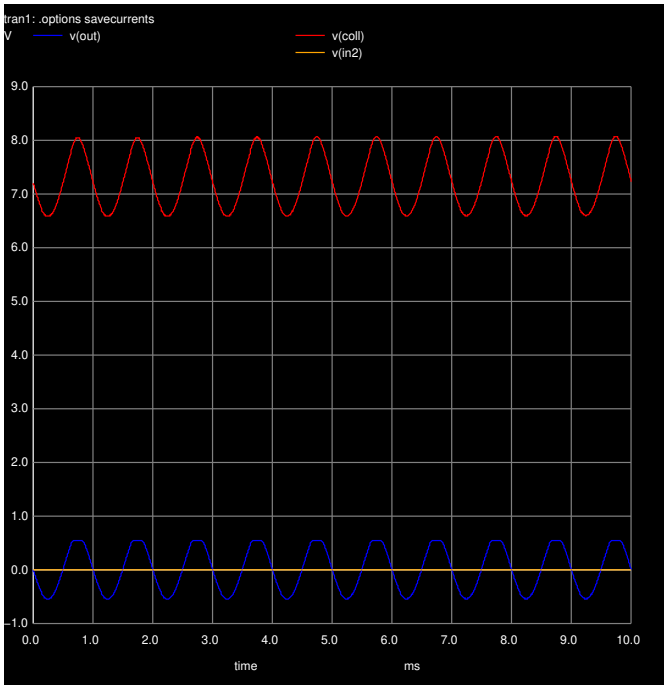

Figure 6: Evolution of the AC signal from input to output.

spectrum in the theoretical analysis. This can be explained by the fact that we disregarded the transistor's internal capacitances in the calculations. That is not the case in the simulation. NGspice accounts for all the variables of the transistor and, therefore, we obtained an upper cut-off frequency of 2.47423+06 Hz. With this, we managed to obtain a circuit that can clearly operate in the 20Hz-20kHz frequency band, making it perfect as an amplifier.

Theoretical	**Value**	**Simulation**	**Value**
Operating point			
V_{vcc}	12 V	vcc[0]	1.200000e+01 V
V_{in}	0 V	in[0]	0.000000e+00 V
V_{in2}	0 V	in2[0]	0.000000e+00 V
V_{base}	1.876319 V	base[0]	1.878920e+00 V
V_{coll}	6.736022 V	coll[0]	7.214695e+00 V
V_{emit}	1.176319 V	emit[0]	1.184175e+00 V
V_{emit2}	7.436022 V	emit2[0]	8.033675e+00 V
V_{out}	0 V	out[0]	0.000000e+00 V
Frequency response and impedances			
$Gain$	158.174605	Gain	65.5843
$Gain(dB)$	43.982735 dB	Gain(dB)	36.336 dB
$LowerCut-offFreq$	20.432601 Hz	Lower cut-off freq	16.6025 Hz
$UpperCut-offFreq$	-	Upper cut-off freq	2.47423E+06 Hz
$Bandwidth$	-	Bandwidth	2.47421E+06 Hz
$InputImpedance$	729.020826 Ohm	Input impedance	0.856866 kOhm
$OutputImpedance$	3.619271 Ohm	Output impedance	8.18142 Ohm

Table 11: Comparison of the theoretical and simulated data results, regarding the operating point, frequency response and impedances.