Circuit Theory and Electronics Fundamentals

MEAer (Integrated Master In Aerospace Engineering), Técnico, University of Lisbon

Laboratory 5: OP-AMP bandpass filter

Group 3

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Contents

1 Introduction **2**

2 Theoretical Analysis **3**

2.1 Circuit frequency response 3

2.2 Central frequency results 4

3 Simulation Analysis **5**

3.1 Frequency response and impedances 5

3.2 Final product and merit 6

4 Conclusion **7**

1 Introduction

The objective of this laboratory assignment is to build a BandPass Filter (BPF) circuit whose specifications are: a central frequency at 1000Hz and a gain at central frequency of 40dB. In order to achieve this, we used a selected number of components whose properties were predefined. Our circuit is comprised of a μA741 OPAMP connected to two resistors, creating a non-inverting amplifier, and a combination of resistors and capacitors to take care of the filtering. These components are arranged according to figure 1.

The signal goes through a first stage where we have a capacitor whose function is to block unwanted DC current and to filter out lower frequencies, hence this stage being a high pass filter, since the rest of the circuit is connected to the terminals of the resistor. Now the signal goes through a combination of resistors and a μ741 OPAMP. This arrangement creates a non-inverting amplifier. In this configuration, the output signal is "in-phase" with the input signal. Feedback control of the non-inverting OPAMP is achieved by applying a small part of the output voltage back to the inverting (-) terminal via R3-R4 voltage divider network. And finally, the signal is subjected to a voltage divider network comprised of resistor R2 and capacitor C2. The desired voltage corresponds to the voltage drop at the terminals of the capacitor which, as a result, is subjected to a low pass filtering. For this to run, we need two supply DC voltage sources overlapped with our main circuit in order to power the transistors inside the OPAMP.

For this laboratory assignment there is a figure of merit, depending on the results obtained in the NGSpice simulation. This figure takes into account the cost of the components used, and the results they provide - a desirably low gain deviation and low central frequency deviation. The figure is calculated using the formula given by equation 1. The cost englobes the cost of transistors (0.1 units per transistor), diodes (0.1 units per diode), resistors (1 unit per KOhm) and capacitors (1 unit per uF). The objective is to achieve the highest merit, so we tried different configurations of components data until we achieved our greatest figure of merit.

$$M = \frac{1}{Cost * (GainDeviation + CentralFrequencyDeviation + 10^{-6})} \tag{1}$$

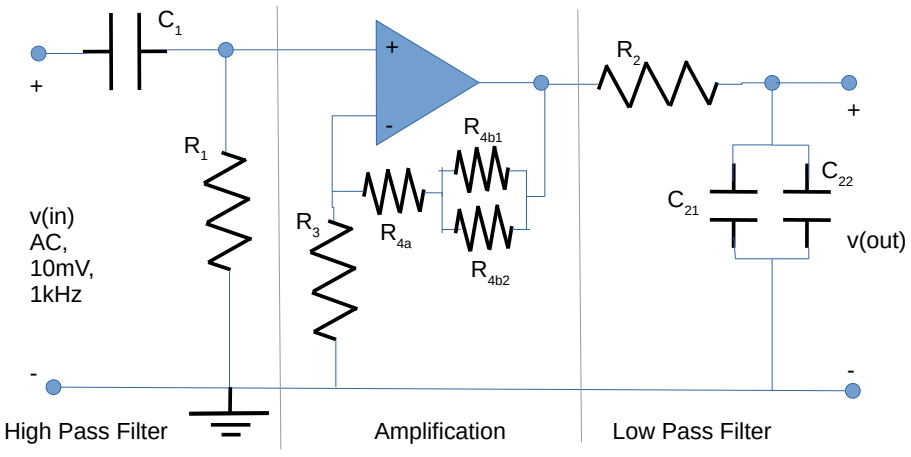

Figure 1: Geometry of our Band-Pass filter circuit.

To analyse this circuit theoretically we computed the transfer function for each stage in order to obtain the overall transfer function. Using the incremental model, we determined the input and output impedances of the overall circuit. That being said, in Section 2 we present the theoretical models and calculations used to determine the transfer function and, therefore, the

frequency response of the circuit, in Section 3 we introduce the results obtained in the simulation. Finally, in Section 4 we compare the two sets of results, looking for possible discrepancies and we lay out our conclusions. In Table 1, we list the numeric values of the components used:

Name	Values
R_1	1.000000 kOhm
C_1	0.220000 uFarad
R_2	1.000000 kOhm
C_{21}	0.220000 uFarad
C_{22}	0.220000 uFarad
R_3	1.000000 kOhm
R_{4a}	100.000000 kOhm
R_{4b1}	100.000000 kOhm
R_{4b2}	100.000000 kOhm

Table 1: Values of components used in our analysis and simulation.

2 Theoretical Analysis

2.1 Circuit frequency response

With the following equations we determined both cutoff frequencies for the band pass circuit (the lower cut-off frequency appears from the high-pass stage, and the upper cut-off frequency appears from the low-pass stage):

$$w_L = \frac{1}{R_1 C_1} \tag{2}$$

$$w_H = \frac{1}{R_2 C_2} \tag{3}$$

This was the definition used to determine the central frequency, which is meant to be 1 kHz.

$$w_O = \sqrt{w_H w_L} \tag{4}$$

Name	Values
Lower Cut-Off Frequency	723.431560 Hz
Upper Cut-Off Frequency	1446.863119 Hz
Central Frequency	1023.086723 Hz

Table 2: Cut off frequencies and central frequency.

This central frequency result represents a 2.309% relative error, which is a fairly great result, that we hope to replicate in the simulation.

As wanted, the plot has the trait of a narrower band-pass filter, with its top gain arriving in the 1 kHz neighbourhood, and the gain itself is on the 40 dB as pretended.

The phase drops from 90 degrees to -90 degrees, which is cause of the 2 poles of the transfer function (which we will present in the next subsection), one pole introduced by the high-pass and the other pole introduced by the low pass. Each pole causes a 90 degree drop, 45º the decade before and 45º the decade after. At the central frequency, the phase is zero, which means the output voltage is in phase with the input voltage.

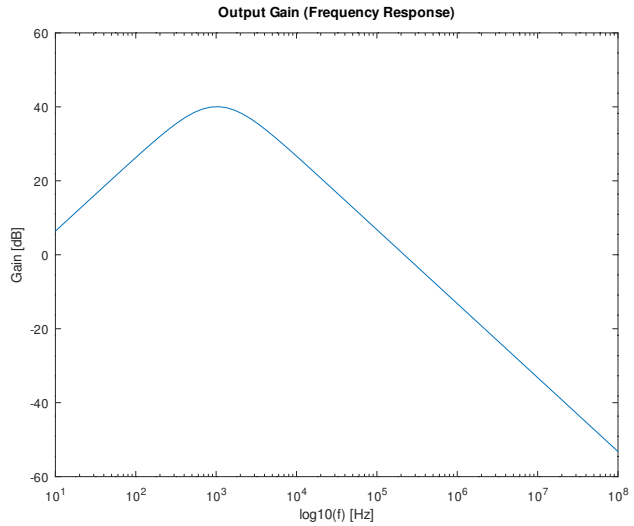

Figure 2: Voltage gain frequency response.

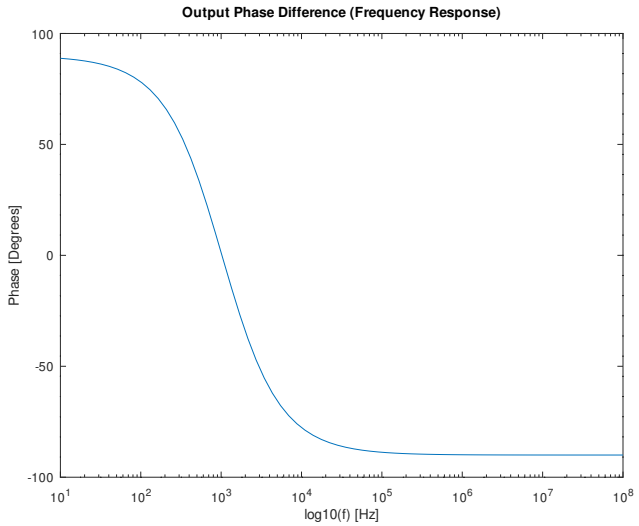

Figure 3: Voltage phase frequency response.

2.2 Central frequency results

For the mentioned central frequency we computed the circuit gain and input and output impedances for the amplifier. Also, we determined a theoretical figure of merit based on the predicted results with the set of values we chose.

The gain value for the entire circuit is obtained by multiplying the individual gains of each of the three stages of the circuit. This is an ideal situation, where we don't take into account the loss of signal between stages, or charge effects between the same stages. These are the equations for the gain values:

$$HighPassGain = |\frac{R_1 C_1 j w_O}{1 + R_1 C_1 j w_O}| \tag{5}$$

$$AmplifierGain = 1 + \frac{R_4}{R_3} \tag{6}$$

$$LowPassGain = |\frac{1}{1 + R_2 C_2 j w_O}| \tag{7}$$

Using the incremental model for the circuit (the input impedance of the OP-AMP is infinite and the output impedance of the OP-AMP is nule, according to the model studied in classes), we determined the following equations for the input and output impedances of the circuit:

$$Z_i = R_1 + \frac{1}{jw_O C_1} \tag{8}$$

$$Z_o = \frac{R_2}{1 + jw_O R_2 C_2} \tag{9}$$

Name	**Values**
Gain	100.666667
Gain (dB)	40.057714 dB
Z_{in}	1000.000000 -707.106781j Ohm
Z_{in} modulus	1224.744871 Ohm
Z_{in} phase	-35.264390 Degrees
Z_{out}	666.666667 -471.404521j Ohm
Z_{out} modulus	816.496581 Ohm
Z_{out} phase	-35.264390 Degrees
Cost	13626.952040MU
Merit	$3.089411 * 10^{-6}$

Table 3: Gain, input and output impedances at the central frequency.

We obtained then a relative error of 0.667% for the gain at central frequency, which is meant to be 100, so this a fantastic theoretical result. The input impedance value is quite high, which is good, so, depending on the resistance of the input, most of the input voltage will flow through ahead to the OP-AMP as pretended. The output impedance value though is quite large, so this circuit will not be suited to loads with very low resistance values, but given the components we had available there wasn't much room for improvement. Also, we don't know the load that would be linked to this circuit, so we can't fully know how good or bad this value is, we just know it is clearly not the most desirable.

3 Simulation Analysis

Since the input voltage source in this circuit is sinusoidal, the voltage and current values of the various components vary in time, and we are interested therefore in analysing how they evolve in time and obviously we want to picture the transformation of our AC input voltage source from the input to the output of the circuit. We will run a transient analysis which will help us measuring the input and output impedances. We will also run a frequency response analysis in order to determine the gain and central frequency of our output amplified sinusoidal signal.

3.1 Frequency response and impedances

We measured the input impedance of the circuit, seen through the perspective of the source, and the output impedance, seen through the perspective of our output (using a dummy test source). With the frequency response, we measured the voltage gain in our output and the lower and upper cut-off frequencies. Using the same equation from the theoretical analysis we determined the central frequency, then extracting the output gain for such frequency. In table 4, we present the results of our calculations. In figures 4and 5 we can see the frequency response for our output's gain and phase, respectively. With this figures we can notice a slightly

narrow band-pass filter, as expected and wanted. Regarding the phase plot though, we notice a full circle phase drop until it reaches the 90 degrees back again, whereas in the theoretical analysis the phase drops from 90 degrees to -90 degrees, stabilizing there. This difference is cause of the aproximation used to study the OP-AMP behaviour in the theoretical section. For study purposes, we considered the OP-AMP did not introduce any phase difference in its output compared to its input, which is not true in reality. Due to the two transistors used in the uA741 OP-AMP, the transfer function in this sector actually presents 2 poles, which causes a double phase drop of 90 degrees (45 degrees the decade before and 45 degrees the decade after) each, which then means the phase actually drops 180 degrees due to the OP-AMP, hence stabilizing not in -90 degrees, but in 90 (-270) degrees.

Name	**Values**
Gain	99.7361
Gain(dB)	39.977
Lower cut-off frequency	403.611 Hz
Upper cut-off frequency	2386.17 Hz
Bandwidth	1982.56 Hz
Central frequency	981.37 Hz
Input impedance	0.999979 + j*-0.723583 kOhm
Input impedance modulus	1.23431 kOhm
Input impedance phase	-35.8894 degrees
Output impedance	0.68172 + j*-0.46675 kOhm
Output impedance modulus	0.826194 kOhm
Output impedance phase	-34.3981 degrees

Table 4: Output gain, center frequency, and input and output impedances of the OP-AMP band-pass filter.

Our input impedance value is reasonably high, so, depending on the input signal's inner resistance, it does allow the great majority of the input voltage to flow through ahead to the OP-AMP. That being said, the output impedance value is also considerably high, which in this case is not desirable. This means that for loads with low resistance values, most of the voltage will be consumed by the circuit's output impedance itself, undoing its very purpose. This band-pass filter is then better suited for loads with greater resistance values. Given the components we had at our disposal, it was very difficult to accomplish a lower value for the output impedance, specially without comprimising the most important goal of this laboratory assignment. Looking now to the central frequency obtained, and the gain for such frequency, we had very slight deviations from the targeted values - 1 kHz and 40 dB. That being said, we obtained a 1.863% relative error for the central frequency value, and a 0.264% error for the output voltage gain, which we consider to be fantastic results, when we take into account the limited components available, which made optimization more difficult than usual.

3.2 Final product and merit

In figure 6, we can compare the output signal to the input. As normal, the output voltage does not possess a DC component. Since the wanted gain was 40 dB, which is the same as 100$\times$ the initial amplitude, we can see the clear evolution from the starting 10mV to the final 1V of amplitude (more or less). For the first few milisseconds there is some small variation in the output sinusoidal wave due to a small transient regime. In table 5, we present the cost and merit of our circuit. As we've already discusseed, we obtained a central frequency and gain very close to the targeted ones, which is expressed by very low relative erros, and therefore very small deviations. The overall cost of the circuit is considerably high, but that is mainly due

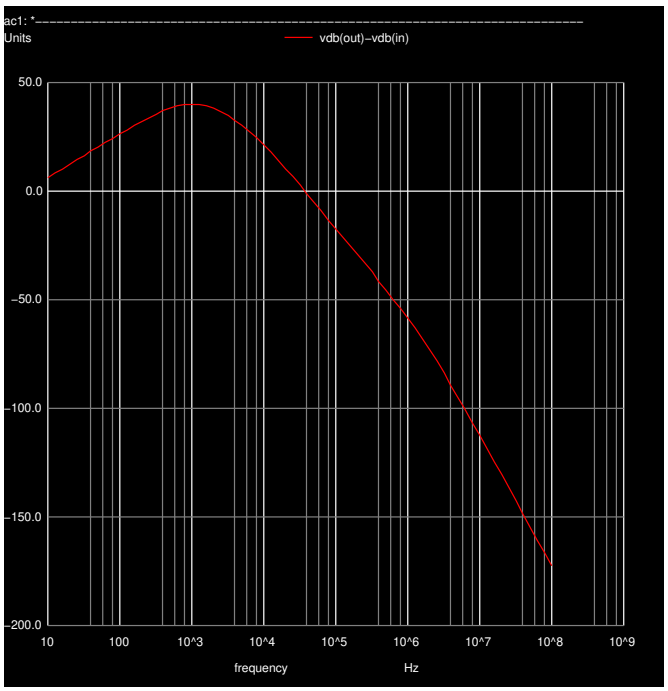

Figure 4: Output voltage gain (frequency response).

to the high cost of the OP-AMP subcircuit itself. Because of this, using higher cost components in the rest of the circuit became more tolerable, since it wouldn't create as much of an effect in the overall cost value. Because of this we used the three 100 kOhm resistors available in the amplification stage, which allowed us to get an almost perfect gain for the central frequency, without harming the merit figure. The merit figure itself is clearly a very low number, but we believe that is only cause of the merit formula itself.

Name	Values
cost	1.362695e+04
merit	3.883972e-06

Table 5: Cost and merit of the OP-AMP band-pass filter.

4 Conclusion

In this laboratory assignment, we managed to build a BandPass Filter (BPF) circuit which is represented in Figure 1. The first step of our analysis was to determine the frequency response by computing the transfer function of the whole circuit.

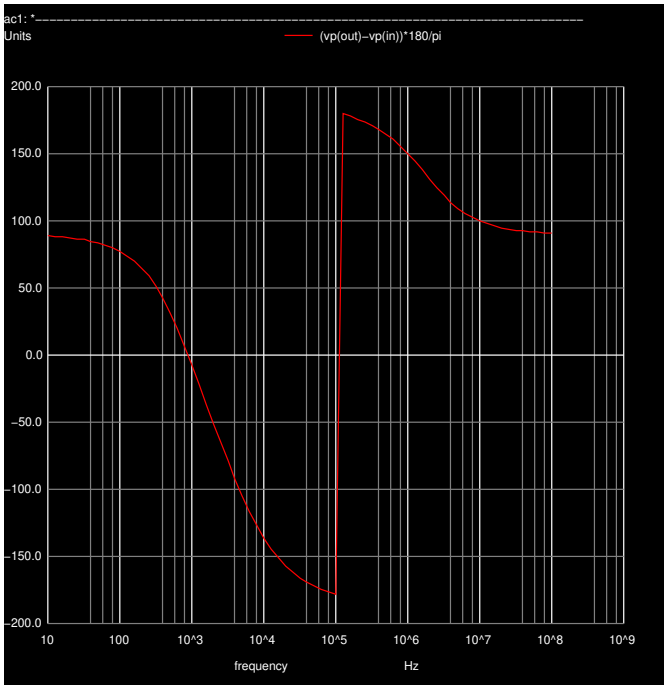

Figure 5: Output voltage phase difference (frequency response).

Theoretical	**Value**	**Simulation**	**Value**
Frequency response and impedances			
$Gain$	100.666667	Gain	99.7361
$Gain(dB)$	40.057714 dB	Gain(dB)	39.977 dB
$LowerCut-offFreq$	723.431560 Hz	Lower cut-off freq	403.611 Hz
$UpperCut-offFreq$	1446.863119 Hz	Upper cut-off freq	2386.17 Hz
$CentralFreq$	1023.086723 Hz	Central freq	981.37 Hz
$Z_{in}Modulus$	1224.744871 Ohm	Zin modulus	1.23431 kOhm
$Z_{in}Phase$	-35.264390 Degrees	Zin phase	-35.8894 Degrees
$Z_{out}Modulus$	816.496581 Ohm	Zout modulus	0.826194 kOhm
$Z_{out}Phase$	-35.264390 Degrees	Zout phase	-34.3981 Degrees
$Cost$	13626.952040	Cost	1.362695e+04
$Merit$	3.089411*10^{-6}	Merit	3.883972e-06

Table 6: Comparison of the theoretical and simulated data results, regarding the frequency response and impedances.

The results from the theoretical and simulation analysis confirm that the transistors were operating in this region for each case. It should be noted that there is a small difference in the node voltages between the two analysis. For the theoretical analysis, we used the ideal

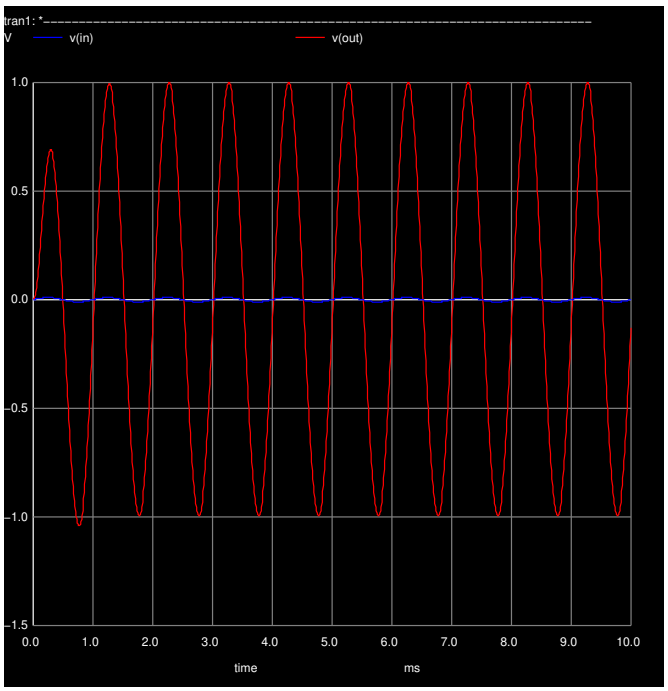

Figure 6: Comparison between the input and the output sinusoidal signals.

transistor model, which is based on the ideal p-n diode model. In this model, we assumed the voltage drop happening on the base-emitter junction of the npn and pnp transistors while it is forwardly biased to be constant, VBEON=0.7. However, in reality, this value oscillates which is taken into account in NGspice. These errors can also be further enhanced by greater values of resistances, like the case of RC1.

In the second part of our analysis, we set off to determine the incremental values of the circuit in order to compute its frequency response, as well as its output gain and input/output impedances. According to Table 11, the discrepancy between the simulation and theoretical values is more significant, particularly in the gain . According to the small signal models, the incremental variables of the transistors depend upon its operating point. Therefore, we can assume the errors committed in the operating point analysis to have been carried to the computation of the Gain and frequency response. These calculations were derived from the Ebers-Moll model which does not consider non-ideal effects such as the base-width modulation and recombination in the depletion region. These effects break the linear relationship between the transistor values assumed in the theoretical analysis. Another very important cause is the approximation for high frequencies that we used for the capacitors, which neglets their effect (they become short-circuits). Given that we are studying medium frequencies, this a major source of error in our theoretical analysis, since it disregards the capacitors' impedances, in order to simplify calculations. The exception to this was the frequency response analysis,

which did produce more accurate results, even though they were still visually different from the simulated ones, due to other factors.

Despite the discrepancies that have been exposed, it should be noted that both analyses yielded satisfactory results for the input and output impedances. The values for the input impedance are approximately 729 Ohm (theoretical) and 857 Ohm (simulation). Despite the error of 18 percent, the value obtained for the real input impedance is still acceptable given the fact that the typical range for professional microphone output impedances is 50-500 Ohms. Therefore, our circuit would be suitable as a microphone amplifier. This same comment can be applied to the output impedance of our circuit. Both theoretical and simulation values land within the typical range for speaker impedance. In the case of this assignment, our circuit is perfectly suitable for the 8 Ohm speaker. Furthermore, when it comes to the frequency response of the circuit, as for the lower cut-off frequency, the values obtained matched perfectly. However, we didn't manage to obtain a value for the higher cut-off frequency within the selected spectrum in the theoretical analysis. This can be explained by the fact that we disregarded the transistor's internal capacitances in the calculations. That is not the case in the simulation. NGspice accounts for all the variables of the transistor and, therefore, we obtained an upper cut-off frequency of 2.47423+06 Hz. With this, we managed to obtain a circuit that can clearly operate in the 20Hz-20kHz frequency band, making it perfect as an amplifier.