EC 413

Pipelined CPU Lab 8 Report

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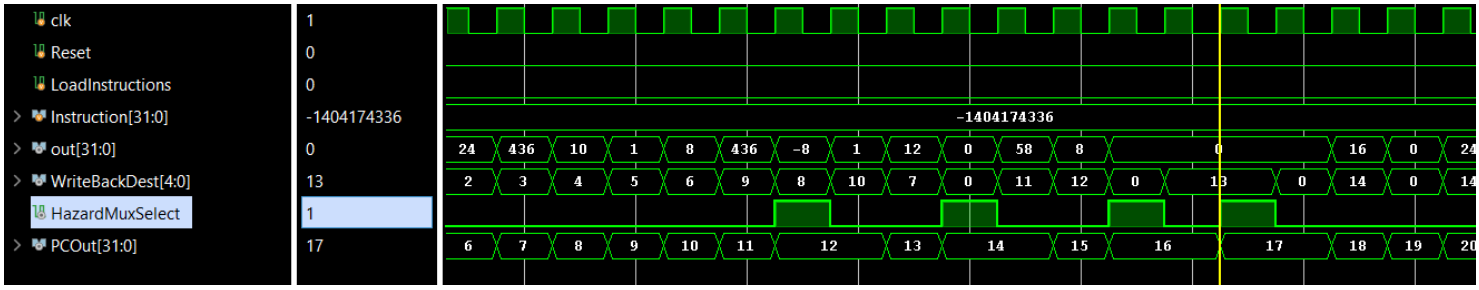
Waveform:



Testbench:

```
Instruction = 32'b100011_00000_00110_0000000000001000;  // LW $R6, 8(R0)
#10;
Instruction = 32'b000000_00110_00011_01001_00000_100101; //or  $R9, $R6, $R3  1 ahead hazard
#10;
Instruction = 32'b000000_00001_00010_01000_00000_100010; //sub  $R8, $R1, $R2
#10;
Instruction = 32'b000000_00101_01001_01010_00000_100000; //add  $R10, $R5, $R9
#10;
Instruction = 32'b101011_00000_00111_0000000000001100;  // SW   $R7, 12(R0)
#10;
Instruction = 32'b001000_01010_01011_0000000000111001; //addi $R11, $R10, 57 2 ahead hazard
#10;
Instruction = 32'b000000_00111_00010_01100_00000_100100; //and  $R12, $R7, $R2
#10;
Instruction = 32'b000000_00100_01100_01101_00000_100100; //and  $R13, $R4, $R12 1 ahead hazard
#10;
Instruction = 32'b000000_01011_01100_01101_00000_101010; //slt  $R13, $R11, $R12
#10
Instruction = 32'b100011_00000_01110_0000000000010000;  // LW $R14, 16(R0)
#10
Instruction = 32'b101011_00010_01110_0000000000000000;  // SW $R14, 0(R2) RAW hazard
#10;
```

For the testbench, we used the provided code and then added 3 additional instructions to show two 1-ahead hazards and one 2-ahead hazard. The testbench includes 4 types of hazards that our hazard flag detects creates the appropriate stall as seen in PC Out.

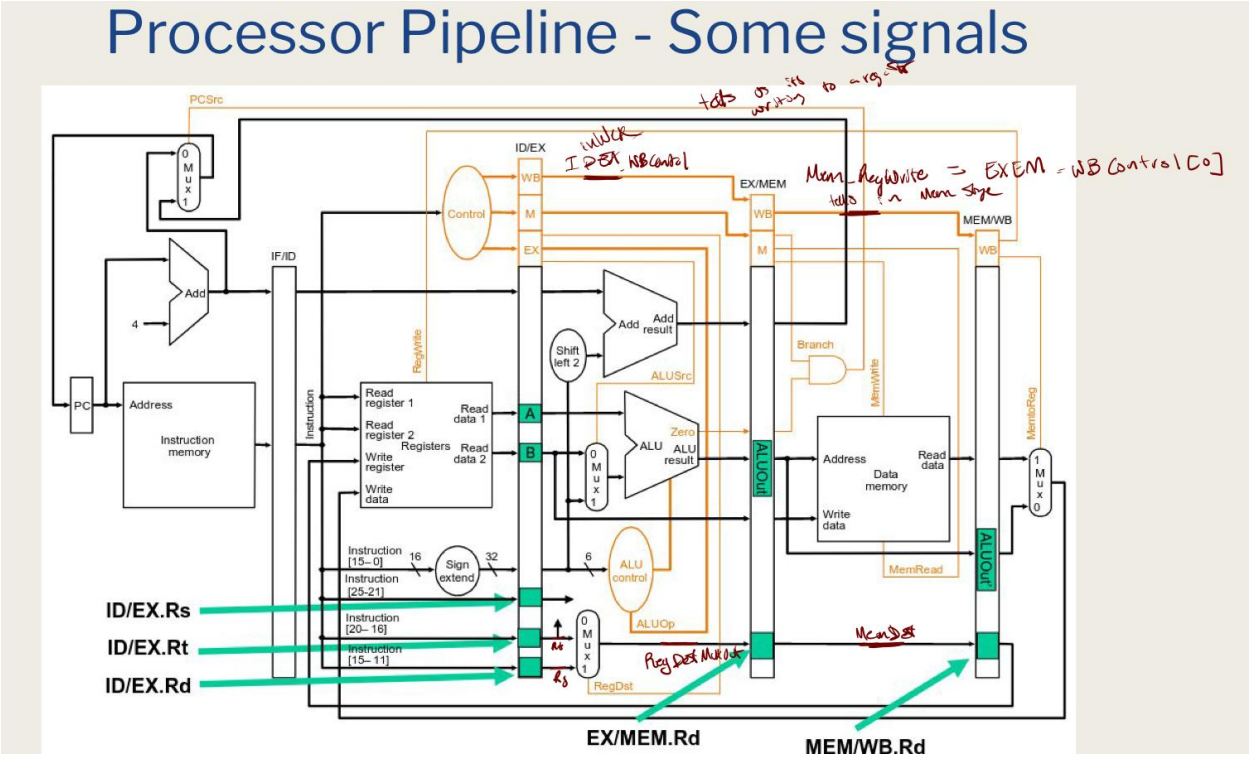
1-ahead Hazard:

In order to detect a 1-ahead hazard, in our hazardunit.v module we compared IDEX_Rd to IDEX_Rs and IDEX_Rt, and depending on if either of those conditions were true, in conjunction with inWex and IDEX_Rd != 0, it would modify IFIDWrite, PCWrite, and HazardMux to stall the pipeline 1 cycle. This part compares the control signals from stage 1 to stage 2 of the pipeline.

2-ahead Hazard:

In order to detect a 2-ahead hazard, in our hazardunit.v module we compared EXMEM_Rd to IDEX_Rs and IDEX_Rt, and depending on if either of those conditions were true, in conjunction with inWmem and when EXMEM_Rd != 0, it would modify IFIDWrite, PCWrite, and HazardMux to stall the pipeline 2 cycles. This part compares the control signals from stage 1 to stage 3 of the pipeline.

Schematic:



This schematic as provided by the Discussion slides aided our understanding of the appropriate control signals and wires.