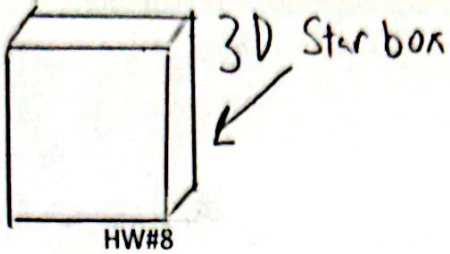


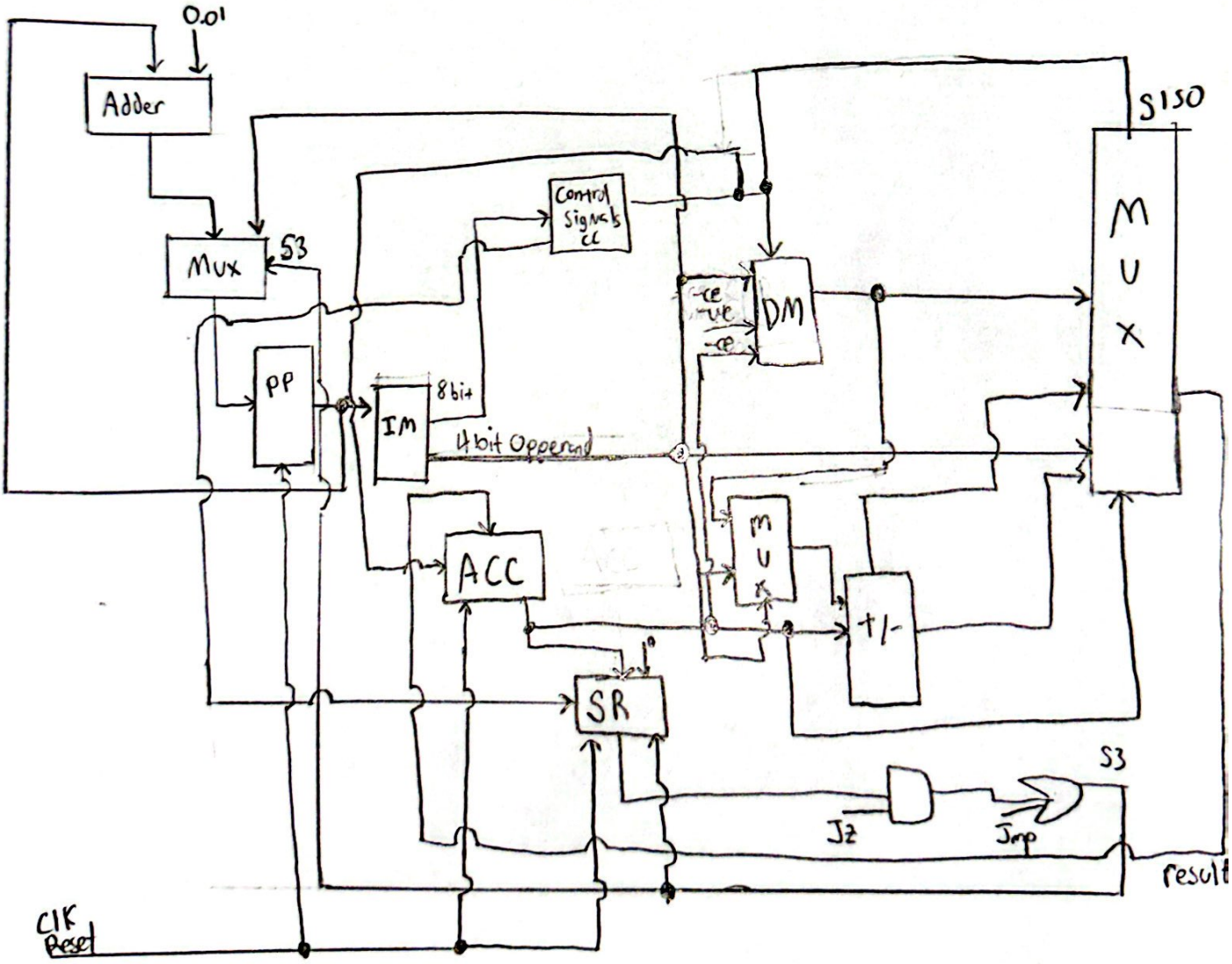
HW#8

CSc 137 (50 pts)

8.3 An Acc-ISA CPU executes the following instructions using 4-bit op-codes and 4-bit address or 2's complement data. Do the following:

LD address	//Acc ← Memory [address], read from LM2
LD data	//Acc ← data (a 2's complement number, sign extended)
ADD data	//Acc ← Acc + data (data is a 2's complement number, sign extended)
SUB data	//Acc ← Acc - data (data is a 2's complement number, sign extended)
ADD (address)	//Acc ← Acc + Memory[address]
STM (address)	//M[address] ← Acc
SUB (address)	//Acc ← Acc - Memory[address]
JMP address	//PP ← address
JZ address	// PP ← address (if result of the operation was zero)

a) Draw a data path for the CPU assuming the DM has separate input and output bus as in the data path shown in Fig. 8.7. Do not include additional data paths not used by the instructions. **(40 pts)**



Problem I. Computation is performed by a RISC ISA. A = B * (C + D). What is the value in R4 after the execution of code line # 6: (B = 5; C = 10; D = 15) ie: Code line # 6 has been completed. (10 pts)

R4 = 5

RISC-ISA: Example of assembly program

1. LD	R1,	(C)		R1 ← 10
2. LD	R2,	(D)		R2 ← 15
3. ADD	R3,	R1, R2		R3 ← 25
4. LD	R4,	(B)		R4 ← 5
5. MUL	R5,	R3, R4		R5 ← 125
6. ST	(A),	R5		A ← 125