CSC 137 11/6/23 HW6

Single cycle

A propagation delay on an 8 bit adder = 0.8 ns, adder/subtractor = 1.1 ns
2 to 1 Mux = 0.3 ns } 4 to 1 mux is 0.6 ns. Assume Tst, Tcq Tcs = 0.05 ns
Adder + Adder + Adder/subtractor + Tst + Tcq + Tcs =
0.8 + 0.8 + 1.1 + (0.5 · 3)
0.8 + 0.8 + 1.1 + .15 = 2.85 $\frac{1}{\text{clockwidth}} = \frac{1}{2.85}$ or $\frac{1}{2.85 \cdot 10^{-9}}$

$= 350 \times 277 \times 2 \frac{\text{cycles}}{1 \text{ sec}} \cdot \frac{1 \text{ mhz}}{10^6} = 350 \text{ mhz}$

Multi cycle

B. Adder/subtractor + mux1 + mux2 + Tst + Tcq + Tcs
(1.1 + 0.3 + 0.6 + .15) = 2.15 or $\frac{1}{\text{Tcq + Tcs + Tcq}} = \frac{1}{2.15 \cdot 10^{-9}} = 465116279$

$465 \times 6279 \frac{\text{cycles}}{\text{sec}} \cdot \frac{1 \text{ mhz}}{10^6} = 465 \text{ mhz}$

C Add/sub + .15 ← Tcq + Tst + Tcs
(1.1 + .15) 1.25 $\frac{1}{1.25 \cdot 10^{-9}} = 800\,000\,000$

$800\,000\,000 \frac{\text{cycles}}{\text{sec}} \cdot \frac{1 \text{ mhz}}{10^6} = 800 \text{ mhz}$

6.2 Estimate Speed up between the data paths N = 1000 For $A_i + B_i + C_i \pm D_i$ For i = 0, 1, 2 ... 999. K = 3 Ignore data reading } writing delay

K = 3 } N = 1000 $\frac{NK}{(k+n-1)}$ $\frac{1000 \cdot 3}{1002} = 2.99$

K = 1 } N = 1000 $\frac{NK}{(k+n-1)}$ $\frac{1000 \cdot 1}{1+1000-1}$ $\frac{1000}{1000} = 1$

Extra Credit Attempt

Current	input	Next	output
q_0	X	d_0	Z
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

When input bit = 0 } constant previous value

000 0010 1111 0101 011

1111 0000 1110 0011