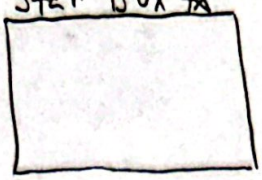
Ruben Ortega
CSC 137 Hw 7

Star Box ☆



1. In order to minimize the duration of a read cycle, the -oe can be asserted at any time within a maximum time after the -ce is asserted as illustrated in the timing diagram
A (True) B False

2. A memory write cycle is similar to a read cycle, except that data must be placed on the data bus as the same time that -ce is asserted or within a maximum delay after -we is asserted to minimize the time the data bus is used
1.A A memory cycle is initiated by which component in the computer motherboard. The CPU
1B. A memory cycle, typically, how many CPU clock cycles to complete. Multiple clock cycles

7.10 Consider a 32 bit data bus SDRAM. Given that the clock frequency of the bus is 200 MHz, what is the peak memory bandwidth in megabyte per seconds MBs. Frequency
(width / type of memory)
32 bit data bus

$$\frac{32 \text{ bits}}{1 \text{ cycle}} \cdot \frac{1 \text{ byte}}{8 \text{ bits}} = 4 \text{ byte/cycle}$$

1mb = 1 million byte
1 Hertz = 1 cycle / 1 second
1 mhz = 1 million hertz
200 MHz = 200,000,000
so
200,000,000 hertz

$$\text{So } \frac{200{,}000{,}000 \text{ cycles}}{1 \text{ second}} \cdot \frac{4 \text{ bytes}}{1 \text{ cycle}} = \frac{800{,}000{,}000 \text{ bytes}}{\text{Second}}$$

$$\text{we want MB/s } \frac{800{,}000{,}000 \text{ bytes}}{1 \text{ second}} \cdot \frac{1 \text{ mb}}{1 \text{ million bytes}} = \boxed{800 \text{ mb/second}}$$

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7.11 Consider a 64 bit data bus SDRAM. Given that the clock Frequency of the bus is 200 mhz, What is the peak memory bandwidth in megabytes per second MBS. Frequency

(width / Type of memory)

1mb = 1 mil bytes
1 hertz = 1 cycle/sec
mhz = 1 mil hertz

$\frac{64 \text{ bits}}{1 \text{ cycle}} \cdot \frac{1 \text{ byte}}{8 \text{ bits}} = 8 \text{ byte/cycle}$

$200 \text{ mhz} = 200 \cdot 1{,}000{,}000 = 200{,}000{,}000 \text{ hertz}$

$\frac{8 \text{ byte}}{1 \text{ cycle}} \cdot \frac{200{,}000{,}000 \text{ cycles}}{1 \text{ second}} = 1{,}600{,}000{,}000 \text{ bytes/sec}$

$\frac{1{,}600{,}000{,}000 \text{ bytes}}{1 \text{ second}} \cdot \frac{1 \text{ mb}}{1{,}000{,}000} = \boxed{1600 \text{ mb/s}}$

(width / type of mem)

7.12 Consider a 32 bit data bus DDR SDRAM. Given that the clock Frequency of the bus is 200 mhz. What is the peak memory bandwidth in megabyte per second (MBS) Frequency

$\frac{32 \text{ bits}}{1 \text{ cycle}} \cdot \frac{1 \text{ byte}}{8 \text{ bits}} = 4 \text{ byte/cycle}$

$200 \text{ mhz} = 200 \cdot 1{,}000{,}000 = 200{,}000{,}000 \text{ mhz}$

$\frac{4 \text{ byte}}{1 \text{ cycle}} \cdot \frac{200{,}000{,}000 \text{ cycles}}{1 \text{ Seccond}} = 800{,}000{,}000 \text{ bytes/second}$

$\frac{800{,}000{,}000 \text{ bytes}}{1 \text{ second}} \cdot \frac{1 \text{ mb}}{1{,}000{,}000 \text{ bytes}} = 800 \text{ mb/second}$

800 mb/second but DDR SDRAM is roughly twice as fast

$800 \cdot 2 = \boxed{1600 \text{ mb/second}}$