

# Lab2

Sorry for not finish the C model and RTL improvement.  
What I have done is finish the Open EDA flow

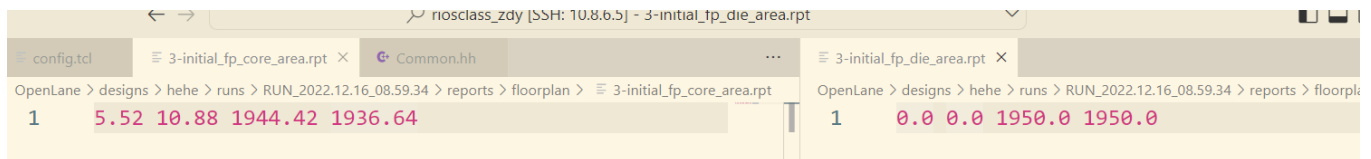
## Open EDA flow

The results are located on `OpenLane/designs/hehe/runs/RUN_2022.12.16_08.59.34`

And config.tcl of hehe is in

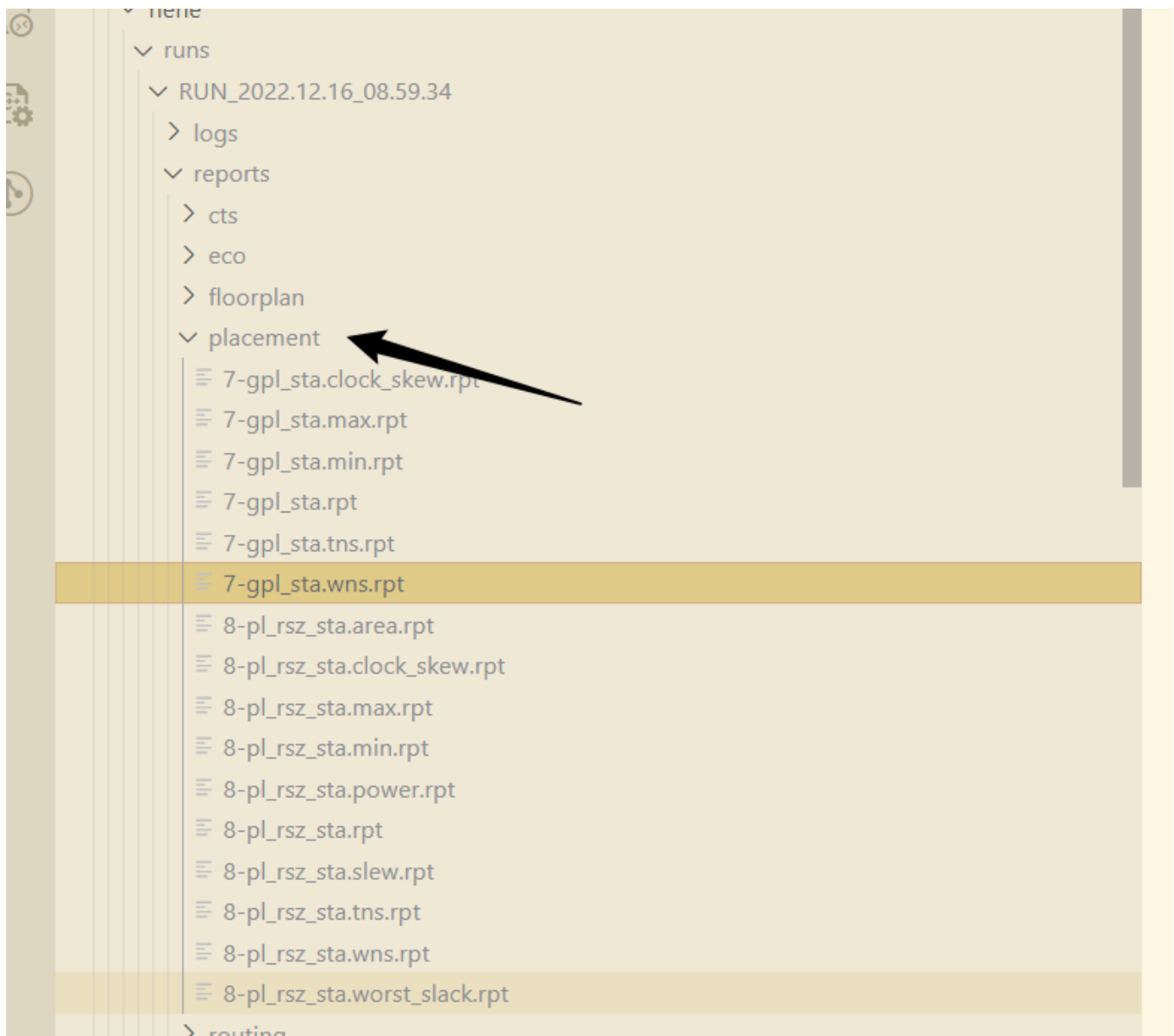
`OpenLane/designs/hehe/runs/RUN_2022.12.16_08.59.34/config.tcl`

## Floor Planning:



OpenLane > designs > hehe > runs > RUN_2022.12.16_08.59.34 > reports > floorplan > 3-initial_fp_core_area.rpt	OpenLane > designs > hehe > runs > RUN_2022.12.16_08.59.34 > reports > floorplan > 3-initial_fp_die_area.rpt
1 5.52 10.88 1944.42 1936.64	1 0.0 0.0 1950.0 1950.0

## Placement



**CTS**

```
11-cts_rsz_sta.worst_slack.rpt X
OpenLane > designs > hehe > runs > RUN_2022.12.16_08.59.34 > reports > cts > 11-cts_rsz_sta.worst_slack.rpt
9
8 =====
7 | report_worst_slack -max (Setup)
6 =====
5 worst slack 2.04
4
3 =====
2 | report_worst_slack -min (Hold)
1 =====
10 worst slack 0.10
1
```

# Routing

```
11-cts_rsz_sta.worst_slack.rpt 12-rt_rsz_sta.area.rpt X
OpenLane > designs > hehe > runs > RUN_2022.12.16_08.59.34 > reports > routing > 12-rt_rsz_sta.area.rpt
1
1 =====
2 | report_design_area
3 =====
4 Design area 663101 u^2 18% utilization.
5
```