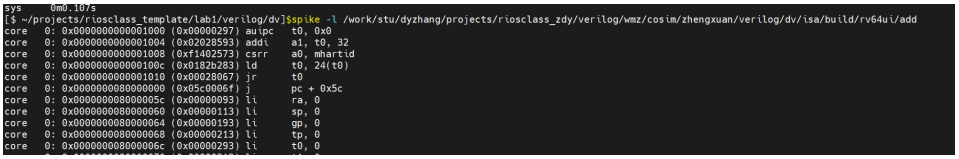
CPUDesign

1. Spike model and co-sim:
   a. spike model

```
[$ ~/projects/riosclass_zdy/co-sim]$ls
hello  hello.c  makefile  template.cc  template.v
[$ ~/projects/riosclass_zdy/co-sim]$spike $(which pk) hello
bbl loader
hello
```

   b. Core RTL pass ISA tests

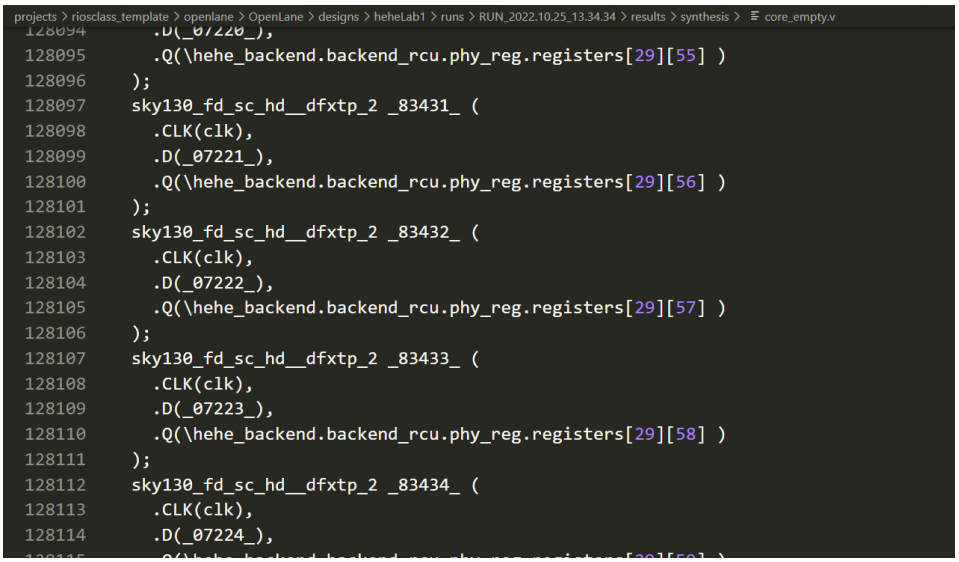
```
 00001f17 80000040
 fc3f2023 80000044
pass test
$finish called from file "./hehe_tb.sv", line 51.
$finish at simulation time             59930000
           V C S   S i m u l a t i o n   R e p o r t
Time: 59930000 ps
CPU Time:      0.600 seconds;       Data structure size:   0.1Mb
Wed Oct 26 17:01:29 2022

real    0m0.734s
user    0m0.524s
sys     0m0.107s
```

   c.
      - i.
      - 

2. Open EDA flow:
   a. GreenRio core logic synthesis by yosys:
      - install openEDA:
        - `git clone https://github.com/The-OpenROAD-Project/OpenLane.git`
        - `cd OpenLane`
        - `make`
        - `make pdk`
        - `make test`
      - Copy rtl of hehe to `OpenLane/designs/heheLab1/src
      - Add config.tcl in OpenLane/designs/heheLab1

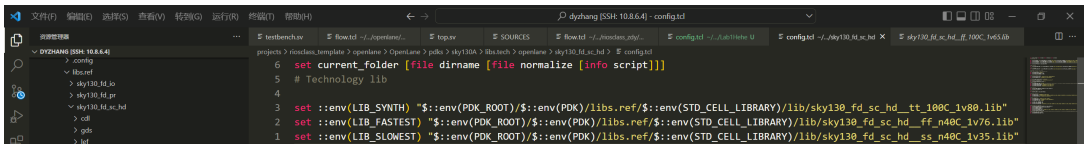
```
set ::env(PDK) "sky130A"
set script_dir $::env(DESIGN_DIR)
set ::env(DESIGN_NAME) core_empty
set ::env(VERILOG_FILES) "\
    $script_dir/src/params.vh \
    $script_dir/src/core_empty/lsu/*.v \
    $script_dir/src/core_empty/pipeline/*.v \
    $script_dir/src/core_empty/units/*.v \
    $script_dir/src/core_empty/*.v \
    $script_dir/src/*.v "
## Clock configurations
set ::env(CLOCK_PORT) "clk"
set ::env(CLOCK_PERIOD) "12.5"

```

- go to OpenLane and `make mount`
- run `./flow.tcl -design heheLab1
- Here comes the result:



b. logic sysnthesis by another lib:

`/work/stu/dyzhang/projects/riosclass_template/openlane/OpenLane/pdks/sky130A/libs.tech/openlane/sky130_fd_sc_hd/config.tcl`



And here is result