

# CPU Design

## 1. Spike model and co-sim:

### a. spike model

```
[~/projects/riosclass_zdy/co-sim]$ls
hello  hello.c  makefile  template.cc  template.v
[~/projects/riosclass_zdy/co-sim]$spike $(which pk) hello
bbl loader
hello
```

### b. Core RTL pass ISA tests

```
031f0263 8000001c
00001f17 80000040
fc3f2023 80000044
pass test
$finish called from file "./hehe_tb.sv", line 51.
$finish at simulation time 59930000
V C S  S i m u l a t i o n  R e p o r t
Time: 59930000 ps
CPU Time: 0.600 seconds; Data structure size: 0.1Mb
Wed Oct 26 17:01:29 2022

real    0m0.734s
user    0m0.524s
sys     0m0.107s
```

### c.

#### o i.

```
sys 0m0.107s
[~/projects/riosclass_template/lab1/verilog/dv]$spike -l /work/stu/dyhzhang/projects/riosclass_zdy/verilog/wmz/cosim/zhengxuan/verilog/dv/isa/build/rv64u1/add
core 0: 0x0000000000001000 (0x00000297) auipc t0, 0x0
core 0: 0x0000000000001004 (0x00000593) addi a1, t0, 32
core 0: 0x0000000000001008 (0xf1402573) csrr a0, mhartid
core 0: 0x000000000000100c (0x0182b283) ld t0, 24(t0)
core 0: 0x0000000000001010 (0x00020067) jr t0
core 0: 0x0000000000000000 (0x05c0006f) j pc + 0x5c
core 0: 0x000000000000005c (0x00000093) li ra, 0
core 0: 0x0000000000000060 (0x00000113) li sp, 0
core 0: 0x0000000000000064 (0x00000153) li gp, 0
core 0: 0x0000000000000068 (0x00000213) li tp, 0
core 0: 0x000000000000006c (0x00000293) li t0, 0
```

## 2. Open EDA flow:

### a. GreenRio core logic synthesis by yosys:

#### o install openEDA:

- `git clone https://github.com/The-OpenROAD-Project/OpenLane.git`
- `cd OpenLane`
- `make`
- `make pdk`
- `make test`

#### o Copy rtl of hehe to `OpenLane/designs/heheLab1/src

#### o Add config.tcl in OpenLane/designs/heheLab1

```

13 set ::env(PDK) "sky130A"
12 set script_dir $::env(DESIGN_DIR)
11 set ::env(DESIGN_NAME) core_empty
10 set ::env(VERILOG_FILES) "\
9   $script_dir/src/params.vh \
8   $script_dir/src/core_empty/lsu/*.v \
7   $script_dir/src/core_empty/pipeline/*.v \
6   $script_dir/src/core_empty/units/*.v \
5   $script_dir/src/core_empty/*.v \
4   $script_dir/src/*.v "
3 ## Clock configurations
2 set ::env(CLOCK_PORT) "clk"
1 set ::env(CLOCK_PERIOD) "12.5"
14

```

- go to OpenLane and **make mount**
- run `./flow.tcl -design heheLab1`
- Here comes the result:

```

projects > riosclass_template > openlane > OpenLane > designs > heheLab1 > runs > RUN_2022.10.25.13.34.34 > results > synthesis > core_empty.v
128095   .D(_07220_),
128096   );
128097   sky130_fd_sc_hd_dfxt2_83431_ (
128098   .CLK(clk),
128099   .D(_07221_),
128100   .Q(\hehe_backend.backend_rcu.phy_reg.registers[29][55] )
128101   );
128102   sky130_fd_sc_hd_dfxt2_83432_ (
128103   .CLK(clk),
128104   .D(_07222_),
128105   .Q(\hehe_backend.backend_rcu.phy_reg.registers[29][56] )
128106   );
128107   sky130_fd_sc_hd_dfxt2_83433_ (
128108   .CLK(clk),
128109   .D(_07223_),
128110   .Q(\hehe_backend.backend_rcu.phy_reg.registers[29][57] )
128111   );
128112   sky130_fd_sc_hd_dfxt2_83434_ (
128113   .CLK(clk),
128114   .D(_07224_),
128115   .Q(\hehe_backend.backend_rcu.phy_reg.registers[29][58] )

```

b. logic synthesis by another lib:

`/work/stu/dyzhang/projects/riosclass_template/openlane/OpenLane/pdks/sky130A/libs.tech/openlane/sky130_fd_sc_hd/config.tcl`

```

6 set current_folder [file dirname [file normalize [info script]]]
7 # Technology lib
8
9 set ::env(LIB_SYNTH) "$::env(PDK_ROOT)/$::env(PDK)/libs.ref/$::env(STD_CELL_LIBRARY)/lib/sky130_fd_sc_hd_tt_100C_1v80.lib"
10 set ::env(LIB_FASTEST) "$::env(PDK_ROOT)/$::env(PDK)/libs.ref/$::env(STD_CELL_LIBRARY)/lib/sky130_fd_sc_hd_ff_n40C_1v76.lib"
11 set ::env(LIB_SLOWEST) "$::env(PDK_ROOT)/$::env(PDK)/libs.ref/$::env(STD_CELL_LIBRARY)/lib/sky130_fd_sc_hd_ss_n40C_1v35.lib"

```

And here is result

```

projects > riosclass_template > openlane > OpenLane > designs > heheLab1 > runs > RUN_2022.10.25.14.34.37 > results > synthesis > core_empty.v
116582   .A(_17032_),
116583   .B(_17871_),
116584   .Y(_17876_)
116585   );
116586   sky130_fd_sc_hd_a221o_2_50367_ (
116587   .A1(_17869_),
116588   .A2(_17029_),
116589   .B1(_17870_),
116590   .B2(\hehe_backend.backend_rcu.phy_reg.registers[11][34] ),
116591   .C1(_17876_),
116592   .X(_02401_)
116593   );
116594   sky130_fd_sc_hd_nor2_2_50368_ (
116595   .A(_17044_),
116596   .B(_17871_),

```