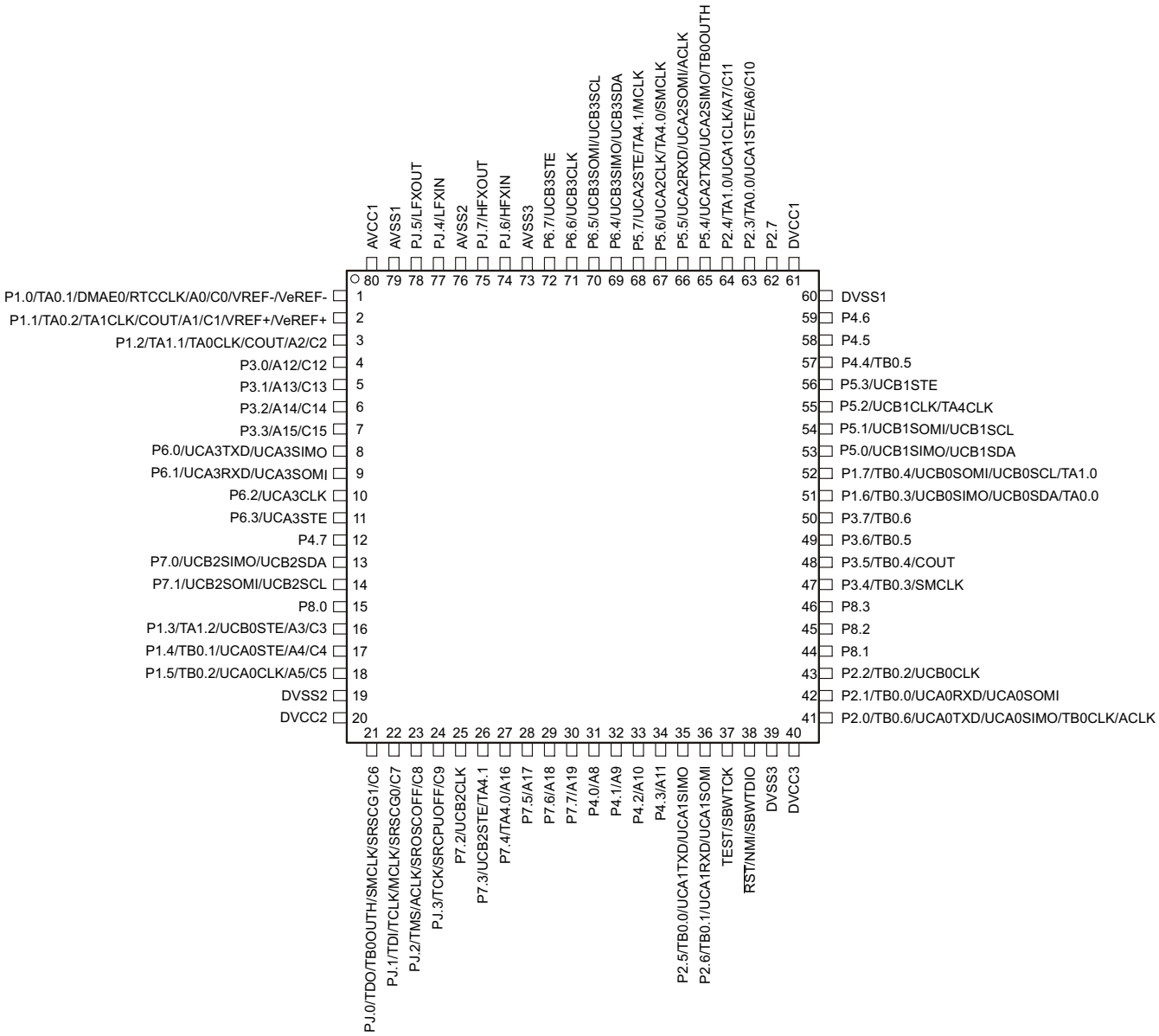
Figure 7-3 shows the pinout of the 80-pin PN package.



On devices with UART BSL: P2.0 is BSLTX, P2.1 is BSLRX
On devices with I²C BSL: P1.6 is BSLSDA, P1.7 is BSLSCL

Figure 7-3. 80-Pin PN Package (Top View)

7.2 Pin Attributes

Table 7-1 summarizes the attributes of the pins.

Table 7-1. Pin Attributes

PIN NUMBER (1)				SIGNAL NAME (2) (3)	SIGNAL TYPE (4)	BUFFER TYPE (5)	POWER SOURCE (6)	RESET STATE AFTER BOR (7)
PN	PM	RGZ	ZVW					
1	1	1	A10	P1.0	I/O	LVCMOS	DVCC	OFF
				TA0.1	I/O	LVCMOS	DVCC	–
				DMAE0	I	LVCMOS	DVCC	–
				RTCCLK	O	LVCMOS	DVCC	–
				A0	I	Analog	DVCC	–
				C0	I	Analog	DVCC	–
				VREF-	O	Analog	DVCC	–
				VeREF-	I	Analog	DVCC	–
2	2	2	A9	P1.1	I/O	LVCMOS	DVCC	OFF
				TA0.2	I/O	LVCMOS	DVCC	–
				TA1CLK	I	LVCMOS	DVCC	–
				COUT	O	LVCMOS	DVCC	–
				A1	I	Analog	DVCC	–
				C1	I	Analog	DVCC	–
				VREF+	O	Analog	DVCC	–
				VeREF+	I	Analog	DVCC	–
3	3	3	B9	P1.2	I/O	LVCMOS	DVCC	OFF
				TA1.1	I/O	LVCMOS	DVCC	–
				TA0CLK	I	LVCMOS	DVCC	–
				COUT	O	LVCMOS	DVCC	–
				A2	I	Analog	DVCC	–
				C2	I	Analog	DVCC	–
4	4	4	A8	P3.0	I/O	LVCMOS	DVCC	OFF
				A12	I	Analog	DVCC	–
				C12	I	Analog	DVCC	–
5	5	5	B8	P3.1	I/O	LVCMOS	DVCC	–
				A13	I	Analog	DVCC	–
				C13	I	Analog	DVCC	–
6	6	6	B7	P3.2	I/O	LVCMOS	DVCC	OFF
				A14	I	Analog	DVCC	–
				C14	I	Analog	DVCC	–
7	7	7	A7	P3.3	I/O	LVCMOS	DVCC	OFF
				A15	I	Analog	DVCC	–
				C15	I	Analog	DVCC	–
8	–	–	D8	P6.0	I/O	LVCMOS	DVCC	OFF
				UCA3TXD	O	LVCMOS	DVCC	–
				UCA3SIMO	I/O	LVCMOS	DVCC	–
9	–	–	D7	P6.1	I/O	LVCMOS	DVCC	OFF
				UCA3RXD	I	LVCMOS	DVCC	–
				UCA3SOMI	I/O	LVCMOS	DVCC	–

Table 7-1. Pin Attributes (continued)

PIN NUMBER (1)				SIGNAL NAME (2) (3)	SIGNAL TYPE (4)	BUFFER TYPE (5)	POWER SOURCE (6)	RESET STATE AFTER BOR (7)
PN	PM	RGZ	ZVW					
10	–	–	A6	P6.2	I/O	LVCMOS	DVCC	OFF
				UCA3CLK	I/O	LVCMOS	DVCC	–
11	–	–	B6	P6.3	I/O	LVCMOS	DVCC	OFF
				UCA3STE	I/O	LVCMOS	DVCC	–
12	8	8	D6	P4.7	I/O	LVCMOS	DVCC	OFF
13	9	–	A5	P7.0	I/O	LVCMOS	DVCC	OFF
				UCB2SIMO	I/O	LVCMOS	DVCC	–
				UCB2SDA	I/O	LVCMOS	DVCC	–
14	10	–	B5	P7.1	I/O	LVCMOS	DVCC	OFF
				UCB2SOMI	I/O	LVCMOS	DVCC	–
				UCB2SCL	I/O	LVCMOS	DVCC	–
15	11	–	D5	P8.0	I/O	LVCMOS	DVCC	OFF
16	12	9	A4	P1.3	I/O	LVCMOS	DVCC	OFF
				TA1.2	I/O	LVCMOS	DVCC	–
				UCB0STE	I/O	LVCMOS	DVCC	–
				A3	I	Analog	DVCC	–
				C3	I	Analog	DVCC	–
17	13	10	B3	P1.4	I/O	LVCMOS	DVCC	OFF
				TB0.1	I/O	LVCMOS	DVCC	–
				UCA0STE	I/O	LVCMOS	DVCC	–
				A4	I	Analog	DVCC	–
				C4	I	Analog	DVCC	–
18	14	11	B4	P1.5	I/O	LVCMOS	DVCC	OFF
				TB0.2	I/O	LVCMOS	DVCC	–
				UCA0CLK	I/O	LVCMOS	DVCC	–
				A5	I	Analog	DVCC	–
				C5	I	Analog	DVCC	–
19	15	–	A2	DVSS2	P	Power	–	N/A
20	16	–	A3	DVCC2	P	Power	–	N/A
21	17	12	B1	PJ.0	I/O	LVCMOS	DVCC	OFF
				TDO	O	LVCMOS	DVCC	–
				TB0OUTH	I	LVCMOS	DVCC	–
				SMCLK	O	LVCMOS	DVCC	–
				SRSCG1	O	LVCMOS	DVCC	–
				C6	I	Analog	DVCC	–
22	18	13	C1	PJ.1	I/O	LVCMOS	DVCC	OFF
				TDI	I	LVCMOS	DVCC	–
				TCLK	I	LVCMOS	DVCC	–
				MCLK	O	LVCMOS	DVCC	–
				SRSCG0	O	LVCMOS	DVCC	–
				C7	I	Analog	DVCC	–

Table 7-1. Pin Attributes (continued)

PIN NUMBER (1)				SIGNAL NAME (2) (3)	SIGNAL TYPE (4)	BUFFER TYPE (5)	POWER SOURCE (6)	RESET STATE AFTER BOR (7)
PN	PM	RGZ	ZVW					
23	19	14	C2	PJ.2	I/O	LVCMOS	DVCC	OFF
				TMS	I	LVCMOS	DVCC	–
				ACLK	O	LVCMOS	DVCC	–
				SROSCOFF	O	LVCMOS	DVCC	–
				C8	I	Analog	DVCC	–
24	20	15	D2	PJ.3	I/O	LVCMOS	DVCC	OFF
				TCK	I	LVCMOS	DVCC	–
				SRCPUOFF	O	LVCMOS	DVCC	–
				C9	I	Analog	DVCC	–
25	21	–	D1	P7.2	I/O	LVCMOS	DVCC	OFF
				UCB2CLK	I/O	LVCMOS	DVCC	–
26	22	–	D4	P7.3	I/O	LVCMOS	DVCC	OFF
				UCB2STE	I/O	LVCMOS	DVCC	–
				TA4.1	I/O	LVCMOS	DVCC	–
27	23	–	E1	P7.4	I/O	LVCMOS	DVCC	OFF
				TA4.0	I/O	LVCMOS	DVCC	–
				A16	I	Analog	DVCC	–
28	–	–	E2	P7.5	I/O	LVCMOS	DVCC	OFF
				A17	I	Analog	DVCC	–
29	–	–	E4	P7.6	I/O	LVCMOS	DVCC	OFF
				A18	I	Analog	DVCC	–
30	–	–	F2	P7.7	I/O	LVCMOS	DVCC	OFF
				A19	I	Analog	DVCC	–
31	24	16	F1	P4.0	I/O	LVCMOS	DVCC	OFF
				A8	I	Analog	DVCC	–
32	25	17	F4	P4.1	I/O	LVCMOS	DVCC	OFF
				A9	I	Analog	DVCC	–
33	26	18	G1	P4.2	I/O	LVCMOS	DVCC	OFF
				A10	I	Analog	DVCC	–
34	27	19	G2	P4.3	I/O	LVCMOS	DVCC	OFF
				A11	I	Analog	DVCC	–
35	28	20	G4	P2.5	I/O	LVCMOS	DVCC	OFF
				TB0.0	I/O	LVCMOS	DVCC	–
				UCA1TXD	O	LVCMOS	DVCC	–
				UCA1SIMO	I/O	LVCMOS	DVCC	–
36	29	21	H1	P2.6	I/O	LVCMOS	DVCC	OFF
				TB0.1	O	LVCMOS	DVCC	–
				UCA1RXD	I	LVCMOS	DVCC	–
				UCA1SOMI	I/O	LVCMOS	DVCC	–
37	30	22	H2	TEST	I	LVCMOS	DVCC	OFF
				SBWTCK	I	LVCMOS	DVCC	–
38	31	23	J2	$\overline{\text{RST}}$	I	LVCMOS	DVCC	OFF
				NMI	I	LVCMOS	DVCC	–
				SBWTDIO	I/O	LVCMOS	DVCC	–

Table 7-1. Pin Attributes (continued)

PIN NUMBER (1)				SIGNAL NAME (2) (3)	SIGNAL TYPE (4)	BUFFER TYPE (5)	POWER SOURCE (6)	RESET STATE AFTER BOR (7)
PN	PM	RGZ	ZVW					
39	–	–	J1	DVSS3	P	Power	–	N/A
40	–	–	K1	DVCC3	P	Power	–	N/A
41	32	24	L2	P2.0	I/O	LVCMOS	DVCC	OFF
				TB0.6	I/O	LVCMOS	DVCC	–
				UCA0TXD	O	LVCMOS	DVCC	–
				BSLTX	O	LVCMOS	DVCC	–
				UCA0SIMO	I/O	LVCMOS	DVCC	–
				TB0CLK	I	LVCMOS	DVCC	–
				ACLK	O	LVCMOS	DVCC	–
42	33	25	L3	P2.1	I/O	LVCMOS	DVCC	OFF
				TB0.0	I/O	LVCMOS	DVCC	–
				UCA0RXD	I	LVCMOS	DVCC	–
				BSLRX	I	LVCMOS	DVCC	–
				UCA0SOMI	I/O	LVCMOS	DVCC	–
43	34	26	K3	P2.2	I/O	LVCMOS	DVCC	OFF
				TB0.2	O	LVCMOS	DVCC	–
				UCB0CLK	I/O	LVCMOS	DVCC	–
44	–	–	L4	P8.1	I/O	LVCMOS	DVCC	OFF
45	–	–	K4	P8.2	I/O	LVCMOS	DVCC	OFF
46	–	–	H4	P8.3	I/O	LVCMOS	DVCC	OFF
47	35	27	K5	P3.4	I/O	LVCMOS	DVCC	OFF
				TB0.3	I/O	LVCMOS	DVCC	–
				SMCLK	O	LVCMOS	DVCC	–
48	36	28	L5	P3.5	I/O	LVCMOS	DVCC	OFF
				TB0.4	I/O	LVCMOS	DVCC	–
				COUT	O	LVCMOS	DVCC	–
49	37	29	H5	P3.6	I/O	LVCMOS	DVCC	OFF
				TB0.5	I/O	LVCMOS	DVCC	–
50	38	30	H6	P3.7	I/O	LVCMOS	DVCC	OFF
				TB0.6	I/O	LVCMOS	DVCC	–
51	39	31	L6	P1.6	I/O	LVCMOS	DVCC	OFF
				TB0.3	I/O	LVCMOS	DVCC	–
				UCB0SIMO	I/O	LVCMOS	DVCC	–
				UCB0SDA	I/O	LVCMOS	DVCC	–
				BSLSDA	I/O	LVCMOS	DVCC	–
				TA0.0	I/O	LVCMOS	DVCC	–
52	40	32	K6	P1.7	I/O	LVCMOS	DVCC	OFF
				TB0.4	I/O	LVCMOS	DVCC	–
				UCB0SOMI	I/O	LVCMOS	DVCC	–
				UCB0SCL	I/O	LVCMOS	DVCC	–
				BSLSCL	I/O	LVCMOS	DVCC	–
				TA1.0	I/O	LVCMOS	DVCC	–

Table 7-1. Pin Attributes (continued)

PIN NUMBER (1)				SIGNAL NAME (2) (3)	SIGNAL TYPE (4)	BUFFER TYPE (5)	POWER SOURCE (6)	RESET STATE AFTER BOR (7)
PN	PM	RGZ	ZVW					
53	41	–	L7	P5.0	I/O	LVCMOS	DVCC	OFF
				UCB1SIMO	I/O	LVCMOS	DVCC	–
				UCB1SDA	I/O	LVCMOS	DVCC	–
54	42	–	K7	P5.1	I/O	LVCMOS	DVCC	OFF
				UCB1SOMI	I/O	LVCMOS	DVCC	–
				UCB1SCL	I/O	LVCMOS	DVCC	–
55	43	–	K8	P5.2	I/O	LVCMOS	DVCC	OFF
				UCB1CLK	I/O	LVCMOS	DVCC	–
				TA4CLK	I	LVCMOS	DVCC	–
56	44	–	L8	P5.3	I/O	LVCMOS	DVCC	OFF
				UCB1STE	I/O	LVCMOS	DVCC	–
57	45	33	H7	P4.4	I/O	LVCMOS	DVCC	OFF
				TB0.5	I/O	LVCMOS	DVCC	–
58	46	34	H8	P4.5	I/O	LVCMOS	DVCC	OFF
59	47	35	K9	P4.6	I/O	LVCMOS	DVCC	OFF
60	48	36	L9	DVSS1	P	Power	–	N/A
61	49	37	L10	DVCC1	P	Power	–	N/A
62	50	38	F11	P2.7	I/O	LVCMOS	DVCC	OFF
63	51	39	J11	P2.3	I/O	LVCMOS	DVCC	OFF
				TA0.0	I/O	LVCMOS	DVCC	–
				UCA1STE	I/O	LVCMOS	DVCC	–
				A6	I	Analog	DVCC	–
				C10	I	Analog	DVCC	–
64	52	40	K11	P2.4	I/O	LVCMOS	DVCC	OFF
				TA1.0	I/O	LVCMOS	DVCC	–
				UCA1CLK	I/O	LVCMOS	DVCC	–
				A7	I	Analog	DVCC	–
				C11	I	Analog	DVCC	–
65	53	–	J10	P5.4	I/O	LVCMOS	DVCC	OFF
				UCA2TXD	O	LVCMOS	DVCC	–
				UCA2SIMO	I/O	LVCMOS	DVCC	–
				TB0OUTH	I	LVCMOS	DVCC	–
66	54	–	H10	P5.5	I/O	LVCMOS	DVCC	OFF
				UCA2RXD	I	LVCMOS	DVCC	–
				UCA2SOMI	I/O	LVCMOS	DVCC	–
				ACLK	O	LVCMOS	DVCC	–
67	55	–	G10	P5.6	I/O	LVCMOS	DVCC	OFF
				UCA2CLK	I/O	LVCMOS	DVCC	–
				TA4.0	I/O	LVCMOS	DVCC	–
				SMCLK	O	LVCMOS	DVCC	–
68	56	–	G8	P5.7	I/O	LVCMOS	DVCC	OFF
				UCA2STE	I/O	LVCMOS	DVCC	–
				TA4.1	I/O	LVCMOS	DVCC	–
				MCLK	O	LVCMOS	DVCC	–

Table 7-1. Pin Attributes (continued)

PIN NUMBER (1)				SIGNAL NAME (2) (3)	SIGNAL TYPE (4)	BUFFER TYPE (5)	POWER SOURCE (6)	RESET STATE AFTER BOR (7)
PN	PM	RGZ	ZVW					
69	–	–	F8	P6.4	I/O	LVCMOS	DVCC	OFF
				UCB3SIMO	I/O	LVCMOS	DVCC	–
				UCB3SDA	I/O	LVCMOS	DVCC	–
70	–	–	F10	P6.5	I/O	LVCMOS	DVCC	OFF
				UCB3SOMI	I/O	LVCMOS	DVCC	–
				UCB3SCL	I/O	LVCMOS	DVCC	–
71	–	–	E8	P6.6	I/O	LVCMOS	DVCC	OFF
				UCB3CLK	I/O	LVCMOS	DVCC	–
72	–	–	C10	P6.7	I/O	LVCMOS	DVCC	OFF
				UCB3STE	I/O	LVCMOS	DVCC	–
73	57	41	E10	AVSS3	P	Power	–	N/A
74	58	42	H11	PJ.6	I/O	LVCMOS	DVCC	–
				HFXIN	I	Analog	DVCC	–
75	59	43	G11	PJ.7	I/O	LVCMOS	DVCC	OFF
				HFXOUT	O	Analog	DVCC	–
76	60	44	D10	AVSS2	P	Power	–	N/A
77	61	45	E11	PJ.4	I/O	LVCMOS	DVCC	OFF
				LFXIN	I	Analog	DVCC	–
78	62	46	D11	PJ.5	I/O	LVCMOS	DVCC	OFF
				LFXOUT	O	Analog	DVCC	–
79	63	47	C11	AVSS1	P	Power	–	N/A
80	64	48	B11	AVCC1	P	Power	–	N/A
–	–	–	A1	DGND	P	Power	–	N/A
–	–	–	A11	AGND	P	Power	–	N/A
–	–	–	B10	AGND	P	Power	–	N/A
–	–	–	K2	DGND	P	Power	–	N/A
–	–	–	K10	DGND	P	Power	–	N/A
–	–	–	L1	DGND	P	Power	–	N/A
–	–	–	L11	DGND	P	Power	–	N/A
–	–	Pad	–	QFN Pad	P	Power	–	N/A

(1) N/A = not available
(2) The signal that is listed first for each pin is the reset default pin name.
(3) Signal Types: I = Input, O = Output, I/O = Input or Output.
(4) Buffer Types: LVCMOS, Analog, or Power (see Table 7-3 for details)
(5) To determine the pin mux encodings for each pin, see Section 9.13.
(6) The power source shown in this table is the I/O power source, which may differ from the module power source.
(7) Reset States:
OFF = High impedance with Schmitt-trigger input and pullup or pulldown (if available) disabled
N/A = Not applicable

7.3 Signal Descriptions

Section 7.3 describes the signals for all device variants and package options.

Table 7-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO.(1)				PIN TYPE(2)	DESCRIPTION
		ZVW	PN	PM	RGZ		
ADC	A0	A10	1	1	1	I	ADC analog input A0
	A1	A9	2	2	2	I	ADC analog input A1
	A2	B9	3	3	3	I	ADC analog input A2
	A3	A4	16	12	9	I	ADC analog input A3
	A4	B3	17	13	10	I	ADC analog input A4
	A5	B4	18	14	11	I	ADC analog input A5
	A6	J11	63	51	39	I	ADC analog input A6
	A7	K11	64	52	40	I	ADC analog input A7
	A8	F1	31	24	16	I	ADC analog input A8
	A9	F4	32	25	17	I	ADC analog input A9
	A10	G1	33	26	18	I	ADC analog input A10
	A11	G2	34	27	19	I	ADC analog input A11
	A12	A8	4	4	4	I	ADC analog input A12
	A13	B8	5	5	5	I	ADC analog input A13
	A14	B7	6	6	6	I	ADC analog input A14
	A15	A7	7	7	7	I	ADC analog input A15
	A16	E1	27	23	–	I	ADC analog input A16
	A17	E2	28	–	–	I	ADC analog input A17
	A18	E4	29	–	–	I	ADC analog input A18
	A19	F2	30	–	–	I	ADC analog input A19
	VREF+	A9	2	2	2	O	Output of positive reference voltage
	VREF-	A10	1	1	1	O	Output of negative reference voltage
	VeREF+	A9	2	2	2	I	Input for an external positive reference voltage to the ADC
	VeREF-	A10	1	1	1	I	Input for an external negative reference voltage to the ADC
BSL (I^2C)	BSLSCL	K6	52	40	32	I/O	I^2C BSL clock
	BSLSDA	L6	51	39	31	I/O	I^2C BSL data
BSL (UART)	BSLRX	L3	42	33	25	I	UART BSL receive
	BSLTX	L2	41	32	24	O	UART BSL transmit
Clock	ACLK	C2 H10	23 41 66	19 32 54	14 24	O	ACLK output
	HFXIN	H11	74	58	42	I	Input for high-frequency crystal oscillator HFXT
	HFXOUT	G11	75	59	43	O	Output for high-frequency crystal oscillator HFXT
	LFXIN	E11	77	61	45	I	Input for low-frequency crystal oscillator LFXT
	LFXOUT	D11	78	62	46	O	Output of low-frequency crystal oscillator LFXT
	MCLK	C1 G8	22 68	18 56	13	O	MCLK output
	SMCLK	B1 G10	21 47 67	17 35 55	12 27	O	SMCLK output

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.(1)				PIN TYPE(2)	DESCRIPTION
		ZVW	PN	PM	RGZ		
Comparator	C0	A10	1	1	1	I	Comparator input C0
	C1	A9	2	2	2	I	Comparator input C1
	C2	B9	3	3	3	I	Comparator input C2
	C3	A4	16	12	9	I	Comparator input C3
	C4	B3	17	13	10	I	Comparator input C4
	C5	B4	18	14	11	I	Comparator input C5
	C6	B1	21	17	12	I	Comparator input C6
	C7	C1	22	18	13	I	Comparator input C7
	C8	C2	23	19	14	I	Comparator input C8
	C9	D2	24	20	15	I	Comparator input C9
	C10	J11	63	51	39	I	Comparator input C10
	C11	K11	64	52	40	I	Comparator input C11
	C12	A8	4	4	4	I	Comparator input C12
	C13	B8	5	5	5	I	Comparator input C13
	C14	B7	6	6	6	I	Comparator input C14
	C15	A7	7	7	7	I	Comparator input C15
	COUT	A9 B9 L5	2 3 48	2 3 36	2 3 28	O	Comparator output
DMA	DMAE0	A10	1	1	1	I	External DMA trigger
Debug	SBWTCK	H2	37	30	22	I	Spy-Bi-Wire input clock
	SBWTDIO	J2	38	31	23	I/O	Spy-Bi-Wire data input/output
	SRCPUOFF	D2	24	20	15	O	Low-power debug: CPU Status register bit CPUOFF
	SROSCOFF	C2	23	19	14	O	Low-power debug: CPU Status register bit OSCOFF
	SRSCG0	C1	22	18	13	O	Low-power debug: CPU Status register bit SCG0
	SRSCG1	B1	21	17	12	O	Low-power debug: CPU Status register bit SCG1
	TCK	D2	24	20	15	I	Test clock
	TCLK	C1	22	18	13	I	Test clock input
	TDI	C1	22	18	13	I	Test data input
	TDO	B1	21	17	12	O	Test data output port
	TEST	H2	37	30	22	I	Test mode pin – select digital I/O on JTAG pins
	TMS	C2	23	19	14	I	Test mode select

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.(1)				PIN TYPE(2)	DESCRIPTION
		ZVW	PN	PM	RGZ		
GPIO	P1.0	A10	1	1	1	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P1.1	A9	2	2	2	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P1.2	B9	3	3	3	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P1.3	A4	16	12	9	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P1.4	B3	17	13	10	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P1.5	B4	18	14	11	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P1.6	L6	51	39	31	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P1.7	K6	52	40	32	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
GPIO	P2.0	L2	41	32	24	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P2.1	L3	42	33	25	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P2.2	K3	43	34	26	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P2.3	J11	63	51	39	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P2.4	K11	64	52	40	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P2.5	G4	35	28	20	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P2.6	H1	36	29	21	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P2.7	F11	62	50	38	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
GPIO	P3.0	A8	4	4	4	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P3.1	B8	5	5	5	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P3.2	B7	6	6	6	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P3.3	A7	7	7	7	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P3.4	K5	47	35	27	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P3.5	L5	48	36	28	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P3.6	H5	49	37	29	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P3.7	H6	50	38	30	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.(1)				PIN TYPE(2)	DESCRIPTION
		ZVW	PN	PM	RGZ		
GPIO	P4.0	F1	31	24	16	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P4.1	F4	32	25	17	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P4.2	G1	33	26	18	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P4.3	G2	34	27	19	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P4.4	H7	57	45	33	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P4.5	H8	58	46	34	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P4.6	K9	59	47	35	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P4.7	D6	12	8	8	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
GPIO	P5.0	L7	53	41	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P5.1	K7	54	42	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P5.2	K8	55	43	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P5.3	L8	56	44	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P5.4	J10	65	53	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P5.5	H10	66	54	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P5.6	G10	67	55	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P5.7	G8	68	56	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
GPIO	P6.0	D8	8	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P6.1	D7	9	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P6.2	A6	10	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P6.3	B6	11	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P6.4	F8	69	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P6.5	F10	70	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P6.6	E8	71	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P6.7	C10	72	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.(1)				PIN TYPE(2)	DESCRIPTION
		ZVW	PN	PM	RGZ		
GPIO	P7.0	A5	13	9	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P7.1	B5	14	10	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P7.2	D1	25	21	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P7.3	D4	26	22	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P7.4	E1	27	23	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P7.5	E2	28	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P7.6	E4	29	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P7.7	F2	30	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
GPIO	P8.0	D5	15	11	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P8.1	L4	44	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P8.2	K4	45	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
	P8.3	H4	46	–	–	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5
GPIO	PJ.0	B1	21	17	12	I/O	General-purpose digital I/O
	PJ.1	C1	22	18	13	I/O	General-purpose digital I/O
	PJ.2	C2	23	19	14	I/O	General-purpose digital I/O
	PJ.3	D2	24	20	15	I/O	General-purpose digital I/O
	PJ.4	E11	77	61	45	I/O	General-purpose digital I/O
	PJ.5	D11	78	62	46	I/O	General-purpose digital I/O
	PJ.6	H11	74	58	42	I/O	General-purpose digital I/O
	PJ.7	G11	75	59	43	I/O	General-purpose digital I/O
I^2C	UCB0SCL	K6	52	40	32	I/O	I^2C clock – eUSCI_B0 I^2C mode
	UCB0SDA	L6	51	39	31	I/O	I^2C data – eUSCI_B0 I^2C mode
	UCB1SCL	K7	54	42	–	I/O	I^2C clock – eUSCI_B1 I^2C mode
	UCB1SDA	L7	53	41	–	I/O	I^2C data – eUSCI_B1 I^2C mode
	UCB2SCL	B5	14	10	–	I/O	I^2C clock – eUSCI_B2 I^2C mode
	UCB2SDA	A5	13	9	–	I/O	I^2C data – eUSCI_B2 I^2C mode
	UCB3SCL	F10	70	–	–	I/O	I^2C clock – eUSCI_B3 I^2C mode
	UCB3SDA	F8	69	–	–	I/O	I^2C data – eUSCI_B3 I^2C mode

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.[1]				PIN TYPE[2]	DESCRIPTION
		ZVW	PN	PM	RGZ		
Power	AGND	B10 A11	–	–	–	P	Analog ground
	AVCC1	B11	80	64	48	P	Analog power supply
	AVSS1	C11	79	63	47	P	Analog ground supply
	AVSS2	D10	76	60	44	P	Analog ground supply
	AVSS3	E10	73	57	41	P	Analog ground supply
	DGND	A1 K2 K10 L1 L11	–	–	–	P	Digital ground
	DVCC1	L10	61	49	37	P	Digital power supply
	DVCC2	A3	20	16	–	P	Digital power supply
	DVCC3	K1	40	–	–	P	Digital power supply
	DVSS1	L9	60	48	36	P	Digital ground supply
	DVSS2	A2	19	15	–	P	Digital ground supply
	DVSS3	J1	39	–	–	P	Digital ground supply
	QFN Pad	–	–	–	Pad	P	QFN package exposed thermal pad. TI recommends connection to V_{SS}.
RTC	RTCCLK	A10	1	1	1	O	RTC clock calibration output (not available on MSP430FR5x5x devices)

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.[1]				PIN TYPE[2]	DESCRIPTION
		ZVW	PN	PM	RGZ		
SPI	UCA0CLK	B4	18	14	11	I/O	Clock signal input – eUSCI_A0 SPI slave mode Clock signal output – eUSCI_A0 SPI master mode
	UCA0SIMO	L2	41	32	24	I/O	Slave in/master out – eUSCI_A0 SPI mode
	UCA0SOMI	L3	42	33	25	I/O	Slave out/master in – eUSCI_A0 SPI mode
	UCA0STE	B3	17	13	10	I/O	Slave transmit enable – eUSCI_A0 SPI mode
	UCA1CLK	K11	64	52	40	I/O	Clock signal input – eUSCI_A1 SPI slave mode Clock signal output – eUSCI_A1 SPI master mode
	UCA1SIMO	G4	35	28	20	I/O	Slave in/master out – eUSCI_A1 SPI mode
	UCA1SOMI	H1	36	29	21	I/O	Slave out/master in – eUSCI_A1 SPI mode
	UCA1STE	J11	63	51	39	I/O	Slave transmit enable – eUSCI_A1 SPI mode
	UCA2CLK	G10	67	55	–	I/O	Clock signal input – eUSCI_A2 SPI slave mode Clock signal output – eUSCI_A2 SPI master mode
	UCA2SIMO	J10	65	53	–	I/O	Slave in/master out – eUSCI_A2 SPI mode
	UCA2SOMI	H10	66	54	–	I/O	Slave out/master in – eUSCI_A2 SPI mode
	UCA2STE	G8	68	56	–	I/O	Slave transmit enable – eUSCI_A2 SPI mode
	UCA3CLK	A6	10	–	–	I/O	Clock signal input – eUSCI_A3 SPI slave mode Clock signal output – eUSCI_A3 SPI master mode
	UCA3SIMO	D8	8	–	–	I/O	Slave in/master out – eUSCI_A3 SPI mode
	UCA3SOMI	D7	9	–	–	I/O	Slave out/master in – eUSCI_A3 SPI mode
	UCA3STE	B6	11	–	–	I/O	Slave transmit enable – eUSCI_A3 SPI mode
	UCB0CLK	K3	43	34	26	I/O	Clock signal input – eUSCI_B0 SPI slave mode Clock signal output – eUSCI_B0 SPI master mode
	UCB0SIMO	L6	51	39	31	I/O	Slave in/master out – eUSCI_B0 SPI mode
	UCB0SOMI	K6	52	40	32	I/O	Slave out/master in – eUSCI_B0 SPI mode
	UCB0STE	A4	16	12	9	I/O	Slave transmit enable – eUSCI_B0 SPI mode
	UCB1CLK	K8	55	43	–	I/O	Clock signal input – eUSCI_B1 SPI slave mode Clock signal output – eUSCI_B1 SPI master mode
	UCB1SIMO	L7	53	41	–	I/O	Slave in/master out – eUSCI_B1 SPI mode
	UCB1SOMI	K7	54	42	–	I/O	Slave out/master in – eUSCI_B1 SPI mode
	UCB1STE	L8	56	44	–	I/O	Slave transmit enable – eUSCI_B1 SPI mode
	UCB2CLK	D1	25	21	–	I/O	Clock signal input – eUSCI_B2 SPI slave mode Clock signal output – eUSCI_B2 SPI master mode
	UCB2SIMO	A5	13	9	–	I/O	Slave in/master out – eUSCI_B2 SPI mode
	UCB2SOMI	B5	14	10	–	I/O	Slave out/master in – eUSCI_B2 SPI mode
	UCB2STE	D4	26	22	–	I/O	Slave transmit enable – eUSCI_B2 SPI mode
	UCB3CLK	E8	71	–	–	I/O	Clock signal input – eUSCI_B3 SPI slave mode Clock signal output – eUSCI_B3 SPI master mode
	UCB3SIMO	F8	69	–	–	I/O	Slave in/master out – eUSCI_B3 SPI mode
	UCB3SOMI	F10	70	–	–	I/O	Slave out/master in – eUSCI_B3 SPI mode
	UCB3STE	C10	72	–	–	I/O	Slave transmit enable – eUSCI_B3 SPI mode
System	NMI	J2	38	31	23	I	Nonmaskable interrupt input
	$\overline{\text{RST}}$	J2	38	31	23	I	Reset input active low

Table 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.(1)				PIN TYPE(2)	DESCRIPTION
		ZVW	PN	PM	RGZ		
Timer	TA0.0	L6	51	39	31	I/O	TA0 CCR0 capture: CCI0A input, compare: Out0
	TA0.0	J11	63	51	39	I/O	TA0 CCR0 capture: CCI0B input, compare: Out0
	TA0.1	A10	1	1	1	I/O	TA0 CCR1 capture: CCI1A input, compare: Out1
	TA0.2	A9	2	2	2	I/O	TA0 CCR2 capture: CCI2A input, compare: Out2
	TA0CLK	B9	3	3	3	I	TA0 input clock
	TA1.0	K6	52	40	32	I/O	TA1 CCR0 capture: CCI0A input, compare: Out0
	TA1.0	K11	64	52	40	I/O	TA1 CCR0 capture: CCI0B input, compare: Out0
	TA1.1	B9	3	3	3	I/O	TA1 CCR1 capture: CCI1A input, compare: Out1
	TA1.2	A4	16	12	9	I/O	TA1 CCR2 capture: CCI2A input, compare: Out2
	TA1CLK	A9	2	2	2	I	TA1 input clock
	TA4.0	E1	27	23	–	I/O	TA4 CCR0 capture: CCI0B input, compare: Out0
	TA4.0	G10	67	55	–	I/O	TA4 CCR0 capture: CCI0A input, compare: Out0
	TA4.1	D4	26	22	–	I/O	TA4CCR1 capture: CCI1B input, compare: Out1
	TA4.1	G8	68	56	–	I/O	TA4 CCR1 capture: CCI1A input, compare: Out1
	TA4CLK	K8	55	43	–	I	TA4 input clock
	TB0.0	G4	35	28	20	I/O	TB0 CCR0 capture: CCI0B input, compare: Out0
	TB0.0	L3	42	33	25	I/O	TB0 CCR0 capture: CCI0A input, compare: Out0
	TB0.1	B3	17	13	10	I/O	TB0 CCR1 capture: CCI1A input, compare: Out1
	TB0.1	H1	36	29	21	O	TB0 CCR1 compare: Out1
	TB0.2	B4	18	14	11	I/O	TB0 CCR2 capture: CCI2A input, compare: Out2
	TB0.2	K3	43	34	26	O	TB0 CCR2 compare: Out2
	TB0.3	K5	47	35	27	I/O	TB0 CCR3 capture: CCI3A input, compare: Out3
	TB0.3	L6	51	39	31	I/O	TB0 CCR3 capture: CCI3B input, compare: Out3
	TB0.4	L5	48	36	28	I/O	TB0 CCR4 capture: CCI4A input, compare: Out4
	TB0.4	K6	52	40	32	I/O	TB0 CCR4 capture: CCI4B input, compare: Out4
	TB0.5	H5	49	37	29	I/O	TB0 CCR5 capture: CCI5A input, compare: Out5
	TB0.5	H7	57	45	33	I/O	TB0CCR5 capture: CCI5B input, compare: Out5
	TB0.6	L2	41	32	24	I/O	TB0 CCR6 capture: CCI6B input, compare: Out6
	TB0.6	H6	50	38	30	I/O	TB0 CCR6 capture: CCI6A input, compare: Out6
	TB0CLK	L2	41	32	24	I	TB0 clock input
	TB0OUTH	B1 J10	21 65	17 53	12	I	Switch all PWM outputs high impedance input – TB0
UART	UCA0RXD	L3	42	33	25	I	Receive data – eUSCI_A0 UART mode
	UCA0TXD	L2	41	32	24	O	Transmit data – eUSCI_A0 UART mode
	UCA1RXD	H1	36	29	21	I	Receive data – eUSCI_A1 UART mode
	UCA1TXD	G4	35	28	20	O	Transmit data – eUSCI_A1 UART mode
	UCA2RXD	H10	66	54	–	I	Receive data – eUSCI_A2 UART mode
	UCA2TXD	J10	65	53	–	O	Transmit data – eUSCI_A2 UART mode
	UCA3RXD	D7	9	–	–	I	Receive data – eUSCI_A3 UART mode
	UCA3TXD	D8	8	–	–	O	Transmit data – eUSCI_A3 UART mode

(1) N/A = not available
(2) I = input, O = output, P = power