American International University- Bangladesh (AIUB)
Faculty of Engineering (EEE)

Course Name :	Digital Logic Design	**Course Code :**	EEE 2206
Semester :	Summer 18-19	**Sec :**	C
Lab Instructor :	MD. Sajid Hossain		

Experiment No :	07
Experiment Name :	**Design of Multiplexer (MUX) and Demultiplexer (DEMUX).**

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Performance Date :	**23-7-2019**	**Due Date :**	**7-8-2019**

Marking Rubrics (to be filled by Lab Instructor)

Category	Proficient [4]	Good [3]	Acceptable [2]	Unacceptable [1]	Secured Marks
Theoretical Background, Methods & procedures sections	All information, measures and variables are provided and explained.	All Information provided that is sufficient, but more explanation is needed.	Most information correct, but some information may be missing or inaccurate.	Much information missing and/or inaccurate.	
Results	All of the criteria are met; results are described clearly and accurately;	Most criteria are met, but there may be some lack of clarity and/or incorrect information.	Experimental results don't match exactly with the theoretical values and/or analysis is unclear.	Experimental results are missing or incorrect;	
Discussion	Demonstrates thorough and sophisticated understanding. Conclusions drawn are appropriate for analyses;	Hypotheses are clearly stated, but some concluding statements not supported by data or data not well integrated.	Some hypotheses missing or misstated; conclusions not supported by data.	Conclusions don't match hypotheses, not supported by data; no integration of data from different sources.	
General formatting	Title page, placement of figures and figure captions, and other formatting issues all correct.	Minor errors in formatting.	Major errors and/or missing information.	Not proper style in text.	
Writing & organization	Writing is strong and easy to understand; ideas are fully elaborated and connected; effective transitions between sentences; no typographic, spelling, or grammatical errors.	Writing is clear and easy to understand; ideas are connected; effective transitions between sentences; minor typographic, spelling, or grammatical errors.	Most of the required criteria are met, but some lack of clarity, typographic, spelling, or grammatical errors are present.	Very unclear, many errors.	
Comments:				Total Marks (Out of **20**):	

Title: Design of Multiplexer (MUX) and Demultiplexer (DEMUX).

Introduction:

We had been learnt how to design and implement multiplexers (MUX) and demultiplexers (DEMUX) of different sizes using basic logic gates from this experiment. By using smaller multiplexers we had also learnt how to construct bigger multiplexer.

Theory and Methodology:

A multiplexer (or mux) is a device that selects one of several inputs and forwards the selected input into a single line. A multiplexer of 2^n inputs has n selection lines, which are used to select which input has to be sent to the output. A multiplexer is also called a data selector.

A demultiplexer (or demux) is a device taking a single input and selecting one of many data-output-lines, which is connected to the single input.

Multiplexer:

In computer system, it is often necessary to choose data from exactly one of a number of possible sources. Suppose that there are four sources of data, provided as input signals D_0 ,D_1, D_2 and D_3. The values of these signals change in time, perhaps at regular intervals. We want to design a circuit that produces an output that has the same value as either D_0 or D_1 or D_2 or D_3, dependent on the values of two selection pins S_1 and S_0. Here, the number of selection pin is two. Four combinations are possible using these two selection pins S_1 and S_0, such as (S_1, S_0) = (0,0), (0,1), (1,0), (1,1). Each combination is dedicated for each input. Let us consider the output variable is f. Now if $S_1 = 0$ and $S_0 = 0$ then $f = D_0$, if $S_1 = 0$ and $S_0 = 1$ then $f = D_1$, if $S_1 = 1$ and $S_0 = 0$ then $f = D_2$ and if $S_1 = 1$ and $S_0 = 1$ then $f = D_3$.

It is important to know that there is a relationship between the number of input and the number of selection pins. If the number of selection pin of a MUX is n, then maximum 2^n inputs are possible for that MUX. And the MUX will be called as 2^nto1 line MUX. The MUX we are going to design is a 4to1 MUX. There could be also 2to1 MUX, 8to1 MUX, 16to1 MUX etc.

For our design, there are 4 inputs and 2 selection pins. So actually we have 6 inputs. Now if we draw the truth table for 6 different inputs, there will be 64 input combinations. But fortunately we can do it in a more convenient way as given below.

Table:1

S_1	S_0	f
0	0	D_0
0	1	D_1
1	0	D_2

1	1	D_3

From the above truth table, we can write the function as given below.

$$= {}_{100} \quad +{}_{101} \quad +{}_{102} \quad + 1\,0\,3 \ldots (1)$$

The logic circuit of the equation (1) is given in figure 1.

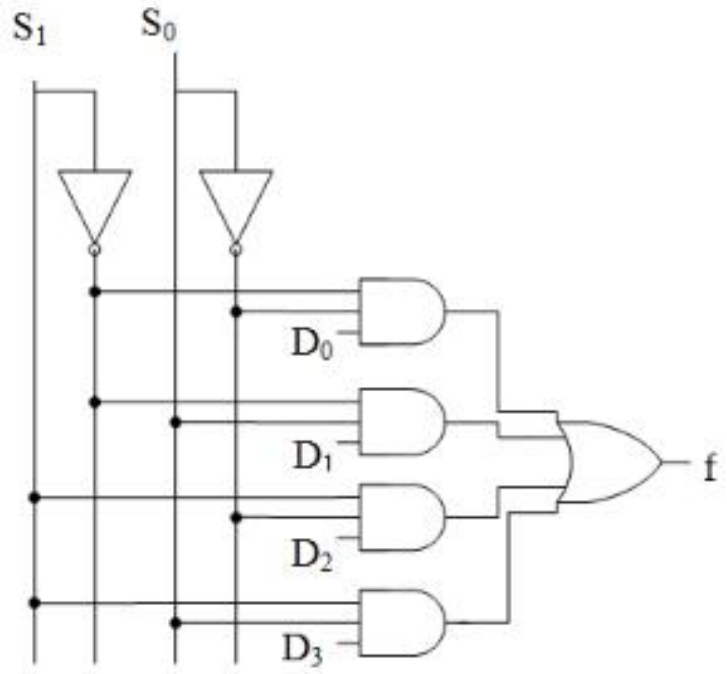


Figure1: 4to1 Multiplexer

Demultiplexer:

A Demultiplexer or Demux is opposite to the multiplexer. It has only one input and several outputs and one or more selection pins. Depending on the combination of selection input, the data input will be routed to one of many outputs. Other inputs will be low. Depending on the number of output, demultiplexers are termed as 1to2, 1to4 and 1to8 demultiplexers etc. If the number of selection pin is n, then maximum 2^n outputs can be accommodated.

We are going to design a 1to4 line demux having an input D_{in}, two selection pins S_1 and S_0 and four outputs D_0 ,D_1, D_2 and D_3. Now if $S_1 = 0$ and $S_0 = 0$ then $D_0 = D_{in}$, if $S_1 = 0$ and $S_0 = 1$ then $D_1 = D_{in}$, if $S_1 = 1$ and $S_0 = 0$ then $D_2 = D_{in}$ and if $S_1 = 1$ and $S_0 = 1$ then $D_3 = D_{in}$. We can draw the truth table as given below.

Table:2

S_1	S_0	D_0	D_1	D_2	D_3
0	0	D_{in}	0	0	0
0	1	0	D_{in}	0	0

1	0	0	0	D_{in}	0
1	1	0	0	0	D_{in}

From the above truth table we can write the functions for D_0 ,D_1, D_2 and D_3 as given below.

… (2)

… (5)

The circuit for 1to4 line demux is given below.

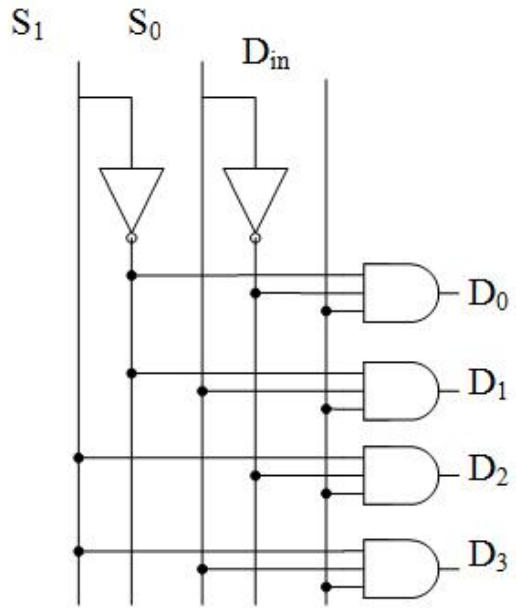


Figure 2: 1 to 4 Demultiplexer

It is also possible to construct 4to1 multiplexer (and 1to4 demultiplexer) using 2to1 multiplexers (1to2 demultiplexers) only. Figure 3 and figure 4 show the construction of 4to1 multiplexer using 2to1 multiplexers and 1to4 demultiplexer using 1to2 demultiplexers only.

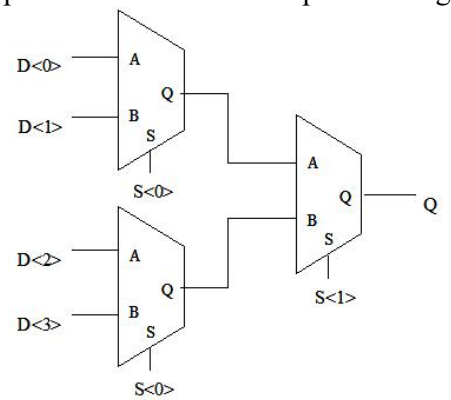


Figure 3: 4to1 multiplexer using 2to1 multiplexers.

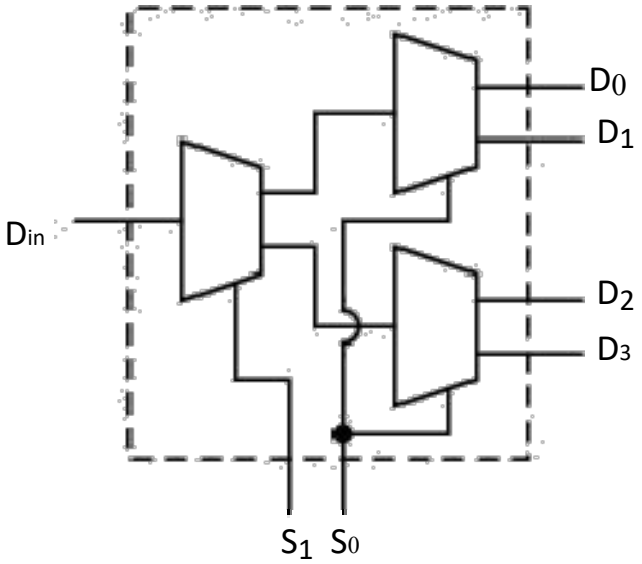


Figure 4: 1to4 demultiplexer using 1to2 dmultiplexers.

Apparatus:

1. NOT Gate - IC 7404
2. AND Gate - IC 7408
3. OR Gate - IC 7408

Experimental Procedure:

1. Connected the circuit according to the figures.

2. Used the toggle switches on the trainer board for providing input signal to the circuits. Connected the outputs to the LEDs on the trainer board.

3. Applied the input signals and observe and note the corresponding output signals.

Simulation & Measurement:

Data table:

S1	S2	f
0	0	D0
0	1	D1
1	0	D2
1	1	D3

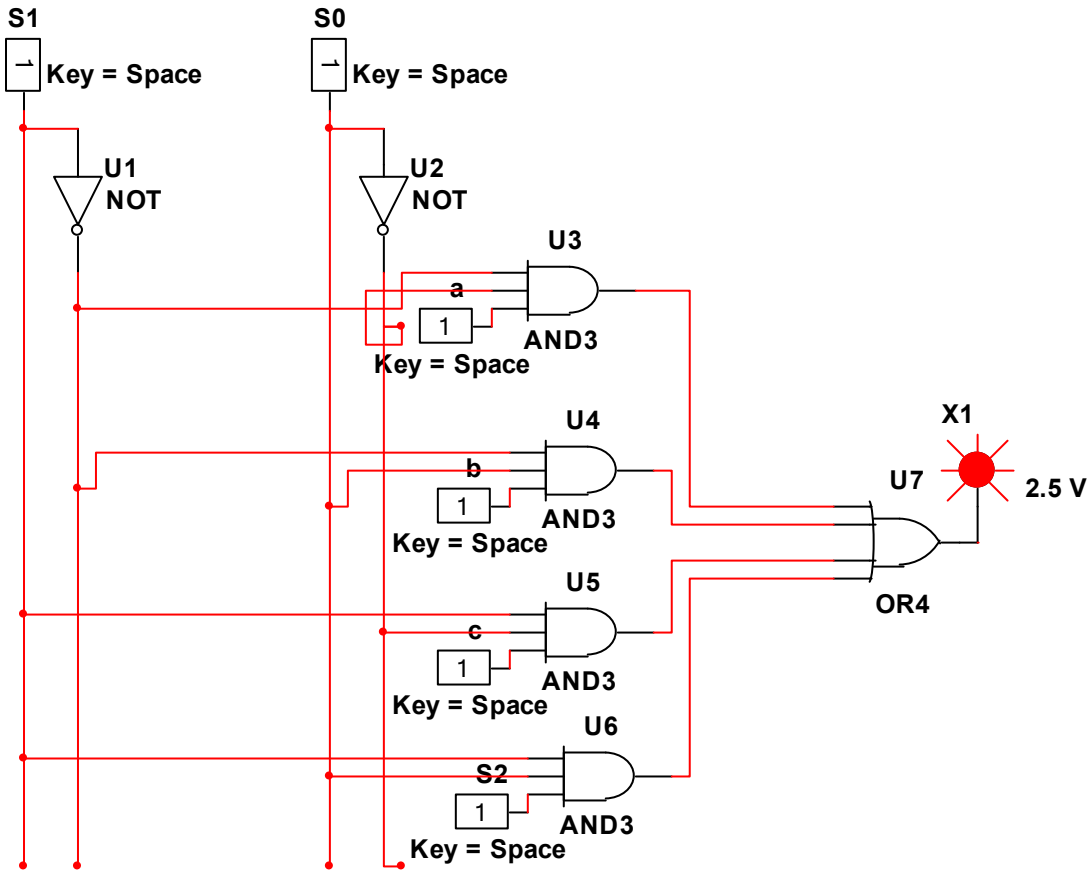
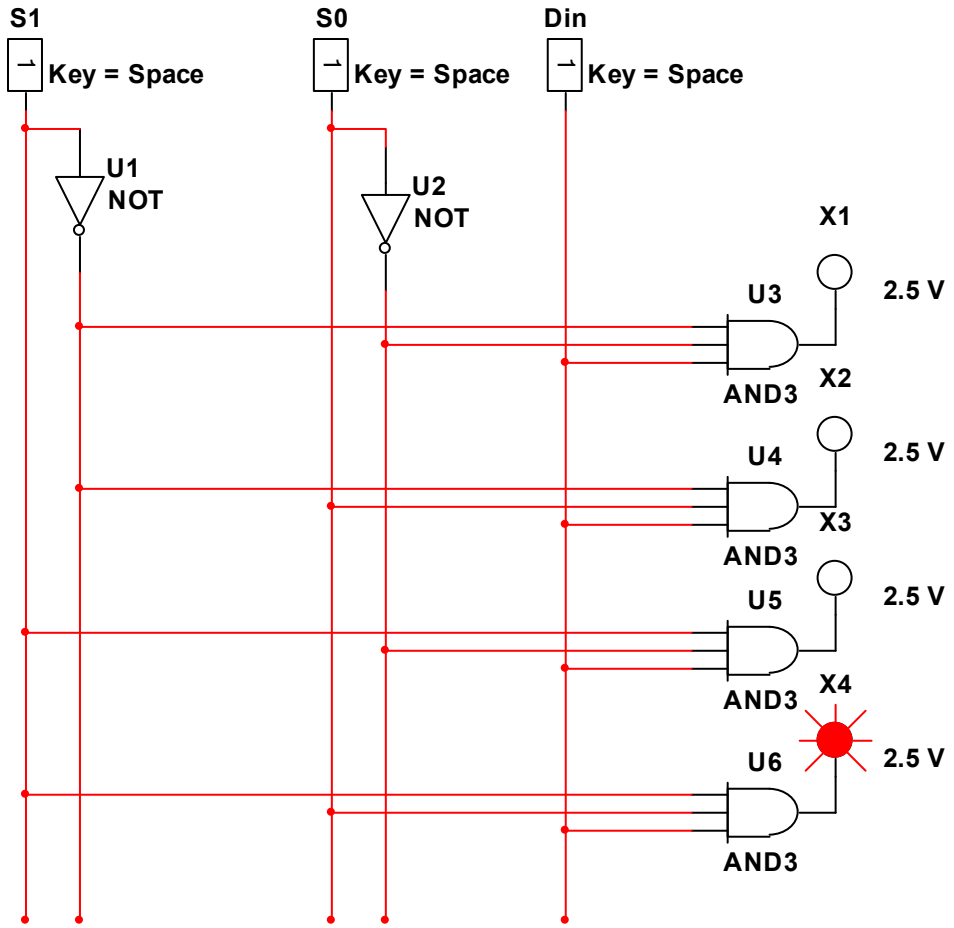
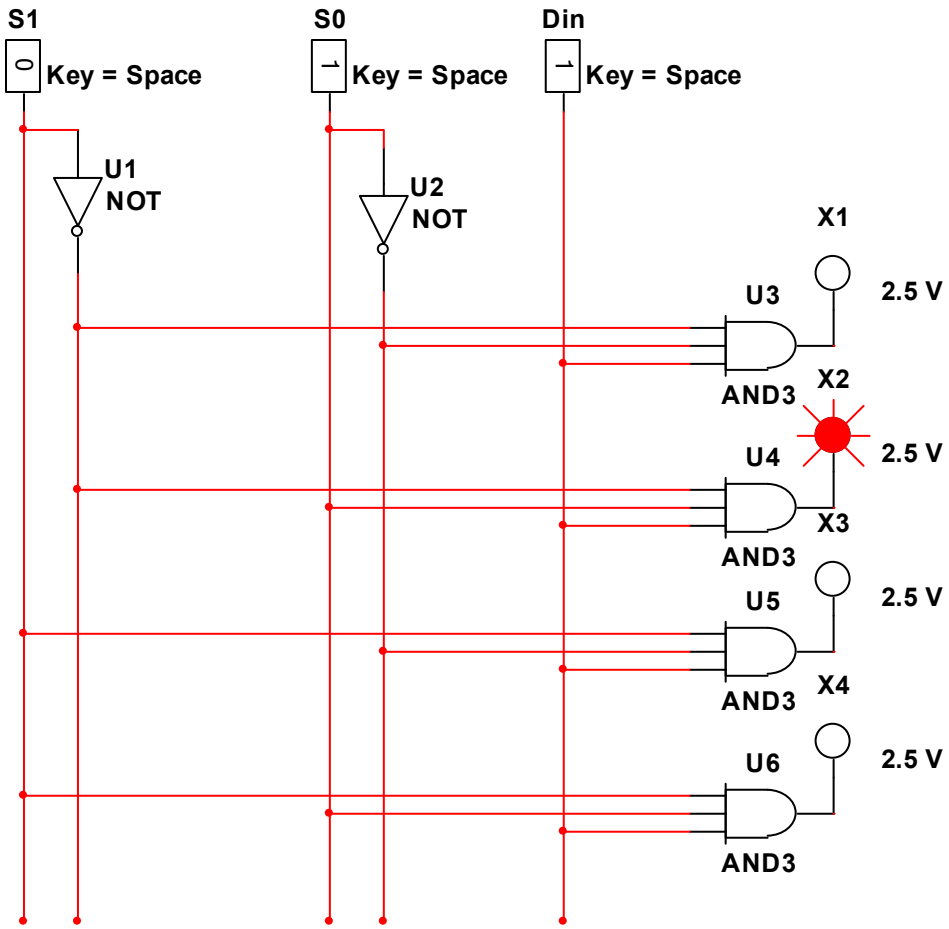
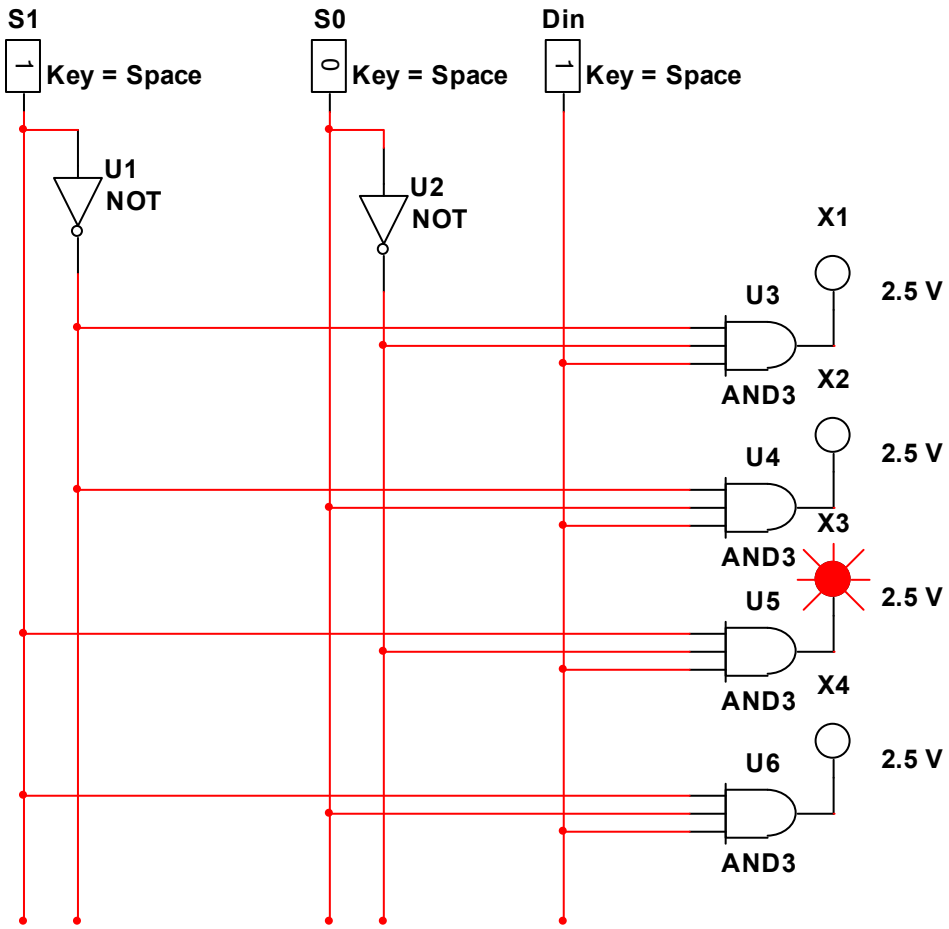


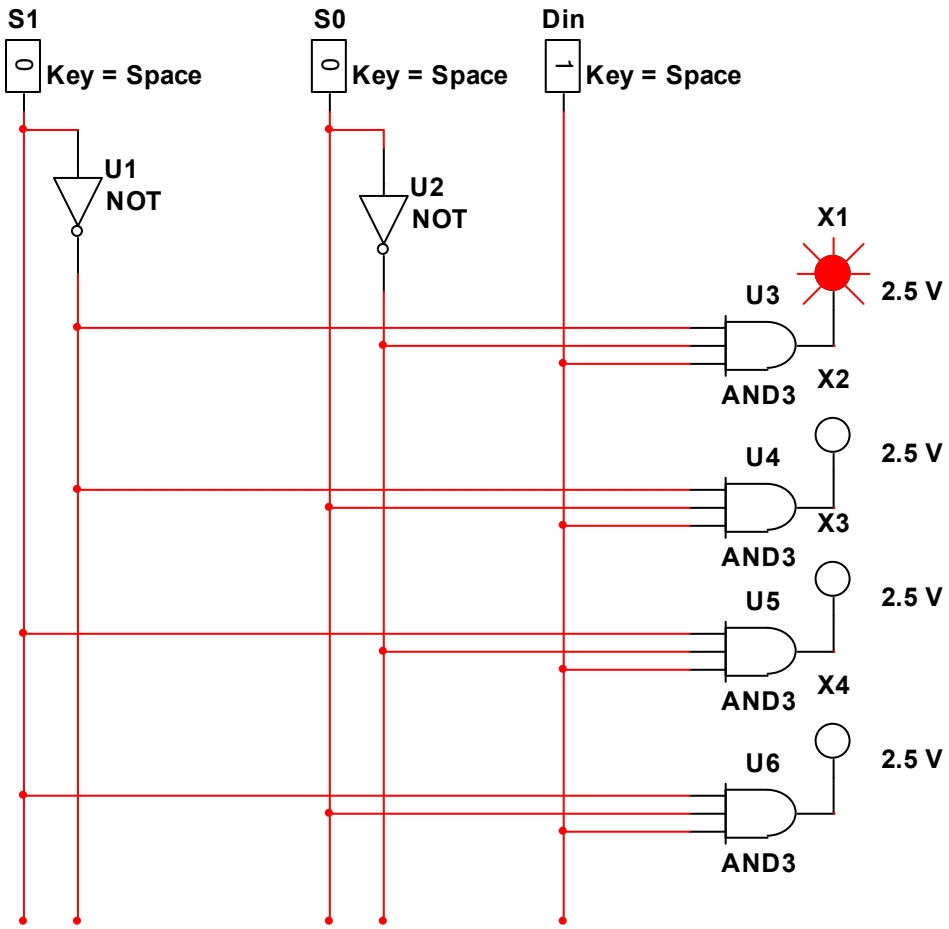
Table:

S1	S0	D0	D1	D2	D3
0	0	Din	0	0	0
0	1	0	Din	0	0
1	0	0	0	Din	0
1	1	0	0	0	Din




S1
0
Key = Space
S0
1
Key = Space
Din
1
Key = Space
U1
NOT
U2
NOT
X1
U3
2.5 V
AND3
X2
U4
2.5 V
X3
AND3
U5
2.5 V
AND3
X4
U6
2.5 V
AND3


S1
Key = Space
S0
Key = Space
Din
Key = Space
U1
NOT
U2
NOT
X1
U3
2.5 V
AND3
X2
U4
2.5 V
X3
AND3
U5
2.5 V
AND3
X4
U6
2.5 V
AND3



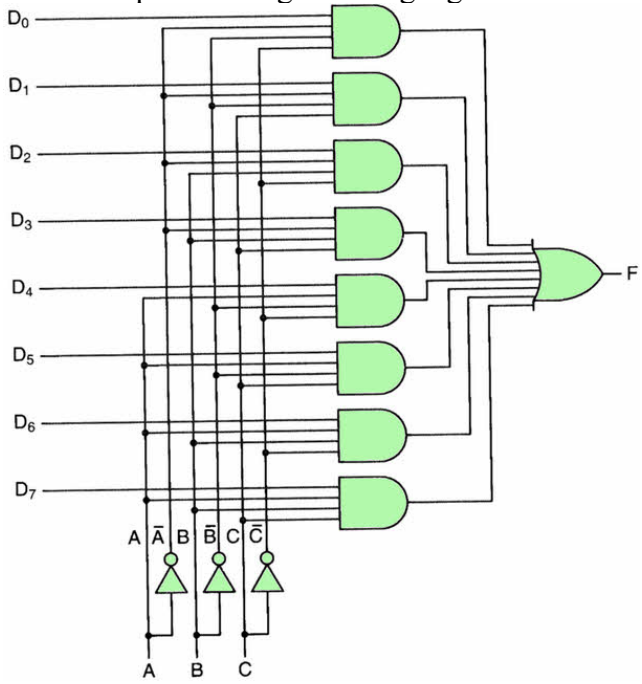
Result & Discussion:

The experiment was successfully conducted. We have seen the operation of multiplexer (MUX) and de-multiplexer (DEMUX). For the multiplexer it was showing the corresponding output as shown in the first truth table. Also demultiplexer was showing results like the 2nd truth table. Demultiplexer acts like a decoder. Overall the circuits were implemented successfully and it was a successful experiment.

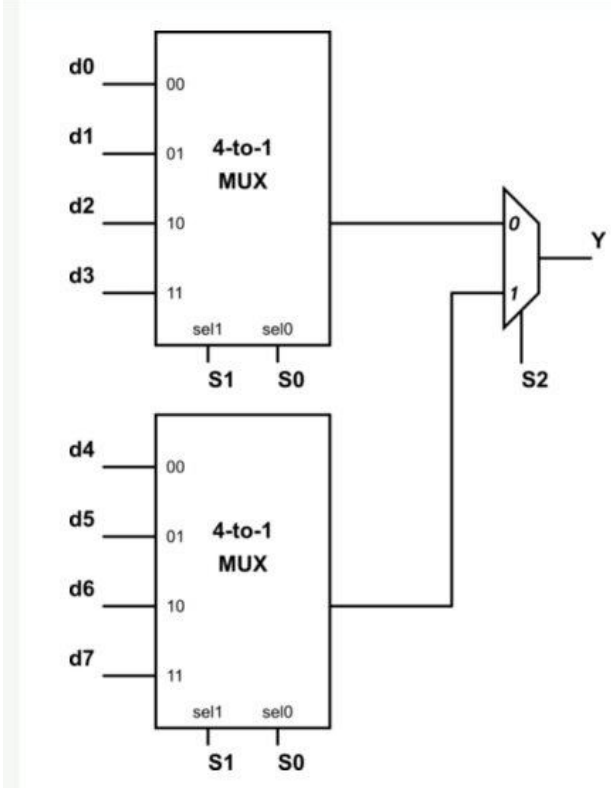
Questions for report writing:

Design and simulate the following circuits.

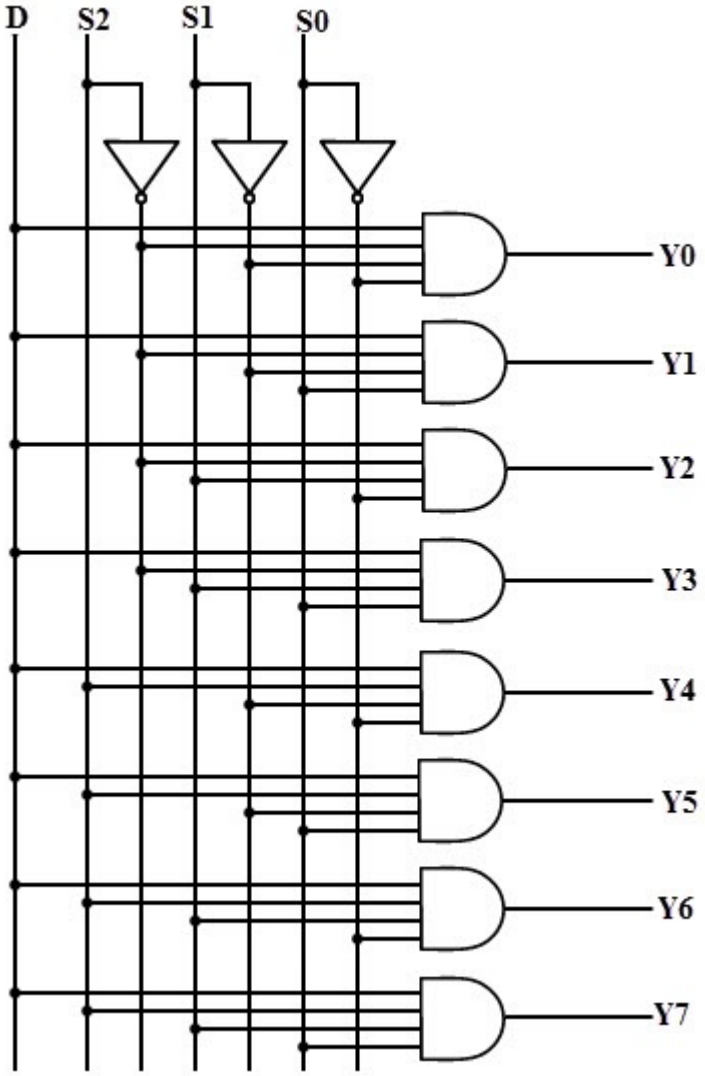
1) 8to1 multiplexer using basic logic gates.



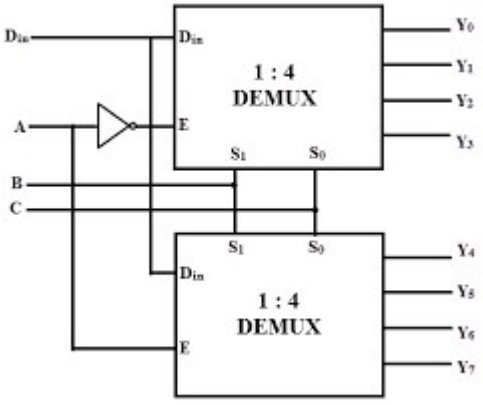
2) 8to1 multiplexer using 4to1 and/or 2to1 multiplexers.



3) 1to8 demultiplexer using basic logic gates.



4) 1to8 demultiplexer using 1to4 and/or 1to2 demultiplexers.



Conclusions:

It had been initially set by interpreting the data and determining the extent to which the experiment had been successful in complying with the goal. We had to discuss about any mistake while conducting the investigation and described ways the study could have been improved which might had made by us.

Appendices:

IC configurations: