

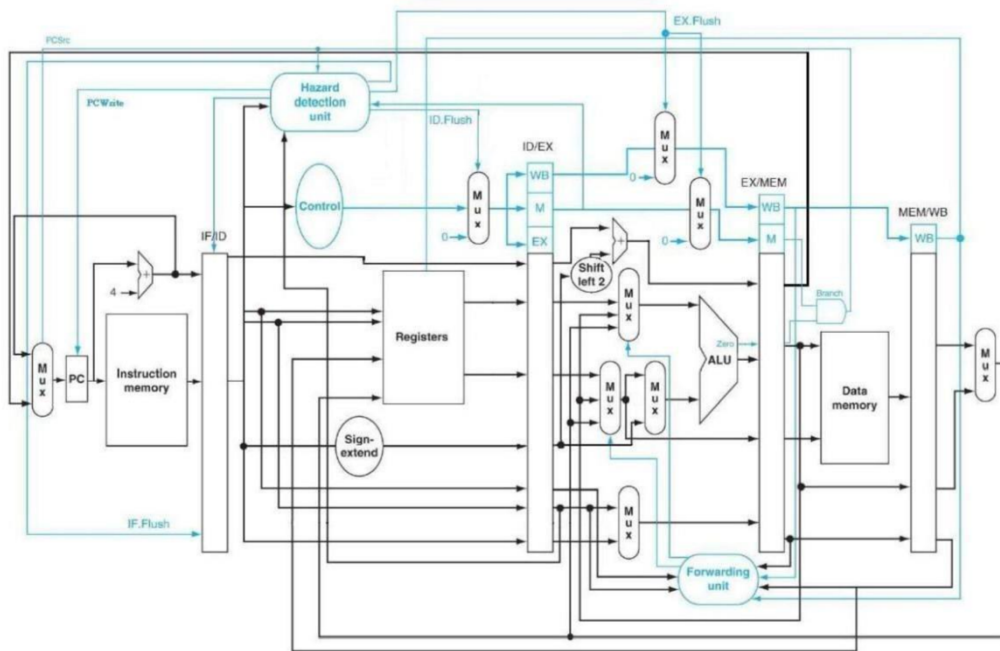
Computer Organization Lab5

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使用iverilog測試

Architecture diagrams:



Hardware module analysis:

Hazard_Detection_Unit:

Check if EX or MEM is branch => Stall

if Load-use => Stall

Forwarding_Unit:

If (WB_Regwrite or MEM_Regwrite) and (WB_Rd == EX_rs or WB_Rd == EX_rt or MEM_Rd == EX_rs or MEM_Rd == EX_rt)
=> Forward

Else is same with Lab4.

Finished part:

TestCase1

```
ruccccc@Rucs-MBP:~/Library/CloudStorage/OneDrive-國立陽明交通大學/Undergrated/Co...
~/L/C1/OneDrive-國/U/C/Compu/Lab/Lab5 | main >1 !8 ?3 ----- 21:56:35
> ./testbench.o
VCD info: dumpfile testbench.vcd opened for output.
WARNING: testbench.v:50: $readmemb(testbench/CO_P5_test_1.txt): Not enough words in the
file for the requested range [0:20].
##### clk_count =17          60 #####
#####
=====Register=====
r0 =0   , r1 =16  , r2 =256 , r3 =8   , r4 =16  , r5 =8   , r6 =24  , r7 =26
r8 =8   , r9 =1   , r10=0   , r11=0   , r12=0   , r13=0   , r14=0   , r15=0
r16=0   , r17=0   , r18=0   , r19=0   , r20=0   , r21=0   , r22=0   , r23=0
r24=0   , r25=0   , r26=0   , r27=0   , r28=0   , r29=0   , r30=0   , r31=0
=====Memory=====
m0 =0   , m1 =16  , m2 =0   , m3 =0   , m4 =0   , m5 =0   , m6 =0   , m7 =0
m8 =0   , m9 =0   , m10=0   , m11=0   , m12=0   , m13=0   , m14=0   , m15=0
m16=0   , m17=0   , m18=0   , m19=0   , m20=0   , m21=0   , m22=0   , m23=0
```

與預期結果相同。

Testcase2:

```
ruccccc@Rucs-MBP:~/Library/CloudStorage/OneDrive-國立陽明交通大學/Undergrated/Co...
~/L/C1/OneDrive-國/U/C/Compu/Lab/Lab5 | main >1 !8 ?3 ----- 21:55:50
> ./testbench.o
VCD info: dumpfile testbench.vcd opened for output.
##### clk_count =70          100 #####
#####
=====Register=====
r0 =0   , r1 =0   , r2 =16  , r3 =6   , r4 =0   , r5 =16  , r6 =0   , r7 =0
r8 =2   , r9 =0   , r10=0   , r11=0   , r12=0   , r13=0   , r14=0   , r15=0
r16=0   , r17=0   , r18=0   , r19=0   , r20=0   , r21=0   , r22=0   , r23=0
r24=0   , r25=0   , r26=0   , r27=0   , r28=0   , r29=0   , r30=0   , r31=0
=====Memory=====
m0 =4   , m1 =1   , m2 =0   , m3 =6   , m4 =0   , m5 =0   , m6 =0   , m7 =0
m8 =0   , m9 =0   , m10=0   , m11=0   , m12=0   , m13=0   , m14=0   , m15=0
m16=0   , m17=0   , m18=0   , m19=0   , m20=0   , m21=0   , m22=0   , m23=0
m24=0   , m25=0   , m26=0   , m27=0   , m28=0   , m29=0   , m30=0   , m31=0
```

與預期結果相同。

Problems you met and solutions:

1. Hazard Detection: 在 Branch 時沒有將前面的東西 flush 掉。
2. Forwarding Unit: MEM 的結果應該優先於 WB 的結果 forwarding 但我少了
這個判斷。

Summary:

這比我想像中的難好多喔。