Computer Organization Lab5

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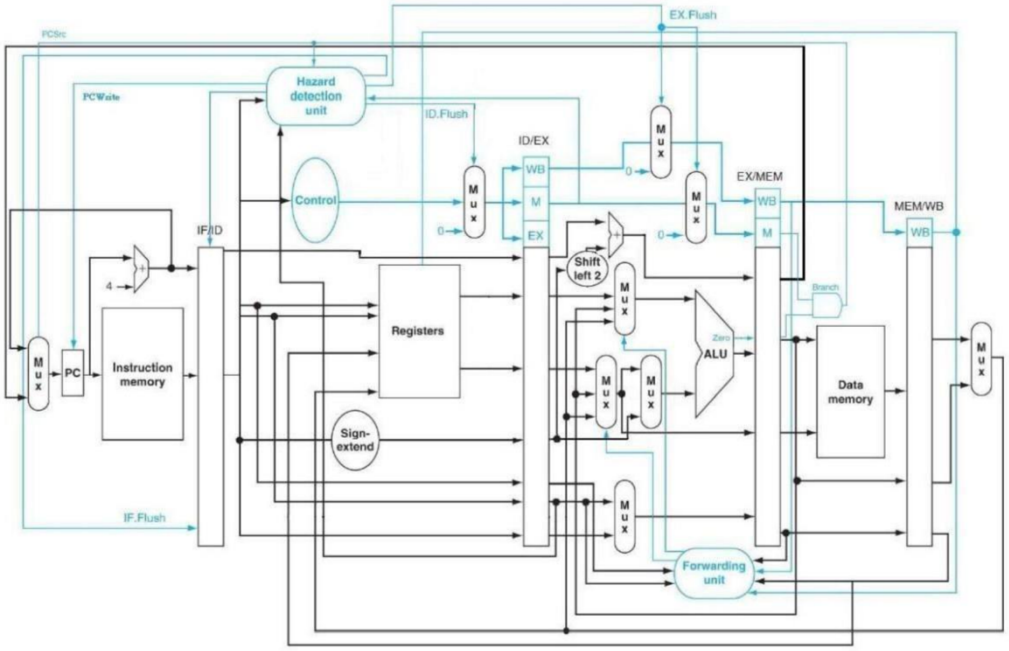
使用iverilog測試

Architecture diagrams:



Hardware module analysis:

Hazard_Detection_Unit:

Check if EX or MEM is branch => Stall

if Load-use => Stall

Forwarding_Unit:

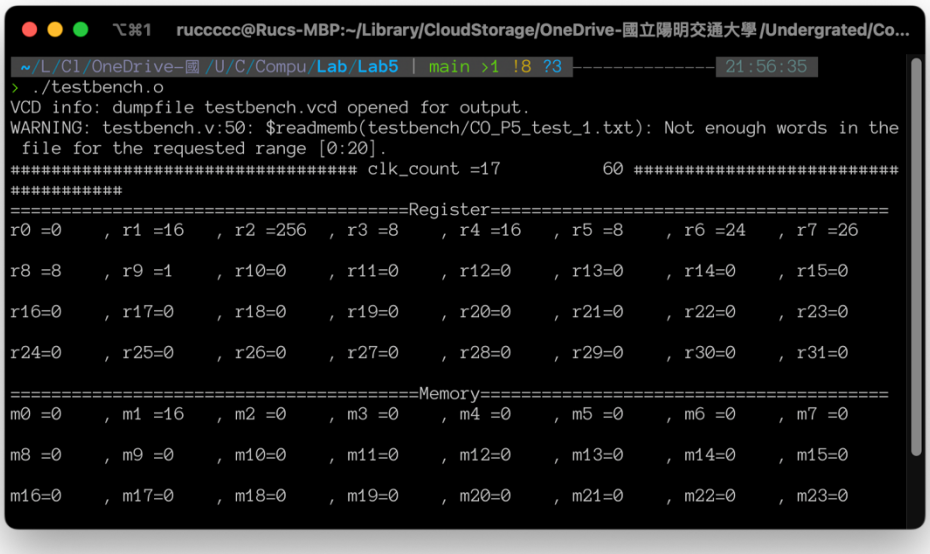
If (WB_Regwrite or MEM_Regwrite) and (WB_Rd == EX_rs or WB_Rd == EX_rt or MEM_Rd == EX_rs or MEM_Rd == EX_rt

=> Forward

Else is same with Lab4.

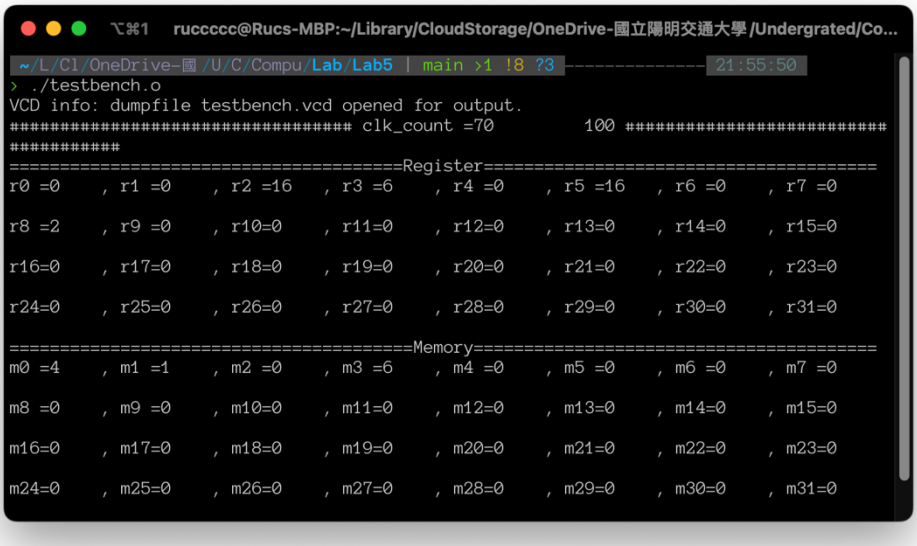
Finished part:

TestCase1



與預期結果相同。

Testcase2:



與預期結果相同。

Problems you met and solutions:

1. **Hazard Detection: 在 Branch 時沒有將前面的東西 flush 掉。**
2. **Forwarding Unit: MEM 的結果應該優先於 WB 的結果 forwarding 但我少了這個判斷。**

Summary:

這比我想像中的難好多喔。