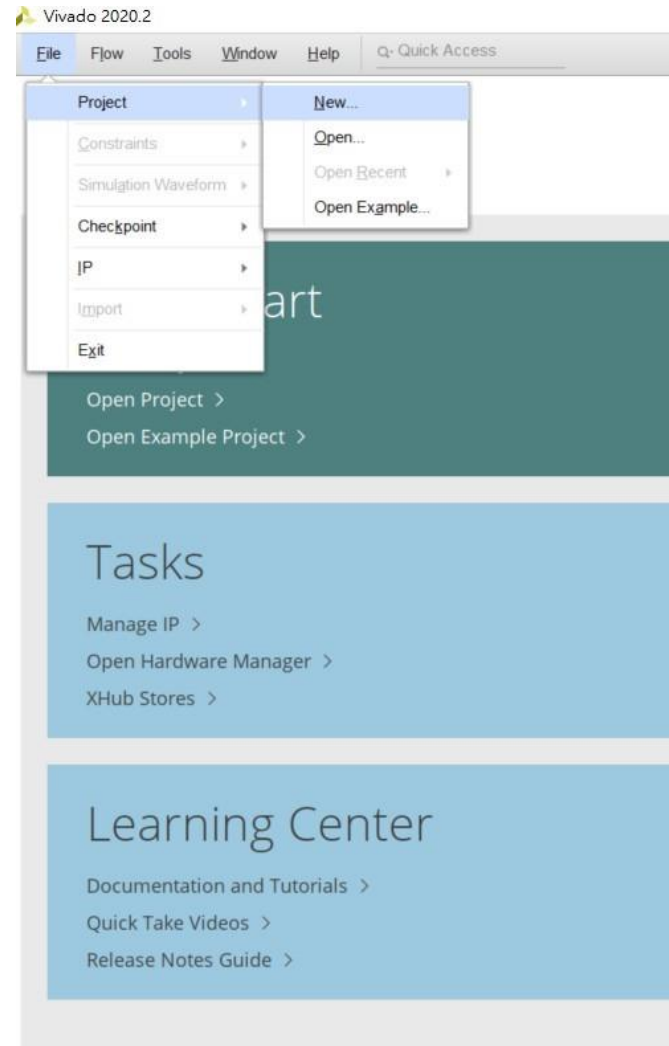


Lab 0

Create a Project in Vivado &
Do a Verilog Practice

Create New Project (1/4)

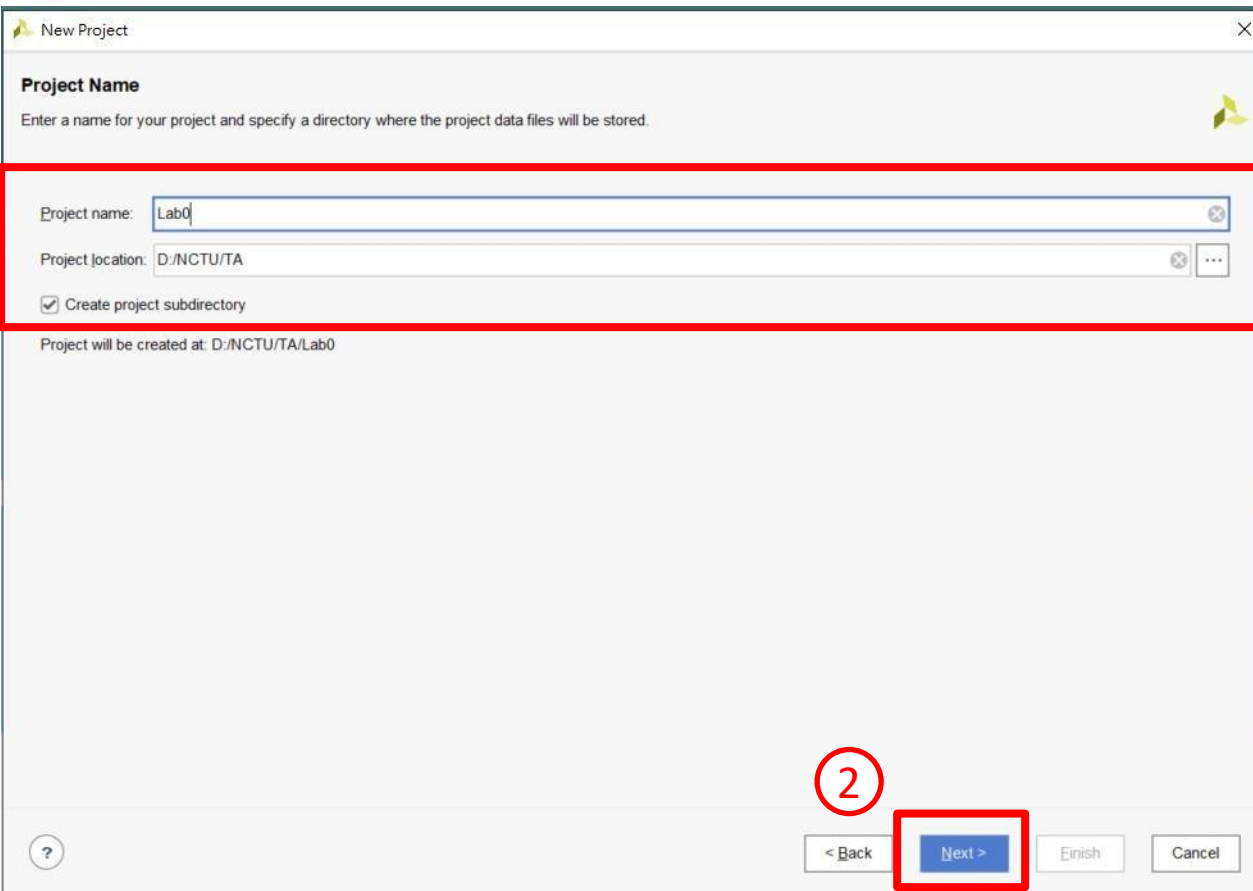
- Create a new project.



Create New Project (2/4)

- Fill in Project name and Project location.

1



New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: Lab0

Project location: D:/NCTU/TA

☒ Create project subdirectory

Project will be created at: D:/NCTU/TA/Lab0

2

< Back Next > Finish Cancel

Create New Project (3/4)

- Choose RTL Project.
 - Tick the following boxes.

New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☒ Do not specify sources at this time
☒ Project is an extensible Vitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

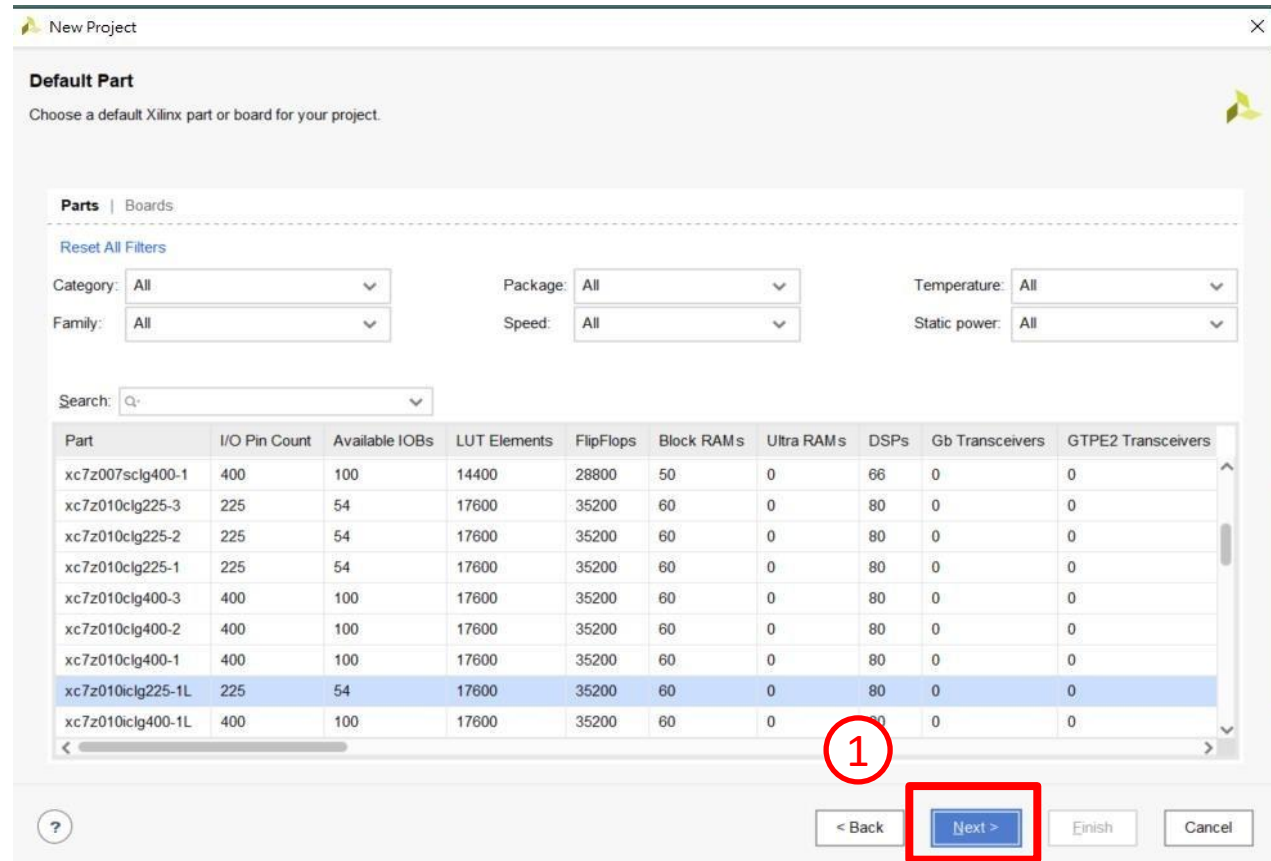
☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

? < Back **Next >** Finish Cancel

Create New Project (4/4)

- Select parts(boards) arbitrarily since we don't have to implement the design on FPGA.



New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All Package: All Temperature: All
Family: All Speed: All Static power: All

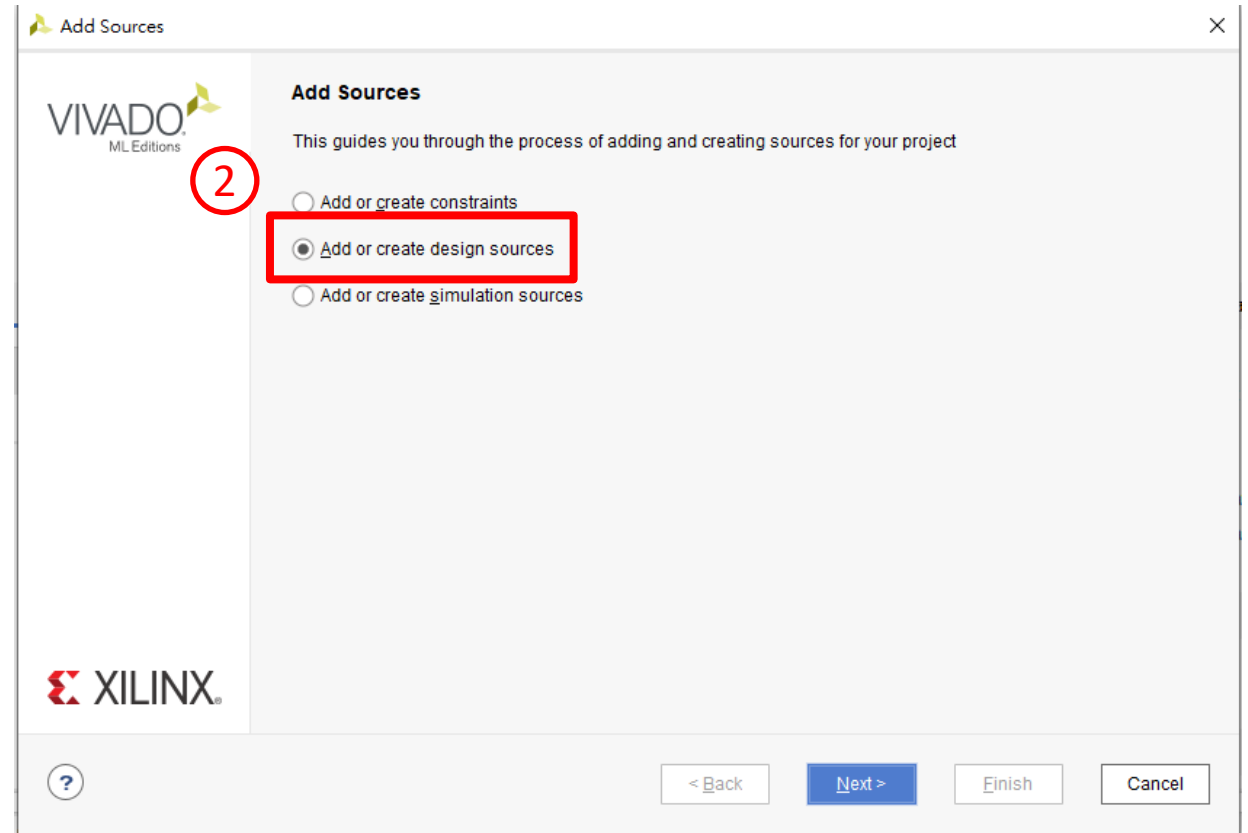
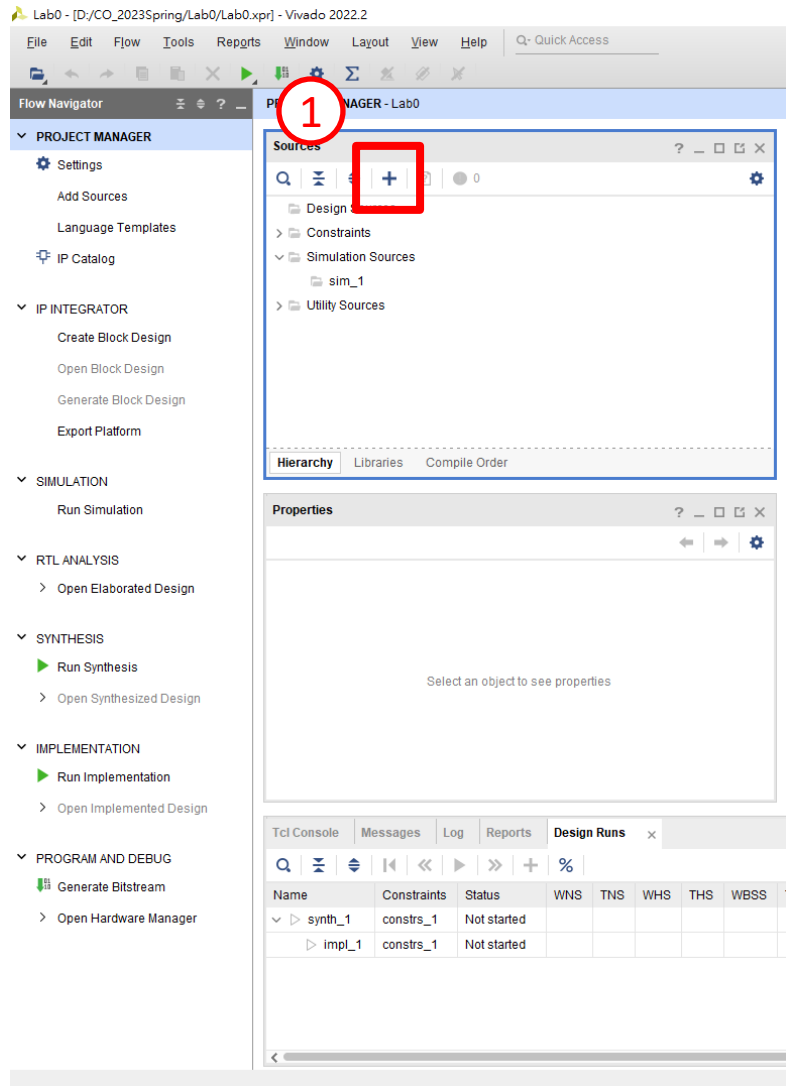
Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transceivers
xc7z007scig400-1	400	100	14400	28800	50	0	66	0	0
xc7z010iclg225-3	225	54	17600	35200	60	0	80	0	0
xc7z010iclg225-2	225	54	17600	35200	60	0	80	0	0
xc7z010iclg225-1	225	54	17600	35200	60	0	80	0	0
xc7z010iclg400-3	400	100	17600	35200	60	0	80	0	0
xc7z010iclg400-2	400	100	17600	35200	60	0	80	0	0
xc7z010iclg400-1	400	100	17600	35200	60	0	80	0	0
xc7z010iclg225-1L	225	54	17600	35200	60	0	80	0	0
xc7z010iclg400-1L	400	100	17600	35200	60	0	80	0	0

1

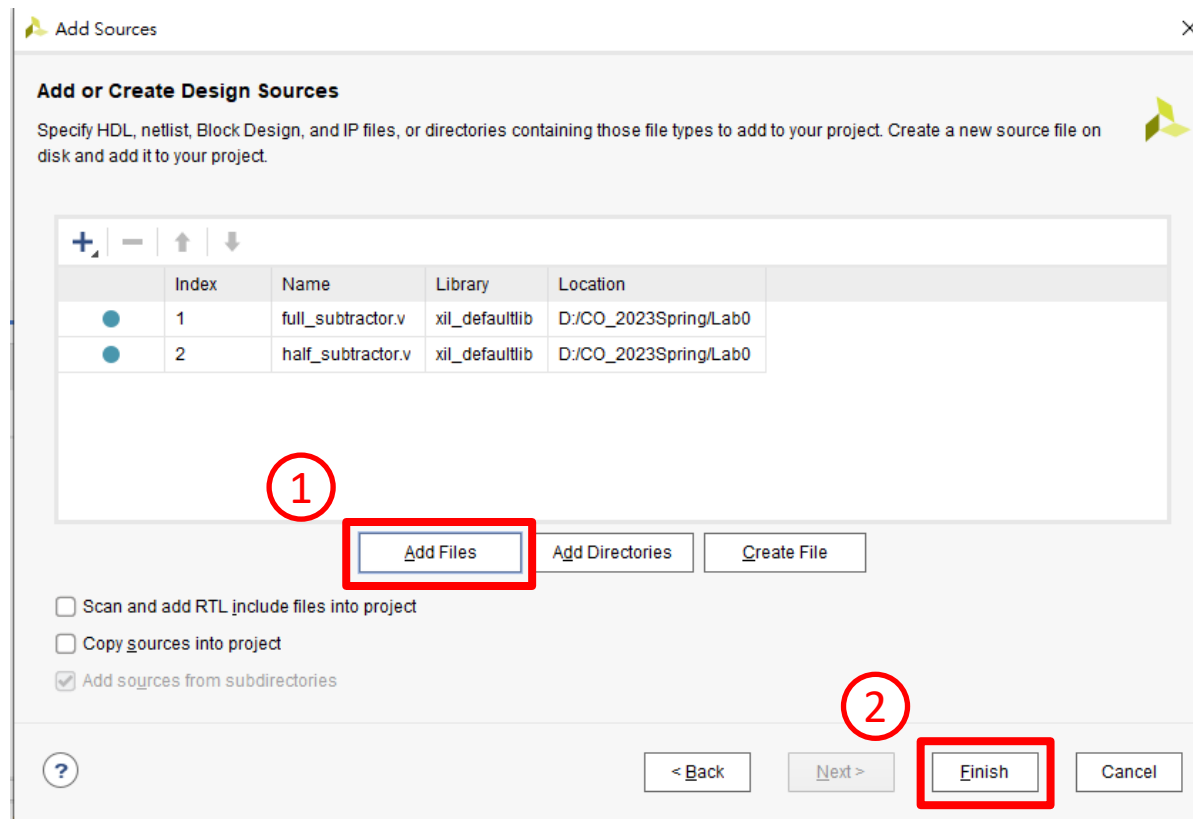
[? < Back](#) **Next >** [Finish](#) [Cancel](#)

Add Design Source (.v files) (1/2)

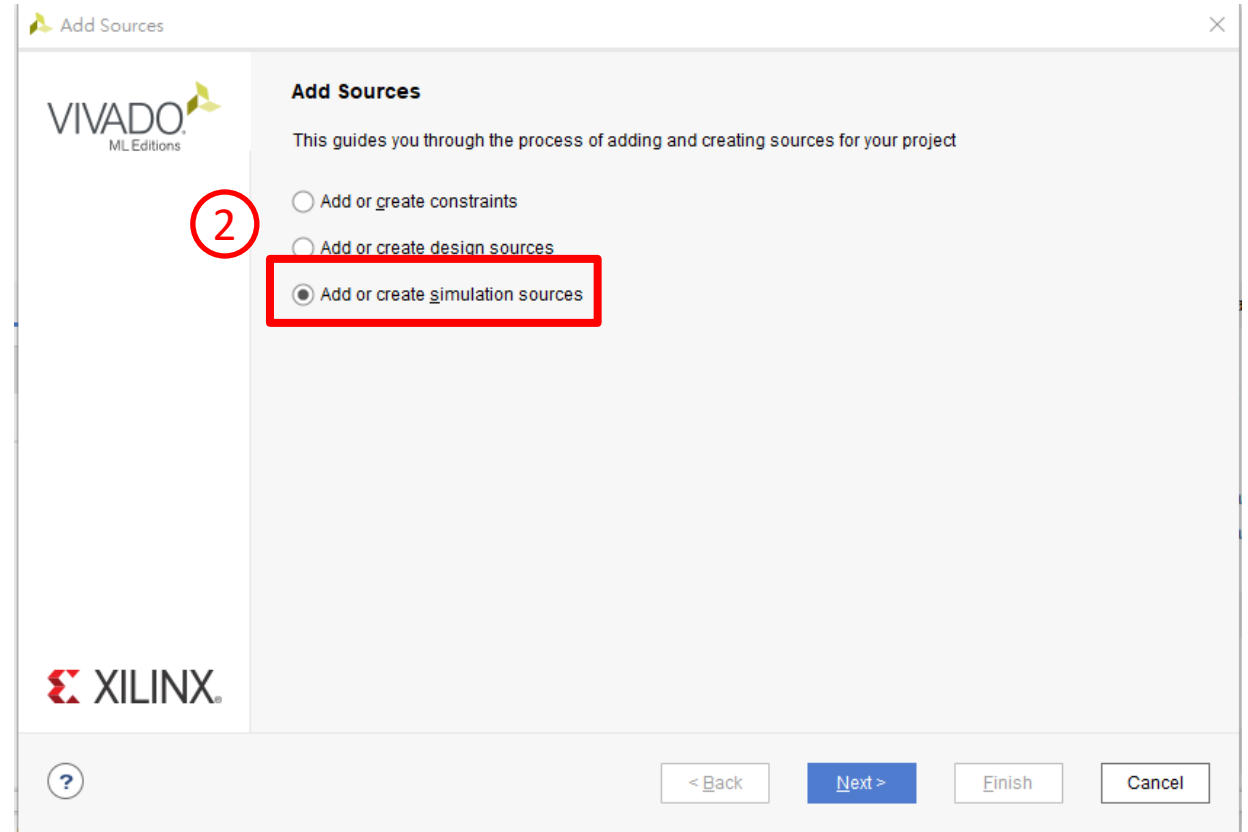
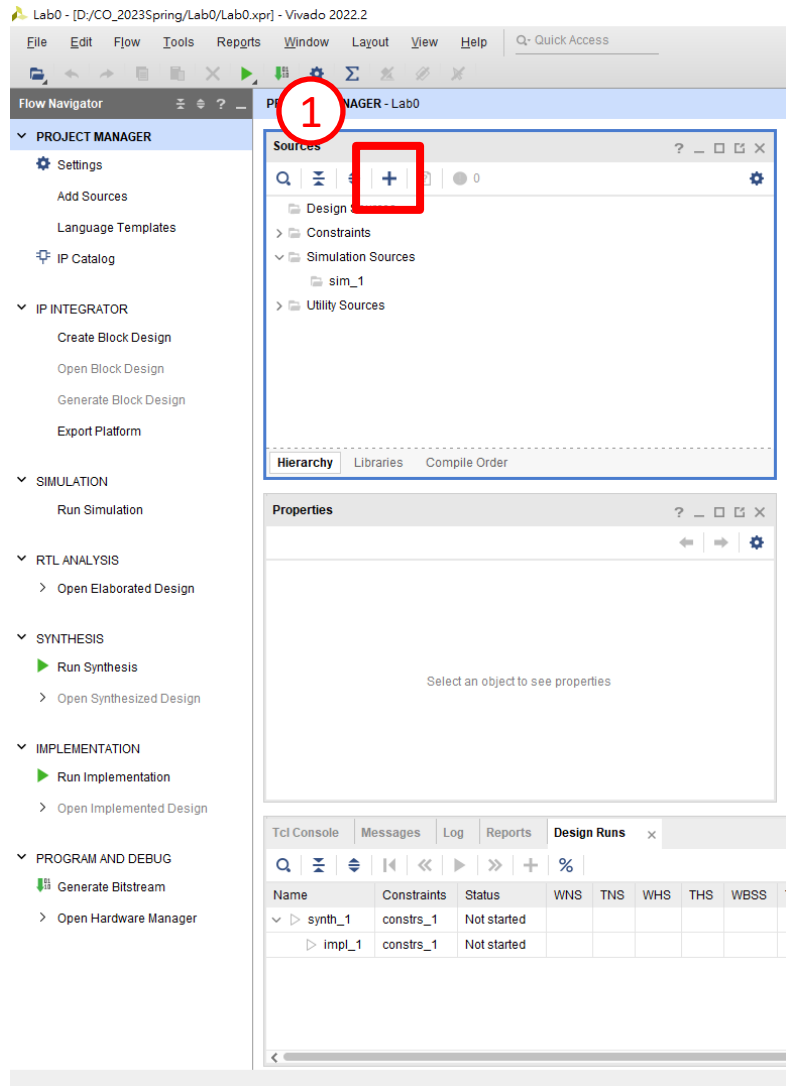


Add Design Source (.v files) (2/2)

- Add design sources
 - Not including testbench.v

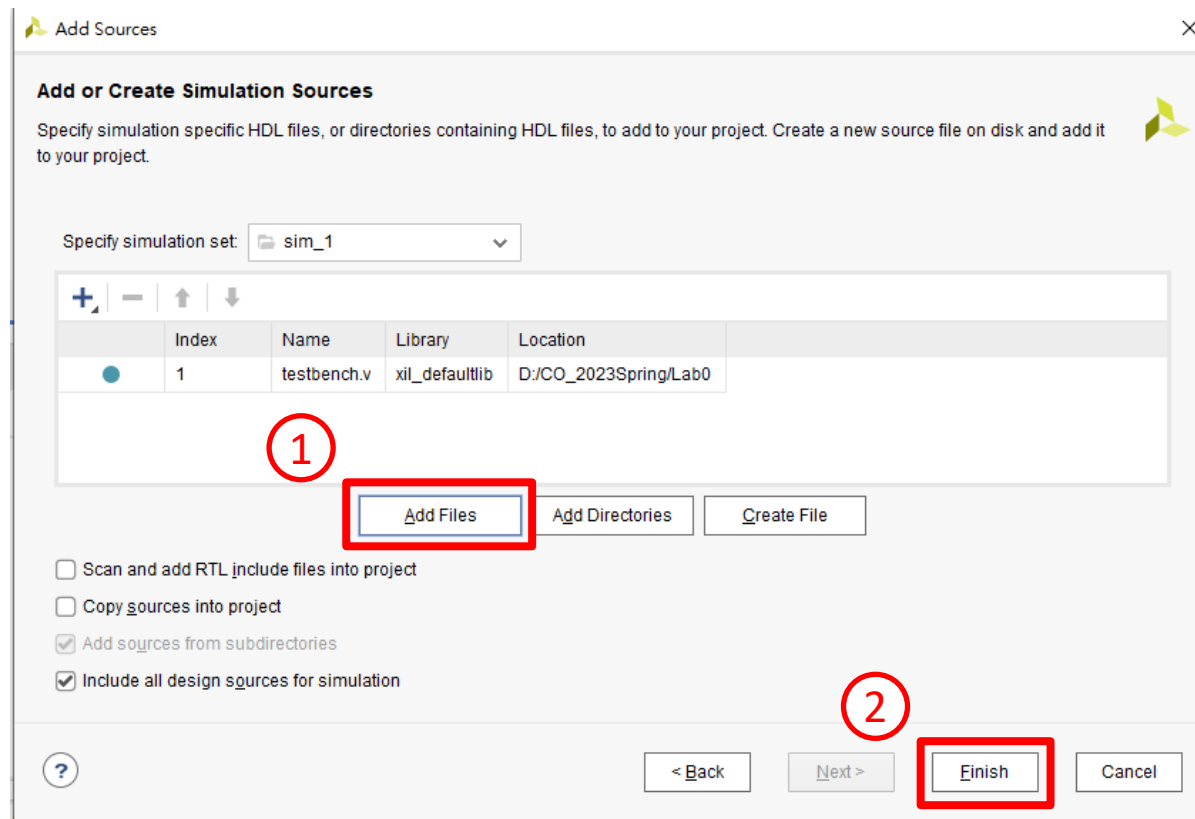


Add Simulation Source (testbench.v) (1/2)



Add Simulation Source (testbench.v) (2/2)

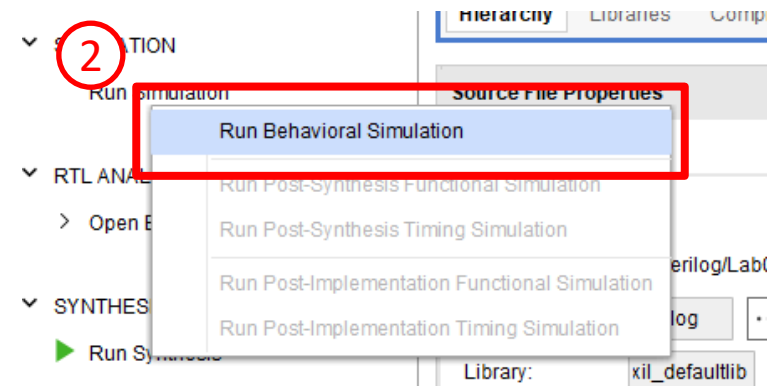
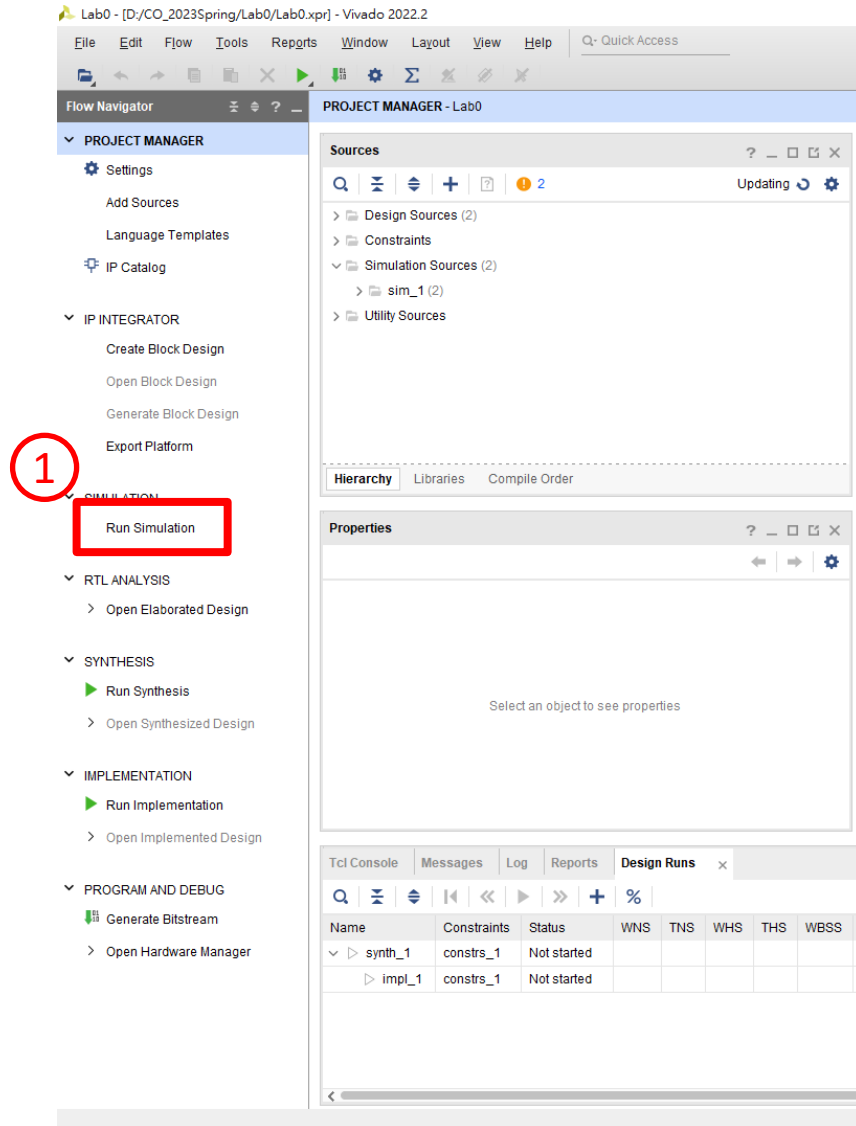
- Add testbench.v



How to Run Simulation (1/2)

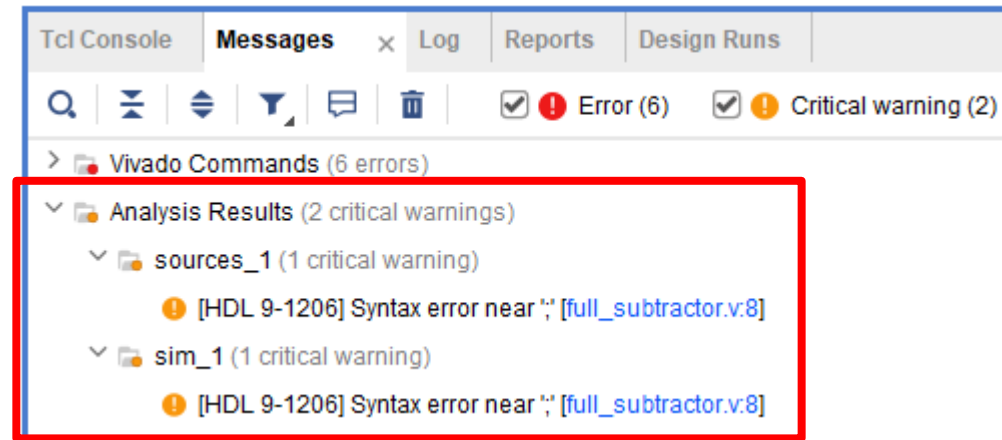
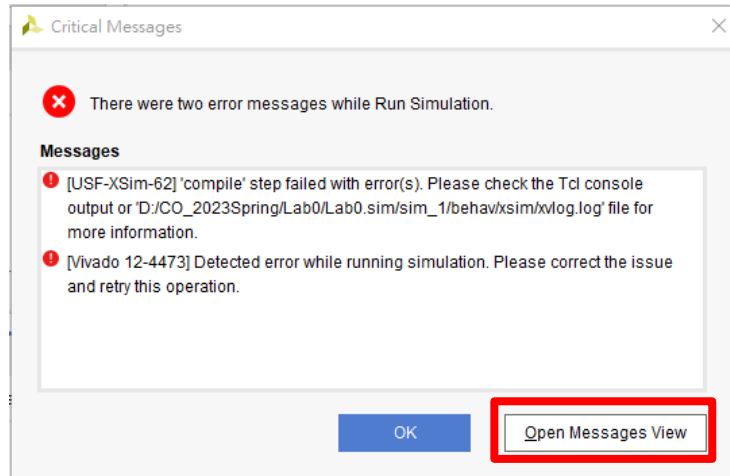
- After adding testbench into project, you can execute the behavioral simulation.
- It can help you debug with the signal waveform and check the correctness of your design.

How to Run Simulation (2/2)



Useful Information (1/2)

You can check out design error messages in Messages.

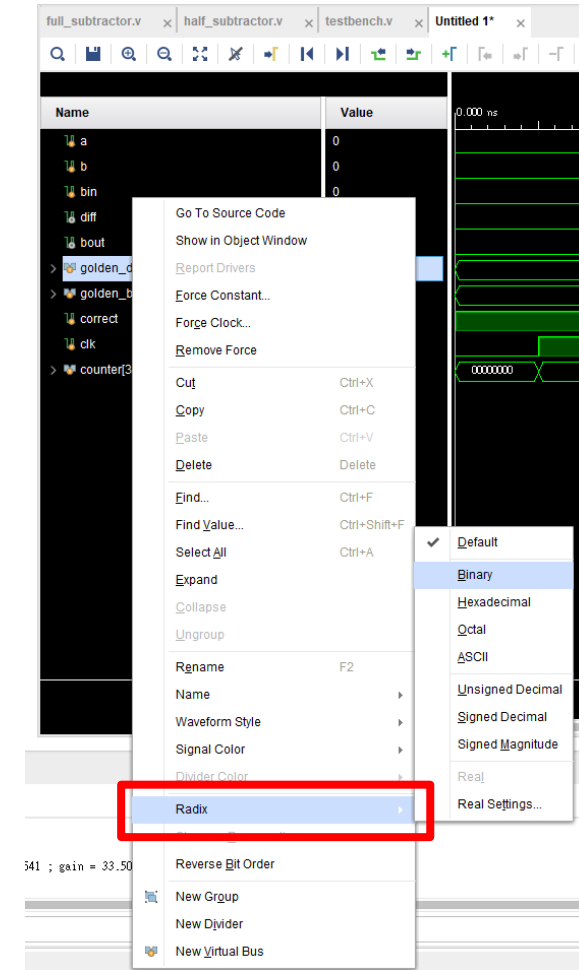
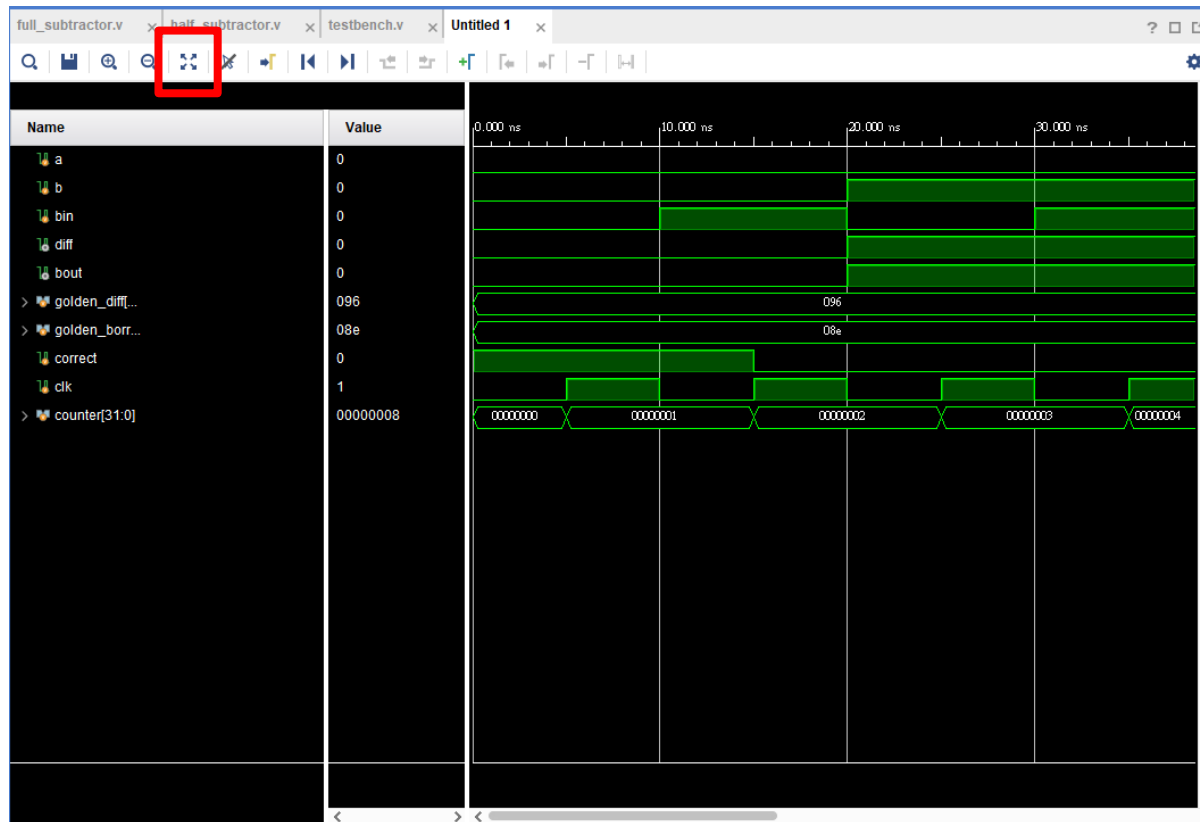


Possible design errors would be underlined in red.

```
module Full_Subtractor(  
    In_A, In_B, Borrow_in, Difference, Borrow_out  
);  
    input In_A, In_B, Borrow_in;  
    output Difference, Borrow_out;  
    wire ;
```

Useful Information (2/2)

This button makes your complete waveform fit your window size.



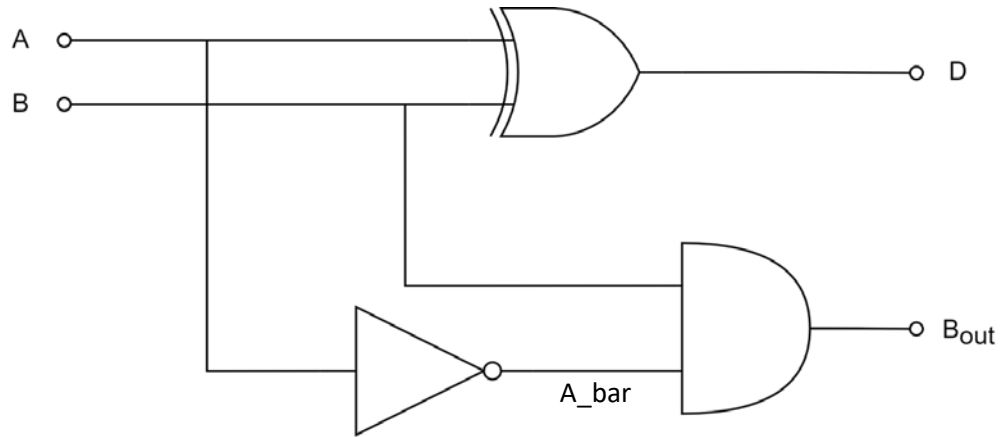
You can change the radix of the signal.
(default radix is decimal)



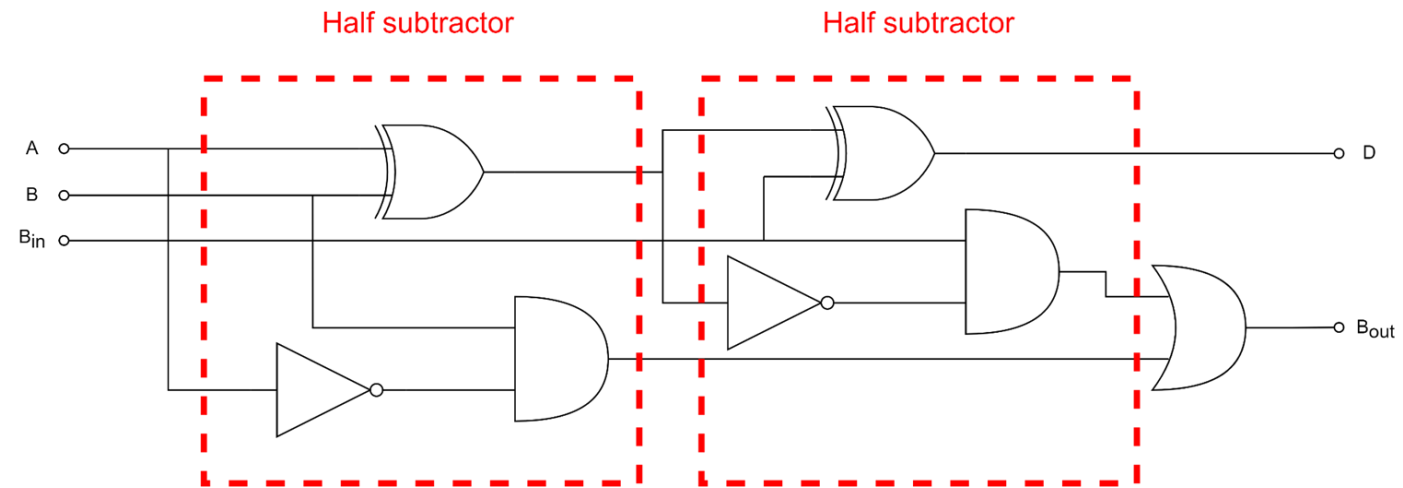
Lab0: Half Subtractor and Full Subtractor

- Implement the half subtractor and full subtractor without using '-' operation.
- We want you to practice how to implement the signal connection within the given circuit. We will give you example design sources and testbench.v.

Half Subtractor and Full Subtractor Circuit



Half Subtractor



Full Subtractor

Truth Table for Full Subtractor

Input			Output	
A	B	B _{in}	D	B _{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Verify the Correctness of Your Design

- We have enumerated all input cases in testbench.v.
- After simulation with our testbench.v, if your design is correct, you should see the message shown below in Tcl Console.

[illegible]

Note

- You don't have to submit anything in this lab.
- However, we recommend you to do this lab, so that you get familiar with Vivado and Verilog. Both of them would be used in future labs.

Any Problem?

- If you have any questions, feel free to ask on the Facebook discussion forum. Your questions may also be other people's questions.
 - <https://www.facebook.com/groups/1185546902165340/>