Banasthali Vidyapith
Faculty of Mathematics and Computing
Course Handout- B.Tech IT (III Semester) July 2023 –Dec 2023

Date: 30-June-2023

Course Code: CS 207 **Course Name: Computer Organization and Architecture**
Credit Points: 4 **Max. Marks: 100 (CA: 40 + ESA: 60)**
Course Instructors: **Dr. Gaurav Sharma (IT)**

Learning Outcomes:
After successful completion of the course, students will be able to:
- Use the concepts and design of all type of sequential and combinational circuits.
- Have knowledge to design and conduct experiments, as well as to analyze of the hardware of a computer system and its components such as control unit, arithmetic and logical (ALU) unit, input/output, and memory unit.
- Design techniques such as pipelining and microprogramming in the design of the central processing unit of a computer system.

Syllabus:

Section A

Computer Codes: Weighted and non-weighted, self-complementing codes.
Logic Gates and Boolean Algebra: Basic and universal gates, laws, canonical forms, simplification, k-map.
Combinational Circuits: Adder, subtractor, decoder, encoder, multiplexer, de-multiplexer, comparator, parity generator and checker.
Sequential Circuits: Introduction, latches and flip flops, timing diagrams, analysis and design of clocked sequential circuits, state reduction and assignment.

Section B

Counters and Registers: Synchronous and asynchronous counters, shift registers, serial adder.
Computer Organization and Design: Instruction formats, instruction set, instruction cycle.
Micro Programmed Control: Control memory, address sequencing, design of control unit.
Central Processing Unit: General register organization, stack organization, addressing modes, CISC and RISC characteristics.

Section C

Pipelining and Vector Processing: Parallel processing, pipelining, arithmetic pipeline, instruction pipeline, RISC pipeline, data control and hazards, vector processing.
Memory Organization: Memory hierarchy, characteristics, RAM and ROM chips, associative memory, cache memory - features, principle of locality, address mapping- direct, associative, set-associative, cache performance, cache coherence.
Input - Output Organization: Interface, modes of transfer -programmed I/O, interrupt initiated, DMA; I/O processor.

Suggested Books:

R1: Mano, M. M. (2017). *Digital logic and Computer Design*. Pearson Education India.
R2: Mano, M. M. (2003). *Computer System Architecture*. Prentice-Hall of India.
R3: Stallings, W. (2003). *Computer organization and architecture: designing for performance*. Pearson Education India.
R4: Tocci, R. J. (1991). *Digital systems: principles and applications.* Pearson Education India.

Suggested E-Learning Material:

E1:http://home.ustc.edu.cn/~louwenqi/reference_books_tools/Computer%20Organization%20and%20Architecture%2010th%20-%20William%20Stallings.pdf
E2: The Computing Technology Inside Your Smartphone https://www.edx.org/course/computing-technology-inside-smartphone-cornellx-engri1210x-0
E3: Computer Organizations and Architecture- https://nptel.ac.in/courses/106103068
E4: Digital Electronics Circuits- https://www.coursera.org/learn/digital-systems

Evaluation Scheme:

Component	Marks	Submission Date	Allotment
Home Assignment I**	10	28 August, 2023	Topics shall be allotted in the class by 12 August 2023
Periodical Test I	10	8-11 September 2023*	Section A
Home Assignment II**	10	11 October, 2023	Topics shall be allotted in the class 25 September 2023
Periodical Test II	10	4-8 November 2023*	Section B
Semester Examination	60	2-18 December 2023*	Whole Syllabus

*Subject to Change

*****Assignment marks will be based on written document, viva-voce, online test, and any other components as decided by the instructors on the regular basis.

Lecture-Wise Schedule:

Lec. No.	Topics to be covered	References
	SECTION A	
1-3	**Computer Codes**: Weighted and non-weighted, self-complementing codes.	R1, R4
4-8	**Logic Gates and Boolean Algebra**: Basic and universal gates, laws, canonical forms, simplification, k-map.	R1, R4, E4
9-12	**Combinational Circuits**: Adder, subtractor, decoder, encoder, multiplexer, de-multiplexer, comparator, parity generator and checker.	R1, R4, E4
13-16	**Sequential Circuits:** Introduction, latches and flip flops, timing diagrams, analysis design of clocked sequential circuits, state reduction and assignment.	R1, R4, E4
17-19	Design of clocked sequential circuits, state reduction and assignment.	R1, R4, E4
	SECTION B	
20-25	**Counters and Registers:** Synchronous and asynchronous counters, shift registers, serial adder.	R2, R3, E3
26-28	**Computer Organization and Design**: Instruction formats, instruction set, instruction cycle.	R2, R3, E3
29-34	**Micro Programmed Control**: Control memory, address sequencing, design of control unit.	R2, R3,E3
35-36	**Central Processing Unit**: General register organization, stack organization, addressing modes, CISC and RISC characteristics.	R2, R3, E3
	SECTION C	
37-40	**Pipelining and Vector Processing**: Parallel processing, pipelining, arithmetic pipeline, instruction pipeline, RISC pipeline, data control and hazards, vector processing	R2, R3, E3
41-45	**Memory Organization:** Memory hierarchy, characteristics, RAM and ROM chips, associative memory, cache memory - features, principle of locality, address mapping- direct, associative, set-associative, cache performance, cache coherence	R2, R3, E3

46-50	**Input - Output Organization**: Interface, modes of transfer -programmed I/O, interrupt initiated, DMA; I/O processor. **Course Revision & Problem Discussions**	R2, R3, E3

Dr. Gaurav Sharma - IT