# Module 2: From Wafer To Package: Assembly & Package Manufacturing Essentials

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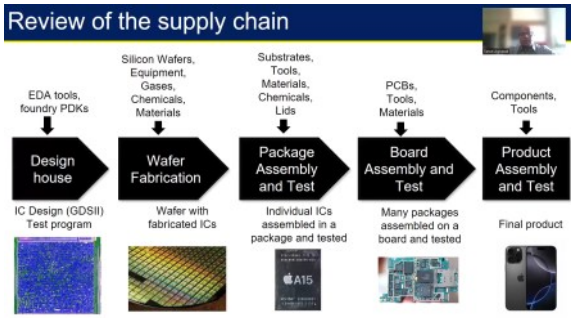
**L1: Setting The Stage: Supply Chain & Facilities**

Review of Supply Chain

1. Design Houses:
   Use EDA tools, Foundry PDKs to design an IC (GDSII) Test program
2. Wafer Fabrication:
   Use silicon wafers, Equipment, Gasses, Chemicals & Materials are used to fabricate the design.
3. Package, Test & Assembly:
   Use substrates, Tools, Material & Chemicals to assemble, test & package individual dies.
4. Board Assembly:
   Take all PCBs, Tools, ICs to assemble packages on a board.
5. Product Assembly & Test:
   Combine boards & other parts to build product & test it




Once dies are fabricated, we probe them & test in order to establish performance & functionality

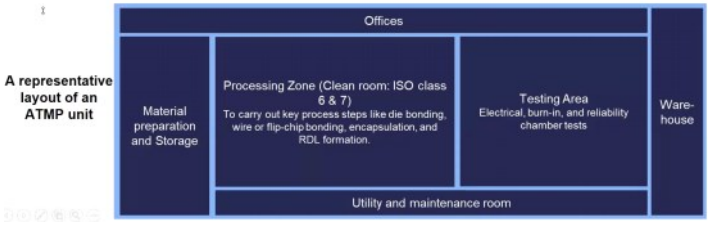
**Intro To Package Manufacturing Unit:**

Process: ATMP: Assembly, Testing, Marking & Packaging
Organizations: OSAT: Outsourced Semiconductor Assembly.
Players: ASE, Amkor & Tata

ATMP units could be in-house & may receive ICs from around the globe.
But OSAT is just outsourced work, someone else manufactures & others package.

E.g.: Micron ATMP at Sanand Total Area: 1.4 M SQFT & clean room (Class 1000/10000) of 500000 SQFT

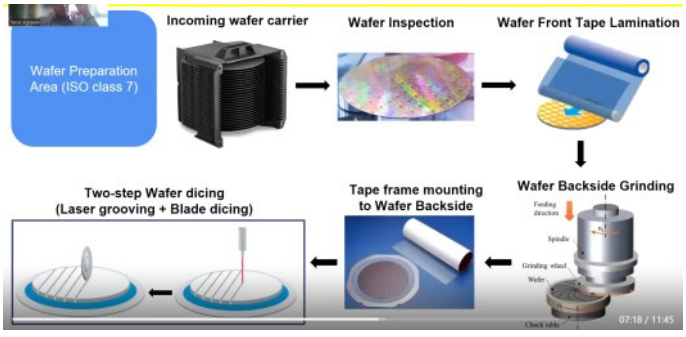
Biggest part of ATMP is done in a cleanroom: Classes could be ISO 6/7. 20-30% space is take by Testing area. Need dedicated HVAC & utilities.




Activities Inside the Cleanroom:

1. Wafer Preparation: Incoming wafer carries are brought into ISO class 7 cleanrooms
   When circuits are fabricated, all processes are carried out on the front side: The back only acts as a substrate & offers mechanical support.
2. Inspection: All wafers are inspected to avoid processing of bad wafers
3. Front Side Lamination: Since all processes are done on back side, we laminate the front side of the wafer
4. Backside Grinding: Wafer is flipped. Wafer is held on a chuck on a table. A spindle with a grinding wheel removes excess silicon. Must be done properly to avoid excess stress.
5. Mounting Backside Frame: Mount a tap frame on the back side of the metal frames on which the wafers are placed.
6. Wafer Dicing: Laser grooving + Blade dicing to split dies from wafer.
7. Inspection & SPC

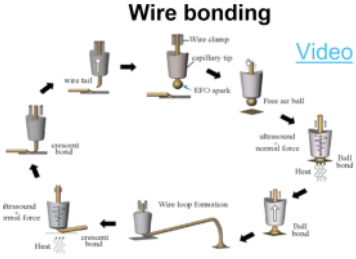
12 Inch Wafers thickness ~ 700 micron thick

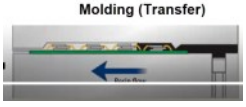


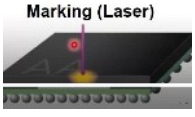

**L3: Wire Bond Packaging: Assembly & Manufacturing Essentials**

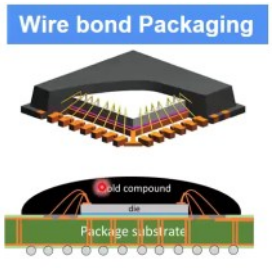
For Packaging, we have 3 options:

1. Wire Bond Packaging:
   a. Die Attach: Here, we firstly apply epoxy on the carrier, pick a die from the diced wafer & place it on the die attach film on the carrier.
      Pattern of the die depends on speed of the process. More quicker the process, more the voids.
   b. Curing: The epoxy is the allowed to cure through UV or in an oven.
   c. Wire Bonding/Stitching:
      i. It starts with a gold wire with a free air ball at the end.
      ii. This ball is pressed on the die pad followed by application of pressure and ultrasound & heating to bond the free air ball.
      iii. The lead is moved up and bent towards the carrier pad.
      iv. The wire is pressed on the pad & we apply pressure, ultrasound and heat the pad to form a crescent bond.
      v. The wire is separated and with an EFO spark, a free air ball is formed.
   d. Moulding:
      The IC is moulded my using resin. It could be through transfer or other methods based on the material.
   e. Marking:
      Product details like codes, dates & batch numbers are printed on the package which help in identification of IC
   f. Singulation: If all packages made on same carrier, we dice them to individual ICs.

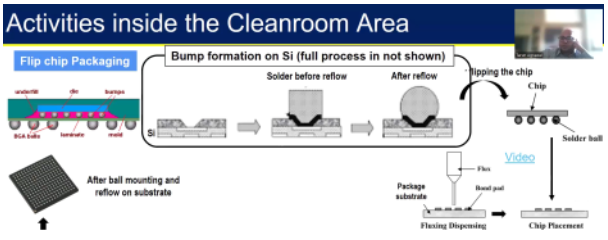




**L4: Flip Chip Assembly - Bump Formation & Underfill**

Pitch for die size balls is lower than the BGA side balls in flip chip.

We start with a diced wafer.
Here, we start with depositing bumps.
After metal & dielectric layers, we deposit solder on the pads & reflow it to form bumps.

Once bumps are deposited, we flip the die.
Here, the substrate already has bond pads to join.
Before placing the die, we deposit solder.



Once bumps are deposited, we flip the die.
Here, the substrate already has bond pads to join.
Before placing the die, we deposit solder.

After placing the die, it is heated & solvent is sprayed to remove excess flux.
Finally, an underfill material is deposited between the die & substrate.

The underfill provides mechanical support to the die & also reduces stress due to CTE (Coefficient of thermal Expansion) difference between the carrier & die.

Once cured, we deposit the moulding compound, engrave markings & balls are mounted

To make chips even smaller, we go for wafer level packaging, where we try to avoid the usage of substrates.

**L5: Wafer Level Packaging & Conclusion**

Here, we use RDL to redistribute connections
RDL layer allows us to route connections, so needs additional steps.

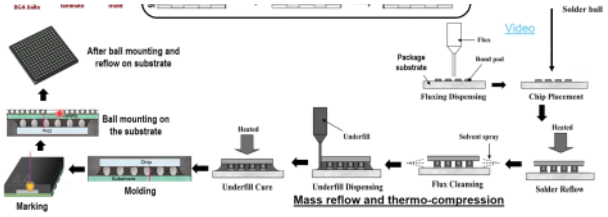
Reconstituted wafer: We place the known good dies over a temporary carrier.
Spacing between the dies is increased to allow for fan out.

So, we place the dies on a temporary wafer with the contact side facing downwards.
We then add the moulding layer & them move on to RDL deposition.

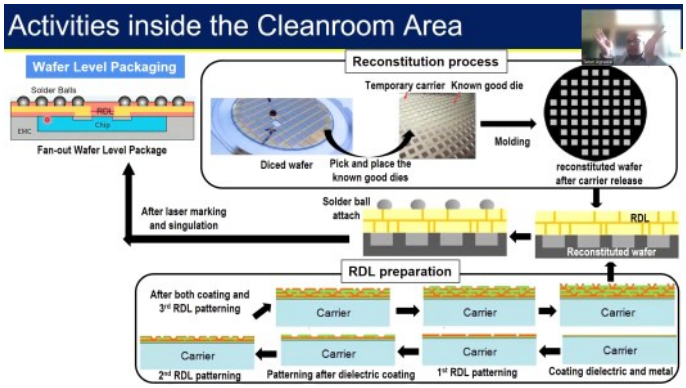
The contact side has a layer of dielectric & metal.
We then etch away the metal layer & fill it with dielectric, followed by a stack of dielectric & metal to get the desired routing pattern, with the last a for solder balls.

We then single out individual ICs.

After clean room procedure:
Once key manufacturing processes are done, we send the ICs to testing area.
Testing carries out extensive analysis of real world performance of the IC & checks for reliability issues.




TLV: Through Laminate Via




Note: Lower the pitch, higher the chances of IC failure.