Module 1: Packaging Evolution: From Basics to 3D Integration

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L1: Introduction To Semiconductor Packaging
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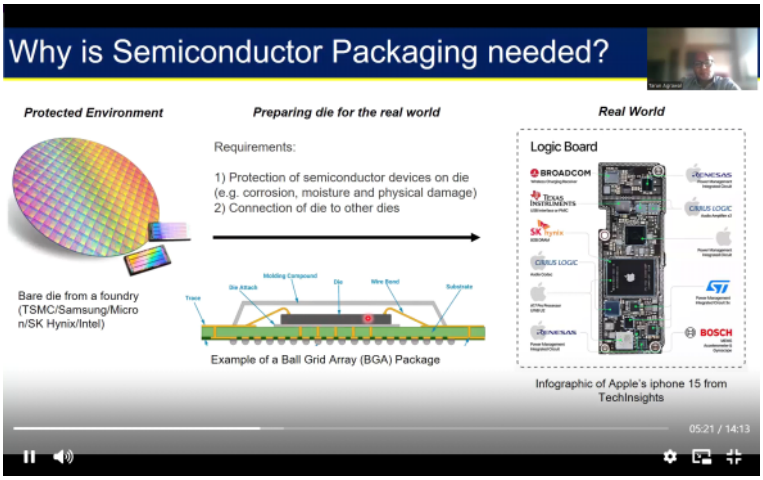
Why Packaging Is Needed?
So, individual chips are cut out from wafers.
They are built in a protected environments.

But when used, these ICs are exposed to the real world.

1. Packaging enables the die to work in the real world (Corrosion, Physical damage, moisture etc.)
2. Allow connection to other dies



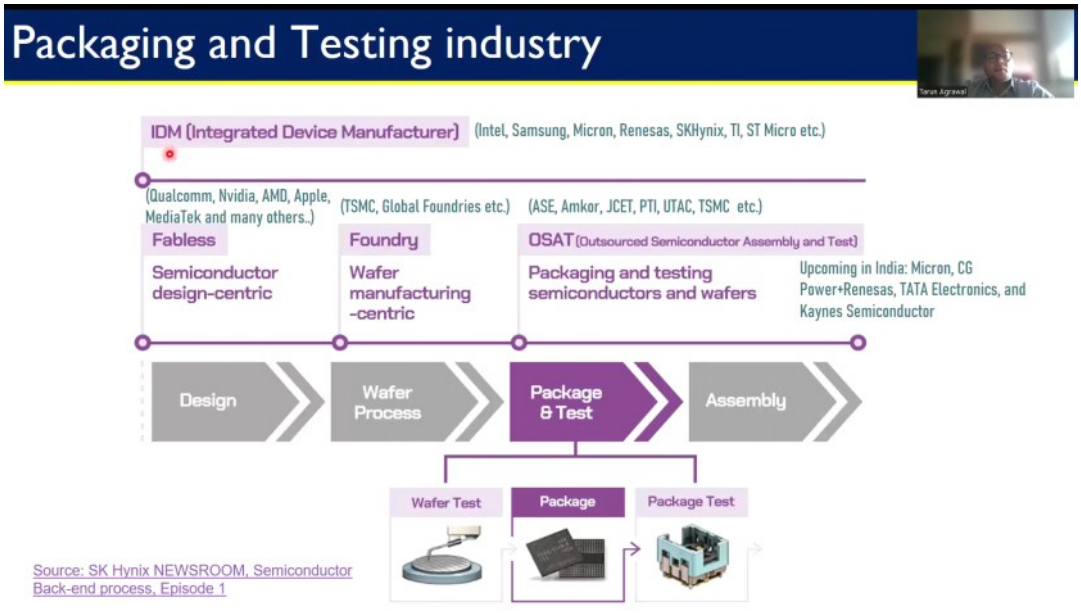
So here, the black outer casing is not the package, but the moulding compound.
The IC is placed within the moulding compound & we use wire bonds to connect it to the substrate.
Wire bond allows us to connect to BGA, which can be used to connect to a system.

So, packaging brings personality to an intelligent chip

Design is the first step in this process, we give designs to a foundry, who manufacture it.
Post manufacturing, we test the wafer, package it & test it in packages & test.
Tested ICs are sent for assembly.

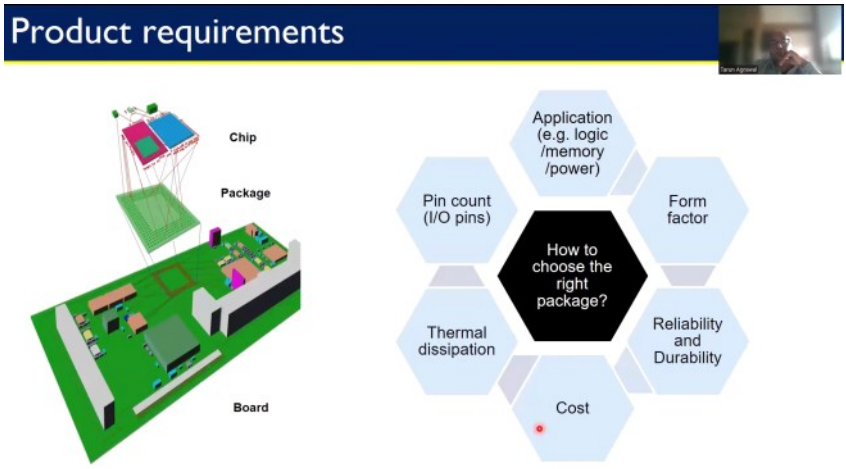
IDMs: Design, Foundry & Packaging: End to End (Intel, Samsung, Micron, SKHynix, TI, ST)
But for fabless companies:

1. Fabless Design Centric Orgs (Qualcomm, nVidia, AMD, Apple)
2. Foundry: Wafer Mfg (TSMC, Global Foundries)
3. OSAT (Outsourced Semiconductor Assembly & Test): Packaging & Testing of all wafers they receive (ASE, Amkor, JCET, PTI, UTAC, TSMC etc.)



Upcoming Units in India: Micron, CG Powers + Renesas, Tata Electronics, Kaynes Semiconductor

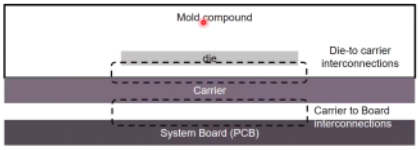
L2: Understanding Package Requirements & Foundational Package Types



Silicon Development Lifecycle:
1. Product Requirements
2. Design
3. Manufacturing
4. Testing
5. Debugging
6. In-field operation

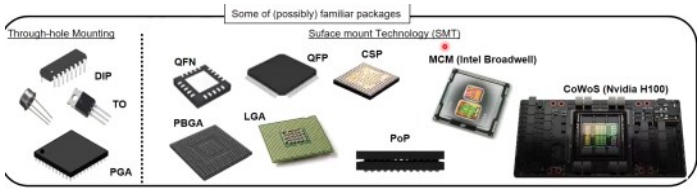
Course Structure:
1. Intro
2. Package Manufacturing
3. Testing: Reliability & QA
4. Design w.r.t Electrical, Thermal & Mechanical Constraints
5. Future Trends

How do we choose the right package: It primarily depends on the application
Other important factors:
1. Bandwidth: Should be able to support required connections / IO.
2. Thermal Dissipation: Heat must be dissipated away from IC, in addition to operating temps.
3. Form Factors: How large can the package be
4. Reliability & Durability: Based on operating environments
5. Cost: Most important factor: Must optimize



Typical Package Structure:
So, 4 basic components:
1. Die: The actual silicon chip
2. Carrier: The layer over which the die is placed. Can be substrate or other materials
3. System Boards: The PCB over which the carrier is placed.
4. Moulding: External layer which protects the die from environmental factors.

Need to establish connections from die to carrier & carrier to system board.



Two Families of Packages:
1. Through Hole Packages: DIP, SIP, PGA. Since have pins: Have larger size
2. Surface Mount Technology: Allows us to optimally use the available area of the package
   Use pads below or around the IC.

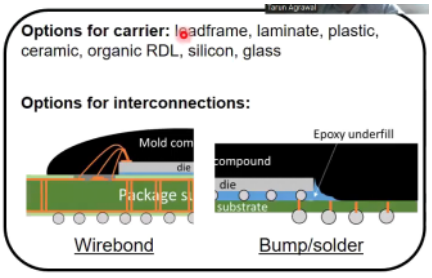
QFP & QFN: Quad flat packages. N - No lead, P - Pins
BGA Class: Ball grid Array. P - Plastic. Use solder balls
LGA: Land Grid Array
CSP: Chip Scale Package: Similar to BGA, but package size is close to die size.

L3: Evolving Package Architecture - Single Chip to Multi-Chip Modules

So most packages covered till now only have a single die on package.
This changed with the introduction of multi-die packages
They are called: MCM : Multichip Packages.
E.g.: Intel Broadwell

PoP: Package-On-Package: Tack & pass interconnect through the lower package.

CoWoS: Advanced packaging seen in Nvidia H100



Options for Carriers:
Started with lead frames : Metallic package backframes with epoxy shells.
Laminates: Stacked layers of material glued together
Modern Materials: Plastic, Ceramics, Organic RDL, Silicon & Glass

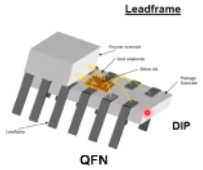
Ideally, choice of carrier is dictated by operating environment

2 Modes of interconnects:
1. Wire Bonding: Use wires to connect die points to package
2. Bumps: Use Solder balls

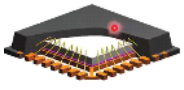
Anatomy of Packages:

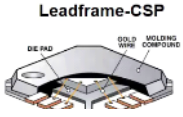
A. Leadframe

1. Lead frame:
   Here, we have a metal support frame on which the die is glued to.
   We use wire bonds to connect die to pins, which may be stamped from the same sheet.
   We apply moulding compound on either sides & bend the leads



2. QFN: Quad Flat No Lead
   Bigger package with connections on all four sides.
   Similar to lead frame, we have a metallic frame & we use a die-attach to hold the die.
   We connect the wires to pads & encase the moulding
   May add thermal pads too.





3. Leadframe CSP:
   Small die size packages

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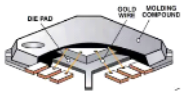
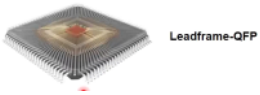
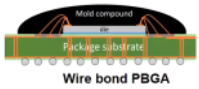


4. Leadframe-QFP: Quad Flat Package with Pins
   Die is placed on a lead frame, but we have physical pins

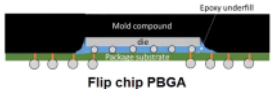


B. Laminate:

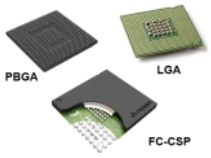
1. Wire Bond PBGA (Plastic Ball Grid Array)
   Die is placed on a laminate, we wire bond connections to the ball grid array & add mould compound on top



2. Flip Chip PBGA:
   Here, we flipped the die, now bumps will connect to solder balls of the substrate.
   We also have an epoxy underfill

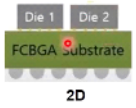


3. Flip Chip CSP: Same as flip chip, but smaller footprint
4. LGA: Land grid Array: Instead of bumps, we use pins & an array of contacts

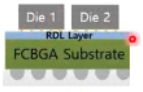


C. Advanced Package Substrates

1. 2D Integration:
   On the same substrate (Maybe FCBGA), we connect two dies.
   Better than having two substrates, but for communication between the dies, need to pass signal from die to BGA & then to the other die

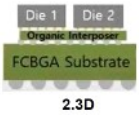


2. 2.1D Integration:
   Eliminates the longer connections by adding a redistribution layer between die & substrate.
   The RDL has internal connections which offer a shorter pathway.

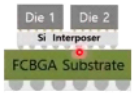


L4: Interposer Redistribution Layer & 2.5D/3D Packaging Approaches

3. 2.3D Integration:
   Here, we place an organic interposer between the FC & FCBGA substrate.
   Intermediate layers allow us to fan out connections when connection density increases.

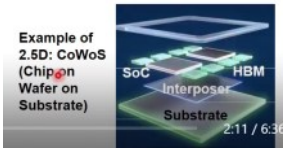


4. 2.5D Integration:
   Here, we need to fan out high density connections & offer minimal latency.
   To achieve this, we add a layer of active silicon as the interposer.

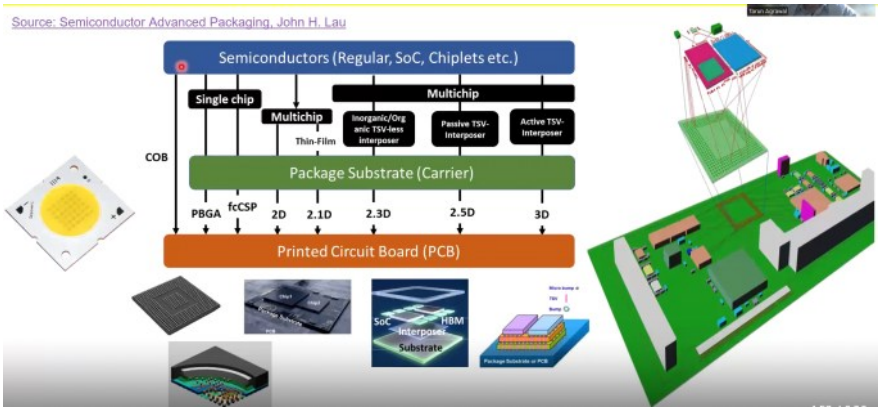


Note:
Pitch Bump: The spacing between adjacent bumps in BGA.

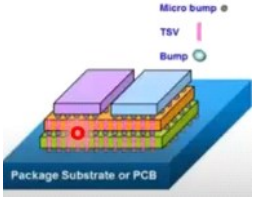
Why not called 3D?: As dies are still not stacked



SoC: System on Chip
HBM: High Bandwidth Memory



3D Integration:
Dies stacked on dies with connections going across them



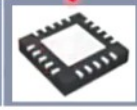
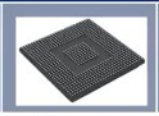
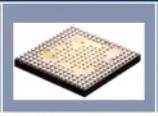
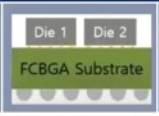
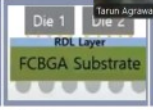
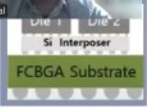
When integrating a die into a design, we deal with 3 levels:

1. Die Level
2. Substrate Level
3. System PCB Level

Why not place a chip directly on PCB: Can be done: Called CoB : Chip On Board

L-5: Comparative Analysis & Selecting The Right Package Solution

Comparison

IC package Type								
Pros	Low cost, easy to manually assemble, durable	Compact, good thermal performance, lightweight	Higher pin density, ease of inspection, ease of solderability	Higher pin count, good electrical and thermal performance	Reduced package size, higher electrical performance at lower cost	Higher level of integration, better performance, and power efficiency	Higher density I/O and routing at lower cost	high I/O throughput, hetero-geneous integration, lower latency
Cons	Bigger size, low pin count, incompatible with automated assembly	Testing accessibility, Reparability, smaller I/O pins than QFP	Pins susceptible to damage, difficult to repair bent pins	Difficult to inspect and rework, limited shelf life, costlier than QFN	Limited I/O pins, reliability issues (solder joint and warpage)	Longer die-to-die connections	Reliability issues in polymer RDL, lower I/O density than 2.5D	Costlier than 2.1D, reliability concerns
Common Application	Consumer electronics, industrial applications, legacy systems	Smartphone, tablets, automotive, telecommunications	Micro-controllers and micro-processors, ASICs	High performance ICs	Smartphones, IoT, wearable devices	Data centre chips, RF wireless modules, Space avionics	High performance computing segments	Data centre GPU for AI

1. DIP : Durable & easy to assemble, but is larger in size & accommodates a lower pin count. Isn't compatible with automated assembly. Used in legacy systems.
2. QFN: Compact & better thermal performance. Lower degree of testability & relative to QFN has lower pin count.
3. QFP: Higher density, easy to test & solder. But is mechanically susceptible to damage.
4. PBGA: Even higher IO count as using entire bottom surface & better thermal performance. But difficult to inspect & more expensive.
5. CSP: Reduced package size, but requires more connections, peripherals & are more prone to mechanical failure.
6. 2D: Higher level of integration, improved efficiency & improved performance. But longer die-to-die connection.
7. 2.1D: Has benefits of 2D, but has RDL to improve communication speed. Stacking materials impacts reliability.
8. 2.5D: Adds active interposer to connect dies. Higher IO count & lower latency. Since additional silicon is added, is more expensive & limitations on die size.

Note: Must understand the manufacturing process or use case of IC to decide on packaging.