**REPORT**

**Name :Balam Ruchith Balaji**

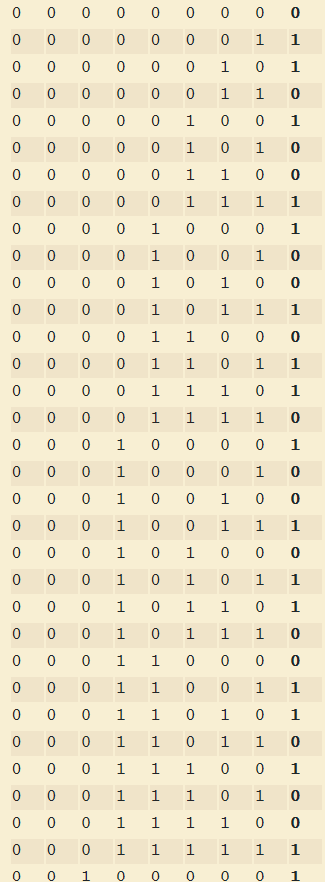
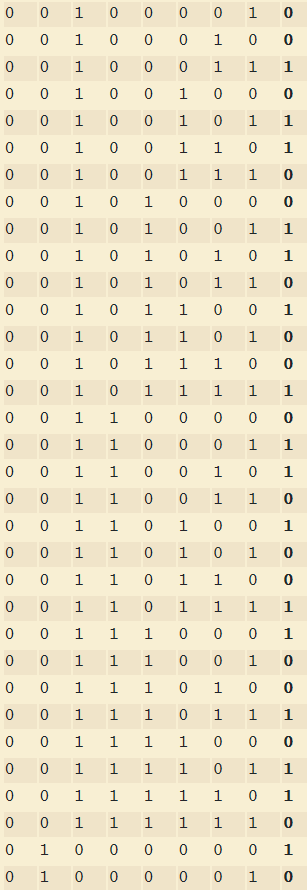
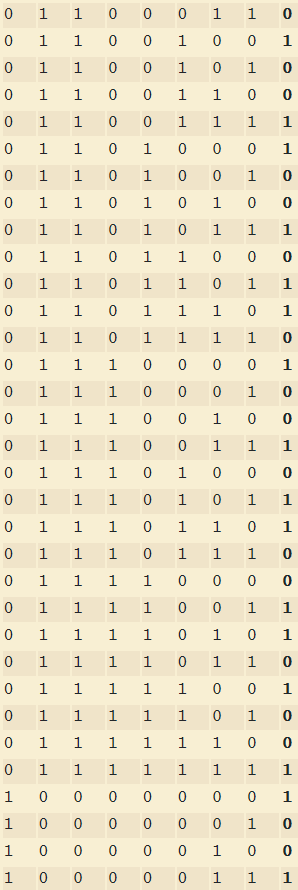
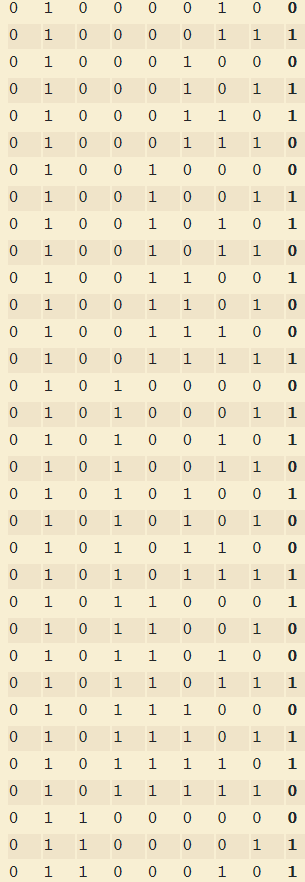
**Reg.no :Bl.EN.U4AIE21017**

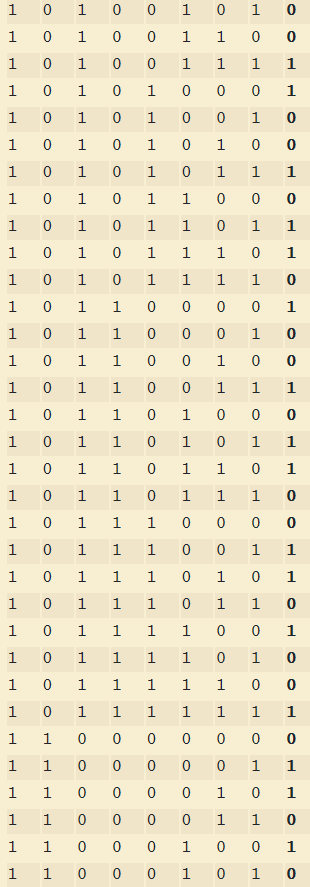
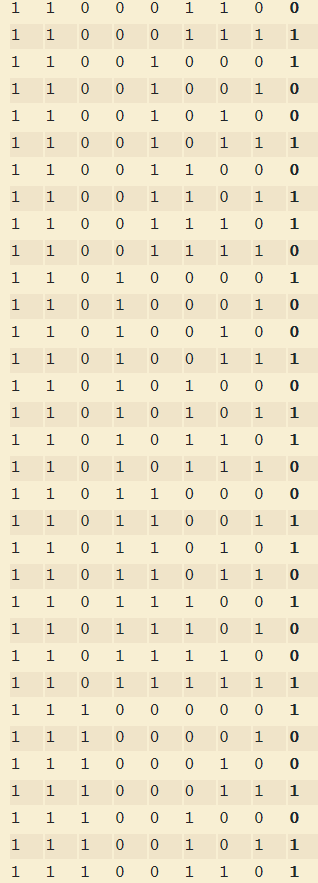
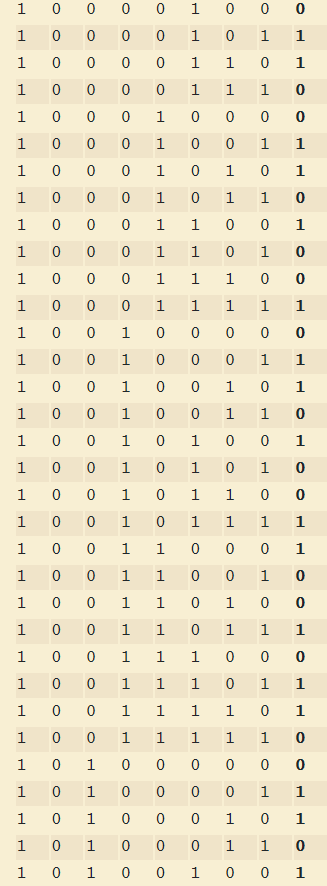
**Project :03**

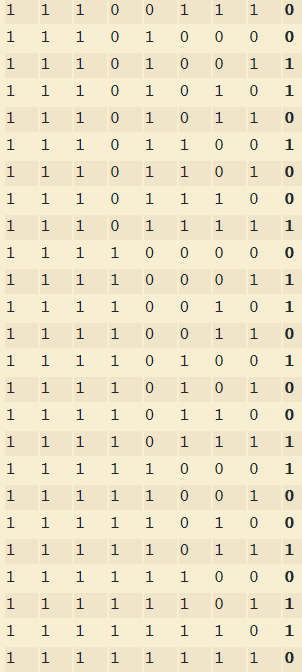
**Team No:E3**

**Problem: 01**

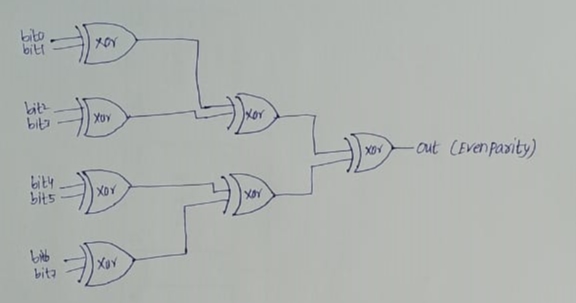
Design and implement a combinational circuit to compute ‘even parity’ of a 8-bit number.

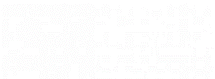
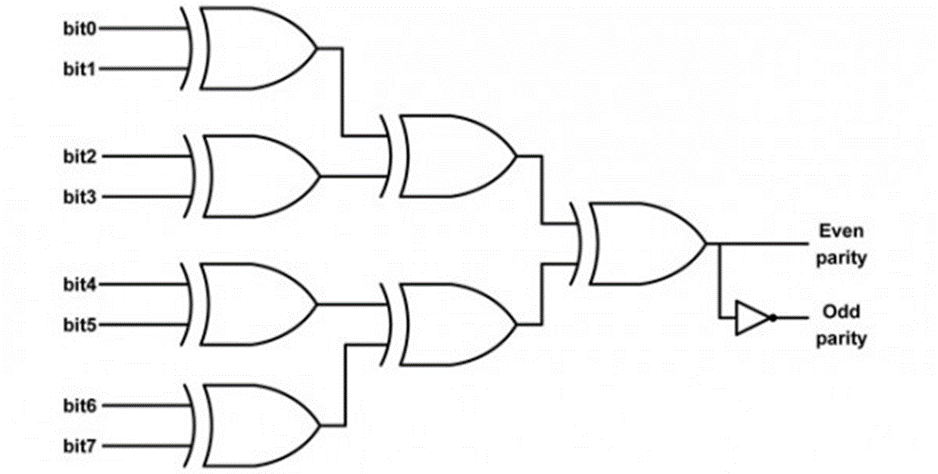
**Truth table: (8bits and output** {bit0, bit1, bit2, bit3, bit4, bit5, bit6, bit7})

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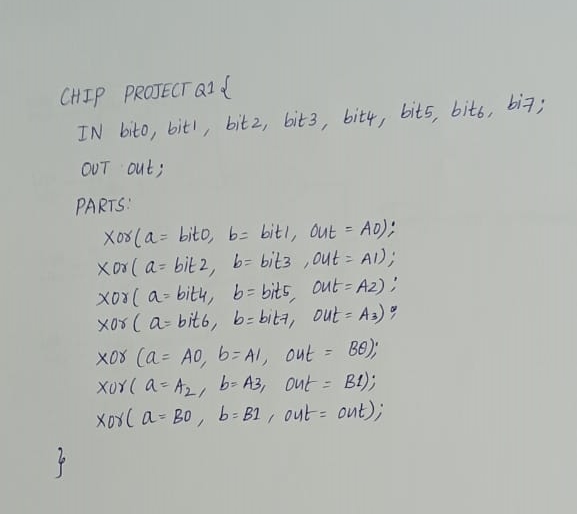
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**DESIGN:**





CODE:(Handwritten)



CODE:(NOTEPAD)

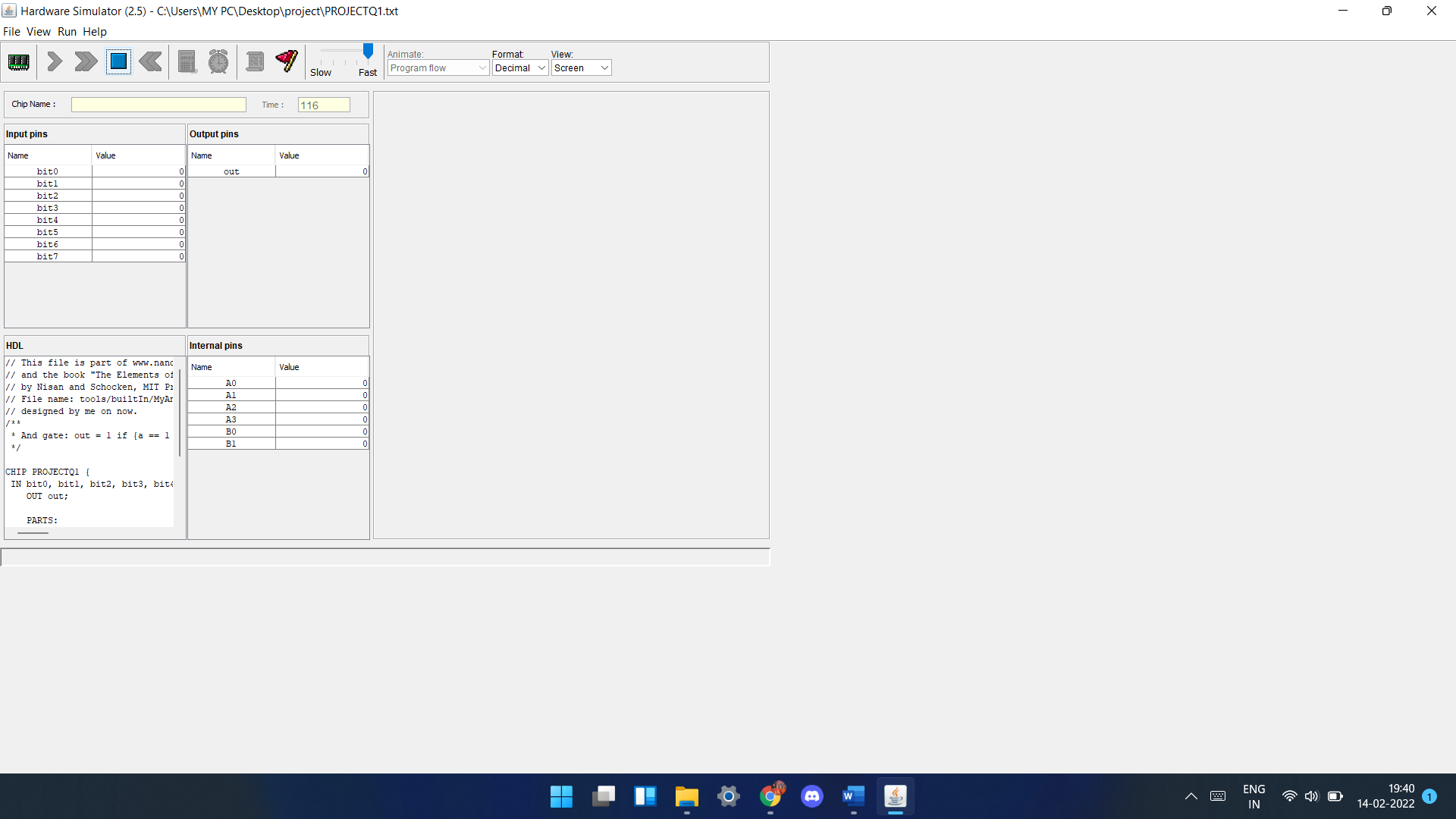


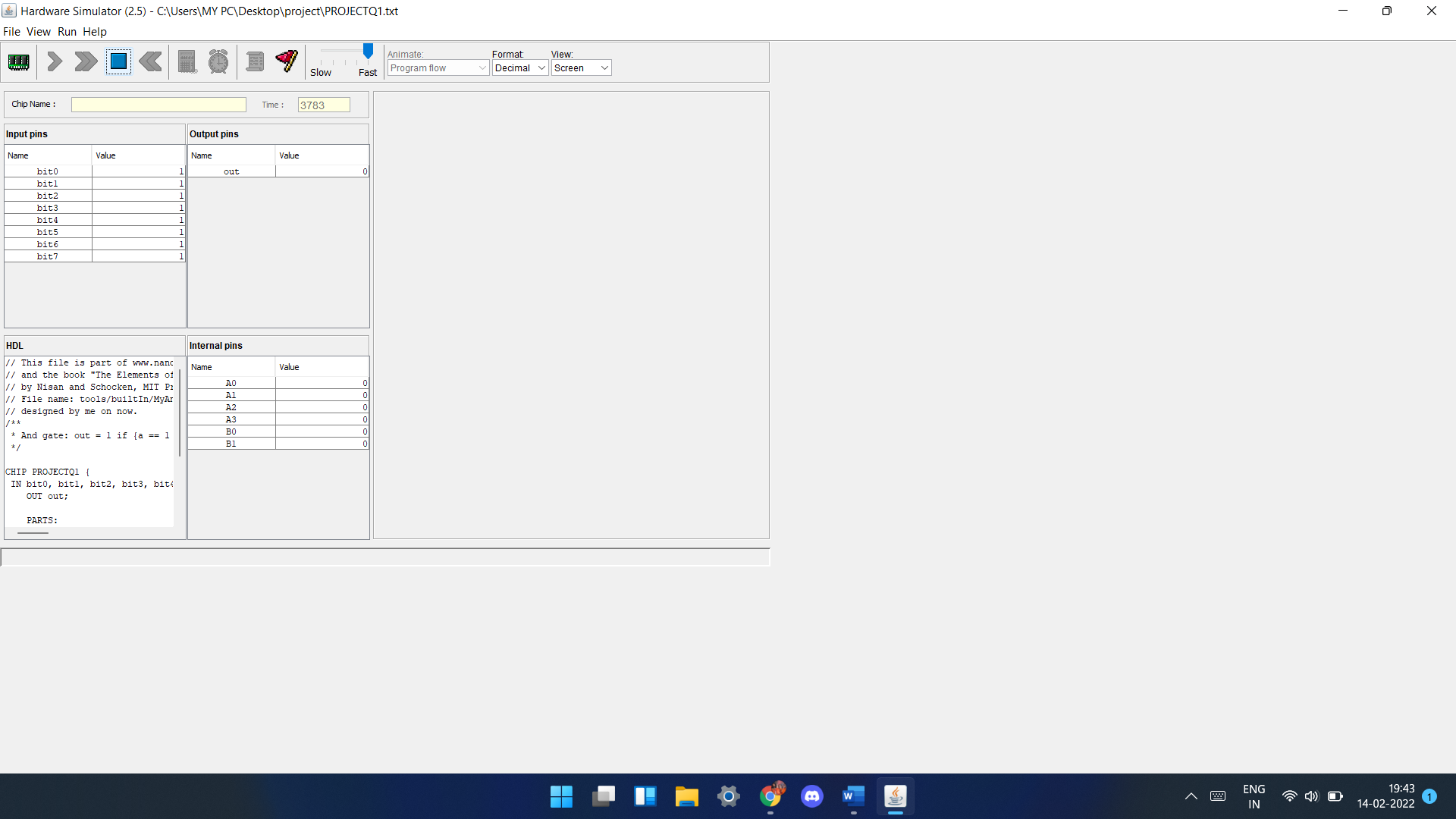
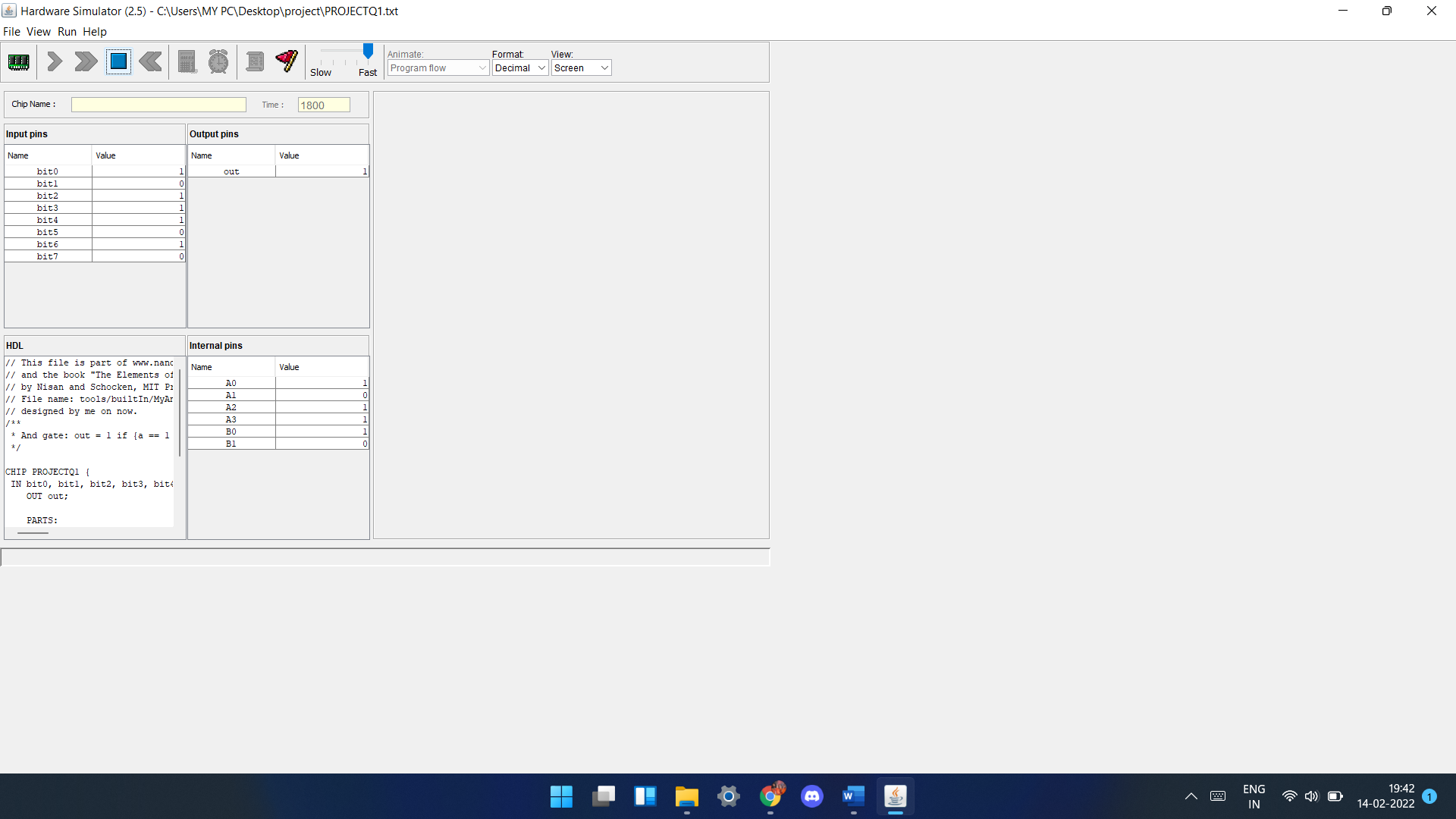
TESTCASES:

1) bit0=0,bit1=0,bit2=0,bit3=0,bit4=0,bit5=0,bit6=0,bit7=0

2) bit0=1,bit1=0,bit2=1,bit3=1,bit4=1,bit5=0,bit6=1,bit7=0

3) bit0=1,bit1=1,bit2=1,bit3=1,bit4=1,bit5=1,bit6=1,bit7=1





**Problem: 02**

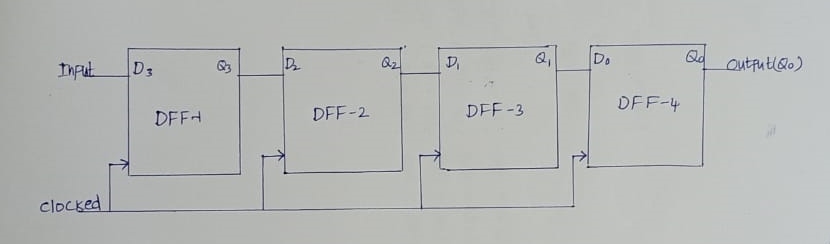
Explain a 4-bit shift register that performs right shifting. Implement it using D Flip Flop.

**TRUTH TABLE**

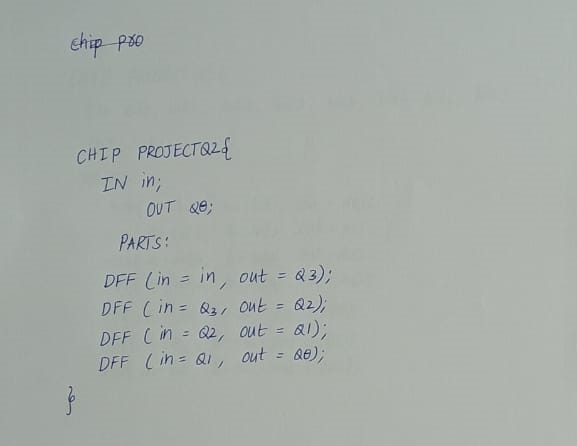
For example take a 4 bit number: 1101

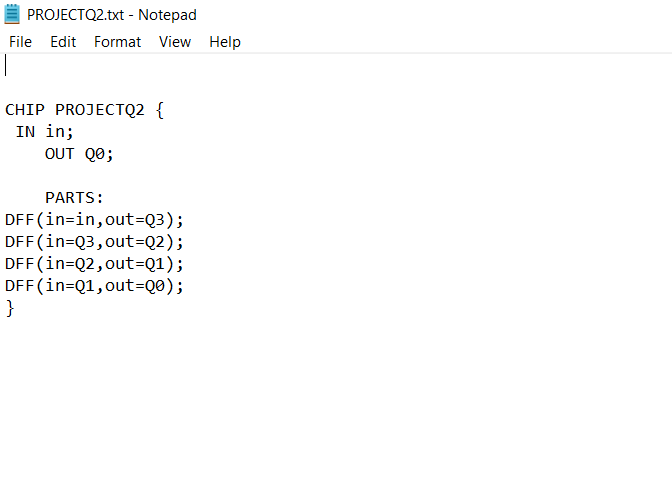
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| CLOCK | **D3**  **(input)** | **D2** | **D1** | **D0** | **Q3** | **Q2** | **Q1** | **Q0**  **(out)** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 3 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 4 | 1 | 1 | 0 | **1** | 1 | 1 | 0 | **1** |

DESIGN:



CODE:(Handwritten)



CODE:(NOTEPAD)

TESTCASES:

Take a 4bit number 1101

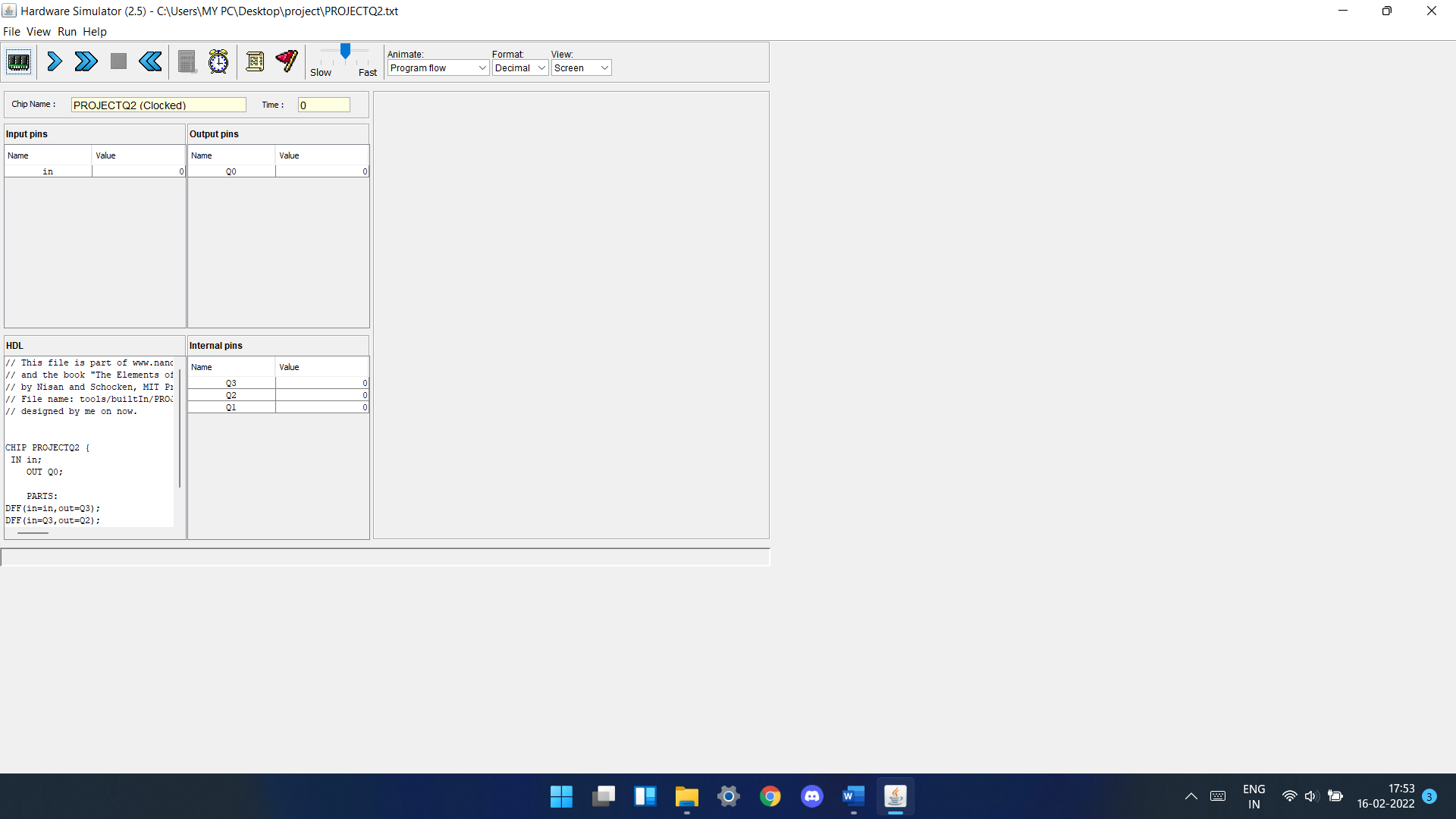
0th second (ALL zeros)

1st second (in=1)

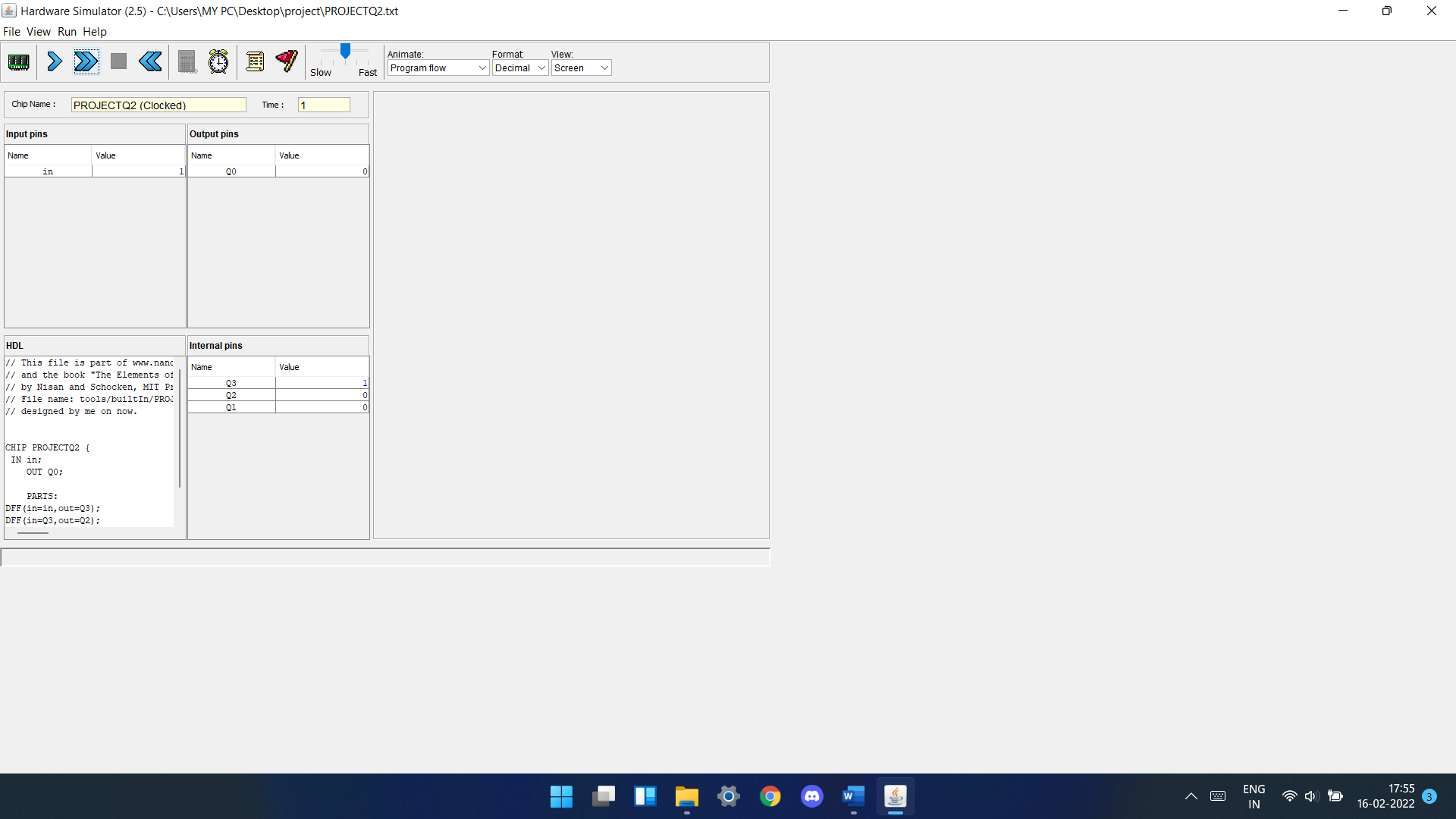
2nd second (in=0)

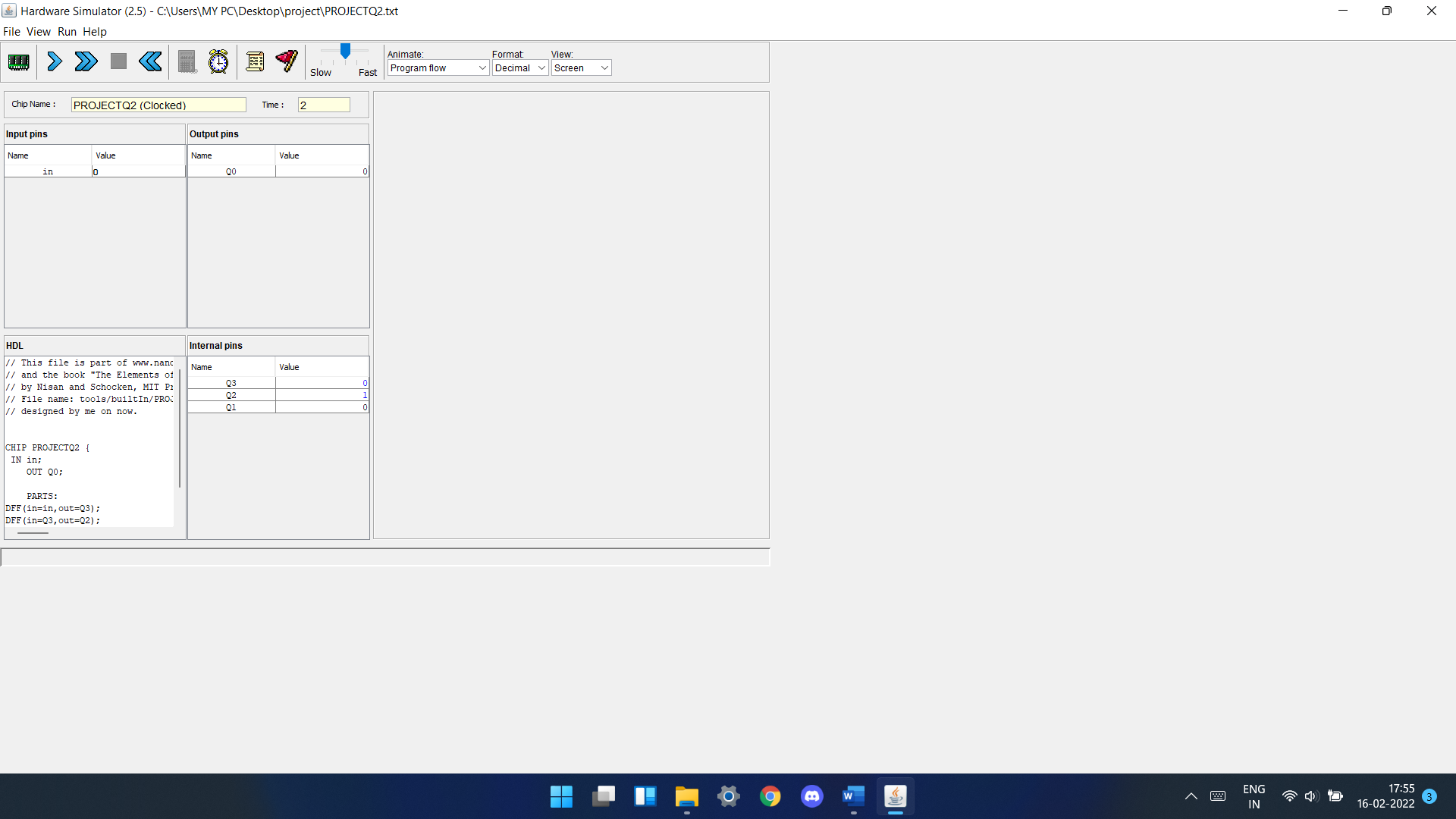
3rd second (in=1)

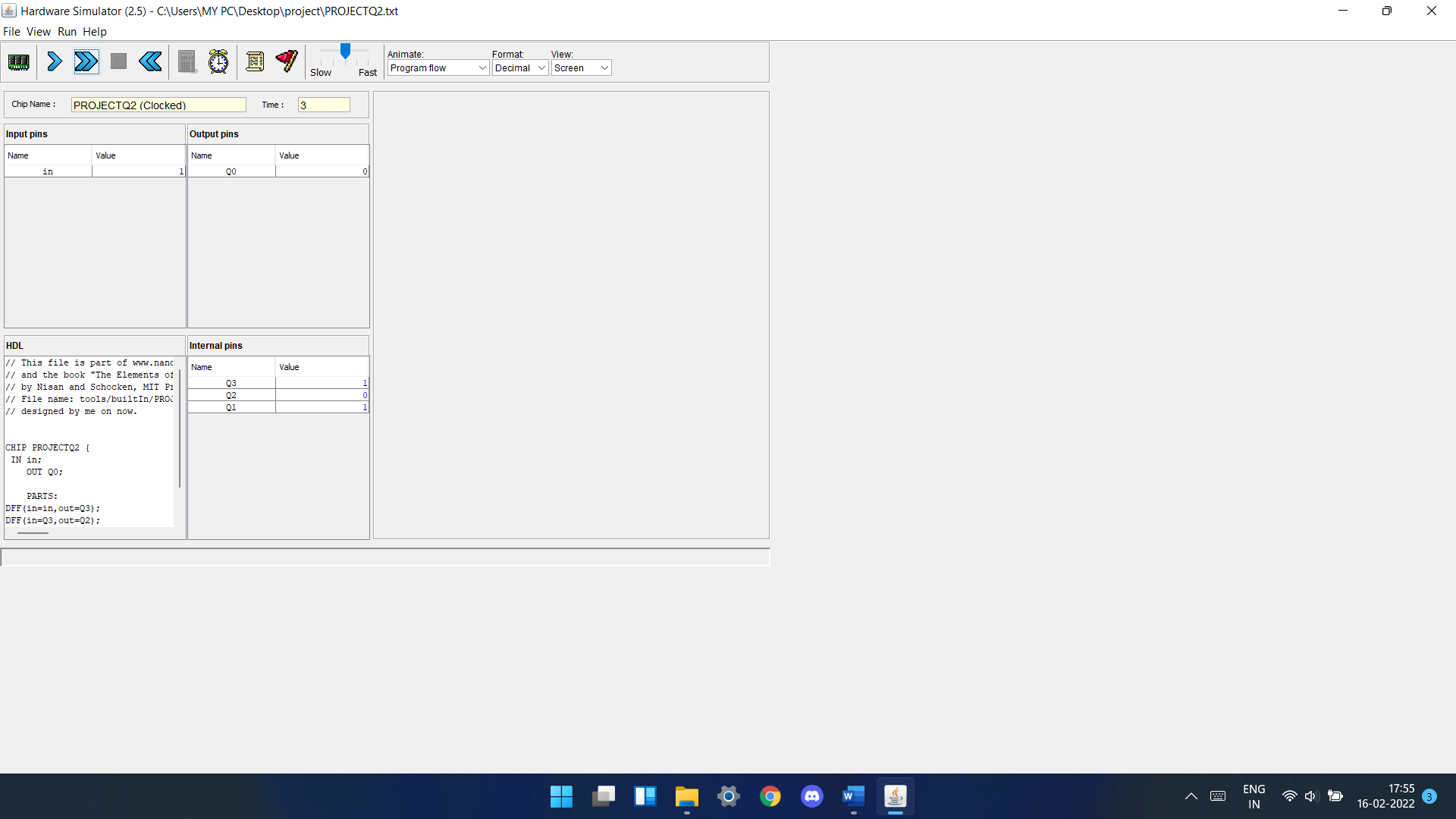
4th second (in=1)

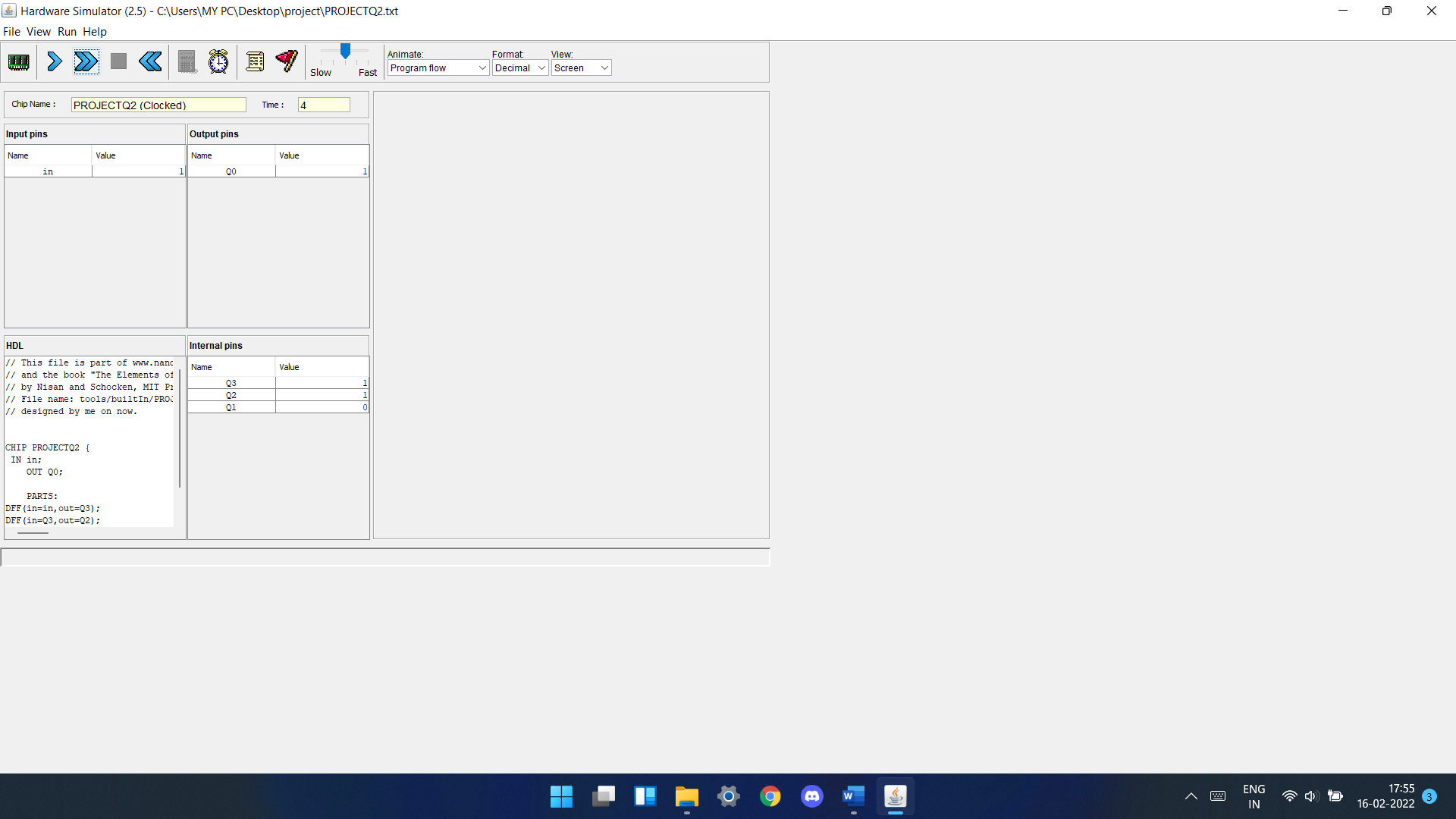
**0th second (in=0):**

**1st second (in=1):**

** 2ndsecond (in=0):**

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**3rd second (in=1):**

**4th second (in=1):**