



Full Length Article

Interfacial chemical vapor deposition of wrinkle-free bilayer graphene on dielectric substrates

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ABSTRACT

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Wrinkles invariably form during graphene growth and post-growth transfer, limiting graphene films' large-scale uniformity for electronic applications. We report a transfer-free synthesis route for highly-uniform bilayer graphene directly on dielectric substrates— SiO_2 , sapphire, and MgO —by interfacial carbon precipitation. Ultrathin Pd leaves having a thickness of 150 nm and grain size up to 100 μm are laminated onto the target dielectric substrate, followed by annealing and press rolling to form a uniform Pd-substrate interface. Rapid heating in a hydrocarbon atmosphere causes carbon diffusion through the Pd layer; upon cooling, precipitation of carbon results in graphene growth at the Pd-substrate interface. The interface-grown graphene remains on the substrate after removing the Pd layer by wet etching. It exhibits sub-nm surface roughness without wrinkles or folds. Over 94 % of the interface-grown area is dominated by bilayer graphene with low twist angles. In addition, the interface-grown graphene is nearly strain-free. From Raman characterization, an average long-range scattering mobility of $\sim 1000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was estimated for as-grown bilayer graphene on sapphire (0001) at room temperature. This technique shows promise to achieve device scale, ultra-uniform graphene fabrication directly on dielectric substrates, with the potential to accelerate graphene applications in electronics, photonics, and sensing.

1. Introduction

Graphene has drawn scientific interest due to its mechanical strength and resilience, high thermal conductivity, and high carrier mobility [1–4]. In particular, bilayer graphene (BLG) is sought-after for electronic applications because it exhibits a tunable bandgap and remarkable conductive properties due to its particular stacking configuration or twist angle [5–9]. Chemical vapor deposition (CVD) synthesis with metal substrates can fabricate large-scale, high-quality graphene films controllably and cost-effectively. Nowadays, wafer-sized high-quality single layer graphene (SLG), BLG, and van der Waals heterostructure films can be produced by CVD [10–13]. However, graphene must be transferred from the metal substrates used for synthesis to device-relevant dielectric substrates. The transfer process typically includes adhesion of a polymer transfer medium to the metal, delamination of the polymer-supported graphene film from the metal, lamination onto a destination substrate, and removal of the polymer supporting layer [14].

Such a transfer process invariably degrades as-grown graphene. For example, impurities like water or oxygen molecules can be trapped between the graphene and target substrates and lead to extrinsic doping or straining of the graphene [15], while polymer supporting layers such as polymethyl methacrylate (PMMA), polylactic acid (PLA), and thermal release tape leave residues on the graphene and can reduce its carrier mobility [16].

Moreover, wrinkles in graphene are a critical defect that persists throughout the CVD synthesis and transfer steps. From the beginning of graphene formation on the metal, thermal expansion mismatch between the graphene and the metal introduce interfacial compressive stress, causing wrinkles or folds [17]. In addition, it is common for the metal surface undergoes complicated reconstruction after graphene growth due to the strong graphene-metal interaction and surface energy minimization [18,19]. This results in high surface roughness, including hierarchical steps and terraces ranging from 1 nm to a few hundred nm in height. Graphene covers these steps almost conformally [20]. Coating a

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transfer medium on top of the graphene templates the abovementioned graphene wrinkles, folds, and surface steps, and therefore the defects are carried through the process. Research toward eliminating graphene wrinkling has involved, for instance, weakening the graphene-metal interaction to release the interfacial stress [12], and adopting an ultra-compliant transfer medium (e.g., Paraffin wax) or volatile solvent with low surface tension (e.g., heptane) to flatten the floating polymer/graphene film [21,22]. However, graphene wrinkling has not been eliminated in previous reports. It is still challenging to achieve conformal contact between the transferred film and the destination substrate.

Transfer-free synthesis of graphene on insulating substrates is a potential route to circumvent the challenges of graphene wrinkling on metal substrates and impurities introduced by polymer-based transfer. Transfer-free formation of BLG and few-layer graphene (FLG) on SiO₂ has been achieved by interfacial carbon precipitation; for instance, deposition of a catalytic metal film on SiO₂, followed by carbon dissolution at high temperature from hydrocarbon gases or solid carbon sources, results in graphene at both the top metal surface and at the metal-SiO₂ interface upon cooling [23–25]. However, in previous studies, the deposited thin metal film had nanoscale grain structures and high grain boundary density, making it challenging to achieve uniform carbon diffusion through the lattice and grain boundaries at the metal-SiO₂ interface. Therefore, the uniformity of the interface-grown graphene in terms of thickness, surface roughness, and quality has yet to be comparable to that of conventional CVD on metal foils.

We report the direct fabrication of highly uniform BLG films on dielectric substrates using interfacial CVD synthesis with commercially-obtained ultrathin Pd foils. Pd has higher carbon solubility than Ni at high temperatures, thereby achieving faster interfacial carbon precipitation. More importantly, despite Pd foils' small thickness of 100–150 nm, they have large grains with a typical width of 20–100 μm (Fig. S1). As a result, we have achieved uniform carbon precipitation at the Pd-substrate interface and directly fabricated wrinkle-free BLG with a sub-nm surface roughness on substrates such as SiO₂, sapphire, and quartz. Further, we studied the strain-doping relations for graphene grown at the Pd-substrate interface and on the top surface of the Pd foil and found that BLG at the Pd-substrate interface is nearly strain-free, while graphene grown on the Pd surface has compressive strains ranging from 0.1 to 0.5 %. This indicates that graphene undergoes different straining paths on the surface versus at the interface during CVD and that, unlike the free (top) surface of Pd forming steps and terraces, the Pd-substrate interface remains flat after the CVD process. In

addition, as-grown BLG films on dielectric substrates are heavily doped with about $15 \times 10^{12} \text{ cm}^{-2}$ charge density. This could be caused by intimate contact and stronger adhesion to the substrates than that of the transferred graphene films.

2. Experimental details

2.1. The Pd-substrate interface preparation

A 4-inch silicon wafer with a 300 nm thermal oxide layer (WaferPro) was first cleaned following the standard RCA clean steps (SC-1: 5 parts DI water, 1 part 27 % ammonium hydroxide, and 1 part 30 % hydrogen peroxide solution cleaning for 15 min at 70 °C; rinse with DI water; SC-2: 6 parts DI water, 1 part 27 % hydrogen chloride, and 1 part 30 % hydrogen peroxide solution cleaning for 10 min at 70 °C; rinse with DI water and blow dry with nitrogen). Similar cleaning steps were used for a 4-inch quartz wafer (WaferPro), 2-inch sapphire wafer (0001) (University Wafer), and 5 mm × 5 mm × 0.5 mm MgO (100) substrate (MTI Corp). Freestanding Pd leaves (Wehrung & Billmeier Gold Leaf) having a thickness of ~150 nm were manually laminated on the pre-cleaned substrates, as illustrated in Fig. 1a. The Pd leaf/substrate stacks were annealed in a cold wall reactor in He (400 sccm) at ~2.2 Torr at 600 °C for 1 h (Fig. 1b). The annealing process can reduce the dislocation density in the Pd, promote the contact between the Pd and SiO₂, and relieve the residual stress from the lamination process. The interface uniformity between the Pd and SiO₂ can be further improved by press rolling with a Φ5 mm quartz rod after annealing (Fig. 1c). We repeated the annealing and press rolling sequence four times until wrinkles in the Pd were flattened (Fig. S1a), and the Pd formed an intimate interface with SiO₂, as shown in Fig. 1d, e.

2.2. Interfacial CVD synthesis method

Interfacial CVD growth was performed in a cold-wall reactor using a quartz tube (Φ1 inch) and a highly-doped silicon heater. An infrared sensor and a PID controller were used for silicon heater temperature control [26]. Prior to growth, the residual carbon deposits around the silicon heater were cleaned by heating to 850 °C for 30 min with dry air flowing. After the reactor cooled down, the Pd/substrate stacks were placed on the silicon heater. The growth process was run at low pressure and with recipes listed in Table S1. For example, the furnace was first evacuated to 1.8 mTorr and purged with the He gas. The substrate was

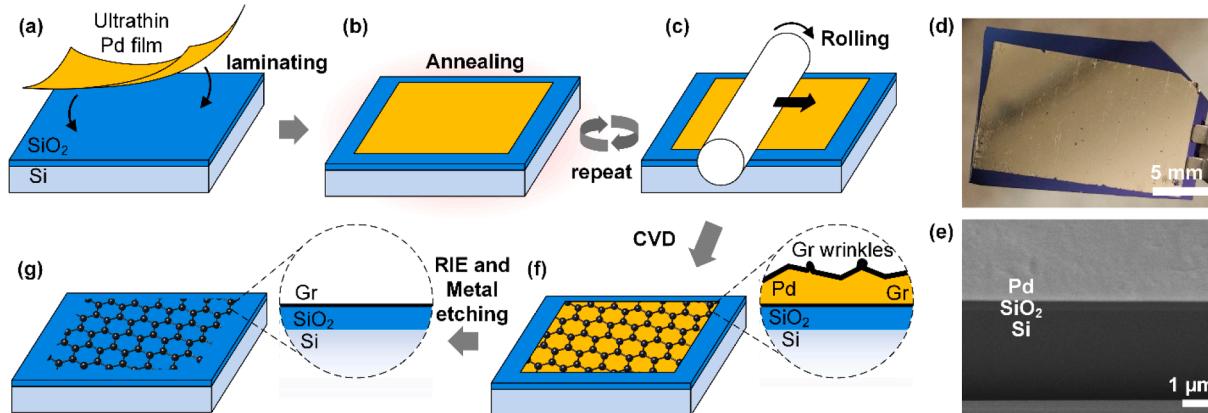


Fig. 1. Interfacial CVD synthesis of graphene on dielectric substrates. (a) Lamination of a freestanding ultrathin (thickness of 150 nm) Pd foil on SiO₂ (300 nm)/Si substrate. (b) Annealing of the Pd/SiO₂/Si stack in a cold-wall reactor. (c) Repeated press rolling of the Pd using a quartz roller to promote conformity of the Pd on SiO₂ surface. (d) Photo of a Pd/SiO₂/Si stack ready for CVD synthesis; Pd wrinkles and folds are flattened after repeated annealing and press rolling. (e) Scanning Electron Microscopy (SEM) image (52° tilted) of the Pd/SiO₂/Si stack cross-section. (f) CVD growth of graphene on the Pd surface and at the Pd-SiO₂ interface in a cold-wall reactor (inset illustrates the Pd surface reconstruction, conformal graphene layer following the Pd surface morphology, and graphene wrinkle formation on the Pd surface). (g) Removing the top graphene layers and the Pd film using RIE and wet etching leaves interface-grown graphene on SiO₂/Si substrate (inset illustrates the flat graphene film on SiO₂ surface).

then heated to 800 °C within 2 min in 400 sccm He (2.23 Torr). After the temperature stabilized, the carbon precursor, 3–5 sccm C₂H₄ was added to the furnace for 30 s (total pressure 2.27 Torr) at 800 °C, followed by cooling with the same C₂H₄ and He gas flowing until the substrate temperature dropped below 200 °C (approximate cooling rate: -13.1 °C s⁻¹). Fig. S2 shows a measured substrate temperature profile during CVD synthesis. This CVD process formed graphene on the Pd top surface (Fig. S1c, d) and at the Pd-SiO₂ interface, as illustrated in Fig. 1f. After growth, graphene films on the upper surface of Pd were removed using a plasma ash (Diener Femto) with 1:2 Ar-O₂ gas flowing. The plasma-etched Pd/substrate stacks were submerged in a commercial Pd etchant solution (Transene) for 10–15 min until the Pd layer was entirely removed (Fig. 1g). The substrates were then rinsed with DI water and gently blown dry with nitrogen. After that, the interface-grown graphene film remained directly on SiO₂ surface.

The Pd leaf has high solid carbon solubility at elevated temperatures. Therefore, carbon radicals from the hydrocarbon precursor decomposition diffuse into the bulk Pd at the CVD synthesis temperature. Upon cooling, carbon segregates towards both sides of the Pd layer and forms graphene. Therefore, the kinetics of carbon diffusion and precipitation are essential to controlling interfacial CVD synthesis of graphene. Commercially-available metal leaves, typically used for gilding [27], have sub-micron thickness and macroscopic grain structures and are therefore attractive for uniform carbon diffusion and precipitation compared to nanocrystalline thin films made by E-beam evaporation or sputtering [28]. It is essential to control the carbon decomposition (C₂H₄) on the Pd surface and the diffusion of carbon through the Pd towards the Pd-SiO₂ interface. The concentration ratio of carbon on the Pd surface (c_{surf}) and that at the Pd-SiO₂ interface (c_{int}) can be expressed as $c_{surf}/c_{int} \sim erfc(h/4Dt)^{1/2}$ according to Fick's diffusion law, where h is the Pd thickness, D is the carbon diffusion coefficient, and t is the growth

time (carbon exposure time at synthesis temperature). Notably, the carbon solubility of the Pd is about 150 times higher than that of the Cu, and D is up to $7.5 \times 10^{-8} \text{ cm}^2 \text{ s}^{-1}$ at ~1000 °C [29]. For $h = 150 \text{ nm}$, c_{int}/c_{surf} can be above 0.9996 within 1 s, which implies that the carbon concentration in the Pd can be readily controlled by the gas-phase C₂H₄ concentration during a short exposure time. The short exposure time also avoids degradation of the Pd by solid-state dewetting [28]. Upon cooling, carbon precipitation forms graphene on both Pd surfaces, as illustrated in Fig. 1f. CVD-grown graphene usually shows strong interaction with underlying metal catalysts [30,31]. This can be reflected by the metal catalyst surface reconstruction [18] or step bunching [19] which significantly increases the surface roughness of the metal, while as-grown graphene is conformal to the rough surface. Notably, the Pd-SiO₂ interface remains highly uniform during the whole process due to the constraint provided by SiO₂ and the intimate interface established by the annealing-rolling cycles.

2.3. Materials characterization

The morphology and microscope structures of the Pd-substrate interface were studied using a SEM (Zeiss Merlin High-resolution SEM), Focus Ion Beam milling system (FEI Helios Nanolab 600 FIB), and a high-resolution TEM (FEI Tecnai Multipurpose Digital TEM working at 120 kV). Raman spectra were collected using a Renishaw Invia Reflex Micro Raman microscope with a 532 nm laser. The morphologies of as-grown BLG were studied using a Park Systems AFM (Park XE7) with Nanosensors™ PPP-NCHR-10 probes.

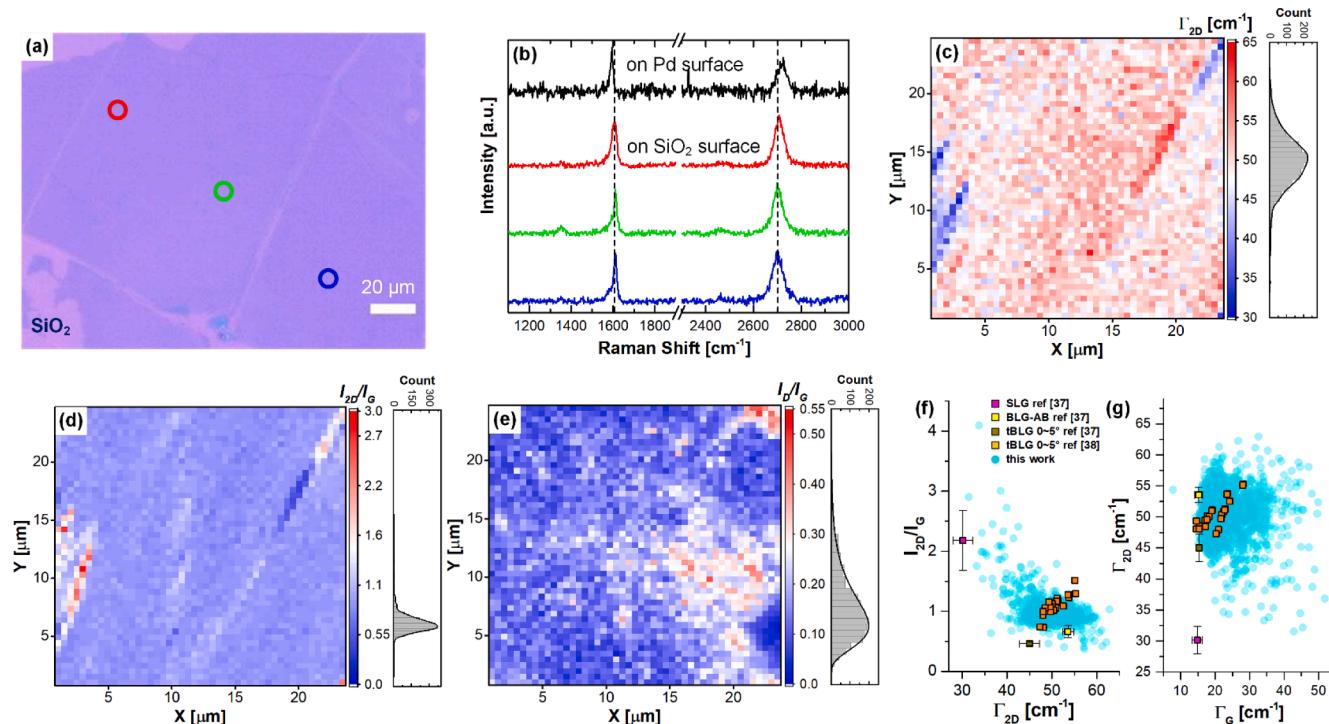


Fig. 2. Raman spectroscopy characterization of interface-grown graphene on SiO₂. (a) Top-view optical microscope image of as-grown graphene on SiO₂ after Pd etching. (b) Comparison of Raman spectra obtained on as-grown Gr-Pd surface and different locations in (a). The black dash lines are guides to the eye. A notable blue shift in the 2D peak of graphene grown on the Pd is observed compared to interface-grown graphene. (c) Raman 2D peak FWHM mapping of as-grown graphene over a 25 × 25 μm² area. The histogram shows Γ_{2D} spans 40–60 cm⁻¹. (d) 2D to G intensity ratio mapping shows uniform I_{2D}/I_G distribution with an average value of 0.89 over a 25 × 25 μm² area. (e) D to G intensity ratio mapping shows relatively low defect density (average I_D/I_G = 0.11) over the same area. (f) Comparison of I_{2D}/I_G vs Γ_{2D} with the reported values of SLG, AB stacked BLG, and BLG with low twist angles of 0–5°. (g) Comparison of Γ_{2D} with those of SLG, AB stacked BLG, and BLG with twist angles of 0–5°. Laser excitation: 532 nm.

3. Results and discussion

3.1. Characterization of as-grown graphene on SiO₂

No large-scale lamination wrinkles or folds in graphene-covered areas are observed on SiO₂/Si via optical imaging, as shown in Fig. 2a and Fig. S3d. A few cracks are present sparsely with spacing over 100 μm. These line defects can be ascribed to several factors including Pd layer creasing during lamination and press rolling processes, and Pd grain boundary effect and cracking due to thermal expansion and contraction during CVD. Fig. S3a-c present typical Pd surface topography images after annealing, and in some regions, we observed sparse line defects, which could lead to additional roughness of tens of nanometers. Corresponding line defects could appear at the Pd-SiO₂ interface and cause non-uniform interfacial carbon precipitation and cracks in interface-grown graphene films after Pd removal. Fig. 2b presents typical Raman spectra of as-grown graphene (laser excitation: 532 nm), comparing graphene on the Pd surface and at the Pd-SiO₂ interface (after etching of the Pd). For the graphene on SiO₂, we observe the G peak at ~1610 cm⁻¹, the 2D peak at ~2700 cm⁻¹, and a small D peak at ~1350 cm⁻¹. Compared with the Raman characteristics of SLG, there is a ~20 cm⁻¹ offset in the G and the 2D peak frequencies. This can be caused by several factors, including the stacking order, straining, and doping effects, which we will discuss in detail later. The uniformity and quality of as-grown graphene are demonstrated by the Raman mapping of the 2D peak full width at half maximum (FWHM, Γ_{2D} in Fig. 2c), the 2D to G peak intensity ratio (I_{2D}/I_G in Fig. 2d), and the D to G peak intensity ratio (I_D/I_G in Fig. 2e) over a 25 × 25 μm² area (approximately 2300 points, all Raman spectra are presented in Fig. S4). The 2D peak is asymmetric and can be well fitted by four Lorentzian curves with different frequencies spanning 40–60 cm⁻¹ (see Fig. S4c and Fig. 2c). This dispersive feature of the 2D peak suggests four double-resonance Raman processes caused by two stacked graphene layers in as-grown graphene [32–36]. Moreover, Fig. 2d shows I_{2D}/I_G distribution ranging from 0.36 to 4.89 with an average value of 0.89 over the mapping area. The I_{2D}/I_G values, the 2D peak frequency, and the lineshape suggest the presence of BLG. Considering the Γ_{2D} (BLG) ranges from 45 to 60 cm⁻¹, and I_{2D}/I_G (BLG) is from 0.7 to 1.3 [23], the BLG coverage in Fig. 2c-e is above 94 % of the area. The formation of BLG films at the Pd-substrate interface can be attributed to the high carbon solubility of the Pd, the high carbon radical concentration from C₂H₄ decomposition, and the high carbon precipitation rate at the interface between the laminated Pd film and the dielectric substrates. When lowering the hydrocarbon load, for example, changing the precursor to CH₄ in the recipe A listed in Table S1, we obtained SLG-preferred interfacial growth implied by Raman characterization that Γ_{2D} less than 40 cm⁻¹ and $I_{2D}/I_G > 3$, as shown in Fig. S5. Moreover, slightly higher C₂H₄ concentration (recipe C in Table S1) resulted in few-layer and multilayer graphene islands growth, as indicated by the Raman characteristics in Fig. S5 (Γ_{2D} spans 30–75 cm⁻¹ and I_{2D}/I_G spans 0.1–1).

Moreover, Fig. 2e presents I_D/I_G distribution with a relatively low average value of 0.11. About 90 % of the mapping area shows I_D/I_G less than 0.25, indicating high crystallinity of interface-grown BLG under the stated CVD condition. Further, the stacking order of as-grown BLG can be roughly determined by simultaneous comparisons of different Raman characteristics [32,37,38]. Fig. 2f and 2g compare the features of I_{2D}/I_G vs Γ_{2D} and Γ_G vs Γ_{2D} with those of SLG, AB stacked BLG, and BLG with twist angles of 0–5° [38,39], respectively. Clearly, as-grown BLG in this work is in the region corresponding to small twist angles. In addition, we analyzed the Γ_G (BLG) / Γ_G (SLG) and found it above 1.5 over ~98 % of the area (Fig. S4d). This also suggests the low twist angle BLG feature since interlayer interaction of AA or AB stacking arrangements can give different local phonon frequencies and broaden the total G spectral width for a large unit cell associated with low twist angles [40].

Further insights come from the surface morphology of the Pd and SiO₂/Si through interfacial CVD. First, after annealing and press rolling,

the Pd leaf becomes flat and conformal to SiO₂ surface, as presented in Fig. 1d, e and Fig. S1. Atomic force microscope (AFM) topography images show the representative microscopic morphology of the annealed Pd surface before CVD, as shown in Fig. 3a, b. The height profile along the line marked in yellow in Fig. 3b is shown in Fig. 3c, implying a root mean square (RMS) roughness of 4.75 nm, which is comparable to the reported surface roughness of annealed copper foils typically used for graphene synthesis [41]. After CVD, surface reconstruction of the graphene-Pd (Gr-Pd) surface results in sharp steps and terraces (Fig. 3d, e) arising from the strong interaction between graphene and the underlying metal catalyst [18,19]. More importantly, graphene wrinkles invariably exist on the Pd surface and are roughly perpendicular to the Pd steps, as highlighted by arrows in Fig. 3e. Fig. 3f shows the height profile across the Pd steps and graphene wrinkles on the as-grown Gr-Pd surface, with a RMS roughness of 4.09 nm. In contrast, the surface roughness of interfacial graphene, measured on SiO₂ surface after etching of the graphene-coated Pd, is 0.96 nm, see Fig. 3g-i. There are no visible graphene wrinkles or folds on SiO₂, as shown in Fig. 3g, h. AFM phase shifts are used to qualitatively evaluate the Gr-Pd interfacial interaction. For the Pd top surface, Fig. S6a, b highlight the non-uniform Gr-Pd bonding with significant phase shifts due to graphene wrinkles and folds. Interfacial graphene on SiO₂ surface exhibits a homogeneous phase shift which indicates its uniform contact with the substrate, as shown in Fig. S6c, d. To further rule out effects from Pd wet etching, we qualitatively evaluated the Gr-Pd interface right after CVD synthesis using Transmission Electron Microscopy (TEM). Fig. 3j-l compare the cross sections of the Pd surface and the Pd-SiO₂ interface after interfacial graphene growth without chemical etching effects. The Pd-SiO₂ interface is comparably flat as SiO₂ while the Pd surface demonstrates certain facets. The flatness of SiO₂ surface and the intimate interface between the Pd and SiO₂ in CVD processes prevented the Pd structure reconstruction at the interface, therefore, enabling the interface-grown graphene to be highly flat and uniform. Here, the existence of BLG on SiO₂ was further verified by cross-sectional TEM imaging (Fig. 3l) and graphene thickness measurement from AFM topography height profile (Fig. 3m, n).

3.2. Synthesis of BLG on various dielectric substrates

While Pd-SiO₂ serves as a proper model system, direct graphene growth on various dielectric substrates via interfacial CVD can be achieved by rationally controlling carbon diffusion and precipitation at the Pd-substrate interface. Simplified thermodynamic calculations were performed to generalize how graphene forms at the Pd-substrate interface. We designate (Fig. S7a): state I as the initial Pd/substrate stack before interfacial CVD; state II-A, graphene forms on both sides of the metal layer; and state II-B, graphene forms only on the metal surface. The energy difference between state I and state II-A can be expressed as: $\Delta G_1 = [\gamma_{Gr} + 2\gamma_{Gr-Pd} + \gamma_{Gr-sub} + t_{surf}\Delta G_{surf} + t_{int}\Delta G_{int}] - [\gamma_{Pd} + \gamma_{Pd-sub}]$ [42]. Here, γ is the interfacial energy, and t_{surf} and t_{int} are the graphene thicknesses on the Pd surface and at the interface, respectively. ΔG_{surf} and ΔG_{int} are the graphene formation energy per unit volume on the Pd surface and at the interface, respectively. Similarly, the energy difference between state I and state II-B is $\Delta G_2 = [\gamma_{Gr} + \gamma_{Gr-Pd} + \gamma_{Pd-sub} + t_{surf}\Delta G_{surf}] - [\gamma_{Pd} + \gamma_{Pd-sub}]$.

Assuming $t_{surf} >> t_{int}$ and $\Delta G_{surf} \approx \Delta G_{int}$, we estimated the relative energy difference $\Delta G_1 - \Delta G_2$, which indicates the thermodynamic feasibility of graphene formation in state II-A versus II-B. We compared $\Delta G_1 - \Delta G_2$ for Pd-SiO₂, Pd-sapphire (0001), Pd-quartz, and Pd-MgO (100) systems. As presented in Fig. S7b, the Pd-SiO₂ and the Pd-sapphire (0001) systems have negative $\Delta G_1 - \Delta G_2$, which indicates that it is more thermodynamically favorable to have graphene grown on both sides of the laminated Pd. However, Pd-quartz and the Pd-MgO (100) show positive $\Delta G_1 - \Delta G_2$, indicating that interfacial graphene is not expected to form on quartz or MgO (100) surface, and more investigation is required to reach state II-A. Following the processes presented in

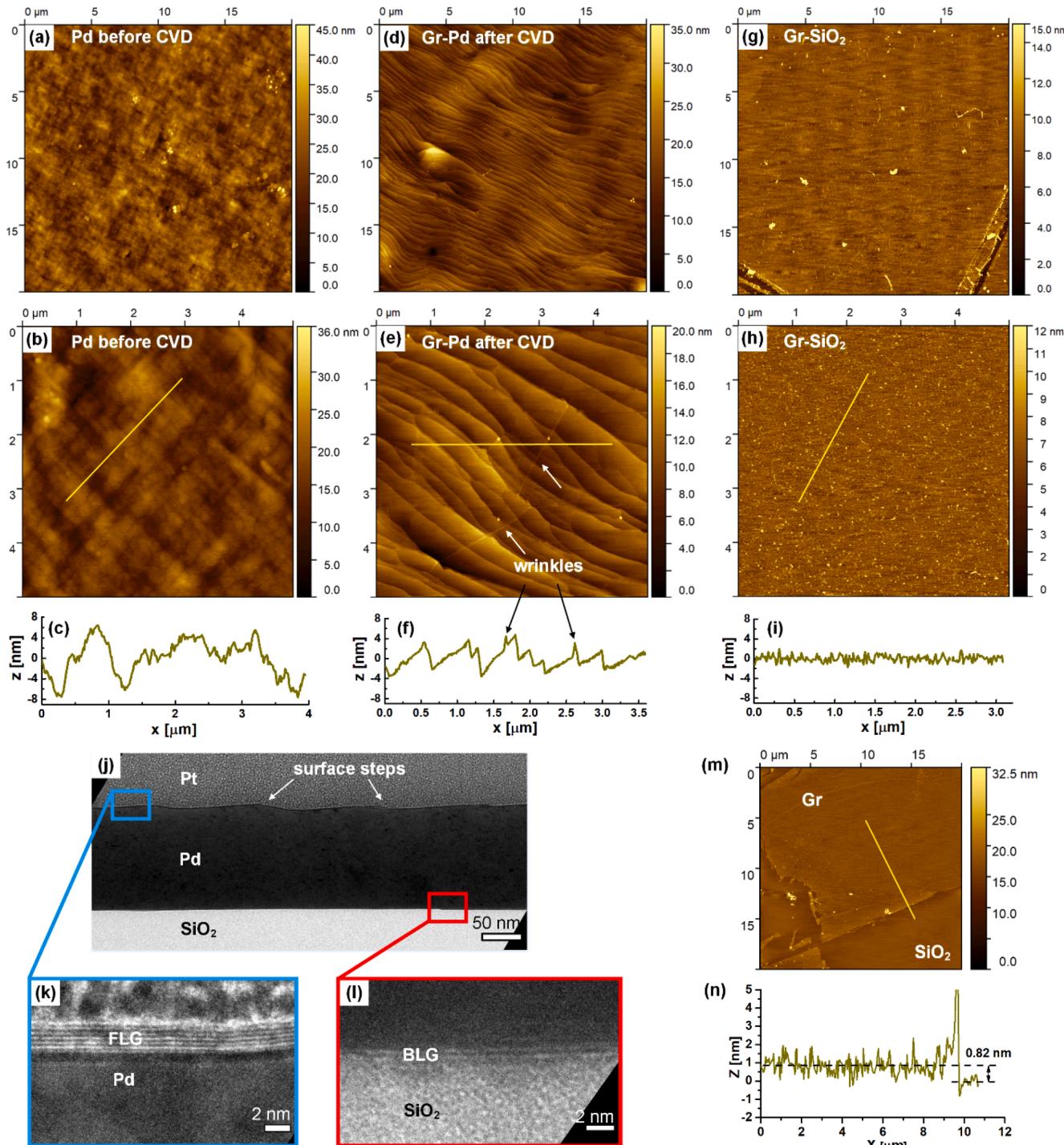


Fig. 3. Surface morphology evolution in interfacial CVD synthesis. (a, b) AFM topography images of annealed Pd film on SiO₂. (c) Height profile of annealed Pd along the line marked in yellow in (b); (d, e) AFM topography images of as-grown Gr-Pd surface show surface steps, terraces, and graphene wrinkle formation after CVD synthesis. (f) Height profile of as-grown Gr-Pd along the yellow line in (e). (g, h) AFM topography images of as-grown graphene on SiO₂ surface. (i) Height profile of as-grown Gr along the yellow line in (h). (j) Cross-sectional bright-field TEM image of as-grown Gr-Pd on SiO₂ showing steps on the Pd top surface versus the flat Pd-SiO₂ interface. (k) TEM image of FLG formation on the Pd surface. (l) TEM image of BLG at the Pd-SiO₂ interface. (m, n) AFM topography image and height profile (along the yellow line) of as-grown graphene on SiO₂ verifying the thickness of BLG as ~0.82 nm.

Fig. 1, we verified interfacial graphene synthesis using Pd leaves on amorphous quartz, sapphire (0001), and MgO (1 0 0) substrates. With the thermodynamic feasibility analysis guidance in **Fig. S7b**, we refined the growth recipe for each Pd-substrate system, as listed in **Table S2**. Uniform BLG films were directly grown on all three dielectric substrates, while FLG covered the Pd top surface for each system, as indicated by the representative Raman spectra in **Fig. 4a-c**. Notably, longer CVD

growth times and higher hydrocarbon flows are required for interfacial BLG growth in Pd-quartz and Pd-MgO systems than those in Pd-SiO₂ and Pd-sapphire cases (**Table S2**). This can be attributed to the low carbon precipitation and high graphene formation energy barrier at the Pd-quartz and Pd-MgO (0 0 1) interfaces, as depicted in **Fig. S7b**.

We further characterized the surface morphologies using AFM, as displayed in **Fig. 4d-i**. Graphene grown on the top Pd surface of the Pd-

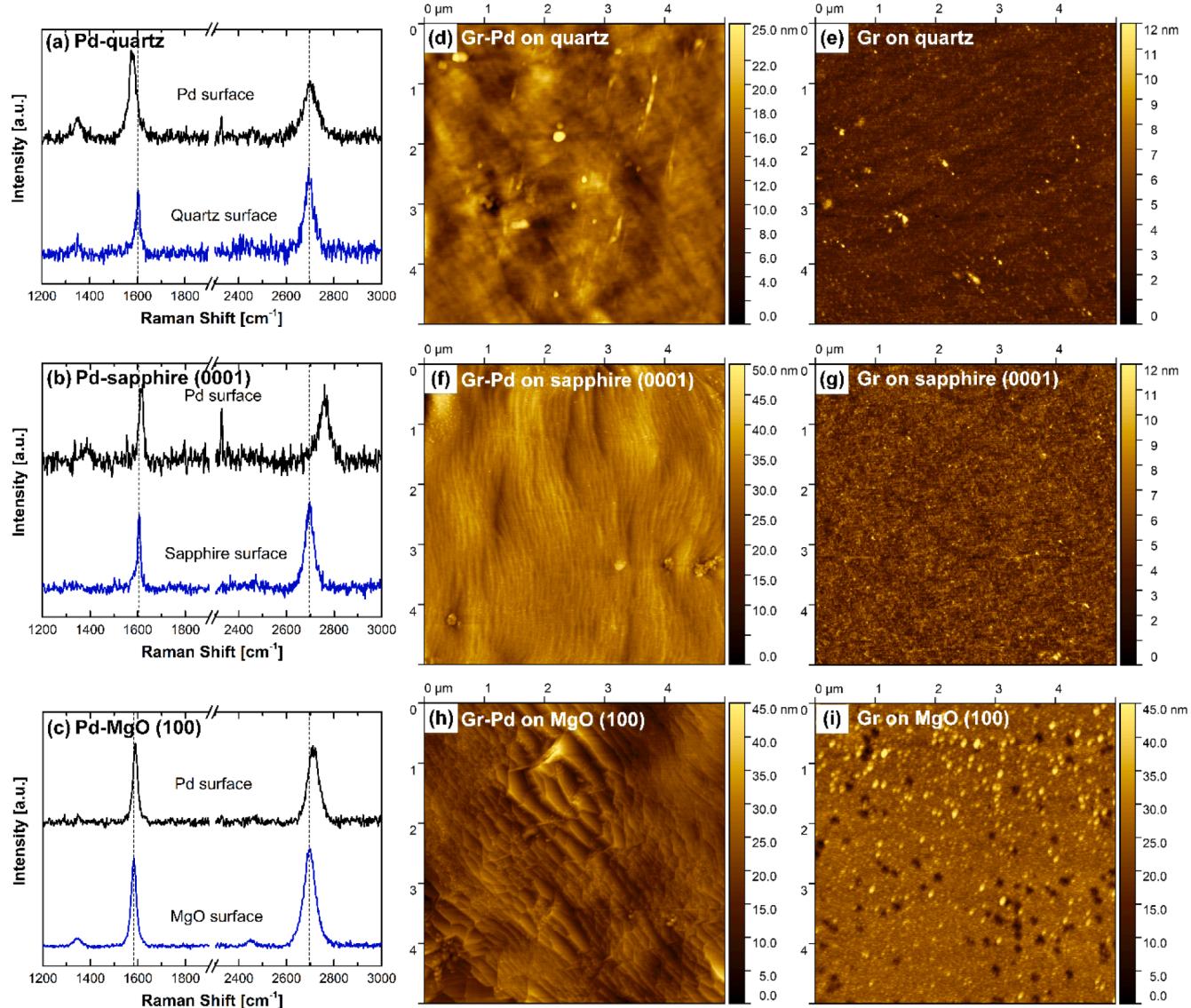


Fig. 4. Characterization of as-grown graphene on various dielectric substrates. (a-c) Raman spectra of as-grown graphene on Pd, quartz, sapphire (0001), and MgO (100), respectively. (d) AFM topography image of as-grown Gr-Pd on quartz, with a RMS roughness ~ 3.20 nm. (e) AFM topography of as-grown graphene on quartz after Pd etching, with a RMS roughness ~ 0.84 nm. (f) AFM topography image of Gr-Pd on sapphire (0001), with a RMS roughness ~ 5.55 nm. (g) AFM topography image of interfacial graphene grown on sapphire (0001) with a RMS roughness ~ 1.20 nm. (h) AFM topography image of Gr-Pd on MgO (100) with a RMS roughness ~ 3.98 nm. (i) AFM topography image of interfacial graphene grown on MgO (100) with a RMS roughness of ~ 4.16 nm.

quartz, Pd-sapphire (0001), and Pd-MgO (100) systems shows various wrinkles, steps, and terraces with RMS surface roughness of 3.20 nm, 5.55 nm, and 3.98 nm, respectively. The Pd is compatible with these substrates at the synthesis temperature (800 °C) without causing interfacial reconstruction or inter-diffusion. BLG at the interface exhibits high uniformity with no wrinkles and lower RMS roughness (0.84 nm and 1.20 nm for Gr-quartz and Gr-sapphire, see comparisons in Fig. S8 and Fig. S9). Notably, the Gr-MgO shows a similar surface roughness of 4.12 nm as that of Gr-Pd/MgO. This is caused by MgO surface reconstruction after high-temperature treatment [43].

3.3. Strain-doping properties of as-grown BLG at the interface

Besides metal surface corrugation, another primary origin of wrinkles in graphene grown on metal surfaces (i.e., foils or on the top surface of the Pd as studied herein) is the thermal expansion coefficient difference between the graphene and the metal. This thermal expansion mismatch introduces significant stress in the graphene layer, making it

prone to delaminate from the underlying metal or buckle to release the stress [12,17,21]. Here, we characterized the strain of as-grown interfacial graphene after removal of the Pd and found a nearly strain-free status approaching that of pristine BLG.

Correlative analysis of the Raman frequency shifts of G and 2D peaks provides quantitative information about the strain and doping properties in the graphene lattice [44,45]. To ascertain the strain-doping properties in BLG layers formed on the dielectric substrates, we analyzed the Raman frequency correlations of as-grown graphene in the Pd-SiO₂, Pd-sapphire, Pd-quartz, and Pd-MgO systems. Fig. 5a presents a correlation map of the G frequency (ω_G) and the 2D frequency (ω_{2D}) for Pd-SiO₂: graphene grown on the Pd surface (referred to as Gr-Pd, orange squares) and BLG grown on SiO₂ (referred to as Gr-SiO₂, violet circles). The colored non-orthogonal lines represent Raman frequencies of purely strained (solid blue line) and purely doped (solid red line) BLG, and their intersection represents strain- and doping-free BLG, which is around ($\omega_G \sim 1579.8$ cm⁻¹, $\omega_{2D} \sim 2692.1$ cm⁻¹) [46,47].

We can decouple the strain and doping effects by projecting the

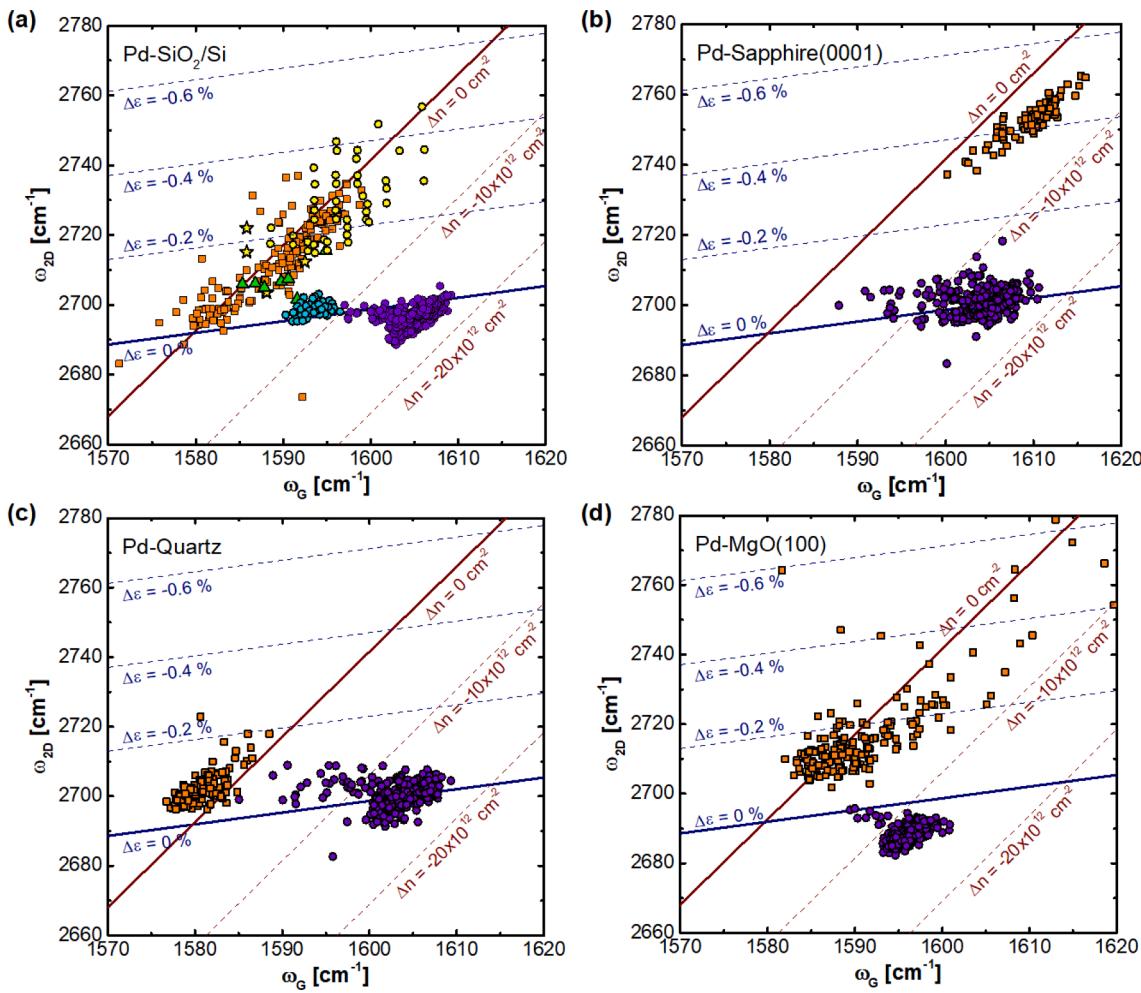


Fig. 5. Correlation between the frequencies of the G and the 2D peaks of as-grown Gr-Pd and graphene on different dielectric substrates. Scatterplots of ω_G vs ω_{2D} obtained from (a) Pd-SiO₂ system; (b) Pd-sapphire (0001) system; (c) Pd-quartz system; (d) Pd-MgO (100) system. The strain and doping axes (zero doping and zero strain) are for BLG from ref. [46] and ref. [47], respectively. The orange square dots represent (ω_G, ω_{2D}) of as-grown BLG on the Pd surface, and the violet circle dots represent (ω_G, ω_{2D}) of as-grown BLG on dielectric substrates. Note: in (a), the yellow stars represent (ω_G, ω_{2D}) of CVD-grown BLG on the evaporated Ni free surface, while the green triangles represent (ω_G, ω_{2D}) of the interface-grown BLG at the evaporated Ni-SiO₂ interface [23]. The yellow circles represent (ω_G, ω_{2D}) of CVD-grown SLG on the Cu foil free surface [49] and the cyan circles are for (ω_G, ω_{2D}) of the transferred SLG on SiO₂/Si substrate with thermal annealing [51].

measured data on purely strained and purely doped axes [45]. Remarkably, Gr-SiO₂ undergoes nearly zero strain with a slight deviation, while, Gr-Pd exhibits compressive stress ranging from 0 to 0.3 %. The reasons are twofold. First, the Pd-SiO₂ interface experienced negligible thermal strain due to the small thermal expansion of SiO₂ ($\alpha_{\text{SiO}_2} \sim 0.55 \times 10^{-6} \text{ K}^{-1}$) compared to that of Pd ($\alpha_{\text{Pd}} \sim 11.8 \times 10^{-6} \text{ K}^{-1}$) within the synthesis temperature range (25–800 °C). BLG formed at the interface unupon interfacial CVD cooling step was also strained subtly with a thermal expansion coefficient changing from $\sim 2.0 \times 10^{-6} \text{ K}^{-1}$ at 800 °C to $\sim 6.0 \times 10^{-6} \text{ K}^{-1}$ at 25 °C [48]. Based on these effects, nearly strain-free BLG on SiO₂ substrate was obtained. Second, the Pd surface, about 150 nm away from the SiO₂ interface, can freely expand and shrink during CVD synthesis. As a result, graphene on the Pd surface is usually compressed. This matches well with the reported observations, and the compressive strain variation is related to the local metal crystal orientation [49].

In terms of doping, although the interface-grown BLG shows small Raman D peaks and atomic-scale defects, we estimate that it is P-doped with a charge concentration of approximately $15 \times 10^{12} \text{ cm}^{-2}$, following the doping axes in Fig. 5a. The charge concentration is about $10 \times 10^{12} \text{ cm}^{-2}$ higher than reported values for BLG transferred to SiO₂/Si with thermal annealing [50,51]. This is because of closer contact between graphene and the substrate, less intercalated molecules effects in

interfacial CVD synthesis, and possible extrinsic doping from chemical wet etching of the Pd. We observed similar strain-doping results in the Pd-sapphire, Pd-quartz, and Pd-MgO systems by Raman spectroscopy, as presented in Fig. 5b-d.

3.4. Carrier mobility of as-grown graphene

Last, via statistical analysis of the Raman 2D peak, we compared the carrier mobility over as-grown BLG on different dielectric substrates [52,53]. The Γ_{2D} distributions, shown in Fig. 6a, agree well with reported data for high-quality BLG on the corresponding dielectric substrates [23,54–56]. In Fig. 6b, we estimated the long-range scattering mobility (μ_l) of the BLG, which is a predominant part of carrier mobility of CVD-grown BLG. Average μ_l values are $490 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $1006 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $343 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and $80 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for BLG on SiO₂, sapphire (0001), quartz, and MgO (100) at room temperature, respectively. These results approach published values for CVD-grown graphene transferred to the dielectric substrates [53]. Our estimates give > 30 % variation in the long-range scattering mobility of as-grown BLG on sapphire and approximately 40 % lower in average value than that of the reported graphene films [4]. This can be ascribed to many factors, for example, the small graphene domain size, variation in number of graphene layers over a large area, extrinsic doping by chemical wet etching,

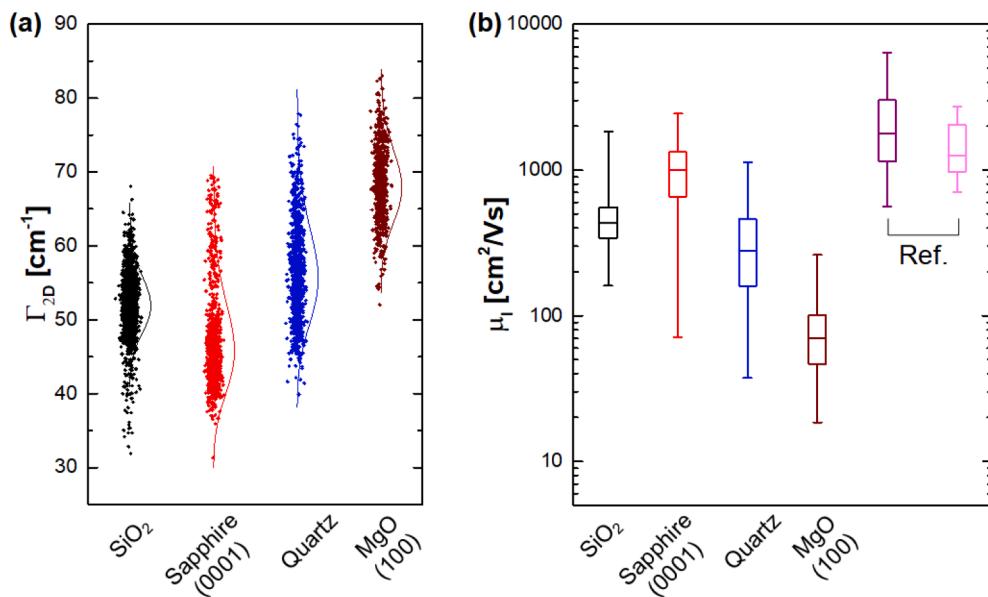


Fig. 6. The estimated carrier mobility of as-grown graphene on dielectric substrates. (a) The Raman 2D peak FWHM (Γ_{2D}) of as-grown BLG on SiO_2 , Sapphire, Quartz, and MgO substrates, after removal of Pd by wet etching. (b) The long-range scattering mobility (μ_1) derived from the Raman FWHM in (a). Note: the purple box in (b) represents the mobility for epitaxial grown graphene on SiC (0001) [52], while the magenta box represents that for transferred graphene on SiO_2/Si [53].

and the influence of air or moisture during Raman spectroscopy.

Although we show the versatility of wrinkle-free BLG growth directly on the dielectric substrates, many issues remain to be explored to manufacture large-scale ultra-flat BLG for electronic applications. The Pd leaf exhibits large grain structures while its thickness can be down-sized to ~ 100 nm. This makes an intimate and uniform metal-substrate interface possible and effectively circumvents the rate mismatch of carbon segregation through the metal lattice and the metal grain boundaries, which usually leads to the formation of multilayer graphene islands when physically deposited films are used for interfacial synthesis [1]. However, more precise control is needed on metal foil handling, lamination, and control of carbon precipitation at the metal-substrate interface. Parameters such as contact force, and residual stress in the metal foil during the press rolling process. Furthermore, foil composition and CVD conditions on the interfacial chemical potential for carbon precipitation must be studied further, as these will influence the quality and integrity of interfacial graphene films. Moreover, carbon precipitation occurs where the conformal metal-substrate interface is; therefore, interfacial CVD can enable direct pattern growth of graphene [25]. One future implementation of interfacial CVD can be the direct integration of wrinkle-free graphene films onto 3D micro-structured substrates. In this case, press rolling of freestanding Pd leaves may not be a good option, but conformal graphene synthesis can be achieved by physically depositing a conformal metal catalyst layer. This is a subject of ongoing work.

4. Conclusions

In summary, we presented a facile and scalable synthesis route for highly-uniform BLG directly on dielectric substrates. Via interfacial carbon precipitation, wrinkle-free BLG films were produced with a sub-nm surface roughness on SiO_2 , sapphire, and quartz substrates. The Pd-substrate interface maintains high flatness and low metal grain boundary density at the graphene synthesis temperature of 800 °C. This approach enables uniform carbon precipitation-mediated graphene growth at the interface, and circumvents the formation of small-scale graphene wrinkles and folds caused by metal structure reconstruction, which is apparent on the free surface of the metal. Further, the constrained Pd-substrate interface results in as-grown BLG under nearly zero strain on the destination substrates. We estimate that a long-range

scattering mobility of $\sim 1000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in as-grown BLG on sapphire (0001) at room temperature. With the development of large-area techniques and further optimization of the metal-substrate interface uniformity, this approach is promising for graphene-based electronics using ultra-flat and even micro-textured 2D layers.

Data availability

The data generated and analyzed during the current study are available from the corresponding authors on reasonable request.

Author contributions

Kaihao Zhang: Conceived of the research topic, Designed and conducted the experiments. **A. John Hart:** Conceived of the research topic. All authors discussed the results and jointly wrote and revised the manuscript.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A. Supplementary material

Supplementary data to this article can be found online at <https://doi.org/10.1016/j.apusc.2022.154367>.

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