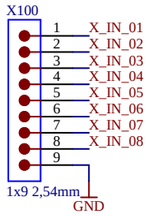
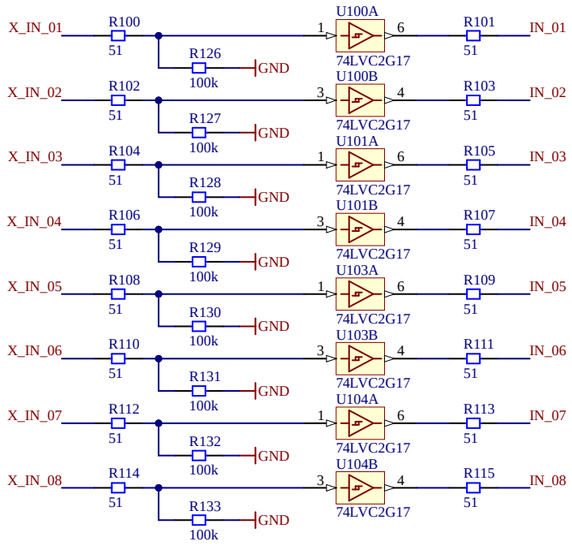
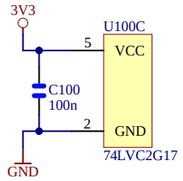
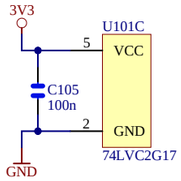
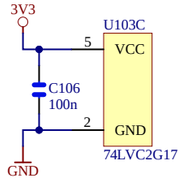
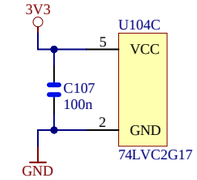


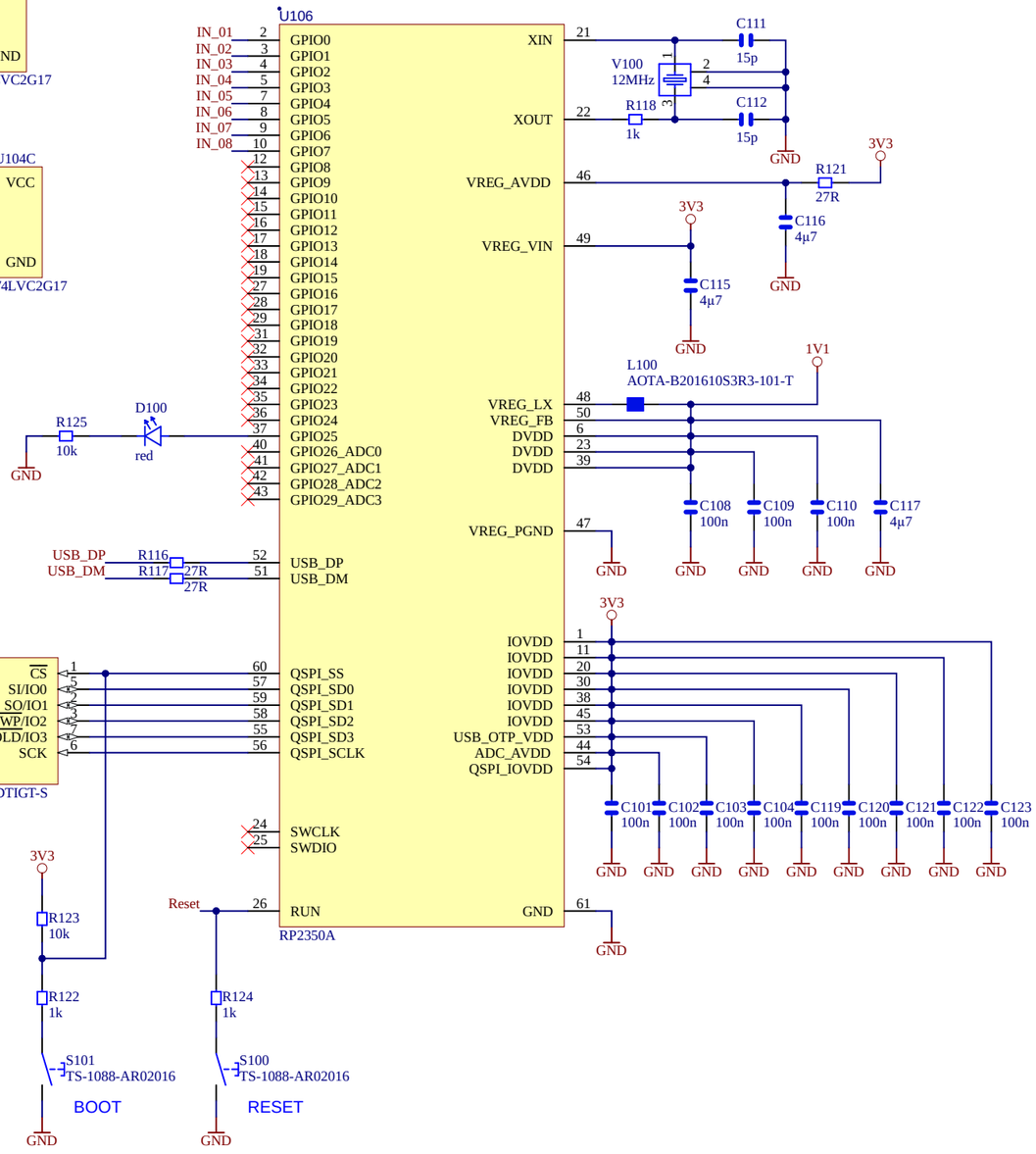


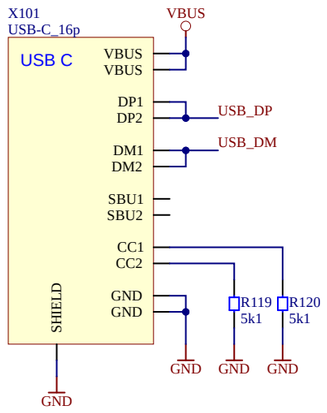


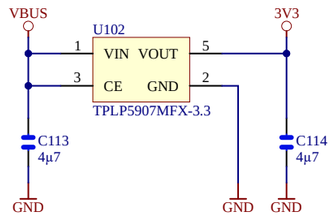












Note: LVC logic is 5V tolerant, even when supplied with 3.3V

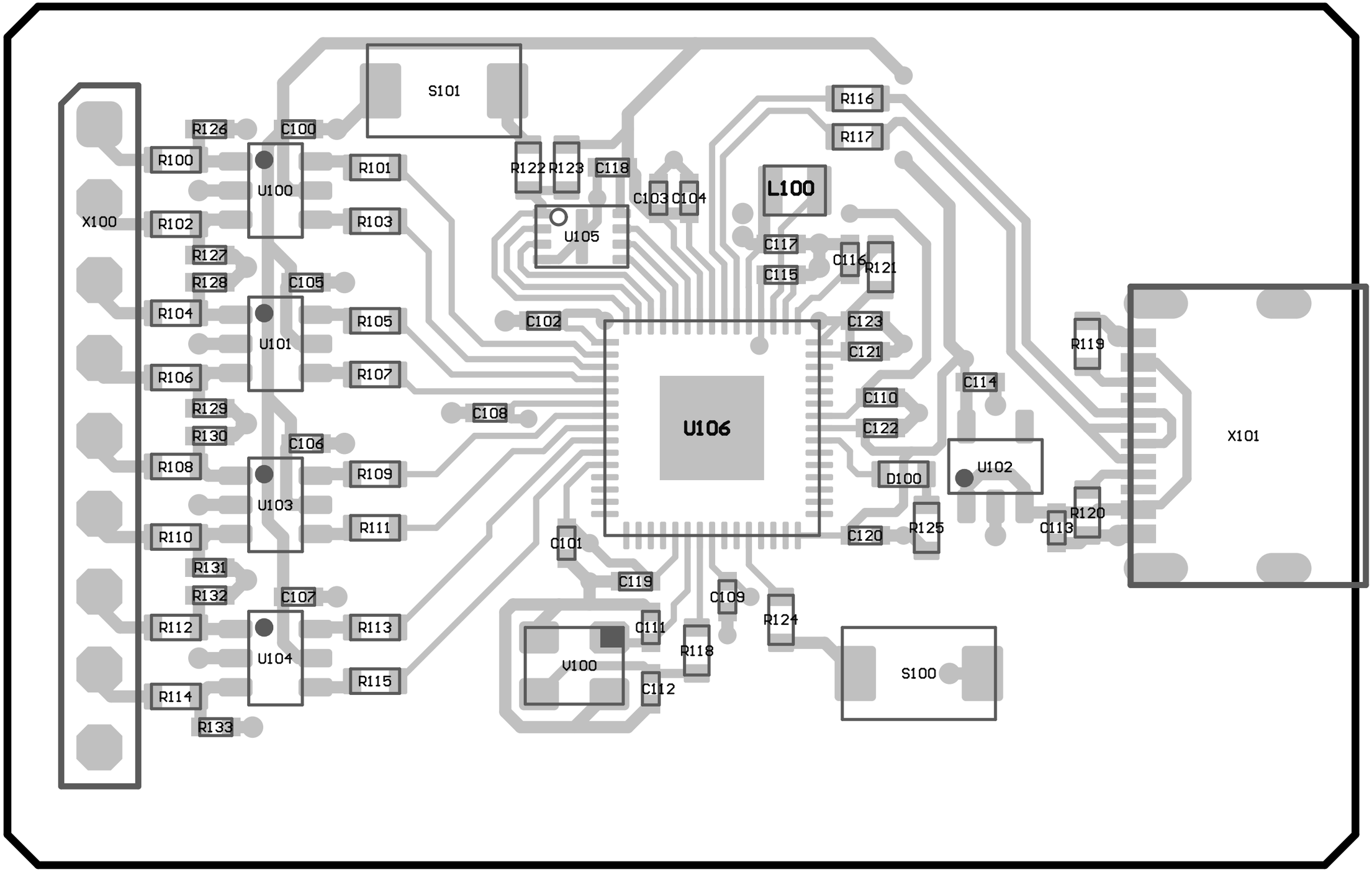
Input voltage range is 0...5.5V with a high detected around 2V, depending on the chip used.

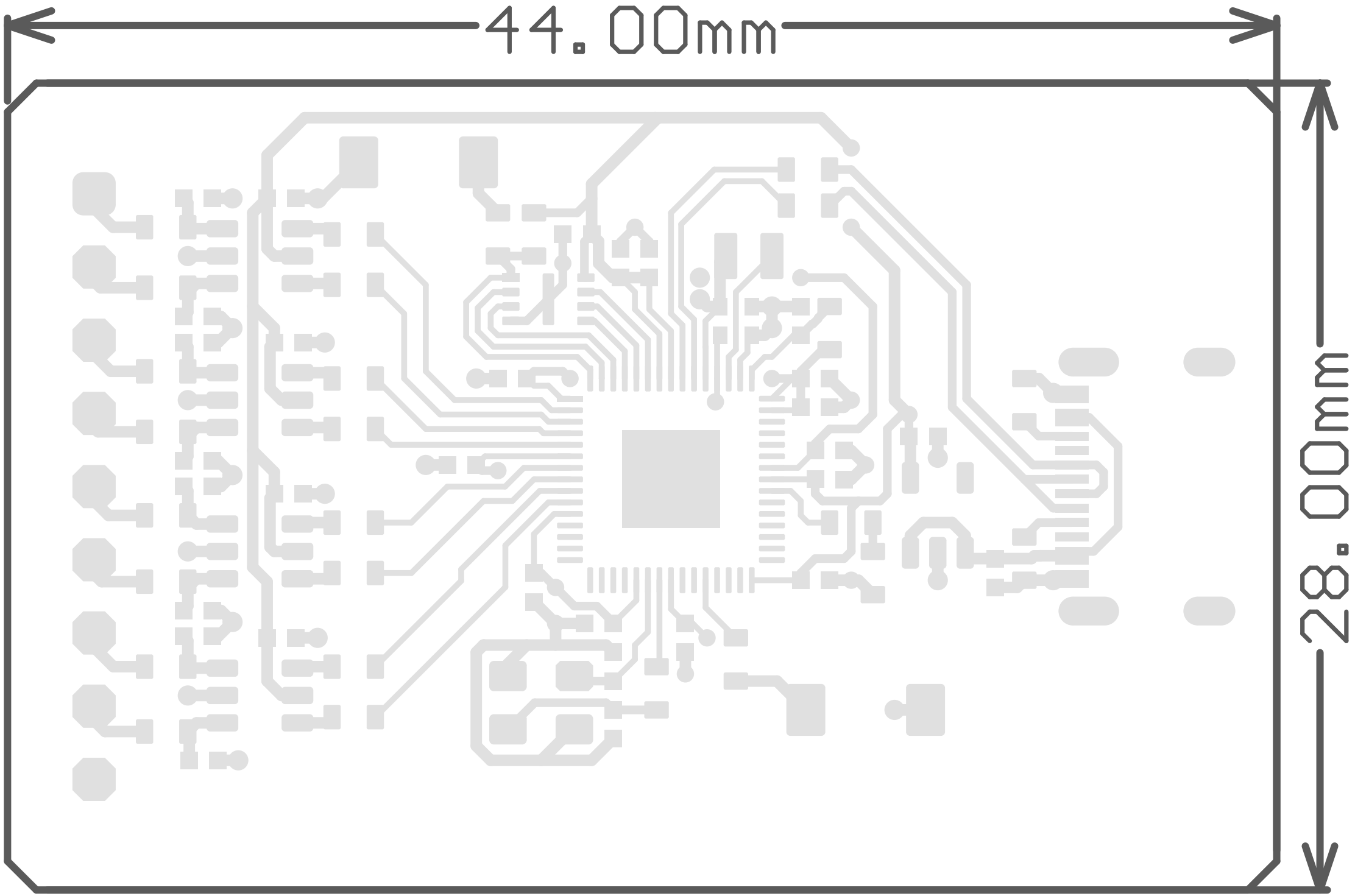
V1.1:
- refined silk-screen, channel numbers where not visible when populating a right angle pin header, added text "Boot"
- added a right angle footprint to X100
- removed the SWD debug header
- changed L100 inductor to RP2350 official type AOTA-B201610S3R3-101-T
- changed V100 crystal to RP2350 official type ABM8-272-T3
- change crystal load capacitors to match ABM8-272-T3
- BOM optimization: decreased AVDD series resistor to 27R to have one position less in the BOM
- added 100k pulldown resistors to prevent unused inputs from floating

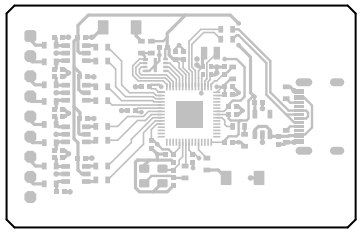
15pF/0402 = JLCPCB C1548
100nF/0402 = JLCPCB C1525
4.7µF/0402 = JLCPCB C23733
3.3µH = JLCPCB C42411119
12MHz = JLCPCB C20625731
USB-C = JLCPCB C2765186
74LVC2G17 = JLCPCB C10429

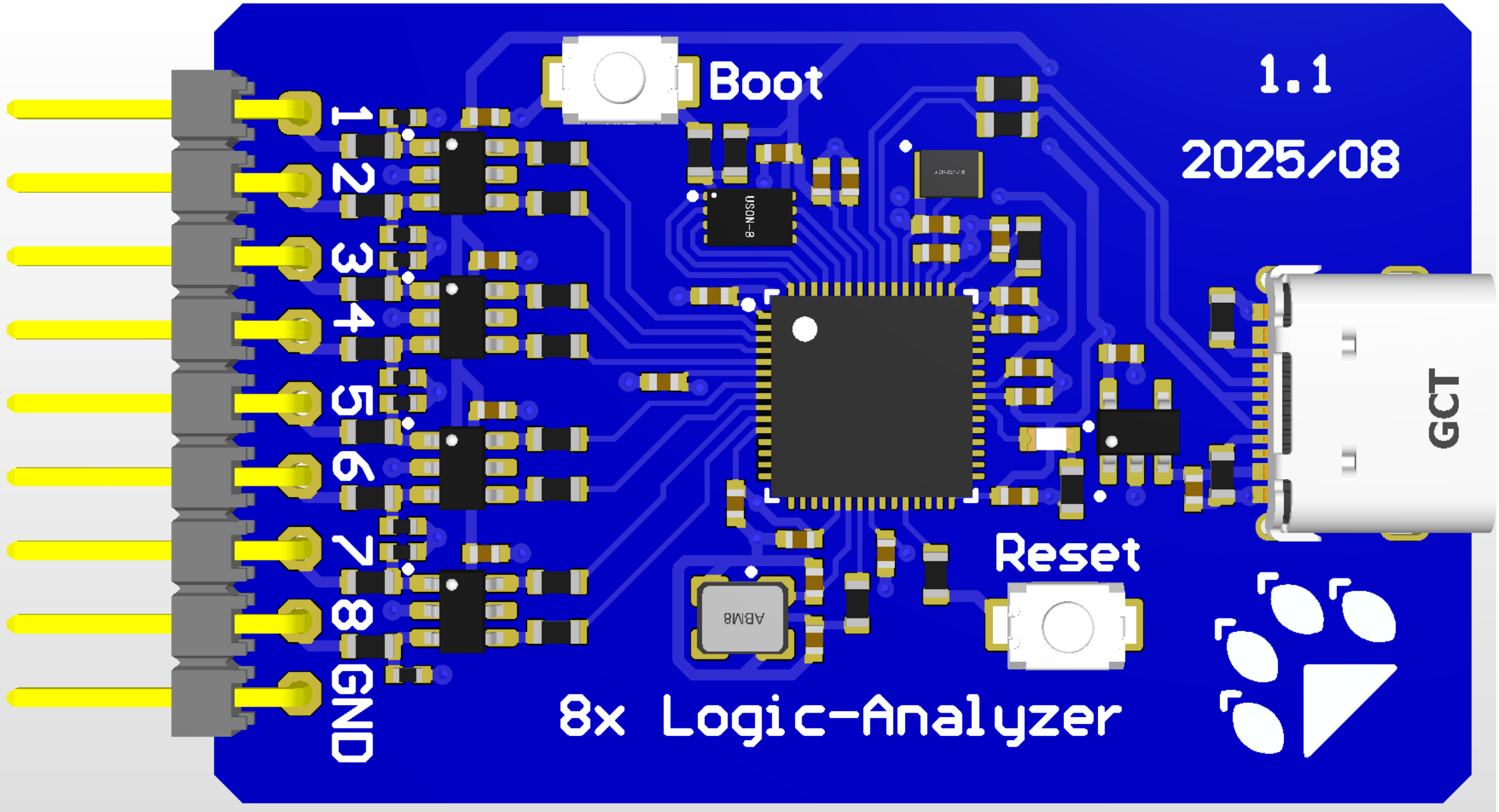
Hardware contribution for this project:
https://github.com/gusmanb/logicanalyzer

Project: 8x Logic Analyzer
Revision: 2
Date: 17.08.2025
Copyright: Rudolph Riedel
License: MIT


S101
R126
C100
R100
U100
R101
R122
R123
C118
R116
R117
L100
X100
R102
R103
C103
C104
U105
C117
C116
R121
R127
R128
C105
C115
R104
U101
R105
C102
C123
R119
C121
R106
R107
C114
R129
C108
C110
U106
R130
C106
C122
X101
R108
R109
D100
U102
U103
R120
R125
C113
R110
R111
C120
C101
R131
C119
R132
C107
C109
R124
R112
C111
R113
R118
U104
V100
S100
R115
C112
R114
R133


44.00mm
28.00mm




Boot
1.1
2025/08
1
2
3
4
5
6
7
8
GND
USON-8
GCT
Reset
ABM8
8x Logic-Analyzer