



EE301 Analog Circuits

Course Project

**Design of Beta Multiplier, Cascode Current Mirror and Cascode Amplifier in
22nm (0.8 V Supply) and 180nm (1.8 V Supply) Technologies**

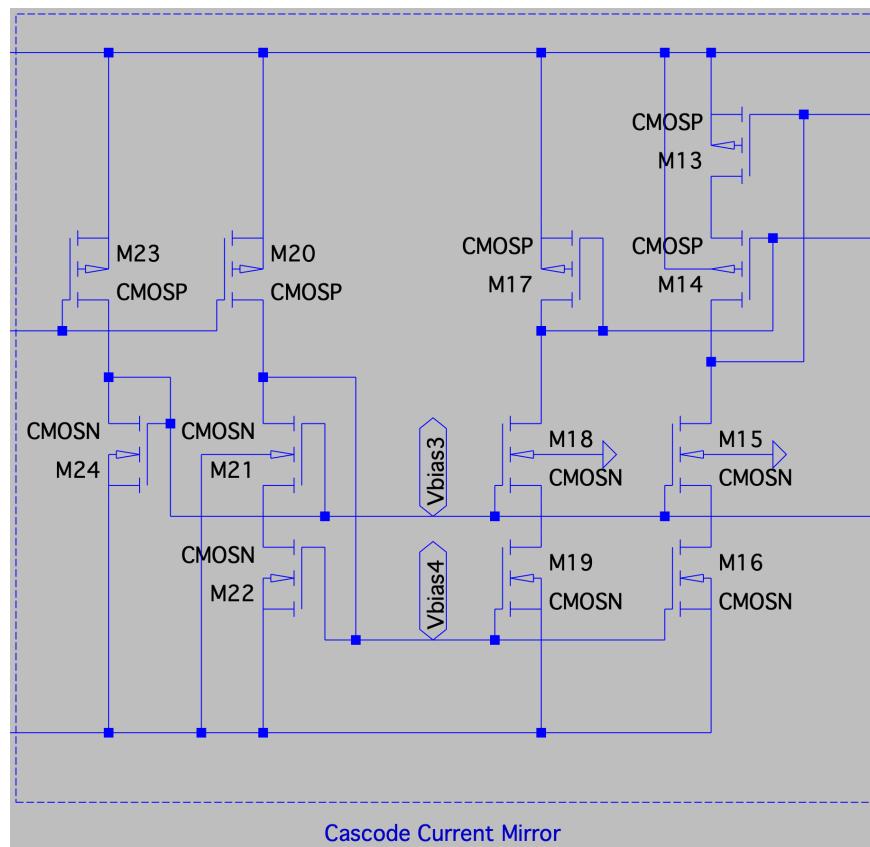
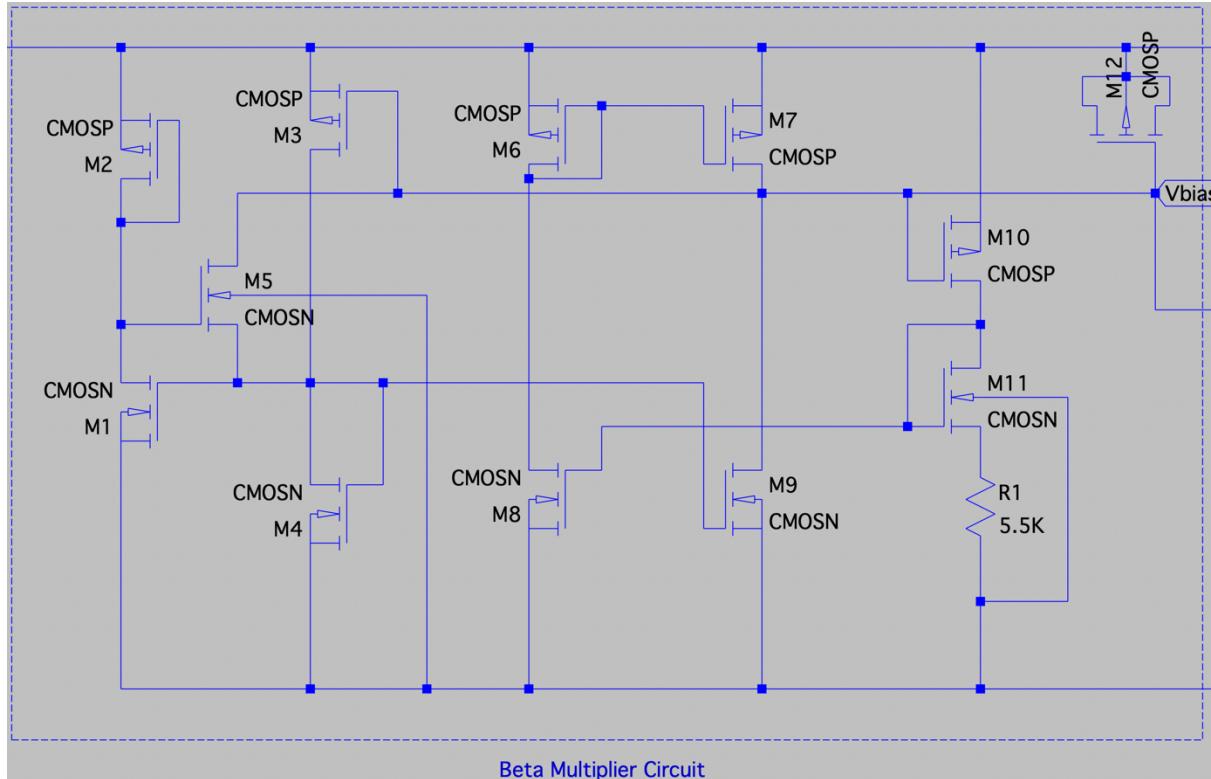
Submitted By: Rudra Kumar Chourasia

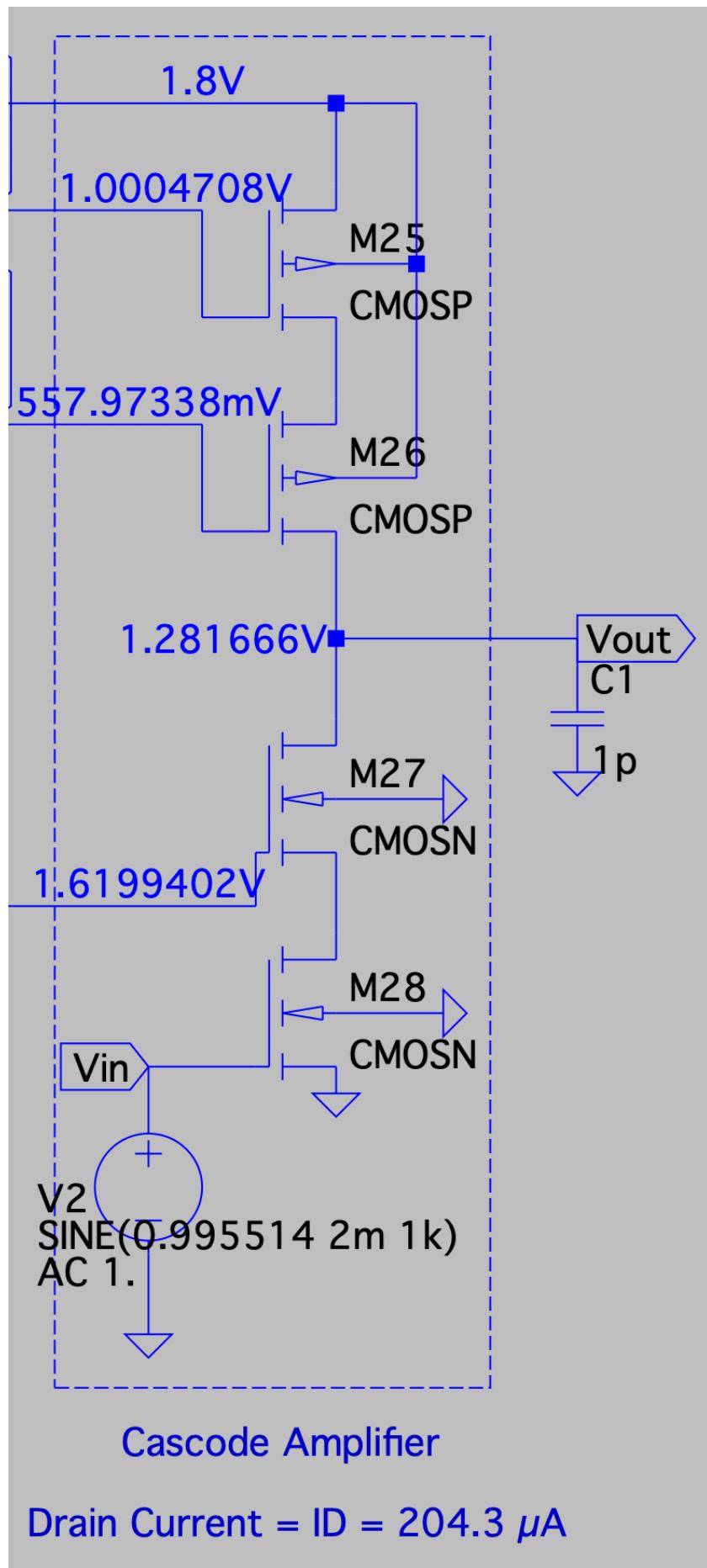
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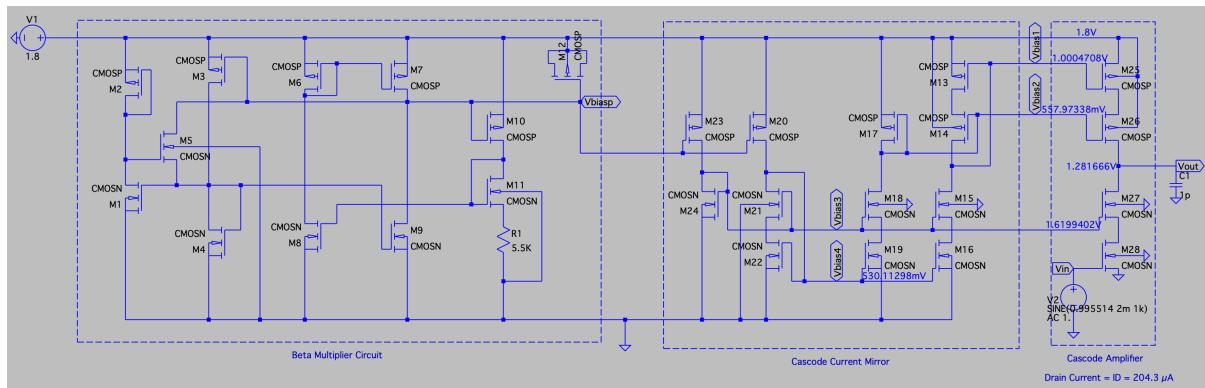
Submitted To: Prof. Mahendra Sakare

Date of Submission: 7th November 2023

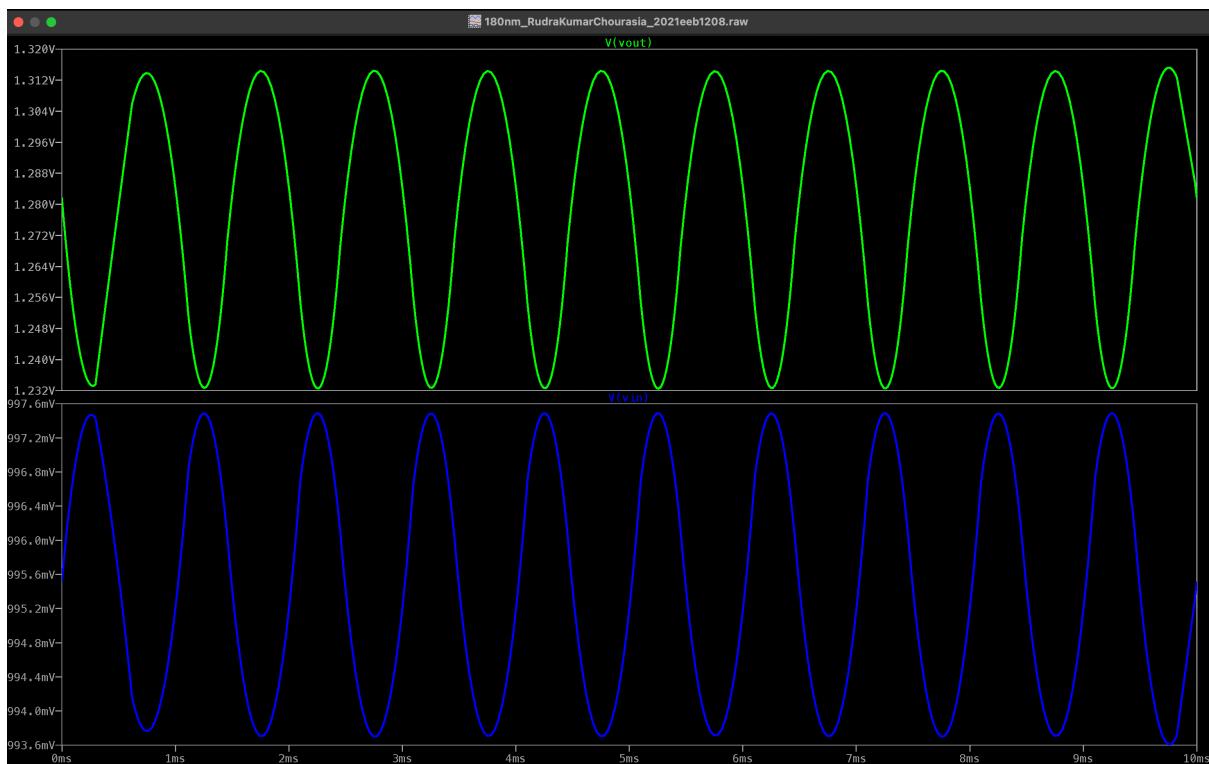
180 nm Technology Schematic Design







Circuit Diagram



Output Waveform for $V_{in} = 2 \text{ mV}$ at 1 KHz

$$V_{bias,1} = 1 \text{ V}$$

$$V_{bias,2} = 0.58 \text{ V}$$

$$V_{bias,3} = 1.62 \text{ V}$$

DC Analysis:

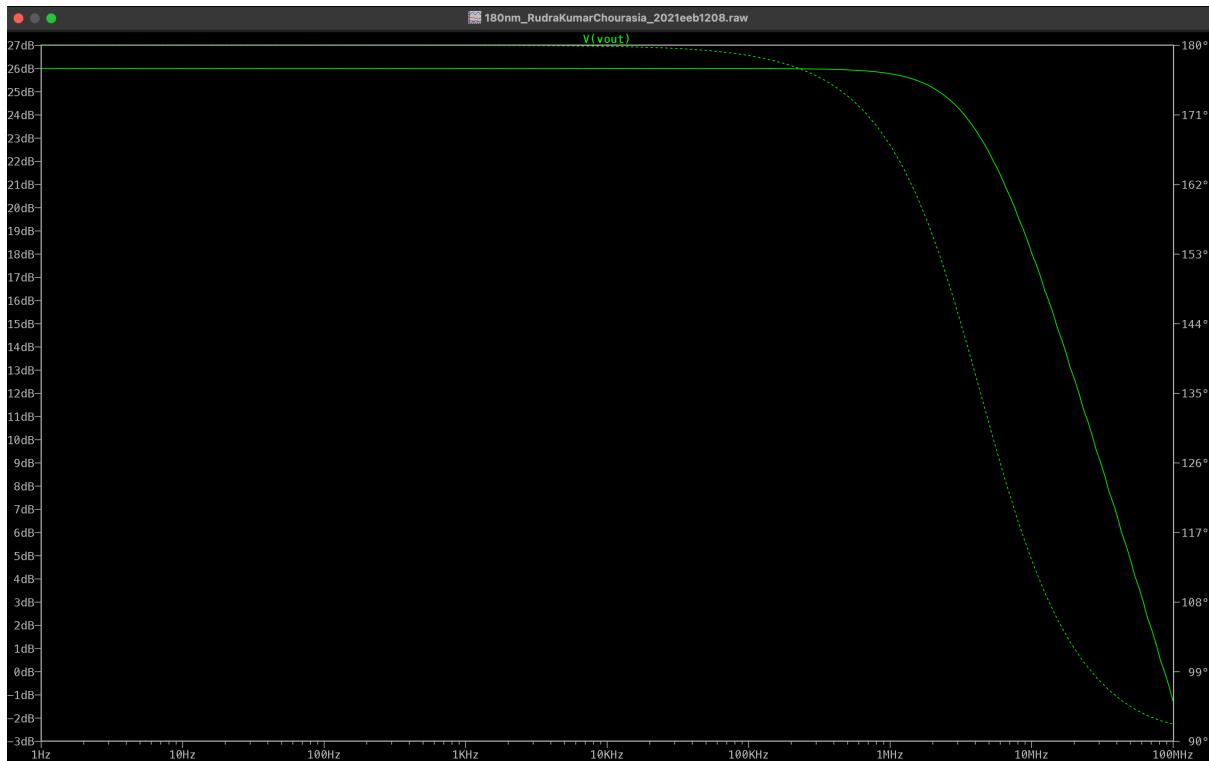
$$\text{DC offset} = 0.995514 \text{ V}$$

$$\text{Output voltage swing} = 1.313795 \text{ V to } 1.232621 \text{ V} = 81.174 \text{ mV}$$

$$\text{Input (or signal) voltage} = 4 \text{ mV}_{pp}$$

$$\text{Required Gain} = 20$$

$$\text{Practical Gain} = \frac{\text{output voltage swing}}{\text{input voltage swing}} = \frac{81.174}{4} = 20.2935$$



Frequency Response

AC Analysis:

We are getting a **low pass filter** whose parameters are:

1. Gain = $A_v = 26 \text{ dB}$
2. Cut-off frequency or f_c (Bandwidth) = 3.347 MHz
3. Unity gain bandwidth (UGB) = 86.909 MHz

Circuit parameters:

$$I_D = 204.3 \mu\text{A}$$

$$\text{Power dissipation} = P_d = V_{DD}I_D = 0.3667 \text{ mW} < 5 \text{ mW}$$

$$\text{Output resistance or } R_{out}: f_c = \frac{1}{2\pi R_{out}C} \Rightarrow R_{out} = \frac{1}{2\pi f_c C} = 47,551.52 \Omega$$

$$\text{Transconductance or } g_m: A_v = g_m R_{out} \Rightarrow g_m = \frac{A_v}{R_{out}} = 0.00042 \text{ S} = 0.42 \text{ mS}$$

Design Procedure:

All MOSFET's of the cascode stage must be in saturation and same current must flow from all of them as we know for the transistors connected in series. Fixed L = 0.36u and variable W was taken for all the transistors.

1. m28 MOSFET or the bottommost NMOS was designed to supply around 0.2 mA current when input is applied to its gate through V_s .

2. m27 MOSFET or NMOS above m28 was designed to support 0.2 mA and saturation region. W was varied accordingly and was determined keeping V_{bias3} and 0.2 mA in mind.
3. m27 and m28 were connected to support the required current and saturation.
4. m26 MOSFET or PMOS above m27 was designed similarly to support 0.2 mA and saturation region. W was varied accordingly and was determined keeping V_{bias2} and 0.2 mA in mind.
5. m25 MOSFET or the uppermost PMOS was designed to complete the circuit and supply the required current. W was varied accordingly and was determined keeping V_{bias1} and 0.2 mA in mind. Power supply or V_{DD} of 1.8 V is applied.

Bias voltages i.e. V_{bias1} , V_{bias2} , V_{bias3} and V_{bias4} were calculated and achieved using trial, error and adjustments.

6. Body effect was considered for all the MOSFETs of the Cascode circuit.

For PMOS, body was connected to the power supply; $V_{DD} = 1.8$ V.

For NMOS, body was connected to the ground; GND = 0 V.

After designing each of the circuits individually i.e. Beta Multiplier Circuit, Cascode Current Mirror and Cascode Amplifier, they were joined together and tested once again and adjustments were made to cancel out the deliberate cascading effects thus achieving the desired design features.

MAGIC Procedure:

Technology file or channel length = $l = 180$ nm or 0.18u

Minimum block length = $\frac{l}{2} = 90$ nm or 0.09u

Therefore 4 blocks refers to 360 nm or 0.36u

Scale = 90 nm or 0.09u

Dimensions of MOSFETs used in MAGIC are as follows:

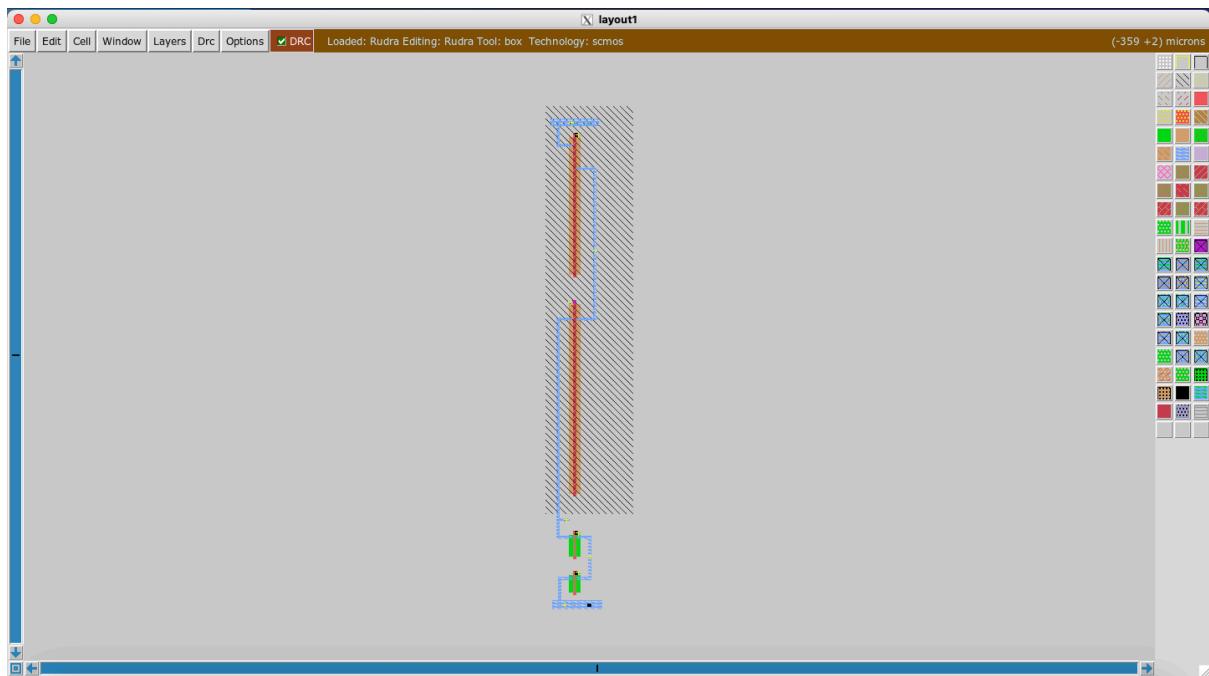
PMOS M25: Length = 4 blocks, Width = 26 blocks

PMOS M26: Length = 4 blocks, Width = 32 blocks

NMOS M27: Length = 4 blocks, Width = 216 blocks

NMOS M28: Length = 4 blocks, Width = 318 blocks

From .spice output, we can see that parasitic capacitance = 88.5 fF



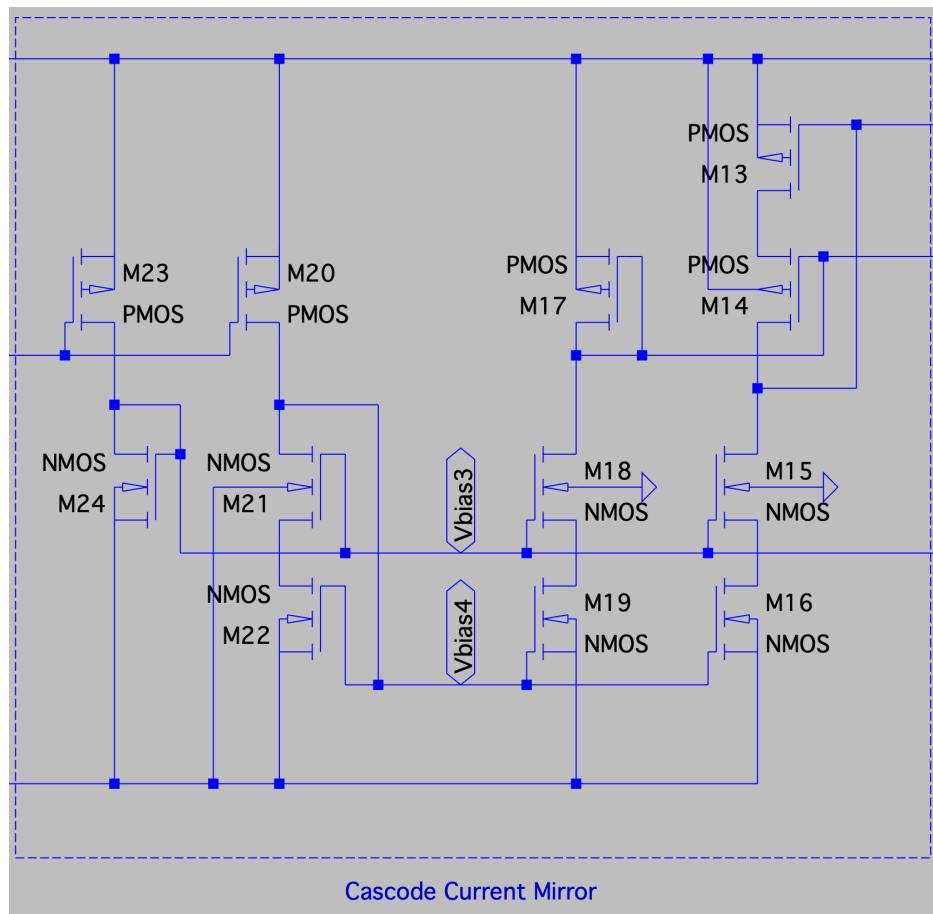
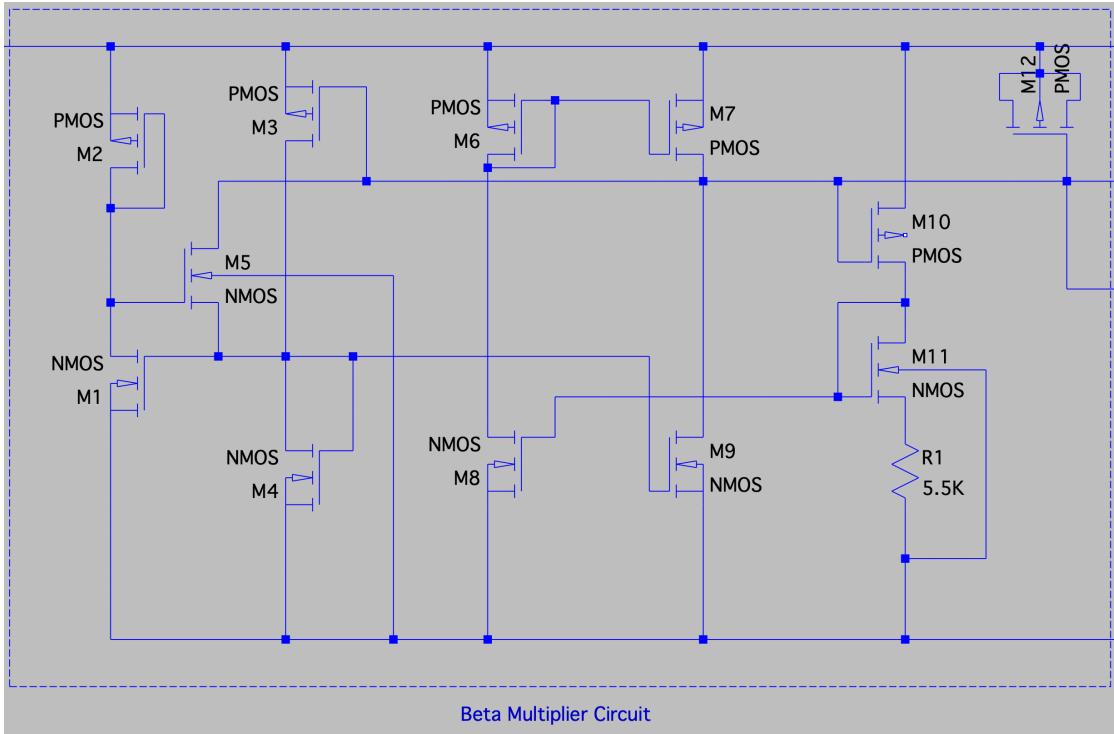
MAGIC Layout

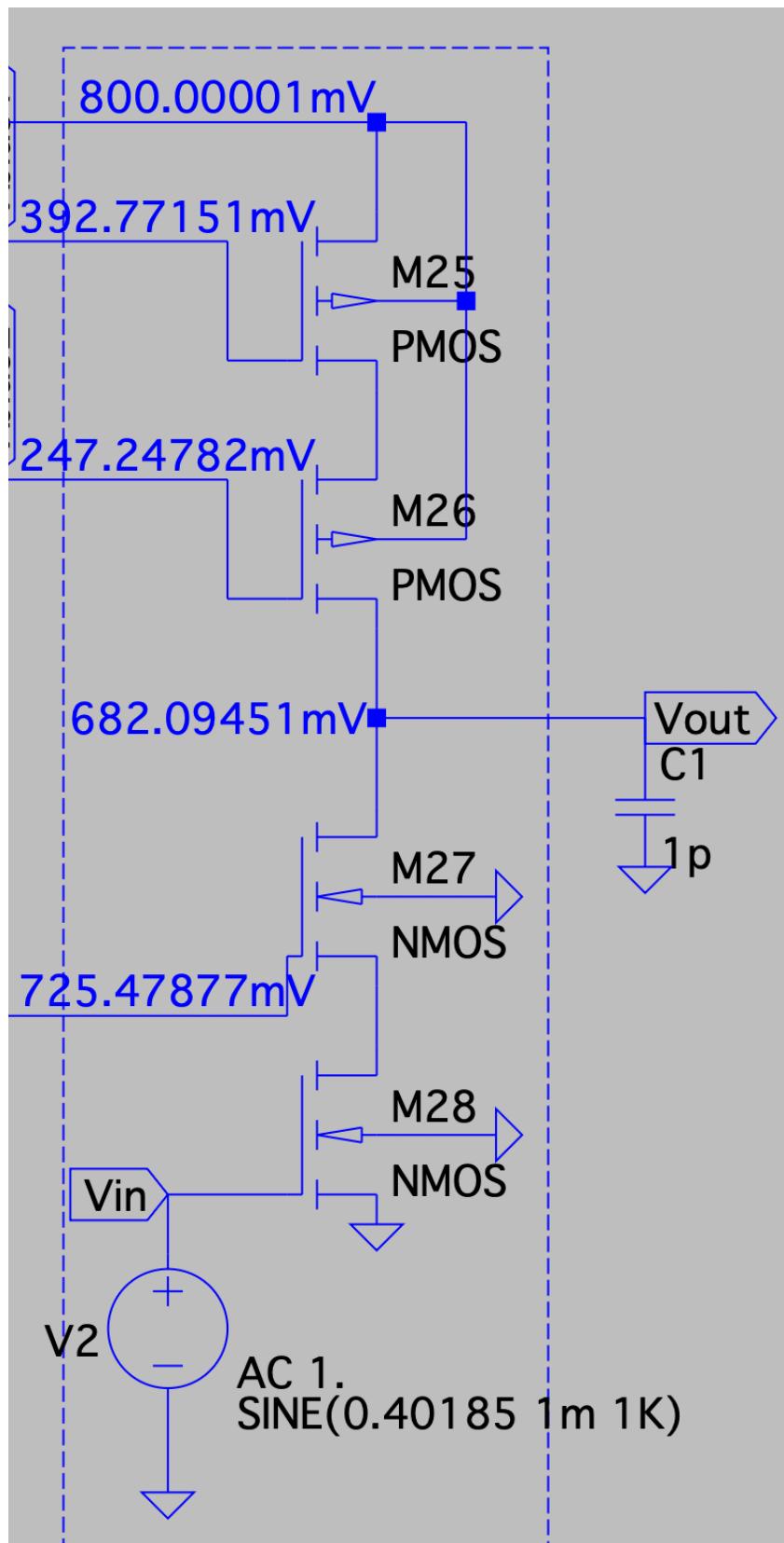
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* SPICE3 file created from Rudra.ext - technology: scmos
.option scale=90n

M1000 w1 Vbias2 Vout vdd pfet w=298 l=4
+ ad=2.09n pd=0.61m as=2.09n ps=0.61m
M1001 w3 Vbias3 Vout Gnd nfet w=32 l=4
+ ad=0.224n pd=78u as=0.224n ps=78u
M1002 w3 Vinpput gnd Gnd nfet w=26 l=4
+ ad=0.182n pd=66u as=0.182n ps=66u
M1003 w1 Vbias1 vdd vdd pfet w=216 l=4
+ ad=1.51n pd=0.446m as=1.51n ps=0.446m
C0 vdd 0 88.5f **FLOATING
```

.spice File Output

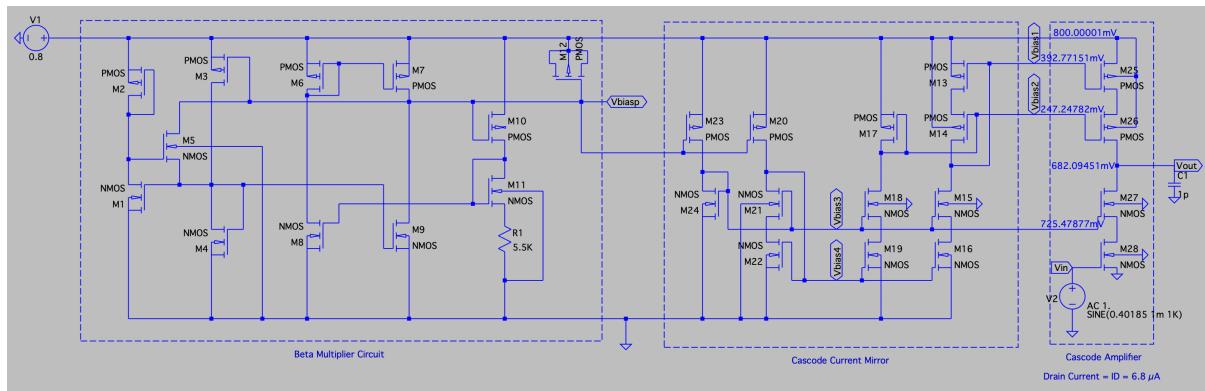
22 nm Technology Schematic Design



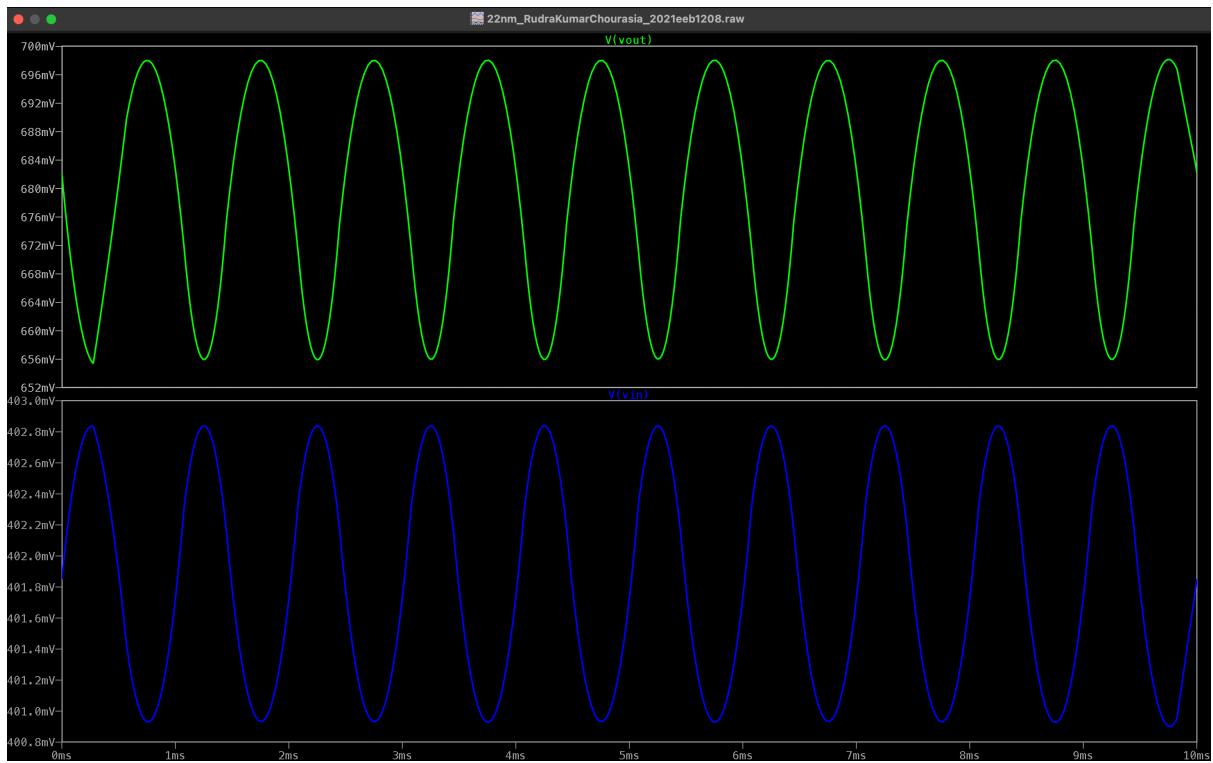


Cascode Amplifier

Drain Current = $ID = 6.8 \mu\text{A}$



Circuit Diagram



Output Waveform for $V_{in} = 1 \text{ mV}$ at 1 KHz

$$V_{bias,1} = 0.393 \text{ V}$$

$$V_{bias,2} = 0.247 \text{ V}$$

$$V_{bias,3} = 0.725 \text{ V}$$

DC Analysis:

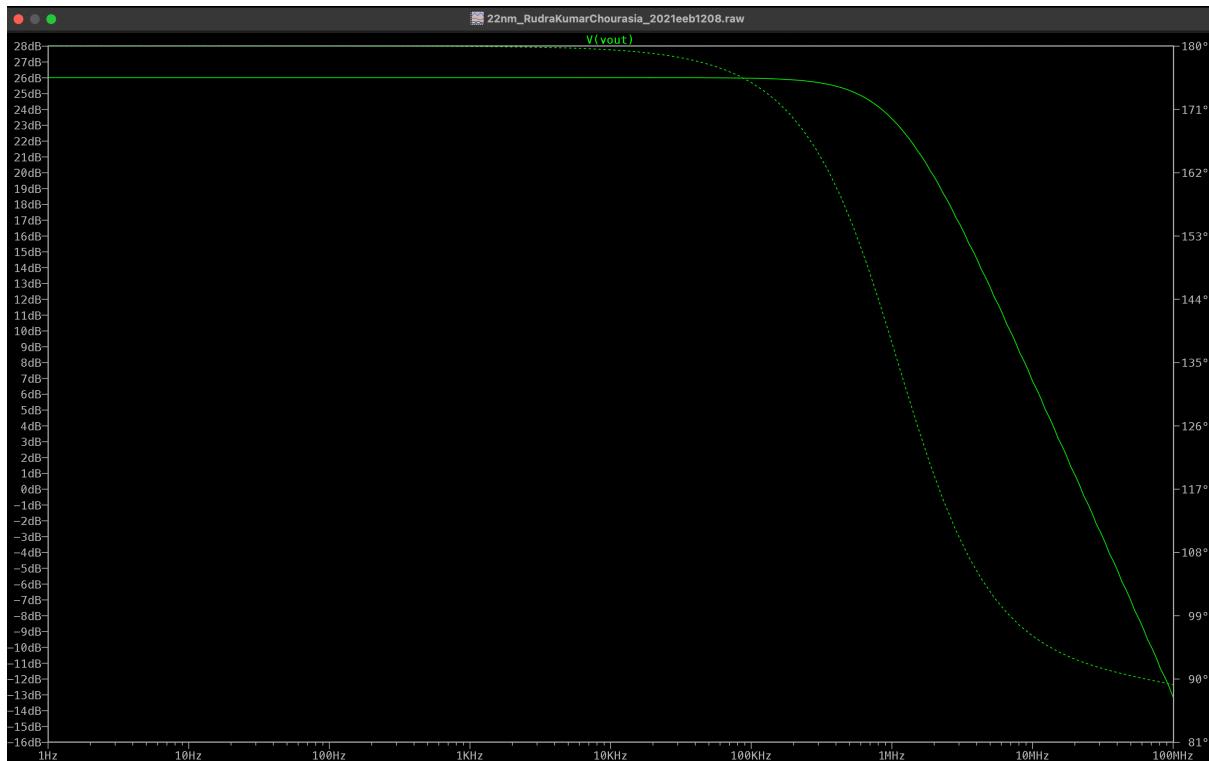
$$\text{DC offset} = 0.40185 \text{ V}$$

$$\text{Output voltage swing} = 698.041 \text{ mV} \text{ to } 655.991 \text{ mV} = 42.05 \text{ mV}$$

$$\text{Input (or signal) voltage} = 2 \text{ mV}_{pp}$$

$$\text{Required Gain} = 20$$

$$\text{Practical Gain} = \frac{\text{output voltage swing}}{\text{input voltage swing}} = \frac{42.05}{2} = 21.0251$$



Frequency Response

AC Analysis:

We are getting a **low pass filter** whose parameters are:

1. Gain = $A_v = 26 \text{ dB}$
2. Cut-off frequency or f_c (Bandwidth) = 856.66 KHz
3. Unity gain bandwidth (UGB) = 22.069 MHz

Circuit parameters:

$$I_D = 6.8 \mu\text{A}$$

$$\text{Power dissipation} = P_d = V_{DD}I_D = 5.44 \text{ mW} < 5 \text{ mW}$$

$$\text{Output resistance or } R_{out}: f_c = \frac{1}{2\pi R_{out} C} \Rightarrow R_{out} = \frac{1}{2\pi f_c C} = 1,85,785.42 \Omega$$

$$\text{Transconductance or } g_m: A_v = g_m R_{out} \Rightarrow g_m = \frac{A_v}{R_{out}} = 0.00011 \text{ S} = 0.11 \text{ mS}$$

Design Procedure:

Procedure of designing is same as that for 180 nm technology with only difference of supply voltage of 0.8 V instead of 1.8 V