Rudra Pratap Rohan

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EDUCATION

Manipal Institute of Technology **2021 – 2025**
B.tech ELectronics and Communication Engineering - ***CGPA - 8.29*** *Bengaluru, India*

COURSEWORK / SKILLS

- Signals & Systems
- Cadence
- Control Systems
- Digital System Design
- Low Power VLSI Design
- Antenna Design
- Analog Circuits
- Physical Design

PROJECTS

Voting machine using Xilinx FPGA | Verilog HDL **10 2022**

- Developed a voting machine using Hardware Description Language (HDL) and implemented it on an FPGA to simulate real-world election systems.
- Created two operational modes: Voting mode for casting votes for different candidates, and Tallying mode to display the total votes each candidate received.
- Successfully integrated a security feature by adding a key system through FPGA switches, ensuring secure voting and accurate tallying. The design worked flawlessly post code implementation on the FPGA.

Antenna Array for vehicular communication | CST studio SUITE **02 2024**

- Designed and implemented a high-performance antenna array for vehicular communication, aiming to enhance signal strength and reliability in various scenarios
- A microstrip patch antenna was designed in CST studio SUITE with various parameter.
- Design was tested and simulated in CST microwave studio ,Vehicle to Vehicle communication was aimed so that we avoid accidents on front on collisions or back on collisions.
- Enhanced data transmission rates by 2x , enabling faster and more reliable exchange of information between vehicles and infrastructure.

Digital Design and layout optimization using Cadence | Cadence Genus/Innovus **09 2024**

- Developed and implemented Euclid's GCD algorithm using Verilog, focusing on hardware optimization for efficient computation.
- Executed synthesis, placement, and routing of the design using Cadence Innovus, generating accurate physical layouts for the GCD circuit.
- Conducted comprehensive timing analysis and functional verification, ensuring design performance met timing constraints and adhered to hardware specifications.

INTERNSHIP

Maven Silicon **05 2024 – 07 2024**
Physical Design Trainee *Remote, India*

- Worked on the full VLSI design flow, including synthesis, placement, routing, and verification, using the Q-flow open-source during the physical design of a Serial Peripheral Interface (SPI).
- Performed critical verification processes like DRC, LVS, and STA to ensure the design met all timing and fabrication requirements.
- Automated design tasks using scripts and optimized design stages by analyzing log files to improve workflow efficiency.During this internship I implemented SPI PnR using Q flow.

TECHNICAL SKILLS

Languages: C/C++, Python, Verilog HDL ,ARM7,Tool command language(TCL)
Softwares Packages: Mentor Graphics, MATLAB, P-spice, AutoCAD, Xilinx Vivado ,CST microwave studio , code composer studio, Keil uVersion4 , LabView , Q-Flow ,Cadence Virtuoso/Innovus
Micro-controller boards: Arduino, Nexys Artix - 7 FPGA board , Raspberry pi , LPC2148 ,ESP32

CERTIFICATIONS

- Completed online B.Sc degree from IIT Madras in Data Science and Programming till foundational level.
- Programming for Everybody
- Introduction to packet Tracer by Cisco
- Networking Essentinals by Cisco