SYNERGY INSTITUTE OF ENGINEERING AND TECHNOLOGY, DHENKANAL
Near NH-55, Banamaliprasad – 759001
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
NBA ACCREDITED

SINCE 1999
SYNERGY
A Modern Day Gurukul

Assignment-I

Full Marks-40 **Duration- Within 1 Week from Notification**

Name- **Registration No-**

Subject with Code: Computer Organization and Architecture (CSPC2005)

Year & Semester: 2nd & IV

Course & Branch: B. Tech. & CSE
Academic Session: 2024-2025

Section-A
Answer All Questions

1. Define Program Counter ? **[2 marks] [CO1] [L2]**
2. What are the primary registers present in CPU? **[2 marks] [CO1] [L2]**
3. What does an instruction contain? **[2 marks] [CO1] [L2]**
4. Why is MAR connection with memory unidirectional? **[2 marks] [CO1] [L2]**

Section-B
Answer All Questions

1. Describe with diagram Von Neumann Architecture. **[6 marks] [CO1] [L2]**
2. Differentiate Big Endian System and Little Endian System. **[6 marks] [CO1] [L2]**

Section-C
Answer All Questions

1. Discuss different types instruction formats with example. **[10 marks] [CO1] [L2]**
2. List the instructions using one-address instruction for the below mentioned example.

   X= (A*B)+(C*D), where A,B,C,D & X are memory locations **[10 marks] [CO1] [L2]**

Additional Questions

1. Describe the different functional units of computer?
2. Draw the connection diagram between memory and processor.
3. Write the Register Transfer Notation for the following instruction

   Add R1,R2,R3

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Assignment-II

Full Marks-40 **Duration- Within 1 Week from Notification**

Name- **Registration No-**

Subject with Code: Computer Organization and Architecture (CSPC2005)

Year & Semester: 2nd & IV

Course & Branch: B. Tech. & CSE
Academic Session: 2024-2025

Course Outcome	Total Marks	Marks Secured	Signature of Evaluator
CO2	40		
Level	Total Marks	Marks Secured	
L1-L3			
L4-L6			

Section-A
Answer All Questions

1. What is locality of reference? **[2 marks] [CO2] [L2]**
2. What is μPC? **[2 marks] [CO2] [L2]**
3. What is the use of **WMFC** control signal? **[2 marks] [CO2] [L2]**
4. What is the difference between memory access and memory cycle time? **[2 marks] [CO2] [L2]**

Section-B
Answer All Questions

1. Explain the conversion of **virtual address** to **physical address**. **[6 marks] [CO2] [L2]**
2. Explain the main memory address format in **direct**, **associative** & **set associative** mapping. **[6 marks] [CO2] [L2]**

Section-C
Answer All Questions

1. Differentiate between write through and write back policies with example. **[10 marks] [CO2] [L2]**
2. **ADD (R3), R1**
   Describe the machine instructions of the above instruction using one bus organization with diagram
   [10 marks] [CO2] [L2]

Additional Questions

1. What is cache memory?
2. What is control store?
3. Explain the two approaches for generating control signals.

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Assignment-III

Full Marks-40 **Duration- Within 1 Week from Notification**

Name- **Registration No-**

Subject with Code: Computer Organization and Architecture (CSPC2005)

Year & Semester: 2nd & IV

Course & Branch: B. Tech. & CSE
Academic Session: 2024-2025

Course Outcome	Total Marks	Marks Secured	Signature of Evaluator
CO3	40		
Level	Total Marks	Marks Secured	
L1-L3			
L4-L6			

Section-A
Answer All Questions

1. What are the classification of data hazards? **[2 marks] [CO3] [L2]**
2. How data hazard can be prevented in pipelining? **[2 marks] [CO3] [L2]**
3. State different types of hazards that can occur in pipeline. **[2 marks] [CO3] [L2]**
4. What are Hazards? **[2 marks] [CO3] [L2]**

Section-B
Answer All Questions

1. Differentiate between vector and array processor **[6 marks] [CO3] [L2]**
2. Explain operand forwarding with an example. **[6 marks] [CO3] [L2]**

Section-C
Answer All Questions

1. Differentiate between RISC and CISC **[10 marks] [CO3] [L2]**
2. Explain Flynn's classification in detail **[10 marks] [CO3] [L2]**

Additional Questions

1. Explain pipelining with example.
2. Differentiate between tightly coupled and loosely couple MIMD.
3. Explain cache coherence.

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Assignment-IV

Full Marks-40 **Duration- Within 1 Week from Notification**

Name- **Registration No-**

Subject with Code: Computer Organization and Architecture (CSPC2005)

Year & Semester: 2nd & IV

Course & Branch: B. Tech. & CSE
Academic Session: 2024-2025

Course Outcome	Total Marks	Marks Secured	Signature of Evaluator
CO4	40		
Level	Total Marks	Marks Secured	
L1-L3			
L4-L6			

Section-A
Answer All Questions

1. What is the advantage of using Booth algorithm? **[2 marks] [CO4] [L2]**
2. Write the algorithm for restoring division **[2 marks] [CO4] [L2]**
3. Write the algorithm for non-restoring division. **[2 marks] [CO4] [L2]**
4. In floating point numbers when so you say that an underflow or overflow has occurred? **[2 marks] [CO4] [L2]**

Section-B
Answer All Questions

1. Generate bit pair recoding of 11010. **[6 marks] [CO4] [L2]**
2. Using restoring division method, divide 8 by 3. **[6 marks] [CO4] [L2]**

Section-C
Answer All Questions

1. Using non-restoring division method, divide 8 by 3. **[10marks] [CO4][L2]**
2. Carry out multiplication of below two numbers using booth algorithm.

   (+13)x(-6) **[10marks] [CO4][L2]**

Additional Questions

1. Explain normalization of floating point numbers.
2. Differentiate between single and double precision floating point numbers..
3. Explain fast multiplication using bit pair recording..