Section-A: Answer All Questions

1. **What is locality of reference?**
   Locality of reference refers to the tendency of a program to access a relatively small portion of its address space at any given time. It can be temporal (repeating access to the same memory) or spatial (accessing memory locations near recently accessed ones).

2. **What is µPC?**
   µPC (Microprogram Counter) holds the address of the next microinstruction to be executed in a control memory during microprogrammed control.

3. **What is the use of WMFC control signal?**
   WMFC (Wait for Memory Function Complete) is a control signal used to pause the CPU until the memory completes the requested operation, ensuring synchronization between CPU and memory.

4. **What is the difference between memory access and memory cycle time?**
    - **Memory access time** is the time taken to access data from a memory location.
    - **Memory cycle time** is the minimum time required between two successive memory operations (accesses), usually longer than access time.

Section-B: Answer All Questions

1. **Explain the conversion of virtual address to physical address:**
   The **virtual address** generated by the CPU is translated to a **physical address** using a Memory Management Unit (MMU). The most common method is paging, where the virtual address is divided into a page number and offset. The page number is mapped to a frame number in the page table, and the physical address is formed by combining the frame number and offset.

2. **Explain the main memory address format in direct, associative & set associative mapping:**

   - **Direct Mapping:**
     Physical Address = (Tag + Line Number + Word)
     Each block maps to only one cache line.

   - **Associative Mapping:**
     Physical Address = (Tag + Word)
     Any block can be placed in any cache line.
     Cache stores tags and searches all lines in parallel.

   - **Set-Associative Mapping:**
     Physical Address = (Tag + Set Number + Word)
     Cache is divided into sets; each set contains several lines. A block maps to a specific set but any line in that set.

Section-C: Answer All Questions

1. **Differentiate between write through and write back policies with example:**

Feature	Write Through	Write Back
Update method	Updates both cache and memory simultaneously	Updates only cache; memory updated later
Speed	Slower due to memory write every time	Faster as memory writes are reduced
Example	Writing 5 to X updates both cache and RAM	Writing 5 to X updates only cache, RAM is updated on block replacement

2. **ADD (R3), R1 – Describe the machine instructions using one-bus organization with diagram:**

   Instruction: `ADD (R3), R1`
   Meaning: Add the value at the memory location pointed to by R3 to R1.

   Sequence (One-bus organization):

   a. MAR ← R3 (Place address from R3 into Memory Address Register)

   b. Read memory → MDR (Memory Data Register)

   c. TEMP ← MDR (Temporary register stores memory value)

   d. R1 ← R1 + TEMP

   Diagram includes:

   - One common bus
   - ALU, Registers (R1, R3), MAR, MDR, Control Unit
   - Control signals orchestrating read/write operations via the bus