1. What are the classification of data hazourds? are Classification of Data Hazards: · Read After Write (RAW) · Write After Read (WAR) Wreite Affer Wreite (WAW) 2. How to Preevent Data Hazards in Pipelining! operand forwarding (data forwarding) · Instruction recordering 2000000 [100001] · Pipeline Stalling (Inserting NOPs)

3. State different types of hazards that can occur in Pipeline 1000000 : 2011 bonilogia.

are Types of Hazards in Pipelines: Ula significant

- · Pata hazards
- · Control hazarras prostrusto bourson , 6
- Grutural Hazords of how.
- 4. What are Hazards? Blooming tugters pallons
- ang. Hazareds are Problems that Prevent the next Instruction in the Pipeline from enecuting during its designated clock cycle.

institution a without worthout.

Section-B

1. Differentiate between vector and array

Processor.

ans Vector vs Arcray Processor : 1000

- · Vectore Precessore: Operates on entirce Vectores Cararays) with a single instruction
- elements working to Parallel on different data.
- Pipelined Alus; arcray Processores USE multiple Alus simultaneously.
- 2. Operand forewareding Emample:
 - Sending output directly from one Pipeline Stage to another.
- Enample: If instruction I computes RI=
 R2+R3, and instruction 2 uses RI,
 operand forwarding sends RI's value to
 instruction 2 without waiting.

- Sec C 1. Differcontiate between RISC and CIBC.
 - · RISC (Reduced Instruction Set Computer): Simple Instructions, fast enecution, fined Instruction length. 20020000 019 Him amin -
 - CISC (Complete Instruction Set Computer): Complem instructions, fever instructions Per Program, variable length.
- 2. Emplein Flynn's classification in details ons flynn's classification!
 - · SISD: Single Instruction Single Data.
 - · SIMD: single Instruction multiple Data.
 - · MISD: multiple Instruction single Data (Rarce).
 - · mimp: multiple instruction multiple.

Douta (most moderan processores)

- SISD: one Processor enecutes a single Instruction on a single Duta Structum. En: Treaditional uniprocessor systems.
- SIMD: One instruction is applied to multiple douta elements in parcallel.

an: GPUs, Vector processors.

MISD: multiple processores emecute different the Source douta stroom instructions on (marroly used) ? nothinited bombogs self. Gris fault - tolercant - Systems. 2001 1) milen signif mimp: multiple processores enecute différent instructions on different doctor independently. an: multi-care processores chesters. Progress, variable length. 8. Fourpleis Physics Chouse Figurtion in destrois instrablissalis simple sin s sist sigle instruction sigle tooks. . Simple Instruction mustiple Date. misto: markiple brishauchien sirry be recida (reme). algitum. doitement orgitum : arain . boda (most brodown processors) THEOR STORES CONSTRUCTS OF STREET Mostria et en e ente Date Staram. On Treaditional criperocesson systems. almos one instruction is applied to multiple deter Cherny is in Parcolles. APPL Water more series.