1. Define Prægram Counter:

one The Progream Counter (PC) is a register in the CPU that holds the olddross of the nent instruction to be enecuted.

a. What care the preimary rugistores prosent

ans Preimarcy CPV registores include the Progream Countere (Pe), Accumulatore (ACC). Instruction Registers (IR), memory Address Register (MAR), and memorry Buffer Register CMBR2.

3. What does an Instruction contour? ans An Instruction typically contains an opcode (opercoution code) and operconds (doctor one addresses used in the operation),

4. Why is mar connection with memory unidirectional

ans: The mar (memory Address Register) Sends addresses to memory, but does not receive deuta back, hence the connection is unidirectional value is stored at 12 lever significant legte store

order order prost Squilliant > 0x31 Stoned at Lawere

some exila stance at hower 1-> Common 10. hitper Forer comm.

9000 ti Lixing Copy

Action of Supplements

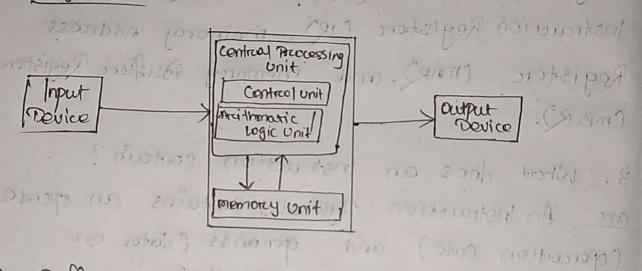
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Sec-B

Describe with Diagram Von Neumann Architecture:

and the Non Neumann Architecturce consists of a Single memory space for both instruction and data. It includes a apr covith ALU, cu reegisters), memory, and 1/0 units connected N'a busos.

Diagram: Loturison A (09) Sisting



2. Differentiate Big Endian System and Little Phalan Systems:

Big Endicun System

Little Endian Systom

Definition: In little Andian the loost -> Definition: In Big-endian, the most significant byte (MSB) of a multi-byte Value is storced at the Lowest memorcy address. -> Byte ardon: most significant -> 0x34 storced out lower > en: 0 x12 storred at Lower

> usago: used in some

Network Pow to cols

andress

> Least significant byte storced firest. address

-> common in Inter Processon.

Significant byte (LSB) of a multi-

byte value is stored at the

lowest memory address.

*A = 323 : 19m3下 (Patr) 1. Discuss different types of instruction.

foremore with enample:

· Zerco - address: Used in Stack - housed

Emaniple: ADD Coperatos on top two Stack architecturus. elements).

· One - addriess: Uses accumulatore and one operand.

Enample: LOAD A ADD B STORE C

· Two-address: Specifies two operands. Emample: ADD A, B (A = A+B).

- · Three address: Uses three operconds: Conample: ADD A, B, C (A=B+C).
- 2. List the Instructions using one- address instruction for 1 = (A*B) + (C*D):

eme Asseming accumulatore - bossed one-address "instractions :

LOAD A ; ACC = A

MULB; ACC = A*B

STORE TEMP1; TEMP = A*B

LOAD C; ACC = C

mul D; Acc = C*D

STORE TEMP2; TEMP2 = C+D

```
LOAD TEMPT; ACC = A*B
    ADD TEMP2; ACC = (A*B)+ (C*D)
    STORE X; X = (A*B)+ (C*D) = Domino
      osd - Adole all bood is south a cook - head
                              CHECKING CHURNES
 Foresight: ADD Copenation on Jop too Stack
                                     Cotogonala
   · Con - ouddicess: Use's occumulations sond.
                               one equiand.
                       Conduction (CAD) A
                       · . & GOR
     Two addiness: Specifics that exerciseds.
            Enough: 400 4, 13 (1) 4116).
   " There addiness there openeds.
            Commence: 400 10, 6 (11:12+ 1).
a list the premier chions coing one address.
         Parshoughton for /= (4 15) + (1775):
me description occumulations bouse a cope address
                               . 1. 2001 hour 1818
                            HEDDA ! HOOD!
                       8 * A = 20 A - 31 1911
                  8108 . Wolf : Make . 11 . Bols
                       1 2 3 3 A : 3 GM31
                       C*) - SOM OF JUM
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