EE 599 Spring 2020 Homework 1 Report

Github repo link: https://github.com/RudrenduMahindar/EE599 mahindar 6343999513

1. Images for Odd-even transposition sort have been attached below:

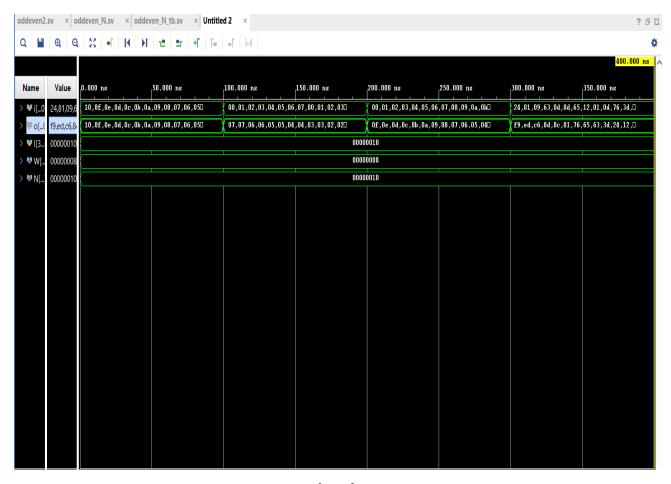


Fig1: Waveform for N=16

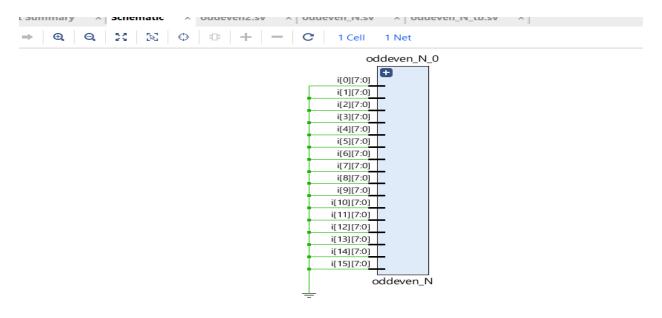


Fig2: Schematic screenshot of module for N=16

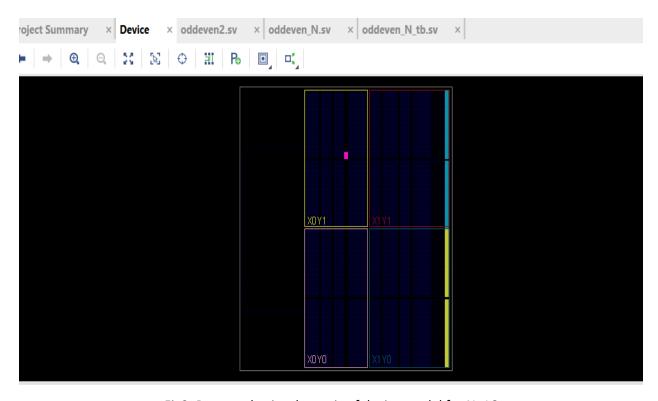


Fig3: Post synthesis schematic of device model for N=16

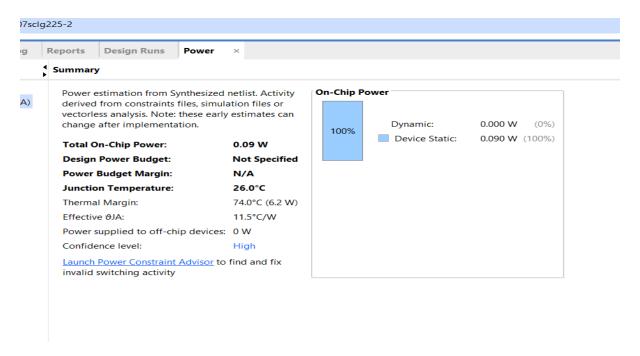


Fig4: Power estimation for N=16

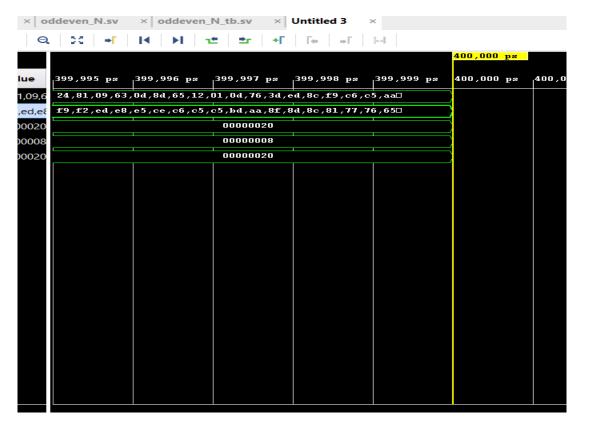


Fig5: Waveform for N=32

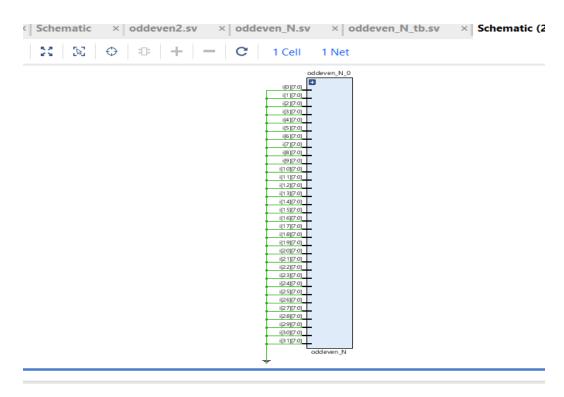


Fig6: Schematic screenshot of module for N=32

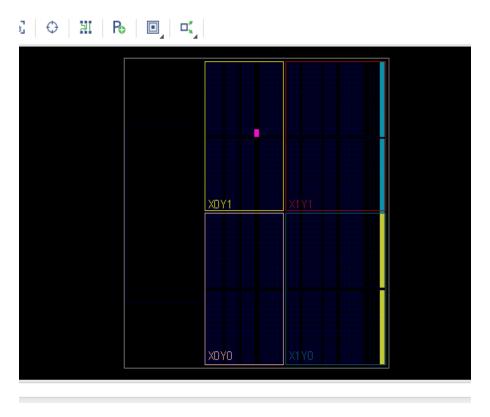


Fig7: Post synthesis schematic of device model for N=32

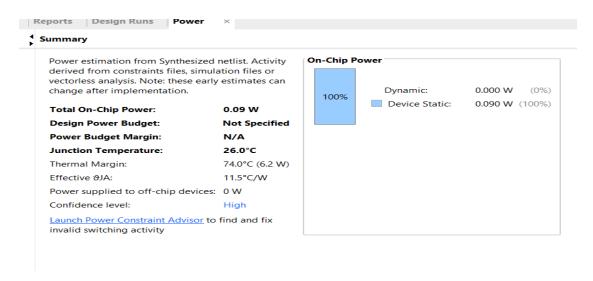


Fig8: Power estimation for N=32

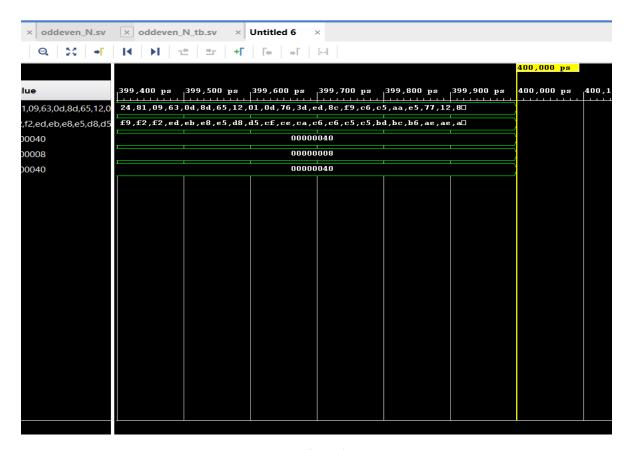


Fig9: Waveform for N=64



Fig10: Post synthesis schematic of device model for N=64

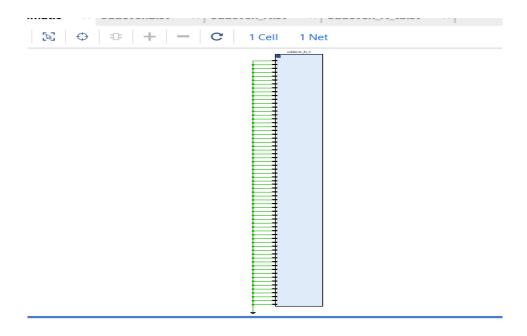


Fig11: Schematic screenshot of module for N=64

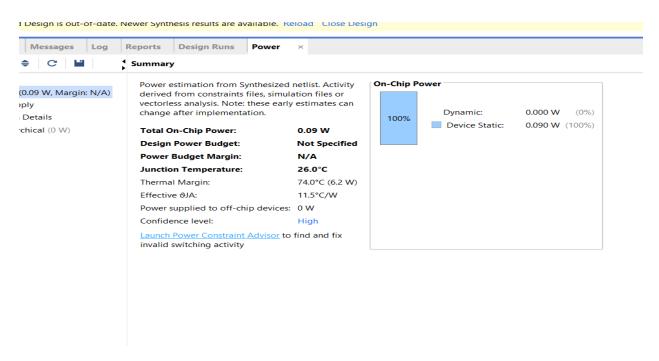


Fig12: Power estimation for N=64

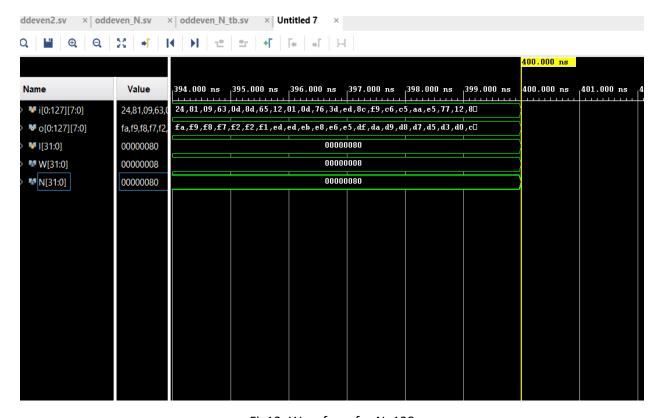


Fig13: Waveform for N=128

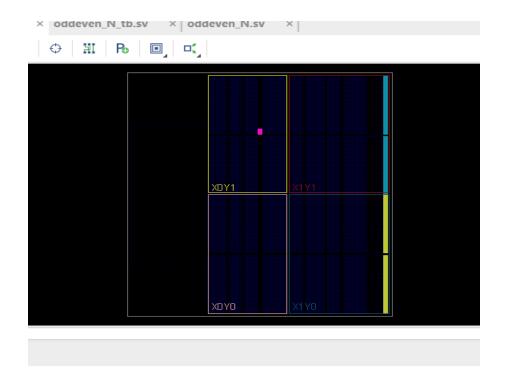


Fig14: Post synthesis schematic of device model for N=128

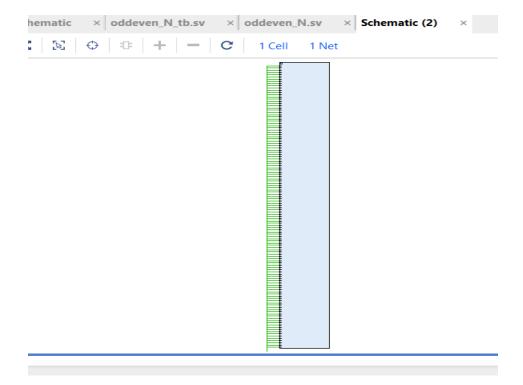


Fig15: Schematic screenshot of module for N=128

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.09 W

Design Power Budget: Not Specified

Power Budget Margin: N/A
Junction Temperature: 26.0°C

Thermal Margin: 74.0°C (6.2 W)
Effective ϑJA : 11.5°C/W

Power supplied to off-chip devices: 0 W
Confidence level: High

<u>Launch Power Constraint Advisor</u> to find and fix

invalid switching activity

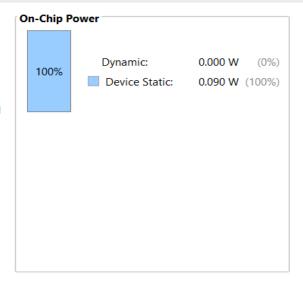


Fig16: Power estimation for N=128