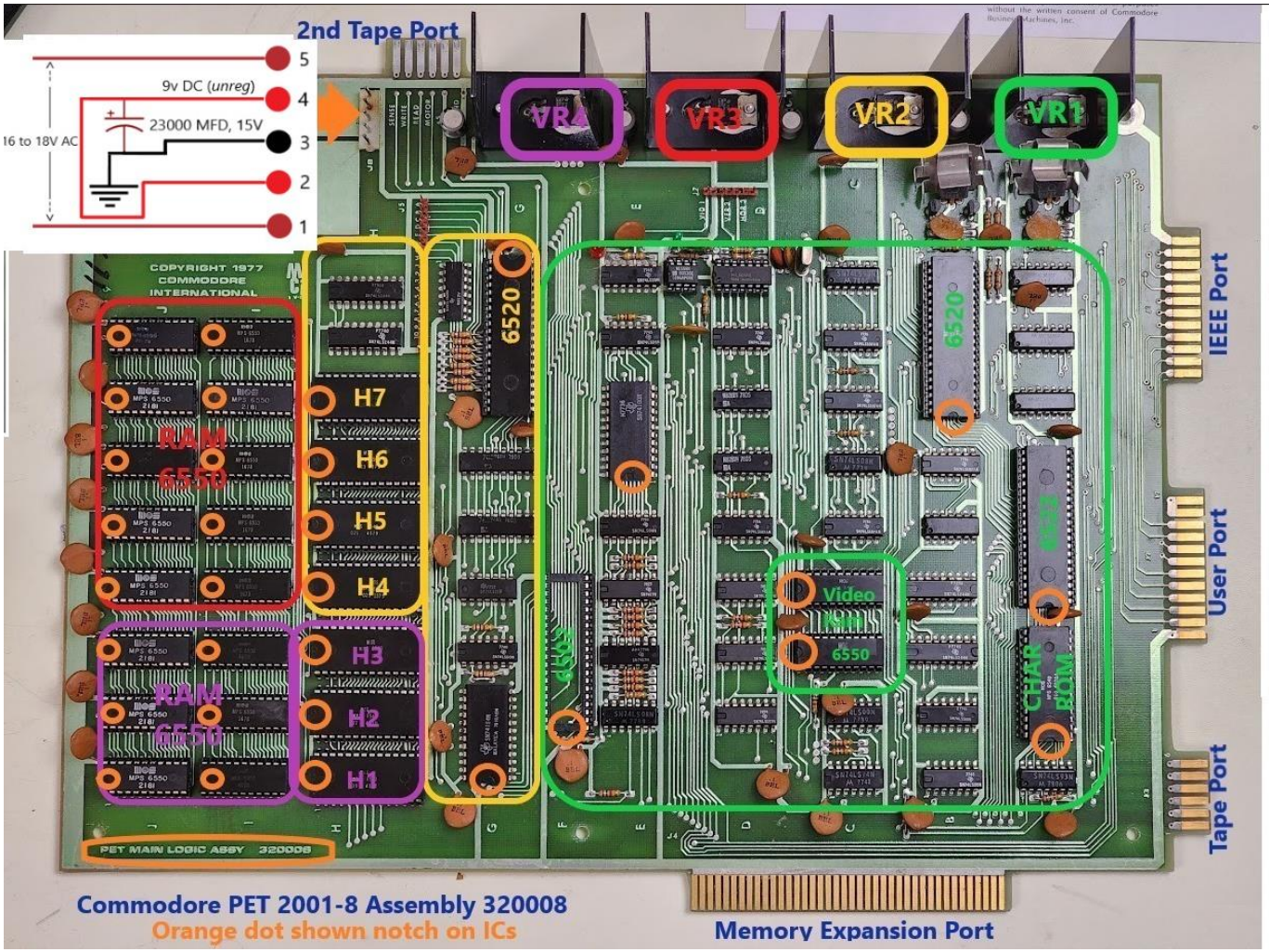
Commodore PET 2001-8 Assembly 320008 Board



PET 2001 (1977 motherboard) Assembly #320008

- PIA#1 controls Cassette I/O, Cassette\Tape #1
- PIA#2 is use ONLY for the IEEE port.
- 6522 is used for the User port and the Cassette\Tape #2
- The EDIT ROM is used for the Keyboard matrix and some other model specific differences.
- On the 2001-8 Video section of the board is all hard coded.
- On later PETs with the CRTC, the EDIT does the CRTC initialization for 40/80 columns etc. and it also run the startup chime.

MOS ROM is 6540. 6550 is RAM. (Character ROM A2)
H4 and H7 are linked and can be replaced by a single 4K ROM in H4
H1/H5 and H2/H6 are similarly linked so that a single 4K ROM can replace two 2K ROMs.
These 4K ROMs weren't available until Basic Level 3

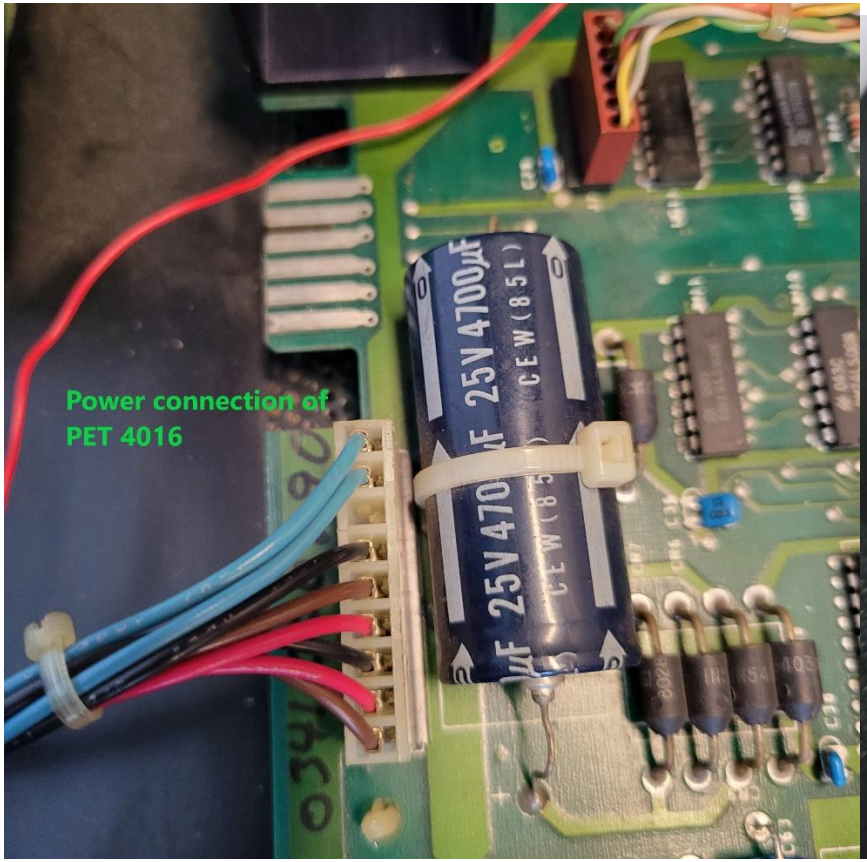
IC Description and Model

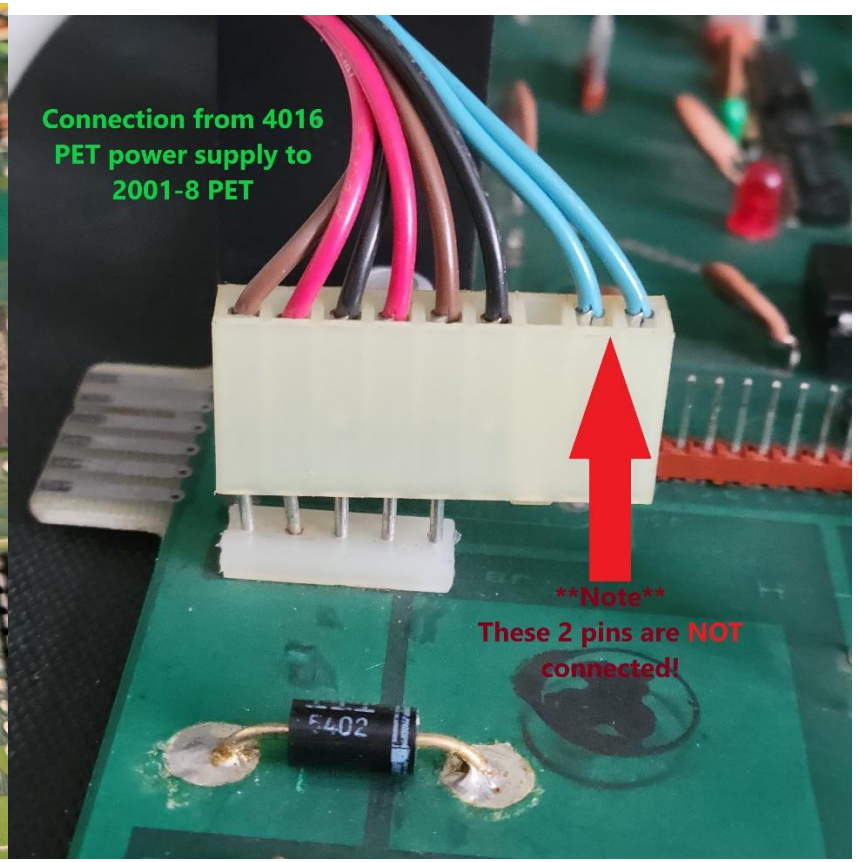
- CPU - 6502
- PIA#1 - 6520
- PIA#2 - 6520
- VIDEO RAM - 6550
- User Port - 6522
- SYSTEM RAM- 6550
- SYSTEM ROM- 6540 (H1-H7)
- CHAR ROM - 6540 A2

ROM 2.0 - Basic Level II - 28 pin ROM type 6540 - Series 2001

Location	ROM #	Part Number	
H1	6540–019	901439–09	BASIC
H2	6540–013	901439–02	BASIC
H3	6540–015	901439–03	EDIT ROM
H4	6540–016	901439–04	KERNAL
H5	6540–012	901439–05	BASIC
H6	6540–014	901439–06	BASIC
H7	6540–018	901439–08	KERNAL
A2	6540–010	901439–01	Character ROM

https://www.youtube.com/@RudysRetroIntel
https://www.youtube.com/@HutchCA


Power connection of
PET 4016
25V 4700µF
CEW(85L)


Connection from 4016
PET power supply to
2001-8 PET
Note
These 2 pins are NOT
connected!
5402

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NMOS

MPS
6522
VERSATILE
INTERFACE
ADAPTER

6522 VERSATILE INTERFACE ADAPTER

PERIPHERALS

DESCRIPTION

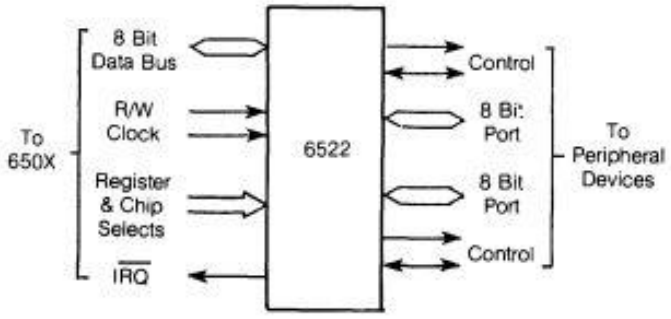
The 6522 Versatile Interface Adapter (VIA) provides all of the capability of the 6520. In addition, this device contains a pair of very powerful interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. Also, several peripheral I/O lines can be controlled directly from the interval timers for generating programmable-frequency square waves and for counting externally generated pulses. To facilitate control of the many powerful features of this chip, the internal registers have been organized into an interrupt flag register, an interrupt enable register and a pair of function control registers.

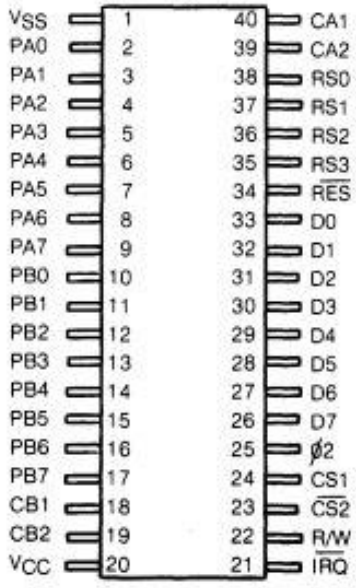
FEATURES

- Very powerful expansion of basic 6520 capability.
- N channel, depletion load technology, single +5V supply.
- Completely static and TTL compatible.
- CMOS compatible peripheral control lines.
- Expanded "handshake" capability allows very positive control of data transfers between processor and peripheral devices.

6522 Interface Diagram



6522



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NMOS

MPS
6520
PERIPHERAL
ADAPTER

6520 PERIPHERAL ADAPTER

PERIPHERALS

DESCRIPTION

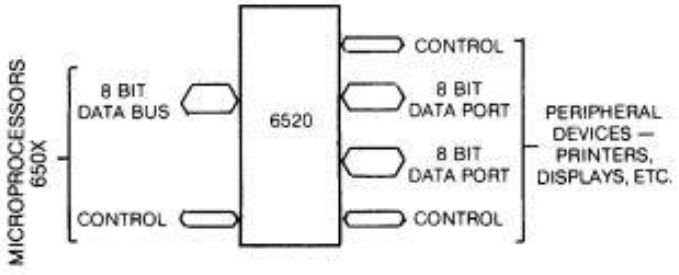
The 6520 Peripheral Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the 6500 family of microprocessors, the 6520 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.

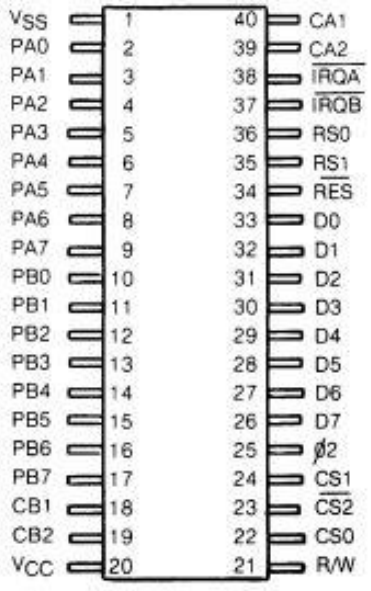
FEATURES

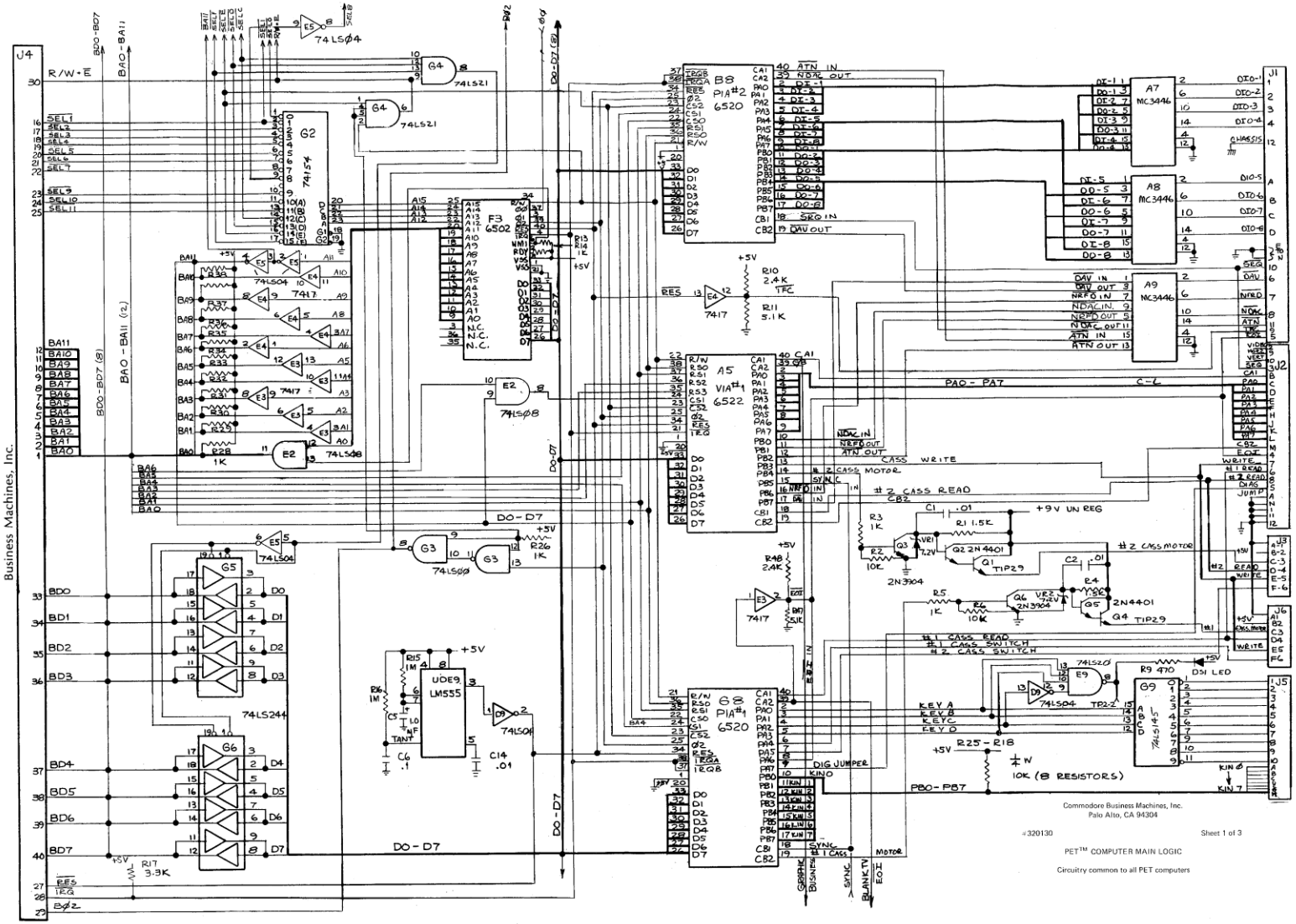
- High performance replacement for Motorola/AMI /MOSTEK/Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows very positive control of data transfers between processor and peripheral devices.

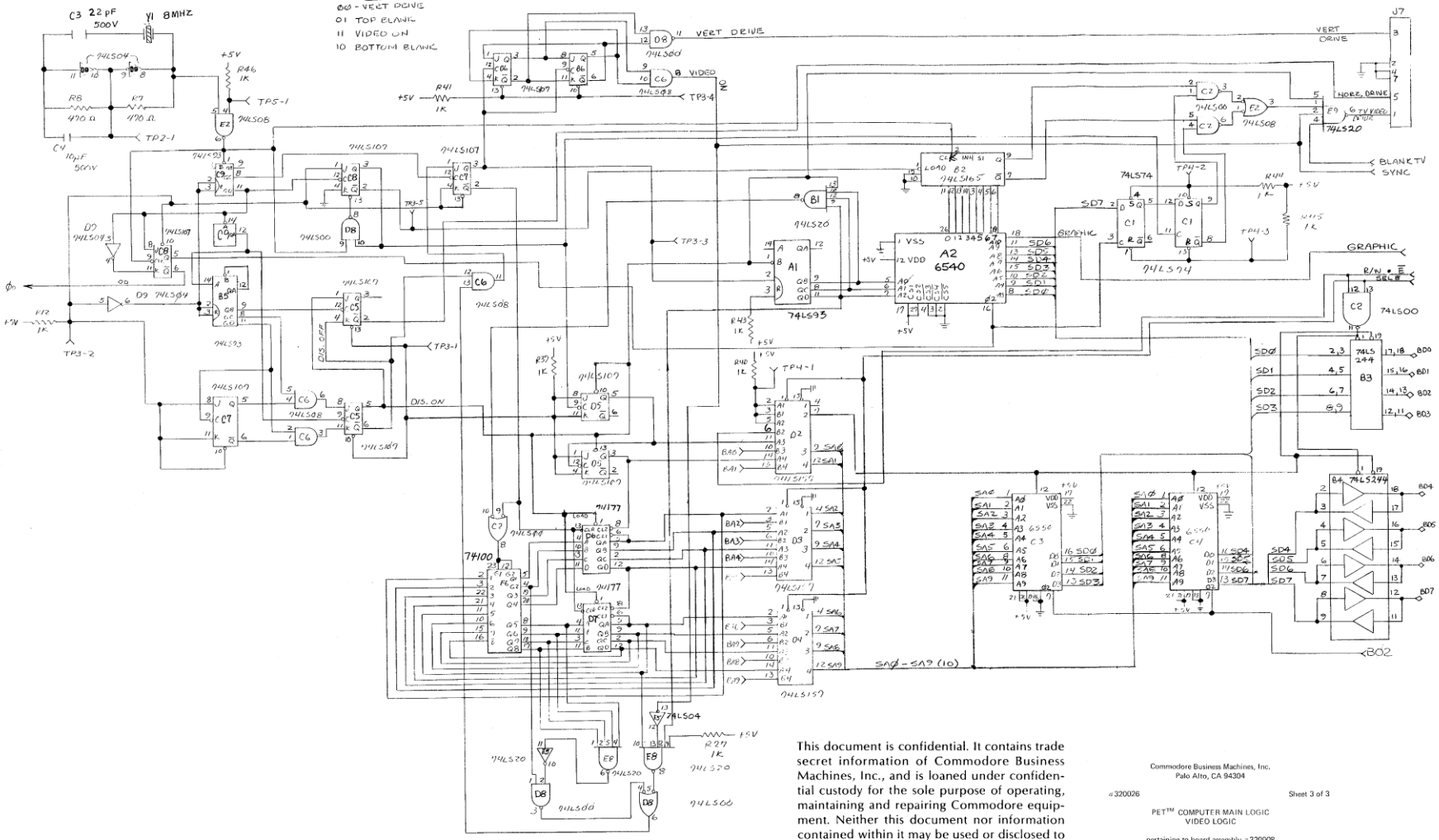
Basic 6520 Interface Diagram



6520







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Palo Alto, CA 94304

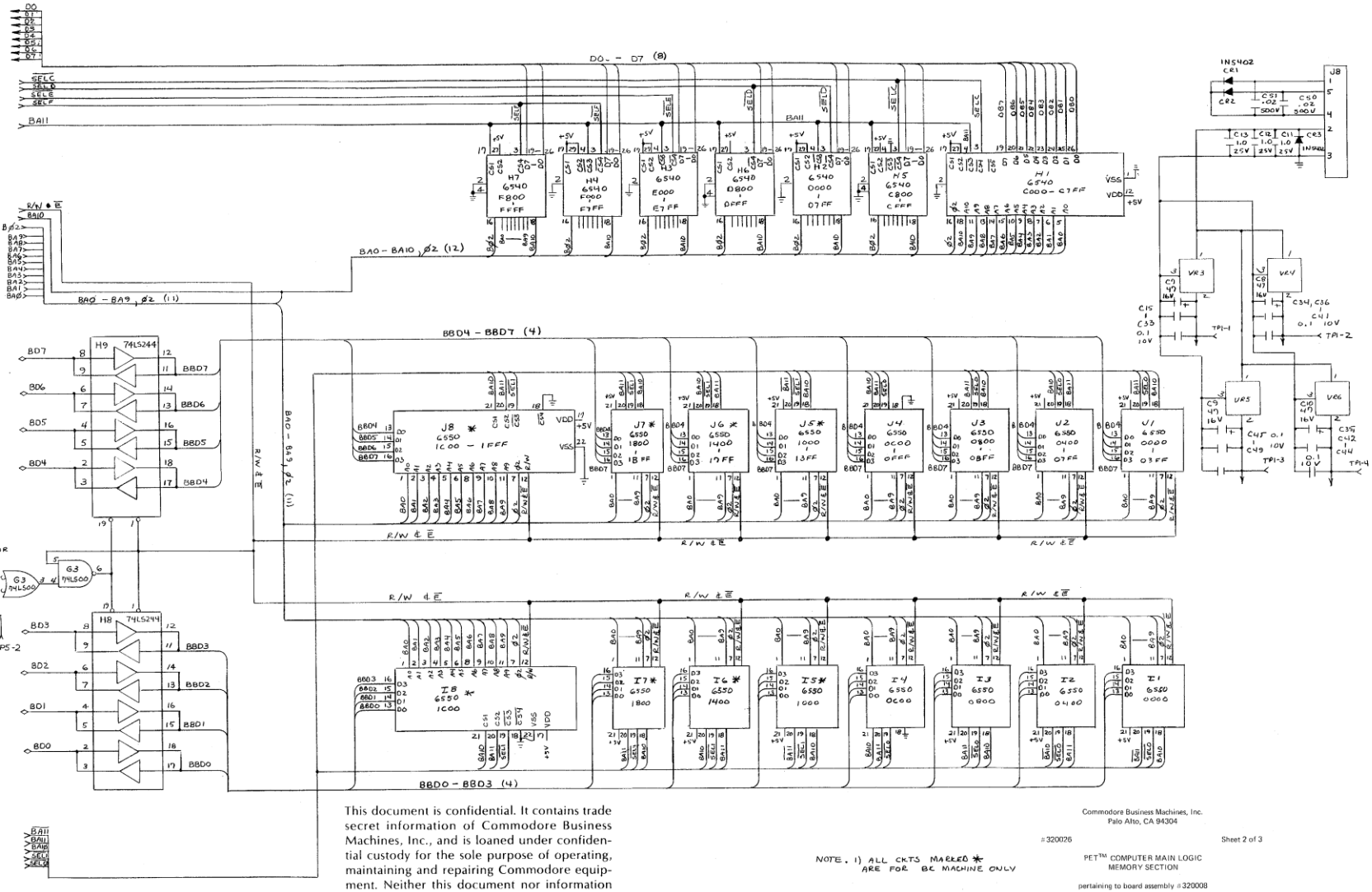
≠320026 Sheet 3 of 3

PET™ COMPUTER MAIN LOGIC
VIDEO LOGIC

pertaining to board assembly ≠320008

NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320081, 320137, 320008.

The identifying board number is in upper left corner.



NOTE. 1) ALL CKTS MARKED * ARE FOR 8K MACHINE ONLY

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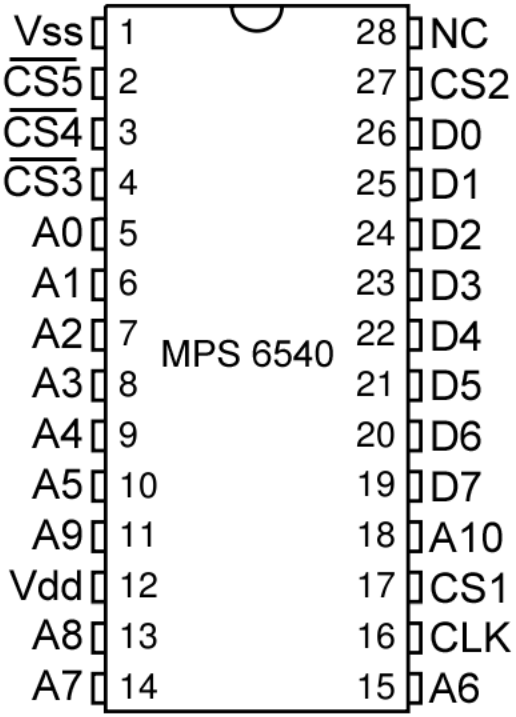
#320026 Sheet 2 of 3

PET™ COMPUTER MAIN LOGIC
MEMORY SECTION

pertaining to board assembly #320008

NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320083, 320137, 320008.

The identifying board number is in upper left corner.


Vss 1
CS5 2
CS4 3
CS3 4
A0 5
A1 6
A2 7
A3 8
A4 9
A5 10
A9 11
Vdd 12
A8 13
A7 14
MPS 6540
28 NC
27 CS2
26 D0
25 D1
24 D2
23 D3
22 D4
21 D5
20 D6
19 D7
18 A10
17 CS1
16 CLK
15 A6