Commodore PET 2001

2nd Tape Port

VR6 VR5 VR4 VR3

J8
16-18v AC
~9VDC (unreg)
23000 MFD

6550 RAM

H7
H6
H5
H4

6520
PIA#1

6502

6550 RAM

H1

6520
PIA#2

6522

6550 VIDEO RAM

CHAR ROM

IEEE Port

User Port

Tape Port

Memory Expansion Port

Red dot = IC orientation

PET 2001 (1977 motherboard) Assembly #320008

- PIA#1 controls Cassette I/O, Cassette\Tape #1
- PIA#2 is use ONLY for the IEEE port.
- 6522 is used for the User port and the Cassette\Tape #2
- The EDIT ROM is used for the Keyboard matrix and some other model specific differences.
- On the 2001-8 Video section of the board is all hard coded.
- On later PETs with the CRTC, the EDIT does the CRTC initialization for 40/80 columns etc. and it also run the startup chime.
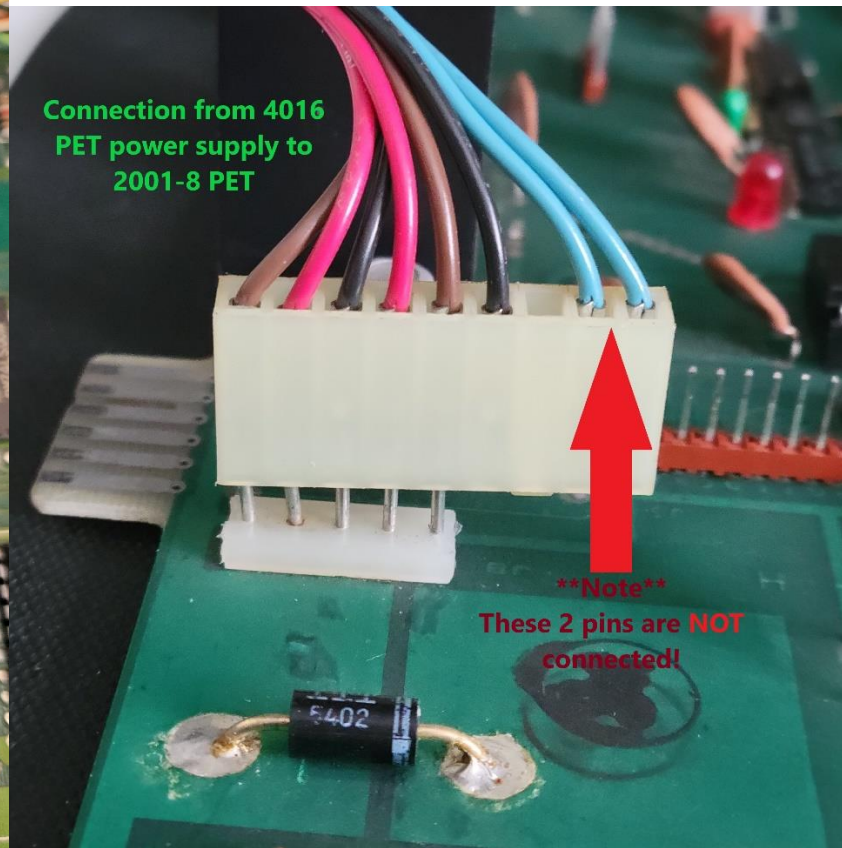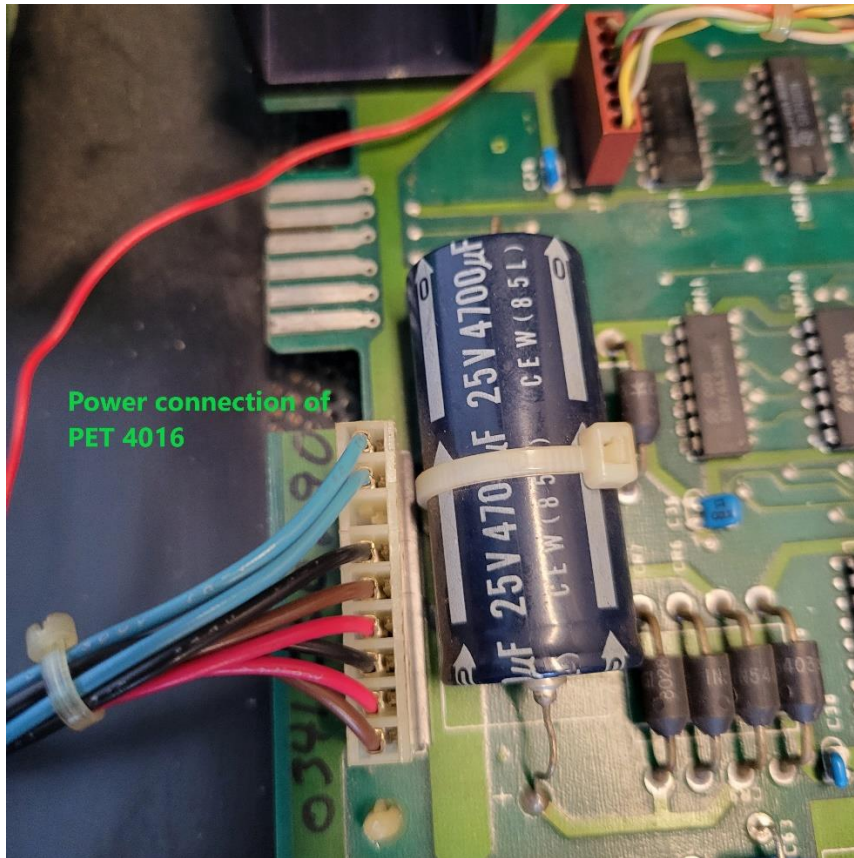
IC Description and Model

- CPU — 6502
- PIA#1 — 6520
- PIA#2 — 6520
- VIDEO RAM — 6550
- User Port — 6522
- SYSTEM RAM — 6550
- SYSTEM ROM — 6540 (H1-H7)
- CHAR ROM — 6550 A2

ROM 2.0 - Basic Level II - 28 pin ROM type 6540 - Series 2001

Location	ROM #	Part Number	
H1	6540-019	901439-09	
H2	6540-013	901439-02	
H3	6540-015	901439-03	EDIT ROM
H4	6540-016	901439-04	
H5	6540-012	901439-05	
H6	6540-014	901439-06	
H7	6540-018	901439-08	
A2	6540-010	901439-01	Character ROM

RUDY'S RETRO INTEL

Power connection of PET 4016

Connection from 4016 PET power supply to 2001-8 PET

Note
These 2 pins are NOT connected!

commodore
semiconductor group
NMOS

MPS
6522
VERSATILE
INTERFACE
ADAPTER

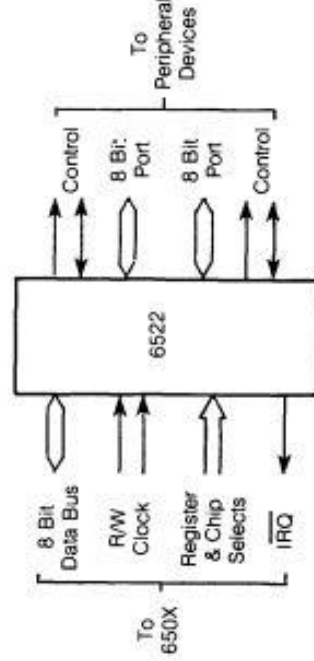# 6522 VERSATILE INTERFACE ADAPTER

DESCRIPTION

The 6522 Versatile Interface Adapter (VIA) provides all of the capability of the 6520. In addition, this device contains a pair of very powerful interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. Also, several peripheral I/O lines can be controlled directly from the interval timers for generating programmable-frequency square waves and for counting externally generated pulses. To facilitate control of the many powerful features of this chip, the internal registers have been organized into an interrupt flag register, an interrupt enable register and a pair of function control registers.
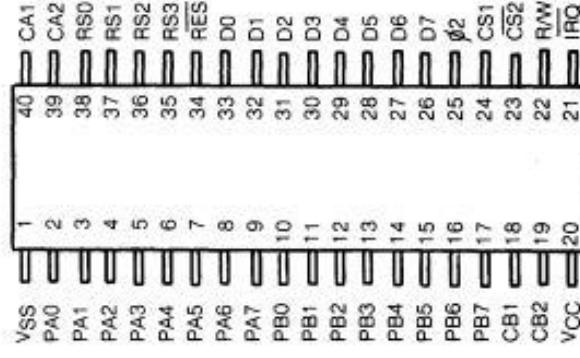
FEATURES

- Very powerful expansion of basic 6520 capability.
- N channel, depletion load technology, single +5V supply.
- Completely static and TTL compatible.
- CMOS compatible peripheral control lines.
- Expanded "handshake" capability allows very positive control of data transfers between processor and peripheral devices.

6522 Interface Diagram

6522 pinout:

Pin	Signal	Pin	Signal
1	Vss	40	CA1
2	PA0	39	CA2
3	PA1	38	RS0
4	PA2	37	RS1
5	PA3	36	RS2
6	PA4	35	RS3
7	PA5	34	RES
8	PA6	33	D0
9	PA7	32	D1
10	PB0	31	D2
11	PB1	30	D3
12	PB2	29	D4
13	PB3	28	D5
14	PB4	27	D6
15	PB5	26	D7
16	PB6	25	ø2
17	PB7	24	CS1
18	CB1	23	$\overline{CS2}$
19	CB2	22	R/W
20	VCC	21	$\overline{IRQ}$

commodore
semiconductor group
NMOS

MPS
6520
PERIPHERAL
ADAPTER

6520 PERIPHERAL ADAPTER
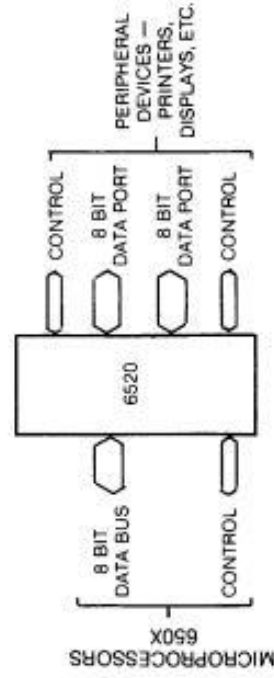
DESCRIPTION

The 6520 Peripheral Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the 6500 family of microprocessors, the 6520 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.
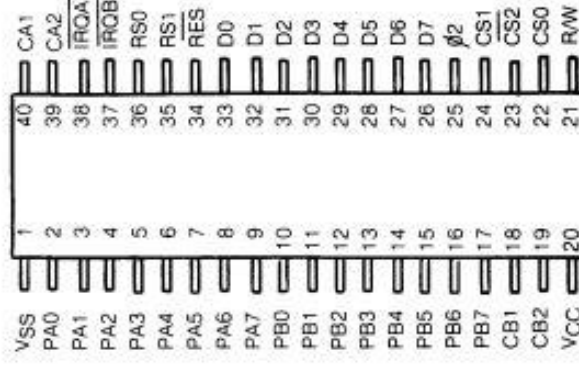
FEATURES

- High performance replacement for Motorola/AMI /MOSTEK/Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows very positive control of data transfers between processor and peripheral devices.
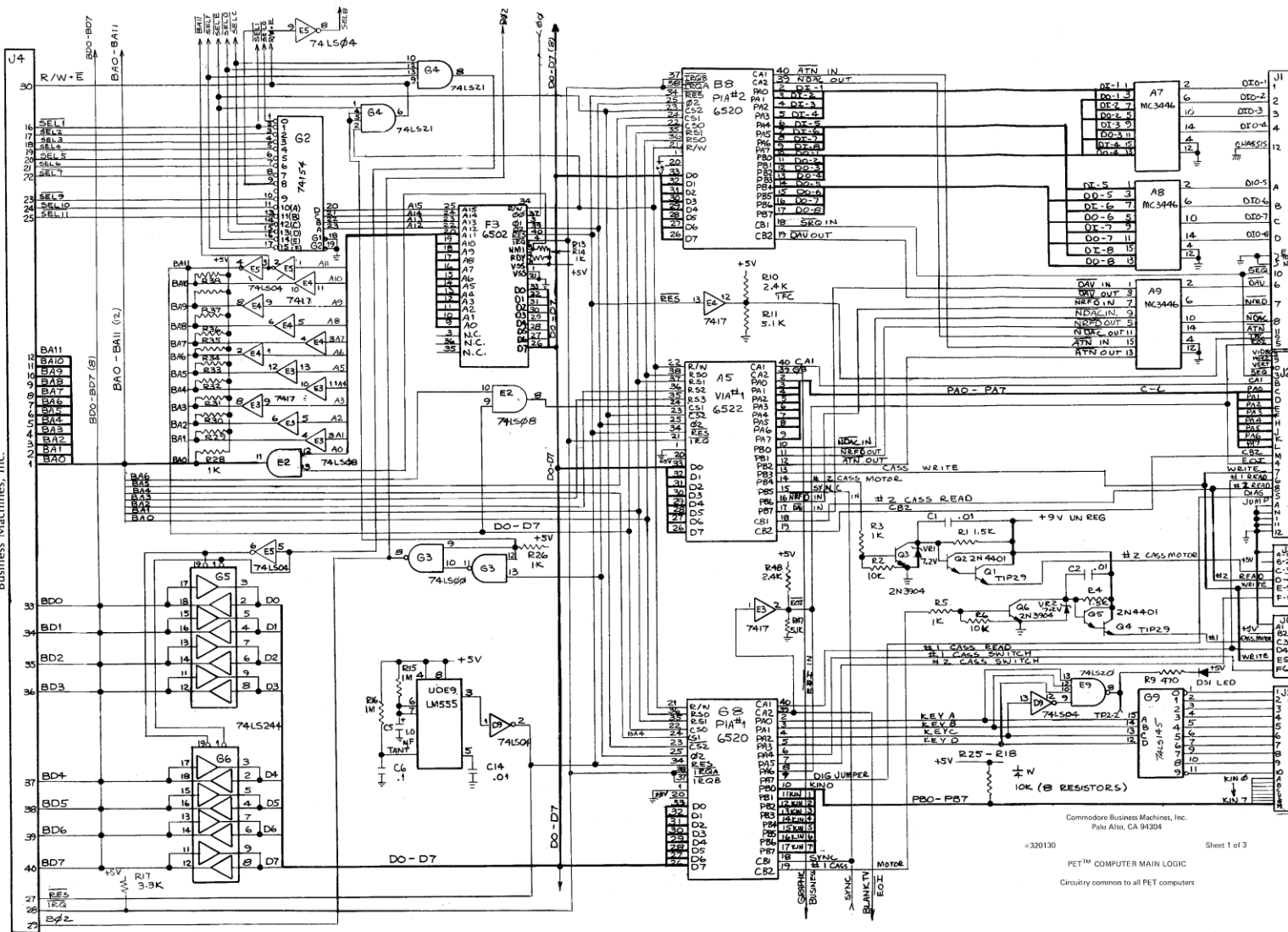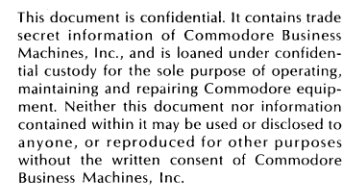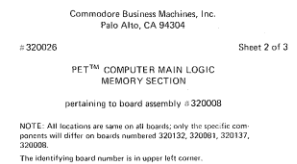
6520

Pin	Signal		Pin	Signal
1	Vss		40	CA1
2	PA0		39	CA2
3	PA1		38	IRQA
4	PA2		37	IRQB
5	PA3		36	RS0
6	PA4		35	RS1
7	PA5		34	RES
8	PA6		33	D0
9	PA7		32	D1
10	PB0		31	D2
11	PB1		30	D3
12	PB2		29	D4
13	PB3		28	D5
14	PB4		27	D6
15	PB5		26	D7
16	PB6		25	∅2
17	PB7		24	CS1
18	CB1		23	CS2
19	CB2		22	CS0
20	VCC		21	R/W

Basic 6520 Interface Diagram

Commodore Business Machines, Inc.
Palo Alto, CA 94304

#320130   Sheet 1 of 3

PET™ COMPUTER MAIN LOGIC

Circuitry common to all PET computers

NOTE. 1) ALL CKTS MARKED ✱ ARE FOR BC MACHINE ONLY

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           ┌────────∪────────┐
      Vss ⊏│ 1            28 │⊐ NC
      CS5 ⊏│ 2            27 │⊐ CS2
      CS4 ⊏│ 3            26 │⊐ D0
      CS3 ⊏│ 4            25 │⊐ D1
       A0 ⊏│ 5            24 │⊐ D2
       A1 ⊏│ 6            23 │⊐ D3
       A2 ⊏│ 7  MPS 6540  22 │⊐ D4
       A3 ⊏│ 8            21 │⊐ D5
       A4 ⊏│ 9            20 │⊐ D6
       A5 ⊏│ 10           19 │⊐ D7
       A9 ⊏│ 11           18 │⊐ A10
      Vdd ⊏│ 12           17 │⊐ CS1
       A8 ⊏│ 13           16 │⊐ CLK
       A7 ⊏│ 14           15 │⊐ A6
           └─────────────────┘
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Pin 2: $\overline{CS5}$
Pin 3: $\overline{CS4}$
Pin 4: $\overline{CS3}$