Digital Circuit Lab

Team 09 / Lab 3 Report

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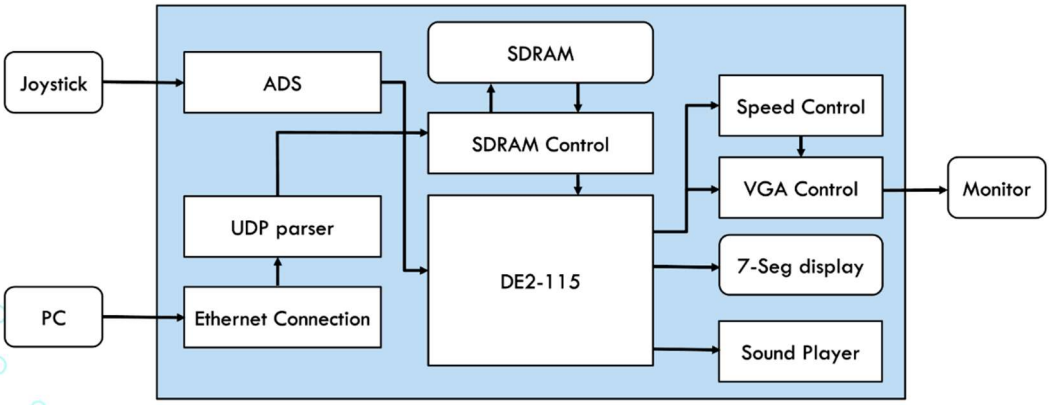
1. File Structure

```
/team09_final
├ team09_final_report.pdf
├ team09_final_presentation.pdf
└ /src
    ├ /ADS
    │   └ ads1115_controller.v
    ├ /DE2-115
    │   ├ DE2_115.sv
    │   ├ Debounce.sv
    │   └ hex_display.v
    ├ /Ethernet
    │   ├ arp.v
    │   ├ arp_cache.v
    │   ├ arp_eth_rx.v
    │   ├ arp_eth_tx.v
    │   ├ axis_gmii_rx.v
    │   ├ axis_gmii_tx.v
    │   ├ eth_arb_mux.v
    │   ├ eth_axis_rx.v
    │   ├ eth_axis_tx.v
    │   ├ eth_mac_1g.v
    │   ├ eth_mac_1g_rgmii.v
    │   ├ eth_mac_1g_rgmii_fifo.v
    │   ├ eth_mux.v
    │   ├ Ethernet.v
    │   ├ iddr.v
    │   ├ ip.v
    │   ├ ip_arc_mux.v
    │   ├ ip_complete.v
    │   ├ ip_eth_rx.v
    │   ├ ip_eth_tx.v
    │   ├ ip_mux.v
    │   ├ lfsr.v
    │   ├ oddr.v
```

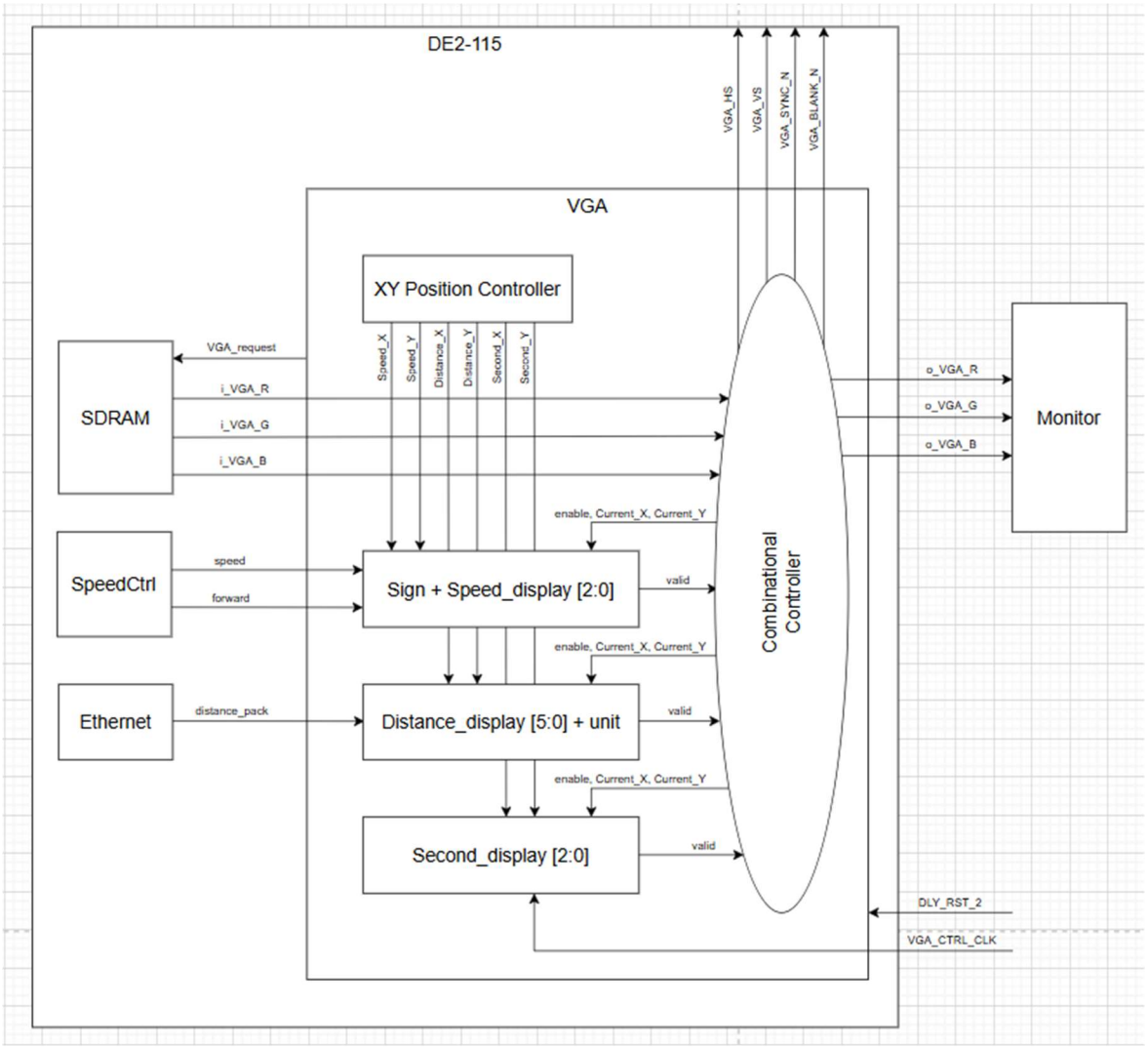
```
│   ├ rgmii_phy_if.v
│   ├ ssio_ddr_in.v
│   ├ ssio_ddr_out.v
│   ├ udp.v
│   ├ udp_checksum_gen.v
│   ├ udp_complete.v
│   ├ udp_ip_rx.v
│   ├ udp_ip_tx.v
│   ├ UDP_parser.v
│   └ /lib
│       ├ arbiter.v
│       ├ axis_async_fifo.v
│       ├ axis_async_fifo_adapter.v
│       ├ axis_fifo.v
│       ├ priority_encoder.v
│       └ sync_reset.v
├ /python
│   └ send_video.py
├ /Sdram
│   ├ command.v
│   ├ control_interface.v
│   ├ sdr_data_path.v
│   ├ Sdram_Control.v
│   ├ Sdram_Params.h
│   ├ sdram_pll.v
│   ├ Sdram_RD_FIFO.v
│   └ Sdram_WR_FIFO.v
├ /SpeedCtrl
│   └ SpeedCtrl.sv
└ /VGA
    ├ Distance_display.v
    ├ Letter_cm_display.v
    ├ Minus_display.v
    ├ Reset_Delay.v
    ├ Speed_display.h
    ├ Time_display.v
    ├ VGA_Controller.h
    └ VGA_Param.h
```

2. System Architecture

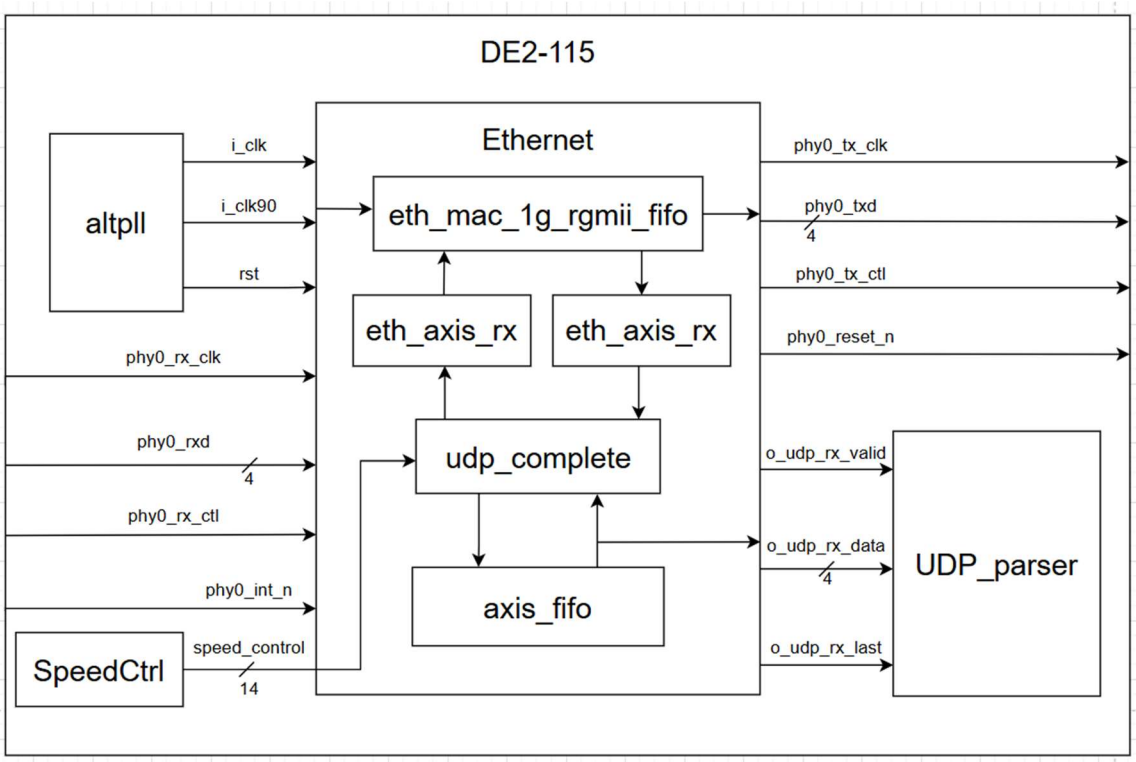
(1) Block Diagram



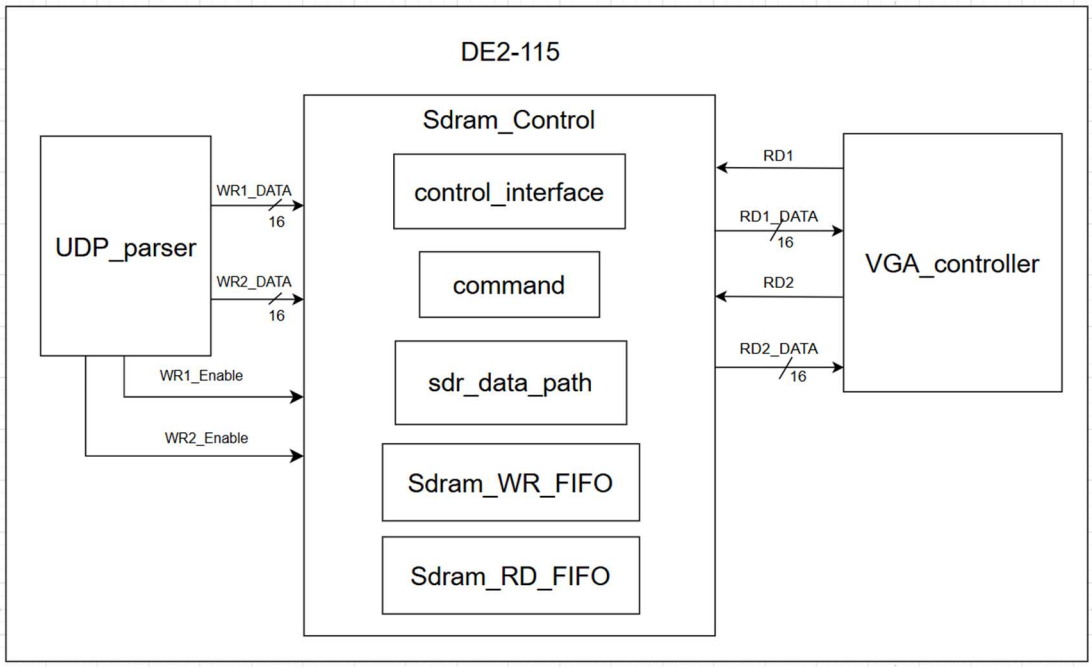
Whole System



VGA

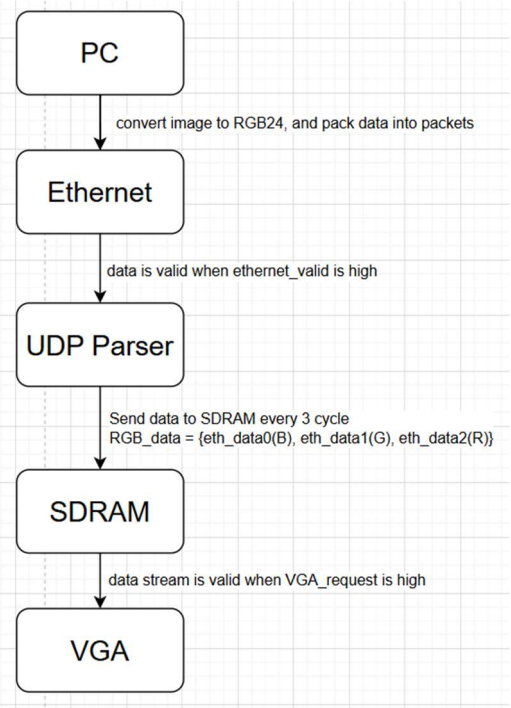


Ethernet



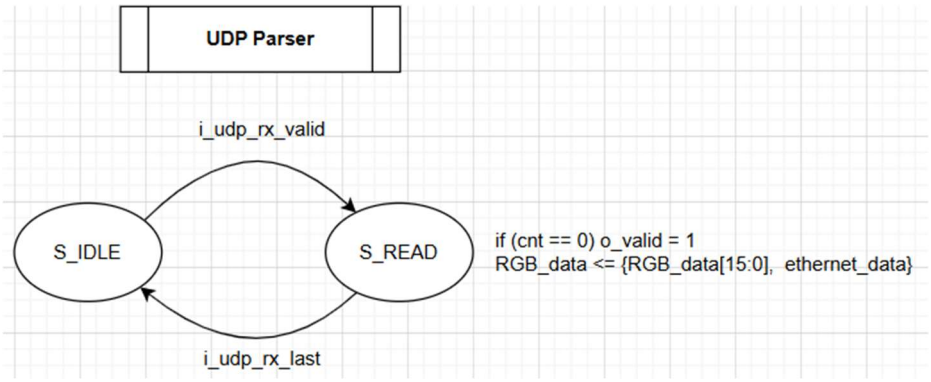
SDRAM

(2) Data Path

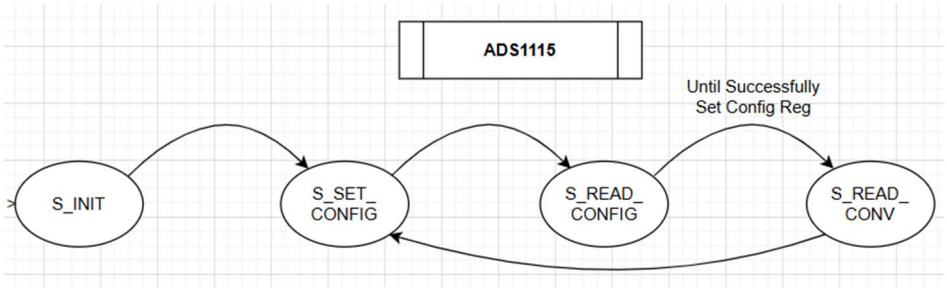


3. Hardware Scheduling

(1) Finite State Machine

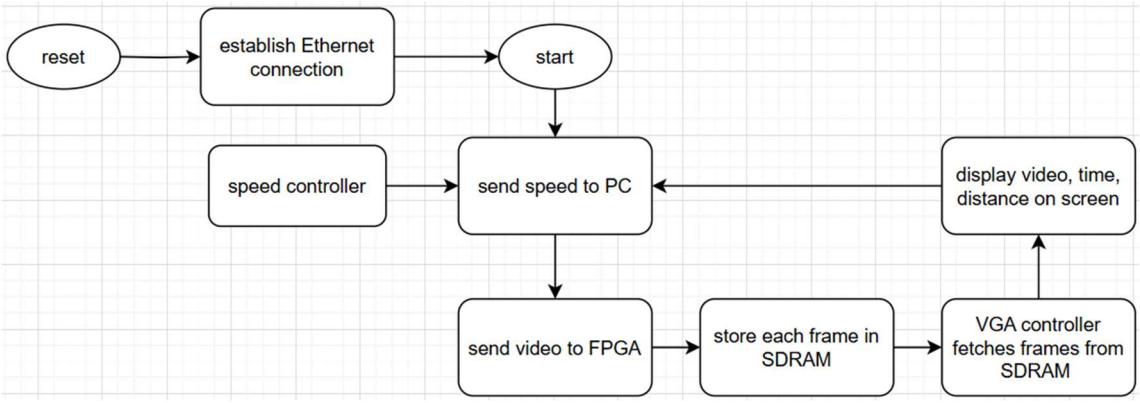


UDP Parser



ADS1115

(2) Flow Chart



4. Fitter Summary

Fitter Summary	
Fitter Status	Successful - Sat Jun 14 14:29:53 2025
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	13,326 / 114,480 (12 %)
Total combinational functions	11,408 / 114,480 (10 %)
Dedicated logic registers	5,211 / 114,480 (5 %)
Total registers	5223
Total pins	480 / 529 (91 %)
Total virtual pins	0
Total memory bits	451,072 / 3,981,312 (11 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	3 / 4 (75 %)

5. Timing Analyzer

Timing Closure Recommendations

Summary [hide details]

This design contains failing setup paths with a worst-case slack of -47.795 ns. Run Report Timing Closure Recommendations for recommendations on how to close setup timing. For recommendations for any particular path, click the appropriate link in the table below.

Top Failing Paths [hide details]

	Slack	From	To	Recommendations
1	-47.795	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[2]	Report recommendations for this path
2	-47.794	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[2]	Report recommendations for this path
3	-47.794	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[2]	Report recommendations for this path
4	-47.793	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[2]	Report recommendations for this path
5	-47.792	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[2]	Report recommendations for this path

Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	u6|altpll_component|auto_generated|pll1|clk[3]	-47.795	-960.272
2	altpll_component|auto_generated|pll1|clk[1]	0.022	0.000
3	altpll_component|auto_generated|pll1|clk[0]	0.463	0.000
4	enet0_rx_clk_125m	0.857	0.000
5	pll|altpll_0|sd1|pll7|clk[0]	2.503	0.000
6	enet0_tx_clk_125m	3.700	0.000
7	altera_reserved_tck	13.878	0.000
8	CLOCK2_50	15.331	0.000
9	pll|altpll_0|sd1|pll7|clk[1]	4988.181	0.000

Slow 1200mV 85C Model Setup: 'u6|altpll_component|auto_generated|pll1|clk[3]'

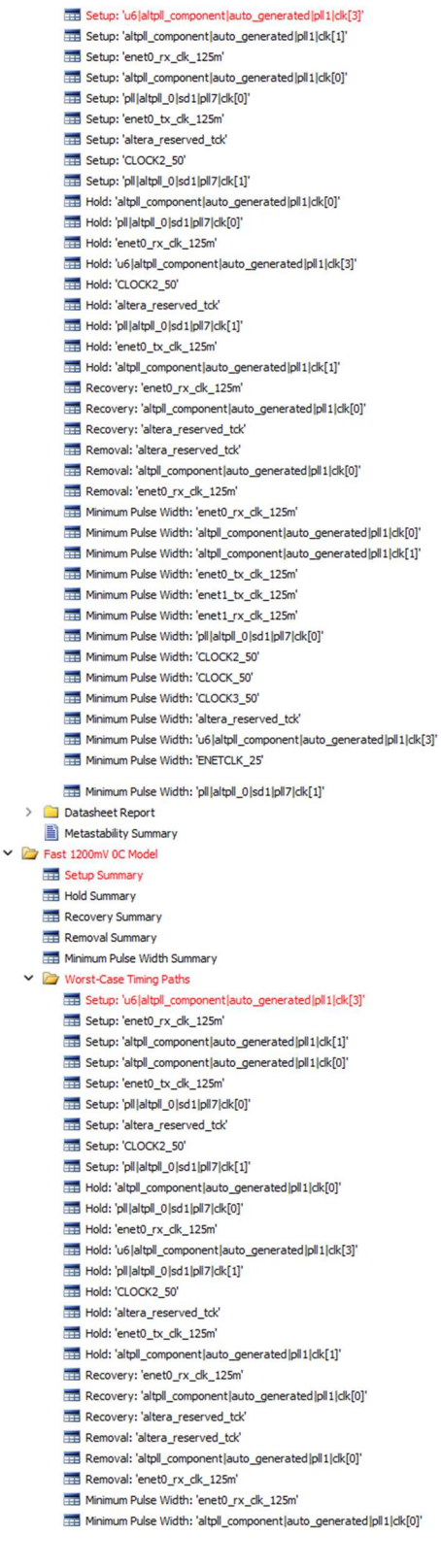
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-47.795	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.272	88.065
2	-47.736	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.272	88.006
3	-47.623	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.894
4	-47.566	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.837
5	-47.564	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.835
6	-47.528	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.799
7	-47.517	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.788
8	-47.469	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.740
9	-47.458	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.729
10	-47.416	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.687
11	-47.394	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.274	87.666
12	-47.365	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.636
13	-47.357	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.628
14	-47.306	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.577
15	-47.299	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.274	87.571
16	-47.288	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.274	87.560
17	-47.259	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.530
18	-47.233	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.504
19	-47.200	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.471
20	-47.187	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.274	87.459
21	-47.174	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	87.445
22	-47.136	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.274	87.408
23	-47.030	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.274	87.302
24	-47.004	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.274	87.276
25	-45.820	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.344	86.162
26	-45.703	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.280	85.983
27	-45.648	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.345	85.991
28	-45.553	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.345	85.896
29	-45.542	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.345	85.885
30	-45.533	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.281	85.812
31	-45.441	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.345	85.784
32	-45.438	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.281	85.717
33	-45.427	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.281	85.706
34	-45.390	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.345	85.733
35	-45.326	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.281	85.605
36	-45.284	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.345	85.627
37	-45.275	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.281	85.554
38	-45.258	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.345	85.601
39	-45.218	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_B[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.273	85.489
40	-45.169	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.281	85.448
41	-45.143	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.281	85.422
42	-45.046	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_B[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.274	85.318
43	-44.951	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_B[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.274	85.223

Slow 1200mV 0C Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	12.62 MHz	12.62 MHz	u6|altpll_component|auto_generated|pll1|clk[3]	
2	46.24 MHz	46.24 MHz	pll|altpll_0|sd1|pll7|clk[1]	
3	50.56 MHz	50.56 MHz	altera_reserved_tck	
4	145.2 MHz	145.2 MHz	pll|altpll_0|sd1|pll7|clk[0]	
5	146.31 MHz	146.31 MHz	altpll_component|auto_generated|pll1|clk[0]	
6	163.83 MHz	163.83 MHz	enet0_rx_clk_125m	
7	233.86 MHz	233.86 MHz	CLOCK2_50	

Slow 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	u6|altpll_component|auto_generated|pll1|clk[3]	-39.266	-768.535
2	altpll_component|auto_generated|pll1|clk[1]	0.182	0.000
3	enet0_rx_clk_125m	0.874	0.000
4	altpll_component|auto_generated|pll1|clk[0]	1.165	0.000
5	pll|altpll_0|sd1|pll7|clk[0]	3.113	0.000
6	enet0_tx_clk_125m	4.000	0.000
7	altera_reserved_tck	14.491	0.000
8	CLOCK2_50	15.724	0.000
9	pll|altpll_0|sd1|pll7|clk[1]	4989.188	0.000



Slow 1200mV 0C Model Setup: 'u6|altpll_component|auto_generated|pll1|clk[3]'

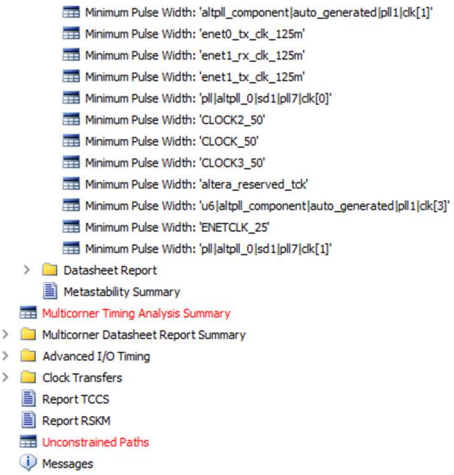
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-39.266	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.238	79.503
2	-39.227	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.238	79.464
3	-39.114	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.352
4	-39.086	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.324
5	-39.075	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.313
6	-39.053	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.291
7	-39.047	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.285
8	-39.023	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.261
9	-38.986	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.224
10	-38.984	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.222
11	-38.947	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.185
12	-38.901	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.240	79.140
13	-38.888	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.126
14	-38.873	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.240	79.112
15	-38.849	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.087
16	-38.849	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.087
17	-38.810	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.048
18	-38.810	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.240	79.049
19	-38.773	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.240	79.012
20	-38.772	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	79.010
21	-38.733	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	78.971
22	-38.675	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.240	78.914
23	-38.636	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.240	78.875
24	-38.559	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.240	78.798
25	-37.517	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.301	77.817
26	-37.400	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.246	77.645
27	-37.365	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.302	77.666
28	-37.337	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.302	77.638
29	-37.274	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.302	77.575
30	-37.248	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.247	77.494
31	-37.237	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.302	77.538
32	-37.220	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.247	77.466
33	-37.157	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.247	77.403
34	-37.139	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.302	77.440
35	-37.120	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.247	77.366
36	-37.100	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.302	77.401
37	-37.023	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.302	77.324
38	-37.022	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.247	77.268
39	-36.983	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.247	77.229
40	-36.924	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_B[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.239	77.172
41	-36.906	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.247	77.152
42	-36.782	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_B[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.240	77.021
43	-36.754	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_B[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.240	76.993

Fast 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	u6|altpll_component|auto_generated|pll1|clk[3]	-2.549	-13.448
2	enet0_rx_clk_125m	0.518	0.000
3	altpll_component|auto_generated|pll1|clk[1]	1.010	0.000
4	altpll_component|auto_generated|pll1|clk[0]	2.256	0.000
5	enet0_tx_clk_125m	5.174	0.000
6	pll|altpll_0|sd1|pll7|clk[0]	6.366	0.000
7	altera_reserved_tck	17.183	0.000
8	CLOCK2_50	17.752	0.000
9	pll|altpll_0|sd1|pll7|clk[1]	4993.997	0.000

Fast 1200mV 0C Model Setup: 'u6|altpll_component|auto_generated|pll1|clk[3]'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-2.549	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.668
2	-2.522	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.641
3	-2.456	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	42.576
4	-2.456	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.575
5	-2.429	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.548
6	-2.423	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.523
7	-2.377	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.496
8	-2.363	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	42.483
9	-2.346	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.464
10	-2.326	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.445
11	-2.318	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.437
12	-2.311	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	42.431
13	-2.299	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.418
14	-2.287	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.406
15	-2.260	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.379
16	-2.258	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.377
17	-2.252	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	42.372
18	-2.233	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	42.353
19	-2.231	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.350
20	-2.208	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_R[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.327
21	-2.194	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	42.314
22	-2.181	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_G[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.132	42.300
23	-2.165	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	42.285
24	-2.115	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_B[2]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	42.235
25	-1.668	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.169	41.824
26	-1.590	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.136	41.713
27	-1.575	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.169	41.731
28	-1.523	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.169	41.679
29	-1.497	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.136	41.620
30	-1.464	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.169	41.620
31	-1.445	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.169	41.601
32	-1.445	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.136	41.568
33	-1.406	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.169	41.562
34	-1.386	VGA_Controller:vga_inst|second_r[2]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.136	41.509
35	-1.377	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.169	41.533
36	-1.367	VGA_Controller:vga_inst|second_r[5]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.136	41.490
37	-1.333	VGA_Controller:vga_inst|second_r[0]	VGA_Controller:vga_inst|oVGA_B[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	41.453
38	-1.328	VGA_Controller:vga_inst|second_r[4]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.136	41.451
39	-1.327	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_R[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.169	41.483
40	-1.299	VGA_Controller:vga_inst|second_r[7]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.136	41.422
41	-1.249	VGA_Controller:vga_inst|second_r[6]	VGA_Controller:vga_inst|oVGA_G[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.136	41.372
42	-1.240	VGA_Controller:vga_inst|second_r[1]	VGA_Controller:vga_inst|oVGA_B[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	41.360
43	-1.188	VGA_Controller:vga_inst|second_r[3]	VGA_Controller:vga_inst|oVGA_B[3]	u6|altpll_component|auto_generated|pll1|clk[3]	u6|altpll_component|auto_generated|pll1|clk[3]	40.000	0.133	41.308



Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-47.795	0.116	1.651	0.557	3.379
1	CLOCK2_50	15.331	0.183	N/A	N/A	9.445
2	CLOCK3_50	N/A	N/A	N/A	N/A	16.000
3	CLOCK_50	N/A	N/A	N/A	N/A	9.574
4	ENETCLK_25	N/A	N/A	N/A	N/A	36.000
5	altera_reserved_tck	13.878	0.183	18.245	0.557	19.457
6	altpll_component|auto_generated|pll1|clk[0]	0.463	0.116	3.766	0.752	3.683
7	altpll_component|auto_generated|pll1|clk[1]	0.022	6.456	N/A	N/A	3.790
8	enet0_rx_clk_125m	0.518	0.142	1.651	0.824	3.379
9	enet0_tx_clk_125m	3.700	4.445	N/A	N/A	3.790
10	enet1_rx_clk_125m	N/A	N/A	N/A	N/A	4.000
11	enet1_tx_clk_125m	N/A	N/A	N/A	N/A	3.790
12	pll|altpll_0|sd1|pll7|clk[0]	2.503	0.139	N/A	N/A	4.682
13	pll|altpll_0|sd1|pll7|clk[1]	4988.181	0.180	N/A	N/A	4999.699
14	u6|altpll_component|auto_generated|pll1|clk[3]	-47.795	0.179	N/A	N/A	19.682
2	Design-wide TNS	-960.272	0.0	0.0	0.0	0.0
1	CLOCK2_50	0.000	0.000	N/A	N/A	0.000
2	CLOCK3_50	N/A	N/A	N/A	N/A	0.000
3	CLOCK_50	N/A	N/A	N/A	N/A	0.000
4	ENETCLK_25	N/A	N/A	N/A	N/A	0.000
5	altera_reserved_tck	0.000	0.000	0.000	0.000	0.000
6	altpll_component|auto_generated|pll1|clk[0]	0.000	0.000	0.000	0.000	0.000
7	altpll_component|auto_generated|pll1|clk[1]	0.000	0.000	N/A	N/A	0.000
8	enet0_rx_clk_125m	0.000	0.000	0.000	0.000	0.000
9	enet0_tx_clk_125m	0.000	0.000	N/A	N/A	0.000
10	enet1_rx_clk_125m	N/A	N/A	N/A	N/A	0.000
11	enet1_tx_clk_125m	N/A	N/A	N/A	N/A	0.000
12	pll|altpll_0|sd1|pll7|clk[0]	0.000	0.000	N/A	N/A	0.000
13	pll|altpll_0|sd1|pll7|clk[1]	0.000	0.000	N/A	N/A	0.000
14	u6|altpll_component|auto_generated|pll1|clk[3]	-960.272	0.000	N/A	N/A	0.000

Unconstrained Paths

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	1	1
3	Unconstrained Input Ports	28	28
4	Unconstrained Input Port Paths	43	43
5	Unconstrained Output Ports	88	88
6	Unconstrained Output Port Paths	187	187

6. Reflection and Feedback

(1) Reflection

At the beginning of our final project, we assumed that implementing the basic functions would be relatively straightforward. However, we encountered a number of unexpected challenges as we began working through them.

We initially had a USB controller that could connect to the Nintendo Switch, but it did not adhere to any known protocol, making it difficult to interpret its communication patterns. As a result, we decided to build our own controller from scratch. We considered using a rotary encoder to detect input signals, but since it only measures relative motion rather than absolute position, we ultimately opted for a potentiometer. To process its output, we used the ADS1115 analog-to-digital converter, which communicates with the FPGA via the I^2C protocol. Unfortunately, the ADS1115 datasheet lacked a clear explanation of the I^2C communication details, so we relied on an Arduino library and a logic analyzer to decode the messages successfully.

Next, we tackled the Ethernet connection between the FPGA board and our PC. We followed instructions from a GitHub repository outlining how to implement Ethernet communication on an FPGA. However, our unfamiliarity with computer networking made it difficult to configure the settings and set up the necessary clock signals. After extensive trial and error, we managed to establish a connection. One limitation we encountered was our inability to control the timing of outbound messages from the FPGA. The original setup only allowed the FPGA to send a response immediately after receiving data from the PC. Although we could modify the content of the response, we couldn't decouple it from the timing of the incoming message. Our workaround was to have the PC transmit data at a higher frequency, enabling the FPGA to maintain near real-time communication.

Lastly, we worked on utilizing the SDRAM on the DE2-115 development board. Although we started with the board’s sample code, we struggled to control the SDRAM's read and write addresses. As a result, we were only able to use it as a simple buffer. Our original plan was to regulate the output frame rate by selectively reading from specific addresses, but due to these limitations, we had to rely on a Python script to control the frame rate externally by adjusting the speed at which frames were sent.

Although we technically achieved all the intended functionalities, we had to employ several workarounds to overcome challenges we didn’t fully understand. In the future, we hope to deepen our understanding of Ethernet communication and SDRAM operations so that we can leverage their full potential and design more robust systems.

(2) Feedback

Over the course of this semester, we became more familiar with FPGA development and Verilog programming. However, we spent a significant amount of time trying to understand—and at times merely manage to implement—the Ethernet and SDRAM functionalities. To help future students overcome similar challenges more efficiently, we recommend that the TAs offer additional lectures or curated learning resources focused on these topics. This would greatly enhance our ability to implement complex features more effectively and with greater confidence.