## **Digital Circuit Lab**

Team 09 / Lab 3 Report

```
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```

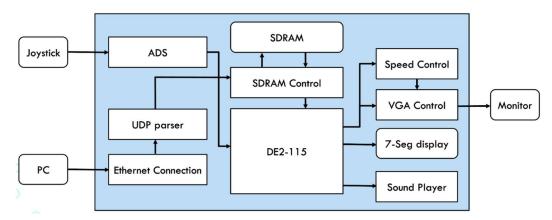
## 1. File Structure

```
/team09_final
- team09_final_report.pdf
- team09 final presentation.pdf
L_{/src}
     -/ADS
          Lads1115 controller.v
     -/DE2-115
          - DE2 115.sv
         - Debounce.sv
         L hex display.v
     -/Ethernet
          - arp.v
          - arp_cache.v
         - arp_eth_rx.v
          - arp_eth_tx.v
          - axis_gmii_rx.v
         - axis_gmii_tx.v
         eth_arb_mux.v
         - eth_axis_rx.v
          - eth_axis_tx.v
          - eth_mac_1g.v
         - eth_mac_1g_rgmii.v
         - eth_mac_1g_rgmii_fifo.v
          eth_mux.v
          - Ethernet.v
          - iddr.v
          - ip.v
          - ip_arc_mux.v
          - ip_complete.v
          - ip_eth_rx.v
          - ip_eth_tx.v
          - ip_mux.v
          lfsr.v
          oddr.v
```

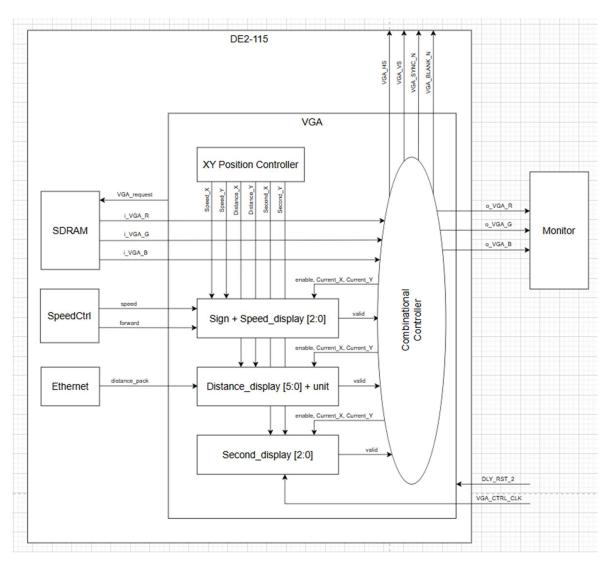
```
rgmii_phy_if.v
    ssio ddr in.v
    - ssio ddr out.v
    - udp.v
    - udp_checksum_gen.v
    - udp_complete.v
    - udp_ip_rx.v
    - udp_ip_tx.v
    - UDP_parser.v
    L/lib
         - arbiter.v
         - axis_async_fifo.v
         - axis_async_fifo_adapter.v
         - axis fifo.v
         - priority_encoder.v
         L<sub>sync</sub> reset.v
-/python
    L_{send\_video.py}
-/Sdram
    - command.v
    - control_interface.v
    - sdr_data_path.v
    - Sdram_Control.v
    - Sdram_Params.h
    sdram pll.v
    - Sdram_RD_FIFO.v
    L Sdram_WR_FIFO.v
-/SpeedCtrl
    L SpeedCtrl.sv
L/VGA
    - Distance display.v
    Letter_cm_display.v
    - Minus display.v
    - Reset_Delay.v
    - Speed_display.h
    - Time_display.v
    - VGA_Controller.h
    LVGA Param.h
```

# 2. System Architecture

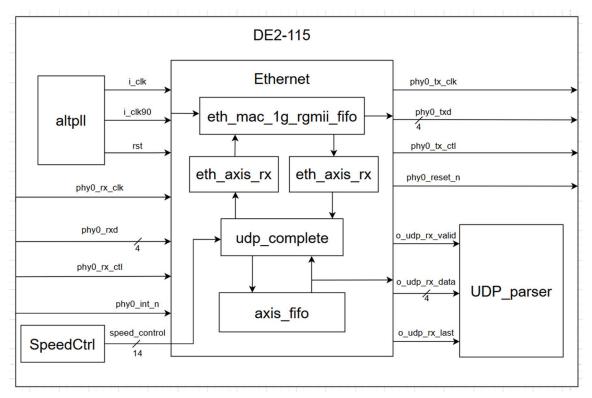
# (1) Block Diagram



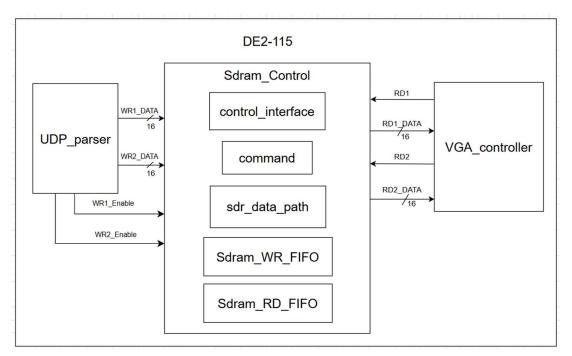
Whole System



**VGA** 

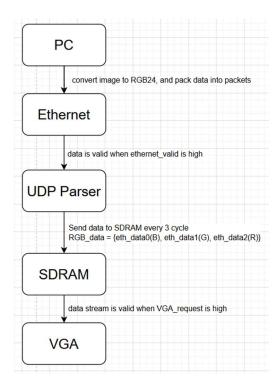


Ethernet



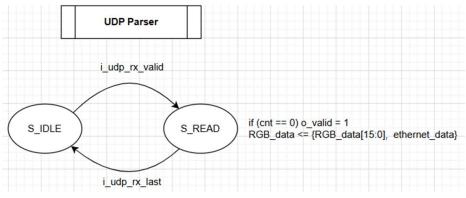
**SDRAM** 

## (2) Data Path

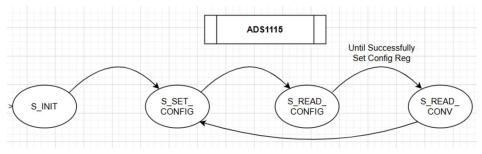


## 3. Hardware Scheduling

# (1) Finite State Machine

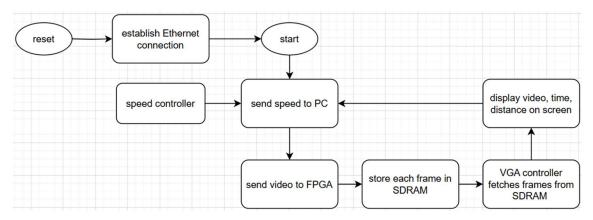


**UDP** Parser



ADS1115

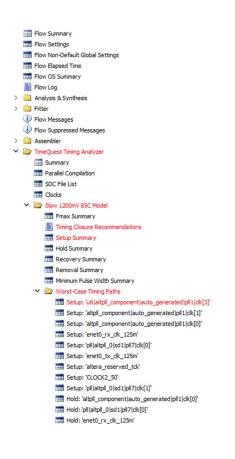
# (2) Flow Chart



# 4. Fitter Summary

Fitter Status	Successful - Sat Jun 14 14:29:53 2025
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	13,326 / 114,480 ( 12 % )
Total combinational functions	11,408 / 114,480 ( 10 % )
Dedicated logic registers	5,211 / 114,480 ( 5 % )
Total registers	5223
Total pins	480 / 529 (91 %)
Total virtual pins	0
Total memory bits	451,072 / 3,981,312 ( 11 % )
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	3/4(75%)

## 5. Timing Analyzer





➤ Worst-Case Timing Paths

# Timing Closure Recommendations Summary [hide details] This design contains failing setup paths with a worst-case slack of -47.795 ns. Run Report Timing Closure Recommendations for recommendations on how to dose setup timing. For recommendations for any particular path, click the appropriate link in the table below. Top Failing Paths [hide details] Slack | From | To | Recommendations for this path | 1-47.795 | VGA\_Controller:vga\_inst]econd\_r[0] | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 3-47.794 | VGA\_Controller:vga\_inst]econd\_r[0] | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 4-7.793 | VGA\_Controller:vga\_inst]econd\_r[0] | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 3-47.792 | VGA\_Controller:vga\_inst]econd\_r[0] | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]econd\_r[0] | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_Controller:vga\_inst]evGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_CONTROLLER:VGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_CONTROLLER:VGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_CONTROLLER:VGA\_R[2] | Report recommendations for this path | 5-47.792 | VGA\_CONTROLLE

	Clock	Slack	End Point TNS
1	u6 altpll_component auto_generated pll1 clk[3]	-47.795	-960.272
2	altpll_component auto_generated pll1 clk[1]	0.022	0.000
3	altpll_component auto_generated pll1 clk[0]	0.463	0.000
4	enet0_rx_dk_125m	0.857	0.000
5	pll altpll_0 sd1 pll7 clk[0]	2.503	0.000
6	enet0_tx_clk_125m	3.700	0.000
7	altera_reserved_tck	13.878	0.000
8	CLOCK2_50	15.331	0.000
9	pll altpll 0 sd1 pll7 dk[1]	4988.181	0.000

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Dela
47,795	VGA_Controller:vga_inst second_r(0)	VGA Controller:vga instioVGA R[2]	u6 laltpli component lauto generated bil 1 lck/3	u6laltpl componentiauto generated[pl[1]dkf3]	40,000	0.272	88.065
47,736	VGA_Controller:vga_inst(second_r[0]	VGA_Controller:vga_inst joVGA_G[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 aitpil_component auto_generated pil1 dk[3]	40.000	0.272	88.006
47,623	VGA_Controllerryga_inst(second_r[1]	VGA_Controller:vga_inst joVGA_R[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 altpll_component auto_generated pll1 dk[3]	40.000	0.273	87.894
47,566	VGA Controllerryga instisecond rf0)	VGA Controller:vga instigVGA B[2]	u6laltpl componentiauto generatedipli1ick/31	u6laltpl componentiauto generatediplilidk[3]	40,000	0.273	87,837
47.564	VGA_Controller:vga_inst(second_r[1]	VGA_Controller:vga_inst(oVGA_G[2]	u6 altpli_component auto_generated pli1 clk[3]	u6 altpli_component jauto_generated [pli1]ck[3]	40.000	0.273	87.835
47.528	VGA_Controllerryga_inst[second_r[2]	VGA_Controller:vga_inst joVGA_R[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 aitpil_component auto_generated pil1 dk[3]	40.000	0.273	87.799
47.517	VGA_Controller:vga_inst[second_r[3]	VGA_Controller:vga_inst loVGA_R[2]	u6 altpli_component auto_generated pl11 clk(3)	u6 altpli_component auto_generated pli1 dk[3]	40.000	0.273	87.788
47,469	VGA_Controller:vga_inst(second_r[2]	VGA_Controller:vga_inst joVGA_G[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 laitpil_component jauto_generated [pli1]ck[3]	40.000	0.273	87.740
47,458	VGA Controller:vga instisecond r[3]	VGA Controller:vga inst joVGA G[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 jailpil component jauto generated jpli 1 jck [3]	40.000	0.273	87,729
47.416	VGA Controller:vga_inst[second_r[4]	VGA_Controller:vga_inst loVGA_R[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 laitpil_component lauto_generated [pil 1 ldk[3]	40.000	0.273	87.687
47.394	VGA Controller:vga instisecond r[1]	VGA Controller:vga inst/oVGA B[2]	u6 laltpli_component  auto_generated pli1 ck(3)	u6 laitpil component lauto generated [pil 1   ck[3]	40.000	0.274	87.666
47,365	VGA Controller:vga instisecond r[5]	VGA Controller:vga inst loVGA R[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 laitpi component lauto generated [pli1] ck[3]	40.000	0.273	87.636
47.357	VGA Controller:vga instisecond r[4]	VGA Controller:vga instioVGA G[2]	u6 laitpil component lauto generated [pl 1 lck[3]	u6-laitpil componentiauto generatedipil1 ick[3]	40.000	0.273	87.628
47,306	VGA Controller:vga instisecond r[5]	VGA Controller:vga instioVGA G[2]	u6 laltpli component lauto generated ipi 1 lck [3]	utilaltpli componentiauto generatedipli1ick[3]	40,000	0.273	87,577
47, 299	VGA Controllerryga instisecond r[2]	VGA_Controller:vga_inst(oVGA_8(2)	u6 laltpli component lauto generated ipi 1 lck [3]	utilaltpli componentiauto generatedipli1ick[3]	40.000	0.274	87.571
47.288	VGA Controllerryga instisecond r[3]	VGA_Controller:vga_inst(oVGA_8(2)	u6 laltpli component lauto generated ipl 1 lck[3]	utilaltpl componentiauto generatediplilick[3]	40.000	0.274	87,560
47,259	VGA Controllerryga instisecond rife)	VGA Controller:vga instioVGA R[2]	u6 laltpli component lauto generated ipli 1 ick [3]	u6 laitpil component lauto generated ipil 1 lck [3]	40.000	0.273	87,530
47,233	VGA Controllerryga instisecond r[7]	VGA Controller:vga instioVGA R[2]	u6laltpli componentiauto generatedipli1ick[3]	u6 laitpil component lauto generated ipil 1 lck[3]	40.000	0.273	87,504
47,200	VGA Controller:vga instisecond rife)	VGA Controller:vga instioVGA G[2]	u6laltoli componentiauto generatediplilick[3]	u6 laitpil component lauto generated [pl 1 lck/3]	40,000	0.273	87,471
47, 187	VGA Controllerryga instisecond r[4]	VGA Controller:vga instioVGA B[2]	u6 laltal component lauto generated [pl 1 lck[3]	u6 laitpil component lauto generated [pil 1 lck/3]	40,000	0.274	87,459
47, 174	VGA_Controller:vga_inst second_r[7]	VGA Controller:vga instigVGA G[2]	u6 laltoli componentiauto generated [pli1] cki[3]	u6 laitpl component lauto generated [pl 1 ldk/3]	40,000	0.273	87,445
47, 136	VGA Controller:vga instisecond r[5]	VGA Controller:voa instioVGA 8(2)	u6 laitoli componentiauto generatedipii 1 icki 3	u6 laitpil component lauto generated [pl 1 lck/3]	40,000	0.274	87,408
47.030	VGA_Controller:vga_inst second_r[6]	VGA_Controller:vga_inst(oVGA_B(2)	u6 laitoli componentiauto generatedipi 1 icki 3	u6 laitpil component lauto generated [pil 1 lck/3]	40.000	0.274	87,302
47,004	VGA Controller:vga instisecond r[7]	VGA Controller:vga instioVGA 8(2)	u6 laitoli componentiauto generated [pli1] cki[3]	u6 laitel component lauto generated [oli 1 lck/3]	40,000	0.274	87,276
45,820	VGA_Controller:vga_inst(second_r[0])	VGA_Controller:vga_inst(oVGA_R[3]	u6 jaltpli_component jauto_generated [pli1]ck(3)	u6 altpll_component auto_generated pll1 ck[3]	40,000	0.344	86.162
45,705	VGA_Controller:vga_inst(second_r[0])	VGA_Controller:vga_inst[oVGA_G[3]	u6  altpli_component  auto_generated pli1 ck(3)	u6 altpil component jauto_generated [pil1]ck[3]	40.000	0.280	85,983
45,648	VGA_Controller:vga_inst second_r[1]	VGA_Controller:vga_inst joVGA_R[3]	u6 [altpli_component jauto_generated]pli1[ck[3]	u6.laltpll_component.jauto_generated.jpll1.jclk[3]	40.000	0.345	85.991
45,553	VGA_Controller:vga_inst second_r[2]	VGA_Controller:vga_instjpVGA_R[3]	u6 [altpli_component jauto_generated]pli1[ck[3]	u6/allpli component/auto_generated/pli1/ck[3]	40.000	0.345	85.896
45,542	VGA Controller:vga instisecond r[3]	VGA Controller:vga instioVGA R[3]	u6 jaitpli component jauto_generated [pli1ick[3]	utilalital componentiauto generated [pll1]ck[3]	40.000	0.345	85.885
45,533	VGA_Controller:vga_instisecond_r[1]	VGA_Controller:vga_inst(oVGA_G[3]	u6 laltpli_component lauto_generated [pli1]ck(3)	u6.laltpll_component.lauto_generated.jpll1.lck[3]	40.000	0.281	85.812
45,441	VGA Controller:vga instisecond r[4]	VGA Controller:vga instioVGA R[3]	u6 laitpil component lauto generated [pil 1 lck[3]	usialtpli componentiauto generatedipli1ick[3]	40.000	0.345	85.784
45,438	VGA Controller:vga instisecond r[2]	VGA Controller:vga instioVGA G[3]	u6 laitpil component lauto generated [pil 1 ick[3]	u6.laltpll componentiauto generated.ipli1ick[3]	40,000	0.281	85.717
45.427	VGA Controler:vga instisecond r[3]	VGA Controller:vga instioVGA G[3]	u6 laitpil component lauto generated [pil 1 ick[3]	u6.laltpll_component.lauto_generated.ipll1.lck[3]	40.000	0.281	85,706
45,390	VGA Controler:vga instisecond r[5]	VGA Controller:vga instioVGA R[3]	u6 altpli component lauto generated [pli] 1 ick(3)	u6 laltpli component lauto generated [pli] (ck[3]	40,000	0.345	85.733
45,326	VGA Controlerryga instisecond r[4]	VGA Controller:vga instigVGA G[3]	u6 laltpli component lauto generated [pl 1 lcki 3]	u6ialtpll componentiauto generatedipli1ick[3]	40,000	0.281	85.605
45,284	VGA Controlerryga instisecond rf6)	VGA Controllerivga InstigVGA R[3]	u6 laltpll component lauto generated [pl ] ick[3]	u6 altpli componentiauto generated ipli 1 ick [3]	40,000	0.345	85.627
45,275	VGA_Controllerryga_inst(second_r[5]	VGA Controller:vga instigVGA G[3]	u6 altpl component lauto generated [pl 1 ick 3]	u6(altpli componentiauto generated)pl1(ck[3]	40,000	0.281	85.554
45,258	VGA Controllerivga instisecond r[7]	VGA_Controller:vga_inst]oVGA_R[3]	u6 lattpli component lauto generated [old 1 lck/3]	u6/altpl component/auto generated/pl/1/ck/3	40,000	0.345	85.601
45.218	VGA_Controllerryga_inst(second_r[0]	VGA Controller:vga insticVGA BISI	u6 laltpl component lauto generated [pl 1 lcki 3]	u6laltoll componentiauto generatedipl11ck/3	40,000	0.273	85,489
45, 169	VGA_Controllerryga_inst(second_r(6)	VGA_Controller:vga_inst]oVGA_G[3]	u6 laltoli component lauto generated [oli 1 icki 3]	u6ialtoli componentiauto generatedipli1ick[3]	40,000	0.281	85,448
45, 143	VGA_Controller:vga_inst[second_r[7]	VGA_Controller:vga_inst[oVGA_G[3]	u6 jaltpli_component jauto_generated jpl 1 jck(3)	u6jaltpli_componentjauto_generatedjpli1[ck[3]	40.000	0.281	85.422
45.046	VGA Controller:vga_rist(second_r[1]	VGA Controller:vga instigVGA B[3]	u6 altoli componentiauto generatedioli 1 (ck/3)	u6 laltoli componentiauto generated pli 1 (ck/3)	40,000	0.274	85.318
44,951	VGA_Controller:vga_inst[second_r[2]	VGA_Controller:vga_inst(oVGA_B[3]	u6 altpli_component auto_generated pi1 ck(3)	u6 altpli_component auto_generated pli1 ck[3]	40,000	0.274	85.223

Slow 1200mV 0C Model Fmax Summary							
	Fmax	Restricted Fmax	Clock Name	Note			
1	12.62 MHz	12.62 MHz	u6 altpll_component auto_generated pll1 clk[3]				
2	46.24 MHz	46.24 MHz	pll altpll_0 sd1 pll7 clk[1]				
3	50.56 MHz	50.56 MHz	altera_reserved_tck				
4	145.2 MHz	145.2 MHz	pll altpll_0 sd1 pll7 clk[0]				
5	146.31 MHz	146.31 MHz	altpll_component auto_generated pll1 clk[0]				
6	163.83 MHz	163.83 MHz	enet0_rx_dk_125m				
7	233.86 MHz	233.86 MHz	CLOCK2_50				

Slow 1200mV 0C Model Setup Summary							
	Clock	Slack	End Point TNS				
1	u6 altpll_component auto_generated pll1 clk[3]	-39.266	-768.535				
2	altpll_component auto_generated pll1 clk[1]	0.182	0.000				
3	enet0_rx_dk_125m	0.874	0.000				
4	altpll_component auto_generated pll1 clk[0]	1.165	0.000				
5	pll altpll_0 sd1 pll7 clk[0]	3.113	0.000				
6	enet0_tx_dk_125m	4.000	0.000				
7	altera_reserved_tck	14.491	0.000				
8	CLOCK2_50	15.724	0.000				
9	pll altpll_0 sd1 pll7 clk[1]	4989.188	0.000				

			<b></b>	Setup: 'u6 altpll_component auto_generated pll1 clk[3]'
			=	$Setup: 'altpll\_component auto\_generated pll1 clk[1]'$
				Setup: 'enet0_rx_dk_125m'
				Setup: 'altpli_component auto_generated pli1 dk[0]'
				Setup: 'pll altpll_0 sd1 pll7 clk[0]' Setup: 'enet0_tx_clk_125m'
				Setup: 'altera_reserved_tck'
			_	Setup: 'CLOCK2_50'
			-	Setup: 'pll altpll_0 sd1 pll7 dk[1]'
			=	Hold: 'altpll_component auto_generated pll1 clk[0]'
				Hold: 'pll altpll_0 sd1 pll7 dk[0]'
			_	Hold: 'enet0_rx_clk_125m' Hold: 'u6 altpll_component auto_generated pll1 dk[3]'
				Hold: 'CLOCK2 50'
			-	Hold: 'altera_reserved_tck'
				Hold: 'pll altpll_0 sd1 pll7 dk[1]'
				Hold: 'enet0_tx_dk_125m'
			_	Hold: 'altpli_component auto_generated pli1 dk[1]'
				Recovery: 'enet0_rx_dk_125m'  Recovery: 'altpll_component auto_generated pll1 dk[0]'
				Recovery: 'altera_reserved_tck'
				Removal: 'altera_reserved_tck'
				$Removal: \ 'altpll\_component  auto\_generated  pll 1  dk[0]'$
				Removal: 'enet0_rx_dk_125m'
				Minimum Pulse Width: 'enet0_rx_dk_125m'
				Minimum Pulse Width: 'altpll_component auto_generated pll1 dk[0]'  Minimum Pulse Width: 'altpll_component auto_generated pll1 dk[1]'
				Minimum Pulse Width: 'enet0_tx_clk_125m'
			<b>=</b>	Minimum Pulse Width: 'enet1_tx_dk_125m'
				Minimum Pulse Width: 'enet1_rx_clk_125m'
				Minimum Pulse Width: 'pll altpll_0 sd1 pll7 dk[0]'
				Minimum Pulse Width: 'CLOCK2_50' Minimum Pulse Width: 'CLOCK 50'
				Minimum Pulse Width: 'CLOCK3_50'
			-	Minimum Pulse Width: 'altera_reserved_tck'
				Minimum Pulse Width: 'u6 altpll_component auto_generated pll1 dk[3]'
				Minimum Pulse Width: 'ENETCLK_25'
				Minimum Pulse Width: 'pll altpll_0 sd1 pll7 clk[1]'
	>	Pality.		asheet Report tastability Summary
~				00mV 0C Model
		_		up Summary
		_		d Summary
				covery Summary
				noval Summary imum Pulse Width Summary
	~			rst-Case Timing Paths
				Setup: 'u6 altpll_component auto_generated pll1 dk[3]'
			_	Setup: 'enet0_rx_dk_125m'
			_	Setup: 'altpll_component auto_generated pll1 clk[1]'
				Setup: 'altpll_component auto_generated pll1 dk[0]' Setup: 'enet0_tx_dk_125m'
				Setup: 'pll altpll_0 sd1 pll7 clk[0]'
				Setup: 'altera_reserved_tck'
				Setup: 'CLOCK2_50'
				Setup: 'pll altpll_0 sd1 pll7 dk[1]'
				Hold: 'altpll_component auto_generated pll1 dk[0]' Hold: 'pll altpll_0 sd1 pll7 dk[0]'
				Hold: 'enet0_rx_dk_125m'
				Hold: 'u6 altpll_component auto_generated pll1 clk[3]'
				Hold: 'pll altpll_0 sd1 pll7 dk[1]'
				Hold: 'CLOCK2_50'
				Hold: 'altera_reserved_tck'
				Hold: 'enet0_tx_clk_125m' Hold: 'altpll_component auto_generated pll1 clk[1]'
				Recovery: 'enet0_rx_dk_125m'
				Recovery: 'altpli_component auto_generated pli1 dk[0]'
				Recovery: 'altera_reserved_tck'
				Removal: 'altera_reserved_tck'
				Removal: 'altpll_component auto_generated pll1 dk[0]' Removal: 'enet0_rx_dk_125m'
				Minimum Pulse Width: 'enet0_rx_dk_125m'
				Minimum Pulse Width: 'altpll_component auto_generated pll1 clk[0]'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Dela
	-39.266	VGA_Controller:vga_inst(second_r(0))	VGA_Controller:vga_inst(oVGA_R[2]	u6 altpll_component auto_generated pll1 clk[3]	u6(altpll_component auto_generated pll1 ck[3]	40.000	0.238	79.503
	-39.227	VGA_Controller:vga_inst(second_r(0))	VGA_Controller:vga_inst joVGA_G[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 altpil_component auto_generated pil1 ck(3)	40.000	0.238	79.464
	-39.114	VGA_Controller:vga_inst(second_r[1]	VGA_Controller:vga_inst]oVGA_R[2]	u6 altpll_component auto_generated pll1 ck(3)	u6 altpli_component auto_generated pli1 ck(3)	40.000	0.239	79.352
	-39.086	VGA Controller:vga_inst(second_r[2])	VGA_Controller:vga_inst[oVGA_R[2]	u6 jaitpii component jauto generated [pii 1 [clk [3]]	u6 laitpii component lauto generated [pii 1 ]ck[3]	40.000	0.239	79.324
	-39.075	VGA Controller:vga instisecond r[1]	VGA_Controller:vga_inst[oVGA_G[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 laitpii component jauto generated [pli 1 [ck [3]]	40.000	0.239	79.313
	-39.053	VGA_Controller:vga_inst(second_r(0))	VGA_Controller:vga_inst(oVGA_B[2])	u6 altpli_component auto_generated pli1 ck(3)	u6 laitpil_component lauto_generated [pli1]ck[3]	40.000	0.239	79.291
	-39.047	VGA Controller:vga instisecond r[2]	VGA_Controller:vga_inst[oVGA_G[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 laitpii component lauto generated [pli 1 ]clk[3]	40.000	0.239	79.285
	-39.023	VGA Controller:vga_inst/second_r[3]	VGA_Controller:vga_inst(oVGA_R[2]	u6 altpli_component auto_generated pli1 ck(3)	u6 laitpii component lauto generated [pli 1 kk[3]	40.000	0.239	79.261
	-38.986	VGA Controller:vga instisecond r[4]	VGA_Controller:vga_inst joVGA_R[2]	u6 laltpli_component   auto_generated  pli 1  clk [3]	u6-laitpil component lauto generated [pil 1  ck[3]	40.000	0.239	79.224
0	-38,984	VGA Controller:vga instisecond r[3]	VGA Controller:vga instioVGA G[2]	u6 jaitpli_component jauto_generated [pli1]ck[3]	u6 laitpil component lauto generated [pil 1 lck[3]	40.000	0.239	79.222
1	-38,947	VGA Controller:vga instisecond r[4]	VGA Controller:vga instioVGA G[2]	u6 altpli_component auto_generated pli1 ck(3)	u6-laitpil componentiauto generated [pli1]ck[3]	40.000	0.239	79.185
2	-38.901	VGA Controller:vga instisecond r[1]	VGA Controller:vga instioVGA 8[2]	u6 altpli component auto generated [pli1] ck[3]	utilaltpli componentiauto generatedipli [ick[3]	40.000	0.240	79.140
3	-38,888	VGA Controller:vga instisecond r[5]	VGA Controller:vga instioVGA R[2]	u6 altpli component auto_generated pli1 ck(3)	u6-laitpil component lauto generated [pli1] ck[3]	40.000	0.239	79.126
4	-38.873	VGA Controller:vga instisecond r[2]	VGA Controller:vga instigVGA 8[2]	u6 laltpli componentiauto generated [pl 1] ckf [i]	u6-laitpil componentiauto generatedipil1[ck[3]	40.000	0.240	79.112
5	-38.849	VGA Controllerryga instisecond r[6]	VGA Controller:vga instioVGA R[2]	u6ialtpli componentiauto generatedipli1icki1il	u6-laltpil componentiauto generated [pl 1 lck[3]	40,000	0.239	79.087
6	-38.849	VGA Controllerryga instisecond r[5]	VGA Controller:vga instioVGA G[2]	u6laltpli componentiauto generatedipli1ick[3]	u6-laitpil component lauto generated [pl 1 lck[3]]	40,000	0.239	79.087
7	-38,810	VGA Controller;vga instisecond r[6]	VGA Controller:vga instioVGA G[2]	u6 laitpil component lauto generated [pil 1 lcki 3]	u6 laitpil componentiauto generated [pl 1 lckf3]	40,000	0.239	79.048
В	-38.810	VGA Controller; vga instisecond r[3]	VGA Controllerryga instiloVGA 8[2]	u6 laltpli component lauto generated [pli] 1 lcki 3	u6.laltpli component lauto generated [pl 1 ldk[3]]	40,000	0.240	79.049
9	-38,773	VGA Controllerivga instisecond r[4]	VGA Controller:vga instiloVGA B[2]	u6 laltpll component lauto generated [pl 1 lck/3]	u6 altpl component lauto generated ipl 1 idk[3]	40,000	0.240	79.012
0	-38.772	VGA Controller:yga instisecond r[7]	VGA Controller:vga insticVGA R[2]	u6 altpli component lauto generated (pl 1 icki 3)	u6 altpl component lauto generated ipl 1 ick [3]	40,000	0.239	79.010
1	-38,733	VGA Controllerivga instisecond r[7]	VGA_Controller:vga_inst[oVGA_G[2]	u6 altoli componentiauto generated (oli 1 icki 3)	u6 altpl component lauto generated ipl 1 ick [3]	40,000	0.239	78.971
2	-38.675	VGA_Controller.vga_inst second_r[5]	VGA_Controller:vga_inst(oVGA_B[2]	u6 altoli componentiauto generatedioli 1 (ck/3)	u6ialtpli componentiauto generated pli i jok 3]	40,000	0.240	78.914
3	-38.636	VGA Controllerivga instisecond rf61	VGA Controller:vga_rist(oVGA B[2]	u6 altoli componentiauto generatedipii (icki3)	u6ialtoli componentiauto generated (oli 1 ick [3]	40,000	0.240	78.875
4	-38,559	VGA Controller:vga_instisecond_r[7]	VGA Controller:vga instigVGA B[2]	u6 altoli componentiauto generated pli 1 (ck/3)	u6.altpil component lauto generated pil 1 (ck/3)	40.000	0.240	78.798
5	-37.517	VGA Controller:vga_instisecond_r[0]	VGA Controller:vga instioVGA R[3]	u6 altoli componentiauto generatedioli 1 (ck/3)	u6 altoli componentiauto generated (pli 1 (ck (3)	40.000	0.301	77.817
6	-37.400			u6 altoli component lauto generated pli 1 (cki 3) u6 laltoli component lauto generated (cli 1 icki 3)	us jarbii_component jauto_generated pii 1 [ck[3] uS laltoli_component lauto_generated [ol 1 [ck[3]]	40,000	0.301	77.645
7		VGA_Controllerryga_inst[second_r[0]	VGA_Controller:vga_inst[oVGA_G[3]					77.666
	-37.365	VGA_Controller:vga_inst[second_r[1]	VGA_Controller:vga_inst[oVGA_R[3]	u6 altpli_component auto_generated pli1 ck(3)	u6 altpll_component auto_generated pll1 ck[3]	40.000	0.302	77.638
В	-37.337	VGA_Controller:vga_inst[second_r[2]	VGA_Controller:vga_inst]oVGA_R[3]	u6 altpli_component auto_generated pli1 ck[3]	u6 altpli_component auto_generated pli1 dk[3]	40.000	0.302	
9	-37.274	VGA_Controller:vga_inst(second_r(3)	VGA_Controller:vga_inst]oVGA_R[3]	u6 altpli_component auto_generated pli1 clk[3]	u6 altpli_component auto_generated pli1 dk[3]	40.000	0.302	77.575
0	-37.248	VGA_Controller:vga_inst(second_r[1]	VGA_Controller:vga_inst joVGA_G[3]	u6 altpli_component auto_generated pli1 ck(3)	u6 altpli_component auto_generated pli1 clk[3]	40.000	0.247	77.494
1	-37.237	VGA_Controller:vga_inst(second_r[4]	VGA_Controller:vga_inst  oVGA_R[3]	u6 altpli_component auto_generated pli1 clk[3]	u6 altpli_component auto_generated pli1 clk[3]	40.000	0.302	77.538
2	-37.220	VGA_Controller:vga_inst(second_r[2]	VGA_Controller:vga_inst(oVGA_G[3]	u6 altpli_component auto_generated pli1 clk[3]	u6 altpli_component auto_generated pli1 clk[3]	40.000	0.247	77.466
3	-37.157	VGA_Controller:vga_inst(second_r[3]	VGA_Controller:vga_inst[oVGA_G[3]	u6 altpli_component auto_generated pli1 ck(3)	u6 aitpil_component auto_generated pil1 ck[3]	40.000	0.247	77.403
4	-37, 139	VGA_Controller:vga_inst(second_r[5]	VGA_Controller:vga_inst(oVGA_R[3]	u6 altpli_component auto_generated pli1 clk[3]	u6 altpli_component auto_generated pli1 dk[3]	40.000	0.302	77.440
5	-37.120	VGA_Controller:vga_inst second_r[4]	VGA_Controller:vga_inst(oVGA_G[3]	u6 altpli_component auto_generated(pli1 ck(3)	u6 altpli_component auto_generated pli1 clk[3]	40.000	0.247	77.366
6	-37, 100	VGA_Controller:vga_inst(second_r[6]	VGA_Controller:vga_inst(oVGA_R[3]	u6 altpli_component auto_generated pli1 ck[3]	u6 altpll_component auto_generated pll1 ck[3]	40.000	0.302	77.401
7	-37.023	VGA_Controller:vga_inst second_r[7]	VGA_Controller:vga_inst oVGA_R[3]	u6 altpli_component auto_generated pli1 ck(1)	u6 altpli_component auto_generated pli1 (ck [3]	40.000	0.302	77.324
8	-37.022	VGA_Controller:vga_inst second_r[5]	VGA_Controller:vga_inst(oVGA_G[3]	u6 altpli_component auto_generated pli1 ck(3)	u6 altpli_component auto_generated pli 1 [ck [3]	40.000	0.247	77.268
9	-36.983	VGA_Controller:vga_inst second_r[6]	VGA_Controller:vga_inst(oVGA_G[3]	u6 altpll_component auto_generated pll1 ck[3]	u6  altpil_component  auto_generated  pil 1  ck [3]	40.000	0.247	77.229
0	-36.934	VGA_Controller:vga_inst(second_r[0])	VGA_Controller:vga_inst(oVGA_B(3)	u6 altpll_component auto_generated pll1 clk[3]	u6 jaltpli_component jauto_generated jpli 1 jck [3]	40.000	0.239	77.172
1	-36,906	VGA_Controller:vga_inst second_r[7]	VGA_Controller:vga_inst[oVGA_G[3]	u6 altpli_component auto_generated pli1 ck[3]	u6 altpll_component auto_generated pll1 ck[3]	40.000	0.247	77.152
2	-36.782	VGA_Controller:vga_inst(second_r[1]	VGA_Controller:vga_inst(oVGA_B[3]	u6 altpli_component auto_generated pli1 ck(3)	u6 jaitpil_component jauto_generated jpil 1 jck [3]	40.000	0.240	77.021
3	-36,754	VGA Controller:vga instisecond r[2]	VGA_Controller:vga_inst(oVGA_B(3)	u6 laltpli component lauto generated [pli 1 lck/3]	u6 laitpil component lauto generated [pli1] ck[3]	40.000	0.240	76,993

	Clock	Slack	End Point TNS
1	u6 altpll_component auto_generated pll1 clk[3]	-2.549	-13.448
2	enet0_rx_dk_125m	0.518	0.000
3	altpll_component auto_generated pll1 clk[1]	1.010	0.000
4	altpll_component auto_generated pll1 clk[0]	2.256	0.000
5	enet0_tx_clk_125m	5.174	0.000
6	pll altpll_0 sd1 pll7 clk[0]	6.366	0.000
7	altera_reserved_tck	17.183	0.000
8	CLOCK2_50	17.752	0.000
9	pll altpll_0 sd1 pll7 clk[1]	4993.997	0.000

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Dela
-2.549	VGA_Controller:vga_inst(second_r[0]	VGA_Controller:vga_inst[oVGA_R[2]	u6 altpli_component auto_generated pl11 dk(3)	u6 altpli_component auto_generated pli1 ck(3)	40.000	0.132	42.668
-2.522	VGA_Controller:vga_inst(second_r(0)	VGA_Controller:vga_inst[oVGA_G[2]	u6 altpli_component auto_generated pli1 clx[3]	u6 altpli_component auto_generated pl1 ck(3)	40.000	0.132	42.641
-2.456	VGA_Controller:vga_inst(second_r[0])	VGA_Controller:vga_inst[oVGA_B[2]	u6 altpl_component auto_generated pl1 ck(3)	u6 altpli_component auto_generated pli1 ck(3)	40.000	0.133	42.576
-2.456	VGA_Controller:vga_inst[second_r[1]	VGA_Controller:vga_inst[oVGA_R[2]	u6 altpl_component auto_generated pl1 ck(3)	u6 Jaltpli_component Jauto_generated [pli1]ck[3]	40.000	0.132	42.575
-2.429	VGA_Controller:vga_inst[second_r[1]	VGA_Controller:vga_inst[oVGA_G[2]	u6 altpl_component auto_generated pl1 ck(3)	u6 laitpil_component   auto_generated  pil 1  cik[3]	40.000	0.132	42.548
-2.404	VGA Controller:vga instisecond r[3]	VGA Controller:vga inst[oVGA R[2]	u6 jaitpil component jauto_generated [pii 1 jck [3]]	u6 laitpii component lauto_generated [pii 1 [cik[3]]	40.000	0.132	42.523
-2.377	VGA Controller:vga instisecond r[3]	VGA Controller:vga instjoVGA G[2]	u6 jaitpil component jauto generated [pli1]ck[3]	u6 laltpli component lauto_generated [pli1]ck[3]	40.000	0.132	42.496
-2.363	VGA Controller:vga instisecond r[1]	VGA Controller:vga instloVGA B[2]	u6 laltpli_component lauto_generated [pli1] ck(3)	u6 laltpli_component lauto_generated [pli1]ck[3]	40.000	0.133	42.483
-2.345	VGA Controller:vga instisecond r[2]	VGA Controller:vga instloVGA R[2]	u6 laltpli component lauto generated [pli 1 lck [3]]	u6 laltpli component lauto generated [pli1] ck[3]	40.000	0.132	42.464
-2.326	VGA_Controller:vga_inst[second_r[5]	VGA_Controller:vga_inst(oVGA_R[2]	u6 laltpli component lauto generated [pli] ick[3]	u6 laltpl component lauto generated [pl 1 lck [3]]	40.000	0.132	42,445
-2.318	VGA_Controller:vga_inst(second_r[2]	VGA Controller:vga instloVGA G[2]	u6 laltpl component lauto generated [pl 1 lck [3]]	u6 laltal component lauto generated [pl ] [ck [3]	40.000	0.132	42,437
-2.311	VGA Controllerryga instisecond r[3]	VGA Controllerivge instloVGA B[2]	u6laltpl componentiauto generatediplilick[3]	u6 laltpl component lauto generated [pl 1 lck[3]	40,000	0.133	42,431
-2,299	VGA Controllerryga instisecond r[5]	VGA Controller:vga instloVGA G[2]	u6laltpl componentiauto generatediplitick[3]	u6 laltal component lauto generated [pl ] ick[3]	40,000	0.132	42,418
-2,287	VGA Controllerryga instisecond r[4]	VGA Controller:vga instloVGA R[2]	u6 laltpl component lauto generated [pl 1 lck/3]	u6 laltal component lauto generated [pl 1 lck/3]	40,000	0.132	42,406
-2,260	VGA_Controller:vga_inst second_r[4]	VGA_Controller:vga_inst[oVGA_G[2]	u6 altpl_component auto_generated pl1 ck(3)	u6 altpl_component auto_generated pl1 ck[3]	40,000	0.132	42,379
-2,258	VGA_Controller:vga_inst[second_r[7]	VGA_Controller:vga_inst[oVGA_R[2]	u6 altpl_component auto_generated pl1 clk[3]	u6 altpl_component auto_generated pl1 ck[3]	40,000	0.132	42,377
-2.252	VGA_Controller:vga_inst[second_r[2]	VGA_Controller:vga_inst[oVGA_B[2]	u6 altpl_component auto_generated pl1 clk[3]	u6 altpl_component auto_generated pl1 ck(3)	40,000	0.133	42,372
-2.233	VGA_Controller:vga_inst[second_r[5]	VGA_Controller:vga_inst[oVGA_B[2]	u6 Jalipil_component jauto_generated [pli1] clk[3]	u6 jaltpl_component jauto_generated [pl 1   ck [3]	40,000	0.133	42,353
-2.231	VGA_Controller:vga_inst second_r[7]	VGA_Controller:vga_inst(oVGA_G[2]	u6 altpl component auto_generated pli1 [ck[3]	u6 Jaltol _component  auto _generated  pl 1  clk[3]	40,000	0.132	42,350
-2.208	VGA_Controller:vga_inst[second_r[6]]	VGA Controller:vga inst[oVGA R[2]	u6 laltpl component auto_generated [pl1]ck[3]	u6 laltpli component lauto_generated [pli1]clk[3]	40.000	0.132	42.327
-2.194	VGA Controller:vga instisecond r[4]	VGA Controller:vga inst[oVGA B[2]	u6 laltpl component lauto_generated [pl 1   ck [3]	u6 laltpl component lauto_generated [pl 1 lck[3]	40.000	0.133	42.314
-2.181	VGA Controller:vga instisecond r[6]	VGA Controller:vga instioVGA G[2]	u6 laltpli component lauto_generated [pli1]clk[3]	u6 laitol component lauto generated [pl 1 lck[3]	40.000	0.132	42.300
-2.165	VGA Controller:vga instisecond r[7]	VGA Controller:vga instioVGA B[2]	utilaltpl componentiauto generatediplilick[3]	u6 laltpli component lauto generated [pli1 lck[3]	40.000	0.133	42.285
-2.115	VGA_Controller:vga_inst second_r[6]	VGA Controller:vga instioVGA B[2]	utilaltal componentiauto generated plilick[3]	u6 laltol component lauto generated [pl 1 lck[3]]	40.000	0.133	42,235
-1.668	VGA Controller;vga instisecond r[0]	VGA Controller:vga instioVGA R[3]	u6-laltpl component lauto generated [pl 1 lck[3]]	u6 laltol component lauto generated [pl 1 lck[3]	40.000	0.169	41.824
-1.590	VGA Controller;vga instisecond rii0)	VGA Controller:vga instioVGA G[3]	u6laltpl componentiauto generatedipl1ick(3)	u6 laltoli componentiauto generated [pli] 1 ick[3]	40.000	0;136	41.713
-1.575	VGA Controller;vga instisecond r[1]	VGA Controllerivga instiloVGA R[3]	u6laltpl componentiauto generatedipl1ick(3)	u6 laitoli componentiauto generated [pl 1 lck[3]]	40.000	0.169	41.731
-1,523	VGA_Controllerryga_inst(second_r[3]	VGA_Controller:vga_inst(oVGA_R[3]	u6 altpl_component auto_generated pl1 clk[3]	u6 jaitpl_component jauto_generated jpl 1 [clk[3]	40,000	0.169	41,679
-1,497	VGA_Controller:vga_inst second_r[1]	VGA_Controller:vga_inst(oVGA_G[3]	u6 altpl_component auto_generated pl1 dk[3]	u6 jaitpl_component jauto_generated jpl 1 jclk[3]	40,000	0,136	41,620
-1,464	VGA_Controller:vga_inst[second_r[2]	VGA_Controller:vga_inst(oVGA_R[3]	u6 altpl_component auto_generated pl1 clk[3]	u6 jaitpl_component jauto_generated jpl1 jclk[3]	40.000	0.169	41.620
-1.445	VGA_Controller:vga_inst(second_r[5]	VGA_Controller:vga_inst(oVGA_R[3]	u6 altpl_component auto_generated pl1 clk[3]	u6 laltoli componentiauto generated [oli 1 lck/3]	40.000	0.169	41.601
-1,445	VGA_Controller:vga_inst[second_r[3]	VGA_Controller:vga_inst(oVGA_G[3]	u6 jaltpll_component jauto_generated [pli1]clk[3]	u6 jaitpl_component jauto_generated jpl 1 jclk[3]	40.000	0.136	41.568
-1,406	VGA_Controller:vga_inst[second_r[4]	VGA_Controller:vga_inst[oVGA_R[3]	u6 jaltp8_component jauto_generated [p81] clk [3]	u6 jaitpl component jauto_generated jpl 1 jclk[3]	40.000	0.169	41.562
-1.386	VGA Controller:vga instisecond r[2]	VGA Controller:vga insticVGA G[3]	u6 jaltp8_component jauto_generated [p81] clk[3]	u6 jaitpl component jauto_generated jpl 1 jclk[3]	40.000	0.136	41.509
-1.377	VGA Controller:vga instisecond r[7]	VGA_Controller:vga_inst(oVGA_R[3]	u6 laltpl _component lauto_generated [pl 1   clk [3]	u6 jaitpil component jauto_generated jpli 1 jclk[3]	40.000	0.169	41.533
-1.367	VGA Controller:vga instisecond r[5]	VGA Controller:vga insticVGA G[3]	u6 laitoli component jauto generated [pli1] clk[3]	u6-ialtpl component jauto generated [pl11ck[3]	40.000	0.136	41.490
-1.333	VGA Controller:vga instisecond r[0]	VGA Controller:vga instigVGA B[3]	u6.ialtpl. component jauto_generated [pl.1.ick[3]	u6.iaitpl component lauto generated ipl 1 iclk[3]	40.000	0.133	41.453
-1.328	VGA_Controller:vga_inst second_r[4]	VGA Controller:vga instloVGA G[3]	u6.laltpl .component.lauto .generated.lpl1.lclk[3]	u6 laitpil component lauto generated ipil 1 ick[3]	40.000	0.136	41.451
-1.327	VGA Controllerryga instisecond r[6]	VGA Controllerryga insticVGA R[3]	u6 laltol component lauto generated [pl ] lick[3]	u6 laltpl component lauto generated [pl 1 lck[3]	40.000	0.169	41,483
-1,299	VGA Controllerryga instisecond r[7]	VGA Controller:vga insticVGA G[3]	u6.laltpl component lauto generated [pl 1 ick [3]	u6 laltpl component lauto generated [pl 1 lck[3]	40.000	0,136	41,422
-1.249	VGA_Controllerryga_inst second_r[6]	VGA_Controller:vga_inst(oVGA_G[3)	u6 altpl_component auto_generated pl 1 [ck(3)]	u6 altpl_component auto_generated pl1 ck[3]	40.000	0.136	41.372
-1.240	VGA_Controllerryga_inst second_r[1]	VGA_Controller:vga_inst(oVGA_B[3]	u6 jaltpl_component jauto_generated [pl 1 jck(3)]	u6 altpl_component auto_generated pl1 ck[3]	40.000	0.133	41,360
	VGA Controlleruna instiserand r[3]	VGA Controller vna instinVGA R[3]	u6laital componentiauto generatedial tidi(3)	u6 laithii component lauto, generated inii 1 idir [3]	40.000	0.133	41,308

===	Minimum Pulse Width: 'altpll_component auto_generated pll1 clk[1]'
-	Minimum Pulse Width: 'enet0_tx_dk_125m'
-	Minimum Pulse Width: 'enet1_rx_dk_125m'
-	Minimum Pulse Width: 'enet1_tx_dk_125m'
-	Minimum Pulse Width: 'pll altpll_0 sd1 pll7 clk[0]'
-	Minimum Pulse Width: 'CLOCK2_50'
	Minimum Pulse Width: 'CLOCK_50'
	Minimum Pulse Width: 'CLOCK3_50'
-	Minimum Pulse Width: 'altera_reserved_tck'
-	$\label{thm:minimum} \mbox{Minimum Pulse Width: $$'u6$  altpll\_component$  auto\_generated$  pll 1$  clk[3]$'}$
-	Minimum Pulse Width: 'ENETCLK_25'
	Minimum Pulse Width: 'pll altpll_0 sd1 pll7 clk[1]'
> 🗀 Dat	tasheet Report
■ Me	tastability Summary
multicon	rner Timing Analysis Summary
Multicor	rner Datasheet Report Summary
Advance	ed I/O Timing
Clock T	ransfers
Report	TCCS
Report	RSKM
- Uncons	trained Paths
Managan	

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
	✓ Worst-case Slack	-47.795	0.116	1.651	0.557	3.379
	CLOCK2_50	15.331	0.183	N/A	N/A	9.445
	CLOCK3 50	N/A	N/A	N/A	N/A	16.000
	CLOCK_50	N/A	N/A	N/A	N/A	9.574
	ENETCLK_25	N/A	N/A	N/A	N/A	36.000
5	altera_reserved_tck	13.878	0.183	18.245	0.557	19.457
	altpll_component auto_generated pll1 clk[0]	0.463	0.116	3.766	0.752	3.683
,	altpll_component auto_generated pll1 clk[1]	0.022	6.456	N/A	N/A	3.790
	enet0_rx_clk_125m	0.518	0.142	1.651	0.824	3.379
9	enet0_tx_dk_125m	3.700	4.445	N/A	N/A	3.790
10	enet1_rx_clk_125m	N/A	N/A	N/A	N/A	4.000
11	enet1_tx_clk_125m	N/A	N/A	N/A	N/A	3.790
12	pll altpll_0 sd1 pll7 clk[0]	2.503	0.139	N/A	N/A	4.682
13	pll altpll_0 sd1 pll7 clk[1]	4988.181	0.180	N/A	N/A	4999.699
14	u6 altpll_component auto_generated pll1 dk[3]	-47.795	0.179	N/A	N/A	19.682
2	➤ Design-wide TNS	-960.272	0.0	0.0	0.0	0.0
L	CLOCK2_50	0.000	0.000	N/A	N/A	0.000
2	CLOCK3_50	N/A	N/A	N/A	N/A	0.000
3	CLOCK_50	N/A	N/A	N/A	N/A	0.000
	ENETCLK_25	N/A	N/A	N/A	N/A	0.000
5	altera_reserved_tck	0.000	0.000	0.000	0.000	0.000
5	altpll_component auto_generated pll1 clk[0]	0.000	0.000	0.000	0.000	0.000
7	altpll_component auto_generated pll1 clk[1]	0.000	0.000	N/A	N/A	0.000
3	enet0_rx_dk_125m	0.000	0.000	0.000	0.000	0.000
,	enet0_tx_dk_125m	0.000	0.000	N/A	N/A	0.000
10	enet1_rx_clk_125m	N/A	N/A	N/A	N/A	0.000
11	enet1_tx_dk_125m	N/A	N/A	N/A	N/A	0.000
12	pll altpll_0 sd1 pll7 dk[0]	0.000	0.000	N/A	N/A	0.000
13	pll altpll_0 sd1 pll7 clk[1]	0.000	0.000	N/A	N/A	0.000
14	u6 altpll_component auto_generated pll1 dk[3]	-960.272	0.000	N/A	N/A	0.000

Unconstrained Paths						
	Property	Setup	Hold			
1	Illegal Clocks	0	0			
2	Unconstrained Clocks	1	1			
3	Unconstrained Input Ports	28	28			
4	Unconstrained Input Port Paths	43	43			
5	Unconstrained Output Ports	88	88			
6	Unconstrained Output Port Paths	187	187			

#### 6. Reflection and Feedback

### (1) Reflection

At the beginning of our final project, we assumed that implementing the basic functions would be relatively straightforward. However, we encountered a number of unexpected challenges as we began working through them.

We initially had a USB controller that could connect to the Nintendo Switch, but it did not adhere to any known protocol, making it difficult to interpret its communication patterns. As a result, we decided to build our own controller from scratch. We considered using a rotary encoder to detect input signals, but since it only measures relative motion rather than absolute position, we ultimately opted for a potentiometer. To process its output, we used the ADS1115 analog-to-digital converter, which communicates with the FPGA via the I<sup>2</sup>C protocol. Unfortunately, the ADS1115 datasheet lacked a clear explanation of the I<sup>2</sup>C communication details, so we relied on an Arduino library and a logic analyzer to decode the messages successfully.

Next, we tackled the Ethernet connection between the FPGA board and our PC. We followed instructions from a GitHub repository outlining how to implement Ethernet communication on an FPGA. However, our unfamiliarity with computer networking made it difficult to configure the settings and set up the necessary clock signals. After extensive trial and error, we managed to establish a connection. One limitation we encountered was our inability to control the timing of outbound messages from the FPGA. The original setup only allowed the FPGA to send a response immediately after receiving data from the PC. Although we could modify the content of the response, we couldn't decouple it from the timing of the incoming message. Our workaround was to have the PC transmit data at a higher frequency, enabling the FPGA to maintain near real-time communication.

Lastly, we worked on utilizing the SDRAM on the DE2-115 development board. Although we started with the board's sample code, we struggled to control the SDRAM's read and write addresses. As a result, we were only able to use it as a simple buffer. Our original plan was to regulate the output frame rate by selectively reading from specific addresses, but due to these limitations, we had to rely on a Python script to control the frame rate externally by adjusting the speed at which frames were sent.

Although we technically achieved all the intended functionalities, we had to employ several workarounds to overcome challenges we didn't fully understand. In the future, we hope to deepen our understanding of Ethernet communication and SDRAM operations so that we can leverage their full potential and design more robust systems.

## (2) Feedback

Over the course of this semester, we became more familiar with FPGA development and Verilog programming. However, we spent a significant amount of time trying to understand—and at times merely manage to implement—the Ethernet and SDRAM functionalities. To help future students overcome similar challenges more efficiently, we recommend that the TAs offer additional lectures or curated learning resources focused on these topics. This would greatly enhance our ability to implement complex features more effectively and with greater confidence.