# AIR UNIVERSITY DEPARTMENT OF COMPUTING AND AL

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AIR UNIVERSITY	EXPERIMENT NO 7					
LAB TITLE: LAB RE	PORT 7					
STUDENT NAME: Ruhr	na Lodhi		_ REG N	O: <u>230452</u>		
LAB ASSESSMENT:						
Attributes	Excellent (5)	Good (4)	Average (3)	Satisfactory (2)	Unsatisfactory (1)	
Ability to Conduct Experiment						
Ability to assimilate the results						
Effective use of lab equipment and follows the lab safety rules						
Total Marks:		_ Ot	otained Mark	(S:		
LAB REPORT ASSESSM	<u>IEN I:</u>					
Attributes	Excellent (5)	Good (4)	Average (3)	Satisfactory (2)	Unsatisfactory (1)	
Data presentation						
Experimental results						
Conclusion						
Total Marks:		Obta	ined Marks:			

Date:

Signature: \_\_\_

# **Experiment 7**

### Seven Segment display

### **OBJECTIVES:**

• To experimentally check the operation of 7-segment display using BCD to 7-segment decoder 4774.

### Requires component and Equipment's:

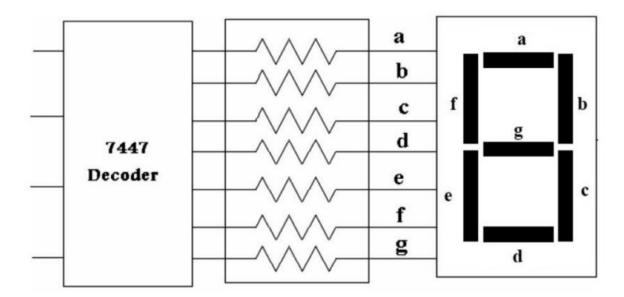
- ICs as required.
- Digital Electronic trainer.

### **Procedure:**

- Check the configuration of your 7-segment display using multi-meter. Find out its configuration and pin-assignment.
- Create the truth table to describing the function of a BCD to 7-segment decoder accordingly to the configuration of your display.

	INF	INPUT			OUTPUT					
A	В	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

1. Design a circuit showing the proper connections of the decoder and the 7-segment display. Invert the outputs of the decoder in case of common cathode display. The output pins of 7447 are connected to the pins of seven segment display chip via resistances as shown below:



**2.** Implement the circuit on the trainer. Enter, BCD numbers from O to 9 and see the corresponding decimal digit on the display.

### **Student Exercise:**

Make K-maps for each of the output of the BCD to 7-segment decoder. Find out the minimal SOP for each output. Design the decoder using minimum number of gates.

Cl	D			
AB \	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

F=A+C+BD+B'D'

### **Equation for "b":**

. C	D			
AB \	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

**F**=B'+C'D'+CD

### **Equation for "c":**

**F**=B+D+C'

Equation for "d":

	, C	D			
AB		00	01	11	10
	00	1	0	1	1
	01	0	1	0	1
	11	X	X	X	X
	10	1	1	X	X

**F**=A+B'C+CD'+B'D'+BC'D

# **Equation for "e":**

\ (	CD			
AB \	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	X	X	X	X
10	1	0	X	X

**F**=CD'+B'D'

### **Equation for "f":**

(	CD			
AB \	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

**F**=A+BD'+BC'+C'D'

**Equation for "g":** 

	CD			
AB \	00	01	11	10
00	0	0	1	1
01	1	0	1	1
11	X	X	X	X
10	1	1	X	X

**F**=A+B+CD'+B'C

