

DD2360

Assignment IV: Advanced CUDA

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Link to github: <https://github.com/RuiShi324/DD2360>

1 Exercise 1 - Thread Scheduling and Execution Efficiency

1. Assume $X=800$ and $Y=600$. Assume that we decided to use a grid of 16×16 blocks. That is, each block is organized as a $2D$ 16×16 array of threads. How many warps will be generated during the execution of the kernel? How many warps will have control divergence? Please explain your answers.

Answer: For each block, there are 16 threads in the horizon and vertical. From the codes, we can see that the organization of the grid will be used as $2D$. So $\lfloor 600/16 \rfloor \times \lfloor 800/16 \rfloor = 37 \times 50 = 1850$ thread blocks will be used, and 50 in x dimension, 37 in y dimension. In y dimension, not all the threads in the last thread block will be executed, only 8 threads will be used. In this case, because of the linearized row-major order, $8 \times 16/32 = 4$ warps will be generated for each thread block, and in total 200 warps will be generated. So for the thread blocks that are fully executed, $37 \times 50 = 1850$ thread blocks will be used and $1850 \times 16 \times 16/32 = 14800$ warps will be generated during the execution of the kernel. In summary, 15000 warps will be generated.

For the last thread block in the y dimension, as discussed before, no thread will have control divergence because of the linearized row-major order.

2. Now assume $X=600$ and $Y=800$ instead, how many warps will have control divergence? Please explain your answers.

Answer: In this case, only 8 threads will be used for the last thread block in the x dimension, because the last 8 threads in x dimension are not in range of the if statement, which causes control divergence. So each warp will have control divergence in this case, $50 \times 8 = 400$ warps will have control divergence.

- Now assume $X=600$ and $Y=799$, how many warps will have control divergence? Please explain your answers.

Answer: In this case, also 1900 blocks will be used, not all the threads will be used for the last thread block in x dimension and y dimension. For the last warp, as all the last threads in y dimension will not be used, it doesn't have control divergence. So 399 warps will have control divergence.

2 Exercise 2 - CUDA Streams

- Compared to the non-streamed vector addition, what performance gain do you get? Present in a plot (you may include comparison at different vector length)

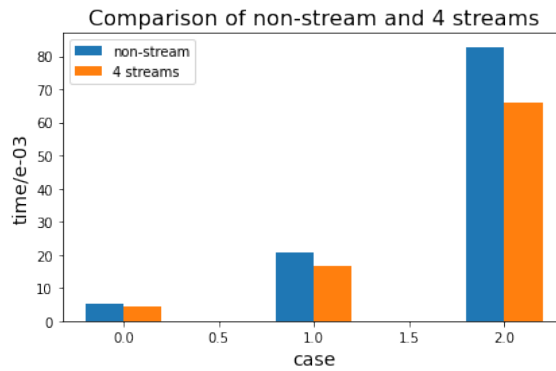


Figure 1: comparison of 4 streams

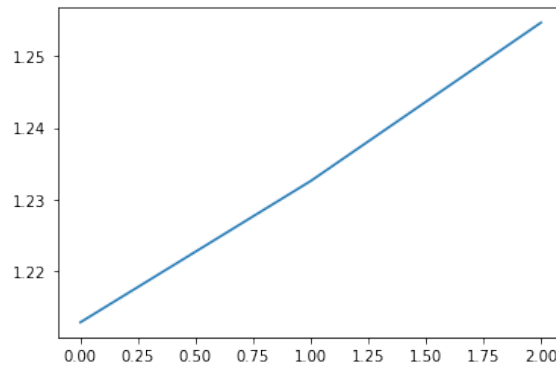


Figure 2: Performance improvement

For non-stream and 4 streams cuda, I set the size of the input vector as 2560000,

10240000 and 40980000. In this range, a larger size of the vector will lead to better improvement of the performance, and it seems to be linear within this range.

2. Use nvprof to collect traces and the NVIDIA Visual Profiler (nvvp) to visualize the overlap of communication and computation. To use nvvp, you can check Tutorial: NVVP - Visualize nvprof Traces

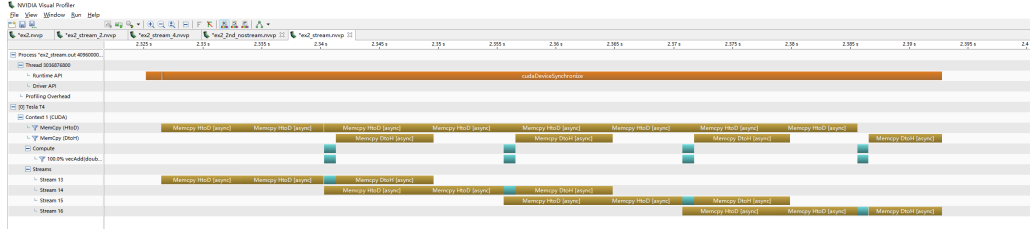


Figure 3: Overlap of communication and computation

3. What is the impact of segment size on performance? Present in a plot (you may choose a large vector and compare 4-8 different segment sizes)

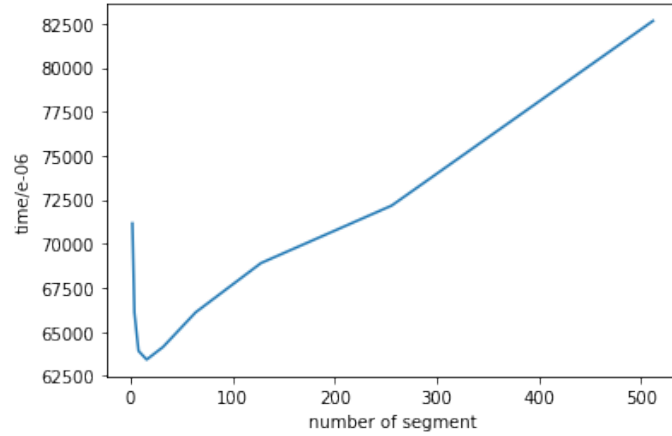


Figure 4: Impact of segment size

From the figure, we can see that at first, more streams could help to improve the performance, as it could be more parallel to save time. However, too many streams will spend more time on task blocking and switching, and especially in this vector addition program, most of the time is spent on memory copy, then too many streams will cost more time, even more time than non-stream Cuda.

3 Exercise 3 - Pinned Memory and Unified Memory

1. What are the differences between pageable memory and pinned memory, what are the tradeoffs?

Answer: Pageable memory is allowed to be paged in or paged out, while pinned memory is not. Too much pageable memory will cause worse performance, as GPU can not directly access it, but pageable memory could extend the space of memory to run more programs.

2. Compare the profiling results between your original code and the new version using pinned memory. Do you see any difference in terms of the breakdown of execution time after changing to pinned memory?

Answer: For the original code, I tested with matrix lengths of 128, 256, 512, and 1024. For the new version of pinned memory, there is no significant difference considering kernel execution. But for memory copy, it spends much less when using pinned memory when the vector length is large.

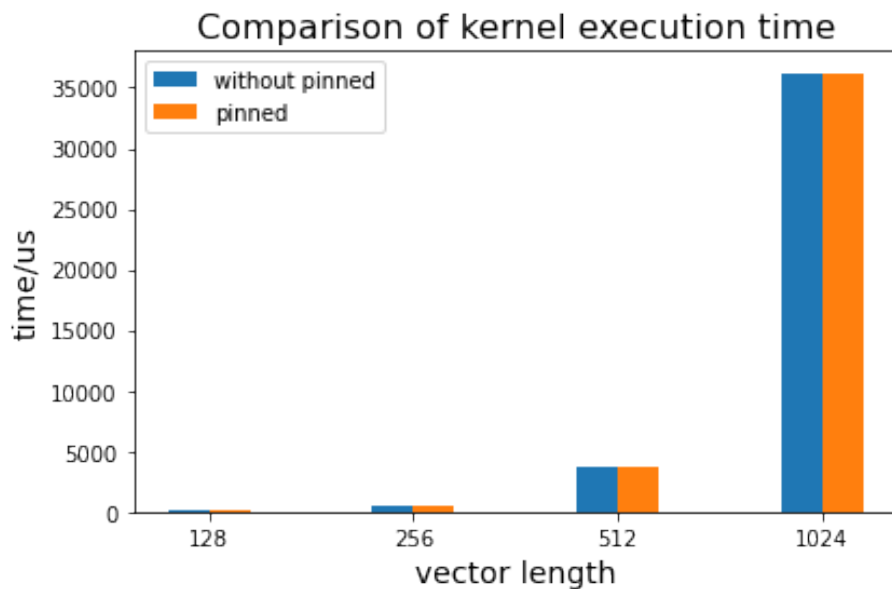


Figure 5: Comparison of kernel execution time

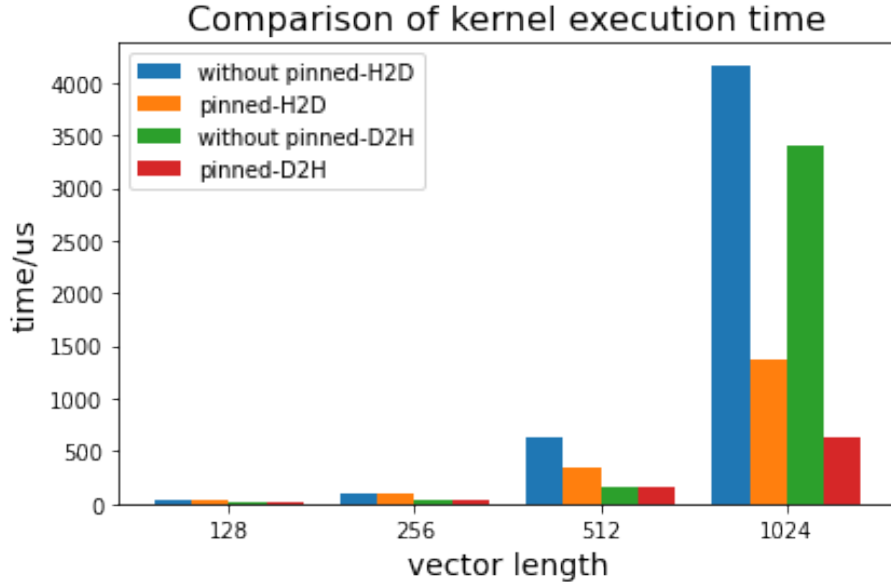


Figure 6: Comparison of memory copy time

As pinned memory on the host allows us to avoid intermediate transfers and achieve higher data transfer rate (bandwidth), it is more efficient when data is larger.

3. What is a managed memory? What are the implications of using managed memory?

Answer: Managed memory is a single memory address space which is accessible from any processor in a system. Allocate data can be read or written from code running on either CPUs or GPUs, and the CUDA system software takes care of migrating memory pages to the memory of the accessing processor.

4. Compare the profiling results between your original code and the new version using managed memory. What do you observe in the profiling results?

Answer: For the version using unified memory, the execution time of the kernel increases significantly, because of the host-to-device page faults, reducing the throughput achieved by the CUDA kernel. So I tried to use Unified Memory prefetching to move the data to the GPU after initializing it, using `cudaMemPrefetchAsync()` for it. After that, the execution time of kernel is similar to the origin version, and it improves the performance because it doesn't need to copy the data from host to device or device to host.

4 Exercise 4 - Heat Equation with using NVIDIA libraries

1. Run the program with different dimX values. For each one, approximate the FLOPS (floating-point operation per second) achieved in computing the SMPV (sparse matrix multiplication). Report FLOPS at different input sizes in a FLOPS. What do you see compared to the peak throughput you report in Lab2?

Answer: For each sparse matrix, there are $3 \times (\dim X - 2)$ non-zero elements in total, so the FLOP can be calculated as the equation 1.

$$FLOP = \frac{no_timesteps * (3 \times (\dim X - 2))}{time_{SMPV}} \quad (1)$$

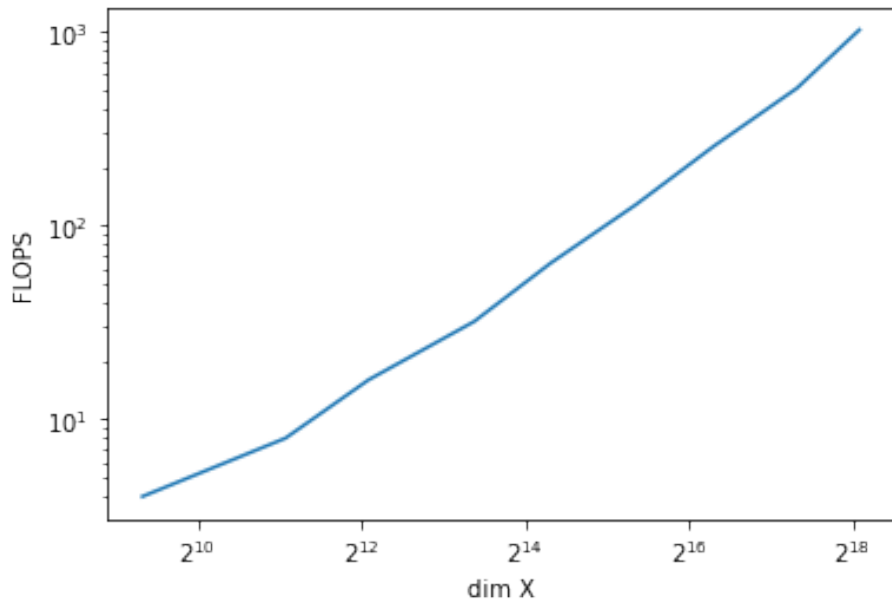


Figure 7: FLOPS at different input sizes

As the figure shown, the larger input size is, the larger FLOP is. However, it will stay stable even increasing the input size, and from the experiments it cannot reach the peak throughput.

2. Run the program with dimX=128 and vary nsteps from 100 to 10000. Plot the relative error of the approximation at different nstep. What do you observe?

Answer: A larger number of timesteps is, a smaller value of relative error is, because the Finite Differences Method can be more accurate to estimate the Heat equation.

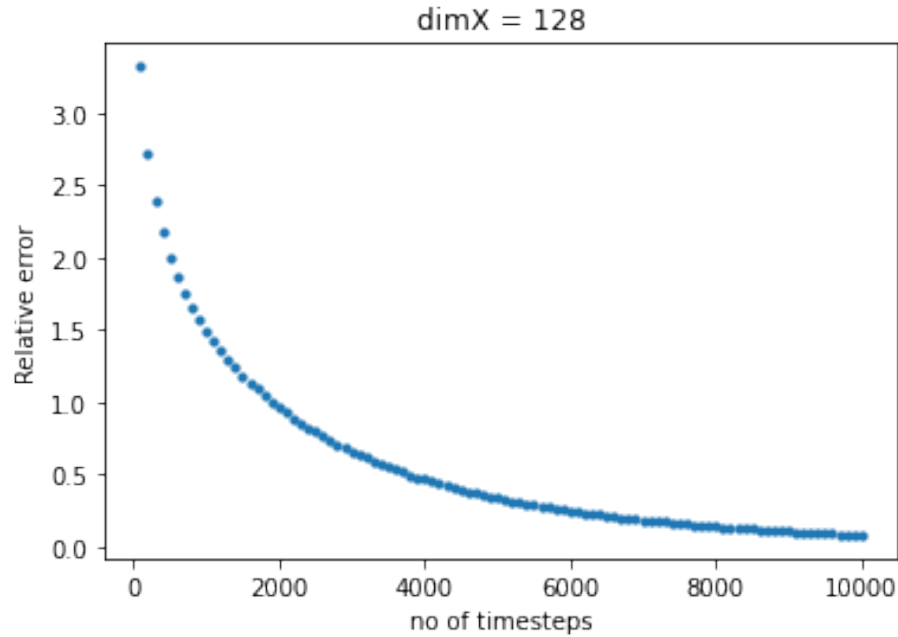


Figure 8: Relative error at different number of steps

3. Compare the performance with and without the prefetching in Unified Memory. How is the performance impact? [Optional: using nvprof to get metrics on UM]

Answer: With prefetching in Unified Memory, the execution time of computing the SMPV decreases from 17917 to 14948 ms, because there is no GPU page fault group, and it is faster to initialize the sparse matrix on the host. And prefetching only takes 46.664 μ s, so it could improve the performance.

[illegible]

Figure 10: With prefetching