|  |  |  |
| --- | --- | --- |
| August 18 - Wednesday | August 19 - Thursday | August 20 - Friday |
| 2:00 –5:00 pm  Half-Day Tutorial 1  Silicon Lifecycle Management for Emerging Memories  Yervant Zorian (Synopsys) | 9:00-9:30am  Opening Session  9:30-10:15am Keynote 1:  How to make chip intelligent–from an architecture perspective  Shaojun Wei (Tsinghua) | 9:00-9:45am Keynote 4:  Ratio based Resistive RAM for Low Error Rate, High Energy Efficiency and In-Memory Computing  Tim Cheng (HKUST)  9:45-10:30am Keynote 5:  Reliability of Carbon-Nanotube FET Circuits: Today’s Challenges and the Road Ahead  Krishnendu Chakrabarty (DUKE) |
| 10:15-10:30am Coffee Break | 10:30-10:45am Coffee Break |
| 10:30-11:15am Keynote 2:  Life-Time Reliability for Memory Devices in AI Chip  Xinli Gu (Huawei)  11:15am-12:00pm Keynote 3:  Towards Robust AI: A Test Perspective  Qiang Xu (CUHK) | 10:45-11:30am Keynote 6:  Emerging Need for Fast Thermal and Dynamic Voltage Drop Predictors for the Optimization of Scan/Functional Test Patterns  Norman Chang (ANSYS)  11:30am -12:30pm RS3, IS3  A4. Circuit Design and Evaluation with Emerging Technology  B4. Diagnosis and Yield Learning |
| 7:00–10:00 pm  Half-Day Tutorial 2  Scan Test Escapes, New Fault Models, and the Effectiveness of Functional System Level Tests  Adit Singh (Auburn University) | 8:00-9:00pm RS1, SS1  A1.When Machine Learning Meets Testing and Security  B1. Fault Tolerant TSV and Latch Designs  9:05-10:05pm RS2, IS1  A2. Fault Monitoring, Detecting, and Modeling  B2. The Advancement of 1149.10  10:10-11:10pm SS2, IS2  A3. Learning based Discovery in ATPG, DfT, and Reverse Engineering  B3. Automotive Test and Reliability | 8:00-9:00pm SS3, IS4  A5. 3D test and 3D DFT  B5. Industry Practice in SoC and Memory Test  9:05-10:25pm SS4, SS5    A6. Test Methods Towards Zero Failure Rate for Safety-Critical ICs  B6. Top Papers of ITC’2020  10:30-10:45pm    Closing Remarks and Best Paper Award |