RUICONG(RAY) CHEN

PhD Candidate of EECS@MIT | raychen@mit.edu | https://ruicong-chen.github.io/

SUMMARY

- I have excellence in analog/mixed-signal/digital chip design with proved record of leading publications such as **VLSI-C 2022**.
- I have experience in complex system design based on custom designed chip with top publication such as **MobiCOM 2020**.
- I have strong technical backgrounds in circuits and system from my 4 years of PhD training at MIT.
- I am co-advised by Prof. **Anantha Chandrakasan** and Prof. **Hae-Seung Lee**.
- I am always curious about new technology and passionate about doing high-impact work.

EDUCATION

- **Ph.D. Candidate**, Department of Electrical Engineering and Computer Science (**EECS**), MIT — *2021-2023, Cambridge, MA*
  - Advisors: Anantha P. Chandrakasan and Hae-Seung Lee
- S.M., Department of Electrical Engineering and Computer Science (EECS), MIT — *2019-2021, Cambridge, MA*
  - Advisors: Anantha P. Chandrakasan and Hae-Seung Lee
- B.S., Department of Electrical Engineering and Computer Science (EECS), Peking University — *2015-2019, Beijing, China*
  - Ranking the 1st in the department

RESEARCH INTERESTS

- **Mixed-signal Application-Specific Integrated Circuit (ASIC) Design**
- Hardware security
- In-memory computing and machine learning

MAIN RESEARCH EXPERIENCE

- Circuit design for secure IoT applications — *July 2021-Present, MIT*
  - Design, simulate, fabricate and test ADCs with side-channel attack resistance
  - Improve the circuit performance with security feature
  - **One work submitted to ISSCC**
  - **One work published on top venue of circuits, VLSI-C**
- Direct hybrid-encoding for signed expressions (HESE) SAR for neuromorphic computing — *Apr 2020-June 2021, MIT*
  - Explore HESE to shorten signed-digit number representations for neuromorphic computing
  - Implement energy-efficient HESE-direct SAR ADC with spare cycles for calibrations
  - **Work published on ISLPED**
- Wireless and Batteryless Micro-Implants — *Sept 2019-Mar 2020, MIT*
  - Design, simulate, fabricate, and test the system with costume designed IC on flexible PCB
  - **Work published on top venue of networking, MobiCOM**

FEATURED PUBLICATIONS

RaM-SAR: A Low Energy and Area Overhead, 11.3fJ/conv.-step 12b 25MS/s Secure Random-Mapping SAR ADC with Power and EM Side-channel Attack Resilience, The 2022 International Symposium on VLSI Circuits (**VLSI-C 2022**)
R.-C Chen, H.-R Wang, A. Chandrakasan, H.-S Lee

A Bit-level Sparsity-aware SAR ADC with Direct Hybrid Encoding for Signed Expressions for AIoT Applications, The 2022 International Symposium on Low Power Electronics and Design (**ISLPED 2022**)
R.-C Chen, H. T. Kung, A. Chandrakasan, H.-S Lee

Enabling Self-Reconfigurability for Wireless and Batteryless Micro-Implant, The 26th Annual International Conference on Mobile Computing and Networking (**MobiCOM 2020**)
M.-R, Abdelhamid, **R.-C Chen**, J.-Y Chou, A. Chandrakasan, F. Adib

SELECTED AWARDS

- Commlab Fellowship — *by MIT School of Engineering*
- National Scholarship 2017 — *by Ministry of Education of the P.R. China*
- Outstanding Graduate in Beijing 2019 — *by Beijing Municipal Commission of Education*
- Outstanding Graduate of Peking University 2019 — *by Peking University*

SERVICE

- Reviewers of TVLSI, T-CAS I and T-CAS II — Current
- Circuit Session Chair of MTL Annual Research Conference (MARC) — 2021
- Commlab Fellow of MIT School of Engineering — 2021-2023

TECHNICAL SKILLS

Programming SKills Python (Pytorch), MATLAB, C/C++
Hardware Skills Verilog, ISE design suit of FPGA, Cadence (Virtuoso, Innovus and Genus), HFSS, SPICE, Eagle, SolidWorks