Common Case

State Clock/ Clock Cycle	1	2	3	4	5	6	7	8	9
SRAM_address	R14 G14	B14 R15	G15 B15	Y 18/19	U 12/13	V 12/13			
SRAM_read_data							Y 18/19	U 12/13	V 12/13
SRAM_write_data	R14 G14	B14 R15	G15 B15						
SRAM_we_n	0(W)	0(W)	0(W)	1(R)	1(R)	1(R)	holding	holding	holding
R_even								16	
G_even									16
B_even							16		
R_odd								17	
G_odd									17
B_odd							17		
Y							Y18/19		
U'_even		U'16							
U'_odd				U'17					
U[(j+5)/2]								12	
U[(j+3)/2]								11	
U[(j+1)								10	

/2]									
U[(j-1)/2]								9	
U[(j-3)/2]								8	
U[(j-5)/2]								7	
V'_even			V'16						
V'_odd				V'17					
V[(j+5)/2]									12
V[(j+3)/2]									11
V[(j+1)/2]									10
V[(j-1)/2]									9
V[(j-3)/2]									8
V[(j-5)/2]									7
Ubuff							U13-	u13	
V buff							V13-		v13
Multiplication	**u(21*)** U11/U6 **v(21*)** V11/V6	**u(52*)** U10/U7 **v(52*)** V10/V7	**u(159*)** U9/U8 **v(159*)** V9/V8	**E(Y)** (76284*Y16) **O(Y)** (76284*Y17)	**E(u')G** (-25624*U'16) **O(u')G** (-25624*U'17)	**E(u')B** (132251*U'16) **O(u')B** (132251*U'17)	**E(v')R** (104595*V'16) **O(v')R** 104595*V'17)	**E(v')G** (-53281*V'16) **O(v')G** (-53281*V'17)	

Lead In

State Clock /Clock Cycle	0	1	2	3	4	5	6	7	8	9	10
SRAM_address	Y0Y1	U0U1	V0V1	U2U3	V2V3						
SRAM_read_data				Y0Y1	U0U1	V0V1	U2U3	V2V3			
SRAM_write_data											R0G0
SRAM_we_n	1	1	1	1	1	1	1	1	1	1	0
R								R0			
G									G0		
B										B0	
Y				Y0Y1							
U’					U0					U1	
U[(j+5)/2]							U3	V3			
U[(j-5)/2]					U0						
U[(j+3)/2]							U2	V2			
U[(j-3)/2]					U0						

U[(j+1)/2]					U1						
U[(j-1)/2]					U0						
V’						V0					
V[(j+5)/2]											
V[(j-5)/2]						V0					
V[(j+3)/2]											
V[(j-3)/2]						V0					
V[(j+1)/2]						V1					
V[(j-1)/2]						V0					

Lead out

State Clock/ Clock Cycle	1	2	3	4	5	6	7	8	9
SRAM_address	R310 G310	B310 R311	G311 B310	Y 314/315	U 314/315	V 314/315			
SRAM_read_data							Y 150/151	U 150/151	V 150/151
SRAM_write_data	R310 G310	B310 R311	G311 B310						
SRAM_we_n	0(W)	0(W)	0(W)	1(R)	1(R)	1(R)	holding	holding	holding
R_even								16	

G_even									16
B_even							16		
R_odd								17	
G_odd									17
B_odd							17		
Y							Y18/19		
U'_even		U'16							
U'_odd				U'17					
U[(j+5)/2]								12	
U[(j+3)/2]								11	
U[(j+1)/2]								10	
U[(j-1)/2]								9	
U[(j-3)/2]								8	
U[(j-5)/2]								7	
V'_even			V'16						
V'_odd				V'17					
V[(j+5)/2]									12
V[(j+3)/2]									11
V[(j+1)/2]									10

V[(j-1)/2]									9
V[(j-3)/2]									8
V[(j-5)/2]									7
Ubuff							U13		
V buff							V13		
Multiplication	**u(21*)** U11/U6 **v(21*)** V11/V6	**u(52*)** U10/U7 **v(52*)** V10/V7	**u(159*)** U9/U8 **v(159*)** V9/V8	**E(Y)** (76284*Y16) **O(Y)** (76284*Y17)	**E(u')G** (-25624*U'16) **O(u')G** (-25624*U'17)	**E(u')B** (132251*U'16) **O(u')B** (132251*U'17)	**E(v')R** (104595*V'16) **O(v')R** 104595*V'17)	**E(v')G** (-53281*V'16) **O(v')G** (-53281*V'17)	

Milestone 2
CC

State Clock/ Clock Cycle	1	2	3	4	5	6	7	8	9
SRAM_address									
SRAM_read_data									
SRAM_write_data									

SRAM_we_n									
Address_0									
Data_in_0									
Write_en_0									
Data_out_0									
Address_1									
Data_in_1									
Write_en_1									
Data_out_1									
S									
S’									
C									