Digital Control in Power Electronics
Regular Sampling & Multisampling Technique on TI f28379D
DQ Step Response HIL vs. Simulink - Three Phase RL Load

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1 Introduction

This document provides a comparison between hardware in the loop (HIL) and Simulink simulation results for regular sampling and multisampling technique implemented on DSP TI F28379. For the purposes of this comparison a single pole system - three phase series RL connection has been used. Current is controlled via Internal Model Principle based current regulator in DQ frame. In terms of update rate (UR) and feedback acquisition (with or without oversampling), eight different cases will be discussed:

OVERSAMPLING	UPDATE RATE
0	1
0	2
0	4
0	8
1	1
1	2
1	4
1	8

Table 1. The cases to be analyzed.

2 HIL vs. Simulink simulation results

2.1 IMC IREG gain $\alpha = 0.04$

Fig. 1-8 show comparison between D & Q current step responses obtained from HIL (data exported from DSP's RAM) and Simulink simulation, for all of the afore mentioned cases when IMC regulator gain is 0.04.

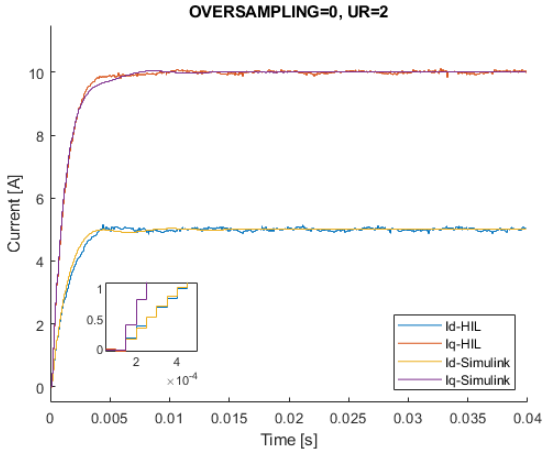

Fig. 1. DQ current step response - HIL vs. Simulink: OVERSAMPLING=0, UR=2.

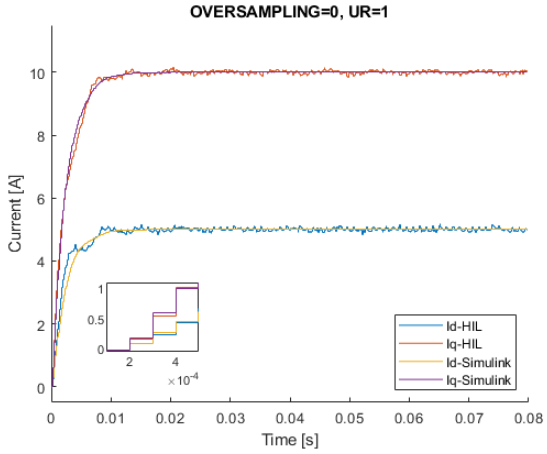

Fig. 2. DQ current step response - HIL vs. Simulink: OVERSAMPLING=0, UR=1.

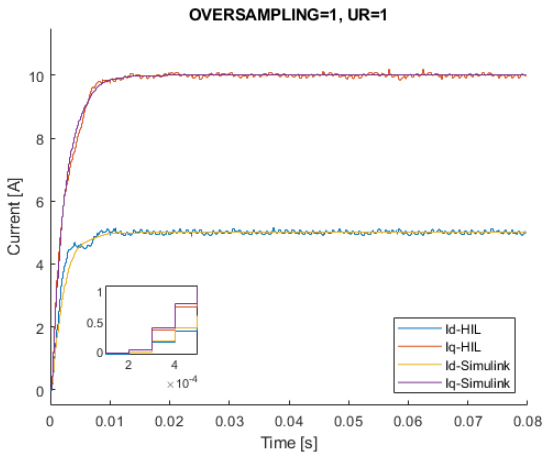

Fig. 3. DQ current step response - HIL vs. Simulink: OVERSAMPLING=1, UR=1.

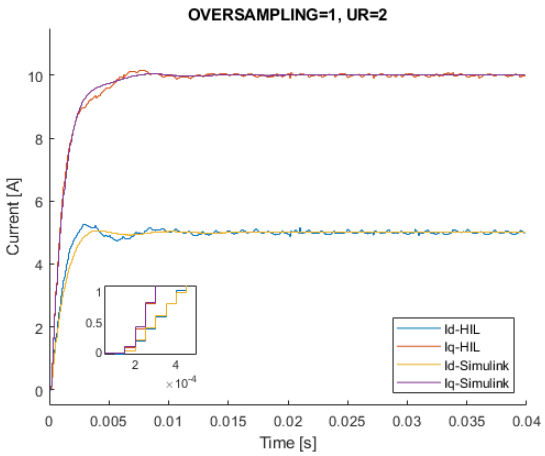

Fig. 4. DQ current step response - HIL vs. Simulink: OVERSAMPLING=1, UR=2.

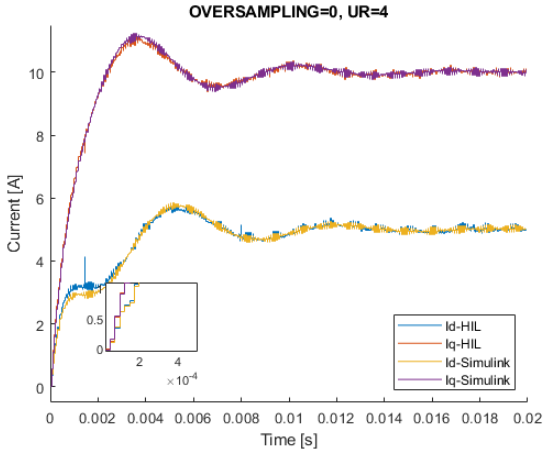

Fig. 5. DQ current step response - HIL vs. Simulink: OVERSAMPLING=0, UR=4.

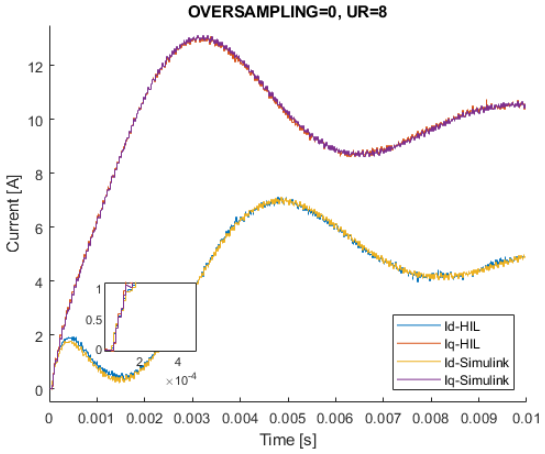

Fig. 6. DQ current step response - HIL vs. Simulink: OVERSAMPLING=0, UR=8.

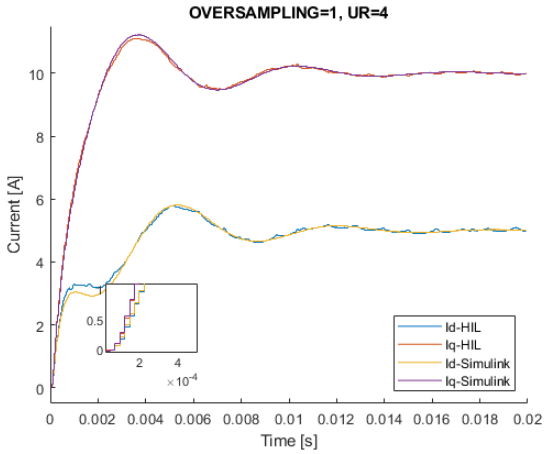

Fig. 7. DQ current step response - HIL vs. Simulink: OVERSAMPLING=1, UR=4.

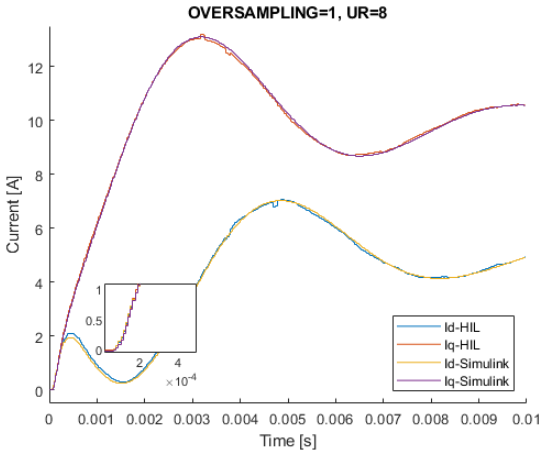

Fig. 8. DQ current step response - HIL vs. Simulink: OVERSAMPLING=1, UR=8.

2.2 IMC IREG gain $\alpha = 0.2$

Fig. 9-12 show comparison between D & Q current step responses obtained from HIL (data exported from DSP's RAM) and Simulink simulation, for $UR = 2$ with and without oversampling when IMC regulator gain is 0.2.

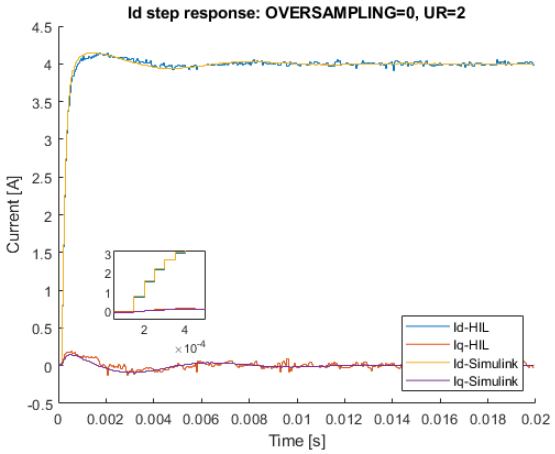

Fig. 9. D current step response - HIL vs. Simulink: OVERSAMPLING=0, UR=2.

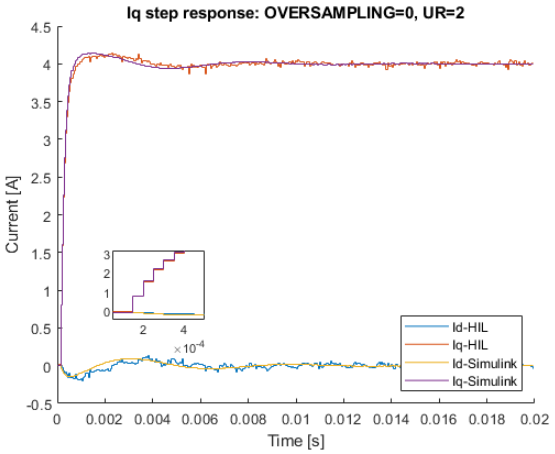

Fig. 10. Q current step response - HIL vs. Simulink: OVERSAMPLING=0, UR=2.

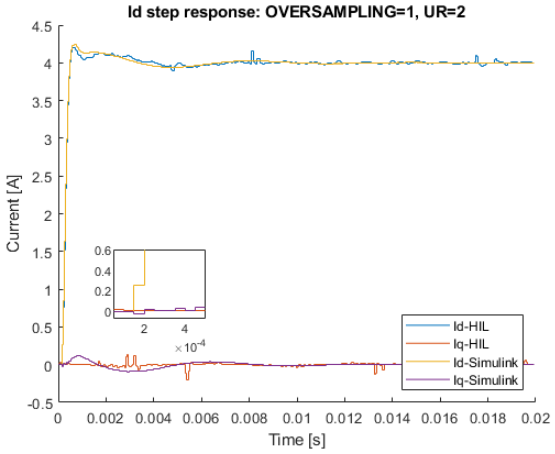

Fig. 11. D current step response - HIL vs. Simulink: OVERSAMPLING=1, UR=2.

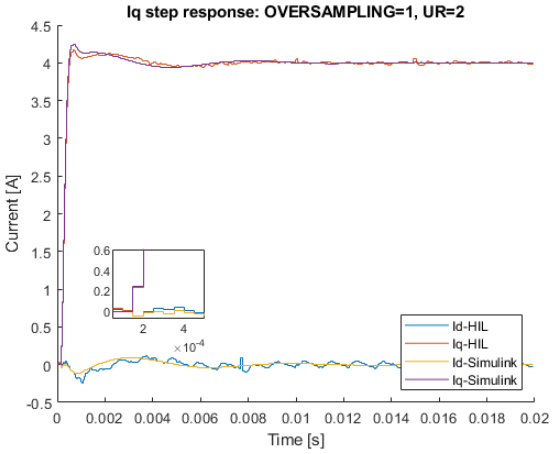

Fig. 12. Q current step response - HIL vs. Simulink: OVERSAMPLING=1, UR=2.