Digital Control in Power Electronics

Regular Sampling Technique on TI f28379D

Experimental Validation on Single Pole System

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August 26, 2020

1 Introduction

This document provides a comparison between simulation and experimental results for regular sampling technique implemented on DSP TI F28379. For the purposes of experimental validation a single pole system - series RC connection - directly driven by PWM output has been used. In terms of update rate (UR) and feedback acquisition, four different cases will be discussed:

- double update rate without oversampling ($OVERSAMPLING = 0$, $UR = 2$)
- single update rate without oversampling ($OVERSAMPLING = 0$, $UR = 1$)
- single update rate with oversampling ($OVERSAMPLING = 1$, $UR = 1$)
- double update rate with oversampling ($OVERSAMPLING = 1$, $UR = 2$)

2 Controller design

For the purposes of capacitor voltage regulation, a voltage controller based on Internal Model Principle is used. Following the procedure described in [1], we arrive at the voltage controller with the following transfer function:

$$W_{reg}(z) = \frac{\alpha}{1-\beta} \cdot \frac{z-\beta}{z-1} \tag{1}$$

where α is a gain of the discrete-time controller and β is a parameter defined by the load time constant:

$$\beta = e^{\frac{T_s}{R \cdot C}} \tag{2}$$

where T_s is the regulation period.

The gain α is set to 0.2, so that with oversampling based feedback acquisition a closed loop bandwidth f_{BW} of $0.0708/T_s$ is achieved, whereas in case without oversampling $f_{BW} = 0.0497/T_s$ [1].

3 Experimental results

In order to examine validity of the DSP configuration, both oscilloscope measurements and simulation runs have been performed. The goal was to compare simulation and experimental results for all four of the afore mentioned cases. MATLAB Simulink has been used to model voltage regulation in discrete time domain, digital pulse width modulation, RC load in continuous time domain, and feedback acquisition.

3.1 Results for $\alpha = 0.2$

Fig. 1-4 show comparison between measured (blue waveform) and simulated (red waveform) capacitor voltage in response to a reference step change (from $0V$ to $0.5V$), for all four of the afore mentioned cases (with or without oversampling and with single or double update rate). As it is clearly noticeable from the attached figures, simulation and experimental results are almost identical. Fig. 5 illustrates a different quality of the step response depending on the update rate and feedback acquisition. Fig. 6 represents a comparison of the control signals (exported from DSP's RAM) for all four cases of interest. According to Fig. 6, regulator is not saturated in any of the discussed cases.

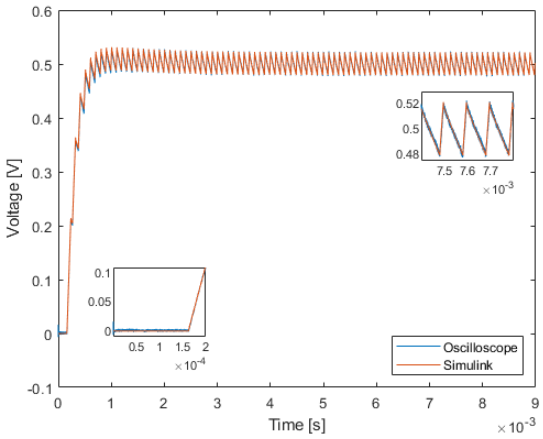

Fig. 1. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=0, UR=2.

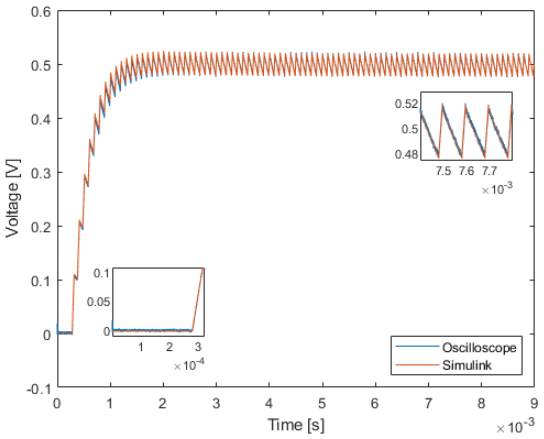

Fig. 2. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=0, UR=1.

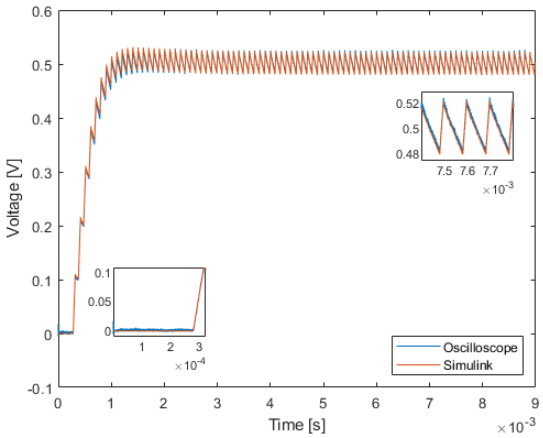

Fig. 3. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=1, UR=1.

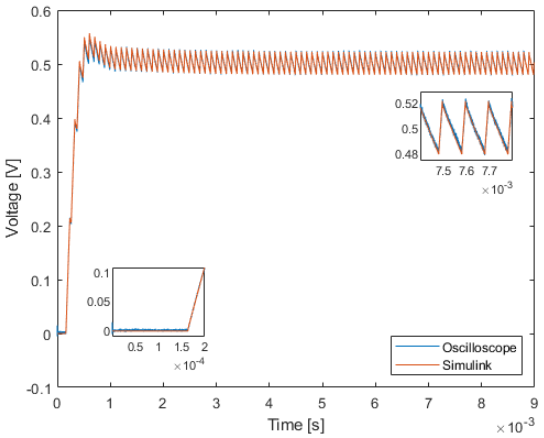

Fig. 4. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=1, UR=2.

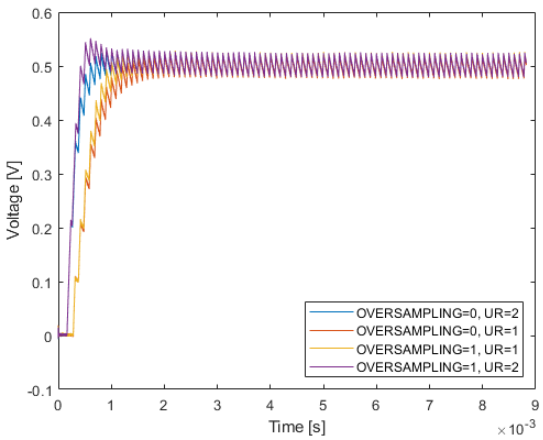

Fig. 5. Capacitor voltage - oscilloscope meas.

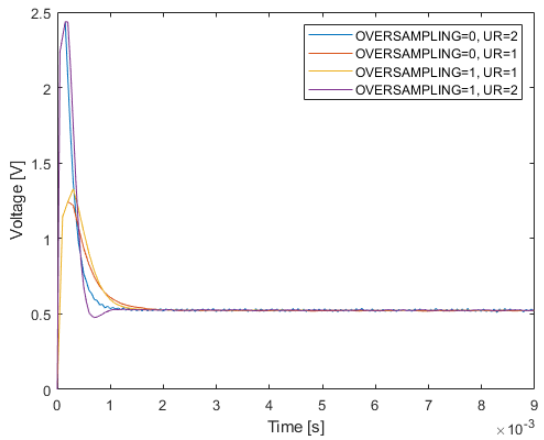

Fig. 6. Control signal - DSP stored data.

3.2 Results for $\alpha = 0.4$

For the purposes of more detailed examination, the controller gain has been set to 0.4 so that the effects of the delays on the step response are more pronounced. Fig. 7-10 show comparison between measured (blue waveform) and simulated (red waveform) capacitor voltage in response to a reference step change (from $0V$ to $0.5V$), in case controller gain α is 0.4. As in the previously analyzed case ($\alpha = 0.2$), differences between simulation and experimental results are hardly noticeable. In this case however, regulator gets saturated (Fig. 12). Fig. 11 illustrates a different quality of the step response depending on the update rate and feedback acquisition.

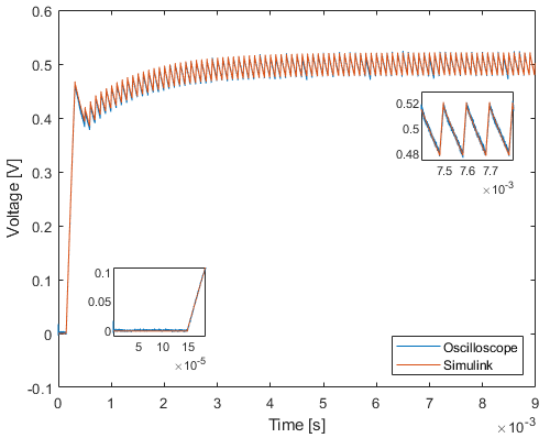

Fig. 7. Capacitor voltage - measurements vs. simulation: $\alpha = 0.4$, OVERSAMPLING=0, UR=2.

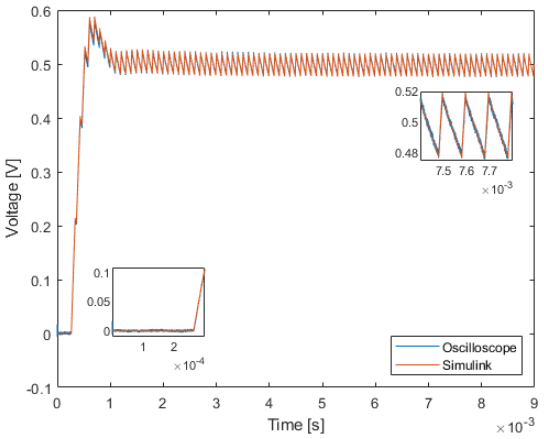

Fig. 8. Capacitor voltage - measurements vs. simulation:$\alpha = 0.4$, OVERSAMPLING=0, UR=1.

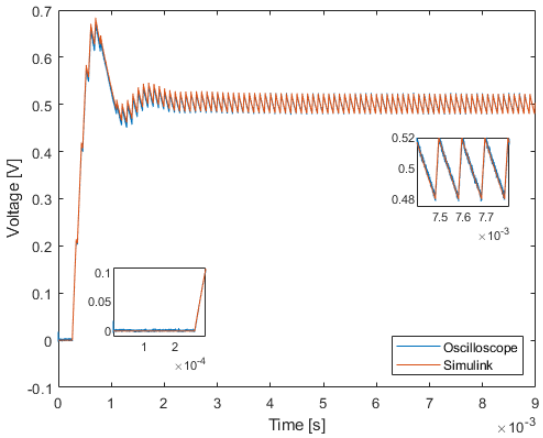

Fig. 9. Capacitor voltage - measurements vs. simulation: $\alpha = 0.4$, OVERSAMPLING=1, UR=1.

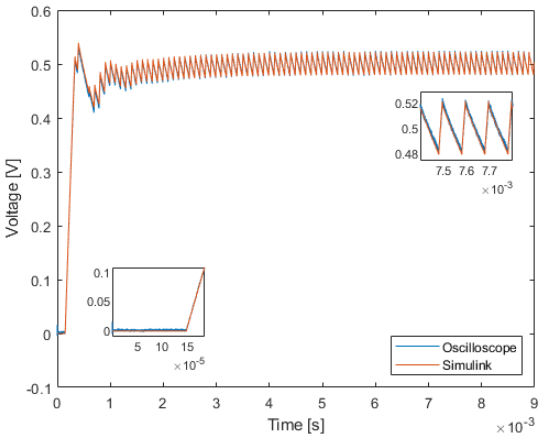

Fig. 10. Capacitor voltage - measurements vs. simulation: $\alpha = 0.4$, OVERSAMPLING=1, UR=2.

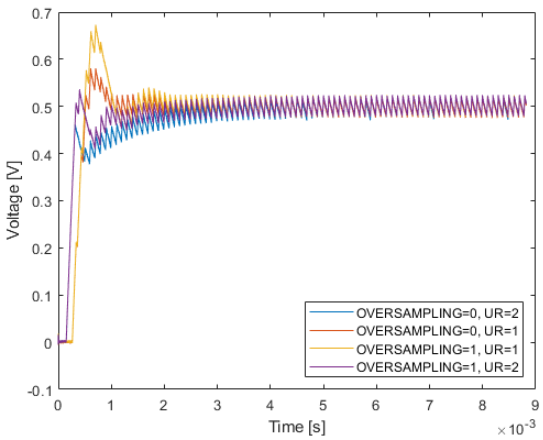

Fig. 11. Capacitor voltage - oscilloscope meas: $\alpha = 0.4$.

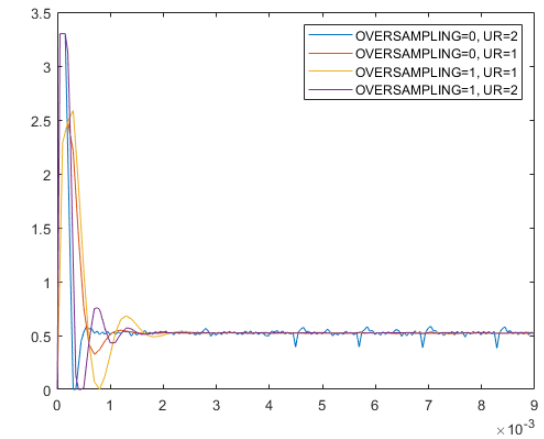

Fig. 12. Control signal - DSP stored data: $\alpha = 0.4$.

3.3 Sampling instances

In order to verify sampling process, a content of the DMA buffer has been stored and exported from DSP's RAM in case of an open loop with the constant duty cycle (equal to 0.5). This is plotted in Fig. 13. An influence of the capacitor's equivalent series resistance (esr) is observable. This effect has been illustrated in Fig. 14, where simulation results have been depicted in cases when esr assumes zero and non-zero value.

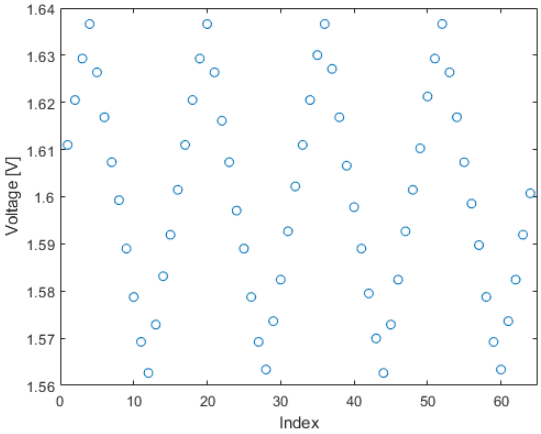

Fig. 13. DMA buffer - DSP stored data.

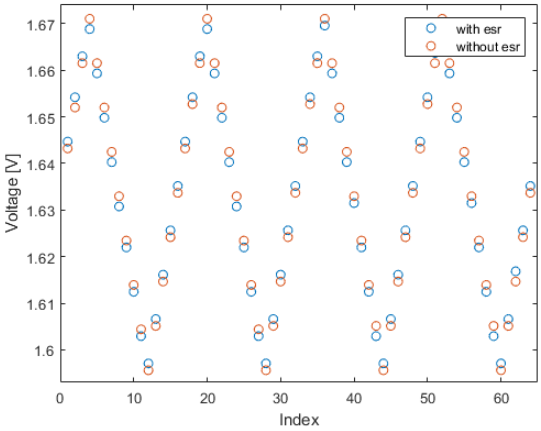

Fig. 14. DMA buffer - simulation results.

4 References

[1] S. Vukosavic, Grid Side Converters - Design and Control, Springer, 2018.