Digital Control in Power Electronics

Regular Sampling & Multisampling Technique on TI f28379D

Experimental Validation on Single Pole System

Ruzica Cvetanovic

August 31, 2020

1 Introduction

This document provides a comparison between simulation and experimental results for regular sampling and multisampling technique implemented on DSP TI F28379. For the purposes of experimental validation a single pole system - series RC connection - directly driven by PWM output has been used. In terms of update rate (UR) and feedback acquisition (with or without oversampling), eight different cases will be discussed:

OVERSAMPLING	UPDATE RATE
0	1
0	2
0	4
0	8
1	1
1	2
1	4
1	8

Table 1. The cases to be analyzed.

2 Controller design

For the purposes of capacitor voltage regulation, a voltage controller based on Internal Model Principle is used. Following the procedure described in [1], we arrive at the voltage controller with the following transfer function:

$$W_{reg}(z) = \frac{\alpha}{1-\beta} \cdot \frac{z-\beta}{z-1} \tag{1}$$

where α is a gain of the discrete-time controller and β is a parameter defined by the load time constant:

$$\beta = e^{\frac{T_s}{R \cdot C}} \tag{2}$$

where T_s is the regulation period. The gain α is set to 0.17.

3 Experimental results

In order to examine validity of the DSP configuration, both oscilloscope measurements and simulation runs have been performed. The goal was to compare simulation and experimental results for all four of the afore mentioned cases. MATLAB Simulink has been used to model voltage regulation in discrete time domain, digital pulse width modulation, RC load in continuous time domain, and feedback acquisition.

Fig. 1-8 show comparison between measured (blue waveform) and simulated (red waveform) capacitor voltage in response to a reference step change (from $0V$ to $0.5V$), for all four of the afore mentioned cases (with

or without oversampling and with single or double update rate). As it is clearly noticeable from the attached figures, simulation and experimental results are almost identical. Slight deviations exist in the damping of the initial peak for the cases with oversampling and higher update rates ($UR = 4$ and $UR = 8$), most likely as a consequence of an insufficient precision in determining capacitor leakage.

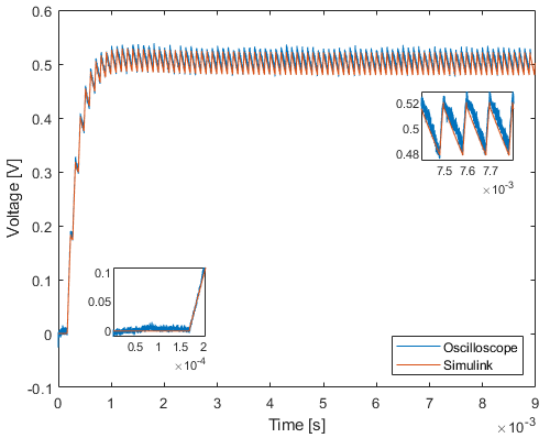

Fig. 1. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=0, UR=2.

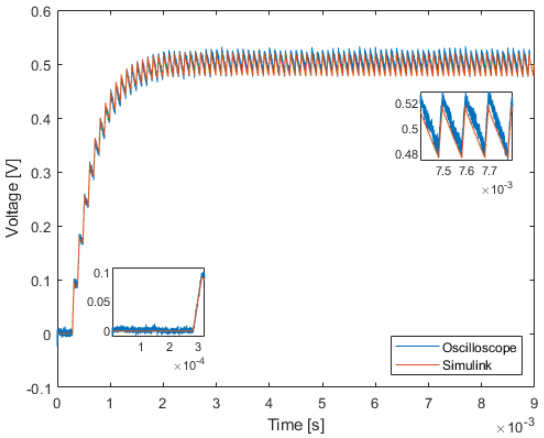

Fig. 2. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=0, UR=1.

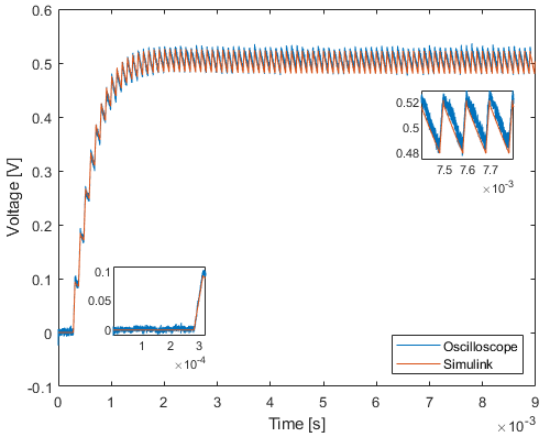

Fig. 3. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=1, UR=1.

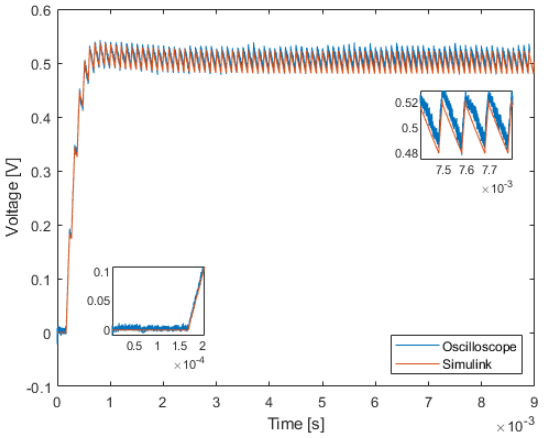

Fig. 4. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=1, UR=2.

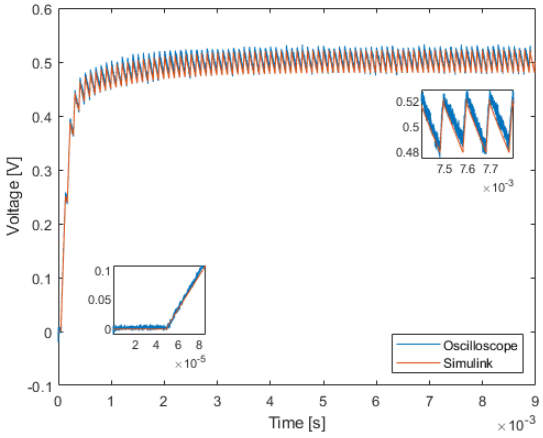

Fig. 5. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=0, UR=4.

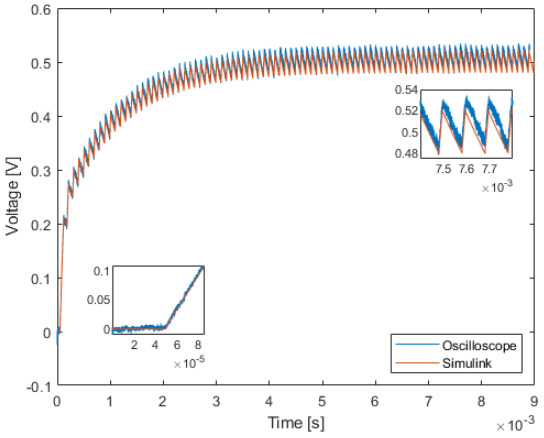

Fig. 6. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=0, UR=8.

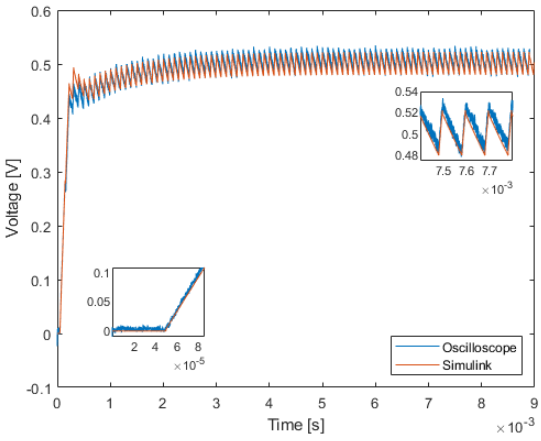

Fig. 7. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=1, UR=4.

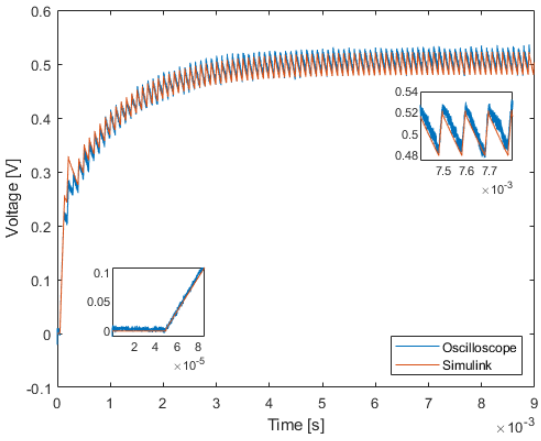

Fig. 8. Capacitor voltage - measurements vs. simulation: OVERSAMPLING=1, UR=8.

4 References

[1] S. Vukosavic, Grid Side Converters - Design and Control, Springer, 2018.