Discrete-Time Current Regulator Design for AC Machine Drives

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***Abstract*—This paper analyzes the behavior of discrete-time current regulators for ac machines operating at high ratios of fundamental-to-sampling frequencies, a situation common for high-speed automotive drives and large-traction drives. At high ratios of fundamental-to-sampling frequencies, highly oscillatory, or unstable, response can occur if the current regulator design does not properly incorporate the effects of the discrete nature of the controller, including delays between the sampling of signals and the application of the voltage commands through pulse-width modulation (PWM). This paper investigates these issues for different design methods and current regulator topologies. As part of this investigation, a simple discrete-time domain ac machine model is developed that includes the delays associated with PWM. This model is then used to design a discrete-time domain version of the complex vector PI current regulator that demonstrates improved response compared with the other regulators studied. Simulation and experimental results are provided to compare the performance, stability, and robustness of the current regulators analyzed.**

***Index Terms*—Complex vector current regulator design, digital delay, discrete-time complex vector current regulator design, ratio of fundamental-to-sampling frequencies.**

I. Introduction

THE SYNCHRONOUS reference frame proportional–integral (PI) current regulator has been the industrial standard for current regulation of ac machine drives for more than 20 years [1]. In a reference frame rotating synchronously with the fundamental excitation, the fundamental excitation signals are transformed into dc signals. As a result, the current regulator forming the innermost loop of the control system is able to regulate ac currents over a wide frequency range with high bandwidth and zero steady-state error [1], [2].

However, the transformation of electric variables to a synchronous reference frame creates cross-coupling between the q- and d-axes that is proportional to the fundamental excitation frequency. As a result, the performance of the current regulator has been shown to degrade as the excitation frequency increases [3]–[5].

Eliminating this dependency on the fundamental excitation frequency has been the subject of significant research for the past two decades. In [3]–[5], the complex vector synchronous frame PI current regulator was introduced, which addresses the cross-coupling as part of the tuning process for achieving pole/zero cancellation, resulting in improved performance and a reduction in the overall parameter sensitivity. A similar solution is proposed in [6] using an internal model control formulation. In [7], cross-coupling decoupling using the complex vector current control approach is generalized with a transfer function matrix.

The design of current regulators in the continuous-time domain, with subsequent discretization of the resulting continuous current regulator, has been widely used and proven adequate for most applications. However, the digital implementation of continuous-time-derived current regulators can show reduced performance when the current regulator is tuned for very high bandwidth or when the drive needs to operate at very high fundamental excitation frequencies relative to the sampling frequency. At high ratios of fundamental-to-sampling frequencies, f_e/f_s, highly oscillatory response, and even instability, can occur if the current regulator design does not properly incorporate the effects of the discrete nature of the controller. In addition, the use of PWM to control the inverter forces additional delays between the sampling of signals and the application of the control response. This further complicates the controller design and decreases the system's overall stability.

The design of current regulators in the discrete-time domain has been addressed by a number of researchers [8], [9]. In those works, delays intrinsic to digital controllers are considered in the regulator design, with superior performance compared to continuous-time-based design methodologies being reported. However, the proposed discrete-time design methods increased the complexity of the controller and the design process, resulting in the loss of design insight and increased computational requirements. In [10], performance degradation of the current regulation loop when the ratio of fundamental-to-sampling frequencies is large was addressed. A complex vector PI controller with predictive active damping terms was developed in order to stabilize the current regulation loop.

This paper analyzes the performance of discrete current regulators as a function of their design space and operating point. Different design methodologies for discrete-time current

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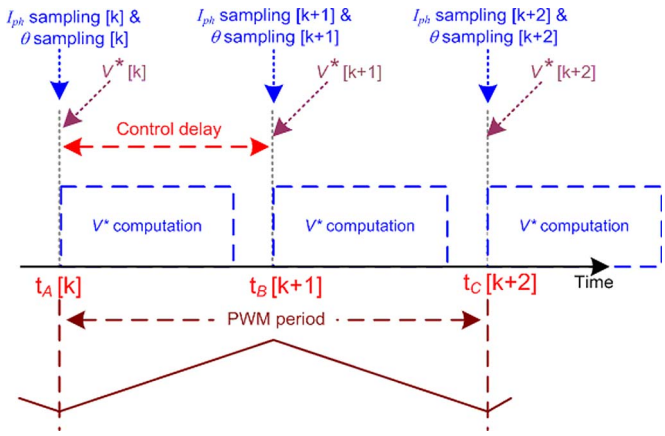

Fig. 1. Control delay in discrete-time ac machine control systems using asymmetric PWM.

regulators are analyzed and compared both in terms of performance, dynamics, and robustness. In addition, a discrete-time domain ac electric machine model is developed that captures the behavior at high ratios of f_e/f_s and the delays associated with PWM. This symmetric machine model is used to design a discrete-time domain version of the complex vector PI current regulator that demonstrates improved response compared to the other controllers studied. The same thought process can also be applied to salient electric machines such as interior permanent magnet synchronous machines. Simulation and experimental results are provided to compare the performance, stability, and robustness of the current regulators analyzed.

II. Discrete Current Regulator Design Approaches

A common practice when designing digital controllers for continuous-time systems is to first develop a continuous-time controller and then convert it to a discrete equivalent using one of the approximations for the continuous s-transform to the discrete z-transform that are available in the control systems literature.

As the sampling frequency decreases, all of the continuous-to-discrete approximations have, in general, degraded behavior compared to the continuous versions. The reasons for this include the intrinsic delay of $T_s/2$ in digital systems, where T_s is the sampling period and the time required to digitize the analog signals and execute the control algorithms. These delays can be made even longer in inverter-fed systems by the requirement that the voltage commands only be updated at certain instances of the PWM cycle (e.g., midpoint of the zero states for space vector PWM or the peak and valleys of the triangle wave for sine-triangle PWM). It is standard practice in inverter-fed system to sample the phase currents and rotor position at the same instant that the voltage commands are updated, or could be updated, if the voltage commands are not updated at every opportunity (e.g., symmetric PWM).

An example of this is shown in Fig. 1, where the $[k]$ sampling occurs at t_A. The voltage command $[k+1]$ is then calculated and applied at the next PWM update opportunity, i.e., t_B, which is equivalent to the controller's output being delayed by one sample period. The response of the system to the application of this voltage command is then obtained at t_C. If the time required to complete the sampling and computation exceed the timing of the PWM update instances, the voltage command update needs to be delayed another complete cycle ($T_{sw}/2$ for asymmetric PWM or T_{sw} for symmetric PWM).

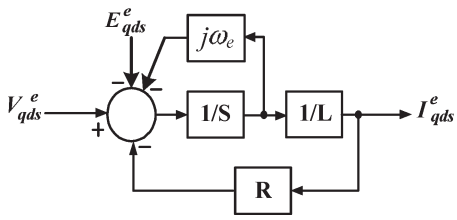

Fig. 2. Continuous-time domain complex vector state block diagram of a symmetric electric machine in a synchronous reference frame.

In addition to the effects intrinsic to digital control systems, current regulators often have an excitation frequency dependence due to the transformation of electrical variables to a synchronous reference frame [2], [4]. The effect of that dependency can be increased again due both to the zero-order hold and the control delay.

An alternative to the discretization of continuous-time controllers is the direct design of discrete controllers. The design of such controllers starts with the derivation of a discrete-time model for the system plant, including the effects of the zero-order hold. A discrete-time model of the electrical subsystem of the ac machine will be developed in Section III, including a one-sample control delay. Once the discrete plant model is obtained, the design and analysis of the controller can follow either a discrete only design methodology or the discrete equivalent of the method used for a continuous-time controller.

III. AC Machine Model

A. Complex Vector AC Machine Model

The state block diagram of a nonsalient permanent magnet synchronous machine using a continuous-time domain complex vector representation is shown in Fig. 2.

Decoupling of the back-emf voltage $\hat{\boldsymbol{E}}^e_{qds}(s)$ allows a symmetric machine (surface permanent magnet synchronous machine or induction machine) to be modeled using a simple resistor/inductor complex vector transfer function (1) [4], [5], [11]. It should be noted that the model shown in Fig. 2 is also valid for induction machines

$$G^s_p(s) = \frac{\mathbf{I}^s_{qds}(s)}{\mathbf{V}^{s*}_{qds}(s)} = \frac{1}{L \cdot s + R} = \frac{1/L}{(s + R/L)} \qquad (1)$$

where complex vector quantities are defined to be of the form $\boldsymbol{f}^s_{qds} = f^s_{qs} - j \cdot f^s_{ds}$ using lower case for time domai, upper case for a transformed variable (s or z), and bold for vectors. Superscripts "s" and "e" denote stationary and synchronous reference frames, respectively.

Accurate modeling of ac machines in the discrete-time domain is essential for the design of a discrete-time current regulator as stated in Section II. The classical transformation of the physical system, (1), to the discrete-time domain can be

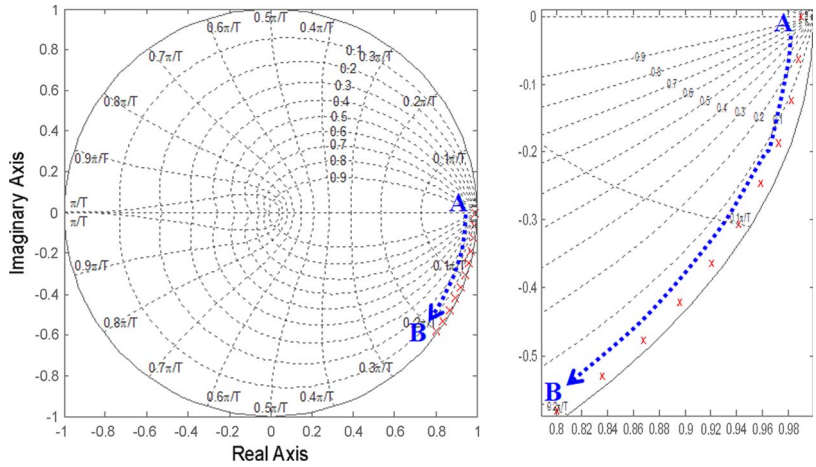

Fig. 3. Synchronous frame complex vector discrete-time pole-zero migration with a frequency increase (0 Hz → 1 kHz, ratio of f_e/f_s : 0 → 0.1) (Conditions: $T_s = 100\ \mu$s, $L = 0.3$ mH, and $R = 15$ mΩ). *Each letter shows the start/end points for each pole and zero migration.

accomplished by modeling the inverter as a unity gain, ideal zero-order hold voltage latch

$$G_p^s(z) = \frac{\boldsymbol{I}_{qds}^s(z)}{\boldsymbol{V}_{qds}^{s*}(z)} = \boldsymbol{Z}\left\{\boldsymbol{L}\{\text{Latch}\}G_p^s(s)\right\} = (1-z^{-1})\boldsymbol{Z}\left\{\frac{G_p^s(s)}{s}\right\} = \frac{\left(1-e^{-(R/L)\cdot T_s}\right)}{R\cdot\left(z-e^{-(R/L)\cdot T_s}\right)}. \quad (2)$$

The resulting difference equation in the stationary frame can be transformed into the difference equation in the synchronous frame, (3), from which the discrete-time domain transfer function in the synchronous frame is obtained (4)

$$\boldsymbol{i}_{qds}^s[k]\cdot e^{-j\cdot\theta_e[k]} = \boldsymbol{i}_{qds}^s[k-1]\cdot e^{-j\cdot\theta_e[k]}\cdot e^{-(R/L)\cdot T_s} + \boldsymbol{v}_{qds}^{s*}[k-1]\cdot e^{-j\cdot\theta_e[k]}\cdot\frac{\left(1-e^{-(R/L)\cdot T_s}\right)}{R} \quad (3)$$

where $\theta_e[k] = \theta_e[k-1] + \omega_e[k-1]\cdot T_s$ and $\boldsymbol{f}_{qds}^s[k-1]\cdot \mathrm{e}^{-j\cdot\theta_e[k]} = \boldsymbol{f}_{qds}^e[k-1]\cdot \mathrm{e}^{-j\cdot\omega_e[k]T_s}$

$$G_p^e(z) = \frac{\boldsymbol{I}_{qds}^e(z)}{\boldsymbol{V}_{qds}^{e*}(z)} = \frac{\left(1-e^{-(R/L)\cdot T_s}\right)}{R\cdot\left(z\cdot e^{j\cdot\omega e[k]\cdot T_s}-e^{-(R/L)\cdot T_s}\right)}. \quad (4)$$

It should be noted that modeling the inverter as a voltage latch neglects the switching harmonics created by the pulse-width-modulation of the power devices. Ignoring the switching harmonics is appropriate in this situation since the ripple current created by these harmonics is eliminated from the feedback signal by the current sampling method and filtering.

B. Fundamental Frequency Dependence

It is evident from (4) that the pole of the physical system is dependent on the fundamental excitation frequency as a result the coordinate transformation. Fig. 3 shows the migration of the synchronous frame physical system discrete-time pole from A to B, as the frequency increases from 0 to 1 kHz. This pole becomes very lightly damped at higher fundamental frequencies, i.e., as it approaches B.

C. Delay Model

The discrete-time model incorporating the one-ample period delay shown in Fig. 1 as the control computation and PWM update delay is shown in (5). The delay in a synchronous reference frame is modeled as $(z\cdot e^{j\cdot\omega^e\cdot T_s})^{-1}$

$$G_{p\_1.0d}^e(z) = \frac{\boldsymbol{I}_{qds}^e(z)}{\boldsymbol{V}_{qds}^{e*}(z)} = \frac{\left(1-e^{-(R/L)\cdot T_s}\right)}{R\cdot z\cdot e^{j\cdot\omega e\cdot T_s}\cdot\left(z\cdot e^{j\cdot\omega e\cdot T_s}-e^{-(R/L)\cdot T_s}\right)}. \quad (5)$$

This model will be used in the following sections to analyze the performance of the different current controllers.

IV. Current Controller Designs

In this section, the different discrete current regulator designs are evaluated. The initial designs will use the commonly chosen Tustin transform to convert the continuous domain controllers to discrete time.

A. Discrete-Time Synchronous Frame PI Current Regulator

Using the Tustin transform to convert the conventional synchronous frame PI current regulator to the discrete domain results in (6), with the closed-loop transfer function being

$$G_c^e(z) = \frac{(K_p + 0.5\cdot K_i\cdot T_s)\cdot z + (0.5\cdot K_i\cdot T_s - K_p)}{(z-1)} = \left[K_p + \frac{K_i\cdot T_s}{z-1}\cdot\frac{z+1}{2}\right] = \left[K_p + \frac{K_i\cdot T_s}{1-z^{-1}}\cdot\frac{1+z^{-1}}{2}\right] \quad (6)$$

$$\frac{\boldsymbol{I}_{qds}^e(z)}{\boldsymbol{I}_{qds}^{e*}(z)} = \frac{G_c^e(z)\cdot G_{p\_1.0d}^e(z)}{1+G_c^e(z)\cdot G_{p\_1.0d}^e(z)}. \quad (7)$$

The control gains for this controller are typically chosen to achieve pole/zero cancellation at zero rotor speed and the desired bandwidth [2]–[4] pole-zero cancellation for the continuous domain would be obtained by setting the controller

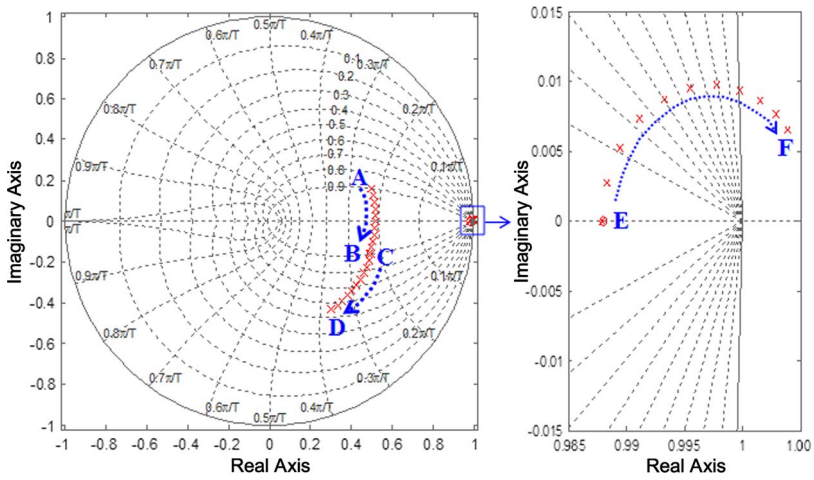

Fig. 4. Synchronous frame complex vector eigenvalue migration with a frequency increase (0 Hz $\rightarrow$ 1 kHz, ratio of $f_e/f_s : 0 \rightarrow 0.1$) for a discrete-time synchronous frame PI current regulator without delay compensation (conditions: $T_s = 100\ \mu$s, $L = 0.3$ mH, $R = 15\ \text{m}\Omega$, and $BW = 1$ kHz.).

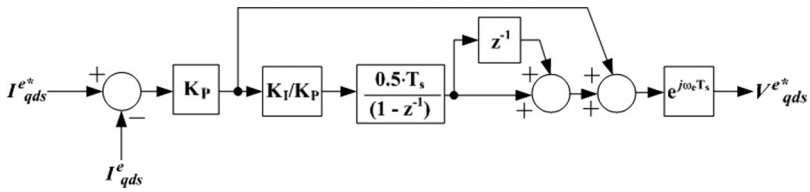

Fig. 5. Complex vector block diagram of the discrete-time synchronous frame PI current regulator including fundamental frequency phase advance.

gains to the following values: $K_i = \hat{R} \cdot \omega_{bw}$ and $K_p = \hat{L} \cdot \omega_{bw}$, where ω_{bw} is the desired closed-loop bandwidth.

To determine the sensitivity of this controller to changes in the fundamental frequency, the migration of its poles/zeros (eigenvalue migration) with varying frequency was calculated (see Fig. 4). Although all of the closed-loop poles migrate as the frequency increases, of particular interest is the closed-loop pole migrating from point E to F, as it approaches and eventually goes out of the unit circle for f_e/f_s ratios > 0.07, resulting in an unstable system.

B. Discrete-Time Synchronous Frame PI Current Regulator With Delay Compensation

The delay created by the PWM generation, Section III-C, needs to be accounted for in order to achieve high-performance current regulation, especially in high-speed operation. The cause of the delay can be understood by recognizing that the desired fundamental excitation changes position during the course of a sample period. If the controller output (voltage command) is not updated to reflect this change, it will appear as a disturbance to the current regulator. As shown in (8) and Fig. 5, the current regulator can compensate for this delay by phase advancing the voltage command (multiplying by $e^{j \cdot \omega^e \cdot T_s}$). The resulting closed-loop transfer function can be calculated using (7)

$$G_c^e(z) = \frac{(K_p + 0.5 \cdot K_i \cdot T_s) \cdot z + (0.5 \cdot K_i \cdot T_s - K_p)}{(z-1)} \cdot e^{j \cdot \omega_e T_s}. \tag{8}$$

Fig. 6 shows the eigenvalue migration with varying fundamental frequency for the discrete-time synchronous frame PI current regulator with delay compensation. All the closed-loop poles migrate as the synchronous frequency increases. In particular, a closed-loop pole migrating from E to F approaches the unit circle, which increases oscillatory dynamics in its response. With delay compensation, however, the system remains stable for the range of fundamental frequencies studied. The addition of delay compensation is responsible for this improvement and will be included in all the remaining current regulators analyzed in this paper.

C. Discrete-Time State Feedback Decoupling Current Regulator

State feedback decoupling has been widely used as a method to compensate the frequency dependence of ac machine drives. In the continuous-time domain, state-feedback decoupling is realized by using an estimated inductance, measured currents, and the instantaneous fundamental frequency to counteract the cross-coupling created by the reference frame transformation. The state-feedback decoupling current regulator can be viewed as using the same control equation as the synchronous frame PI regulator (8), with a modified plant model to reflect the physical system decoupling provided by the controller (9), shown at the bottom of the next page. The resulting closed-loop transfer function can then be calculated using (7).

Fig. 7 shows the eigenvalue migration of the discrete equivalent state-feedback decoupling current regulator with delay compensation. For this investigation, $\hat{L}$ was set to the same value as the physical inductance value. All three closed-loop poles migrate as the frequency increases and all closed-loop poles are lightly damped. As a result, the system behavior of

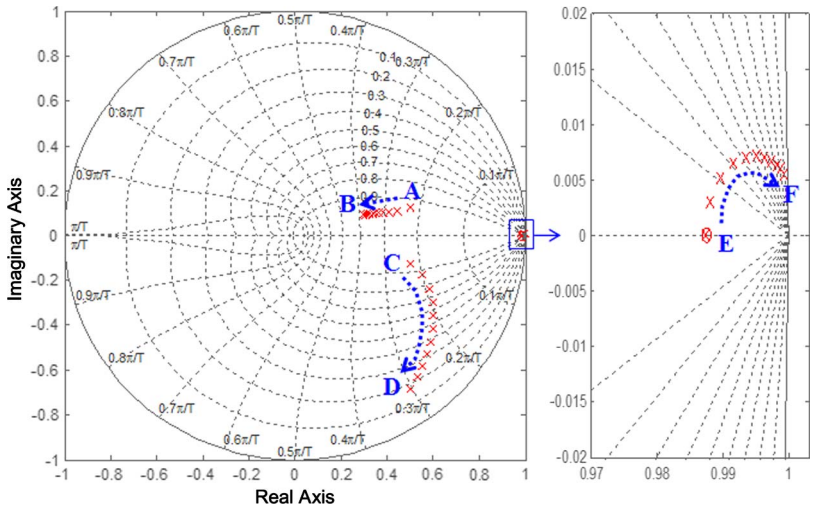

Fig. 6. Synchronous frame complex vector eigenvalue migration with a frequency increase (0 Hz → 1 kHz, ratio of $f_e/f_s : 0 \rightarrow 0.1$) for the discrete-time synchronous frame PI current regulator with delay compensation (conditions: $T_s = 100\ \mu$s, $L = 0.3$ mH, $R = 15$ mΩ, and $BW = 1$ kHz.).

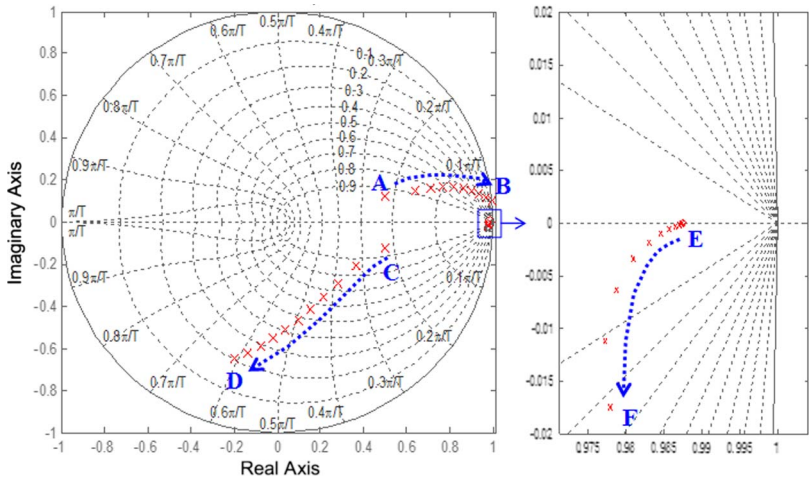

Fig. 7. Synchronous frame complex vector eigenvalue migration with a frequency increase (0 Hz → 1 kHz, ratio of $f_e/f_s : 0 \rightarrow 0.1$) for the discrete-time state feedback decoupling current regulator with delay compensation (conditions: $T_s = 100\ \mu$s, $L = 0.3$ mH, $R = 15$ mΩ, $\hat{L} = L$, and $BW = 1$ kHz.).

the control system is highly oscillatory when operating at high synchronous frequencies.

D. Discrete-Time Complex Vector Synchronous Frame PI Current Regulator Using Tustin Transform

Using the Tustin transform, the discrete equivalent of the complex vector synchronous frame PI current regulator is shown in (10) and Fig. 8, with the closed-loop transfer function calculated using (7)

$$G^e_{c\_cv}(z) = \frac{1}{z-1} \cdot [(K_p + 0.5 \cdot K_i \cdot T_s + j \cdot 0.5 \cdot \omega_e \cdot K_p \cdot T_s) \cdot z - (K_p - 0.5 \cdot K_i \cdot T_s - j \cdot 0.5 \cdot \omega_e \cdot K_p \cdot T_s)] \cdot e^{j \cdot \omega_e T_s}. \quad (10)$$

The eigenvalue migration with varying fundamental frequency is shown in Fig. 9. Good pole-zero cancellation is achieved for the frequency-dependent, closed-loop pole migrating from A to B, with some small deviations at higher fundamental frequencies.

E. Discrete-Time Complex Vector Synchronous Frame PI Current Regulator Without Using the Tustin Transform

It is also possible to design the current regulator in the discrete-time domain using classical direct digital design methods, therefore avoiding the use of the Tustin transform. The design philosophy used for the complex vector PI current regulator in [3]–[5] extended the classical PI approach to select

$$G^e_{p\_d}(z) = \frac{\left(1 - e^{-(R/L)\cdot T_s}\right)}{R \cdot e^{j\cdot\omega_e\cdot T_s} \cdot z \left(e^{j\cdot\omega_e\cdot T_s} \cdot z + e^{-(R/L)\cdot T_s}\right) + \left(1 - e^{-(R/L)\cdot T_s}\right) \cdot j\cdot\omega_e\cdot\hat{L}} \quad (9)$$

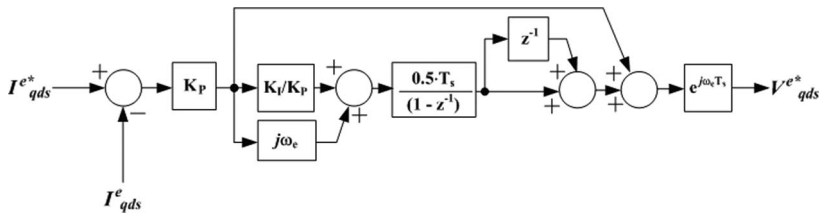

Fig. 8. Complex vector block diagram of a discrete-time complex vector synchronous frame PI current regulator based on the Tustin transform.

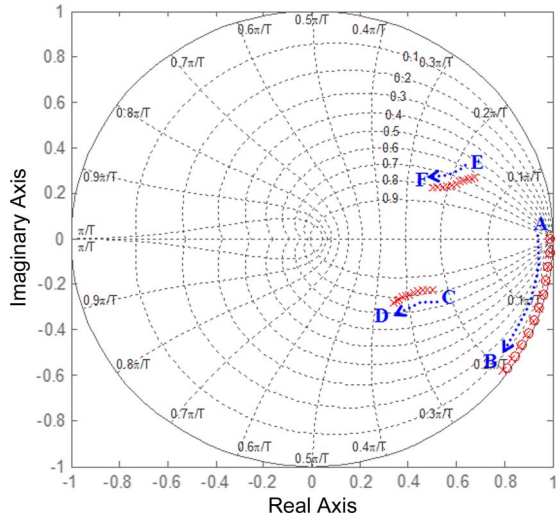

Fig. 9. Synchronous frame complex vector eigenvalue migration with frequency increase (0 Hz $\rightarrow$ 1 kHz, ratio of f_e/f_s : 0 $\rightarrow$ 0.1) for the discrete-time complex vector synchronous frame PI current regulator based on the Tustin transform (conditions: $T_s = 100$ μs, $BW = 1$ kHz, $L = 0.3$ mH, and $R = 15$ mΩ.).

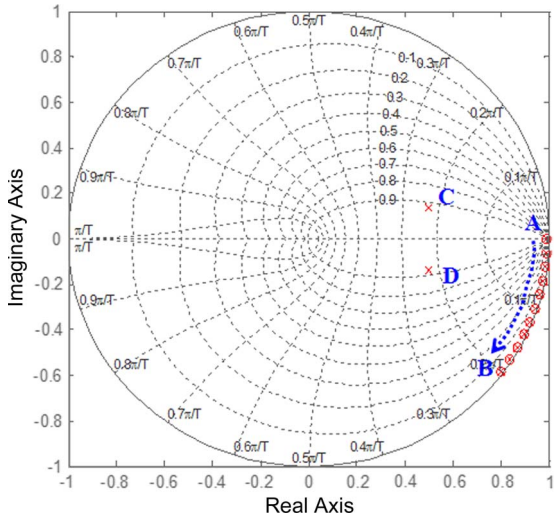

Fig. 11. Synchronous frame complex vector eigenvalue migration with frequency increase (0 Hz $\rightarrow$ 1 kHz, ratio of f_e/f_s : 0 $\rightarrow$ 0.1) for the discrete-time complex vector synchronous frame PI current regulator designed directly and not based on the Tustin transform (conditions: $T_s = 100$ μs, $BW = 1$ kHz, $\hat{R} = R$, and $\hat{L} = L$.).

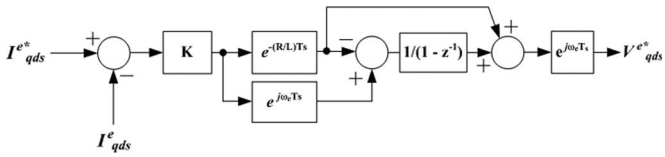

Fig. 10. Complex vector block diagram of a discrete-time complex vector synchronous frame PI current regulator not based on the Tustin transform.

a controller zero that would cancel both the real and the synchronous frequency-dependent component of the complex vector synchronous frame model. This can also be applied here directly without the need for the Tustin transform. The resulting controller is shown in (11) and Fig. 10. The closed-loop system, (12), derived using (7), demonstrates the desired fundamental (excitation) frequency-independent response observed in the continuous implementation

$$G^e_{c\_dcv}(z) = \frac{K \cdot \left(e^{j\cdot\omega_e\cdot T_s} - z - 1 \cdot e^{-\hat{R}/\hat{L}\cdot T_s}\right)}{(1 - z^{-1})} \cdot e^{j\cdot\omega_e T_s} \quad (11)$$

$$\frac{\boldsymbol{I}^e_{qds}(z)}{\boldsymbol{I}^{e*}_{qds}(z)} = \frac{K \cdot (1 - e^{-R/L\cdot T_s})}{R \cdot z^2 - R \cdot z + K \cdot (1 - e^{-R/L\cdot T_s})}. \quad (12)$$

The performance characteristics of this direct design form the discrete-time complex vector synchronous frame PI current regulator was analytically investigated using eigenvalue migration as shown in Fig. 11. Excellent pole-zero cancellation for the pole migrating from A to B is achieved, allowing the control performance to be decoupled from the speed.

Fig. 12 shows the eigenvalue migration with varying frequency for errors in the resistance and inductance estimates, $\hat{R} = 0.7 \times R$ and $\hat{L} = 1.3 \times L$. For the pole migrating from A to B, good pole-zero cancellation is still achieved, allowing the control performance to be decoupled from the speed. As a result, the proposed direct design form of the discrete-time complex vector current regulator design can be seen as relatively insensitive to parameters.

A similar form of this controller was derived in [8] using a more complex formulation and different assumptions for the PWM method and sampling/control updates. The behavior of these two controllers is expected to be very similar/identical, so further analysis of the controller presented in [8] is not included in this paper.

Classical, direct design PI control methods, i.e., not using the Tustin transform, can also be applied to the standard synchronous frame PI current regulator, which does not decouple the synchronous frequency-dependent cross-coupling. The control law for this controller is shown in

$$G^e_{c\_dcv}(z) = \frac{K \cdot (1 - z^{-1} \cdot e^{-\hat{R}/\hat{L}\cdot T_s})}{(1 - z^{-1})} \cdot e^{j\cdot\omega_e T_s}. \quad (13)$$

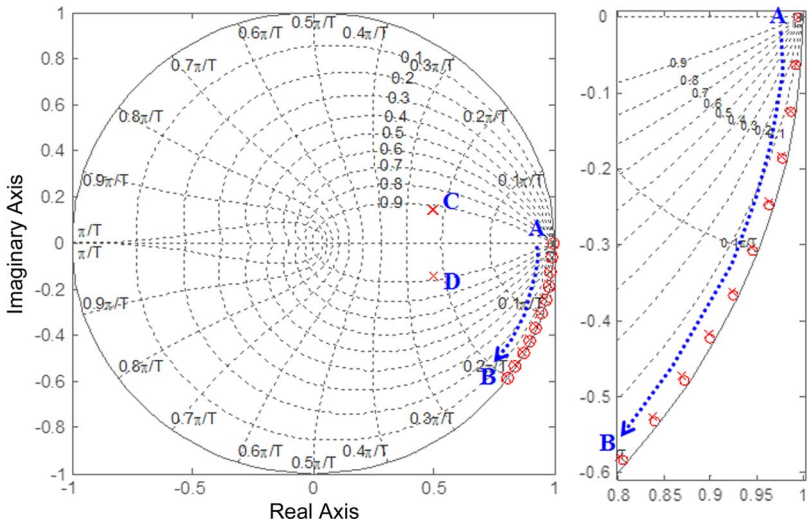

Fig. 12. Synchronous frame complex vector eigenvalue migration with parameter variations and frequency increase (0 Hz → 1 kHz, ratio of f_e/f_s : 0 → 0.1) for the discrete-time complex vector synchronous frame PI current regulator design designed directly and not based on the Tustin transform (conditions: $T_s = 100$ μs, $BW = 1$ kHz, $\hat{R} = 0.7 \times R$, and $\hat{L} = 1.3 \times L$.).

Its eigenvalue migration is not included in this paper but its performance is included as part of the analysis presented in the following section.

V. Current Regulator Performance

Two of the main concerns when designing current regulators for ac drives are the dynamics and the robustness of the closed-loop system as a function of its design space and operating point. This section investigates the effect of the fundamental excitation frequency (ratio of fundamental, f_e, to sampling, f_s, or Nyquist, $f_s/2$, frequencies) and regulator tuning (ratio of closed-loop pole location to sampling or Nyquist frequency) on both characteristics.

The assessment of a controller's dynamics and robustness can be done through a variety of methods. The analysis presented in this paper will focus on two metrics: bandwidth and vector margin. Bandwidth is the range of frequencies over which sinusoidal command signals are correctly tracked. It is one of the most classical parameters for characterizing the dynamic response of closed-loop systems. The vector margin combines the attributes of the commonly used gain and phase margins in a single value that assesses the overall stability of a system.

A. Command Tracking Bandwidth

Several definitions of the bandwidth can be found in the literature, with the most broadly used being when the amplitude of the tracked signal is attenuated no more than 3 dB with respect to dc gain. That definition is also valid as a measure of the noise sensitivity of the system. If the phase of the signal is the main concern, the bandwidth can be defined as the frequency at which the output lags the command by 45°. Both definitions agree for a first-order system, and are equal to the system pole location.

When a current regulator is tuned to have a particular bandwidth using the pole-zero cancellation tuning procedure, it attempts to fix the pole position as that of a first-order system (since the plant after back-emf decoupling is first-order). Any pole-zero mismatch due to the fundamental frequency changes, parameter errors, or control delays create a difference between the desired bandwidth (pole position) and the actual bandwidth obtained using either the -3 dB or $-45°$ definitions. The following will use the $-45°$ definition since it better defines the reference tracking performance both in magnitude and in phase. Similar conclusions would be expected with the -3 dB or other definitions.

The closeness of the actual bandwidth to the desired bandwidth (pole location) of the current regulators analyzed in Section VI has been calculated for different fundamental excitation frequencies and pole locations, both normalized to the Nyquist frequency. The results can be seen in Fig. 13. Values under zero mean an unstable response for that excitation frequency and pole location combination.

Taking the discrete-time synchronous frame PI current regulator using the Tustin transform as a baseline for comparison [Fig. 13(a)], it can be seen that adding delay compensation [Fig. 13(b)] has no meaningful effect on the system bandwidth.

A significant improvement can be obtained by using state feedback decoupling, as shown in Fig. 13(c). The bandwidth of the system has improved in the high-excitation frequency regions where the discrete-time synchronous frame PI current regulator had null or very limited bandwidth.

The discrete-time complex vector synchronous frame PI current regulator using the Tustin transform exhibits further improvement in the bandwidth, as shown in Fig. 13(d).

The classical, direct design discrete-time synchronous frame PI current regulator not based on the Tustin transform [Fig. 13(e)] exhibits improvements in bandwidth compared to its Tustin transform-based versions [Fig. 13(a) and (b)]. This demonstrates the advantage of direct digital controller design.

The direct design discrete-time complex vector synchronous frame PI current regulator not based on the Tustin transform [Fig. 13(f)] exhibits an increased bandwidth for almost all

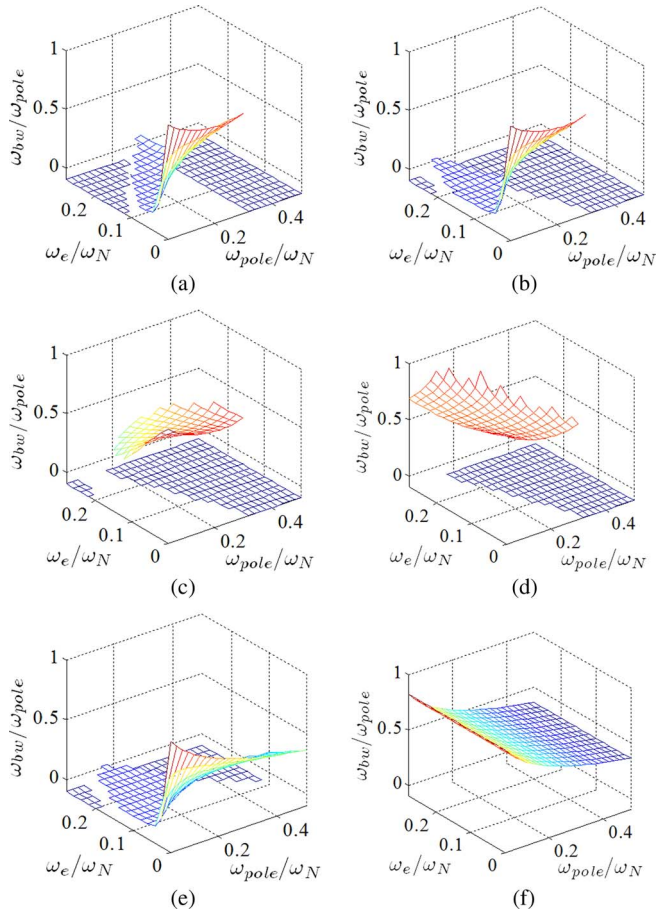

Fig. 13. Bandwidth as a function of the fundamental frequency to Nyquist frequency ratio, and pole location to Nyquist frequency ratio. Unstable regions are represented as -0.1 value. Ideal parameters are used. (a) Discrete-time synchronous frame PI current regulator using the Tustin transform without delay compensation. (b) Discrete-time synchronous frame PI current regulator using the Tustin transform with delay compensation. (c) Discrete-time state-feedback decoupling current regulator using the Tustin transform. (d) Discrete-time complex vector synchronous frame PI current regulator using the Tustin transform. (e) Discrete-time synchronous frame PI current regulator not using the Tustin transform and not decoupling the synchronous frequency cross-coupling. (f) Discrete-time complex vector synchronous frame PI current regulator not using the Tustin transform.

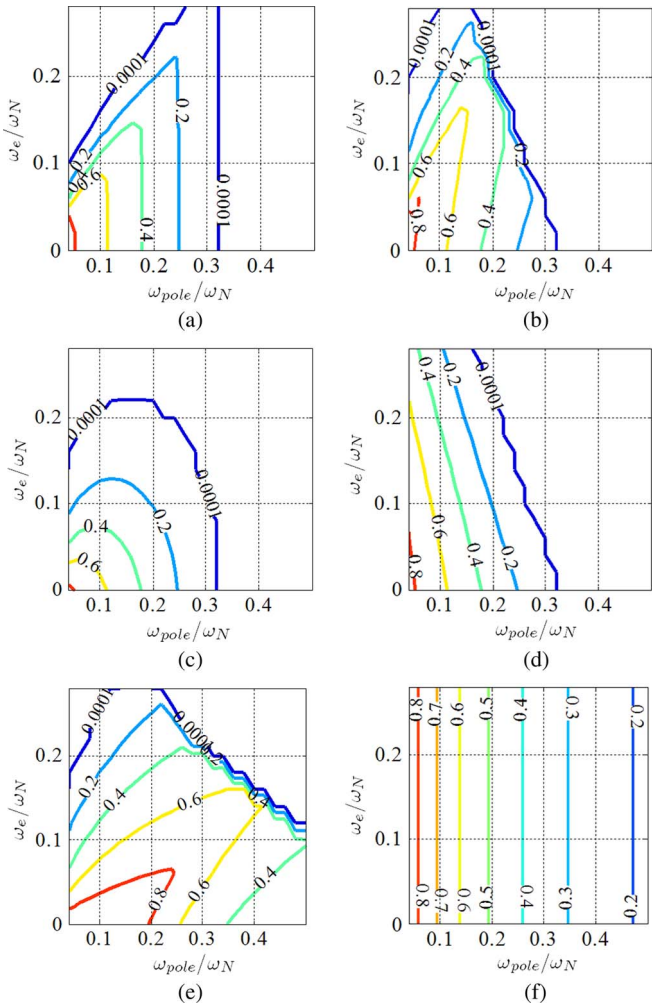

Fig. 14. Vector margin as a function of the fundamental frequency to Nyquist frequency ratio and pole location to Nyquist frequency ratio. (a) Discrete-time synchronous frame PI current regulator using the Tustin transform without delay compensation. (b) Discrete-time synchronous frame PI current regulator using the Tustin transform with delay compensation. (c) Discrete-time state-feedback decoupling current regulator using the Tustin transform. (d) Discrete-time complex vector synchronous frame PI current regulator using the Tustin transform. (e) Discrete-time synchronous frame PI current regulator not using the Tustin transform and not decoupling the synchronous frequency cross-coupling. (f) Discrete-time complex vector synchronous frame PI current regulator not using the Tustin transform.

design and operating points compared to the other designs. This can be seen by the fact that it maintains a relatively constant bandwidth as a function of the fundamental excitation frequency and that it significantly expands the range in which the pole can be located with respect to the Nyquist frequency.

It should finally be noted that the graphs in Fig. 13 do not show the actual bandwidth but instead show the closeness of the actual bandwidth to the tuning of the pole location. The actual bandwidth for all controllers analyzed increases with increasing pole location.

B. Vector Margin

The robustness or relative stability of the closed-loop system can be analyzed through the sensitivity function

$$S(z) = \frac{1}{1 + G_c^e(z) \cdot G_{p\_1.0d}^e(z)}. \tag{14}$$

TABLE I
CONDITIONS OF SIMULATION AND EXPERIMENT

Motor	Pole pairs	R_S [$m\Omega$]	L_q [mH]	L_d [mH]
IPMSM	8	16	0.45	0.22
λ_{pm} [Wb]	f_e [Hz]	f_{pwm} [kHz]	f_{sample} [kHz]	BW [kHz]
0.066	826.7	5	10	1

The frequency response function (FRF) of the sensitivity function provides information about the sensitivity of the closed-loop system to changes in the open-loop controlled system at any frequency. The defining value of the sensitivity function is its peak value since this quantity is the inverse of the vector margin, which is defined as the distance from the closest point of a Nyquist plot to the $-1 + j \cdot 0$ point. Therefore, the vector margin is a single value that defines the system's relative stability and will be used to compare the controllers studied.

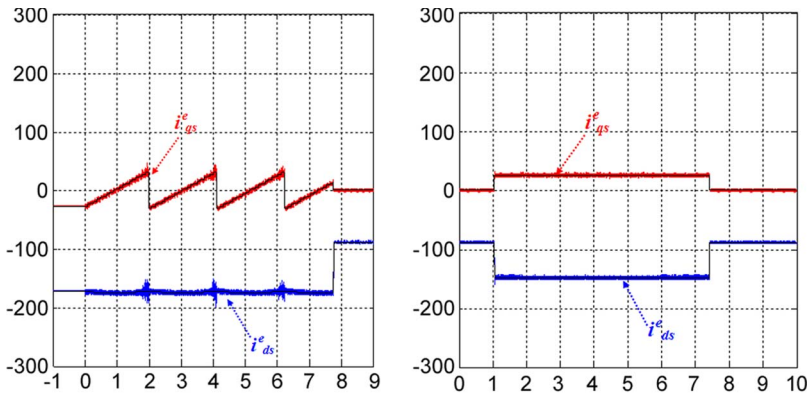

Fig. 15. Experimental sawtooth and step responses for the direct design, discrete-time complex vector current regulator at constant speed (Conditions: $\omega_{rm} =$ 6200 RPM and $V_{\rm dc} = 220$ V). (a) Current command sweep. (b) Step of current command.

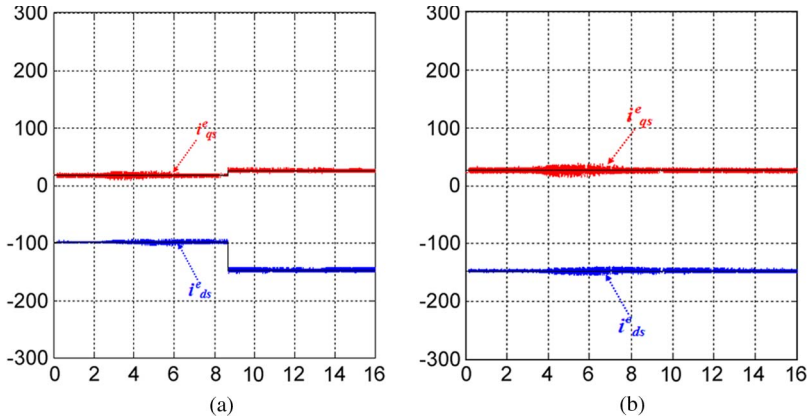

Fig. 16. Experimental step response and null response for the direct design discrete-time complex vector current regulator during a speed sweep (Conditions: $\omega_{rm} = 512$ RPM to 6200 RPM and $V_{\rm dc} = 220$ V). (a) Step of current command. (b) Constant current command.

The vector margin provides a numerical value between 0 and 1, with 0 being an unstable system. Engineers familiar with the classic stability margin metrics, gain and phase margin, can estimate them by means of

$$GM^* = \frac{1}{1+VM} \tag{15}$$

$$PM^* = 2\arcsin\frac{VM}{2}. \tag{16}$$

The vector margins for the six current regulators, the different fundamental excitation frequencies and pole locations, and normalized to the Nyquist frequency can be seen in Fig. 14. These plots are based on ideal parameters.

The vector margin for the discrete-time synchronous frame PI current regulator using the Tustin transform is seen in Fig. 14(a). It should be noted that vector margins under 0.5 would normally mean highly oscillatory response.

It can be concluded from Fig. 14(a) that the application range of this regulator is limited.

The delay compensation was seen not to introduce a significant improvement in the bandwidth [Fig. 13(b)], but Fig. 14(b) shows that it significantly increases the system stability.

The bandwidth improvement of the discrete-time state-feedback decoupling current regulator [Fig. 13(c)] is due to the positive feedback introduced to decouple the cross-coupling term in the open-loop system. This decreases the relative stability of the system, as shown in Fig. 14(c). It should be noted that for single-loop systems, the vector margin is also a measure of the closed-loop system damping, meaning a low-vector margin corresponds to a poorly damped system. Whereas in cascaded control systems such as this one, this direct relation with the closed-loop system damping is lost.

Therefore, vector margin values under 0.5 do not necessarily correspond to a highly oscillatory system.

The discrete-time complex vector synchronous frame PI current regulator using the Tustin transform, as seen in Fig. 14(d), shows increased stability for the system at high ratios of excitation frequency to Nyquist frequency, as expected.

The two direct design discrete-time current regulators not based on the Tustin transform [Fig. 14(e) and (f)] both show significant improvements in the range of stable operation, with the discrete-time complex vector synchronous frame PI current regulator exhibiting the best overall characteristics, especially for high fundamental excitation frequencies.

VI. Experimental Results

The performance of the direct design, discrete-time complex vector synchronous frame PI current regulator was evaluated experimentally using an interior permanent magnet (IPM)

synchronous machine drive. The parameters for the test machine are shown in Table I.

Fig. 15 shows the high-speed performance of this regulator for a sawtooth and step-current commands at a constant speed of 6 200 RPM, which is equivalent to a fundamental frequency of 826.7 Hz and a f_e/f_s of 0.083.

Fig. 16(a) and (b) illustrate step and null responses of the regulator for speed sweeps from 512 to 6 200 RPM.

For the step and sawtooth current commands and during a speed sweep, the direct design discrete-time complex vector current regulator shows excellent regulation and stability.

VII. Conclusion

This paper has investigated the design of digital current regulators operating at high fundamental-to-sampling frequencies. Digital current regulators designed using Tustin transforms show significant degradation as the fundamental frequency increases when compared to direct design methods in the discrete time.

The design of discrete-time current regulators requires accurate discrete models of the machine and inverter. This paper included models that captured the effect of high fundamental-to-sampling frequencies and inherent PWM delays. These models were used to design and evaluate several discrete-time ac machine current regulators.

Metrics for the assessment of performance and stability were introduced and used to evaluate the regulators.

Simulation and experimental results confirmed that the direct design complex vector regulator was the best of those evaluated.

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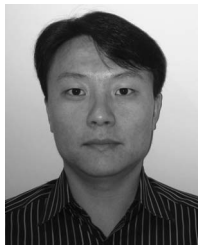

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