Analysis and DSP Implementation of Multisampled Three-Phase Current Controllers

***Abstract*—nothing yet**

***Index Terms*—nothing yet**

I. Introduction

FIELD oriented control (FOC) in electrical drives and voltage oriented control (VOC) in grid-connected converters is a well-established strategy for the control of high performance three-phase electrical systems [1]. An essential part of this concept is the inner current control loop, which regulates the synchronous rotating frame (SRF) currents [2]. A prerequisite for the proper operation of the outer control loops is a precise and rapid current controller [3], [4]. The SRF controller must provide a decoupling function between d and q axis currents []. This is particularly challenging for high-speed or high pole-pair electrical drives, which require robustness at very high output frequencies [4]–[6].

Due to simplicity and added flexibility, current controllers are nowadays mostly realized in digital form [Buso Matta]. The demerit of digital control systems is the introduction of delays due to the analog-to-digital conversion (ADC), algorithm execution time, and digital pulse width modulation (DPWM) [Buso Matta]. These delays limit the achievable bandwidths and impair the decoupling function of SRF current controllers. In most state-of-the-art applications, double-sampled double-update (DS-DU-PWM) control strategy is used, where the inductor currents are sampled twice per PWM period, with acquisition instants being synchronized so that average current values are obtained []. In industrial applications, feedback signal is often strongly corrupted by various noise sources, which requires additional filtering []. This is well-achieved by oversampling the signal and then averaging it over the PWM period. In this way, true-average is obtained with additional high noise suppression. The filtered signal is then decimated so that the control action is executed with double-update rate. This kind of strategy, implemented in [7], is labeled as multi-sampled double-update (MS-DU-PWM) control. The MS-DU-PWM strategy results in a high quality feedback signal, but with a highly negative impact on the system dynamics. Achieving high bandwidths, with the additional delay due to the averaging, requires modification of the controller structure to compensate the phase lag[].

The delay-related limitations have inspired investigating multisampled PWM control, with purpose of enabling analog-like control bandwidths in digital systems. The multisampled multi-update (MS-MU-PWM) approach relies on acquiring the control variables and updating the modulating waveform multiple times per switching period [8]. The concept of MS-MU-PWM digital control offers significant reduction of digital delays and is therefore a promising solution for breaking the bandwidth limitations [9] [MS in electric drives]. Besides small-signal improvement, MS-MU-PWM also provides a nonlinear advantage as the modulating waveform can be updated multiple times per switching period. This yields a lower response delay to large-signal perturbations [active filtering]. On the other hand, MS-MU-PWM introduces a set of nonlinearities due to sampling of the switching ripple, which is why some digital filtering should always be implemented [10], [11]. The impact of nonlinearities is strongly reduced by completely filtering the switching ripple, for example using moving average filters (MAFs).

Regarding controller structures, SRF PI controllers are the most frequently encountered current control strategies for three-phase RL loads due to their simplicity and satisfactory performance for the majority of the industry requirements [3], [12], [13]. With a proper parameter setting procedure, high bandwidths can be achieved [2], [3]. Nevertheless, their transient decoupling capability is rather limited, especially at high output frequencies [14]. Achieving robust operation with high bandwidths has driven the design of high-performance current controllers directly in discrete-time domain [13] [lorenz...]. The dead-beat current controllers offer very fast transient response but at the cost of considerable performance degradation in the presence of measurement errors and parameter mismatch, which is often the case in control of electric drives [15]–[17]. More robust operation is achieved with the use of the discrete internal model controller (IMC) design [18]. This strategy has proven to offer high closed loop bandwidths at very high output frequencies [7], [19], [20].

This paper analyzes the use of the discrete IMC based current controller with MS-MU-PWM, suitable for implementation on standard DSP platforms. The main goal of the paper is to analyze the performance of MS-MU-PWM in standard industrial applications, and to compare it with standardly used DS-DU-PWM and MS-DU-PWM methods. The target is to show that the MS-MU-PWM control with feedback averaging can offer high quality feedback signal as in MS-DU-PWM, while also providing improved dynamic performance compared to DS-DU-PWM. This gives potential of implementing MS-MU-PWM with feedback averaging as standard industrial procedure for current control.

II. Multi-rate control system

The multi-rate control system of a three-phase RL load in dq frame is shown in Fig. 1. The system can be separated into digital and continuous-time domain. An ADC is used to transform feedback signal from analog to digital domain. This action is performed with a sampling frequency $f_s = N_s f_{pwm}$, where N_s is the multisampling (oversampling) factor and

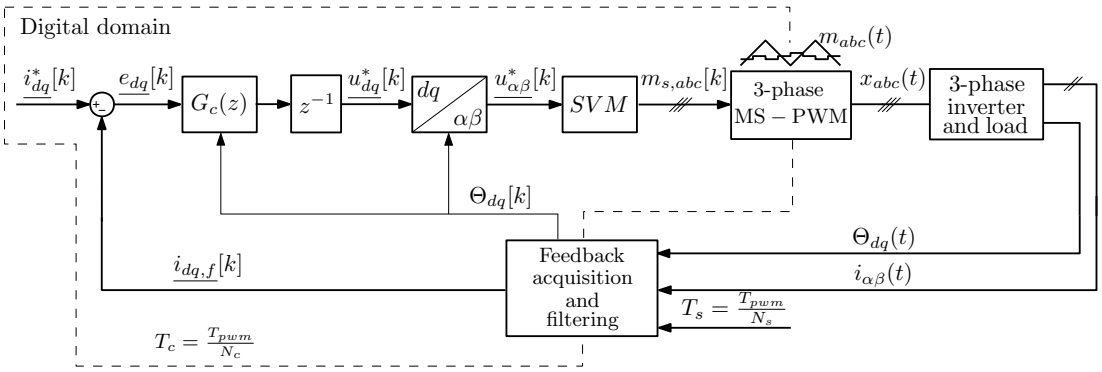

Fig. 1: Multisampled control loop of a three-phase inverter.

f_{pwm} is the switching frequency of the inverter. The digital domain operates with frequency $f_c = N_c f_{pwm}$, where N_c is the multi-update factor that determines the update rate of the controller output. The choice of this frequency is independent of the sampling frequency, as the feedback signal can be oversampled with frequency f_s and then filtered and decimated to control frequency f_c. The digital domain is comprised of feedback filter $G_{fb}(z)$, controller $G_c(z)$, coordinate frame transformation block, and space vector modulation (SVM) block. The controller $G_c(z)$ outputs reference voltage in dq frame, $\underline{u_{dq}}^*[k]$, which is then transformed to $\alpha\beta$ frame. This reference voltage is used to obtain digital modulating waveform for each inverter phase, $m_{s,abc}[k]$. Conversion from digital to analog domain is performed by MS-PWM. Its inherent zero-order hold function transforms the digital impulse train $m_{s,abc}[k]$ into the continuous-time modulating waveform $m_{abc}(t)$. MS-PWM with the triangular carrier is used due to its favorable characteristics in MS-MU-PWM control []. The PWM output is used as a gate signal $x_{abc}(t)$. The three-phase inverter is used to supply a generic RL load, which can model either an AC electrical machine or the electrical grid. The sensed feedback includes line currents $i_{\alpha\beta}(t)$ and the angle of the dq coordinate frame Θ_{dq}.

A. Motivation behind MS-MU-PWM control

Modern processors feature high computational power, which enables short execution times for control routines. However, switching frequencies of power converters are hardware limited, and do not go over several tens of kHz for medium power applications. This hardware based limitation directly affects the realizable bandwidths of the current control loop, which subsequently limits the outer control loops. Therefore, pushing for highest possible bandwidths relative to the switching frequency is often a design criterion. One way of achieving that is the implementation of MS-MU-PWM [].

Using describing function approach, small-signal model of the multisampled PWM with triangular carrier is found to be almost equal to a pure delay of $\frac{T_c}{2}$, where T_c is the modulating waveform update period []:

$$G_{DPWM}(s) = \frac{d(s)}{m(s)} = A(\omega, D, N_c)e^{-s\frac{T_c}{2}}, \tag{1}$$

where s is the complex variable of the Laplace transform, d is the continuous-time duty cycle used for averaged modeling [], ω is the angular frequency, and D is the steady-state duty cycle. The gain A can be approximated with unity gain with negligible losses in modeling accuracy []. In DSP applications, update of the modulating waveform is usually delayed by one control period T_c, due to the non-negligible computational time []. This update delay can be represented in s-domain as:

$$G_{ud}(s) = e^{-sT_c}. \tag{2}$$

Combining delays due to modulation (1) and algorithm computation (2) results in total digital delay being equal to:

$$\tau_d = \frac{3}{2}T_c = \frac{3}{2}\frac{T_{pwm}}{N_c}. \tag{3}$$

From (3), it can be seen that multi-update control reduces digital delays inversely to the multi-update factor N_c. Traditionally, double-update is the most often used method, which results in twice decreased delays compared to single-update. The term multisampled (multi-update) control is most often used when N_c is increased above 2. This kind of control is a promising way of bringing the digital control close to analog regarding achievable bandwidths []. However, care must be taken as significant nonlinearities are also introduced in the control system, mainly due to the discontinuity of the modulating waveform, which now features switching ripple component as well. For this reason, multi-update control is most often followed by feedback filtering, which entirely removes the switching ripple from the feedback signal [].

B. Discrete-time model of a three-phase RL load

Given the simplicity of the inverter topology with a RL load, its model can be easily derived directly in discrete-time domain, without the use of Tustin's method and transport delay approximations []. This kind of modeling is important for design of digital controllers, as it enables highest achievable bandwidths with inherent decoupling of dq axes []. Note that for direct-discrete modeling, the action of the PWM is assumed to be equal to a zero-order hold in stationary $\alpha\beta$ frame []:

$$G_{DPWM,\alpha\beta} \approx \frac{1 - e^{-sT_c}}{s}. \tag{4}$$

This is true for the case of single- and double-update PWM, however, for $N_c > 2$, the exact model is shown in (1). For the

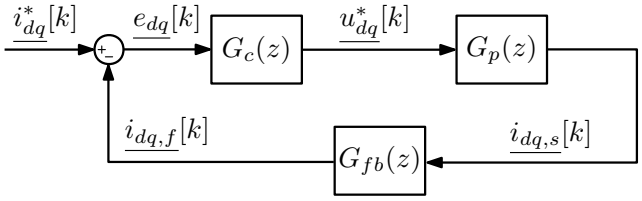

Fig. 2: Small-signal block diagram of the system from Fig. 1 in discrete-time domain.

very specific case of triangular carrier, MS-PWM can still be well-approximated with a ZOH with update rate equal to f_c, specially regarding its phase response [].

The direct discrete-time modeling can be found in [lorenz2010,vukosavic2016,DOI 10.1109/TPEL.2018.2841206]. This paper follows the procedure from [DOI 10.1109/TPEL.2018.2841206]. In order to analyze the three-phase RL load as single-input single-output (SISO) system, complex variables are used []. Starting from the $\alpha\beta$ frame, the differential equations necessary for modeling are:

$$\underline{u}_{\alpha\beta}(t) = R\underline{i}_{\alpha\beta}(t) + L\frac{d}{dt}\underline{i}_{\alpha\beta}(t), \tag{5}$$

where R and L are the line resistance and the line inductance, respectively. The machine back-emf or the grid voltage is neglected in this analysis, as the paper focuses purely on enhancing the current-loop response, without taking into account disturbance rejection. The s-domain transfer function from applied voltage to the line current, corresponding to (5) is:

$$G_{i,\alpha\beta} = \frac{1}{R}\frac{1}{1+s\frac{L}{R}}. \tag{6}$$

Multiplication of (2), (4) and (6) yields the plant model in $\alpha\beta$ frame. The transformation from $\alpha\beta$ to dq frame is obtained using the substitution $s \to s + j\omega_o$, where ω_o is the dq frame rotating frequency. This yields the following s-domain plant transfer function in dq frame:

$$G_{p,dq}(s) = e^{-(s+j\omega_o)T_c}\frac{1-e^{-(s+j\omega_o)T_c}}{s+j\omega_o}\frac{1}{R}\frac{1}{1+s\frac{L}{R}+j\omega_o\frac{L}{R}}. \tag{7}$$

The discrete-time model is obtained directly from (7) using $\mathcal{Z}$ transform table:

$$G_{p,dq}(z) = \frac{\left(1-e^{-\frac{R}{L}T_c}\right)e^{-2j\omega_o T_c}}{R}\frac{1}{z\left(z-e^{-\left(\frac{R}{L}+j\omega_o\right)T_c}\right)}, \tag{8}$$

where z is the complex variable of the $\mathcal{Z}$ transform.

The model obtained in (8) is used for the subsequent derivation of the model-based controller.

C. Discrete IMC controller

The dq frame discrete-time small signal block diagram of the control system in Fig. 1 is shown in Fig. 2. In this paper, IMC method is used to obtain the controller structure []. The goal of the method is to invert the plant model with addition of an integrator with gain α that determines the crossover frequency []. For the sake of causality, due to digital delays, additional factor of $\frac{1}{z^2}$ is added to the controller structure, which results in the following transfer function:

$$G_c(z) = \frac{\alpha\cdot z}{z-1}\frac{1}{z^2}G^{-1}_{p,dq}(z) = \frac{\alpha\cdot R\cdot e^{j\omega_o T_c}}{\left(1-e^{-\frac{R}{L}T_c}\right)}\frac{ze^{j\omega_o T_c}-e^{-\frac{R}{L}T_c}}{z-1}. \tag{9}$$

By implementing controller from (9), without any feedback filters, open-loop transfer function is obtained:

$$W_{ol,1}(z) = G_c(z)G_p(z) = \frac{\alpha}{z(z-1)} \tag{10}$$

In [vukosavic] it is shown that relying on two samples per T_{pwm} often results in unacceptable feedback signal deterioration in industrial applications. This is due to the unalignement between the voltage impulse and sampling instants due to limited current sensor bandwidths, analog feedback filters, delays in driver circuits, and similar. Furthermore, feedback signal often comprises oscillations due to the LC parasitics of long cables that are present in industrial drives. This is a motivation behind the implementation of MS-DU-PWM in[] and MS-MU-PWM in this paper, where the signal is highly oversampled and then averaged over T_{pwm}.

III. Feedback acquisition, coordinate frame transformation, and filtering

A. Feedback acquisition and $\alpha\beta - dq$ transformation

The timing diagram of feedback acquisition, coordinate frame transformation and controller update is shown in Fig. 3. The modulating waveform is illustrated for one phase, $m_a(t)$. The digital system analyzed in this paper features two independent frequencies. First one is the control frequency, which defines the controller execution rate and update of the modulating waveform. It is defined by the multi-update factor $f_c = N_c f_{pwm}$. Control interrupts over the switching period are synchronized with the carrier $w(t)$ such that the first one is occurs when the carrier is equal to 0 while other $N_c - 1$ are delayed by T_c each. The second frequency is the sampling frequency, which is defined by the multisampling factor $f_s = N_s f_{pwm}$. This factor allows the DSP to acquire the signal with much higher rate than it can calculate the control algorithm, by employing the standardly available DMA module. High sampling rates allow the use of digital filters, for example MAFs, and subsequent decimation to provide the feedback $i_{dq,f}[k]$ at the control execution rate. Again, sampling instants are synchronized with the carrier such that the first one occurs when the carrier is equal to 0. Note that it is sometimes useful to offset the sampling instants in order to compensate system delays for aliasing suppression [].

Fig. 3 is given for $N_c = 4$ and $N_s = 16$. At instant kT_c, dq frame feedback current $i_{dq,f}[k]$ is obtained and used to calculate the voltage reference $u^*_{dq}[k]$, which is used to calculate the segment of the modulating waveform that is applied at the beginning of the following control interrupt.

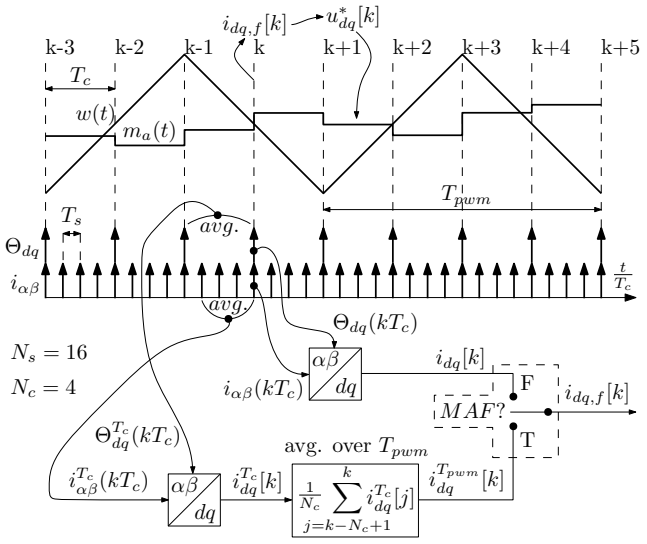

Fig. 3: nothing yet

The synchronous frame signal Θ_{dq} is obtained each T_c by implementing a PLL or using resolver/encoder sensors.

As shown in Fig. 3, the selector $MAF?$ chooses whether the feedback is provided without any filtering, or using a MAF over the switching period. In the first case, the latest samples of $i_{\alpha\beta}(kT_c)$ and $\Theta_{dq}(kT_c)$ are used to obtain the dq frame current $i_{dq}[k]$, which is used as the feedback signal. In case when $N_c = N_s = 2$, we obtain the standardly used DS-DU control. In cases when $N_c = N_s > 2$, we obtain the MS-MU-PWM with switching ripple in the feedback signal []. Due to the presence of switching ripple, this control method introduces nonlinearities caused by the discontinuity of the modulating waveform, which is more emphasized for lower values of N_c [].

In cases when the MAF is used, the goal is to obtain a true average value of dq currents over one switching period. The $\alpha\beta$ currents are first averaged over T_c, using $\frac{N_s}{N_c}$ latest current samples, to obtain $i^{T_c}_{\alpha\beta}(kT_c)$. This average current is then transformed to dq frame to obtain $i^{T_c}_{dq}[k]$. The transformation is performed using the angle $\Theta^{T_c}_{dq}(kT_c)$, calculated as an average of two latest angle values. If $N_c \geq 2$, currents are further averaged using N_c values of $i^{T_c}_{dq}$ to obtain the average value during the previous switching period $i^{T_{pwm}}_{dq}[k]$. For this filtering strategy, in cases when $N_s > N_c = 2$, we obtain MS-DU control, where the filtering is used to obtain a true-average value at the expense of reduced system dynamics []. In cases when $N_s \geq N_c > 2$, we obtain MS-MU-PWM control with switching ripple being filtered from the feedback signal. The factor N_s is chosen to be as high as allowed by the maximal ADC sampling rate.

B. Total time delay in DSP application

For control loop analysis and comparison between DS-DU-PWM, MS-DU-PWM, and MS-MU-PWM based on the crossover frequency and phase margin it is of interest to analyze the loop delays in continuous-time domain.

The equivalent time delay of the algorithm calculation and the DPWM modulation is shown in (3). For DS-DU-PWM without any feedback filtering, this corresponds to the total delay:

$$\tau_{d,DS-DU} = \frac{3}{2}\frac{T_{pwm}}{2}. \tag{11}$$

For MS-DU-PWM, MAF is most often used [] to filter out the switching frequency component. The phase lag of the MAF over T_{pwm} can be closely approximated by a pure delay equal to $\frac{T_{pwm}}{2}$ []. This results in the equivalent time-delay:

$$\tau_{d,MS-DU,MAF} = \frac{3}{2}\frac{T_{pwm}}{2} + \frac{T_{pwm}}{2} = \frac{5}{4}T_{pwm}. \tag{12}$$

For MS-MU-PWM without MAF, equivalent time-delay is equal to (3). Finally, for MS-MU-PWM with MAF, equivalent time-delay is:

$$\tau_{d,MS-MU,MAF} = \frac{3}{2}\frac{T_{pwm}}{N_c} + \frac{T_{pwm}}{2} = \frac{\frac{3}{N_c}+1}{2}T_{pwm}. \tag{13}$$

The MS-DU-PWM features significant time-delay due to MAF and high modulating and control delays. This kind of feedback acquisition is indeed often necessary due to high deterioration of the signal quality in industrial drives []. However, for high dynamic performance, MS-DU-PWM controller structure needs to include additional derivative gain compared to (9), to compensate for the high delays []. Regarding dynamics, best case is represented by the MS-MU-PWM without MAF. With high multi-update factors $N_c \geq 8$ [], control delays are practically removed and dynamic capabilities become equal to the ones of analog controllers []. Finally, from (13) it can be seen that for MS-MU-PWM with a MAF, starting from $N_c > 6$, equivalent time delay is lower than for the DS-DU-PWM. This is important as it states that the same kind of filtering as in MS-DU-PWM can be used to obtain a high quality feedback signal, while the dynamics is improved instead of deteriorated compared to standardly used DS-DU-PWM. Furthermore, this method removes the switching ripple, which is favorable regarding the MS-PWM nonlinearities related to the discontinuity of the modulating waveform [].

IV. Controller parameter design

For the purpose of controller tuning, the analysis is performed in discrete-time domain, with a rate equal to f_c. For this purpose, even if $N_s > N_c$, the MAF is approximated as a filter at frequency f_c using the following transfer function [vukosavic]:

$$G_{MAF}(z) = \frac{1 + 2z^{-\frac{N_c}{2}} + z^{-N_c}}{4}. \tag{14}$$

For the tested methods that do not use the feedback filter, the open-loop transfer function is given in (10). For methods that use the MAF, the open loop transfer function is equal to:

$$W_{ol,2}(z) = W_{ol,1}(z)G_{MAF}(z) \tag{15}$$

For a clear dynamic comparison, the controller gain α in (9) is set such that the phase margin equal to 70^o is achieved

for all tested methods. In this way, the crossover frequency is increased for methods with a lower equivalent time delay. In this paper, the verification is performed on a BLDC motor, with parameters shown in Table X.:

TABELA SA PARAMETRIMA MOTORA.

The first tested strategy is the standardly used DS-DU approach. For a 70^o phase margin, the value of α is equal to xxx and the achieved crossover frequency is equal to $xxxf_{pwm}$.. Even though the DS-DU strategy provides a satisfactory dynamic performance, it may exhibit poor behavior in presence of various noise sources, which is often the case in industrial applications []. The second tested strategy is the MS-DU control, which presents a modification of the DS-DU obtained with an addition of the oversampled MAF in the feedback path. This strategy provides a more robust feedback signal in the presence of high noise, however, it negatively impacts the dynamic performance. The controller gain α is equal to x, which sets the crossover frequency to $xxxf_{pwm}$. The proposed MS-MU method with a MAF based feedback acquisition is considered next. The controller gain α is equal to x, which set the crossover frequency to $xxxf_{pwm}$. DODATI I MS-MU BEZ MAF-a!

The summary of achieved crossover frequencies and phase margins are shown in Table I for all tested methods.

TABLE I: Control loop parameters

MS-MU+MAF	label	value	unit
IMC gain	α	0.0636	/
Cross-over frequency	f_c	798.5845	Hz
Phase margin	pm	70.2667	°
DS-DU	**label**	**value**	**unit**
IMC gain	α	0.25	/
Cross-over frequency	f_c	799.1594	Hz
Phase margin	pm	68.4572	°
MS-DU	**label**	**value**	**unit**
IMC gain	α	0.17	/
Cross-over frequency	f_c	538.7873	Hz
Phase margin	pm	65.7934	°

A. Verification of discrete-time modelling

For each of the tested control strategies, simulations in MATLAB/Simulink were performed in order to verify the discrete-time modeling. The sweep frequency response analysis (SFRA) is performed to verify open-loop models from (10) and (15). The current controller is modeled in discrete domain whereas all relevant delays are taken into account. A detailed model of DPWM, which resembles the action qualifier module realization within the DSP TI f28379d EPWM peripheral, is implemented. The load is modeled in continuous time domain using the Simulink abc frame machine model. The simulations are performed for the BLDC motor described in Table X. For the proposed MS-MU controller, the multi-update factor N_c is set to eight, which was limited by the total execution time of the FOC algorithm, implemented in the DSP TI f28379d

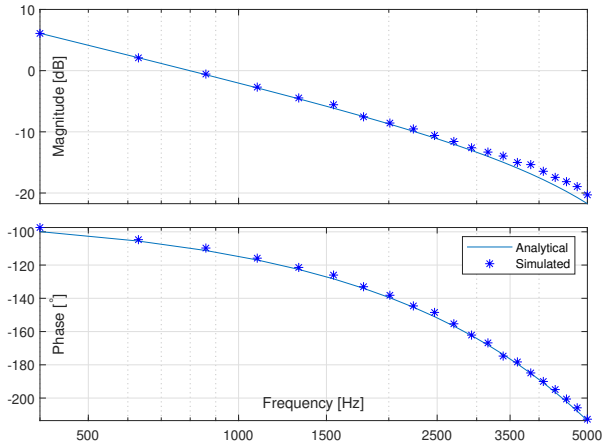

Fig. 4: Simulated open loop FRA results for MS-MU + MAF controller.

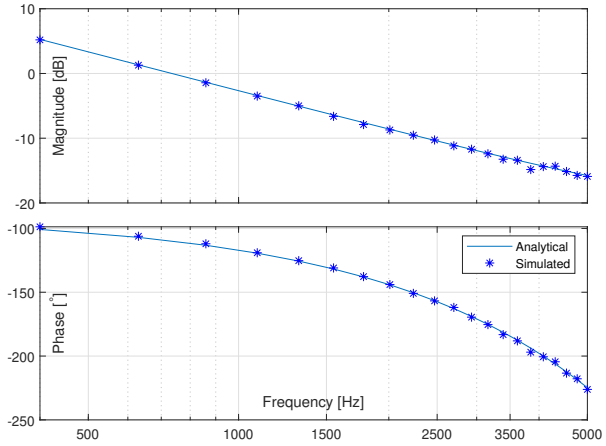

Fig. 5: Simulated open loop FRA results for DS-DU controller.

for later experimental validation. The multisampling factor N_s is set equal to 16. Additionally, anti-aliasing analog low-pass filter with time-constant of $\tau_{fil} = 5\mu s$) is used. Dead-time is set to 1% of the switching period. The motor speed is set to xxx rpm, which results in the output frequency $f_o = xxx$ Hz.

For the measured axis response, the perturbation magnitude is set to $0.1A$, while for the other axis the controller input is set to 0. The perturbation frequencies are an arithmetic sequence from $400Hz$ to $5000Hz$, with a step of $230Hz$. The q-axis open loop SFRA results for the three tested methods are shown in Fig. 4-6. The simulated results are compared to the analytics and it can be seen that a very good match is achieved for all compared strategies.

V. Experimental verification

This section provides the experimental validation of the previously discussed controllers using Typhoon HIL 402 platform and DSP TI F28379D. Power stage is implemented within Hardware-In-the-Loop simulation model and comprises DC voltage source, IGBT inverter and BLDC motor with parameters from Table. Two motor currents are displayed on HIL's analog outputs and routed to DSP's ADC inputs.

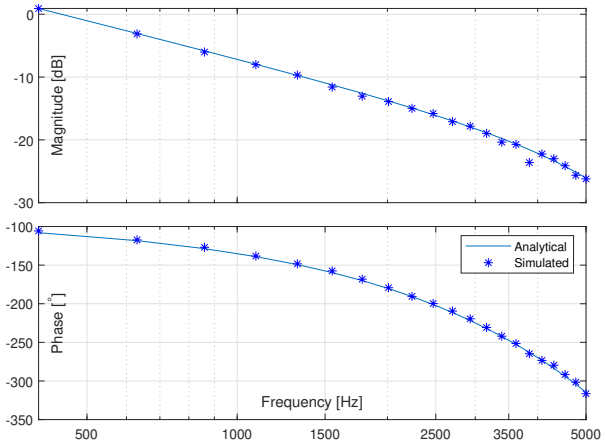

Fig. 6: Simulated open loop FRA results for MS-DU controller.

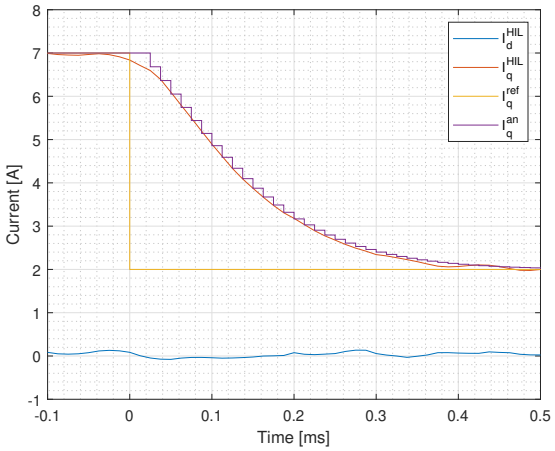

Fig. 7: Simulated step response for MS-MU + MAF controller.

Encoder signals from HIL's digital outputs are driven to the DSP's QEP inputs. These current and position feedback signals are used to perform FOC algorithm in the DSP in the same way as described in Section III. The resulting control signals are applied as gate signals by connecting DSP's EPWM outputs and HIL's digital inputs.

For each of the control strategies analyzed in Section IV, HIL simulations were performed to obtain q-axis current step responses and compare them to the step response of the closed loop transfer functions obtained via modelling approach described in Sections II and III. For the proposed MS-MU controller, the multi-update factor N_c is set to 8, which was limited by the total execution time. Note that in order for the DSP implementation of the MS-PWM to be immune to the pulse skipping due to the vertical crossings (Fig. 3), an adequate logic needs to be implemented in code. This prolongs the execution time, but still results in the execution time which allows use of $N_c = 8$. Dead-time is set to 1% of the switching period. The motor speed is set to $565rpm$, which results in the output frequency $f_o = 270Hz$.

Step responses are shown in Fig. 7-9. Note that the presented HIL results are obtained by post-processing of the signals exported from DSP's RAM. The abc domain currents are acquired at T_s and angle is acquired on T_c. Post-processing assumes transformation and averaging in the similar manner as described in Section III, with the only difference that non-causal MAF is used to remove switching ripple without introducing additional delay, so that the results are comparable to the ones obtained from analytics. According to the presented results there is a very good match between experimental and analytical results for all compared control strategies. DC error which is visible in case of DSDU controller (Fig. 8) is due to the aliasing present as a consequence of the delay introduced by HIL. This delay prevents the sampling instant to coincide with the middle of the current ripple. This emphasizes the shortcoming of the feedback acquisition which relies only on one sample.

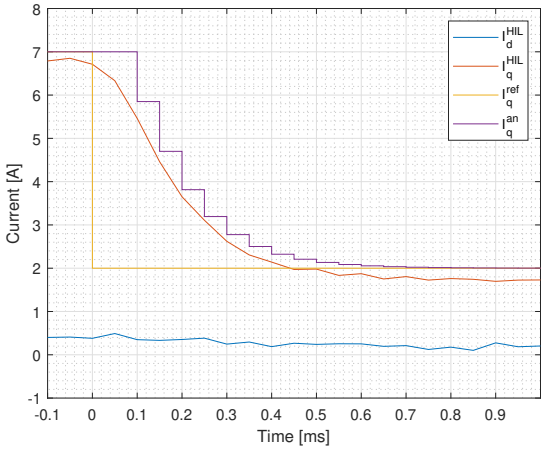

Fig. 8: Simulated step response for DS-DU controller.

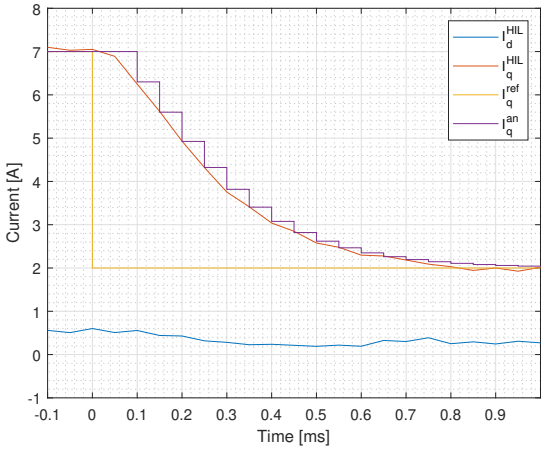

Fig. 9: Simulated step response for MS-DU controller.

VI. Further steps before publication

The steps are sorted from most important to less important.

- Experimental verification for all regimes tested in simulations, on f28379d DSP platform. It is important to obtain results on a standard, industrial DSP. f28335 is also an option, however it has lower CPU frequency, so I am not sure we would be able to get entire FOC with N =8. The

entire code for f28379d is already made, and tested in HIL simulations, so we are sure that the method works properly.
- Experimental veryfication of improvement obtained regarding jittering suppression. Motor currents should have much lower noise floor in multisampled case!
- Also, from experimental setup, it will be possible to see how does controller behave with multisampled control, without MAFs (perhaps just with some weaker digital filters). In simulations, it was working very well, but there we do not have switching noise due to high dV/dT.
- Perhaps, add part where phase lag due to MAF is compensated using proportional-derivative action, as in [10.1109/JESTPE.2018.2888980].

VII. Conclusion

Nothing yet.

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