Analysis and DSP Implementation of Multisampled Three-Phase Current Controller

***Abstract*—nothing yet**

***Index Terms*—nothing yet**

I. Introduction

FIELD oriented control (FOC) in electrical drives and voltage oriented control (VOC) in grid-connected converters is a well-established strategy for the control of high performance three-phase electrical systems [**?**]. An essential part of this concept is the inner current control loop, which regulates the synchronous rotating frame (SRF) currents [**?**]. A prerequisite for the proper operation of the outer control loops is a precise and rapid current controller [**?**], [**?**]. The SRF controller must provide a decoupling function between d and q axis currents []. This is particularly challenging for high-speed or high pole-pair electrical drives, which require robustness at very high output frequencies [**?**], [**?**], [**?**].

Due to simplicity and added flexibility, current controllers are nowadays mostly realized in digital form [Buso Matta]. The demerit of digital control systems is the introduction of delays due to the analog-to-digital conversion (ADC), algorithm execution time, and digital pulse width modulation (DPWM) [Buso Matta]. These delays limit the achievable bandwidths and impair the decoupling function of SRF current controllers. In most state-of-the-art applications, double-sampled double-update (DS-DU-PWM) control strategy is used, where the inductor currents are sampled twice per PWM period, with acquisition instants being synchronized so that average current values are obtained []. In industrial applications, feedback signal is often strongly corrupted by various noise sources, which requires additional filtering []. This is well-achieved by oversampling the signal and then averaging it over the PWM period. In this way, true-average is obtained with additional high noise suppression. The filtered signal is then decimated so that the control action is executed with double-update rate. This kind of strategy, implemented in [], is labeled as multi-sampled double-update (MS-DU-PWM) control. The MS-DU-PWM strategy results in a high quality feedback signal, however, with a highly negative impact on the system dynamics. Achieving high bandwidths with the additional delay due to the averaging requires modification of the controller structure to compensate the averaging phase lag [].

The delay-related limitations have inspired investigating multisampled PWM control, with purpose of enabling analog-like control bandwidths in digital systems. The multisampled multi-update (MS-MU-PWM) approach relies on acquiring the control variables and updating the modulating waveform multiple times per switching period [**?**]. The concept of MS-MU-PWM digital control offers significant reduction of digital delays and is therefore a promising solution for breaking the bandwidth limitations [**?**] [jos gomila citata za multisamping electrical drives]. Besides small-signal improvement, MS-MU-PWM has always additional nonlinear advantage that is obtained with the capability of modifying the modulating waveform multiple times per switching period. This is important for large-signal disturbance rejection [active filtering]. On the other hand, MS-MU-PWM introduces a set of nonlinearities due to sampling of the switching ripple, which is why some digital filtering should always be implemented [petric2021]. The impact of nonlinearities is strongly reduced by completely filtering the switching ripple, for example using moving average filters (MAFs).

Regarding controller structures, SRF PI controllers are the most frequently encountered current control strategies for three-phase RL loads due to their simplicity and satisfactory performance for the majority of the industry requirements [**?**], [**?**], [**?**]. With a proper parameter setting procedure, high bandwidths can be achieved [**?**], [**?**]. Nevertheless, their transient decoupling capability is rather limited, especially at high output frequencies [**?**]. Achieving robust operation with high bandwidths has driven the design of high-performance current controllers directly in discrete-time domain [**?**] [lorenz...]. The dead-beat current controllers offer very fast transient response but at the cost of considerable performance degradation in the presence of measurement errors and parameter mismatch, which is often the case in control of electric drives [**?**], [**?**], [**?**]. More robust operation is achieved with the use of the discrete internal model controller (IMC) design [**?**]. This strategy has proven to offer high closed loop bandwidths at very high output frequencies [**?**], [**?**] [petric IMC salient].

This paper analyzes the use of the discrete IMC based current controller with MS-MU-PWM, suitable for implementation on standard DSP platforms. The main goal of the paper is to analyze the performance of MS-MU-PWM in standard industrial applications, and to compare it with standardly used DS-DU-PWM and MS-DU-PWM methods. The target is to show that the MS-MU-PWM control with feedback averaging can offer high quality feedback signal as in MS-DU-PWM, while also providing improved dynamic performance compared to DS-DU-PWM. This gives potential of implementing MS-MU-PWM with feedback averaging as standard industrial procedure for current control.

II. Multi-rate control system

The multi-rate control system of a three-phase RL load in dq frame is shown in Fig. 1. The system can be separated into digital and continuous-time domain. An ADC is used to transform feedback signal from analog to digital domain. This action is performed with a sampling frequency $f_s = N_s f_{pwm}$,

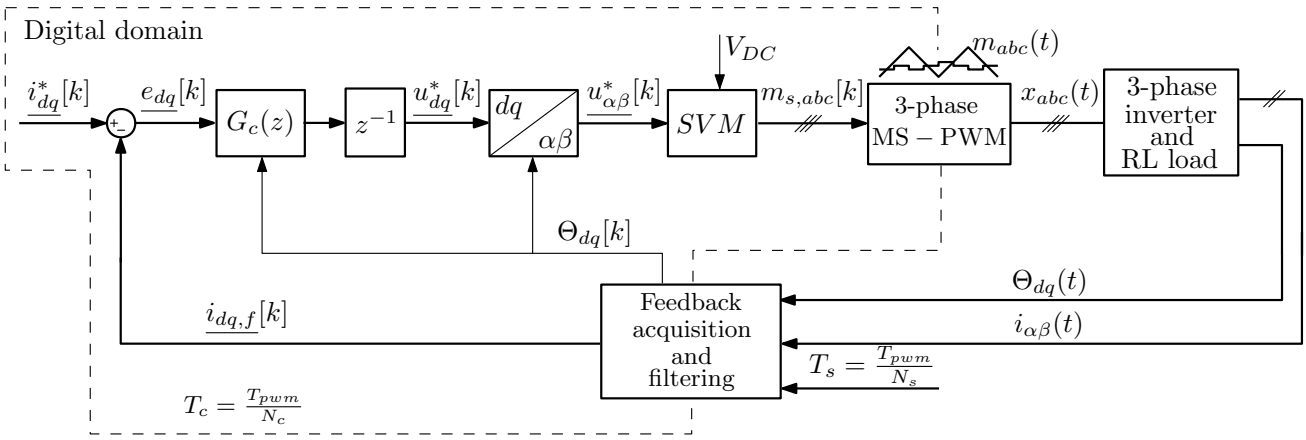


Fig. 1: Multisampled control loop of a three-phase inverter. ubaci 1/z da bi bio kompatibilan sa tajming dijagramom. Takodje, ubaci Feedback acquisition park transform and filtering

where N_s is the multisampling (oversampling) factor and f_{pwm} is the switching frequency of the inverter. The digital domain operates with frequency $f_c = N_c f_{pwm}$, where N_c is the multi-update factor that determines the update rate of the controller output. The choice of this frequency is independent of the sampling frequency, as the feedback signal can be oversampled with frequency f_s and then filtered and decimated to control frequency f_c. The digital domain is comprised of feedback filter $G_{fb}(z)$, controller $G_c(z)$, coordinate frame transformation block, and space vector modulation (SVM) block. The controller $G_c(z)$ outputs reference voltage in dq frame, $\underline{u_{dq}}^*[k]$, which is then transformed to $\alpha\beta$ frame. This reference voltage is used to obtain digital modulating waveform for each inverter phase, $m_{s,abc}[k]$. Conversion from digital to analog domain is performed by MS-PWM. Its inherent zero-order hold function transforms the digital impulse train $m_{s,abc}[k]$ into the continuous-time modulating waveform $m_{abc}(t)$. MS-PWM with the triangular carrier is used due to its favorable characteristics in MS-MU-PWM control []. The PWM output is used as a gate signal $x_{abc}(t)$. The three-phase inverter is used to supply the RL load, which can be an AC electrical machine or electrical grid. The sensed feedback includes line currents $i_{\alpha\beta}(t)$ and the angle of the dq coordinate frame Θ_{dq}.

A. Motivation behind MS-MU-PWM control

Modern processors feature high computational power, which enables short execution times for control routines. However, switching frequencies of power converters are hardware limited, and do not go over several tens of kHz for medium power applications. This hardware based limitation directly affects the realizable bandwidths of the current control loop, which subsequently limits the outer control loops. Therefore, pushing for highest possible bandwidths relative to the switching frequency is often a design criterion. One way of achieving that is the implementation of MS-MU-PWM [].

Using describing function approach, small-signal model of the multisampled PWM with triangular carrier is found to be almost equal to a pure delay of $\frac{T_c}{2}$, where T_c is the modulating waveform update period []:

$$G_{DPWM}(s) = \frac{d(s)}{m(s)} = A(\omega, D, N_c)e^{-s\frac{T_c}{2}}, \tag{1}$$

where s is the complex variable of the Laplace transform, d is the continuous-time duty cycle used for averaged modeling [], ω is the angular frequency, and D is the steady-state duty cycle. The gain A can be approximated with unity gain with negligible losses in modeling accuracy []. In DSP applications, update of the modulating waveform is usually delayed by one control period T_c, due to the non-negligible computational time []. This update delay can be represented in s-domain as:

$$G_{ud}(s) = e^{-sT_c}. \tag{2}$$

Combining delays due to modulation (1) and algorithm computation (2) results in total digital delay being equal to:

$$\tau_d = \frac{3}{2}T_c = \frac{3}{2}\frac{T_{pwm}}{N_c} \tag{3}$$

From (3), it can be seen that multi-update control reduces digital delays inversely proportionate to the multi-update factor N_c. Traditionally, double-update is the most often used method, which results in twice decreased delays compared to single-update. Term multisampled (multi-update) control is most often used when N_c is increased above 2. This kind of control is a promising way of bringing the digital control close to analog regarding achievable bandwidths []. However, care must be taken as significant nonlinearities are also introduced in the control system, mainly due to the discontinuity of the modulating waveform, which now features switching ripple component as well. For this reason, multi-update control is most often followed by feedback filtering, which entirely removes the switching ripple from the feedback signal [].

B. Discrete-time model of a three-phase RL load

Given the simplicity of the inverter topology with a RL load, its model can be easily derived directly in discrete-time domain, without the use of Tustin's method and transport delay approximations []. This kind of modeling is important for design of digital controllers, as it enables highest achievable bandwidths with inherent decoupling of dq axes []. Note

that for direct-discrete modeling, the action of the PWM is assumed to be equal to a zero-order hold in stationary $\alpha\beta$ frame []:

$$G_{DPWM,\alpha\beta} \approx \frac{1-e^{-sT_c}}{s}. \tag{4}$$

This is true for the case of single- and double-update PWM, however, for $N_c > 2$, the exact model is shown in (1). For the very specific case of triangular carrier, MS-PWM can still be well-approximated with a ZOH with update rate equal to f_c, specially regarding its phase response [].

The direct discrete-time modeling can be found in [lorenz2010,vuksa2016,DOI 10.1109/TPEL.2018.2841206]. This paper follows the procedure from [DOI 10.1109/TPEL.2018.2841206]. In order to analyze the three-phase RL load as single-input single-output (SISO) system, complex variables are used []. Starting from $\alpha\beta$ frame differential equations necessary for modeling are:

$$\underline{u}_{\alpha\beta}(t) = R\underline{i}_{\alpha\beta}(t) + L\frac{d}{dt}\underline{i}_{\alpha\beta}(t), \tag{5}$$

where R and L are the line resistance and the line inductance, respectively. The machine back-emf or the grid voltage is neglected in this analysis, as the paper focuses purely on enhancing the current-loop response, without taking into account disturbance rejection. The s-domain transfer function from applied voltage to the line current, corresponding to (5) is:

$$G_{i,\alpha\beta} = \frac{1}{R}\frac{1}{1+s\frac{L}{R}}. \tag{6}$$

Multiplication of (2), (4) and (6) yields the plant model in $\alpha\beta$ frame. The transformation from $\alpha\beta$ to dq frame is obtained using the substitution $s \to s + j\omega_o$, where ω_o is the dq frame rotating frequency. This yields the following s-domain plant transfer function in dq frame:

$$G_{p,dq}(s) = e^{-sT_c}e^{-j\omega_o}\frac{1-e^{-sT_c}e^{-j\omega_o T_c}}{s+j\omega_o}\frac{1}{R}\frac{1}{1+s\frac{L}{R}+j\omega_o\frac{L}{R}}. \tag{7}$$

The discrete-time model is obtained directly from (7) using $\mathcal{Z}$ transform table:

$$G_{p,dq}(z) = \frac{\left(1-e^{-\frac{R}{L}T_c}\right)e^{-2j\omega_o T_c}}{R}\frac{1}{z\left(z-e^{-\left(\frac{R}{L}+j\omega_o\right)T_c}\right)}, \tag{8}$$

where z is the complex variable of the $\mathcal{Z}$ transform.

The model obtained in 8 is used for the subsequent derivation of the model-based controller.

C. Discrete IMC controller

The dq frame discrete-time small signal block diagram of the control system in Fig. 1 is shown in Fig. 2. In this paper, IMC method is used to obtain the controller structure []. The goal of the method is to inverse the plant model with addition of an integrator with gain α that determines the crossover frequency []. For the sake of causality, due to digital delays, additional factor of $\frac{1}{z^2}$ is added to the controller structure, which results in the following transfer function:

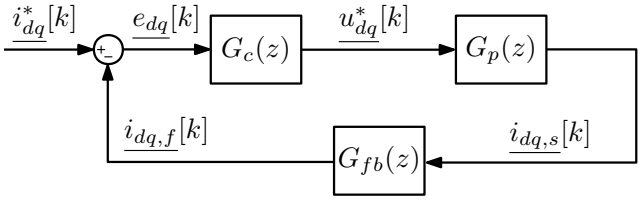


Fig. 2: Small-signal block diagram of the system from Fig. 1 in discrete-time domain.

$$G_c(z) = \frac{\alpha\cdot z}{z-1}\frac{1}{z^2}G^{-1}_{p,dq}(z) = \frac{\alpha\cdot R\cdot e^{j\omega_o T_c}}{\left(1-e^{-\frac{R}{L}T_c}\right)}\frac{ze^{j\omega_o T_c}-e^{-\frac{R}{L}T_c}}{z-1}. \tag{9}$$

By implementing controller from (9), without any feedback filters, open-loop transfer function is obtained:

$$W_{ol,1}(z) = G_c(z)G_p(z) = \alpha\frac{z}{z-1} \tag{10}$$

In [vuksa] it is shown that relying on two samples per T_{pwm} often results in unacceptable feedback signal deterioration in industrial applications. This is due to the unalignement between the voltage impulse and sampling instants due to limited current sensor bandwidths, analog feedback filters, delays in driver circuits, and similar. Furthermore, feedback signal often comprises oscillations due to the LC parasitics of long cables that are present in industrial drives. This is a motivation behind the implementation of MS-DU-PWM in[] and MS-MU-PWM in this paper, where the signal is highly oversampled and then averaged over T_{pwm}.

III. Feedback acquisition, coordinate frame transformation, and filtering

A. Feedback acquisition and $\alpha\beta - dq$ transformation

The timing diagram of feedback acquisition, coordinate frame transformation and controller update is shown in Fig. 3. The modulating waveform is illustrated for one phase, $m_a(t)$. The system analyzed in this paper features two independent discrete-time frequencies. First one is the control frequency, which defines the controller execution rate and update of the modulating waveform. It is defined by the multi-update factor $f_c = N_c f_{pwm}$. Control interrupts are synchronized with the carrier $w(t)$ such that two are always occurring at instants when carrier is equal to its maximum and zero value. Fig. 3 is given for $N_c = 4$. At instant k, dq frame feedback current $i_{dq,f}[k]$ is obtained and used to calculate the voltage reference $u^*_{dq}[k]$, which is used to calculate the segment of the modulating waveform that is applied at the beginning of the following control interrupt. As reported in [], N_c should be chosen as the highest possible value allowed by the DSP processing power, in order to decrease the MS-PWM nonlinearities introduced by the discontinuities of the modulating waveforms. The synchronous frame signal Θ_{dq} is obtained each T_c by implementing a PLL or using resolver/encoder sensors. The second frequency is the sampling frequency, which is defined by the multisampling factor $f_s = N_s f_{pwm}$. This

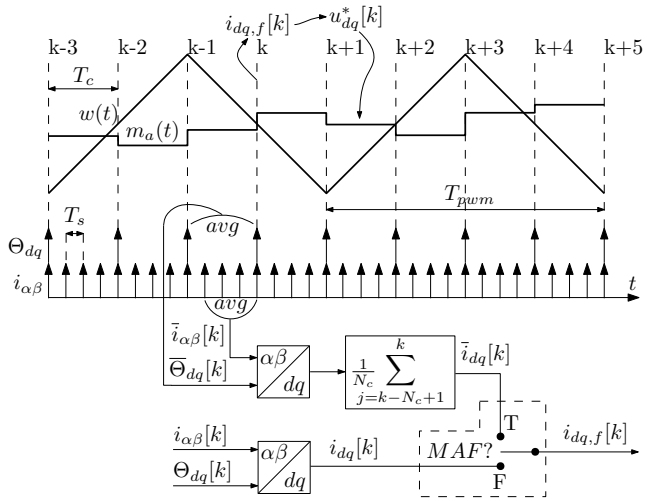


Fig. 3: nothing yet

factor allows the DSP to acquire the signal with much higher rate than it can calculate control algorithms, by employing standardly available DMA module. High sampling rates allow the subsequent use of digital filters, for example MAFs, to obtain a true average value each T_c - $i_{dq,f}[k]$.

In case of DS-DU-PWM method, $N_c = N_s = 2$, $i_{\alpha\beta}[k]$ and $\Theta_{dq}[k]$ are used to obtain $i_{dq,f}[k]$. This is the standard control method, most-often used in the state-of-the-art digital current controllers [].

In case of MS-DU-PWM methods, $N_c = 2$, $N_s > 2$. This kind of feedback acquisition is analyzed in []. The factor N_s is chosen to be as high as allowed by the maximal ADC sampling rate. At each control interrupt, package of $\alpha\beta$ frame currents is obtained via a DMA buffer, and averaged over T_c. This averaged current $\bar{i}_{\alpha\beta}[k]$ is transformed to dq frame using the average value of $\Theta_{dq}[k]$ and $\Theta_{dq}[k-1]$. Finally, the resulting dq frame current is filtered using MAF with the result from the previous interrupt to obtain feedback current averaged over the entire switching period, $\bar{i}_{dq}[k]$.

Finally, for the case of MS-MU-PWM methods, the procedure is the same as for MS-DU-PWM methods, except that $N_s \geq N_c > 2$. For MS-MU-PWM methods, MAF can be used in the same manner as for MS-DU-PWM, in order to avoid introducing switching ripple into the control loop. This filtering is not always used for MS-MU-PWM, when highest dynamic performance is required []. However, for three-phase industrial drives, the effect of nonlinearities introduced by the modulating waveform discontinuities still needs to be investigated.

For the purpose of later controller tuning, multi-rate system should be analyzed in a unique discrete-time domain, corresponding to the frequency f_c. For this reason, to avoid modified $\mathcal{Z}$ transform, MAF action can be closely analyzed using the following transfer function [vuksa]:

$$G_{MAF}(z) = \frac{1 + 2z^{-\frac{N_c}{2}} + z^{-N_c}}{4}. \tag{11}$$

B. Total time delay in DSP application

For control loop analysis and comparison between DS-DU-PWM, MS-DU-PWM, and MS-MU-PWM based on the crossover frequency and phase margin it is of interest to analyze loop delays in continuous-time domain.

The equivalent time delay of calculation and DPWM modulation is shown in (3). For DS-DU-PWM without any feedback filtering, this corresponds to the total delay:

$$\tau_{d,DS-DU} = \frac{3}{2}\frac{T_{pwm}}{2}. \tag{12}$$

For MS-DU-PWM, MAF is most often used [] to filter out the switching frequency component. The phase lag of the MAF over T_{pwm} can be closely approximated by a pure delay equal to $\frac{T_{pwm}}{2}$ []. This results in the equivalent time-delay:

$$\tau_{d,MS-DU,MAF} = \frac{3}{2}\frac{T_{pwm}}{2} + \frac{T_{pwm}}{2} = \frac{5}{4}T_{pwm}. \tag{13}$$

For MS-MU-PWM without MAF, equivalent time-delay is equal to (3). Finally, for MS-MU-PWM with MAF, equivalent time-delay is:

$$\tau_{d,MS-MU,MAF} = \frac{3}{2}\frac{T_{pwm}}{N_c} + \frac{T_{pwm}}{2} = \frac{\frac{3}{N_c}+1}{2}T_{pwm}. \tag{14}$$

From above the following can be concluded. First of all, MS-DU-PWM features significant time-delay due to MAF and high modulating and control delays. This kind of feedback acquisition is indeed often necessary due to high deterioration of the signal quality in industrial drives []. However, for high dynamic performance, MS-DU-PWM controller structure needs to include additional derivative gain compared to (9), to compensate for the high delays. Regarding dynamics, best case represents MS-MU-PWM without MAF. With high multi-update factors $N_c \geq 8$ [], control delays are practically removed and dynamic capabilities approach analog control. This means that the achievable bandwidths are limited purely by PWM frequency. However, strong nonlinearities may exhibit due to the introduction of the switching ripple component Finally, from (14) it can be seen that for MS-MU-PWM with a MAF, starting from $N_c > 6$, equivalent time delay is reduced compared to DS-DU-PWM. This is important, as the same kind of filtering as in MS-DU-PWM is used, which results in a high quality feedback signal, while the dynamics is improved compared to traditionally used DS-DU-PWM. By filtering the switching ripple, high nonlinearities due to multi-update control are strongly attenuated. In the end, it should be mentioned that multi-update control always features additional nonlinear advantage compared to DU, as the reference voltage can be modified N_c times per PWM period, which improves large-signal response of the controller.

IV. Simulation Results

In order to illustrate benefits of the proposed MS-PWM methodology, three different control loop architectures are examined in this section and their performance is evaluated by means of computer simulations in MATLAB/Simulink. It is distinguished between different MS-PWM control loop architectures based on current controller structure (IMC with

or without differential compensator) and feedback acquisition (with or without MAF). For each architecture of interest, at first, an appropriate benchmark controller is determined. Then, parameter setting procedure for the proposed MS-PWM controllers is explained. Finally, a comparison between proposed and benchmark controllers is illustrated by performance evaluation of the simulated step responses and open-loop frequency response analyses. In addition to this, analytically obtained results are compared with those from simulation, with the aim of verifying modelling approach explained in Section III.

Simulation is organized as follows. Current controller is modelled in discrete domain whereas all relevant delays are taken into account. Detailed model of DPWM, which resembles action qualifier module realization within DSP EPWM peripheral, is implemented. Load is modeled in continuous time domain using Simulink abc machine model. Simulation is developed so that it is easily adjustable for different update rates, controller structures and feedback acquisition paths. Simulation results presented in this section are obtained with BLDC motor from [**?**]. Switching frequency is set to 10kHz. For the proposed MS-PWM controllers, update rate is set to eight, i.e. acquiring the control variables and updating the modulating waveform is done eight times per switching period. MAF, when used for the feedback acquisition, assumes averaging of 16 samples per switching period.

The same simulation model is used to simulate step responses and perform FRA. However, the presented step responses are obtained with $1\mu s$ dead-time, whereas dead-time is set to 0 when running FRA simulations, so that non-linear effects which could mask FRA responses are avoided. Step responses are obtained at 270Hz electrical frequency. Open loop FRA simulations are organized in the following manner. For the analyzed axis, sinusoidal perturbation of 0.1 A is used as an excitation signal. Error in the other axis is set to zero. The perturbation frequencies are an arithmetic sequence starting from 400 Hz to 5000 Hz, with a step of 50 Hz.

A. Control loop architecture 1: N=8 with MAF, IMC

MS-PWM control loop architecture analyzed in this subsection (further on denoted as C1) assumes IMC controller from [**?**] with MAF in the feedback path. The benchmark for this case (further on denoted as B1) is the state-of-the art double update rate controller with the same IMC and standard synchronous sampling based feedback acquisition, with IMC gain α set to the highest value which results in the response without an overshoot [**?**]. The main advantage of C1, compared to B1, is a considerably enhanced noise suppression capability and a slightly improved dynamic response. IMC gain for C1 is set analytically so that the same cross-over frequency is obtained as for B1. Parameters for B1 and C1 are shown in Table I. Results presented within this subsection are denoted as test case 1 results.

Q current step responses for C1 and B1 are shown in Fig. 4-5. Presented waveforms are dq currents obtained by sampling and transformation process described in Section II. Acc. to the results in Fig. 4 no coupling between axes is present.

TABLE I: Parameters of controllers C1 and B1

C1 parameters	label	value
Update rate	N	8
IMC gain	α	0.0636
Feedback acquisition	/	MAF
B1 parameters	**label**	**value**
Update rate	N	2
IMC gain	α	0.25
Feedback acquisition	/	sync. sampl.

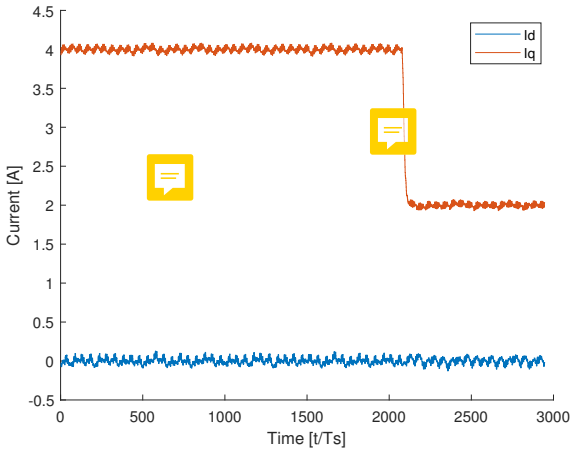


Fig. 4: Simulated step response for C1.

Even though step response itself is insufficient to fully describe dynamic behaviour of the control loop, it might be useful to get an insight and a rough estimate of the controller performance. Simulated and analytical step response characteristics for C1 and B1 are listed in Table II. Note that analytical rise time is calculated as $\pi/(10 * f^{an}_{bw-3dB})$. According to the results in Table II, C1 offers slightly improved dynamic performance compared to B1, which is expected, taking into account parameter setting procedure for the proposed controller. A slight mismatch between analytically calculated and simulated rise times both for C1 and B1, might be a consequence of the unmodelled dead-time non-linearities and an approximation used when deriving a feedback averaging model.

TABLE II: Simulated step response characteristics for test case 1

C1 characteristics	label	value	unit
Analytical 3dB closed loop bandwidth	f^{an}_{bw-3dB}	1.3871	kHz
Analytical rise time	$t^{an}_{rise}/Tpwm$	2.2685	/
Simulated rise time	$t^{sim}_{rise}/Tpwm$	2.75	/
B1 characteristics	**label**	**value**	**unit**
Analytical 3dB closed loop bandwidth	f^{an}_{bw-3dB}	1.4607	kHz
Analytical rise time	$t^{an}_{rise}/Tpwm$	2.1542	/
Simulated rise time	$t^{sim}_{rise}/Tpwm$	2.4	/

Q axis open loop FRA results for test case 1 are shown in Fig. 6. Comparison between simulated and analytical C1 FRA

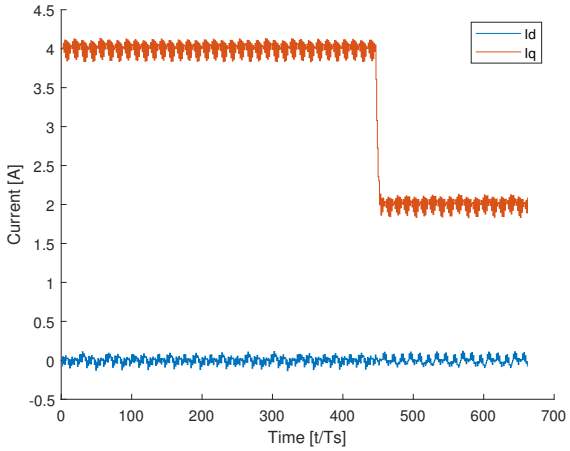


Fig. 5: Simulated step response for B1.

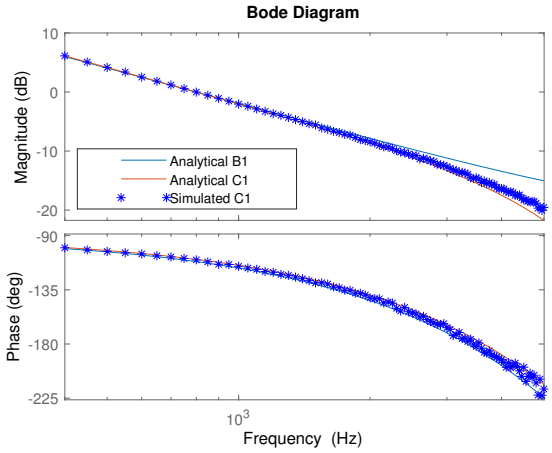


Fig. 6: Simulated open loop FRA for test case 1.

performance, as well as analytical B1 performance are listed in Table III. These results validate derived MS-PWM control loop analytical model, since mismatch between analytical and simulated C1 waveforms is hardly noticeable and exists only in the higher frequency range. In addition to this, cross-over frequency and phase margin of the simulated C1 control loop are similar to those of B1, which is in agreement with the parameter setting procedure described above. Therefore, test case 1 illustrates that MS-PWM approach offers MAF based feedback acquisition without degrading control loop dynamic performance. In this way, the noise and sampling errors in the feedback path are successfully eliminated due to MAF based feedback acquisition, but also the dynamic performance is kept high.

B. Control loop architecture C2: N=8 with MAF, IMC + dif.

MS-PWM control loop architecture analyzed in this subsection (further on denoted as C2) assumes IMC controller with differential compensator from [**?**] and MAF in the feedback path. This case is given to demonstrate that MS-PWM can offer even better dynamics than reported in [**?**]. The benchmark for this case (further on denoted as B2) assumes controller

TABLE III: Open loop FRA performance for test case 1

C1 characteristics	label	value	unit
Analytical cross-over frequency	f_c^{an}	798.5845	Hz
Simulated cross-over frequency	f_c^{sim}	800	Hz
Analytical phase margin	pm^{an}	70.2667	°
Simulated phase margin	pm^{sim}	70	°
B1 characteristics	**label**	**value**	**unit**
Analytical cross-over frequency	f_c^{an}	799.1594	Hz
Analytical phase margin	pm^{an}	68.4572	°

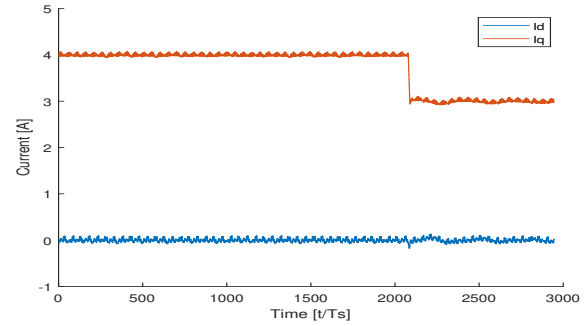
structure proposed in [**?**] - double update rate IMC controller with improved performance indices, differential compensator and MAF based feedback acquisition. In simulations, the advanced scheduling scheme for B2 is implemented without neglecting execution time so that the results are suitable for comparison with standard code implementation which does not assume execution time optimization. Gains for IMC and differential compensator in case of B2 are set to the optimal values from [**?**]. Parameter setting procedure used for C2 is similar to the one proposed in [**?**]. Parameters for B2 and C2 are shown in Table IV. Results presented within this subsection are denoted as test case 2 results.

TABLE IV: Parameters for controllers C2 and B2

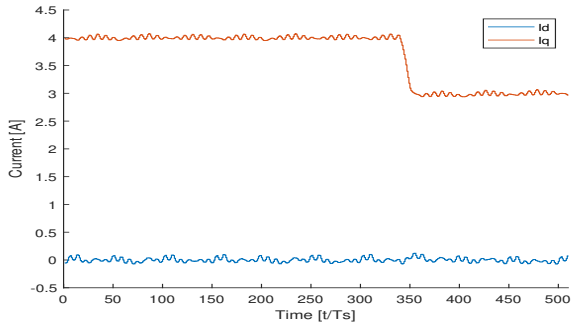
C2 parameters	label	value
Update rate	N	8
IMC gain	α	0.12038
Differential gain	d	2.1948
Feedback acquisition	/	MAF
B2 parameters	**label**	**value**
Update rate	N	2
IMC gain	α	0.38
Differential gain	d	0.444
Feedback acquisition	/	MAF

Q current step responses for C2 and B2 are shown in Fig. 7-8. Presented waveforms are dq currents obtained by sampling and transformation process described in Section II. Oscillations at the fundamental frequency are visible in C2 step response (Fig. 7a). Poor disturbance rejection capability due to small phase resistance might be the root cause of these oscillations, since with 5 times larger stator phase resistance oscillations are not present (Fig. 7b). In Fig. 8, two different step responses are shown to illustrate that oscillations at the fundamental frequency exist in the benchmark response too, but are of smaller amplitude and present only in case step reference change is larger. Source of the aforementioned oscillations needs to examined in more detail and will be considered as part of the future work. Addition of an active resistance feedback could be considered [**?**] if insufficient disturbance rejection capability of the proposed MS-PWM controller proves to be an issue.

Simulated and analytical step response characteristics for



(a)



(b)

Fig. 7: Simulated step response for C2: (a) original phase resistance; (b) 5 times larger phase resistance.

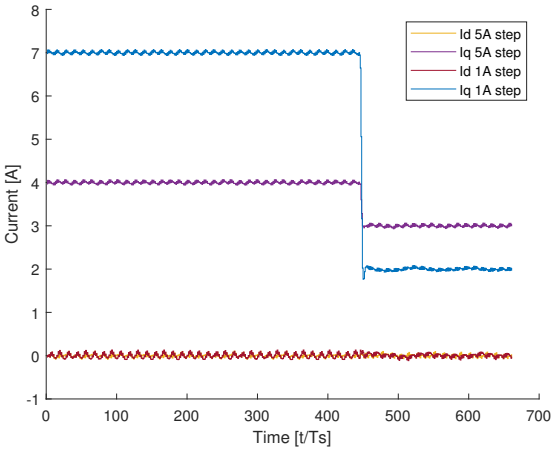


Fig. 8: Simulated step response for B2.

C1 and B1 are listed in Table V. Note that analytical transfer function for B2 assumed zero delay i.e. neglected execution time as in [**?**], since analytical representation of execution time which is smaller than regulation period would require modified Z transform. According to the results in Table V, C2 offers better dynamic performance than B2.

Q axis open loop FRA results for test case 2 are shown in Fig. 9. Comparison between simulated and analytical C2 FRA performance, as well as analytical B2 performance are listed in Table VI. Analytical and simulated waveforms for C2 are in good agreement, despite in the high frequency range where the MS-PWM control loop modelling approach described in Section II is of lower precision. C2 results in

TABLE V: Simulated step response characteristics for test case 2

C2 characteristics	label	value	unit
Analytical 3dB closed loop bandwidth	f_{bw-3dB}^{an}	3.9846	kHz
Analytical rise time	$t_{rise}^{an}/Tpwm$	0.7897	/
Simulated rise time	$t_{rise}^{sim}/Tpwm$	1.125	/
B2 characteristics	**label**	**value**	**unit**
Analytical 3dB closed loop bandwidth	f_{bw-3dB}^{an}	3.5105	kHz
Analytical rise time	$t_{rise}^{an}/Tpwm$	0.8964	/
Simulated rise time	$t_{rise}^{sim}/Tpwm$	1.25	/

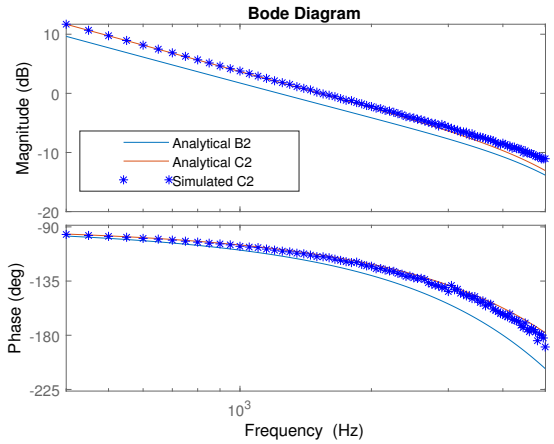


Fig. 9: Simulated open loop FRA for test case 2.

$1.5kHz$ cross-over frequency which is 25% higher than that of B2, whereas phase margin remains around $66°$ for both control loop architectures. Thus, the test case 2 illustrates that the MS-PWM approach offers better dynamic performance than the controller proposed in [**?**].

TABLE VI: Open loop FRA performance for test case 2

C2 characteristics	label	value	unit
Analytical cross-over frequency	f_c^{an}	1.5209	kHz
Simulated cross-over frequency	f_c^{sim}	1.55	kHz
Analytical phase margin	pm^{an}	66.838	°
Simulated phase margin	pm^{sim}	65.135	°
B2 characteristics	**label**	**value**	**unit**
Analytical cross-over frequency	f_c^{an}	1.2283	kHz
Analytical phase margin	pm^{an}	66.068	°

C. Control loop architecture C3: N=8 without MAF, IMC

MS-PWM control loop architecture analyzed in this subsection (further on denoted as C3) consists of IMC controller without any filters in the feedback. A benchmark for this case is the same as the benchmark for the previously analyzed case. C3 is expected to provide the dynamics better than B2, using discrete IMC without differential compensator. IMC gain for C3 is set analytically so that higher -3dB bandwidth is

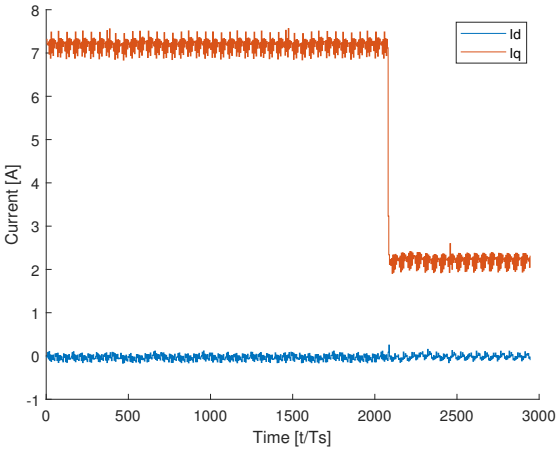


Fig. 10: Simulated step response for C3.

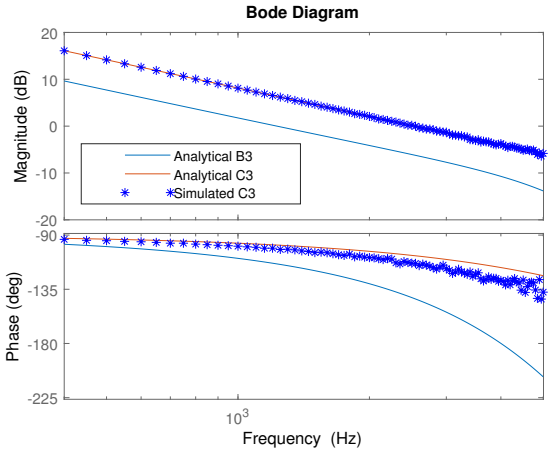


Fig. 11: Simulated open loop FRA for test case 3.

achieved than in case of the benchmark. Parameters for C3 are shown in Table VII. Results presented within this subsection are denoted as test case 3 results.

TABLE VII: Parameters for controller C3

C3 parameters	label	value
Update rate	N	8
IMC gain	α	0.2
Feedback acquisition	/	no filters

Q current step response for C3 is shown in Fig. 10. Presented waveforms are obtained by taking each 4th sample of the dq currents which are result of the sampling and transformation process described in Section II. The aim of such a representation is to avoid plotting switching ripple which, in case of C3, is present in the sampled dq currents, so that the results are comparable with previously presented ones. In this way, represented waveforms are equivalent, in terms of switching ripple magnitude, as those obtained by conventional double update synchronous sampling. Note that no coupling between axis is present in Fig. 10. Simulated and analytical C3 step response characteristics are listed in Table VIII. According to the results in Table V and VIII, C3 offers slightly improved dynamics compared to B2. Further increase of IMC gain for C3 could theoretically result in even faster step response. However, practical implementation aspects of the higher gains without any filters in the feedback have to be carefully examined.

TABLE VIII: Simulated step response characteristics for test case 3

C3 characteristics	label	value	unit
Analytical 3dB closed loop bandwidth	f_{bw-3dB}^{an}	3.9467	kHz
Analytical rise time	$t_{rise}^{an}/Tpwm$	0.7973	/
Simulated rise time	$t_{rise}^{sim}/Tpwm$	0.8594	/

Q axis open loop FRA results for test case 3 are shown in Fig. 11. Magnitude of the analytical and simulated waveforms for C3 are in good agreement. Simulated C3 phase characteristic, however, is slightly lower the analytical one. Comparison between simulated and analytical C3 FRA performance, as well as analytical B2 performance are listed in Table IX. According to the results in Table VI and IX, C3 offers considerably higher cross-over frequency than B2, whereas phase margin remains the same. Practical implementation of C3 might require addition of a low-pass filter in the feedback path in order to avoid issues which might arise as a consequence of sampling the switching noise. For $N = 8$, this is especially pronounced in the vicinity of the duty cycles which are equal to $0.25, 0.5$ and 0.75 ref?.

TABLE IX: Open loop FRA performance for test case 3

C3 characteristics	label	value	unit
Analytical cross-over frequency	f_c^{an}	2.5548	kHz
Simulated cross-over frequency	f_c^{sim}	2.55	kHz
Analytical phase margin	pm^{an}	72.7824	$^\circ$
Simulated phase margin	pm^{sim}	66.5165	$^\circ$

V. Experimental verification

VI. Conclusion