Analysis and DSP Implementation of Multisampled Digital Control of Electrical Drives

***Abstract*—nothing yet**

***Index Terms*—nothing yet**

I. Introduction

FIELD oriented control (FOC) is a well-established strategy for the control of high performance electrical drives [**?**]. An essential part of this concept is the inner current control loop [**?**]. A prerequisite for the proper operation of the outer control loops is a precise and rapid digital current controller [**?**]. In order to achieve the desirable performance of the overall control system high current loop bandwidth is imperative [**?**]. Robustness at high output frequencies, along with a decoupled d and q axis transient operation is also required [**?**], [**?**], [**?**]. Digital control introduces delays due to the sampling process, execution time and digital pulse width modulation (DPWM) [**?**]. These delays limit the achievable bandwidths and motivate the direct discrete-time domain design of high-performance current controllers [**?**]. These limitations have inspired investigating multisampled PWM control, with purpose of enabling analog-like control bandwidths in digital systems. The multisampling approach relies on acquiring the control variables and updating the modulating waveform multiple times per switching period [**?**]. The concept of multisampled digital control offers significant reduction of the modulator delays and therefore is a promising solution for breaking the bandwidth limitations [**?**]. Besides improvements in dynamic perofrmance, MS-PWM is also reported to have a positive impact on the noise attenuation [**?**].

Synchronous rotating frame (SRF) PI controllers are the most frequently encountered current control concepts since they are simple and successfully cover the majority of the industry requirements [**?**], [**?**], [**?**]. With a proper parameter setting procedure, high bandwidths can be achieved [**?**], [**?**]. Nevertheless, their transient decoupling capability is rather limited, especially at high speeds [**?**]. On the other hand, model predictive dead-beat current controllers offer very fast transient response but at the cost of considerable performance degradation when parameter mismatch occurs [**?**], [**?**]. Since saturation and temperature variations are very often encountered in electrical drives, a simple dead-beat approach might lead to insufficient performance. An FPGA implementation of the robust multisampled dead-beat control has been proposed in [**?**]. Another promising current control approach is the discrete internal model principle (IMC) design [**?**]. Since no S domain based delay approximations are used, axes cross-coupling is inherently eliminated and high closed loop bandwidths can be achieved [**?**], [**?**]. Despite all of the benefits of feedback averaging, the addition of a moving average filter in feedback path can considerably degrade the performance of the current control loop [**?**]. The IMC concept however, with some enhancements of the controller structure in terms of addition of differential compensator and advanced scheduling scheme, achieves very fast and robust current tracking even with MAF in the feedback path [**?**]. Further improvements in terms of active resistance feedback result in high disturbance rejection capability [**?**].

This paper analyzes the use of MS-PWM in discrete IMC based current controller, suitable for implementation on standard DSP platforms. The main goal of the paper is to demonstrate a current control structure, which offers improved dynamic response and high noise suppression compared to the state-of-the-art double update rate solutions. This is achieved without relying on expensive and complicated control platforms, but on a standard industrial DSP. The MS-PWM control strategy is analyzed for three different control loop organizations. The first one uses discrete IMC controller from [**?**], with a moving average filter (MAF) in the feedback. This case is found to offer slightly improved dynamics compared to standard use of double-update with the same discrete IMC (without filter in feedback) [**?**], [**?**], with significant improvement in jitter suppression. Due to added delays introduced by the MAF, the second case adds a derivative action to the controller structure, as in [**?**]. This case is given to demonstrate that MS-PWM can offer even better dynamics than reported in [**?**]. The final case implements MS-PWM based discrete IMC, without any filters in feedback. This case is expected to provide the best dynamics, using discrete IMC without derivative gain. The feedback quality is expected to worsen compared to cases with MAFs, hower, it still retains higher quality compared to double-update [**?**]. The target is to show that with the multisampling approach delays introduced by feedback averaging can be successfully compensated, by extent determined with the multisampling factor, enabling both robust and error-free feedback acquisition and a high dynamic performance of the current loop.

This paper is organized as follows. Section II addresses discrete time machine model, controller structure and analyzes delays introduced by feedback averaging, calculation and DPWM. The multisampling PWM approach, with an outline of its merits and demerits, is explained in Section III. A DSP implementation of the multisampling algorithm is also presented. Exact controller structures and parameter setting procedures for the three aforementioned cases of interest are derived in Section IV. Effectiveness of the derived analytical model is illustrated via simulated current loop step responses and frequency response analyses. Comparison between performance of the proposed methodology and benchmark controllers is also provided. Experimental results are shown in section V. Conclusions are drawn in section VI, along with a proposal

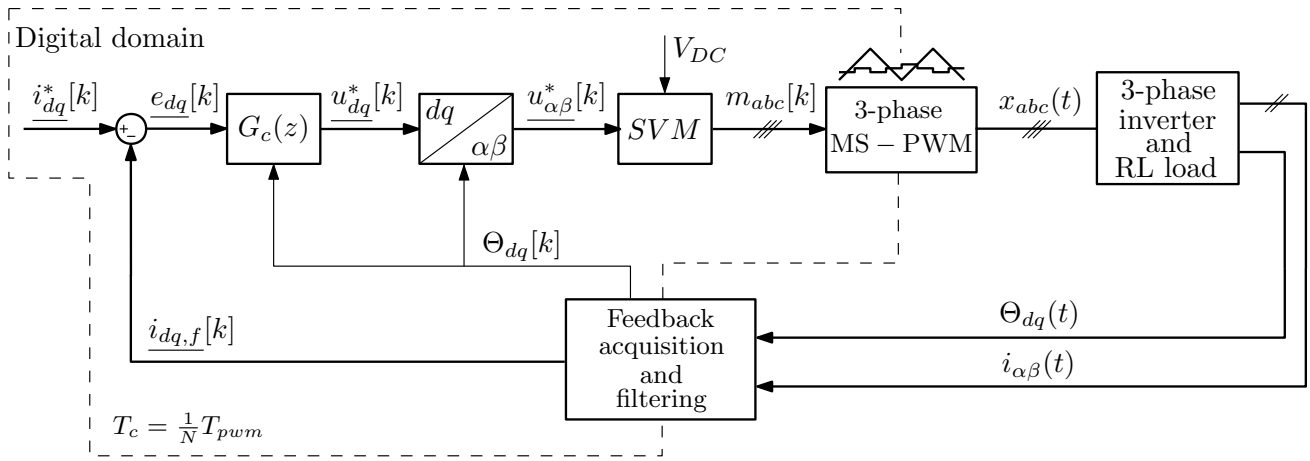


Fig. 1: Multisampled control loop of a three-phase inverter. ubaci 1/z da bi bio kompatibilan sa tajming dijagramom

for further studies on the presented topic.

II. Multi-rate control system

A. Control system overview and AC machine modeling

Ovde imas blok dijagram sa strukturom sistema, i small-signal blok dijagram. Nakon toga imas modelovanje masine sa jednacinama...

B. Motivation behind multisampling

Modern processors enable feature very high computational power, which enables short execution times for control routines. However, switching frequencies of the converter are still hardware limited, and do not go over several tens of kHz for industrial drive applications. This hardware based limitation directly affects the realizable bandwidths of the current control loop, which subsequently limits the speed and position responses as well. Therefore, using multisampled PWM control [] seems to be a logical step forward in the high-performance drive control. Using describing function approach, small-signal model of the multisampled PWM with triangular carrier is found to be almost equal to a pure delay of $\frac{T_c}{2}$, where T_c is the modulating waveform update period. Regarding its phase response, the triangular MS-PWM can be well-approximated with the zero-order hold, which is useful for later discrete-time modeling:

$$G_{DPWM}(s) \approx \frac{1 - e^{-sT_c}}{sT_c}, \tag{1}$$

where s is the complex variable of the Laplace transform.

C. Feedback acquisition and $\alpha\beta - dq$ transformation

Ovde onaj blok dijagram od ruzice lep sa transformacijama, pa da se objasni da zapravo koristis i DMA i bla bla .... Prethodno negde na pocetku rada prikazi multi-rate sliku i tu ubaci blok koji se zove feedback acquistion, ulaz su alpha beta struje i ugao, izlaz su dq struje, pa iza toga ide filtar u dq sistemu...

Ovde mozes da kazes: da bi stao ceo kod, ipak ne moze preveliki oversampling faktor. Zbog toga, umesto koriscenja

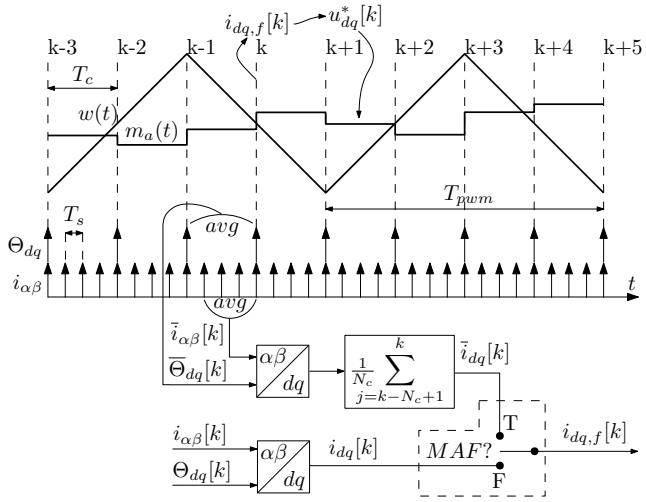


Fig. 2: nothing yet

klasicnog koda kao u subsection koji vec, koristi se DMA modul koji sempluje jos n puta brze tako da je ukupan oversampling rate jednak n*N. Nakon tih n odbiraka se zapravo trigeruje interrupt koji je povezan sa N oversamplingom uradi se MAF i decimira se tako da kontrolni kod radi na fc ucestanosti.

Depending on the algorithm complexity, $N_{max} \approx 8$ for 20 kHz PWM. Since this number cannot be too high, DMA module of the DSP can be used for higher oversampling action that is motivated by noise attenuation and error-free feedback acquisition []. This is performed by triggering sampling each $f_s = nf_c$ and storing results in an DMA array. After n samples are ready, interrupt flag is raised

Znaci razdvoj ucestanosti: fpwm - switching fs - sampling (fc - control frequency (Nfpwm)

III. Controller and feedback filter design

A. Discrete IMC controller

B. Total time delay in DSP application

Ovde pricaj o zbirnom kasnjenju, itd.... Mozda nakon price o modelovanju masine...

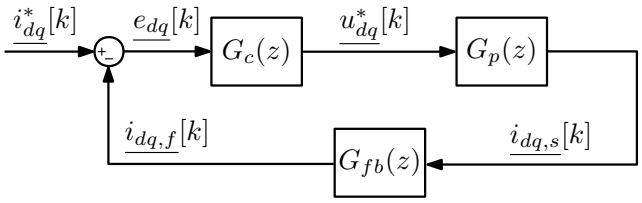


Fig. 3: Small-signal block diagram of the system from Fig. **??** in discrete-time domain.

IV. Simulation results

In order to illustrate benefits of the proposed MS-PWM methodology, three different control loop architectures are examined in this section and their performance is evaluated by means of computer simulations in MATLAB/Simulink. It is distinguished between different MS-PWM control loop architectures based on current controller structure (IMC with or without differential compensator) and feedback acquisition (with or without MAF). For each architecture of interest, at first, an appropriate benchmark controller is determined. Then, parameter setting procedure for the proposed MS-PWM controllers is explained. Finally, a comparison between proposed and benchmark controllers is illustrated by performance evaluation of the simulated step responses and open-loop frequency response analyses. In addition to this, analytically obtained results are compared with those from simulation, with the aim of verifying modelling approach explained in Section III.

Simulation is organized as follows. Current controller is modelled in discrete domain whereas all relevant delays are taken into account. Detailed model of DPWM, which resembles action qualifier module realization within DSP EPWM peripheral, is implemented. Load is modeled in continuous time domain using Simulink abc machine model. Simulation is developed so that it is easily adjustable for different update rates, controller structures and feedback acquisition paths. Simulation results presented in this section are obtained with BLDC motor from [**?**]. Switching frequency is set to 10kHz. For the proposed MS-PWM controllers, update rate is set to eight, i.e. acquiring the control variables and updating the modulating waveform is done eight times per switching period. MAF, when used for the feedback acquisition, assumes averaging of 16 samples per switching period.

The same simulation model is used to simulate step responses and perform FRA. However, the presented step responses are obtained with $1\mu s$ dead-time, whereas dead-time is set to 0 when running FRA simulations, so that non-linear effects which could mask FRA responses are avoided. Step responses are obtained at 270Hz electrical frequency. Open loop FRA simulations are organized in the following manner. For the analyzed axis, sinusoidal perturbation of 0.1 A is used as an excitation signal. Error in the other axis is set to zero. The perturbation frequencies are an arithmetic sequence starting from 400 Hz to 5000 Hz, with a step of 50 Hz.

A. Control loop architecture 1: N=8 with MAF, IMC

MS-PWM control loop architecture analyzed in this subsection (further on denoted as C1) assumes IMC controller from [**?**] with MAF in the feedback path. The benchmark for this case (further on denoted as B1) is the state-of-the art double update rate controller with the same IMC and standard synchronous sampling based feedback acquisition, with IMC gain α set to the highest value which results in the response without an overshoot [**?**]. The main advantage of C1, compared to B1, is a considerably enhanced noise suppression capability and a slightly improved dynamic response. IMC gain for C1 is set analytically so that the same cross-over frequency is obtained as for B1. Parameters for B1 and C1 are shown in Table **??**. Results presented within this subsection are denoted as test case 1 results.

TABLE I: Parameters of controllers C1 and B1

C1 parameters	label	value
Update rate	N	8
IMC gain	α	0.0636
Feedback acquisition	/	MAF
B1 parameters	**label**	**value**
Update rate	N	2
IMC gain	α	0.25
Feedback acquisition	/	sync. sampl.

Q current step responses for C1 and B1 are shown in Fig. **??**-**??**. Presented waveforms are dq currents obtained by sampling and transformation process described in Section II. Acc. to the results in Fig. **??** no coupling between axes is present. Even though step response itself is insufficient to fully describe dynamic behaviour of the control loop, it might be useful to get an insight and a rough estimate of the controller performance. Simulated and analytical step response characteristics for C1 and B1 are listed in Table **??**. Note that analytical rise time is calculated as $\pi/(10 * f^{an}_{bw-3dB})$. According to the results in Table **??**, C1 offers slightly improved dynamic performance compared to B1, which is expected, taking into account parameter setting procedure for the proposed controller. A slight mismatch between analytically calculated and simulated rise times both for C1 and B1, might be a consequence of the unmodelled dead-time non-linearities and an approximation used when deriving a feedback averaging model.

TABLE II: Simulated step response characteristics for test case 1

C1 characteristics	label	value	unit
Analytical 3dB closed loop bandwidth	f^{an}_{bw-3dB}	1.3871	kHz
Analytical rise time	$t^{an}_{rise}/Tpwm$	2.2685	/
Simulated rise time	$t^{sim}_{rise}/Tpwm$	2.75	/
B1 characteristics	**label**	**value**	**unit**
Analytical 3dB closed loop bandwidth	f^{an}_{bw-3dB}	1.4607	kHz
Analytical rise time	$t^{an}_{rise}/Tpwm$	2.1542	/
Simulated rise time	$t^{sim}_{rise}/Tpwm$	2.4	/

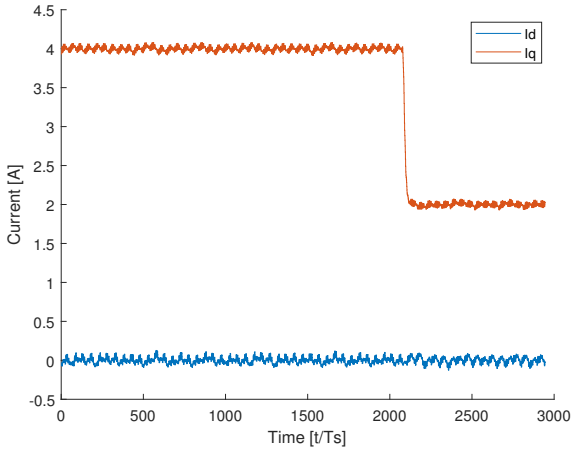


Fig. 4: Simulated step response for C1.

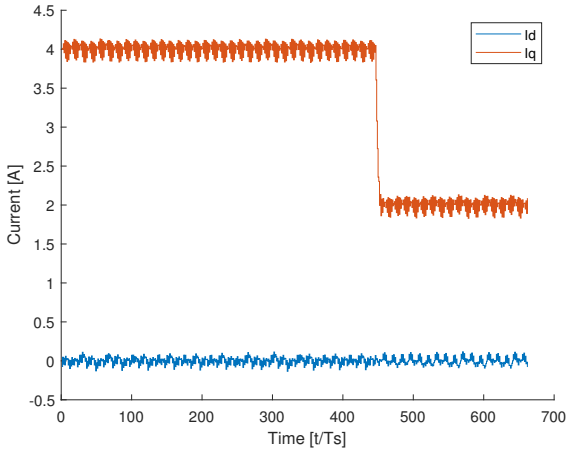


Fig. 5: Simulated step response for B1.

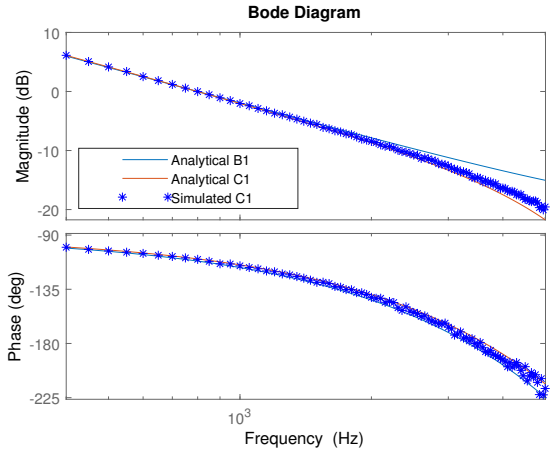


Fig. 6: Simulated open loop FRA for test case 1.

TABLE III: Open loop FRA performance for test case 1

C1 characteristics	label	value	unit
Analytical cross-over frequency	f_c^{an}	798.5845	Hz
Simulated cross-over frequency	f_c^{sim}	800	Hz
Analytical phase margin	pm^{an}	70.2667	°
Simulated phase margin	pm^{sim}	70	°
B1 characteristics	**label**	**value**	**unit**
Analytical cross-over frequency	f_c^{an}	799.1594	Hz
Analytical phase margin	pm^{an}	68.4572	°

Q axis open loop FRA results for test case 1 are shown in Fig. **??**. Comparison between simulated and analytical C1 FRA performance, as well as analytical B1 performance are listed in Table **??**. These results validate derived MS-PWM control loop analytical model, since mismatch between analytical and simulated C1 waveforms is hardly noticeable and exists only in the higher frequency range. In addition to this, cross-over frequency and phase margin of the simulated C1 control loop are similar to those of B1, which is in agreement with the parameter setting procedure described above. Therefore, test case 1 illustrates that MS-PWM approach offers MAF based feedback acquisition without degrading control loop dynamic performance. In this way, the noise and sampling errors in the feedback path are successfully eliminated due to MAF based feedback acquisition, but also the dynamic performance is kept high.

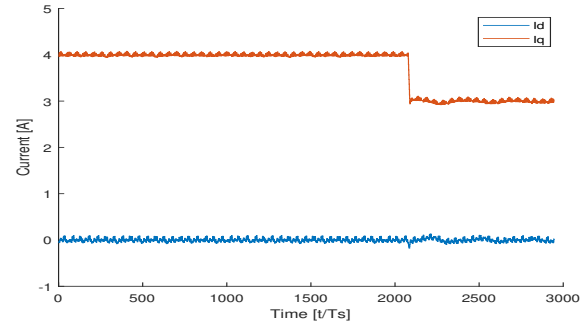
B. Control loop architecture C2: N=8 with MAF, IMC + dif.

MS-PWM control loop architecture analyzed in this subsection (further on denoted as C2) assumes IMC controller with differential compensator from [**?**] and MAF in the feedback path. This case is given to demonstrate that MS-PWM can offer even better dynamics than reported in [**?**]. The benchmark for this case (further on denoted as B2) assumes controller structure proposed in [**?**] - double update rate IMC controller with improved performance indices, differential compensator and MAF based feedback acquisition. In simulations, the advanced scheduling scheme for B2 is implemented without neglecting execution time so that the results are suitable for comparison with standard code implementation which does not assume execution time optimization. Gains for IMC and differential compensator in case of B2 are set to the optimal values from [**?**]. Parameter setting procedure used for C2 is similar to the one proposed in [**?**]. Parameters for B2 and C2 are shown in Table **??**. Results presented within this subsection are denoted as test case 2 results.

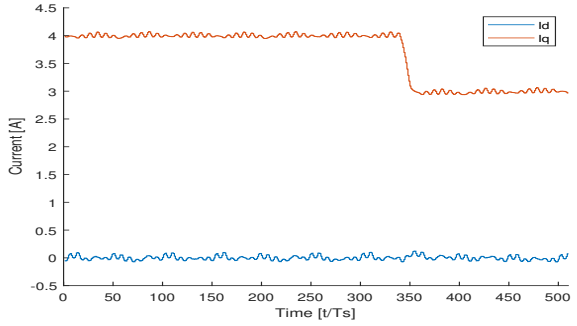
Q current step responses for C2 and B2 are shown in Fig. **??**-**??**. Presented waveforms are dq currents obtained by sampling and transformation process described in Section II. Oscillations at the fundamental frequency are visible in C2 step response (Fig. **??**). Poor disturbance rejection capability due to small phase resistance might be the root cause of these oscillations, since with 5 times larger stator phase resistance oscillations are not present (Fig. **??**). In Fig. **??**, two different step responses are shown to illustrate that oscillations at the fundamental frequency exist in the benchmark response too, but are of smaller amplitude and present only in case step reference change is larger. Source of the aforementioned oscillations needs to examined in more detail and will be

TABLE IV: Parameters for controllers C2 and B2

C2 parameters	label	value
Update rate	N	8
IMC gain	α	0.12038
Differential gain	d	2.1948
Feedback acquisition	/	MAF
B2 parameters	**label**	**value**
Update rate	N	2
IMC gain	α	0.38
Differential gain	d	0.444
Feedback acquisition	/	MAF



(a)



(b)

Fig. 7: Simulated step response for C2: (a) original phase resistance; (b) 5 times larger phase resistance.

considered as part of the future work. Addition of an active resistance feedback could be considered [**?**] if insufficient disturbance rejection capability of the proposed MS-PWM controller proves to be an issue.

Simulated and analytical step response characteristics for C1 and B1 are listed in Table **??**. Note that analytical transfer function for B2 assumed zero delay i.e. neglected execution time as in [**?**], since analytical representation of execution time which is smaller than regulation period would require modified Z transform. According to the results in Table **??**, C2 offers better dynamic performance than B2.

Q axis open loop FRA results for test case 2 are shown in Fig. **??**. Comparison between simulated and analytical C2 FRA performance, as well as analytical B2 performance are listed in Table **??**. Analytical and simulated waveforms for C2 are in good agreement, despite in the high frequency

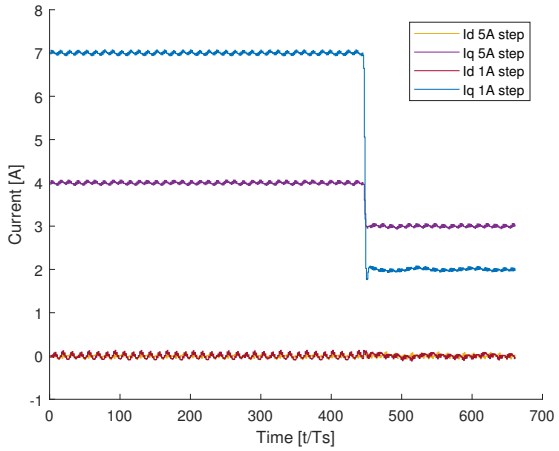


Fig. 8: Simulated step response for B2.

TABLE V: Simulated step response characteristics for test case 2

C2 characteristics	label	value	unit
Analytical 3dB closed loop bandwidth	f_{bw-3dB}^{an}	3.9846	kHz
Analytical rise time	$t_{rise}^{an}/Tpwm$	0.7897	/
Simulated rise time	$t_{rise}^{sim}/Tpwm$	1.125	/
B2 characteristics	**label**	**value**	**unit**
Analytical 3dB closed loop bandwidth	f_{bw-3dB}^{an}	3.5105	kHz
Analytical rise time	$t_{rise}^{an}/Tpwm$	0.8964	/
Simulated rise time	$t_{rise}^{sim}/Tpwm$	1.25	/

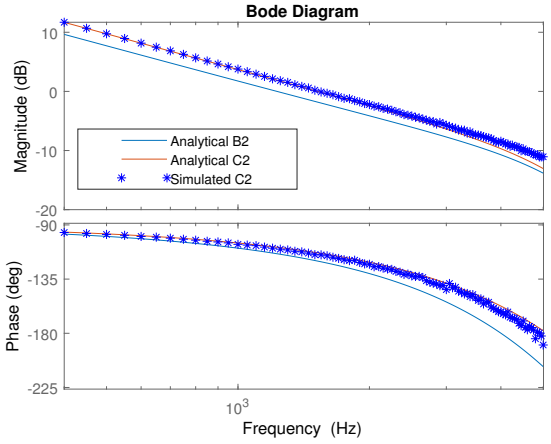


Fig. 9: Simulated open loop FRA for test case 2.

range where the MS-PWM control loop modelling approach described in Section II is of lower precision. C2 results in $1.5kHz$ cross-over frequency which is 25% higher than that of B2, whereas phase margin remains around $66°$ for both control loop architectures. Thus, the test case 2 illustrates that the MS-PWM approach offers better dynamic performance than the controller proposed in [**?**].

TABLE VI: Open loop FRA performance for test case 2

C2 characteristics	label	value	unit
Analytical cross-over frequency	f_c^{an}	1.5209	kHz
Simulated cross-over frequency	f_c^{sim}	1.55	kHz
Analytical phase margin	pm^{an}	66.838	°
Simulated phase margin	pm^{sim}	65.135	°
B2 characteristics	**label**	**value**	**unit**
Analytical cross-over frequency	f_c^{an}	1.2283	kHz
Analytical phase margin	pm^{an}	66.068	°

C. Control loop architecture C3: N=8 without MAF, IMC

MS-PWM control loop architecture analyzed in this subsection (further on denoted as C3) consists of IMC controller without any filters in the feedback. A benchmark for this case is the same as the benchmark for the previously analyzed case. C3 is expected to provide the dynamics better than B2, using discrete IMC without differential compensator. IMC gain for C3 is set analytically so that higher -3dB bandwidth is achieved than in case of the benchmark. Parameters for C3 are shown in Table **??**. Results presented within this subsection are denoted as test case 3 results.

TABLE VII: Parameters for controller C3

C3 parameters	label	value
Update rate	N	8
IMC gain	α	0.2
Feedback acquisition	/	no filters

Q current step response for C3 is shown in Fig. **??**. Presented waveforms are obtained by taking each 4th sample of the dq currents which are result of the sampling and transformation process described in Section II. The aim of such a representation is to avoid plotting switching ripple which, in case of C3, is present in the sampled dq currents, so that the results are comparable with previously presented ones. In this way, represented waveforms are equivalent, in terms of switching ripple magnitude, as those obtained by conventional double update synchronous sampling. Note that no coupling between axis is present in Fig. **??**. Simulated and analytical C3 step response characteristics are listed in Table **??**. According to the results in Table **??** and **??**, C3 offers slightly improved dynamics compared to B2. Further increase of IMC gain for C3 could theoretically result in even faster step response. However, practical implementation aspects of the higher gains without any filters in the feedback have to be carefully examined.

TABLE VIII: Simulated step response characteristics for test case 3

C3 characteristics	label	value	unit
Analytical 3dB closed loop bandwidth	f_{bw-3dB}^{an}	3.9467	kHz
Analytical rise time	$t_{rise}^{an}/Tpwm$	0.7973	/
Simulated rise time	$t_{rise}^{sim}/Tpwm$	0.8594	/

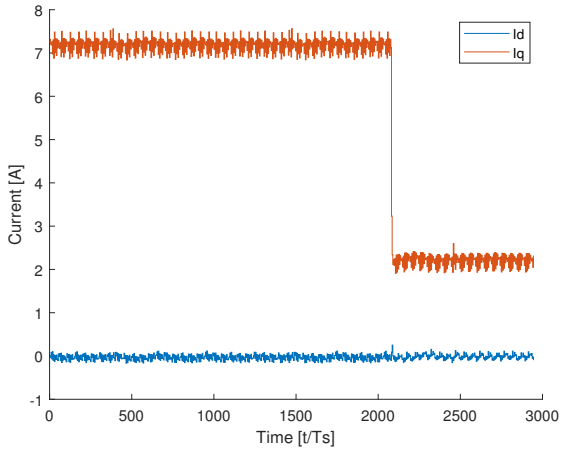


Fig. 10: Simulated step response for C3.

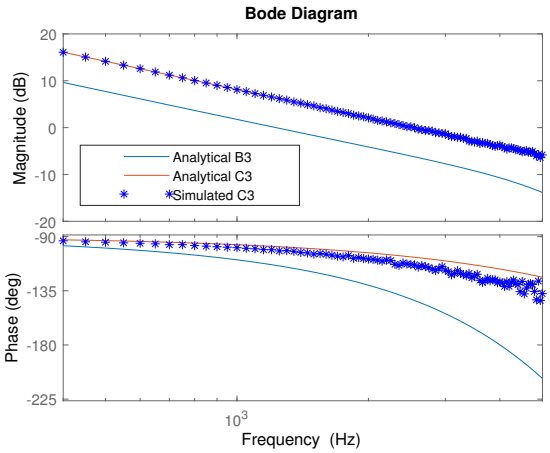


Fig. 11: Simulated open loop FRA for test case 3.

Q axis open loop FRA results for test case 3 are shown in Fig. **??**. Magnitude of the analytical and simulated waveforms for C3 are in good agreement. Simulated C3 phase characteristic, however, is slightly lower the analytical one. Comparison between simulated and analytical C3 FRA performance, as well as analytical B2 performance are listed in Table **??**. According to the results in Table **??** and **??**, C3 offers considerably higher cross-over frequency than B2, whereas phase margin remains the same. Practical implementation of C3 might require addition of a low-pass filter in the feedback path in order to avoid issues which might arise as a consequence of sampling the switching noise. For $N = 8$, this is especially pronounced in the vicinity of the duty cycles which are equal to $0.25, 0.5$ and 0.75 ref?.

TABLE IX: Open loop FRA performance for test case 3

C3 characteristics	label	value	unit
Analytical cross-over frequency	f_c^{an}	2.5548	kHz
Simulated cross-over frequency	f_c^{sim}	2.55	kHz
Analytical phase margin	pm^{an}	72.7824	°
Simulated phase margin	pm^{sim}	66.5165	°

V. Experimental verification
VI. Conclusion