

Analysis and DSP Implementation of Multisampled Digital Control of Electrical Drives

Abstract—nothing yet

Index Terms—nothing yet

I. INTRODUCTION

FIELD oriented control (FOC) is a well-established strategy for the control of high performance electrical drives [1]. An essential part of this concept is the inner current control loop [2]. A prerequisite for the proper operation of the outer control loops is a precise and rapid digital current controller [3]. In order to achieve the desirable performance of the overall control system high current loop bandwidth is imperative [4]. Robustness at high output frequencies, along with a decoupled d and q axis transient operation is also required [4]–[6]. Digital control introduces delays due to the sampling process, execution time and digital pulse width modulation (DPWM) [2]. These delays limit the achievable bandwidths and motivate the direct discrete-time domain design of high-performance current controllers [7]. These limitations have inspired investigating multisampled PWM control, with purpose of enabling analog-like control bandwidths in digital systems. The multisampling approach relies on acquiring the control variables and updating the modulating waveform multiple times per switching period [8]. The concept of multisampled digital control offers significant reduction of the modulator delays and therefore is a promising solution for breaking the bandwidth limitations [9]. Besides improvements in dynamic performance, MS-PWM is also reported to have a positive impact on the noise attenuation [10].

Synchronous rotating frame (SRF) PI controllers are the most frequently encountered current control concepts since they are simple and successfully cover the majority of the industry requirements [3], [7], [11]. With a proper parameter setting procedure, high bandwidths can be achieved [2], [3]. Nevertheless, their transient decoupling capability is rather limited, especially at high speeds [12]. On the other hand, model predictive dead-beat current controllers offer very fast transient response but at the cost of considerable performance degradation when parameter mismatch occurs [13], [14]. Since saturation and temperature variations are very often encountered in electrical drives, a simple dead-beat approach might lead to insufficient performance. An FPGA implementation of the robust multisampled dead-beat control has been proposed in [15]. Another promising current control approach is the discrete internal model principle (IMC) design [16]. Since no S domain based delay approximations are used, axes cross-coupling is inherently eliminated and high closed loop bandwidths can be achieved [17], [18]. Despite all of the benefits of feedback averaging, the addition of a moving average filter in feedback path can considerably degrade the

performance of the current control loop [18]. The IMC concept however, with some enhancements of the controller structure in terms of addition of differential compensator and advanced scheduling scheme, achieves very fast and robust current tracking even with MAF in the feedback path [19]. Further improvements in terms of active resistance feedback result in high disturbance rejection capability [20].

This paper analyzes the use of MS-PWM in discrete IMC based current controller, suitable for implementation on standard DSP platforms. The main goal of the paper is to demonstrate a current control structure, which offers improved dynamic response and high noise suppression compared to the state-of-the-art double update rate solutions. This is achieved without relying on expensive and complicated control platforms, but on a standard industrial DSP. The MS-PWM control strategy is analyzed for three different control loop organizations. The first one uses discrete IMC controller from [18], with a moving average filter (MAF) in the feedback. This case is found to offer slightly improved dynamics compared to standard use of double-update with the same discrete IMC (without filter in feedback) [16], [18], with significant improvement in jitter suppression. Due to added delays introduced by the MAF, the second case adds a derivative action to the controller structure, as in [18]. This case is given to demonstrate that MS-PWM can offer even better dynamics than reported in [18]. The final case implements MS-PWM based discrete IMC, without any filters in feedback. This case is expected to provide the best dynamics, using discrete IMC without derivative gain. The feedback quality is expected to worsen compared to cases with MAFs, however, it still retains higher quality compared to double-update [10]. The target is to show that with the multisampling approach delays introduced by feedback averaging can be successfully compensated, by extent determined with the multisampling factor, enabling both robust and error-free feedback acquisition and a high dynamic performance of the current loop.

This paper is organized as follows. Section II addresses discrete time machine model, controller structure and analyzes delays introduced by feedback averaging, calculation and DPWM. The multisampling PWM approach, with an outline of its merits and demerits, is explained in Section III. A DSP implementation of the multisampling algorithm is also presented. Exact controller structures and parameter setting procedures for the three aforementioned cases of interest are derived in Section IV. Effectiveness of the derived analytical model is illustrated via simulated current loop step responses and frequency response analyses. Comparison between performance of the proposed methodology and benchmark controllers is also provided. Experimental results are shown in section V. Conclusions are drawn in section VI, along with a proposal

for further studies on the presented topic.

II. MULTI-RATE CONTROL SYSTEM

A. Control system overview and AC machine modeling

Ovde imas blok dijagram sa strukturom sistema, i small-signal blok dijagram. Nakon toga imas modelovanje masine sa jednacina...

B. Motivation behind multisampling

Modern processors enable feature very high computational power, which enables short execution times for control routines. However, switching frequencies of the converter are still hardware limited, and do not go over several tens of kHz for industrial drive applications. This hardware based limitation directly affects the realizable bandwidths of the current control loop, which subsequently limits the speed and position responses as well. Therefore, using multisampled PWM control [1] seems to be a logical step forward in the high-performance drive control. Using describing function approach, small-signal model of the multisampled PWM with triangular carrier is found to be almost equal to a pure delay of $\frac{T_c}{2}$, where T_c is the modulating waveform update period. Regarding its phase response, the triangular MS-PWM can be well-approximated with the zero-order hold, which is useful for later discrete-time modeling:

$$G_{DPWM}(s) \approx \frac{1 - e^{-sT_c}}{sT_c}, \quad (1)$$

where s is the complex variable of the Laplace transform.

C. DSP algorithm for multisampled modulation

The results of this paper are obtained using a digital signal processor from Texas Instruments C2000 series, TMS320F28379D. The algorithm is referred to this DSP series, however, the algorithm nature is general and can be implemented regardless of the platform. When implementing multisampled control, the important thing is the synchronization between the main PWM carrier, which provides the output gate signal, and the multisampled carrier, which triggers the sampling and control interrupts. This is easily achievable using FPGA, however, in DSP applications additional measures need to be implemented. The main problem in DSP applications is that the PWM comparator triggers the switching action when the modulating waveform is equal to the carrier. In multisampled systems, this is not acceptable as vertical crossings between the modulating waveform and the carrier would cause pulse skipping [2]. In this subsection, an algorithm is proposed to be used in DSPs for multisampling applications. The algorithm is of general nature, and can be used for DC-DC converters as well [compel]. The description below is written for one modulating waveform, which is simply extended when using three-phase modulation.

One PWM module that runs on frequency $f_c = Nf_{pwm}$ is used for each inverter leg. This carrier triggers the ADC module to perform sampling and subsequently trigger the interrupt routine. The oversampling factor N is limited by

the code execution time and T_{pwm} . As for the carrier c that dictates the PWM frequency, it exists only virtually, and its values at the beginning and end of each interrupt is calculated by keeping track of the interrupt number. Due to considerable relative time for code execution, modulating waveform update features one step delay compared. Due to favourable characteristics for the MS-PWM control, triangular counter is used for the virtual carrier c . For oversampled carrier, trailing-edge counter is implemented, as this counter has no impact on the converter dynamics.

The controller output, $m[k]$, is used to determine whether the switching action should occur during the following period of the oversampled carrier. This is done by first transforming $m[k]$ to the value of the compare register, relative to the maximal value of the virtual carrier c_{max} . The switching actions are determined using two compare registers, $CMPA$ and $CMPB$. The true value of compare action $c = CMPA$ causes turn-on, and $c = CMPB$ causes turn-off of the referent transistor. During the up-count of the virtual carrier c , only the turn-off action is allowed, in order to prevent multiple switching. Hence, value of $CMPA$ is set to be higher than the maximum value of the oversampled carrier. Vice versa, the value of $CMPB$ is set to be higher than the maximum value of the oversampled carrier during the down-count of the virtual carrier. The value of $CMPA$ and $CMPB$, during respective count-modes, is calculated by keeping track of the interrupt number, relative to the virtual carrier. If the switching action has not yet occurred, the value of $CMPA$ or $CMPB$ will be higher than the maximal value of the oversampled carrier. Once the switching action occurs,

so, value of the compare register is calculated so that the switching action of the PWM module operating at f_c occurs exactly at the instant where it would occur for the virtual PWM carrier. For cases when the vertical crossing occurs, value of the compare register is set to be loaded to minimal possible value at the beginning of the following interrupt, so that the switching action would coincide with that interrupt instant. Note that this value might not be equal to 0, as it takes some time for the shadow compare register to be loaded to the active register. If 0 was used, the condition $c = CMP$ might not be satisfied, and the switching action would skip that interrupt period. Heuristically, this value is set to be equal to 7 in the implemented code. For the clarity of illustrations, this limit value is shown as equal to 0.

An example for $c_{max} = 8$ and $N = 4$ is given in Fig...

III. CONTROLLER AND FEEDBACK FILTER DESIGN

A. Discrete IMC controller

B. Feedback acquisition and $\alpha\beta - dq$ transformation

Ovde onaj blok dijagram od ruzice lep sa transformacijama, pa da se objasni da zapravo koristis i DMA i bla bla Prethodno negde na pocetku rada prikazi multi-rate sliku i tu ubaci blok koji se zove feedback acquisition, ulaz su alpha beta struje i ugao, izlaz su dq struje, pa iza toga ide filter u dq sistemu...

Ovde mozes da kazes: da bi stao ceo kod, ipak ne moze preveliki oversampling faktor. Zbog toga, umesto koriscenja

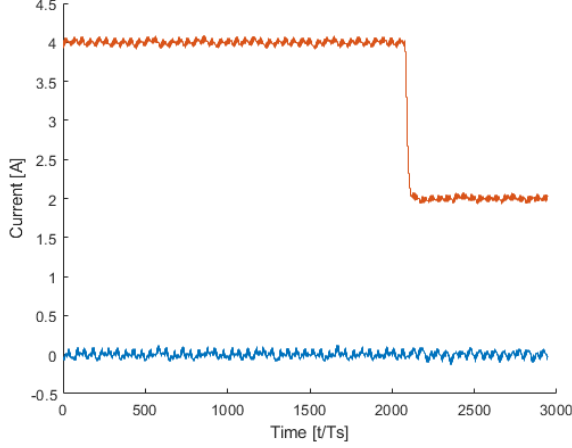


Fig. 1: Multisampled control loop of a buck converter.

klasicnog koda kao u subsection koji vec, koristi se DMA modul koji sempluje jos n puta brze tako da je ukupan oversampling rate jednak $n \cdot N$. Nakon tih n odbiraka se zapravo trigeruje interrupt koji je povezan sa N oversamplingom uradi se MAF i decimira se tako da kontrolni kod radi na f_c ucestanosti.

Depending on the algorithm complexity, $N_{max} \approx 8$ for 20 kHz PWM. Since this number cannot be too high, DMA module of the DSP can be used for higher oversampling action that is motivated by noise attenuation and error-free feedback acquisition [1]. This is performed by triggering sampling each $f_s = n f_c$ and storing results in an DMA array. After n samples are ready, interrupt flag is raised

Znaci razdvoj ucestanosti: fpwm - switching f_s - sampling (f_c - control frequency ($N f_{pwm}$))

C. Digital filter design

D. Total time delay in DSP application

Ovde pricaj o zbirnom kasnjenju, itd.... Mozda nakon price o modelovanju masine...

E. Multisampled control stage of a buck converter

IV. SIMULATION RESULTS

V. EXPERIMENTAL VERIFICATION

VI. CONCLUSION

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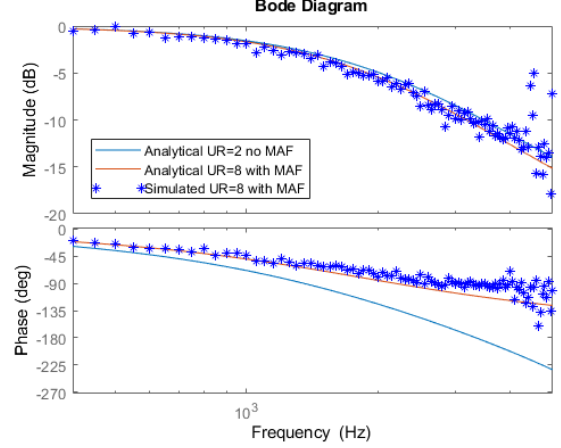


Fig. 2: Modulating signal $m_h(t)$ and carrier $w(t)$ with a) counter-phase and b) in-phase operation.

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